1 Features

- Light to Digital Converter Integrated Circuit for SteamVR™ Tracking
- High performance, 3rd generation design
- 50% lower active power than TS4231
- Deep Sleep mode
- Compatible with all versions of SteamVR™
- Convert infrared light pulses to digital envelope pulses used to track position.
- Convert infrared light pulses to digital pulses that follow the optical carrier.
- 1MHz to 10MHz optical carrier frequencies
- 50Hz/60Hz ambient noise rejection
- Two-wire control bus shares E/D pins
    - Sleep command
    - Configuration
- DVDD: 3.3V
- Small package size simplifies industrial design of tracked objects
    - 9 Bump WLCSP Package
    - 1.2mm x 1.2mm

2 Applications

- SteamVR Tracking Applications
- Room-scale Virtual Reality Tracking
- Virtual Reality Controllers
- Tracking of Physical Objects in VR
- Adding SteamVR Tracking to VR Head Mounted Displays

3 Description

Triad Semiconductor's TS4631 enables cost effective deployment of Valve Corporation's SteamVR Tracking System. Working with a photodiode, the TS4631 converts infrared light pulses into position-indicating digital envelope signals. The device also includes a digital output data pin that is a representation of the optical carrier waveform applied to the photodiode. The TS4631 includes circuits for photodiode biasing and provides high gain, noise filtering and envelope detection of pulsed IR light sources. The Envelope output of the TS4631 is a digital signal that tracks the envelope of the amplitude modulated (OOK or ASK) infrared light that is incident on the photodiode. The data output is a digital signal that tracks the modulated light input. The TS4631 is configured by a two-wire bus that shares the E/D pins of the device.

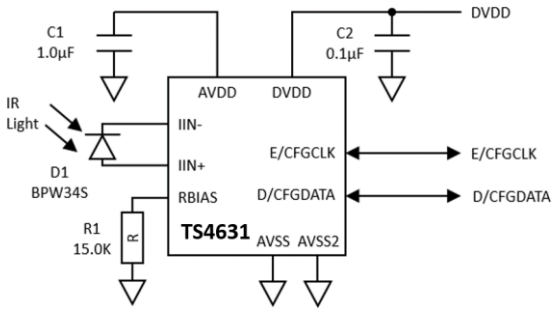
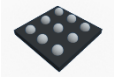


Figure 1: Simplified Application Circuit



TS4631 Device Size
1.2mm x 1.2mm

4 Device Overview

The TS4631 is a mixed-signal integrated circuit for use in optical position tracking applications. Utilizing Wafer Level Chip Scale Packaging (WLCSP), it achieves a minimal footprint size for use in space-constrained assemblies. The TS4631 provides pulse detection circuitry for use in room scale tracking/positioning for virtual reality gaming and other applications which require millimeter position accuracy. The signal path is driven from an external photodiode which is connected directly to the IIN+ and IIN- package inputs, then AC coupled to the inputs of a differential TIA. Internal bias blocks provide the necessary biasing for the photodiode. The output of the differential TIA is followed by filtering and gain blocks to limit noise before the signal drives an envelope detector and data slicer to generate the output signals. Figure 2 shows the block diagram of the TS4631. The TS4631 is available in a 9-bump WLCSP package.

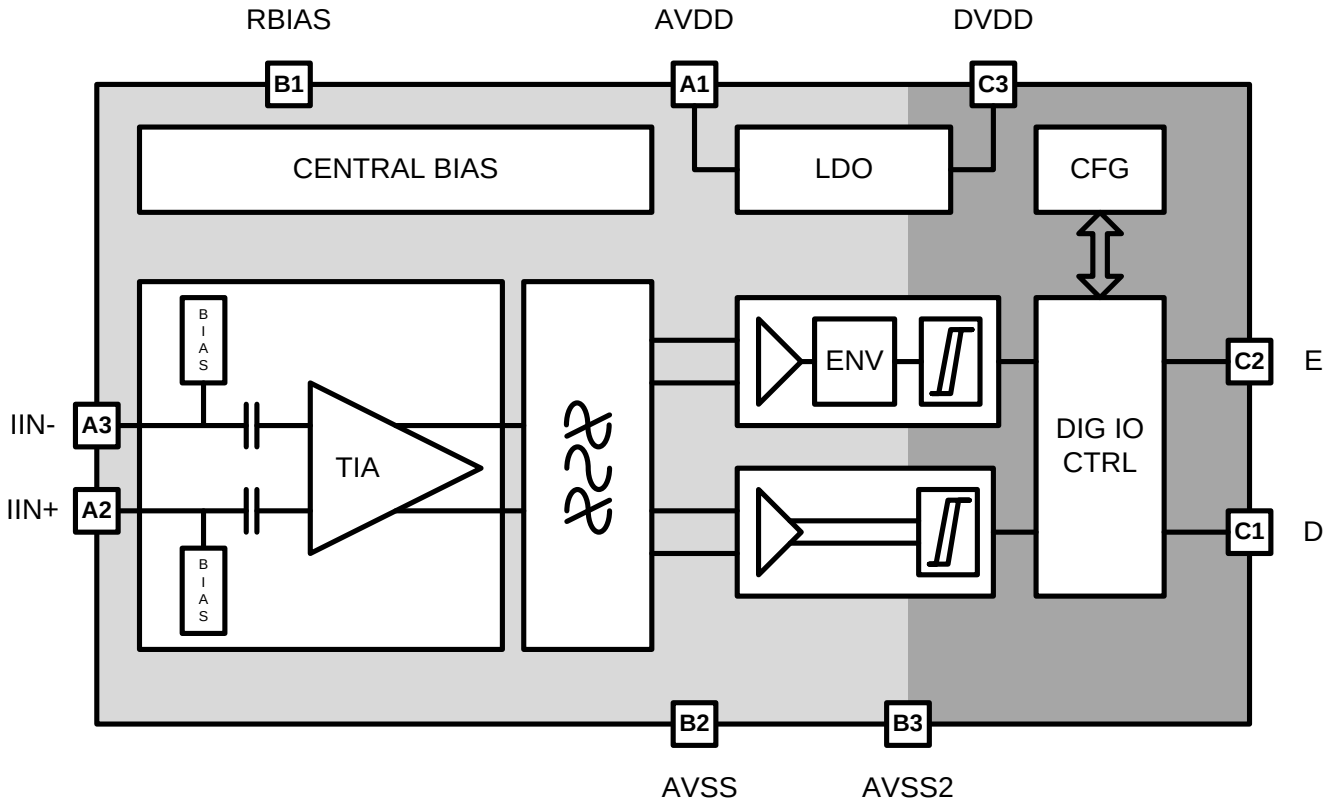


Figure 2: TS4631 Basic Block Diagram

5 Bias Circuitry

The TS4631 contains an internal reference system that controls the device's internal detection levels. An external resistor connected to the RBIAS input is used to set the internal reference. The internal reference will remain constant (within the resistor and reference tolerance) over process corners.

6 Signal Path

6.1 TIA & Filter Amplifier

The TIA is designed to amplify a differential input current pulse, created by an optical detector diode, into an output voltage pulse. A detector diode input load of 30 pF is expected for nominal operation. Detector sensitivity will vary with diode input load and can also be affected by stray capacitance due to PCB layout at the IIN+, IIN- and RBIAS inputs. The Filter Amplifier is implemented using successive band limiting gain stages.

6.2 Envelope and Data Detectors

The envelope detector is triggered by an amplified and filtered signal crossing a configured threshold. The Envelope output is asserted during detection of light pulses incident on the external photodiode. The data detector is implemented using a comparator with controlled hysteresis. The Data pin low time is qualified with an internal one-shot and is forced to return low if the low duration exceeds a 600-900ns timeout. See Figure 3.

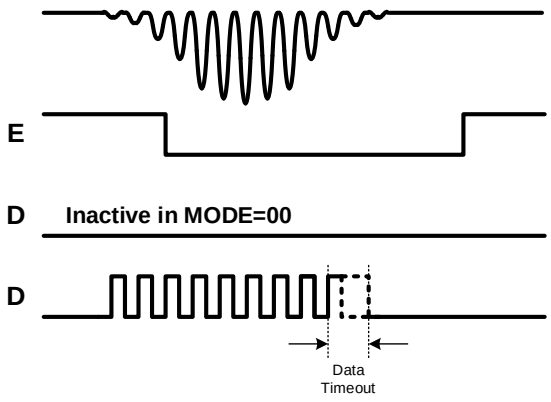


Figure 3: Output Waveforms for Modulated IR light with Gaussian Envelope

7 Digital Control Interface

7.1 Configuration and Operating Modes

The TS4631 provides a digital control interface on its E and D pins that can be used to set operating modes and access the device's internal register set for configuration (refer to Figure 4 and Table 1). After device power on, the SteamVR Tracking HDK communicates with the TS4631 over the E and D pins to configure the device (see Figure 5). Waiting for initial IR light detection is not required for TS4631. After being configured, the device will be in normal Watch mode looking for modulated IR light. When the device's photodiode is exposed to modulated IR light within the frequency range of the device, the envelope output is asserted on the E pin and the carrier data is output on the D pin, if enabled. Additionally, the same interface pins can be used to quickly put the device to sleep or wake it up.

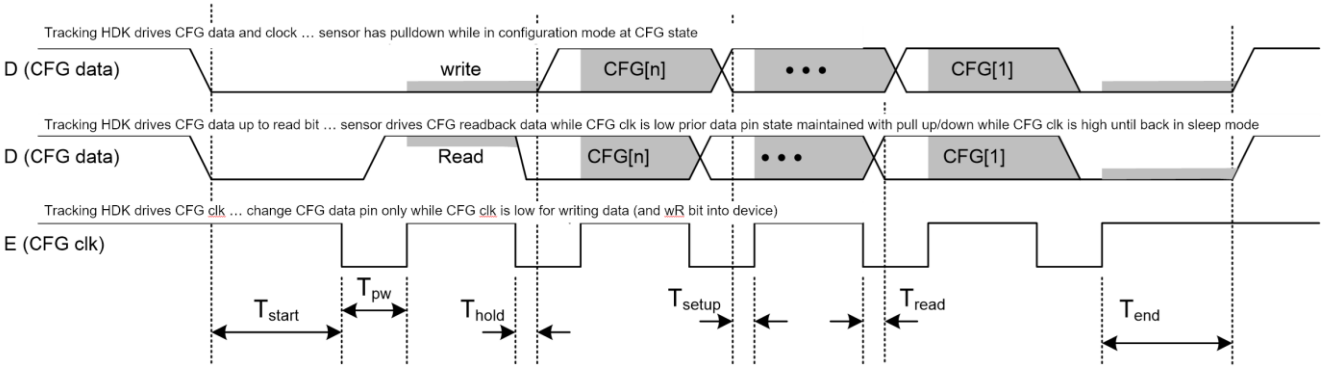


Figure 4: Configuration Timing

Register Bit Name	Register Bit	Description (settings are binary)
TIA_G40k	14	TIA gain control 00: ~95 dB (default) 01: ~83dB 10: ~89 dB 11: reserved
TIA_G20k	13	
BW_VS_IDD_1	12	TIA BW control (~0.5mA steps in overall IDD) 00: lower BW and current 01: (default) 10: higher BW and current 11: reserved
BW_VS_IDD_0	11	
D_G	10	Data gain control 1 = high gain, 0 = low gain (default)
DSLICE1	9	Data slicer thresholds † controlled by internal current DACs 00: 100mV 01: 150mV (default) 10: 200mV 11: 250mV
DSLICE0	8	
E_G	7	Envelope gain control 1 = high gain, 0 = low gain (default)
ESLICE1	6	Envelope slicer thresholds controlled by internal current DACs 00: 200mV 01: 300mV (default) 10: 400mV 11: 500mV
ESLICE0	5	
TC	4	Envelope Detector Attack Time Selection 0: Fast (θ = 1/3 that of slow setting) 1: Slow (default)
NB	3	Envelope low pass filter BW setting 0: 400 kHz low pass (default) 1: 200 kHz low pass
MODE_1	2	MODE 00: Data Disabled, normal sleep behavior (default) 01: Data Enabled, normal sleep behavior 10: Data Enabled, deep sleep behavior 11: Test Mode - reserved for test
MODE_0	1	

Notes: † Program Data Slicer threshold and D_G to ensure RTZ data (idle low) when no light is present

Table 1: TS4631 Control Register Set

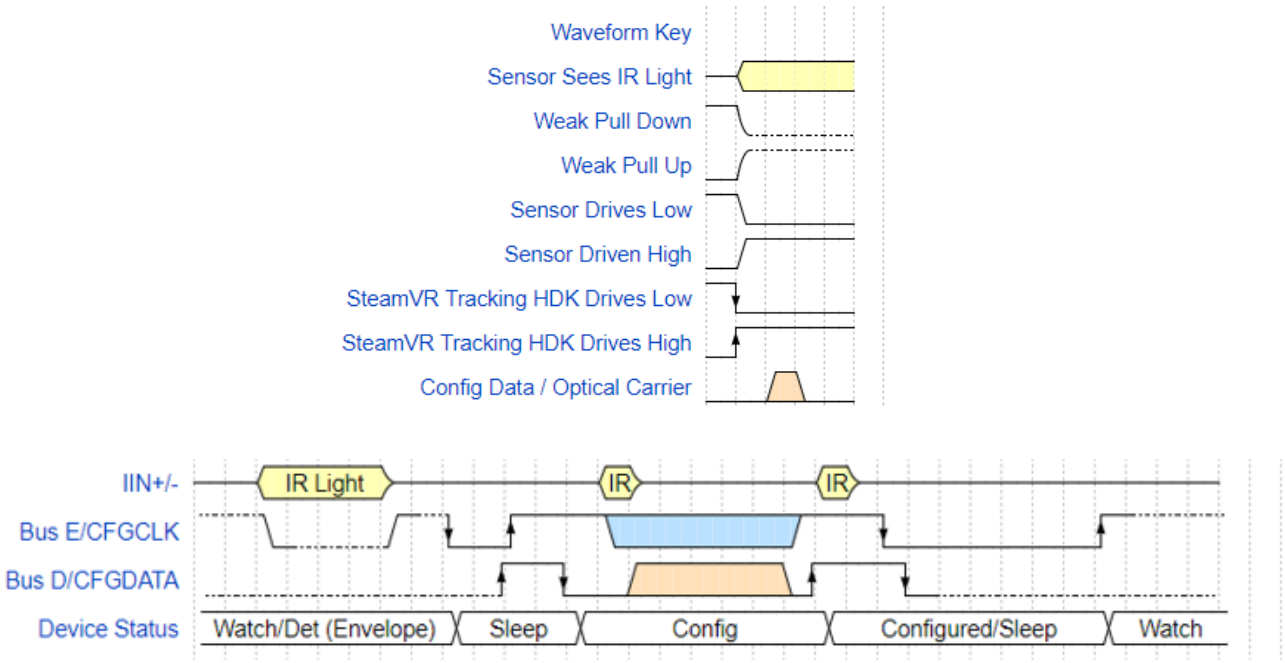


Figure 5: TS4631 powers up Un-configured then the SteamVR Tracking HDK configures the device.

7.2 Sleep & Deep Sleep Mode

While in Watch mode, the Tracking HDK may put the TS4631 into Sleep mode or Deep Sleep mode, if enabled, by driving the E and/or D pins as shown in Figure 6 and Figure 7. To return to Watch mode, the Tracking HDK will drive the E and/or D pins again.

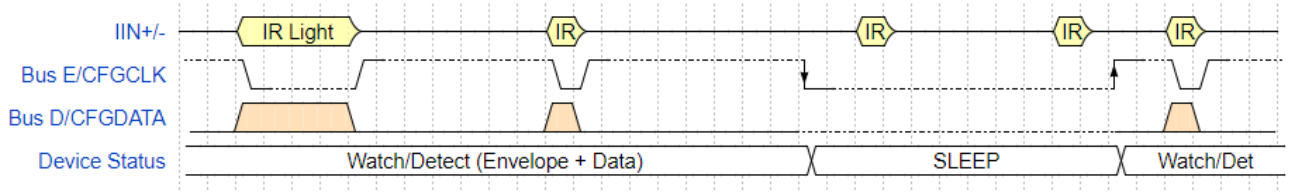


Figure 6: Sleep Timing

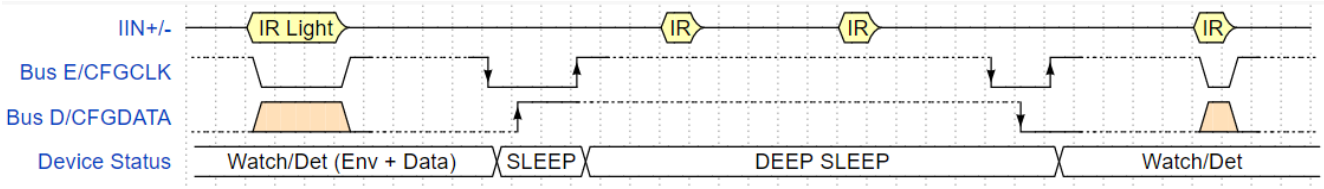


Figure 7: Deep Sleep Timing

7.3 Enabling Deep Sleep Mode

In addition to Sleep mode, TS4631 also supports a Deep Sleep mode. Deep Sleep mode has a significantly lower power consumption but requires additional time to transition from Deep Sleep to the Watch/Detect state. The specifications for Sleep and Deep Sleep performance are listed in Section Electrical Characteristics. The example configuration words listed in Section Configuration Words describe how to configure TS4631 to use Sleep or Deep Sleep mode.

7.4 Configuration Words

The following table shows 2 example configuration words for TS4631. These 14-bit configurations can be written to the device as described in Section Configuration and Operating Modes.

Configuration Word	Mode
0x0499	Envelope and Data Enabled with Sleep Mode (Faster Wake up)
0x049A	Envelope and Data Enabled with Deep Sleep Mode (Lower Current)

8 Performance Characteristics

8.1 Absolute Maximum Ratings

Parameter (1)(2)	Notes/Conditions	MIN	MAX	units
DVDD			3.6	V
Digital Input Voltage		-0.3	3.6	V
Junction Temperature T_{JMAX}	Maximum junction temperature		150	°C
Storage Temperature, T_{STOR}	Storage temperature range	-40	150	°C
Soldering Information: infrared or convection (30 sec)	Peak body temperature (reflow)		260	°C

(1) All Voltages are specified with respect to GND = 0Vdc

(2) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

Parameter	Notes/Conditions	MIN	TYP	MAX	units
DVDD	Supply voltage	3.0	3.3	3.6	V
T_{AMB} (1)	Operating temperature range	0		85	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)} - T_{AMB}$)/ θ_{JA}. All numbers apply for packages soldered directly onto a PC Board

8.3 Thermal Information

Parameter	Thermal Metric	9 Ball WLCSP	units
$R\theta_{JA}$	Junction-to-ambient thermal resistance	60	°C/W

8.4 Electrical Characteristics

Operating conditions: DVDD = 3.3V, T_{AMB} = 25 °C unless otherwise noted (1).

Parameter	Notes/Conditions		MIN (2)	TYP (3)	MAX (2)	units
Power Supply						
I_{VDD}	Operating current			2.5	3.5	mA
Sleep_I_{VDD}	Sleep mode current			0.5	0.7	mA
Deep Sleep_I_{VDD}	Deep Sleep mode current				0.15	mA
Digital IO						
V_{IL}	Input Low Voltage				0.25 * VDD	V
V_{IH}	Input High Voltage		0.75 * VDD			V
V_{OL}	Output Low Voltage	@ 2 mA load			0.1 * VDD	V
V_{OH}	Output High Voltage	@ 2 mA load	0.9 * VDD			V
I_{PU}	Output Pullup Current		70	105	140	µA
I_{PD}	Output Pulldown Current		70	105	140	µA
Rise (2)	10/90% Output Rise Time	Slew rate limited 5-20pF load	7		36	nS
Fall	10/90% Output Fall Time	Slew rate limited 5-20pF load	7		36	nS
T_{start}			80			ns
T_{pw}			80			ns
T_{setup}			30			ns
T_{hold}			30			ns
T_{end}			80			ns
T_{read}					75	ns
System						
Freq	Input pulse frequency	HiPass – LoPass 3dB corners	1.5		10	MHz
I_{INDET}	In band detection input current level (max gain)	w/ App Schematic			1.0	µA
I_{INMAX}	In band input current level max	w/ App Schematic			100	µA
$Sleep_{RCVRY}$	Sleep Mode Recovery timing E and D outputs should be ignored during recovery time	10 – 90% on I_{VDD}			50	µS
$Sleep_{PDN}$	Sleep Mode Power Down timing	10 – 90% on I_{VDD}			50	µS
$DeepSleep_{RCVRY}$	Deep Sleep Mode Recovery timing E and D outputs should be ignored during recovery time	10 – 90% on I_{VDD}			200	µS
REJ_{50KHz}	50KHz Rejection	@ filter output	40			dB
	RBIAS pin stray capacitance				10	pF
	RBIAS resistor value	1% tolerance		15		kΩ

(1) Electrical Characteristic values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested.

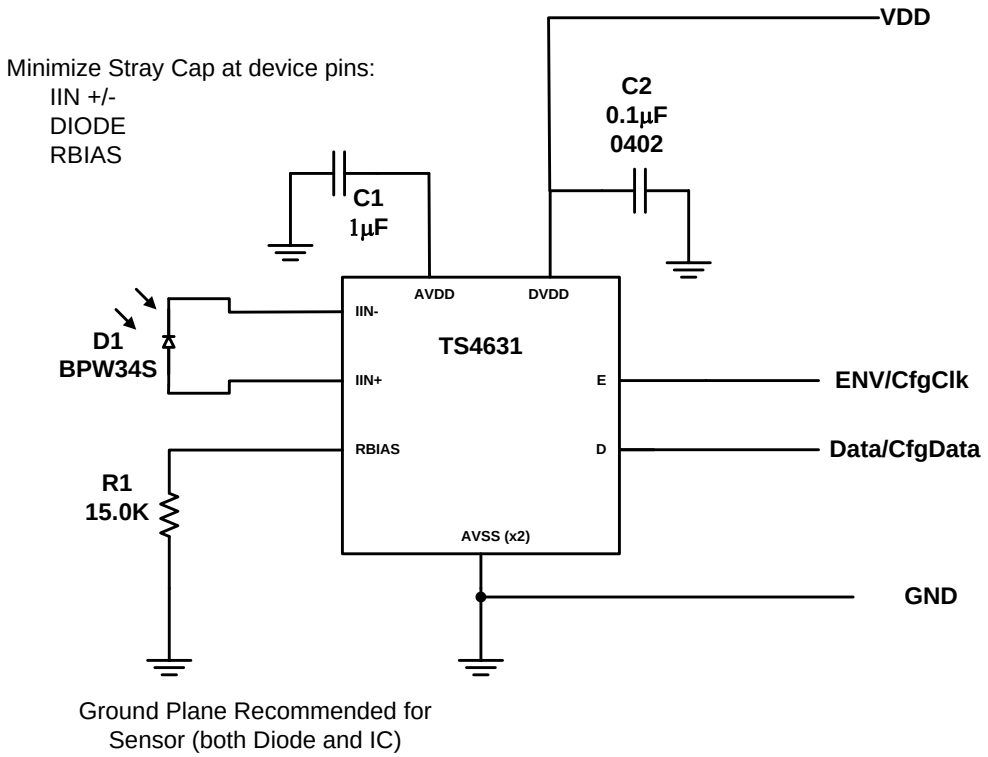
(2) Rise and Fall Times are ensured by design and not production tested.

(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.

(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

9 Applications and Design Considerations

9.1 Application Schematic (1)



(1) Minimize stray capacitance at device pins IIN+, IIN-, RBIAS, and at D1.

Figure 8: TS4631 Application Schematic

9.2 Power Supply Recommendations

The TS4631 was designed to be operated from a 3.3V power supply. The voltage range for DVDD is shown in Recommended Operating Conditions. Power supply accuracy of 10% or better is advised. The internal LDO output at the AVDD pin should be bypassed with a 1µF capacitor.

9.3 Capacitor Selection

To achieve the best performance, C1 and C2 should have low ESR / ESL, and a self-resonant frequency above the maximum input signal bandwidth. Typically, size 0402 or smaller is better for high self-resonance.

9.4 Layout Guidelines

Optimum performance can be achieved with the TS4631 by adhering to the following layout guidelines which will help minimize performance degradation due to layout parasitics and noise. The following guidelines are assuming the implementation of the application schematic shown in Figure 8.

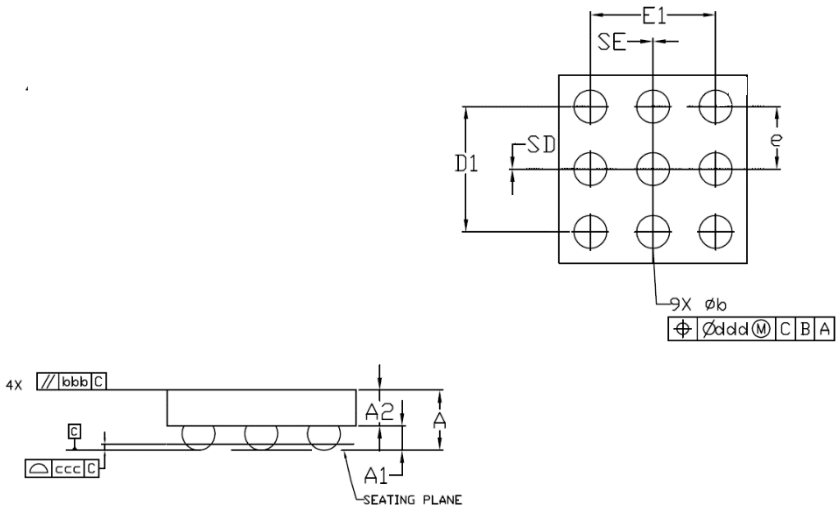
1) C1 and C2 should be placed as close as practical to their respective AVDD and DVDD package bumps.
2) Shield the IIN- and IIN+ nets with ground fills.
3) Minimize routing lengths on the IIN-, IIN+ and RBIAS nets.

4) The D and E outputs should be routed over a solid or cross hatched ground plane.

10 Part Packaging Information

10.1 Package Drawing

The TS4631 – Light to Digital Converter is packaged as a 9 bump WLCSP. Figure 9 shows the WLCSP configuration. Recommended Land Pattern is 0.200mm for each bump (per IPC 7351A guidelines).



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.465	0.515	0.565
A1	0.135	0.160	0.185
A2	0.330	0.355	0.380
D	1.155	1.170	1.185
E	1.155	1.170	1.185
D1	0.750	0.800	0.850
E1	0.750	0.800	0.850
b	0.170	0.210	0.250
e	0.400 BSC		
SD	0.000 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

Figure 9: TS4631 Outline Drawing

10.2 Date Code

The manufacturing date code is printed on the package. The date code has the format of YYWW where YY is the last 2 digits of the manufacturing year, and WW is the week of manufacture in the year.

11 Pin List

A1	AVDD	Supply	Power (bypass with 1uF)
A2	IIN+	Input	TIA Input (TS4631 internally provides bias to AVSS for photodiode Anode and has internal AC coupling cap)
A3	IIN-	Input	TIA Input (TS4631 internally provides bias to AVDD for photodiode Cathode and has internal AC coupling cap)
B1	RBIAS	Input	1% 15k Resistor for current reference
B2	AVSS	Supply	Ground (must be connected)
B3	AVSS2	Supply	Ground (connect for best performance and to access middle bump without buried/blind via in FPC or PCB landing site)
C1	D	Digital I/O	Data Output / Configuration Data I/O
C2	E	Digital I/O	Envelope Output / Configuration Clock input
C3	DVDD	Digital Supply	LDO input supply and Digital IO power (bypass with 0.1uF)

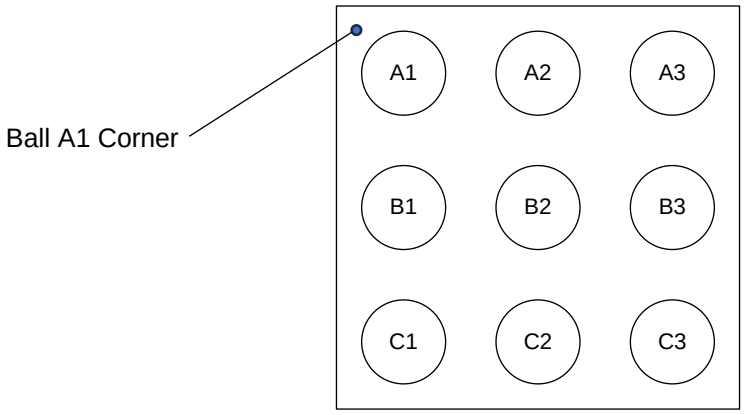


Figure 10: Top View Pin Location

12 IO Map

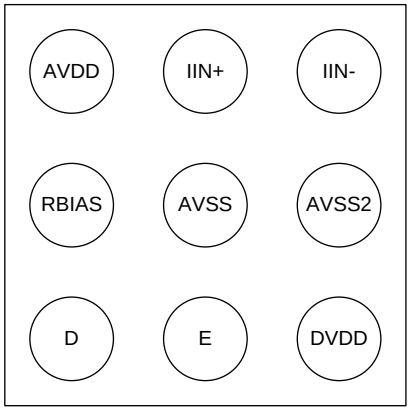
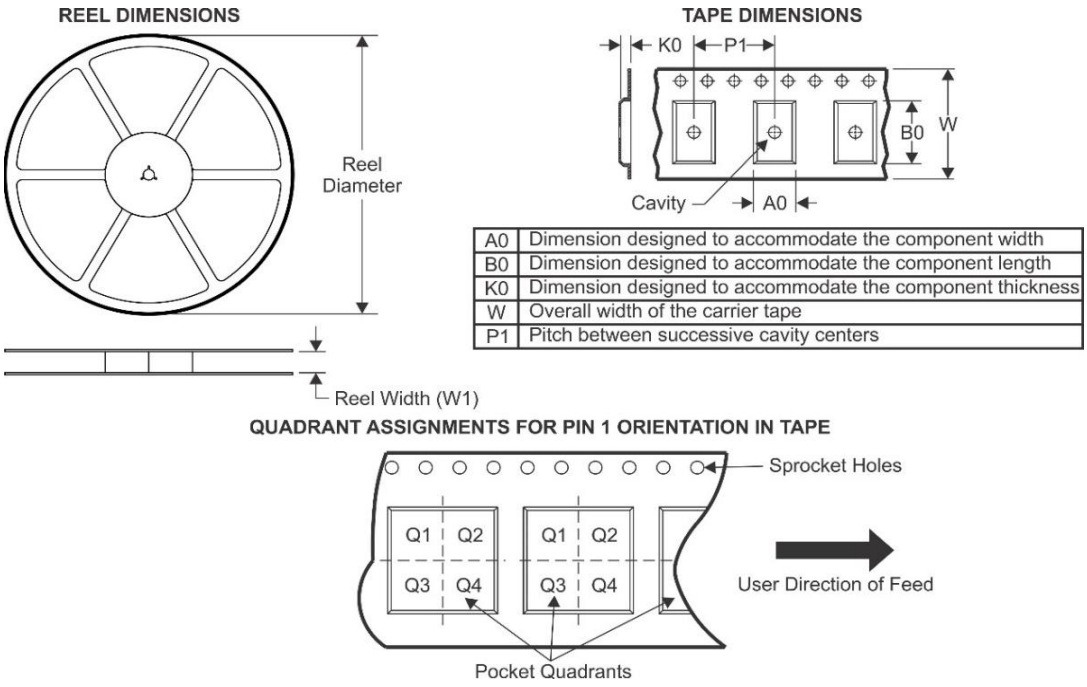


Figure 11: Top View – 3x3 Bump WLCSP IO MAP

13 Tape and Reel Packaging

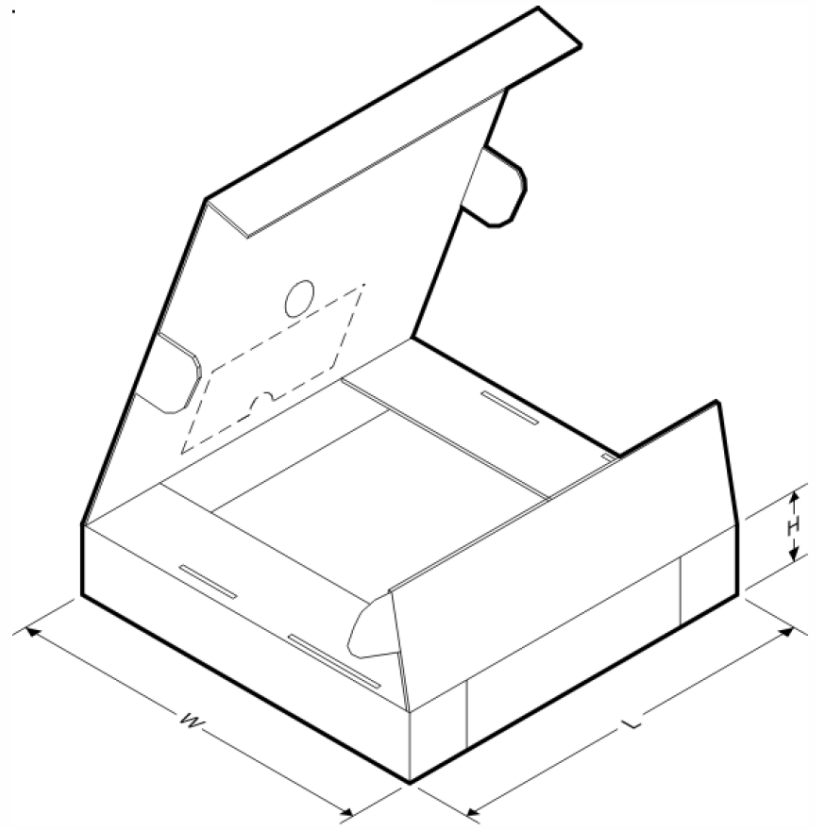
13.1 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Bumps	Qty / Reel	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
TS4631	WLCSP	9	4000	178.0	9.0	1.26	1.26	0.69	4.0	8.0	Q1

13.2 Tape and Reel Box Dimensions



Device	Package	Bumps	Qty / Reel	Length (mm)	Width (mm)	Height (mm)
TS4631	WLCSP	9	4000	215.0	200.0	40.0

Note: All dimensions are nominal

14 Mechanical, Packaging and Handling Information

Device	Package Type	Bumps	Package Qty	RoHS Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Storage Temp (°C)	Device Marking
TS4631	WLCSP	9	4000	RoHS & no Sb/Br	Cu Sn Ag	Level-1-260C-168 HR	0 to 85	-40 to 150	TS4631

14.1 Electrostatic Discharge Caution

TS4631 is an ESD sensitive device with an HBM rating of Class 2 (2,000V) per JS-001-2023. The device should be placed in conductive foam during storage or handling to prevent damage due to electrostatic discharge. Refer to JESD625 for handling precautions.

14.2 MSL

TS4631 is an MSL1 device per J-STD-020. Refer to J-STD-033 for specific handling requirements and conditions.

14.3 Shelf Life

Shelf life is 12 months as per J-STD-033. Refer to J-STD-033 for additional shelf-life information.

15 RoHS

TS4631 fully complies with the RoHS Directive 2011/65/EU requirements without exemption and is Halogen-Free as defined by IEC 61249-2-21.

Revision History

Revision	Modifications	Modification Date
A	Initial release Rev A Datasheet	17 May 2018
B	Added configuration register definitions	28 July 2022
C	Converted datasheet formatting	16 Nov 2023
D	Updated branding, added binary labels, fixed formatting	29 Nov 2023

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