TE0808 TRM

Revision v.50

Exported on 2024-09-24

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0808+TRM

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4 Overview

The Trenz Electronic TE0808 is an industrial grade MPSoC SOM integrating an AMD Zynq UltraScale+ MPSoC, DDR4 SDRAM with 64-Bit width data bus connection, SPI Boot Flash memory for configuration and operation, transceivers and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking connections in a compact 5.2 cm x 7.6 cm form factor.

Refer to http://trenz.org/te0808-info for the current online version of this manual and other available documentation.

4.1 Key Features

- **SoC**
  - Device: ZU6 / ZU9 / ZU15 [1) 2)]
  - Engine: CG / EG [1)]
  - Speedgrade: -1 / -2 [1)]
  - Temperature Range: Extended / Industrial [1)]
  - Package: FFVC900
- **RAM/Storage**
  - 4 GByte DDR4 SDRAM [3)]
  - 2 x 64 MByte Serial Flash [4)]
  - EEPROM with MAC address
- **On Board**
  - Oscillator
- **Interface**
  - 4 x B2B Connector (ST5)
    - up to 204 PL IO
      - HP: 156
      - HD: 48
    - up to 65 PS MIO
    - 4 GTR
    - 16 GTH
    - I2C, JTAG, CONFIG
- **Power**
  - 3.3 V power supply via B2B Connector needed [5)].
- **Dimension**
  - 76 mm x 52 mm
- **Notes**

  [1)] Please, take care of the possible assembly options. Furthermore, check whether the power supply is powerful enough for your FPGA design.

  [2)] without PCIe Core on PL, see XMP104

  [3)] Up to 8 GByte are possible with a maximum bandwidth of 2400 MBit/s.

  [4)] Please, take care of the possible assembly options.

  [5)] Dependent on the assembly option a higher input voltage may be possible

4.2 Block Diagram

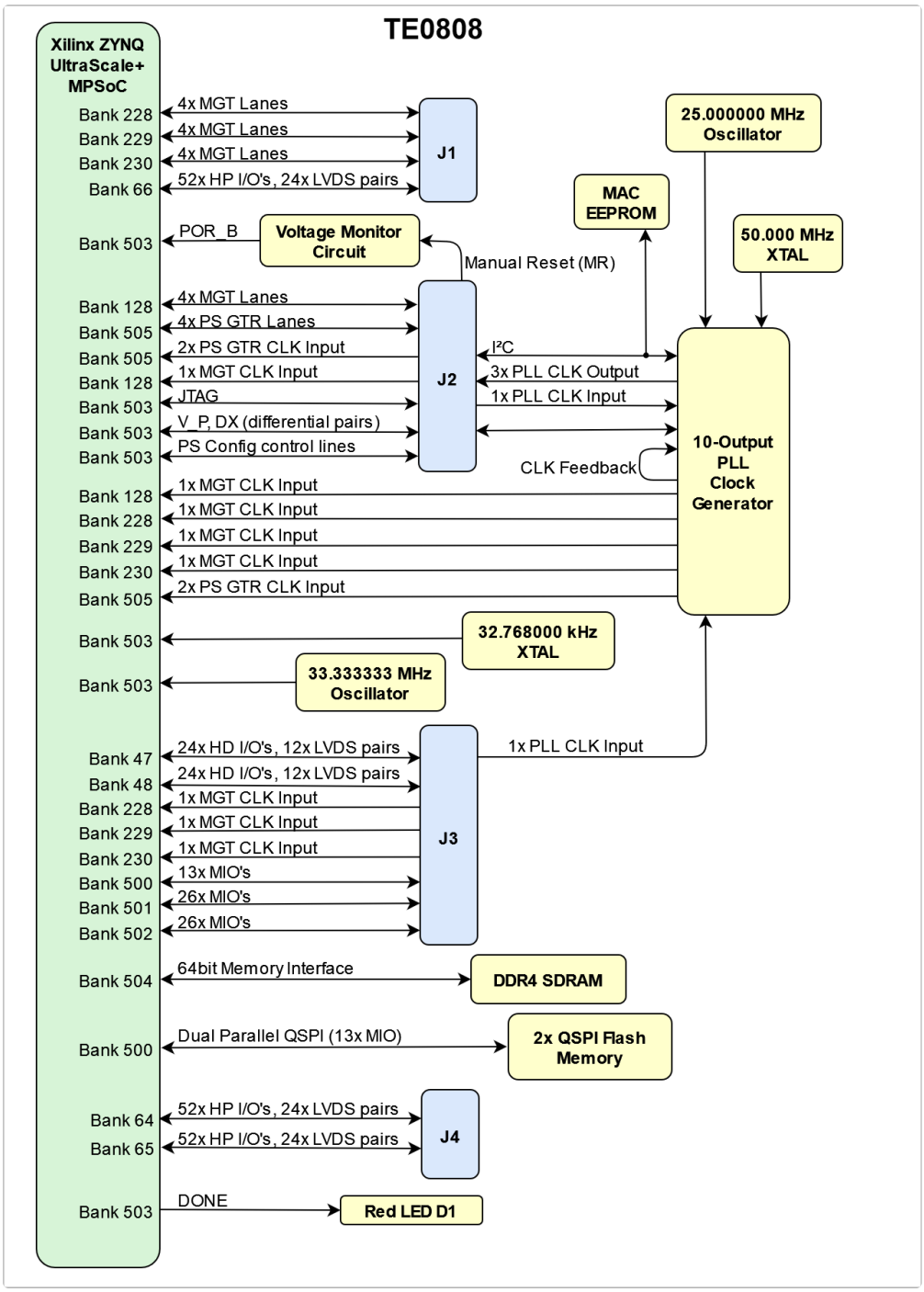

Figure 1: TE0808 block diagram

4.3 Main Components

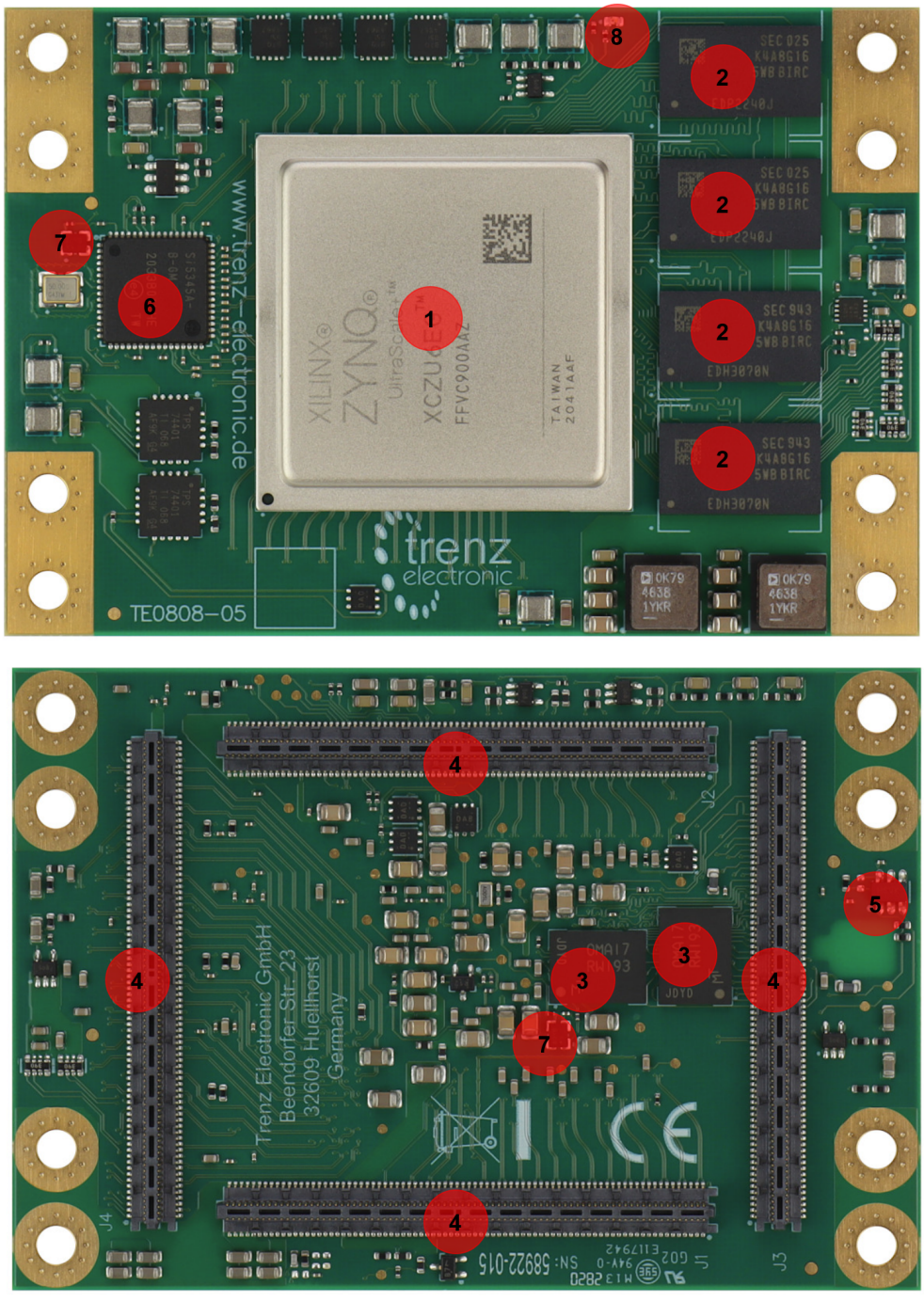

Figure 2: TE0808 main components

1. SoC, U1
2. DDR4, U2, U3, U9, U12
3. Quad SPI Flash, U7, U17
4. Connector, J1, J2, J3, J4
5. EEPROM, U4
6. Clock Generator, U5
7. Oscillator, U25, U32
8. Done LED D1

4.4 Initial Delivery State

Storage device name	Content	Notes
DDR4 SDRAM	not programmed	
Quad SPI Flash	not programmed	
EEPROM	not programmed besides factory programmed MAC address	
Programmable Clock Generator	not programmed	

Table 1: Initial delivery state of programmable devices on the module

5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO CNT	Notes
B2B	JM1	MGT PL	12 x MGT (RX/TX)	
B2B	JM1	HP	52 SE / 24 DIFF	
B2B	JM2	MGT PS	2 x MGT CLK	
B2B	JM2	CLK	4 x DIFF CLK	PLL
B2B	JM2	MGT PL	4 x MGT (RX/TX)	
B2B	JM2	MGT PS	4 x MGT (RX/TX)	
B2B	JM2	CFG[1)]	1 x JTAG	
B2B	JM2	CFG[1)]	4 x MODE	
B2B	JM2	CFG[1)]	1 x I2C	PLL, EEPROM
B2B	JM2	CFG[1)]	34 CTRL/Status	
B2B	JM3	HD	48 SE / 24 DIFF	
B2B	JM3	MGT PL	3 x MGT CLK	
B2B	JM3	CLK	DIFF CLK	PLL
B2B	JM3	MIO	65 PS GPIO	
B2B	JM4	HP	104 SE / 48 DIFF	

Table 2: Board Connectors

[1)] see Configuration and System Control Signals (see page 13)

5.2 Test Points

Test Point	Signal	Notes
TP1	PLL_SCL	pulled-up to PS_1V8
TP2	PLL_SDA	pulled-up to PS_1V8
TP3	LP_DCDC	
TP4	DCDCIN	
TP5	GND	
TP6	TCK	
TP7	PL_DCIN	
TP8	GND	
TP9	GT_DCDC	
TP10	GND	
TP11	TDI	
TP12	TDO	
TP13	TMS	
TP14	PS_1V8	
TP15	No Net Name	REF3312AIDCKT (U33) ouput voltage
TP16	FP_0V85	
TP17	DDR_2V5	
TP18	DDR_PLL	

Test Point	Signal	Notes
TP19	PL_VCCINT	
TP20	AUX_R	
TP21	AVTT_R	
TP22	AUX_L	
TP24	AVCC_R	
TP26	AVTT_L	
TP28	AVCC_L	
TP30	PS_PLL	
TP31	PS_AVTT	
TP32	LP_0V85	
TP33	PS_AUX	
TP34	PS_AVCC	
TP36	POR_B	pulled-up to PS_1V8

Table 3: Test Points Information

6 On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
DDR4 SDRAM	U2, U3, U9, U12	SoC - PS	
Quad SPI Flash	U7, U17	SoC - PS	Booting.
EEPROM	U4	B2B - J2	
Clock Generator	U5	B2B - J2 SoC, - MGT	
Oscillator	U25	Clock Generator	25 MHz
Oscillator	U32	SoC - PS	33.333333 MHz

Table 4: On board peripherals

7 Configuration and System Control Signals

Connector+Pin	Signal Name	Direction[1)]	Description
JM2-77	EN_PLL_PWR	IN	Enable PLL power supply.
JM2-79	EN_GT_L	IN	Enable left GTH transceiver power-up.
JM2-80	PG_PLL_1V8	OUT	SI_PLL_1V8 power rail powered-up.
JM2-81	PLL_FINC	IN	PLL Frequency incrementation.
JM2-82	PG_PSGT	OUT	GTR transceivers powered-up.
JM2-83	MR	IN	Manual reset.
JM2-84	EN_PSGT	IN	Enable GTR transceiver power-up.
JM2-85	PLL_LOLn	OUT	Loss of lock status.
JM2-86	ERR_STATUS	OUT	PS error status [2)].
JM2-87	PLL_SEL1	IN	PLL clock selection.
JM2-88	ERR_OUT	OUT	PS error indication [2)].
JM2-89	PLL_RST	IN	PLL reset.
JM2-90	PLL_SCL	IN	I2C clock. Pulled up to PS_1V8.
JM2-91	PG_GT_R	OUT	Right GTH Transceivers powered-up.
JM2-92	PLL_SDA	IN/OUT	I2C data. Pulled up to PS_1V8.

Connector+Pin	Signal Name	Direction[1)]	Description
JM2-93	PLL_SEL0	IN	PLL clock selection.
JM2-94	PLL_FDEC	IN	PLL Frequency decrementation.
JM2-95	EN_GT_R	IN	Enable right GTH transceiver power-up.
JM2-96	SRST_B	IN	System reset [2)]. Pulled-up to PS_1V8.
JM2-97	PG_GT_L	OUT	Left GTH Transceivers powered-up.
JM2-98	INIT_B	IN/ OUT	Initialization completion indicator after POR [2)]. Pulled-up to PS_1V8.
JM2-100	PROG_B	IN/ OUT	Power-on reset [2)]. Pulled-up to PS_1V8.
JM2-101	EN_PL	IN	Enable programable logic power-up.
JM2-102	EN_FPD	IN	Enable full-power domain power-up.
JM2-103 / JM2-105 / JM2-107 / JM2-109	MODE3..0	IN	Boot mode selection [2)]: • JTAG • QUAD-SPI (32 Bit) • SD1 (2.0) • eMMC (1.8 V) • SD1 LS (3.0) Supported Modes depends also on used Carrier.
JM2-104	PG_PL	OUT	Programmable logic powered-up. Pulled-up to PL_DCIN.
JM2-106	LP_GOOD	OUT	Low-power domain powered-up. Pulled up to LP_DCDC.
JM2-108	EN_LPD	IN	Enable low-power domain power-up.

Connector+Pin	Signal Name	Direction[1)]	Description
JM2-110	PG_FPD	OUT	Full-power domain powered-up. Pulled-up to DCDCIN.
JM2-112	EN_DDR	IN	Enable DDR power-up.
JM2-114	PG_DDR	OUT	DDR power supply powered-up. Pulled-up to DCDCIN.
JM2-116	DONE	OUT	PS done signal [2)]. Pulled-up to PS_1V8.
JM2-119 / JM2-121	DX_P / DX_N	-	SoC temperatur sensing diode pins [2)].
JM2-120 / JM2-122 / JM2-124 / JM2-126	TCK / TDI / TDO / TMS	Signal-dependent	JTAG configuration and debugging interface. JTAG reference voltage: PS_1V8
JM2-125	PSBATT	IN	PS RTC Battery supply voltage [2) 3)].
JM2-127	PUDC_B	IN	Configuration pull-ups setting [2)]. Pulled-up to PL_1V8.

Table 5: Controller signal.

1) Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

2) See UG1085 for additional information.

3) See Recommended Operating Conditions (see page 25).

8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name/ Schematic Name	Connector + Pin	Direction[1)]	Notes
VCCO_66	JM1-90 / JM1-120	IN	
VREF_66	JM1-108	IN	
PL_1V8	JM1-91 / JM1-121	OUT	
PL_DCIN	JM1-151 / JM1-153 / JM1-155 / JM1-157 / JM1-159	IN	
LP_DCDC	JM2-138 / JM2-140 / JM2-142 / JM2-144	IN	
DCDCIN	JM2-153 / JM2-154 / JM2-155 / JM2-156 / JM2-157 / JM2-158 / JM2-159 / JM2-160	IN	
PS_1V8	JM2-99 / JM3-147 / JM3-148	OUT	
PS_BATT	JM2-125	IN	
DDR_1V2	JM2-135	OUT	
VCCO_48	JM3-15 / JM3-16	IN	
VCCO_47	JM3-43 / JM3-44	IN	
PLL_3V3	JM3-152	IN	
SI_PLL_1V8	JM3-151	OUT	

Power Rail Name/ Schematic Name	Connector + Pin	Direction[1)]	Notes
GT_DCDC	JM3-157 / JM3-158 / JM3-159 / JM3-160	IN	
VCCO_64	JM4-58 / JM4-106	IN	
VREF_64	JM4-88	IN	
VCCO_65	JM4-69 / JM4-105	IN	
VREF_65	JM4-15	IN	

Table 6: Module power rails.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

8.2 Recommended Power up Sequencing

The power up sequencing highly depends on the use case. In general, it should be possible to enable/disable the processing system (PS) / programmable logic (PL) independently. Furthermore, within the processing logic it should be possible to enable/disable only low-power domain and/or low-power and full-power domain. Additionally, usage of GTR for PS side and GTH for PL side should be possible. GTH transceivers on left and right side are usable independently. Because of this flexibility the needed parts of the following table needs to be selected individually. For detailed information take a look into schematics. **Attention: PL usage is not completely independent of PS side. For PL usage it is necessary to enable PS low-power domain.**

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
0	-	-	-	Configuration signal setup.	See Configuration and System Control Signals (see page 13).
1 [1)]	PSBATT	1.2 V ... 1.5 V	-	Battery connection.	Battery Power Domain usage. When not used, tie to GND.

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
2	Processing System (PS):			Procedure for PS starting.	
2.1	Low-power domain:			Bring-up for low-power domain PS.	
2.1.1	LP_DCDC	3.3 V (± 5 %) 2)	-	Low-power domain power supply.	Main module power supply for low-power domain. 5.5 A recommended. Power consumption depends mainly on design and cooling solution.
2.1.2	EN_LPD	-	-	Low-power domain power enable.	
2.1.3	LP_GOOD	-	PU 3), LP_DCDC	Low-power domain power good status.	Module power-on sequencing for low-power domain finished.
2.2	Full-power domain:			Bring-up for full-power domain PS.	Full-power PS domain needs powered low-power PS domain.
2.2.1	DCDCIN	3.3 V (± 5 %) 2)		Full-power domain and GTR transceiver power supply.	Main module power supply for full-power domain. 7 A recommended. Power consumption depends mainly on design and cooling solution.

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
2.2.2	EN_FPD	DCDCIN	-	Full-power domain power enable.	
2.2.3	PG_FPD	-	PU [3], DCDCIN	Full-power domain power good status.	Module power-on sequencing for full-power domain finished.
2.2.4	EN_DDR	DCDCIN	-	DDR memory power enable.	
2.2.5	PG_DDR	-	PU [3], DCDCIN	DDR memory power good status.	Module power-on sequencing for DDR memory finished.
2.3	GTR Transceiver			Procedure for GTR transceiver starting.	PS transceiver usage needs powered PS (low- and full-power domain).
2.3.1	EN_PSGT	DCDCIN	-	GTR transceiver power enable.	
2.3.2	PG_PSGT	-	-	GTR transceiver power good status.	Module power-on sequencing for GTR transceiver finished.
2	Programmable Logic (PL)			Procedure for PL starting.	PL usage needs powered PS low-power domain.
2.1	PL_DCIN	3.3 V (± 5 %) [2]	-	Programmable logic power supply.	Main module power supply for programmable logic. 12 A recommended. Power consumption depends mainly on design and cooling solution.

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
2.2	EN_PL	-	PU [3], PL_DCIN	Programmable logic power enable.	
2.3	PG_PL	-	PU [3], PL_DCIN	Programmable logic power good status.	Module power-on sequencing for programmable logic finished. Periphery and variable bank voltages can be enabled on carrier.
2.4	VCCO_47 / VCCO_48 / VCCO_64 / VCCO_65 / VCCO_66	[4]	-	Module bank voltages.	Enable bank voltages after PG_PL deassertion.
3	GTH / GTY Transceiver			Procedure for GTH / GTY transceiver starting.	PL transceiver usage needs powered PL and low-power PS domain.
3.1	GT_DCDC	3.3 V (± 5 %) [2]	-	GTH transceiver power supply.	Main module power supply for GTH transceiver. 5 A recommended. Power consumption depends mainly on design and cooling solution.
3.2[1]	EN_PLL_PWR	-	-	PLL power enable.	

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
3.2[1)]	PG_PLL_1V8	-	-	PLL power good status.	
3.2[1)]	PLL_3V3	3.3 V (± 5 %)		PLL power supply	
3.3	EN_GT_L / EN_GT_R	GT_DCDC	-	GTH / GTY left / right transceiver power enable.	Transceivers on left / right side can be used independently.
3.4	PG_GT_L / PG_GT_R	-	-	GTH / GTY transceiver power good status.	
4	MR			Manual Reset	Low active release after all needed power domains are enabled.

Table 7: Baseboard Design Hints

[1)] Optional

[2)] Dependent on the assembly option a higher input voltage may be possible.

[3)] On module

[4)] See DS925 for additional information.

9 Board to Board Connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec Razor Beam LP Terminal Strip (ST5[1]) on the bottom side.

- 4x REF-192552-02 (160-pins)
  - ST5 Mates with SS5

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec Razor Beam LP Socket Strip (SS5[2]) on the top side.

- 4x REF192552-01 (160-pins)
  - SS5 Mates with ST5

9.1 Features

- Board-to-Board Connector 160-pins, 80 contacts per row
- Ultrafine .0197" (0.50 mm) pitch
- Narrow body design saves space on board
- Lead style -03.5
- Samtec 28+ Gbps Solution
- Mates with: ST5
- Insulator Material: Liquid Crystal Polymer, schwarz
- Operating Temperature Range: -55°C bis +125°C
- Lead-Free Solderable: Yes
- RoHS Konform: Yes

9.2 Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
27219	REF192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	3.5mm	Standard connector used on carrier
27018	REF-189545-02	SS5-80-3.00-L-D-K-TR	Baseboard connector	3 mm	Assembly option on request
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	1.5 mm	Standard connector

1 https://www.samtec.com/products/st5
2 https://www.samtec.com/products/st5

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
					used on modules
27017	REF-189545-01	ST5-80-1.00-L-D-P-TR	Module connector	1 mm	Assembly option on request

Table 8: Connectors.

The module can be manufactured using other connectors upon request.

9.3 Current Rating

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

9.4 Connector Speed Ratings

The connector speed rating depends on the stacking height:

Stacking height	Speed rating
4 mm, Single-Ended	13GHz/26Gbps
4 mm, Differential	13.5GHz/27Gbps
5 mm, Single-Ended	13.5GHz/27Gbps
5 mm, Differential	20GHz/40 Gbps

Table 9: Speed rating.
The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

10 Technical Specifications

10.1 Absolute Maximum Ratings *)

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
LP_DCDC	Micromodule Power	-0.300	4.0	V
DCDCIN	Micromodule Power	-0.300	6.0	V
GT_DCDC	Micromodule Power	-0.300	6.0	V
PL_DCIN	Micromodule Power	-0.300	3.6	V
PLL_3V3	PLL power supply	-0.500	3.8	V
PS_BATT	RTC / BBRAM	-0.500	2.000	V
VCCO_47	HD IO Bank power supply	-0.500	3.400	V
VCCO_48	HD IO Bank power supply	-0.500	3.400	V
VCCO_64	HP IO Bank power supply	-0.500	2.000	V
VCCO_65	HP IO Bank power supply	-0.500	2.000	V
VCCO_66	HP IO Bank power supply	-0.500	2.000	V
VREF_64	Bank input reference voltage	-0.500	2.000	V
VREF_65	Bank input reference voltage	-0.500	2.000	V
VREF_66	Bank input reference voltage	-0.500	2.000	V

Table 10: Absolute maximum ratings

*) Stresses beyond those listed under Absolute Maximum Ratings (see page 24) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition (see page 0). Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

10.2 Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be differ depending on the assembly version. Voltage range is mostly the same during variants (exceptions are possible, depending on custom request)

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

- Variants of modules are described here: Article Number Information[3]
- Modules with commercial temperature grade are equipped with components that cover at least the range of 0°C to 75°C
- Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C
- Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C
- The actual operating temperature range will depend on the FPGA / SoC design / usage and cooling and other variables.

Parameter	Min	Max	Units	Reference Document
LP_DCDC 1)	3.135	3.465	V	
DCDCIN 1)	3.135	3.465	V	
GT_DCDC 1)	3.135	3.465	V	
PL_DCIN 1)	3.135	3.465	V	
PLL_3V3	3.14	3.465	V	
PS_BATT	1.200	1.500	V	See FPGA datasheet.
VCCO_47	1.140	3.400	V	See FPGA datasheet.
VCCO_48	1.140	3.400	V	See FPGA datasheet.
VCCO_64	0.950	1.900	V	See FPGA datasheet.

3 https://wiki.trenz-electronic.de/display/PD/Article+Number+Information

Parameter	Min	Max	Units	Reference Document
VCCO_65	0.950	1.900	V	See FPGA datasheet.
VCCO_66	0.950	1.900	V	See FPGA datasheet.
VREF_64	0.6	1.2	V	See FPGA datasheet.
VREF_65	0.6	1.2	V	See FPGA datasheet.
VREF_66	0.6	1.2	V	See FPGA datasheet.

Table 11: Recommended operating conditions.

[1)] Higher values may possible. For more information consult schematic and according datasheets.

10.3 Physical Dimensions

- Module size: 76 mm × 52 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.

PCB thickness: 1.6 mm (± 10 %).

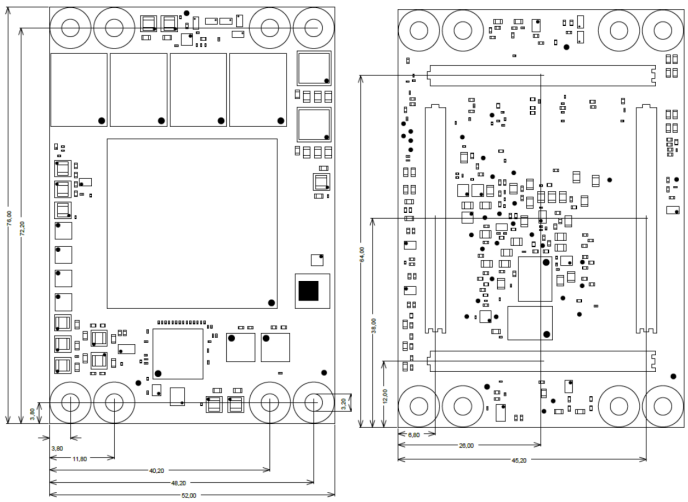

Figure 3: Physical Dimension

11 Currently Offered Variants

Trenz shop TE0808 overview page	
English page[4]	German page[5]

Table 12: Trenz Electronic Shop Overview

4 https://shop.trenz-electronic.de/en/search?sSearch=TE0808
5 https://shop.trenz-electronic.de/de/search?sSearch=TE0808

12 Revision History

12.1 Hardware Revision History

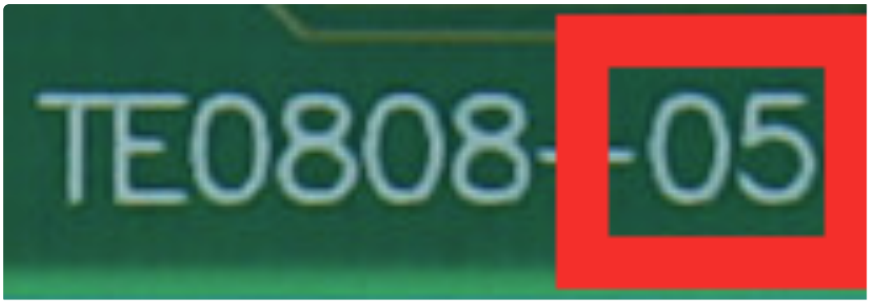

Figure 4: Board hardware revision number.

Date	Revision	Changes	Documentation Link
-	05	Second production silicon: • revised PL_VCCINT power supply. PCB: revised routing and components placement; • added signal BG1 for DDP DDR4 IC. Added support of new packages. PCB: revised routing and components placement; • R5 pulled up to 1.2V. R5 value changed to 49.9R; • added test points; • added MAC EEPROM U48. I2C bus PLL_SCL/SDA. Added pull up resistor to I2C bus; • PCB - revised FPGA location. Package placed 1.5mm closer to connector J3; • PCB - updated silckscreen. Added company address, CE and WEEE symbols; • PCB - updated signal trace lengths. • (29.11.2022) Changed note near J2.97 and net PG_GT_L from "On board pull-up R" to "External pull-up R Required"	TE0808-05[6]
-	04	First production silicon:	TE0808-04[7]

6 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0808/REV05
7 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0808/REV04

Date	Revision	Changes	Documentation Link
		• Added resistors R65,R82,R86,R87 (240R) for each DDR4-chip for supporting DDP DDR4 chips • Full library update • (09.06.2020) R19 value was changed to 10K (was: 4K99) to set PS_MGTRAVCC 0.85V	
-	03	Second ES production release	TE0808-03[8]
2016-03-09	02	First ES production release	TE0808-02[9]
-	01	Prototypes	-

Table 13: Hardware Revision History
Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

12.2 Document Change History

Date	Revision	Contributors	Description
2024-09-24	v.50 (see page 5)	John Hartfiel[10]	• change default RAM size on key feature section • typo and revision history update
2024-09-18	v.48	John Hartfiel	• Review and Public Update
2023-10-13	v.44	ED	• Updated to new TRM style

8 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0808/REV03
9 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0808/REV02
10 https://wiki.trenz-electronic.de/display/~j.hartfiel

Date	Revision	Contributors	Description
2022-09-13	v.41	Vadim Yunitski	• Updated PG_PL pull-up resistor requirements
2021-09-07	V.39	John Hartfiel	• Correction Power section
2021-05-17	v.37	John Hartfiel	• typo correction in DDR section
2021-03-11	v.35	Antti Lukats	• typo correction in PLL_RST • add pin on power rails table • correction MGT Lane assignment • correction MGT CLK assignment
2019-01-27	v.30	Martin Rohrmüller	• Corrected clock connection to J2
2018-11-20	v.29	John Hartfiel	• Notes for power supply
2018-08-27	v.27	John Hartfiel	• typo correction SI5345 I2C address
2028-06-28	v.26	John Hartfiel	• typo SI5348 B2B IOs + link correction
2017-11-13	v.24	Ali Naseri	• updated B2B connector max. current rating per pin
2017-11-13	v.22	John Hartfiel	• rework B2B section
2017-10-20	v.21	Ali Naseri	• Update links (pdf, documentation) to revision 4 • ES silicon note removed
2017-08-28	v.15	John Hartfiel	• Update section: Variants Currently In Production
2017-08-28	v.14	Jan Kumann	• Block diagram changed. • SPI flash section fixed. • Few smaller improvements.

Date	Revision	Contributors	Description
2017-08-15	v.12	Vitali Tsiukala	Changed signals count in the B2B connectors table
2017-08-15	v.11	John Hartfiel, Ali Naseri	• PCB REV04 Initial release • update boot mode section
2017-02-06	v.1	Jan Kumann	Initial document
--	all	Vitali Tsiukala[11], Antonio Luppi[12], Ali Naseri[13], Antti Lukats[14], John Hartfiel[15], Jan Kumann[16], Martin Rohrmüller[17], Thorsten Trenz[18], Vadim Yunitski[19]	• --

Table 14: Document change history.

11 https://wiki.trenz-electronic.de/display/~Vitali.Tsiukala
12 https://wiki.trenz-electronic.de/display/~a.luppi
13 https://wiki.trenz-electronic.de/display/~a.naseri
14 https://wiki.trenz-electronic.de/display/~antti.lukats
15 https://wiki.trenz-electronic.de/display/~j.hartfiel
16 https://wiki.trenz-electronic.de/display/~j.kumann
17 https://wiki.trenz-electronic.de/display/~m.rohrmueller
18 https://wiki.trenz-electronic.de/display/~tht
19 https://wiki.trenz-electronic.de/display/~v.yunitzki

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2019-06-07

20 http://guidance.echa.europa.eu/
21 https://echa.europa.eu/candidate-list-table
22 http://www.echa.europa.eu/