

## AM68x Processors, Silicon Revision 1.0

### 1 Features

#### Processor cores:

- Up to dual 64-bit Arm® Cortex®-A72 microprocessor subsystem at up to 2GHz
  - 1MB shared L2 cache per dual-core Cortex®-A72 cluster
  - 32KB L1 D-Cache and 48KB L1 I-Cache per Cortex®-A72 core
- Deep Learning Accelerator:
  - Up to 8 Trillion Operations Per Second (TOPS)
- Vision Processing Accelerators (VPAC) with Image Signal Processor (ISP) and multiple vision assist accelerators
- Dual-core Arm® Cortex®-R5F MCUs at up to 1.0GHz in General Compute partition with FFI
  - 16KB L1 D-Cache, 16KB L1 I-Cache, and 64KB L2 TCM
- Dual-core Arm® Cortex®-R5F MCUs at up to 1.0 GHz to support Device Management
  - 32K L1 D-Cache, 32K I-Cache, and 64K L2 TCM with SECEDED ECC on all memories
- Vision Processing Accelerators (VPAC) with Image Signal Processor (ISP) and multiple vision assist accelerators
  - 480 MPixel/s ISP
  - Support for up to 16-bit input RAW format
  - Wide Dynamic Range (WDR), Lens Distortion Correction (LDC), Vision Imaging Subsystem (VISS), and Multi-Scalar (MSC) support
  - Output color format : 8-bits, 12-bits, and YUV 4:2:2, YUV 4:2:0, RGB, HSV/HSL

#### Multimedia:

- Display subsystem supports:
  - Up to 4 displays
  - Up to two DSI 4L TX (up to 2.5K)
  - One eDP 4L
  - One DPI 24-bit RGB parallel interface
  - Safety features such as freeze frame detection and MISR data check
- 3D Graphics Processing Unit
  - IMG BXS-4-64, up to 800MHz
  - 50GFLOPS, 4GTexels/s
  - >500MTexels/s, >8GFLOPs
  - Supports at least 2 composition layers
  - Supports up to 2048x1080 @60fps
  - Supports ARGB32, RGB565 and YUV formats
  - 2D graphics capable
  - OpenGL ES 3.1, Vulkan 1.2

- Two CSI2.0 4L Camera Serial interface (CSI-Rx) Plus CSI2.- 4L Tx (CSI-Tx) with DPHY
  - MIPI CSI 1.3 Compliant + MIPI-DPHY 1.2
  - Support for 1,2,3, or 4 data lane mode up to 2.5Gbps
  - ECC verification/correction with CRC check + ECC on RAM
  - Virtual Channel support (up to 16)
  - Ability to write stream data directly to DDR via DMA
- Video Encoder/Decoder
  - Support for HEVC (H.265) Main profiles at Level 5.1 High-tier
  - Support for H.264 BaseLine/Main/High Profiles at Level 5.2
  - Support for up to 4K UHD resolution (3840 × 2160)
  - 4K60 H.264/H.265 Encode/Decode (up to 480MP/s)

#### Memory subsystem:

- Up to 4MB of on-chip L3 RAM with ECC and coherency
  - ECC error protection
  - Shared coherent cache
  - Supports internal DMA engine
- Up to two External Memory Interface (EMIF) modules with ECC
  - Supports LPDDR4 memory types
  - Supports speeds up to 4266MT/s
  - Up to two 32-bit data bus with inline ECC up to 17GB/s per EMIF
- General-Purpose Memory Controller (GPMC)
- Up to two 512KB on-chip SRAM in MAIN domain, protected by ECC

#### Device security:

- Secure boot with secure run-time support
- Customer programmable root key, up to RSA-4K or ECC-512
- Embedded hardware security module
- Crypto hardware accelerators – PKA with ECC, AES, SHA, RNG, DES and 3DES

#### High speed serial interfaces:

- One PCI-Express® (PCIe) Gen3 controllers
  - Up to four lanes per controller
  - Gen1 (2.5GT/s), Gen2 (5.0GT/s), and Gen3 (8.0GT/s) operation with auto-negotiation



- One USB 3.0 dual-role device (DRD) subsystem
  - Enhanced SuperSpeed Gen1 Port
  - Supports Type-C switching
  - Independently configurable as USB host, USB peripheral, or USB DRD
- Two CSI2.0 4L Camera Serial interface RX (CSI-RX) plus two CSI2.0 4L TX (CSI-TX) with DPHY
  - MIPI CSI 1.3 Compliant + MIPI-DPHY 1.2
  - CSI-RX supports for 1,2,3, or 4 data lane mode up to 2.5Gbps per lane
  - CSI-TX supports for 1,2, or 4 data lane mode up to 2.5Gbps per lane

#### Ethernet:

- Two Ethernet RMII/RGMII interfaces

#### Flash memory interfaces:

- Embedded MultiMediaCard Interface (eMMC™ 5.1)
- One Secure Digital® 3.0/Secure Digital Input Output 3.0 interfaces (SD3.0/SDIO3.0)
- Two simultaneous flash interfaces configured as
  - One OSPI or HyperBus™ or QSPI, and
  - One QSPI

#### Technology / Package:

- 16-nm FinFET technology
- 23mm x 23mm, 0.8-mm pitch, 770-pin FCBGA (ALZ)

## 2 Applications

- Machine Vision Camera and computers
- Smart shopping cart
- Retail automation
- Smart agriculture
- Video surveillance
- Traffic monitoring
- Autonomous Mobile Robots (AMR)
- Drone
- Industrial transport
- Industrial Human Machine Interfaces (HMI)
- Industrial PC
- Single board computers
- Patient monitoring and medical devices

## 3 Description

The AM68 scalable processor family is based on the evolutionary Jacinto™ 7 architecture, targeted at Smart Vision Camera and General Compute applications and built on extensive market knowledge accumulated over a decade of TI's leadership in the Vision processor market. The AM68x family is built for a broad set of cost-sensitive high-performance compute applications in Factory Automation, Building Automation, and other markets.

The AM68 provides high performance compute technology for both traditional and deep learning algorithms at industry leading power/performance ratios with a high level of system integration to enable scalability and lower costs for advanced vision camera applications. Key cores include the latest Arm and GPU processors for general compute, next generation DSP with scalar and vector cores, dedicated deep learning and traditional algorithm accelerators, an integrated next generation imaging subsystem (ISP), video codec, and isolated MCU island. All protected by industrial-grade safety and security hardware accelerators.

**General Compute Cores and Integration Overview:** Separate dual core cluster configuration of Arm® Cortex®-A72 facilitates multi-OS applications with minimal need for a software hypervisor. Up to two Arm® Cortex®-R5F subsystems enable low-level, timing critical processing tasks to leave the Arm® Cortex®-A72 core's unencumbered for applications. Building on the existing world-class ISP, TI's 7th generation ISP includes flexibility to process a broader sensor suite, support for higher bit depth, and features targeting analytics applications. Integrated diagnostics and safety features support operations up to SIL-2 levels while the integrated security features protect data against modern day attacks. CSI2.0 ports enable multi sensor inputs.

**Key Performance Cores Overview:** The C7000™ DSP next generation core ("C7x") combines TI's industry leading DSP and EVE cores into a single higher performance core and adds floating-point vector calculation capabilities, enabling backward compatibility for legacy code while simplifying software programming. The new "MMA" deep learning accelerator enables performance up to 8 Trillion Operations Per Second (TOPS) within the lowest power envelope in the industry even when operating even at the worst case junction temperatures of 105°C and 125°C. The dedicated Vision hardware accelerators provide vision pre-processing with no impact on system performance. The C7x/MMA cores are available only for deep learning function in the AM68 class of processors.

**Package Information**

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| AM68x       | ALZ (FCBGA, 770)       | 23 mm × 23 mm               |

- (1) For more information, see the [Mechanical, Packaging, and Orderable Information](#) section.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.

### 3.1 Functional Block Diagram

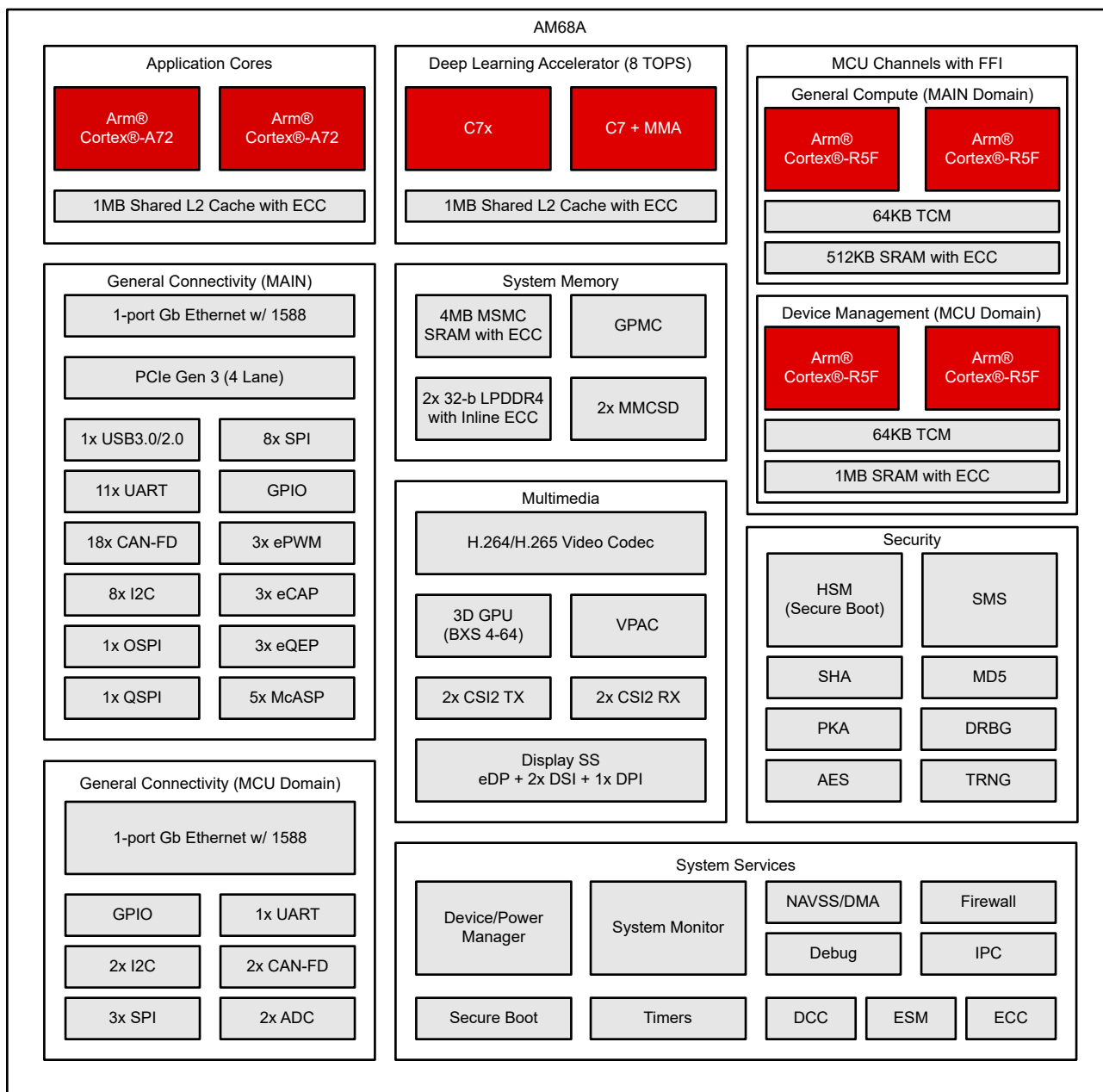
[Figure 1-1](#) is functional block diagram for the device.

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**Note**

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the [AM68 Software Build Sheet \(PROCESSOR-SDK-AM68\)](#) and [AM68A Software Build Sheet \(PROCESSOR-SDK-AM68A\)](#).

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**Figure 3-1. Functional Block Diagram**

## Table of Contents

|                                                                    |            |                                                                  |            |
|--------------------------------------------------------------------|------------|------------------------------------------------------------------|------------|
| <b>1 Features</b> .....                                            | <b>1</b>   | 6.9 Temperature Sensor Characteristics.....                      | <b>120</b> |
| <b>2 Applications</b> .....                                        | <b>3</b>   | 6.10 Timing and Switching Characteristics.....                   | <b>121</b> |
| <b>3 Description</b> .....                                         | <b>3</b>   | <b>7 Detailed Description</b> .....                              | <b>243</b> |
| 3.1 Functional Block Diagram.....                                  | <b>4</b>   | <b>8 Applications, Implementation, and Layout</b> .....          | <b>244</b> |
| <b>4 Device Comparison</b> .....                                   | <b>7</b>   | 8.1 Device Connection and Layout Fundamentals.....               | <b>244</b> |
| <b>5 Terminal Configuration and Functions</b> .....                | <b>10</b>  | 8.2 Peripheral- and Interface-Specific Design Information.....   | <b>244</b> |
| 5.1 Pin Diagrams.....                                              | <b>10</b>  | <b>9 Device and Documentation Support</b> .....                  | <b>251</b> |
| 5.2 Pin Attributes.....                                            | <b>10</b>  | 9.1 Device Nomenclature.....                                     | <b>251</b> |
| 5.3 Signal Descriptions.....                                       | <b>64</b>  | 9.2 Tools and Software.....                                      | <b>253</b> |
| 5.4 Connection for Unused Pins.....                                | <b>100</b> | 9.3 Documentation Support.....                                   | <b>254</b> |
| <b>6 Specifications</b> .....                                      | <b>104</b> | 9.4 Trademarks.....                                              | <b>254</b> |
| 6.1 Absolute Maximum Ratings.....                                  | <b>104</b> | 9.5 Support Resources.....                                       | <b>254</b> |
| 6.2 ESD Ratings.....                                               | <b>106</b> | 9.6 Electrostatic Discharge Caution.....                         | <b>254</b> |
| 6.3 Recommended Operating Conditions.....                          | <b>106</b> | 9.7 Glossary.....                                                | <b>254</b> |
| 6.4 Power-On-Hour (POH) Limits.....                                | <b>108</b> | <b>10 Revision History</b> .....                                 | <b>255</b> |
| 6.5 Operating Performance Points.....                              | <b>110</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>257</b> |
| 6.6 Electrical Characteristics.....                                | <b>111</b> | 11.1 Packaging Information.....                                  | <b>257</b> |
| 6.7 VPP Specifications for One-Time Programmable (OTP) eFuses..... | <b>117</b> |                                                                  |            |
| 6.8 Thermal Resistance Characteristics.....                        | <b>119</b> |                                                                  |            |

## 4 Device Comparison

Table 4-1 shows the features of the SoC.

### Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the [AM68 Software Build Sheet \(PROCESSOR-SDK-AM68\)](#) and [AM68A Software Build Sheet \(PROCESSOR-SDK-AM68A\)](#).

**Table 4-1. Device Comparison**

| FEATURES <sup>(7)</sup>                                            | REFERENCE NAME            | AM68A9                                  | AM68A7 | AM685 | AM683 |
|--------------------------------------------------------------------|---------------------------|-----------------------------------------|--------|-------|-------|
| PROCESSORS AND ACCELERATORS                                        |                           |                                         |        |       |       |
| Speed Grades                                                       |                           | T                                       | T, H   | T     | T     |
| Arm Cortex-A72 Microprocessor Subsystem                            | Arm A72                   | Dual Core                               |        |       |       |
| Arm Cortex-R5F                                                     | Arm R5F Device Management | Dual Core <sup>(10)</sup>               |        |       |       |
|                                                                    | Arm R5F General Compute   | Dual Core <sup>(10)</sup>               |        |       |       |
| Security Management Subsystem                                      | SMS                       | Yes                                     |        |       |       |
| Security Accelerators                                              | SA                        | Yes                                     |        |       |       |
| Deep Learning Accelerator (8 TOPS)                                 | C7x DSP                   | Yes <sup>(11)</sup>                     |        | No    |       |
|                                                                    | C7x DSP + MMA             | Yes <sup>(11)</sup>                     |        | No    |       |
| Graphics Accelerator IMG BXS-4-64                                  | GPU                       | Yes                                     | No     | Yes   | No    |
| Depth and Motion Processing Accelerators                           | DMPAC                     | No                                      |        |       |       |
| Vision Processing Accelerators                                     | VPAC                      | Yes                                     |        | No    |       |
| Video Encoder/Decoder                                              | VENC/VDEC                 | Encode/Decode                           |        |       | No    |
| SAFETY AND SECURITY                                                |                           |                                         |        |       |       |
| Safety Targeted                                                    | Safety                    | No <sup>(1)</sup>                       |        |       |       |
| Device Security                                                    | Security                  | Optional <sup>(2)</sup>                 |        |       |       |
| AEC-Q100 Qualified                                                 | Q1                        | Optional <sup>(3)</sup>                 |        |       |       |
| PROGRAM AND DATA STORAGE                                           |                           |                                         |        |       |       |
| On-Chip Shared Memory (RAM) in MAIN Domain                         | OCSRAM                    | 512KB SRAM                              |        |       |       |
| On-Chip Shared Memory (RAM) in MCU Domain                          | MCU_MSRAM                 | 1MB SRAM                                |        |       |       |
| Multicore Shared Memory Controller                                 | MSMC                      | 4MB (On-Chip SRAM with ECC)             |        |       |       |
| LPDDR4 DDR Subsystem                                               | DDRSS0 <sup>(4)</sup>     | Up to 8GB (32-bit data) with inline ECC |        |       |       |
|                                                                    | DDRSS1 <sup>(4)</sup>     | Up to 8GB (32-bit data) with inline ECC |        |       |       |
|                                                                    | SECEDED                   | Yes                                     |        |       |       |
| General-Purpose Memory Controller                                  | GPMC                      | Up to 1GB with ECC                      |        |       |       |
| PERIPHERALS                                                        |                           |                                         |        |       |       |
| Display Subsystem                                                  | DSS                       | Yes                                     |        |       |       |
|                                                                    | DSI 4L TX                 | 2                                       |        |       |       |
|                                                                    | eDP 4L                    | 1                                       |        |       |       |
|                                                                    | DPI                       | 1                                       |        |       |       |
| Modular Controller Area Network Interface with Full CAN-FD Support | MCAN                      | 20                                      |        |       |       |

**Table 4-1. Device Comparison (continued)**

| FEATURES <sup>(7)</sup>                                                           | REFERENCE NAME       | AM68A9                          | AM68A7 | AM685 | AM683 |
|-----------------------------------------------------------------------------------|----------------------|---------------------------------|--------|-------|-------|
| General-Purpose I/O                                                               | GPIO                 | 155                             |        |       |       |
| Inter-Integrated Circuit Interface                                                | I2C                  | 10                              |        |       |       |
| Improved Inter-Integrated Circuit Interface                                       | I3C                  | 1                               |        |       |       |
| Analog-to-Digital Converter                                                       | ADC                  | 2                               |        |       |       |
| Capture Subsystem with Camera Serial Interface (CSI2)                             | CSI2.0 4L RX         | 2                               |        |       |       |
|                                                                                   | CSI2.0 4L TX         | 2                               |        |       |       |
| Multichannel Serial Peripheral Interface                                          | MCSPi                | 11                              |        |       |       |
| Multichannel Audio Serial Port                                                    | MCASP0               | 16 Serializers                  |        |       |       |
|                                                                                   | MCASP1               | 5 Serializers                   |        |       |       |
|                                                                                   | MCASP2               | 5 Serializers                   |        |       |       |
|                                                                                   | MCASP3               | 3 Serializers                   |        |       |       |
|                                                                                   | MCASP4               | 5 Serializers                   |        |       |       |
| MultiMedia Card/ Secure Digital Interface                                         | MMCSd0               | eMMC (8-bits)                   |        |       |       |
|                                                                                   | MMCSd1               | SD/SDIO (4-bits)                |        |       |       |
| Universal Flash Storage                                                           | UFS 2L               | No                              |        |       |       |
| Flash Subsystem (FSS)                                                             | OSPI0                | 8-bits <sup>(6)</sup>           |        |       |       |
|                                                                                   | OSPI1 <sup>(8)</sup> | 4-bits                          |        |       |       |
|                                                                                   | HyperBus             | Yes <sup>(6)</sup>              |        |       |       |
| 4x PCI Express Port with Integrated PHY                                           | PCIE0                | Up to Four Lanes <sup>(5)</sup> |        |       |       |
| Hyperlink                                                                         | HYP                  | No <sup>(9)</sup>               |        |       |       |
| Gigabit Ethernet Interface                                                        | MCU                  | 1x RGMII or RMII                |        |       |       |
|                                                                                   | Main                 | 1x RGMII or RMII                |        |       |       |
| General-Purpose Timers                                                            | TIMER                | 30                              |        |       |       |
| Enhanced High Resolution Pulse-Width Modulator Module                             | eHRPWM               | 6                               |        |       |       |
| Enhanced Capture Module                                                           | eCAP                 | 3                               |        |       |       |
| Enhanced Quadrature Encoder Pulse Module                                          | eQEP                 | 3                               |        |       |       |
| Universal Asynchronous Receiver and Transmitter                                   | UART                 | 12                              |        |       |       |
| Universal Serial Bus (USB3.1) SuperSpeed Dual-Role-Device (DRD) Ports with SS PHY | USB0                 | Yes <sup>(5)</sup>              |        |       |       |

- (1) Functional Safety is not supported on this device family, if interested in this feature, please see the [TDA4VE device family](#).
- (2) Device security features including Secure Boot and Customer Programmable Keys are applicable to select part number variants as indicated by the Device Type (Y) identifier in the Table 10-1, Nomenclature Description table
- (3) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the Table 10-1, Nomenclature Description table
- (4) DDRSS0 and DDRSS1 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0\_\* interface.
- (5) USB3.0 and PCIE share a total of four SerDes lanes.
- (6) Two simultaneous flash interfaces configured as OSPI0 and OSPI1, or HyperBus and OSPI1.
- (7) J721S2 is the base part number for the superset device. Software should constrain the features used to match the intended production device.
- (8) OSPI1 module only pins out 4 pins and is referred to as QSPI in some contexts.
- (9) Hyperlink is not supported on this SoC. System designs should not use the signals HYP\_\*, HYP0\_\*, HYP1\_\*.
- (10) MCU\_R5FSS0 includes Dual-Core R5F that provides Device Management functionality, and is reserved for executing TI provided code.

- R5FSS1 is a Dual-Core R5F that provides Multimedia Control functionality, and is reserved for executing TI provided code.
- (11) The two C7x DSPs are reserved for executing TI provided code, and are not available for custom code.

## 5 Terminal Configuration and Functions

### 5.1 Pin Diagrams

See Packaging Information.

### 5.2 Pin Attributes

1. **BALL NUMBER:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **BALL NAME:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **SIGNAL NAME:** Signal name of all dedicated and pin multiplexed signal functions associated with a ball.

---

#### Note

The *Pin Attributes* table, defines the SoC pin multiplexed signal function implemented at the pin and **does not** define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

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4. **MUXMODE:** The MUXMODE value associated with each pin multiplexed signal function:
  - MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.
  - MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only valid values of MUXMODE can be used.
  - Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz\_OUT. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
  - An empty box or "-" means Not Applicable.

---

#### Note

- The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU\_PORz is deasserted.
  - Configuring two pins to the same pin multiplexed signal function can yield unexpected results and is not supported. This can be prevented with proper software configuration.
  - Configuring a pad to an undefined multiplexing mode results in undefined behavior and must be avoided.
- 

5. **TYPE:** Signal type and direction:
  - I = Input
  - O = Output
  - OD = Output, with open-drain output function
  - IO = Input, Output, or simultaneously Input and Output
  - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
  - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
  - OZ = Output with three-state output function
  - A = Analog
  - CAP = LDO capacitor
  - PWR = Power
  - GND = Ground
6. **I/O OPERATING VOLTAGE:** This column describes the IO voltage value (the corresponding power supply). An empty box means Not Applicable.

7. **BALL STATE DURING RESET:** State of the terminal while MCU\_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
  - RX (Input buffer)
    - Off: The input buffer is **disabled**.
    - On: The input buffer is **enabled**.
  - TX (Output buffer)
    - Off: The output buffer is **disabled**.
    - Low: The output buffer is **enabled** and drives  $V_{OL}$ .
    - High: The output buffer is **enabled** and drives  $V_{OH}$ .
  - PULL (Internal pull resistors)
    - Off: Internal pull resistors are turned **off**.
    - Up: Internal **pull-up** resistor is turned on.
    - Down: Internal **pull-down** resistor is turned on.
    - NA: No internal pull resistor.
  - An empty box, or "-" means Not Applicable.
8. **BALL STATE AFTER RESET:** State of the terminal after MCU\_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
  - RX (Input buffer)
    - Off: The input buffer is **disabled**.
    - On: The input buffer is **enabled**.
  - TX (Output buffer)
    - Off: The output buffer is **disabled**.
    - SS: The subsystem selected with MUXMODE determines the output buffer state.
  - PULL (Internal pull resistors)
    - Off: Internal pull resistors are turned **off**.
    - Up: Internal **pull-up resistor** is turned on.
    - Down: Internal **pull-down resistor** is turned on.
    - NA: No internal pull resistor.
  - An empty box, NA, or "-" means Not Applicable.
9. **MUX MODE AFTER RESET:** The value found in this column defines the **default** pin multiplexed signal function after MCU\_PORz is deasserted.
  - An empty box, NA, or "-" means Not Applicable.
10. **PULL TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
  - PU: Internal pull-up Only
  - PD: Internal pull-down Only
  - PU/PD: Internal pull-up and pull-down
  - An empty box, NA, or "-" means No internal pull.

---

#### Note

Configuring two pins to the same pin multiplexed signal function is not supported as this yields unexpected results. Issues can be easily prevented with the proper software configuration.

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This must be avoided.

---

11. **POWER:** The power supply of the associated I/O, when applicable.
  - An empty box, NA, or "-" means Not Applicable.
12. **HYS:** Indicates if the input buffer associated with this I/O has hysteresis:
  - Yes: Hysteresis Support

- No: **No** Hysteresis Support
- An empty box, NA, or "-" means Not Applicable.

For more information, see the hysteresis values in [Electrical Characteristics](#) section.

13. **VOLTAGE BUFFER TYPE:** This column defines the buffer type associated with a terminal. This information can be used to determine the applicable Electrical Characteristics table.

- An empty box, NA, or "-" means Not Applicable.

For electrical characteristics, refer to the appropriate buffer type table in [Electrical Characteristics](#) section.

14. **IO RET:** Yes means WKUP and IO retention supported.
15. **PADCFG NAME:** This is the name of the device pad/pin configuration register.
16. **PADCFG ADDRESS:** This is the memory address of the device pad/pin configuration register.

Table 5-1. Pin Attributes (ALZ Package)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                       | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------------------------------|----------|--------------------------|-------------|
| T21          | CAP_VDDS0                                                    | CAP_VDDS0       |              | CAP             |                           |                                          |                                         |                          |                |                                                  |          |                          |             |
| J20          | CAP_VDDS0_MCU                                                | CAP_VDDS0_MCU   |              | CAP             |                           |                                          |                                         |                          |                |                                                  |          |                          |             |
| G16          | CAP_VDDS1_MCU                                                | CAP_VDDS1_MCU   |              | CAP             |                           |                                          |                                         |                          |                |                                                  |          |                          |             |
| P21          | CAP_VDDS2                                                    | CAP_VDDS2       |              | CAP             |                           |                                          |                                         |                          |                |                                                  |          |                          |             |
| H17          | CAP_VDDS2_MCU                                                | CAP_VDDS2_MCU   |              | CAP             |                           |                                          |                                         |                          |                |                                                  |          |                          |             |
| M22          | CAP_VDDS5                                                    | CAP_VDDS5       |              | CAP             |                           |                                          |                                         |                          |                |                                                  |          |                          |             |
| AH19         | CSI0_RXCLKN                                                  | CSI0_RXCLKN     |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AH20         | CSI0_RXCLKP                                                  | CSI0_RXCLKP     |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AC18         | CSI0_RXRCALIB                                                | CSI0_RXRCALIB   |              | A               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AH22         | CSI1_RXCLKN                                                  | CSI1_RXCLKN     |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AH23         | CSI1_RXCLKP                                                  | CSI1_RXCLKP     |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AC21         | CSI1_RXRCALIB                                                | CSI1_RXRCALIB   |              | A               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AG18         | CSI0_RXN0                                                    | CSI0_RXN0       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AF19         | CSI0_RXN1                                                    | CSI0_RXN1       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AE18         | CSI0_RXN2                                                    | CSI0_RXN2       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AD19         | CSI0_RXN3                                                    | CSI0_RXN3       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                       | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------------------------------|----------|--------------------------|-------------|
| AG19         | CSI0_RXP0                                                    | CSI0_RXP0       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AF20         | CSI0_RXP1                                                    | CSI0_RXP1       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AE19         | CSI0_RXP2                                                    | CSI0_RXP2       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AD20         | CSI0_RXP3                                                    | CSI0_RXP3       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AG21         | CSI1_RXN0                                                    | CSI1_RXN0       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AF22         | CSI1_RXN1                                                    | CSI1_RXN1       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AE21         | CSI1_RXN2                                                    | CSI1_RXN2       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AD22         | CSI1_RXN3                                                    | CSI1_RXN3       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AG22         | CSI1_RXP0                                                    | CSI1_RXP0       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AF23         | CSI1_RXP1                                                    | CSI1_RXP1       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AE22         | CSI1_RXP2                                                    | CSI1_RXP2       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AD23         | CSI1_RXP3                                                    | CSI1_RXP3       |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| R1           | DDR0_CKN                                                     | DDR0_CKN        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR /<br>VDDS_DDR_ C0                       |          | DDR                      |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| P1           | DDR0_CKP                                                     | DDR0_CKP        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| R5           | DDR0_RESETh                                                  | DDR0_RESETh     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| T8           | DDR0_RET                                                     | DDR0_RET        |              | I               | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| A9           | DDR1_CKN                                                     | DDR1_CKN        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A10          | DDR1_CKP                                                     | DDR1_CKP        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F12          | DDR1_RESETh                                                  | DDR1_RESETh     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| J10          | DDR1_RET                                                     | DDR1_RET        |              | I               | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| P3           | DDR0_CA0                                                     | DDR0_CA0        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| P5           | DDR0_CA1                                                     | DDR0_CA1        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| N5           | DDR0_CA2                                                     | DDR0_CA2        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| P2           | DDR0_CA3                                                     | DDR0_CA3        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| P4           | DDR0_CA4                                                     | DDR0_CA4        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| R3           | DDR0_CA5                                                     | DDR0_CA5        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| R8           | DDR0_CAL0                                                    | DDR0_CAL0       |              | A               | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| R2           | DDR0_CKE0                                                    | DDR0_CKE0       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| R4           | DDR0_CKE1                                                    | DDR0_CKE1       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| V5           | DDR0_CSn0_0                                                  | DDR0_CSn0_0     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| W5           | DDR0_CSn0_1                                                  | DDR0_CSn0_1     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| T5           | DDR0_CSn1_0                                                  | DDR0_CSn1_0     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| U6           | DDR0_CSn1_1                                                  | DDR0_CSn1_1     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| H5           | DDR0_DM0                                                     | DDR0_DM0        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| M3           | DDR0_DM1                                                     | DDR0_DM1        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| U4           | DDR0_DM2                                                     | DDR0_DM2        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AD1          | DDR0_DM3                                                     | DDR0_DM3        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| F3           | DDR0_DQ0                                                     | DDR0_DQ0        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| G4           | DDR0_DQ1                                                     | DDR0_DQ1        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| F5           | DDR0_DQ2                                                     | DDR0_DQ2        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| F1           | DDR0_DQ3                                                     | DDR0_DQ3        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| J4           | DDR0_DQ4                                                     | DDR0_DQ4        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| H3           | DDR0_DQ5                                                     | DDR0_DQ5        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| J2           | DDR0_DQ6                                                     | DDR0_DQ6        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| G2           | DDR0_DQ7                                                     | DDR0_DQ7        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| K5           | DDR0_DQ8                                                     | DDR0_DQ8        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| M5           | DDR0_DQ9                                                     | DDR0_DQ9        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| K3           | DDR0_DQ10                                                    | DDR0_DQ10       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| K1           | DDR0_DQ11                                                    | DDR0_DQ11       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| N4           | DDR0_DQ12                                                    | DDR0_DQ12       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| N2           | DDR0_DQ13                                                    | DDR0_DQ13       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| L4           | DDR0_DQ14                                                    | DDR0_DQ14       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| L2           | DDR0_DQ15                                                    | DDR0_DQ15       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| T1           | DDR0_DQ16                                                    | DDR0_DQ16       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| T3           | DDR0_DQ17                                                    | DDR0_DQ17       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| V3           | DDR0_DQ18                                                    | DDR0_DQ18       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| U2           | DDR0_DQ19                                                    | DDR0_DQ19       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| W2           | DDR0_DQ20                                                    | DDR0_DQ20       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| W4           | DDR0_DQ21                                                    | DDR0_DQ21       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| Y1           | DDR0_DQ22                                                    | DDR0_DQ22       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| Y3           | DDR0_DQ23                                                    | DDR0_DQ23       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| AB3          | DDR0_DQ24                                                    | DDR0_DQ24       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AA2          | DDR0_DQ25                                                    | DDR0_DQ25       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AA4          | DDR0_DQ26                                                    | DDR0_DQ26       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| Y5           | DDR0_DQ27                                                    | DDR0_DQ27       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AC2          | DDR0_DQ28                                                    | DDR0_DQ28       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AB5          | DDR0_DQ29                                                    | DDR0_DQ29       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AD2          | DDR0_DQ30                                                    | DDR0_DQ30       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AC4          | DDR0_DQ31                                                    | DDR0_DQ31       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| H1           | DDR0_QS0N                                                    | DDR0_QS0N       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| G1           | DDR0_QS0P                                                    | DDR0_QS0P       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| M1           | DDR0_QS1N                                                    | DDR0_QS1N       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| L1           | DDR0_QS1P                                                    | DDR0_QS1P       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| U1           | DDR0_QS2N                                                    | DDR0_QS2N       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| V1           | DDR0_QS2P                                                    | DDR0_QS2P       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AC1          | DDR0_QS3N                                                    | DDR0_QS3N       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AB1          | DDR0_QS3P                                                    | DDR0_QS3P       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| C10          | DDR1_CA0                                                     | DDR1_CA0        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E10          | DDR1_CA1                                                     | DDR1_CA1        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E9           | DDR1_CA2                                                     | DDR1_CA2        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B10          | DDR1_CA3                                                     | DDR1_CA3        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D10          | DDR1_CA4                                                     | DDR1_CA4        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C9           | DDR1_CA5                                                     | DDR1_CA5        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E8           | DDR1_CAL0                                                    | DDR1_CAL0       |              | A               | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B9           | DDR1_CKE0                                                    | DDR1_CKE0       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D9           | DDR1_CKE1                                                    | DDR1_CKE1       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F9           | DDR1_CSn0_0                                                  | DDR1_CSn0_0     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F8           | DDR1_CSn0_1                                                  | DDR1_CSn0_1     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F11          | DDR1_CSn1_0                                                  | DDR1_CSn1_0     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F10          | DDR1_CSn1_1                                                  | DDR1_CSn1_1     |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D16          | DDR1_DM0                                                     | DDR1_DM0        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E13          | DDR1_DM1                                                     | DDR1_DM1        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F7           | DDR1_DM2                                                     | DDR1_DM2        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]             | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------------------|----------|--------------------------|-------------|
| B3           | DDR1_DM3                                                     | DDR1_DM3        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| B18          | DDR1_DQ0                                                     | DDR1_DQ0        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| E17          | DDR1_DQ1                                                     | DDR1_DQ1        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| D18          | DDR1_DQ2                                                     | DDR1_DQ2        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| A17          | DDR1_DQ3                                                     | DDR1_DQ3        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| E15          | DDR1_DQ4                                                     | DDR1_DQ4        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| B16          | DDR1_DQ5                                                     | DDR1_DQ5        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| C15          | DDR1_DQ6                                                     | DDR1_DQ6        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| C17          | DDR1_DQ7                                                     | DDR1_DQ7        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| B14          | DDR1_DQ8                                                     | DDR1_DQ8        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| D14          | DDR1_DQ9                                                     | DDR1_DQ9        |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| C13          | DDR1_DQ10                                                    | DDR1_DQ10       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| C11          | DDR1_DQ11                                                    | DDR1_DQ11       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| E11          | DDR1_DQ12                                                    | DDR1_DQ12       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| A11          | DDR1_DQ13                                                    | DDR1_DQ13       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |
| B12          | DDR1_DQ14                                                    | DDR1_DQ14       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDS_DDR / VDDS_DDR_C1 |          | DDR                      |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| D12          | DDR1_DQ15                                                    | DDR1_DQ15       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B7           | DDR1_DQ16                                                    | DDR1_DQ16       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D7           | DDR1_DQ17                                                    | DDR1_DQ17       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C8           | DDR1_DQ18                                                    | DDR1_DQ18       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A8           | DDR1_DQ19                                                    | DDR1_DQ19       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C6           | DDR1_DQ20                                                    | DDR1_DQ20       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E6           | DDR1_DQ21                                                    | DDR1_DQ21       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B5           | DDR1_DQ22                                                    | DDR1_DQ22       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D5           | DDR1_DQ23                                                    | DDR1_DQ23       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B1           | DDR1_DQ24                                                    | DDR1_DQ24       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A4           | DDR1_DQ25                                                    | DDR1_DQ25       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C4           | DDR1_DQ26                                                    | DDR1_DQ26       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E4           | DDR1_DQ27                                                    | DDR1_DQ27       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D1           | DDR1_DQ28                                                    | DDR1_DQ28       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D3           | DDR1_DQ29                                                    | DDR1_DQ29       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C2           | DDR1_DQ30                                                    | DDR1_DQ30       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                            | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------|----------|--------------------------|-------------|
| E2           | DDR1_DQ31                                                    | DDR1_DQ31       |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1                              |          | DDR                      |             |
| A15          | DDR1_DQS0N                                                   | DDR1_DQS0N      |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1                              |          | DDR                      |             |
| A16          | DDR1_DQS0P                                                   | DDR1_DQS0P      |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1                              |          | DDR                      |             |
| A12          | DDR1_DQS1N                                                   | DDR1_DQS1N      |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1                              |          | DDR                      |             |
| A13          | DDR1_DQS1P                                                   | DDR1_DQS1P      |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1                              |          | DDR                      |             |
| A7           | DDR1_DQS2N                                                   | DDR1_DQS2N      |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1                              |          | DDR                      |             |
| A6           | DDR1_DQS2P                                                   | DDR1_DQS2P      |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1                              |          | DDR                      |             |
| A2           | DDR1_DQS3N                                                   | DDR1_DQS3N      |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1                              |          | DDR                      |             |
| A3           | DDR1_DQS3P                                                   | DDR1_DQS3P      |              | IO              | 1.1 V                     |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1                              |          | DDR                      |             |
| AG11         | DP0_AUXN                                                     | DP0_AUXN        |              | IO              | 1.8 V                     |                                          |                                         |                          |                | VDDA_1P8_S ERDES2_4                                   |          | AUX-PHY                  |             |
| AF11         | DP0_AUXP                                                     | DP0_AUXP        |              | IO              | 1.8 V                     |                                          |                                         |                          |                | VDDA_1P8_S ERDES2_4                                   |          | AUX-PHY                  |             |
| AH13         | DSIO_TXCLKN                                                  | DSIO_TXCLKN     | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D SITX / VDDA_0P8_D SITX_C / VDDA_1P8_D SITX |          | D-PHY                    |             |
|              |                                                              | CSIO_TXCLKN     | 1            | O               |                           |                                          |                                         |                          |                | VDDA_0P8_D SITX / VDDA_0P8_D SITX_C / VDDA_1P8_D SITX |          |                          |             |
| AH14         | DSIO_TXCLKP                                                  | DSIO_TXCLKP     | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D SITX / VDDA_0P8_D SITX_C / VDDA_1P8_D SITX |          | D-PHY                    |             |
|              |                                                              | CSIO_TXCLKP     | 1            | O               |                           |                                          |                                         |                          |                | VDDA_0P8_D SITX / VDDA_0P8_D SITX_C / VDDA_1P8_D SITX |          |                          |             |
| AC13         | DSIO_TXRCALIB                                                | DSIO_TXRCALIB   |              | A               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D SITX / VDDA_0P8_D SITX_C / VDDA_1P8_D SITX |          | D-PHY                    |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------------------------------------------------------|----------|--------------------------|-------------|
| AH16         | DSI1_TXCLKN                                                  | DSI1_TXCLKN     | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXCLKN     | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AH17         | DSI1_TXCLKP                                                  | DSI1_TXCLKP     | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXCLKP     | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AC15         | DSI1_TXRCALIB                                                | DSI1_TXRCALIB   |              | A               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
| AG12         | DSI0_TXN0                                                    | DSI0_TXN0       | 0            | IO              | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXN0       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AF13         | DSI0_TXN1                                                    | DSI0_TXN1       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXN1       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AE12         | DSI0_TXN2                                                    | DSI0_TXN2       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXN2       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AD13         | DSI0_TXN3                                                    | DSI0_TXN3       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXN3       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AG13         | DSI0_TXP0                                                    | DSI0_TXP0       | 0            | IO              | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXP0       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AF14         | DSI0_TXP1                                                    | DSI0_TXP1       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXP1       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------------------------------------------------------|----------|--------------------------|-------------|
| AE13         | DSI0_TXP2                                                    | DSI0_TXP2       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXP2       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AD14         | DSI0_TXP3                                                    | DSI0_TXP3       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXP3       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AG15         | DSI1_TXN0                                                    | DSI1_TXN0       | 0            | IO              | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXN0       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AF16         | DSI1_TXN1                                                    | DSI1_TXN1       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXN1       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AE15         | DSI1_TXN2                                                    | DSI1_TXN2       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXN2       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AD16         | DSI1_TXN3                                                    | DSI1_TXN3       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXN3       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AG16         | DSI1_TXP0                                                    | DSI1_TXP0       | 0            | IO              | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXP0       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AF17         | DSI1_TXP1                                                    | DSI1_TXP1       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXP1       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AE16         | DSI1_TXP2                                                    | DSI1_TXP2       | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXP2       | 1            | O               |                           |                                          |                                         |                          |                |                                                                      |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                            | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------|----------|--------------------------|-------------|
| AD17         | DSI1_TXP3                                                    | DSI1_TXP3         | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_D SITX / VDDA_0P8_D SITX_C / VDDA_1P8_D SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXP3         | 1            | O               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
| AB26         | ECAP0_IN_APWM_OUT<br><br>PADCFG: PADCONFIG_49<br>0x0011C0C4  | ECAP0_IN_APWM_OUT | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2                                               | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_AXR2       | 1            | IO              |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | CPTS0_RFT_CLK     | 2            | I               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | HYP1_TXFLCLK      | 3            | I               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | MCAN12_TX         | 4            | O               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | VOUT0_DATA23      | 5            | O               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | GPMC0_AD5         | 6            | IO              |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | GPIO0_49          | 7            | IO              |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | SPI6_D0           | 8            | IO              |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | SYNC0_OUT         | 9            | O               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | TRC_DATA1         | 10           | O               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | UART2_CTSn        | 11           | I               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | CPTS0_HW1TSPUSH   | 12           | I               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
|              |                                                              | I2C1_SCL          | 13           | IOD             |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
| UART3_RXD    | 14                                                           | I                 |              |                 |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
| A27          | EMU0<br><br>PADCFG: WKUP_PADCONFIG_75<br>0x4301C12C          | EMU0              | 0            | IO              | 1.8 V/3.3 V               | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_MCU                                           | Yes      | LVCMOS                   | No          |
| C26          | EMU1<br><br>PADCFG: WKUP_PADCONFIG_76<br>0x4301C130          | EMU1              | 0            | IO              | 1.8 V/3.3 V               | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_MCU                                           | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_OBSCLK0       | 15           | O               |                           |                                          |                                         |                          |                |                                                       |          |                          |             |
| AG24         | EXTINTn<br><br>PADCFG: PADCONFIG_0<br>0x0011C000             | EXTINTn           | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / SS / Off                          | 7                        |                | VDDSHV0                                               | Yes      | I2C OPEN DRAIN           | No          |
|              |                                                              | GPIO0_0           | 7            | IO              |                           |                                          |                                         |                          |                |                                                       |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AD28         | EXT_REFCLK1<br>PADCFG: PADCONFIG_50<br>0x0011C0C8            | EXT_REFCLK1     | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_ACLKX    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA16    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_TXFLDAT    | 3            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCAN1_RX        | 4            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD6       | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_50        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SYNC1_OUT       | 9            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_CLK         | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_RTSn      | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | CPTS0_HW2TSPUSH | 12           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SDA        | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_TXD       | 14           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              |                 |              |                 |                           |                                          |                                         |                          |                |            |          |                          |             |
| V23          | GPIO0_11<br>PADCFG: PADCONFIG_11<br>0x0011C02C               | MCAN17_TX       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA18    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A14       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_11        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CS3        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA25      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CS2       | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART7_RXD       | 13           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | USB0_DRVVBUS    | 14           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| T26          | GPIO0_12<br>PADCFG: PADCONFIG_12<br>0x0011C030               | MCAN12_RX       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA17    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_RXFLDAT    | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA22    | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD4       | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_12        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_CLK        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP1_I         | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA2       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_CTSn      | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_RXD       | 12           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AH25         | I2C0_SCL<br>PADCFG: PADCONFIG_56<br>0x0011C0E0               | I2C0_SCL        | 0            | IOD             | 1.8 V/3.3 V               | Off / Off / Off                          | On / SS / Off                           | 7                        |                | VDDSHV0    | Yes      | I2C OPEN DRAIN           | No          |
|              |                                                              | GPIO0_56        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AE24         | I2C0_SDA<br><br>PADCFG:<br>PADCONFIG_57<br>0x0011C0E4        | I2C0_SDA        | 0            | IOD             | 1.8 V/3.3 V               | Off / Off / Off                          | On / SS / Off                           | 7                        |                | VDDSHV0    | Yes      | I2C OPEN DRAIN           | No          |
|              |                                                              | GPIO0_57        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
| U28          | MCAN0_RX<br><br>PADCFG:<br>PADCONFIG_26<br>0x0011C068        | MCAN0_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_AXR1     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOU0_DATA3      | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD15      | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_26        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CS0        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_A       | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA16      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_RTSn      | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_D0         | 13           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
| W28          | MCAN0_TX<br><br>PADCFG:<br>PADCONFIG_25<br>0x0011C064        | MCAN0_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_AXR2     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOU0_DATA4      | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD14      | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_25        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CS1        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_B       | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA11      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_CTSn      | 12           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C3_SCL        | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
| R27          | MCAN1_RX<br><br>PADCFG:<br>PADCONFIG_28<br>0x0011C070        | MCAN1_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_AXR3     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOU0_DATA1      | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOU0_DATA19     | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_BE0n_CLE  | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_28        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_D0         | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_SYNCI   | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA5       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_RTSn      | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| V26          | MCAN1_TX<br>PADCFG:<br>PADCONFIG_27<br>0x0011C06C            | MCAN1_TX          | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_AFSX       | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_EXTCLKIN    | 2            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_TXPMCLK      | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNC0        | 4            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD7         | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_27          | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN5    | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_CTL           | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_TXD         | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| Y25          | MCAN2_RX<br>PADCFG:<br>PADCONFIG_30<br>0x0011C078            | MCAN2_RX          | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | AUDIO_EXT_REFCLK1 | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_PCLK        | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CSn1        | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_30          | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_CS1          | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM4_B         | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA17        | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_TXD         | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_DIR         | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| R28          | MCAN2_TX<br>PADCFG:<br>PADCONFIG_29<br>0x0011C074            | I2C5_SDA          | 13           | IOD             | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCAN2_TX          | 0            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP2_AXR3       | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA0       | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA18      | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WAIT0       | 6            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_29          | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_D1           | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM1_B         | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA3         | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_RXD         | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_DIR         | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C5_SCL          | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AC24         | MCAN12_RX<br>PADCFG:<br>PADCONFIG_2<br>0x0011C008            | MCAN12_RX       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART0_DCDn      | 1            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNC1      | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A23       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_2         | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_CTL         | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CSn3      | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| W25          | MCAN12_TX<br>PADCFG:<br>PADCONFIG_1<br>0x0011C004            | MCAN12_TX       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | DSS_FSYNC0      | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A24       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_1         | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_CLK         | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CLK       | 12           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
| AF28         | MCAN13_RX<br>PADCFG:<br>PADCONFIG_4<br>0x0011C010            | MCAN13_RX       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART0_DTRn      | 1            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNC3      | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A21       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_4         | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SDA        | 8            | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA1       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AE28         | MCAN13_TX<br>PADCFG:<br>PADCONFIG_3<br>0x0011C00C            | MCAN13_TX       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART0_DSRn      | 1            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNC2      | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A22       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_3         | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA0       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WAIT2     | 12           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| W23          | MCAN14_RX<br>PADCFG:<br>PADCONFIG_6<br>0x0011C018            | MCAN14_RX       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA23    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A19       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_6         | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C5_SDA        | 8            | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA3       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AD25         | MCAN14_TX<br>PADCFG:<br>PADCONFIG_5<br>0x0011C014            | MCAN14_TX       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART0_RIn       | 1            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A20       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_5         | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SCL        | 8            | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA2       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AA23         | MCAN15_RX<br>PADCFG:<br>PADCONFIG_8<br>0x0011C020            | MCAN15_RX       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA21    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A17       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_8         | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI0_CS2        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA22      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SCL        | 12           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
| Y24          | MCAN15_TX<br>PADCFG:<br>PADCONFIG_7<br>0x0011C01C            | MCAN15_TX       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA22    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A18       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_7         | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C5_SCL        | 8            | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA21      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AB24         | MCAN16_RX<br>PADCFG:<br>PADCONFIG_10<br>0x0011C028           | MCAN16_RX       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA19    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A15       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_10        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI0_CS3        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA24      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WAIT1     | 12           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| Y28          | MCAN16_TX<br>PADCFG:<br>PADCONFIG_9<br>0x0011C024            | MCAN16_TX       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA20    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A16       | 6            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_9         | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_CS3        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA23      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SDA        | 12           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
| AB28         | MCASP0_ACLKX<br>PADCFG:<br>PADCONFIG_14<br>0x0011C038        | MCAN5_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_ACLKX    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA15    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_RXFLCLK    | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD0       | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_14        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN2  | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| U27          | MCASP0_AFSX<br>PADCFG:<br>PADCONFIG_15<br>0x0011C03C         | UART8_RXD       | 11           | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCAN5_RX        | 0            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP0_AFSX     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA14    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_RXFLDAT    | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD1       | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_15        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
| AA24         | MCASP1_ACLKX<br>PADCFG:<br>PADCONFIG_46<br>0x0011C0B8        | EHRPWM2_B       | 9            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART8_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCAN10_RX       | 0            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP1_ACLKX    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DP0_HPDP        | 3            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A11       | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_RD0       | 6            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_46        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP0_S         | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RTSn      | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CS3        | 12           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_RTSn      | 13           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| V28          | MCASP1_AFSX<br>PADCFG:<br>PADCONFIG_47<br>0x0011C0BC         | MCAN11_TX       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AFSX     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A12       | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MDIO0_MDIO      | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_47        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CS0        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP0_I         | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| Y27          | MCASP2_ACLKX<br>PADCFG:<br>PADCONFIG_21<br>0x0011C054        | MCAN8_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_ACLKX    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA8     | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_TXPMCLK    | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA20    | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD10      | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_21        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CS2        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP2_S         | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA4       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART1_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CS1        | 13           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SYNC3_OUT       | 14           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              |                 |              |                 |                           |                                          |                                         |                          |                |            |          |                          |             |
| AA27         | MCASP2_AFSX<br>PADCFG:<br>PADCONFIG_22<br>0x0011C058         | MCAN9_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_AFSX     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA7     | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_TXPMDAT    | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD11      | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_22        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CS3        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_SOCA     | 9            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA9       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART1_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CS2        | 13           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AC28         | MCASP0_AXR0<br>PADCFG:<br>PADCONFIG_16<br>0x0011C040         | MCAN6_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR0     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA13    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_TXFLCLK    | 3            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD2       | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_16        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CS2        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM2_A       | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA14      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CLK        | 13           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART8_CTSn      | 14           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| Y26          | MCASP0_AXR1<br>PADCFG:<br>PADCONFIG_17<br>0x0011C044         | MCAN6_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR1     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA12    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_TXFLDAT    | 3            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | OBCLK1          | 4            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD3       | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_17        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CS3        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_SYNCO   | 9            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA12      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CS0        | 13           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART8_RTSn      | 14           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AB27         | MCASP0_AXR2<br>PADCFG:<br>PADCONFIG_18<br>0x0011C048         | MCAN7_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR2     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA11    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_RXFLCLK    | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_ADVn_ALE  | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_18        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP2_A         | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA10      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_CTSn      | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WPn       | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_CTSn      | 13           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| T27          | MCASP0_AXR3<br>PADCFG:<br>PADCONFIG_31<br>0x0011C07C         | MCAN3_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR3     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA2     | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_BE1n      | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_31        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CLK        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN0  | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA7       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_CTSn      | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CS1        | 12           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_D1         | 13           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
| U26          | MCASP0_AXR4<br>PADCFG:<br>PADCONFIG_32<br>0x0011C080         | MCAN3_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR4     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_HSYNC     | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_TXPMDAT    | 3            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP0_HSYNC | 4            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP2_HSYNC | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_OEn_REn   | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_32        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_CS2        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM5_B       | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA18      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AA28         | MCASP0_AXR5<br>PADCFG:<br>PADCONFIG_33<br>0x0011C084         | I2C4_SDA        | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCAN4_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR5     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DE        | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP1_ACLKR    | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP0_DE    | 4            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP2_DE    | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CSn0      | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_33        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_CS3        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM5_A       | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA19      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SCL        | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AD27         | MCASP0_AXR6<br>PADCFG:<br>PADCONFIG_34<br>0x0011C088         | MCAN4_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR6     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VSYNC     | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP1_AFSR     | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP0_VSYNC | 4            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP2_VSYNC | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CLKOUT    | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_34        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CS2        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN4  | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA20      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_D1         | 11           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_FCLK_MUX  | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| T25          | MCASP0_AXR7<br>PADCFG:<br>PADCONFIG_35<br>0x0011C08C         | MCAN5_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR7     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP4_ACLKR    | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A0        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TD0       | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_35        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A14       | 8            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_A       | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CS2       | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | USB0_DRVVBUS    | 14           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| W24          | MCASP0_AXR8<br>PADCFG:<br>PADCONFIG_36<br>0x0011C090         | MCAN5_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR8     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP4_AFSR     | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A1        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TD1       | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_36        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_RXD0      | 8            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN3  | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AA25         | MCASP0_AXR9<br>PADCFG:<br>PADCONFIG_37<br>0x0011C094         | MCAN6_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR9     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP4_AXR4     | 2            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A2        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TD2       | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_37        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_RXD1      | 8            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_SYNCO   | 9            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_CTSn      | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| V25          | MCASP0_AXR10<br>PADCFG:<br>PADCONFIG_38<br>0x0011C098        | MCAN6_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR10    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A3        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TD3       | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_38        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_CRS_DV    | 8            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_SYNCI   | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RTSn      | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| T24          | MCASP0_AXR11<br>PADCFG:<br>PADCONFIG_39<br>0x0011C09C        | MCAN7_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR11    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A4        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TX_CTL    | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_39        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_RX_ER     | 8            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_B       | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CS1        | 10           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AB25         | MCASP0_AXR12<br>PADCFG:<br>PADCONFIG_40<br>0x0011C0A0        | MCAN7_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR12    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP2_ACLKR    | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A5        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_RD1       | 6            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_40        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_TXD0      | 8            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_SOCB    | 9            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CLK        | 10           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| T23          | MCASP0_AXR13<br>PADCFG:<br>PADCONFIG_41<br>0x0011C0A4        | MCAN8_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR13    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP2_AFSR     | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A6        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMII1_RD2      | 6            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_41        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII_REF_CLK    | 8            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM4_A       | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CS0        | 10           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_CTSn      | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART7_RXD       | 13           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| U24          | MCASP0_AXR14<br>PADCFG:<br>PADCONFIG_42<br>0x0011C0A8        | MCAN8_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR14    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP2_AXR4     | 2            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP0_ACLKR    | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A7        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMII1_RD3      | 6            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_42        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | CLKOUT          | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP0_A         | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_D0         | 10           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RTSn      | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AC25         | MCASP0_AXR15<br>PADCFG:<br>PADCONFIG_43<br>0x0011C0AC        | UART7_TXD       | 13           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCAN9_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR15    | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP0_AFSR     | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A8        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMII1_RX_CTL   | 6            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_43        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_TX_EN     | 8            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP0_B         | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_D1         | 10           | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART8_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SCL        | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| T28          | MCASP1_AXR0<br>PADCFG:<br>PADCONFIG_48<br>0x0011C0C0         | MCAN11_RX       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR0     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A13       | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MDIO0_MDC       | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_48        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CLK        | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP1_S         | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WAIT3     | 12           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SYNC2_OUT       | 14           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| V27          | MCASP1_AXR1<br>PADCFG:<br>PADCONFIG_19<br>0x0011C04C         | MCAN7_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR1     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA10    | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_RXPMCLK    | 3            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD8       | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_19        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_D0         | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN1  | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA8       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_CTSn      | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_RXD       | 12           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C2_SCL        | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
| W27          | MCASP1_AXR2<br>PADCFG:<br>PADCONFIG_20<br>0x0011C050         | MCAN8_TX        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR2     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA9     | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_RXPMDAT    | 3            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA21    | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD9       | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_20        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_D1         | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP2_B         | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA6       | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_RTSn      | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_TXD       | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C2_SDA        | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AD26         | MCASP1_AXR3<br>PADCFG:<br>PADCONFIG_44<br>0x0011C0B0         | MCAN9_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR3     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A9        | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMII1_RXC      | 6            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_44        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_TXD1      | 8            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP1_A         | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART8_TXD       | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SDA        | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
| U25          | MCASP1_AXR4<br>PADCFG:<br>PADCONFIG_45<br>0x0011C0B4         | MCAN10_TX       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR4     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A10       | 5            | OZ              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMII1_TXC      | 6            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_45        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP1_B         | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RXD       | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AA26         | MCASP2_AXR0<br>PADCFG:<br>PADCONFIG_23<br>0x0011C05C         | MCAN9_RX        | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_AXR0     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA6     | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_RXPMCLK    | 3            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD12      | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_23        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP2_I         | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA15      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART1_CTSn      | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_RXD       | 12           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AC27         | MCASP2_AXR1<br>PADCFG:<br>PADCONFIG_24<br>0x0011C060         | MCAN17_RX       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_AXR1     | 1            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA5     | 2            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_RXPMDAT    | 3            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD13      | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_24        | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM1_A       | 9            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA13      | 10           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART1_RTSn      | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_TXD       | 12           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C3_SDA        | 13           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| L25          | MCU_ADC0_AIN0<br>PADCFG:<br>WKUP_PADCONFIG_77<br>0x4301C134  | MCU_ADC0_AIN0   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_71   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| K25          | MCU_ADC0_AIN1<br>PADCFG:<br>WKUP_PADCONFIG_78<br>0x4301C138  | MCU_ADC0_AIN1   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_72   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| M24          | MCU_ADC0_AIN2<br>PADCFG:<br>WKUP_PADCONFIG_79<br>0x4301C13C  | MCU_ADC0_AIN2   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_73   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| L24          | MCU_ADC0_AIN3<br>PADCFG:<br>WKUP_PADCONFIG_80<br>0x4301C140  | MCU_ADC0_AIN3   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_74   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| L27          | MCU_ADC0_AIN4<br>PADCFG:<br>WKUP_PADCONFIG_81<br>0x4301C144  | MCU_ADC0_AIN4   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_75   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| K24          | MCU_ADC0_AIN5<br>PADCFG:<br>WKUP_PADCONFIG_82<br>0x4301C148  | MCU_ADC0_AIN5   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_76   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| M27          | MCU_ADC0_AIN6<br>PADCFG:<br>WKUP_PADCONFIG_83<br>0x4301C14C  | MCU_ADC0_AIN6   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_77   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| M26          | MCU_ADC0_AIN7<br>PADCFG:<br>WKUP_PADCONFIG_84<br>0x4301C150  | MCU_ADC0_AIN7   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_78   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| P25          | MCU_ADC1_AIN0<br>PADCFG:<br>WKUP_PADCONFIG_85<br>0x4301C154  | MCU_ADC1_AIN0   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC1  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_79   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| R25          | MCU_ADC1_AIN1<br>PADCFG:<br>WKUP_PADCONFIG_86<br>0x4301C158  | MCU_ADC1_AIN1   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC1  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_80   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| P28          | MCU_ADC1_AIN2<br>PADCFG:<br>WKUP_PADCONFIG_87<br>0x4301C15C  | MCU_ADC1_AIN2   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC1  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_81   | 7            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]      | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-----------------|----------|--------------------------|-------------|
| P27          | MCU_ADC1_AIN3<br>PADCFG:<br>WKUP_PADCONFIG_88<br>0x4301C160  | MCU_ADC1_AIN3   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC1       |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_82   | 7            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| N25          | MCU_ADC1_AIN4<br>PADCFG:<br>WKUP_PADCONFIG_89<br>0x4301C164  | MCU_ADC1_AIN4   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC1       |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_83   | 7            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| P26          | MCU_ADC1_AIN5<br>PADCFG:<br>WKUP_PADCONFIG_90<br>0x4301C168  | MCU_ADC1_AIN5   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC1       |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_84   | 7            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| N26          | MCU_ADC1_AIN6<br>PADCFG:<br>WKUP_PADCONFIG_91<br>0x4301C16C  | MCU_ADC1_AIN6   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC1       |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_85   | 7            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| N27          | MCU_ADC1_AIN7<br>PADCFG:<br>WKUP_PADCONFIG_92<br>0x4301C170  | MCU_ADC1_AIN7   | 0            | A               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_ADC1       |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_86   | 7            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| G24          | MCU_I2C0_SCL<br>PADCFG:<br>WKUP_PADCONFIG_66<br>0x4301C108   | MCU_I2C0_SCL    | 0            | IOD             | 1.8 V/3.3 V               | Off / Off / Off                          | On / SS / Off                           | 0                        |                | VDDSHV0_M<br>CU | Yes      | I2C OPEN<br>DRAIN        | Yes         |
|              |                                                              | WKUP_GPIO0_65   | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| J25          | MCU_I2C0_SDA<br>PADCFG:<br>WKUP_PADCONFIG_67<br>0x4301C10C   | MCU_I2C0_SDA    | 0            | IOD             | 1.8 V/3.3 V               | Off / Off / Off                          | On / SS / Off                           | 0                        |                | VDDSHV0_M<br>CU | Yes      | I2C OPEN<br>DRAIN        | Yes         |
|              |                                                              | WKUP_GPIO0_87   | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| E28          | MCU_MCAN0_RX<br>PADCFG:<br>WKUP_PADCONFIG_47<br>0x4301C0BC   | MCU_MCAN0_RX    | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_61   | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| E27          | MCU_MCAN0_TX<br>PADCFG:<br>WKUP_PADCONFIG_46<br>0x4301C0B8   | MCU_MCAN0_TX    | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_60   | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| A21          | MCU_MDIO0_MDC<br>PADCFG:<br>WKUP_PADCONFIG_39<br>0x4301C09C  | MCU_MDIO0_MDC   | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_53   | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| A22          | MCU_MDIO0_MDIO<br>PADCFG:<br>WKUP_PADCONFIG_38<br>0x4301C098 | MCU_MDIO0_MDIO  | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_52   | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16]              | Signal Name [3]                   | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|---------------------------------------------------------------------------|-----------------------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| D19          | MCU_OSPi0_CLK<br>PADCFG:<br>WKUP_PADCONFIG_0<br>0x4301C000                | MCU_OSPi0_CLK                     | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_CK                  | 1            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | WKUP_GPIO0_16                     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| E18          | MCU_OSPi0_DQS<br>PADCFG:<br>WKUP_PADCONFIG_2<br>0x4301C008                | MCU_OSPi0_DQS                     | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_RWDS                | 1            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | WKUP_GPIO0_18                     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| E20          | MCU_OSPi0_LBCLKO<br>PADCFG:<br>WKUP_PADCONFIG_1<br>0x4301C004             | MCU_OSPi0_LBCLKO                  | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_CK <sub>n</sub>     | 1            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | WKUP_GPIO0_17                     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| A19          | MCU_OSPi1_CLK<br>PADCFG:<br>WKUP_PADCONFIG_16<br>0x4301C040               | MCU_OSPi1_CLK                     | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                           | WKUP_GPIO0_31                     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| B19          | MCU_OSPi1_DQS<br>PADCFG:<br>WKUP_PADCONFIG_18<br>0x4301C048               | MCU_OSPi1_DQS                     | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_OSPi0_CS <sub>n</sub> 3       | 1            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | MCU_HYPERBUS0_INT <sub>n</sub>    | 2            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | MCU_OSPi0_ECC_FAIL                | 6            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | WKUP_GPIO0_33                     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| B20          | MCU_OSPi1_LBCLKO<br>PADCFG:<br>WKUP_PADCONFIG_17<br>0x4301C044            | MCU_OSPi1_LBCLKO                  | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_OSPi0_CS <sub>n</sub> 2       | 1            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | MCU_HYPERBUS0_RESETO <sub>n</sub> | 2            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | MCU_OSPi0_RESET_OUT0              | 6            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | WKUP_GPIO0_32                     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| F15          | MCU_OSPi0_CS <sub>n</sub> 0<br>PADCFG:<br>WKUP_PADCONFIG_11<br>0x4301C02C | MCU_OSPi0_CS <sub>n</sub> 0       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_CS <sub>n</sub> 0   | 1            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | WKUP_GPIO0_27                     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| G17          | MCU_OSPi0_CS <sub>n</sub> 1<br>PADCFG:<br>WKUP_PADCONFIG_12<br>0x4301C030 | MCU_OSPi0_CS <sub>n</sub> 1       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_RESETO <sub>n</sub> | 1            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | WKUP_GPIO0_28                     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| F14          | MCU_OSPi0_CS <sub>n</sub> 2<br>PADCFG:<br>WKUP_PADCONFIG_14<br>0x4301C038 | MCU_OSPi0_CS <sub>n</sub> 2       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_OSPi0_CS <sub>n</sub> 2       | 1            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | MCU_HYPERBUS0_RESETO <sub>n</sub> | 2            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | MCU_HYPERBUS0_WP <sub>n</sub>     | 3            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | MCU_HYPERBUS0_CS <sub>n</sub> 1   | 4            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | MCU_OSPi0_RESET_OUT0              | 6            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                           | WKUP_GPIO0_29                     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16]              | Signal Name [3]                | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]      | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|---------------------------------------------------------------------------|--------------------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-----------------|----------|--------------------------|-------------|
| F17          | MCU_OSPI0_CS <sub>n</sub> 3<br>PADCFG:<br>WKUP_PADCONFIG_15<br>0x4301C03C | MCU_OSPI0_CS <sub>n</sub> 3    | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_OSPI0_CS <sub>n</sub> 3    | 1            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | MCU_HYPERBUS0_INT <sub>n</sub> | 2            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | MCU_HYPERBUS0_WP <sub>n</sub>  | 3            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | MCU_OSPI0_RESET_OUT1           | 5            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | MCU_OSPI0_ECC_FAIL             | 6            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | WKUP_GPIO0_30                  | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| C19          | MCU_OSPI0_D0<br>PADCFG:<br>WKUP_PADCONFIG_3<br>0x4301C00C                 | MCU_OSPI0_D0                   | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_DQ0              | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | WKUP_GPIO0_19                  | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | BOOTMODE00                     | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| F16          | MCU_OSPI0_D1<br>PADCFG:<br>WKUP_PADCONFIG_4<br>0x4301C010                 | MCU_OSPI0_D1                   | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_DQ1              | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | WKUP_GPIO0_20                  | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | BOOTMODE01                     | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| G15          | MCU_OSPI0_D2<br>PADCFG:<br>WKUP_PADCONFIG_5<br>0x4301C014                 | MCU_OSPI0_D2                   | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_DQ2              | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | WKUP_GPIO0_21                  | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| F18          | MCU_OSPI0_D3<br>PADCFG:<br>WKUP_PADCONFIG_6<br>0x4301C018                 | MCU_OSPI0_D3                   | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_DQ3              | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | WKUP_GPIO0_22                  | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| E19          | MCU_OSPI0_D4<br>PADCFG:<br>WKUP_PADCONFIG_7<br>0x4301C01C                 | MCU_OSPI0_D4                   | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_DQ4              | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | WKUP_GPIO0_23                  | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | BOOTMODE02                     | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| G19          | MCU_OSPI0_D5<br>PADCFG:<br>WKUP_PADCONFIG_8<br>0x4301C020                 | MCU_OSPI0_D5                   | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_DQ5              | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | WKUP_GPIO0_24                  | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | BOOTMODE03                     | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| F19          | MCU_OSPI0_D6<br>PADCFG:<br>WKUP_PADCONFIG_9<br>0x4301C024                 | MCU_OSPI0_D6                   | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                           | MCU_HYPERBUS0_DQ6              | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                           | WKUP_GPIO0_25                  | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]      | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|----------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-----------------|----------|--------------------------|-------------|
| F20          | MCU_OSPiO_D7<br>PADCFG:<br>WKUP_PADCONFIG_10<br>0x4301C028   | MCU_OSPiO_D7         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_DQ7    | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | WKUP_GPIO0_26        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| D20          | MCU_OSPi1_CSn0<br>PADCFG:<br>WKUP_PADCONFIG_23<br>0x4301C05C | MCU_OSPi1_CSn0       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_38        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| C21          | MCU_OSPi1_CSn1<br>PADCFG:<br>WKUP_PADCONFIG_24<br>0x4301C060 | MCU_OSPi1_CSn1       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_WPn    | 1            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_TIMER_IO0        | 2            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_HYPERBUS0_CSn1   | 3            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_UART0_RTSn       | 4            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_SPI0_CS2         | 5            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_OSPi0_RESET_OUT1 | 6            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| D21          | MCU_OSPi1_D0<br>PADCFG:<br>WKUP_PADCONFIG_19<br>0x4301C04C   | MCU_OSPi1_D0         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_34        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| G20          | MCU_OSPi1_D1<br>PADCFG:<br>WKUP_PADCONFIG_20<br>0x4301C050   | MCU_OSPi1_D1         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_UART0_RXD        | 4            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_SPI1_CS1         | 5            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | WKUP_GPIO0_35        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| C20          | MCU_OSPi1_D2<br>PADCFG:<br>WKUP_PADCONFIG_21<br>0x4301C054   | MCU_OSPi1_D2         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_UART0_TXD        | 4            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_SPI1_CS2         | 5            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | WKUP_GPIO0_36        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| A20          | MCU_OSPi1_D3<br>PADCFG:<br>WKUP_PADCONFIG_22<br>0x4301C058   | MCU_OSPi1_D3         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_UART0_CTSn       | 4            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_SPI0_CS1         | 5            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | WKUP_GPIO0_37        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| G23          | MCU_PORz                                                     | MCU_PORz             |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_WKUP       | Yes      | FS_RESET                 | No          |
| A23          | MCU_RESETSTATz<br>PADCFG:<br>WKUP_PADCONFIG_71<br>0x4301C11C | MCU_RESETSTATz       | 0            | O               | 1.8 V/3.3 V               | Off / Low / Off                          | Off / SS / Off                          | 0                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_68        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| A26          | MCU_RESETz<br>PADCFG:<br>WKUP_PADCONFIG_70<br>0x4301C118     | MCU_RESETz           | 0            | I               | 1.8 V/3.3 V               | On / NA / Up                             | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | No          |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16]    | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]      | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|-----------------------------------------------------------------|----------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-----------------|----------|--------------------------|-------------|
| D22          | MCU_RGMII1_RXC<br>PADCFG:<br>WKUP_PADCONFIG_33<br>0x4301C084    | MCU_RGMII1_RXC       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_REF_CLK    | 1            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_47        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| E23          | MCU_RGMII1_RX_CTL<br>PADCFG:<br>WKUP_PADCONFIG_27<br>0x4301C06C | MCU_RGMII1_RX_CTL    | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_RX_ER      | 1            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_41        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| F21          | MCU_RGMII1_TXC<br>PADCFG:<br>WKUP_PADCONFIG_32<br>0x4301C080    | MCU_RGMII1_TXC       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_TX_EN      | 1            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_46        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| F22          | MCU_RGMII1_TX_CTL<br>PADCFG:<br>WKUP_PADCONFIG_26<br>0x4301C068 | MCU_RGMII1_TX_CTL    | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_CRS_DV     | 1            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_40        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| B22          | MCU_RGMII1_RD0<br>PADCFG:<br>WKUP_PADCONFIG_37<br>0x4301C094    | MCU_RGMII1_RD0       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_RXD0       | 1            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_51        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| B21          | MCU_RGMII1_RD1<br>PADCFG:<br>WKUP_PADCONFIG_36<br>0x4301C090    | MCU_RGMII1_RD1       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_RXD1       | 1            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_50        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| C22          | MCU_RGMII1_RD2<br>PADCFG:<br>WKUP_PADCONFIG_35<br>0x4301C08C    | MCU_RGMII1_RD2       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_TIMER_IO5        | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_62        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| D23          | MCU_RGMII1_RD3<br>PADCFG:<br>WKUP_PADCONFIG_34<br>0x4301C088    | MCU_RGMII1_RD3       | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_TIMER_IO4        | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_48        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| F23          | MCU_RGMII1_TD0<br>PADCFG:<br>WKUP_PADCONFIG_31<br>0x4301C07C    | MCU_RGMII1_TD0       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_TXD0       | 1            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_45        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| G22          | MCU_RGMII1_TD1<br>PADCFG:<br>WKUP_PADCONFIG_30<br>0x4301C078    | MCU_RGMII1_TD1       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_TXD1       | 1            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_44        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| E21          | MCU_RGMII1_TD2<br>PADCFG:<br>WKUP_PADCONFIG_29<br>0x4301C074    | MCU_RGMII1_TD2       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_TIMER_IO3        | 1            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | MCU_ADC_EXT_TRIGGER1 | 3            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_43        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16]    | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|-----------------------------------------------------------------|----------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| E22          | MCU_RGMII1_TD3<br>PADCFG:<br>WKUP_PADCONFIG_28<br>0x4301C070    | MCU_RGMII1_TD3       | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_TIMER_I02        | 1            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_ADC_EXT_TRIGGER0 | 3            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | WKUP_GPIO0_42        | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| J23          | MCU_SAFETY_ERRORn<br>PADCFG:<br>WKUP_PADCONFIG_69<br>0x4301C114 | MCU_SAFETY_ERRORn    | 0            | IO              | 1.8 V                     | Off / Off / Down                         | On / SS / Down                          | 0                        | PU/PD          | VDDA_WKUP   | Yes      | LVCMOS                   | No          |
| B27          | MCU_SPI0_CLK<br>PADCFG:<br>WKUP_PADCONFIG_40<br>0x4301C0A0      | MCU_SPI0_CLK         | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                                 | WKUP_GPIO0_54        | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_BOOTMODE00       | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| B26          | MCU_SPI0_CS0<br>PADCFG:<br>WKUP_PADCONFIG_43<br>0x4301C0AC      | MCU_SPI0_CS0         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                                 | MCU_TIMER_I01        | 4            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | WKUP_GPIO0_70        | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| D24          | MCU_SPI0_D0<br>PADCFG:<br>WKUP_PADCONFIG_41<br>0x4301C0A4       | MCU_SPI0_D0          | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                                 | WKUP_GPIO0_55        | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_BOOTMODE01       | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| B25          | MCU_SPI0_D1<br>PADCFG:<br>WKUP_PADCONFIG_42<br>0x4301C0A8       | MCU_SPI0_D1          | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                                 | MCU_TIMER_I00        | 4            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | WKUP_GPIO0_69        | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_BOOTMODE02       | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| AF1          | MMC0_CALPAD                                                     | MMC0_CALPAD          |              | A               | 1.8 V                     |                                          |                                         |                          | PU/PD          | VDDS_MMC0   |          | eMMC PHY                 | No          |
| AC6          | MMC0_CLK                                                        | MMC0_CLK             |              | O               | 1.8 V                     | On / Low / Off                           | On / SS / Off                           |                          | PU/PD          | VDDS_MMC0   |          | eMMC PHY                 | No          |
| AF2          | MMC0_CMD                                                        | MMC0_CMD             |              | IO              | 1.8 V                     | On / Off / Up                            | On / SS / Up                            |                          | PU/PD          | VDDS_MMC0   |          | eMMC PHY                 | No          |
| AE3          | MMC0_DS                                                         | MMC0_DS              |              | IO              | 1.8 V                     | On / Off / Down                          | On / Off / Down                         |                          | PU/PD          | VDDS_MMC0   |          | eMMC PHY                 | No          |
| P23          | MMC1_CLK<br>PADCFG:<br>PADCONFIG_65<br>0x0011C104               | MMC1_CLK             | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5     | Yes      | SDIO                     | No          |
|              |                                                                 | UART8_RXD            | 1            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | TIMER_I06            | 3            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | EHRPWM2_B            | 4            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | UART4_CTSn           | 5            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | EHRPWM5_A            | 6            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | GPIO0_64             | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | SPI1_CLK             | 8            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | UART0_RTSn           | 9            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | I2C6_SDA             | 10           | IOD             |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCAN15_TX            | 11           | O               |                           |                                          |                                         |                          |                |             |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| N24          | MMC1_CMD<br>PADCFG:<br>PADCONFIG_66<br>0x0011C108            | MMC1_CMD          | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART8_TXD         | 1            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO7         | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM2_A         | 4            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RTSn        | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_65          | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_D1           | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C6_SCL          | 10           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCAN15_RX         | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| AF4          | MMC0_DAT0                                                    | MMC0_DAT0         |              | IO              | 1.8 V                     | On / Off / Up                            | On / SS / Up                            |                          | PU/PD          | VDDS_MMC0  |          | eMMC PHY                 | No          |
| AD3          | MMC0_DAT1                                                    | MMC0_DAT1         |              | IO              | 1.8 V                     | On / Off / Up                            | On / SS / Up                            |                          | PU/PD          | VDDS_MMC0  |          | eMMC PHY                 | No          |
| AD4          | MMC0_DAT2                                                    | MMC0_DAT2         |              | IO              | 1.8 V                     | On / Off / Up                            | On / SS / Up                            |                          | PU/PD          | VDDS_MMC0  |          | eMMC PHY                 | No          |
| AF3          | MMC0_DAT3                                                    | MMC0_DAT3         |              | IO              | 1.8 V                     | On / Off / Up                            | On / SS / Up                            |                          | PU/PD          | VDDS_MMC0  |          | eMMC PHY                 | No          |
| AE2          | MMC0_DAT4                                                    | MMC0_DAT4         |              | IO              | 1.8 V                     | On / Off / Up                            | On / SS / Up                            |                          | PU/PD          | VDDS_MMC0  |          | eMMC PHY                 | No          |
| AG3          | MMC0_DAT5                                                    | MMC0_DAT5         |              | IO              | 1.8 V                     | On / Off / Up                            | On / SS / Up                            |                          | PU/PD          | VDDS_MMC0  |          | eMMC PHY                 | No          |
| AE1          | MMC0_DAT6                                                    | MMC0_DAT6         |              | IO              | 1.8 V                     | On / Off / Up                            | On / SS / Up                            |                          | PU/PD          | VDDS_MMC0  |          | eMMC PHY                 | No          |
| AG1          | MMC0_DAT7                                                    | MMC0_DAT7         |              | IO              | 1.8 V                     | On / Off / Up                            | On / SS / Up                            |                          | PU/PD          | VDDS_MMC0  |          | eMMC PHY                 | No          |
| M23          | MMC1_DAT0<br>PADCFG:<br>PADCONFIG_63<br>0x0011C0FC           | MMC1_DAT0         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART7_RTSn        | 1            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | ECAP1_IN_APWM_OUT | 2            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO5         | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM1_A         | 4            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_TXD         | 5            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_63          | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_D0           | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RTSn        | 9            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SCL          | 10           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_TXD         | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| P24          | MMC1_DAT1<br>PADCFG:<br>PADCONFIG_62<br>0x0011C0F8           | MMC1_DAT1         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART7_CTSn        | 1            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | ECAP0_IN_APWM_OUT | 2            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO4         | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM1_B         | 4            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RXD         | 5            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM4_A         | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_62          | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_CS2          | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_CTSn        | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SDA          | 10           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_RXD         | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| R24          | MMC1_DAT2<br>PADCFG:<br>PADCONFIG_61<br>0x0011C0F4           | MMC1_DAT2         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART7_TXD         | 1            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO3         | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_A         | 4            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_61          | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_CS1          | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | CPTS0_TS_SYNC     | 9            | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C3_SDA          | 10           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_TXD         | 11           | O               |                           |                                          |                                         |                          |                |            |          |                          |             |
| R22          | MMC1_DAT3<br>PADCFG:<br>PADCONFIG_60<br>0x0011C0F0           | MMC1_DAT3         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART7_RXD         | 1            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | PCIE1_CLKREQn     | 2            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO2         | 3            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_B         | 4            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_A         | 6            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_60          | 7            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_CS0          | 8            | IO              |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_CTSn        | 9            | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C3_SCL          | 10           | IOD             |                           |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RXD         | 11           | I               |                           |                                          |                                         |                          |                |            |          |                          |             |
| M28          | OSC1_XI                                                      | OSC1_XI           |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_OSC1  | Yes      | HFXOSC                   |             |
| L28          | OSC1_XO                                                      | OSC1_XO           |              | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_OSC1  | Yes      | HFXOSC                   |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]    | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|--------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AH10         | PCIE_REFCLK1_N_OUT                                           | PCIE_REFCLK1_N_OUT |              | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AH11         | PCIE_REFCLK1_P_OUT                                           | PCIE_REFCLK1_P_OUT |              | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| G26          | PMIC_POWER_EN1<br>PADCFG:<br>WKUP_PADCONFIG_68<br>0x4301C110 | PMIC_POWER_EN1     | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU                                                                     | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_I3C0_SDAPULLEN | 5            | OD              |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | WKUP_GPIO0_88      | 7            | IO              |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AD24         | PMIC_WAKE0<br>PADCFG:<br>PADCONFIG_13<br>0x0011C034          | PMIC_WAKE0         | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2                                                                             | Yes      | LVCMOS                   | No          |
|              |                                                              | MCASP4_AXR0        | 1            | IO              |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | DSS_FSYNC1         | 4            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | MCAN17_RX          | 5            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | GPMC0_WEn          | 6            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | GPIO0_13           | 7            | IO              |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | SPI6_CS0           | 8            | IO              |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | TRC_DATA0          | 10           | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | UART9_RTSn         | 11           | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| K23          | PORz<br>PADCFG:<br>WKUP_PADCONFIG_94<br>0x4301C178           | PORz               | 0            | I               | 1.8 V                     |                                          |                                         | 0                        |                | VDDA_WKUP                                                                           | Yes      | FS_RESET                 | No          |
|              |                                                              |                    |              |                 |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              |                    |              |                 |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AF27         | RESETSTATz<br>PADCFG:<br>PADCONFIG_67<br>0x0011C10C          | RESETSTATz         | 0            | O               | 1.8 V/3.3 V               | Off / Low / Off                          | Off / SS / Off                          | 0                        | PU/PD          | VDDSHV0                                                                             | Yes      | LVCMOS                   | No          |
| A24          | RESET_REQz<br>PADCFG:<br>WKUP_PADCONFIG_93<br>0x4301C174     | RESET_REQz         | 0            | I               | 1.8 V/3.3 V               | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_M<br>CU                                                                     | Yes      | LVCMOS                   | No          |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]  | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AH4          | SERDES0_REFCLK_N                                             | SERDES0_REFCLK_N | 0            | IO              | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AH5          | SERDES0_REFCLK_P                                             | SERDES0_REFCLK_P | 0            | IO              | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AC10         | SERDES0_REXT                                                 | SERDES0_REXT     |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AF9          | SERDES0_RX0_N                                                | PCIE1_RXN0       | 1            | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX1N      | 2            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXN0         | 4            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AF10         | SERDES0_RX0_P                                                | PCIE1_RXP0       | 1            | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX1P      | 2            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXP0         | 4            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AE8          | SERDES0_RX1_N                                                | PCIE1_RXN1       | 1            | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX2N      | 2            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXN1         | 4            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AE9          | SERDES0_RX1_P                                                | PCIE1_RXP1       | 1            | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX2P      | 2            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXP1         | 4            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AF6          | SERDES0_RX2_N                                                | PCIE1_RXN2      | 1            | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX1N     | 2            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXN2        | 4            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AF7          | SERDES0_RX2_P                                                | PCIE1_RXP2      | 1            | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX1P     | 2            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXP2        | 4            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AE5          | SERDES0_RX3_N                                                | PCIE1_RXN3      | 1            | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX2N     | 2            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXN3        | 4            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AE6          | SERDES0_RX3_P                                                | PCIE1_RXP3      | 1            | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX2P     | 2            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXP3        | 4            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AH7          | SERDES0_TX0_N                                                | DP0_TXN0        | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_TXN0      | 1            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSTX1N     | 2            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXN0        | 4            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AH8          | SERDES0_TX0_P                                                | DP0_TXP0        | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_TXP0      | 1            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSTX1P     | 2            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXP0        | 4            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AG8          | SERDES0_TX1_N                                                | DP0_TXN1        | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_TXN1      | 1            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSTX2N     | 2            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXN1        | 4            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AG9          | SERDES0_TX1_P                                                | DP0_TXP1          | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_TXP1        | 1            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSTX2P       | 2            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXP1          | 4            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AG5          | SERDES0_TX2_N                                                | DP0_TXN2          | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_TXN2        | 1            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSTX1N       | 2            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | DP0_TXN0          | 3            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXN2          | 4            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AG6          | SERDES0_TX2_P                                                | DP0_TXP2          | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_TXP2        | 1            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSTX1P       | 2            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | DP0_TXP0          | 3            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXP2          | 4            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AD7          | SERDES0_TX3_N                                                | DP0_TXN3          | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_TXN3        | 1            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSTX2N       | 2            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | DP0_TXN1          | 3            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXN3          | 4            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AD8          | SERDES0_TX3_P                                                | DP0_TXP3          | 0            | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_TXP3        | 1            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSTX2P       | 2            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | DP0_TXP1          | 3            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXP3          | 4            | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AF25         | SOC_SAFETY_ERRORn<br>PADCFG:<br>PADCONFIG_68<br>0x0011C110   | SOC_SAFETY_ERRORn | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Down                         | On / SS / Down                          | 0                        | PU/PD          | VDDSHV0                                                                             | Yes      | LVC MOS                  | No          |
| AH27         | SPIO_CLK<br>PADCFG:<br>PADCONFIG_53<br>0x0011C0D4            | SPIO_CLK          | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0                                                                             | Yes      | LVC MOS                  | No          |
|              |                                                              | UART1_CTSn        | 1            | I               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | I2C2_SCL          | 2            | IOD             |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | MCASP3_AXR0       | 3            | IO              |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | EHRPWM2_A         | 5            | IO              |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | GPIO0_53          | 7            | IO              |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | UART8_TXD         | 11           | O               |                           |                                          |                                         |                          |                |                                                                                     |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]      | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-----------------|----------|--------------------------|-------------|
| AE27         | SPI0_CS0<br>PADCFG:<br>PADCONFIG_51<br>0x0011C0CC            | SPI0_CS0        | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0         | Yes      | LVCMOS                   | No          |
|              |                                                              | MCASP3_ACLKX    | 3            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCASP3_ACLKR    | 4            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | EHRPWM0_A       | 5            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | GPIO0_51        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCAN14_TX       | 9            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| AF26         | SPI0_CS1<br>PADCFG:<br>PADCONFIG_52<br>0x0011C0D0            | SPI0_CS1        | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0         | Yes      | LVCMOS                   | No          |
|              |                                                              | CPTS0_TS_COMP   | 1            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | UART0_RTSn      | 2            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCASP3_AFSX     | 3            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCASP3_AFSR     | 4            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | EHRPWM1_A       | 5            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | GPIO0_52        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCAN14_RX       | 9            | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| AG26         | SPI0_D0<br>PADCFG:<br>PADCONFIG_54<br>0x0011C0D8             | UART8_RXD       | 11           | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0         | Yes      | LVCMOS                   | No          |
|              |                                                              | SPI0_D0         | 0            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | UART1_RTSn      | 1            | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | I2C2_SDA        | 2            | IOD             |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCASP3_AXR1     | 3            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | EHRPWM3_A       | 5            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | GPIO0_54        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| AH26         | SPI0_D1<br>PADCFG:<br>PADCONFIG_55<br>0x0011C0DC             | UART2_RXD       | 11           | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0         | Yes      | LVCMOS                   | No          |
|              |                                                              | SPI0_D1         | 0            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCASP3_AXR2     | 3            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | EHRPWM4_A       | 5            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | GPIO0_55        | 7            | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| A25          | TCK<br>PADCFG:<br>WKUP_PADCONFIG_73<br>0x4301C124            | TCK             | 0            | I               | 1.8 V/3.3 V               | On / NA / Up                             | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | No          |
| AG28         | TDI<br>PADCFG:<br>PADCONFIG_69<br>0x0011C114                 | TDI             | 0            | I               | 1.8 V/3.3 V               | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0         | Yes      | LVCMOS                   | No          |
| AE26         | TDO<br>PADCFG:<br>PADCONFIG_70<br>0x0011C118                 | TDO             | 0            | OZ              | 1.8 V/3.3 V               | Off / Off / Up                           | Off / SS / Up                           | 0                        | PU/PD          | VDDSHV0         | Yes      | LVCMOS                   | No          |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                   | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------------------------------------------|----------|--------------------------|-------------|
| AE25         | TIMER_IO0<br>PADCFG:<br>PADCONFIG_58<br>0x0011C0E8           | TIMER_IO0         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0                                                      | Yes      | LVCMOS                   | No          |
|              |                                                              | ECAP1_IN_APWM_OUT | 1            | IO              |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | SYSCLKOUT0        | 2            | O               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | UART3_RXD         | 5            | I               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | PCIE1_CLKREQn     | 6            | IO              |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | GPIO0_58          | 7            | IO              |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | MMC1_SDCD         | 8            | I               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | MCAN13_TX         | 9            | O               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | I2C6_SDA          | 13           | IOD             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AG25         | TIMER_IO1<br>PADCFG:<br>PADCONFIG_59<br>0x0011C0EC           | TIMER_IO1         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0                                                      | Yes      | LVCMOS                   | No          |
|              |                                                              | ECAP2_IN_APWM_OUT | 1            | IO              |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | OBSClk0           | 2            | O               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | UART3_TXD         | 5            | O               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | USB0_DRVVBUS      | 6            | O               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | GPIO0_59          | 7            | IO              |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | MMC1_SDWFP        | 8            | I               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | MCAN13_RX         | 9            | I               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | I2C6_SCL          | 13           | IOD             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
|              |                                                              | OBSClk0           | 15           | O               |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AG27         | TMS<br>PADCFG:<br>PADCONFIG_71<br>0x0011C11C                 | TMS               | 0            | I               | 1.8 V/3.3 V               | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0                                                      | Yes      | LVCMOS                   | No          |
| B28          | TRSTn<br>PADCFG:<br>WKUP_PADCONFIG_74<br>0x4301C128          | TRSTn             | 0            | I               | 1.8 V/3.3 V               | On / NA / Down                           | On / Off / Down                         | 0                        | PU/PD          | VDDSHV0_MCU                                                  | Yes      | LVCMOS                   | No          |
| AG2          | USB0_DM                                                      | USB0_DM           |              | IO              | 3.3 V                     |                                          |                                         |                          |                | VDDA_0P8_U<br>SB /<br>VDDA_1P8_U<br>SB /<br>VDDA_3P3_U<br>SB |          | USB2PHY                  |             |
| AH2          | USB0_DP                                                      | USB0_DP           |              | IO              | 3.3 V                     |                                          |                                         |                          |                | VDDA_0P8_U<br>SB /<br>VDDA_1P8_U<br>SB /<br>VDDA_3P3_U<br>SB |          | USB2PHY                  |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1]                 | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                   | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|------------------------------|--------------------------------------------------------------|----------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------------------------------------------|----------|--------------------------|-------------|
| AC9                          | USB0_ID                                                      | USB0_ID              |              | A               | 3.3 V                     |                                          |                                         |                          |                | VDDA_0P8_U<br>SB /<br>VDDA_1P8_U<br>SB /<br>VDDA_3P3_U<br>SB |          | USB2PHY                  |             |
| AA6                          | USB0_RCALIB                                                  | USB0_RCALIB          |              | A               | 3.3 V                     |                                          |                                         |                          |                | VDDA_0P8_U<br>SB /<br>VDDA_1P8_U<br>SB /<br>VDDA_3P3_U<br>SB |          | USB2PHY                  |             |
| AA8                          | USB0_VBUS                                                    | USB0_VBUS            |              | A               | 5.0 V                     |                                          |                                         |                          |                | VDDA_0P8_U<br>SB /<br>VDDA_1P8_U<br>SB /<br>VDDA_3P3_U<br>SB |          | DDR                      |             |
| N17, V11,<br>V16, Y20        | VDDAR_CORE                                                   | VDDAR_CORE           |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| H9, K14,<br>P11, P14,<br>V13 | VDDAR_CPU                                                    | VDDAR_CPU            |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| K17, K19                     | VDDAR_MCU                                                    | VDDAR_MCU            |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AB14                         | VDDA_0P8_DSITX                                               | VDDA_0P8_DSITX       |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AB15                         | VDDA_0P8_DSITX_C                                             | VDDA_0P8_DSITX_C     |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AB8                          | VDDA_0P8_USB                                                 | VDDA_0P8_USB         |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AB17, AB18                   | VDDA_0P8_CSIRX0_1                                            | VDDA_0P8_CSIRX0_1    |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| W7                           | VDDA_0P8_DLL_MMC0                                            | VDDA_0P8_DLL_MMC0    |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| P10                          | VDDA_0P8_PLL_DDR0                                            | VDDA_0P8_PLL_DDR0    |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| J14                          | VDDA_0P8_PLL_DDR1                                            | VDDA_0P8_PLL_DDR1    |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AB10, AB11                   | VDDA_0P8_SERDES0_1                                           | VDDA_0P8_SERDES0_1   |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AA10, AA11                   | VDDA_0P8_SERDES_C0_1                                         | VDDA_0P8_SERDES_C0_1 |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AA14, AA15                   | VDDA_1P8_DSITX                                               | VDDA_1P8_DSITX       |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AB7                          | VDDA_1P8_USB                                                 | VDDA_1P8_USB         |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AA17, AA19                   | VDDA_1P8_CSIRX0_1                                            | VDDA_1P8_CSIRX0_1    |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AA12                         | VDDA_1P8_SERDES0_1                                           | VDDA_1P8_SERDES0_1   |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AB13                         | VDDA_1P8_SERDES2_4                                           | VDDA_1P8_SERDES2_4   |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| AB9                          | VDDA_3P3_USB                                                 | VDDA_3P3_USB         |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| J21                          | VDDA_ADC0                                                    | VDDA_ADC0            |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| K21                          | VDDA_ADC1                                                    | VDDA_ADC1            |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| K22                          | VDDA_MCU_PLLGRP0                                             | VDDA_MCU_PLLGRP0     |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| J17                          | VDDA_MCU_TEMP                                                | VDDA_MCU_TEMP        |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |
| L21                          | VDDA_OSC1                                                    | VDDA_OSC1            |              | PWR             |                           |                                          |                                         |                          |                |                                                              |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1]                                                                   | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| U18                                                                            | VDDA_PLLGRP0                                                 | VDDA_PLLGRP0    |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| V19                                                                            | VDDA_PLLGRP1                                                 | VDDA_PLLGRP1    |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| Y11                                                                            | VDDA_PLLGRP2                                                 | VDDA_PLLGRP2    |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| N14                                                                            | VDDA_PLLGRP5                                                 | VDDA_PLLGRP5    |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| R12                                                                            | VDDA_PLLGRP6                                                 | VDDA_PLLGRP6    |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| R11                                                                            | VDDA_PLLGRP7                                                 | VDDA_PLLGRP7    |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| K12                                                                            | VDDA_PLLGRP8                                                 | VDDA_PLLGRP8    |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| T18                                                                            | VDDA_PLLGRP9                                                 | VDDA_PLLGRP9    |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| Y16                                                                            | VDDA_PLLGRP10                                                | VDDA_PLLGRP10   |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| Y18                                                                            | VDDA_PLLGRP12                                                | VDDA_PLLGRP12   |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| V12                                                                            | VDDA_PLLGRP13                                                | VDDA_PLLGRP13   |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| L20                                                                            | VDDA_POR_WKUP                                                | VDDA_POR_WKUP   |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| U19                                                                            | VDDA_TEMP0                                                   | VDDA_TEMP0      |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| K10                                                                            | VDDA_TEMP1                                                   | VDDA_TEMP1      |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| T16                                                                            | VDDA_TEMP2                                                   | VDDA_TEMP2      |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| U10                                                                            | VDDA_TEMP3                                                   | VDDA_TEMP3      |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| Y14                                                                            | VDDA_TEMP4                                                   | VDDA_TEMP4      |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| J22                                                                            | VDDA_WKUP                                                    | VDDA_WKUP       |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| R21, U21, U22                                                                  | VDDSHV0                                                      | VDDSHV0         |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| H19, H20                                                                       | VDDSHV0_MCU                                                  | VDDSHV0_MCU     |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| H16, J16                                                                       | VDDSHV1_MCU                                                  | VDDSHV1_MCU     |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| M20, R20                                                                       | VDDSHV2                                                      | VDDSHV2         |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| G18, H18                                                                       | VDDSHV2_MCU                                                  | VDDSHV2_MCU     |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| M21, N22                                                                       | VDDSHV5                                                      | VDDSHV5         |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| A1, A18, AA1, G10, G12, G14, G6, H11, H13, H15, J6, L6, N6, N9, P7, P8, R6, U9 | VDDS_DDR                                                     | VDDS_DDR        |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| R9                                                                             | VDDS_DDR_C0                                                  | VDDS_DDR_C0     |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| J12                                                                            | VDDS_DDR_C1                                                  | VDDS_DDR_C1     |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |
| Y7, Y8                                                                         | VDDS_MMC0                                                    | VDDS_MMC0       |              | PWR             |                           |                                          |                                         |                          |                |            |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1]                                                                                                                                      | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]  | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|---------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| AA21, AB20, J13, J15, M16, M19, N10, P18, R17, R19, T10, T20, U15, U17, U8, V14, V18, V20, V7, V9, W10, W13, W15, W17, W19, W21, W8, Y12, Y22, Y9 | VDD_CORE                                                     | VDD_CORE         |              | PWR             |                           |                                          |                                         |                          |                |             |          |                          |             |
| G8, H7, J8, K11, K13, K7, K9, L8, M14, M7, M9, N11, N15, P16, R13, R15, T12, T14, U11, U13                                                        | VDD_CPU                                                      | VDD_CPU          |              | PWR             |                           |                                          |                                         |                          |                |             |          |                          |             |
| K16, K18, L15, L17, L19                                                                                                                           | VDD_MCU                                                      | VDD_MCU          |              | PWR             |                           |                                          |                                         |                          |                |             |          |                          |             |
| J19                                                                                                                                               | VDD_MCU_WAKE1                                                | VDD_MCU_WAKE1    |              | PWR             |                           |                                          |                                         |                          |                |             |          |                          |             |
| P20                                                                                                                                               | VDD_WAKE0                                                    | VDD_WAKE0        |              | PWR             |                           |                                          |                                         |                          |                |             |          |                          |             |
| H23                                                                                                                                               | VMON1_ER_VSYS                                                | VMON1_ER_VSYS    |              | A               |                           |                                          |                                         |                          |                |             |          |                          |             |
| M18                                                                                                                                               | VMON2_IR_VCPU                                                | VMON2_IR_VCPU    |              | A               |                           |                                          |                                         |                          |                |             |          |                          |             |
| L22                                                                                                                                               | VMON3_IR_VEXT1P8                                             | VMON3_IR_VEXT1P8 |              | A               |                           |                                          |                                         |                          |                |             |          |                          |             |
| N19                                                                                                                                               | VMON4_IR_VEXT1P8                                             | VMON4_IR_VEXT1P8 |              | A               |                           |                                          |                                         |                          |                |             |          |                          |             |
| N20                                                                                                                                               | VMON5_IR_VEXT3P3                                             | VMON5_IR_VEXT3P3 |              | A               |                           |                                          |                                         |                          |                |             |          |                          |             |
| L18                                                                                                                                               | VMON6_IR_VEXT0P8                                             | VMON6_IR_VEXT0P8 |              | A               |                           |                                          |                                         |                          |                |             |          |                          |             |
| V22                                                                                                                                               | VPP_CORE                                                     | VPP_CORE         |              | PWR             |                           |                                          |                                         |                          |                |             |          |                          |             |
| H22                                                                                                                                               | VPP_MCU                                                      | VPP_MCU          |              | PWR             |                           |                                          |                                         |                          |                |             |          |                          |             |
| D26                                                                                                                                               | WKUP_GPIO0_0<br>PADCFG:<br>WKUP_PADCONFIG_48<br>0x4301C0C0   | MCU_SPI1_CLK     | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|                                                                                                                                                   |                                                              | MCU_SPI1_CLK     | 1            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                   |                                                              | WKUP_GPIO0_0     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                   |                                                              | MCU_BOOTMODE03   | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| E24                                                                                                                                               | WKUP_GPIO0_1<br>PADCFG:<br>WKUP_PADCONFIG_49<br>0x4301C0C4   | MCU_SPI1_D0      | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|                                                                                                                                                   |                                                              | MCU_SPI1_D0      | 1            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                   |                                                              | WKUP_GPIO0_1     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                   |                                                              | MCU_BOOTMODE04   | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|----------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| C28          | WKUP_GPIO0_2<br>PADCFG:<br>WKUP_PADCONFIG_50<br>0x4301C0C8   | MCU_SPI1_D1          | 0            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_SPI1_D1          | 1            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_2         | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_BOOTMODE05       | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| C27          | WKUP_GPIO0_3<br>PADCFG:<br>WKUP_PADCONFIG_51<br>0x4301C0CC   | MCU_SPI1_CS0         | 0            | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_SPI1_CS0         | 1            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_3         | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| C23          | WKUP_GPIO0_4<br>PADCFG:<br>WKUP_PADCONFIG_52<br>0x4301C0D0   | MCU_MCAN1_TX         | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_MCAN1_TX         | 1            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_SPI0_CS3         | 2            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_ADC_EXT_TRIGGER0 | 3            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_4         | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| F26          | WKUP_GPIO0_5<br>PADCFG:<br>WKUP_PADCONFIG_53<br>0x4301C0D4   | MCU_MCAN1_RX         | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_MCAN1_RX         | 1            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_SPI1_CS3         | 2            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_ADC_EXT_TRIGGER1 | 3            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_5         | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| E25          | WKUP_GPIO0_6<br>PADCFG:<br>WKUP_PADCONFIG_54<br>0x4301C0D8   | WKUP_UART0_CTSn      | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_UART0_CTSn      | 1            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CPTS0_HW1TSPUSH  | 2            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I2C1_SCL         | 3            | IOD             |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_6         | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| F28          | WKUP_GPIO0_7<br>PADCFG:<br>WKUP_PADCONFIG_55<br>0x4301C0DC   | WKUP_UART0_RTSn      | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_UART0_RTSn      | 1            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CPTS0_HW2TSPUSH  | 2            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I2C1_SDA         | 3            | IOD             |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_7         | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| F24          | WKUP_GPIO0_8<br>PADCFG:<br>WKUP_PADCONFIG_56<br>0x4301C0E0   | MCU_I2C1_SCL         | 0            | IOD             | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_I2C1_SCL         | 1            | IOD             |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CPTS0_TS_SYNC    | 2            | O               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I3C0_SCL         | 3            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_TIMER_JO6        | 4            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_8         | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]      | Mux Mode [4]  | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]      | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|----------------------|---------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-----------------|----------|--------------------------|-------------|
| H26          | WKUP_GPIO0_9<br>PADCFG:<br>WKUP_PADCONFIG_57<br>0x4301C0E4   | MCU_I2C1_SDA         | 0             | IOD             | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_I2C1_SDA         | 1             | IOD             |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_CPTS0_TS_COMP    | 2             | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_I3C0_SDA         | 3             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_TIMER_IO7        | 4             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | WKUP_GPIO0_9         | 7             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| F27          | WKUP_GPIO0_10<br>PADCFG:<br>WKUP_PADCONFIG_58<br>0x4301C0E8  | MCU_EXT_REFCLK0      | 0             | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_EXT_REFCLK0      | 1             | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_UART0_TXD        | 2             | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_ADC_EXT_TRIGGER0 | 3             | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_CPTS0_RFT_CLK    | 4             | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_SYSCLKOUT0       | 5             | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
| F25          | WKUP_GPIO0_11<br>PADCFG:<br>WKUP_PADCONFIG_59<br>0x4301C0EC  | WKUP_GPIO0_10        | 7             | IO              | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_OBSCLK0          | 0             | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_OBSCLK0          | 1             | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_UART0_RXD        | 2             | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_ADC_EXT_TRIGGER1 | 3             | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_TIMER_IO1        | 4             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_I3C0_SDAPULLEN   | 5             | OD              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| C25          | WKUP_GPIO0_12<br>PADCFG:<br>WKUP_PADCONFIG_60<br>0x4301C0F0  | MCU_CLKOUT0          | 6             | OZ              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_11        | 7             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_UART0_TXD        | 0             | O               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_SPI0_CS1         | 1             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| C24          | WKUP_GPIO0_13<br>PADCFG:<br>WKUP_PADCONFIG_61<br>0x4301C0F4  | MCU_BOOTMODE08       | BOOTS<br>TRAP | I               | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_UART0_RXD        | 0             | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_SPI1_CS1         | 1             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | WKUP_GPIO0_13        | 7             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
| B24          | WKUP_GPIO0_14<br>PADCFG:<br>WKUP_PADCONFIG_62<br>0x4301C0F8  | MCU_BOOTMODE09       | BOOTS<br>TRAP | I               | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_UART0_CTSn       | 0             | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_SPI0_CS2         | 1             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_TIMER_IO8        | 4             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | WKUP_GPIO0_14        | 7             | IO              |                           |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_BOOTMODE06       | BOOTS<br>TRAP | I               |                           |                                          |                                         |                          |                |                 |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| D25          | WKUP_GPIO0_15<br>PADCFG:<br>WKUP_PADCONFIG_63<br>0x4301C0FC  | MCU_UART0_RTSn    | 0            | O               | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_SPI1_CS2      | 1            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_TIMER_I09     | 4            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_15     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_BOOTMODE07    | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| K26          | WKUP_GPIO0_49<br>PADCFG:<br>WKUP_PADCONFIG_100<br>0x4301C190 | PMIC_WAKE1        | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_EXT_REFCLK0   | 1            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CPTS0_RFT_CLK | 2            | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_49     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| G27          | WKUP_GPIO0_56<br>PADCFG:<br>WKUP_PADCONFIG_72<br>0x4301C120  | MCU_TIMER_I06     | 4            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_56     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | BOOTMODE04        | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| J26          | WKUP_GPIO0_57<br>PADCFG:<br>WKUP_PADCONFIG_95<br>0x4301C17C  | MCU_TIMER_I07     | 4            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_57     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | BOOTMODE05        | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| G25          | WKUP_GPIO0_66<br>PADCFG:<br>WKUP_PADCONFIG_96<br>0x4301C180  | WKUP_GPIO0_66     | 7            | IO              | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | BOOTMODE06        | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| J27          | WKUP_GPIO0_67<br>PADCFG:<br>WKUP_PADCONFIG_97<br>0x4301C184  | WKUP_LF_CLKIN     | 1            | I               | 1.8 V/3.3 V               | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_67     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | BOOTMODE07        | BOOTS TRAP   | I               |                           |                                          |                                         |                          |                |             |          |                          |             |
| H24          | WKUP_I2C0_SCL<br>PADCFG:<br>WKUP_PADCONFIG_64<br>0x4301C100  | WKUP_I2C0_SCL     | 0            | IOD             | 1.8 V/3.3 V               | Off / Off / Off                          | On / SS / Off                           | 0                        |                | VDDSHV0_MCU | Yes      | I2C OPEN DRAIN           | Yes         |
|              |                                                              | WKUP_GPIO0_63     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| H27          | WKUP_I2C0_SDA<br>PADCFG:<br>WKUP_PADCONFIG_65<br>0x4301C104  | WKUP_I2C0_SDA     | 0            | IOD             | 1.8 V/3.3 V               | Off / Off / Off                          | On / SS / Off                           | 0                        |                | VDDSHV0_MCU | Yes      | I2C OPEN DRAIN           | Yes         |
|              |                                                              | WKUP_GPIO0_64     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |
| H28          | WKUP_OSC0_XI                                                 | WKUP_OSC0_XI      |              | I               | 1.8 V                     |                                          |                                         |                          |                | VDDA_WKUP   | Yes      | HFXOSC                   | No          |
| J28          | WKUP_OSC0_XO                                                 | WKUP_OSC0_XO      |              | O               | 1.8 V                     |                                          |                                         |                          |                | VDDA_WKUP   | Yes      | HFXOSC                   | No          |
| D28          | WKUP_UART0_RXD<br>PADCFG:<br>WKUP_PADCONFIG_44<br>0x4301C0B0 | WKUP_UART0_RXD    | 0            | I               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_58     | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16]     | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|------------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| D27          | WKUP_UART0_TXD<br><br>PADCFG:<br>WKUP_PADCONFIG_45<br>0x4301C0B4 | WKUP_UART0_TXD  | 0            | O               | 1.8 V/3.3 V               | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                                  | WKUP_GPIO0_59   | 7            | IO              |                           |                                          |                                         |                          |                |             |          |                          |             |

Table 5-1. Pin Attributes (ALZ Package) (continued)

| Ball Num [1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| A14, A5,<br>AA13, AA16,<br>AA18, AA20,<br>AA22, AA3,<br>AA5, AA7,<br>AA9, AB12,<br>AB16, AB19,<br>AB2, AB21,<br>AB23, AB4,<br>AB6, AC11,<br>AC22,<br>AC26, AC3,<br>AC5, AC7,<br>AC8, AD15,<br>AD18,<br>AD21, AD6,<br>AD9, AE10,<br>AE14, AE17,<br>AE20, AE23,<br>AE4, AE7,<br>AF12, AF15,<br>AF18, AF21,<br>AF24, AF5,<br>AF8, AG10,<br>AG14,<br>AG17,<br>AG20,<br>AG23, AG4,<br>AG7, AH1,<br>AH12,<br>AH15,<br>AH18,<br>AH21,<br>AH24, AH3,<br>AH6, AH9,<br>B11, B13,<br>B15, B17,<br>B2, B23, B4,<br>B6, B8, C1,<br>C12, C14,<br>C16, C18,<br>C3, C5, C7,<br>D11, D13,<br>D15, D17,<br>D2, D4, D6,<br>D8, E1, E12,<br>E14, E16,<br>E26, E3, E5,<br>E7, F2, F4,<br>F6, G13,<br>G28, G3,<br>G5, G7, G9,<br>H10, H12,<br>H14, H2,<br>H21, H4,<br>H6, H8, J1,<br>J11, J18,<br>J24, J3, J5,<br>J7, J9, K15, | VSS                                                          | VSS             |              | GND             |                           |                                          |                                         |                          |                |            |          |                          |             |

**Table 5-1. Pin Attributes (ALZ Package) (continued)**

| Ball Num [1]                                                                                                                                                                                                                                                            | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Operating Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------|--------------|-----------------|---------------------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| K2, K20, K27, K4, K6, K8, L14, L16, L3, L5, L7, L9, M15, M17, M2, M25, M4, M6, M8, N1, N16, N18, N21, N23, N3, N7, P15, P17, P19, P22, P6                                                                                                                               |                                                              |                 |              |                 |                           |                                          |                                         |                          |                |            |          |                          |             |
| P9, R10, R14, R16, R18, R23, R26, R7, T11, T13, T15, T17, T19, T2, T22, T4, T6, T9, U12, U14, U16, U20, U23, U3, U5, U7, V10, V15, V17, V2, V21, V24, V4, V6, V8, W1, W11, W12, W14, W16, W18, W20, W22, W26, W3, W6, W9, Y10, Y13, Y15, Y17, Y19, Y2, Y21, Y23, Y4, Y6 | VSS (continued)                                              | VSS             |              | GND             |                           |                                          |                                         |                          |                |            |          |                          |             |

## 5.3 Signal Descriptions

1. **SIGNAL NAME:** The name of the signal passing through the pin.

### Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via PADCONFIG registers. Device subsystems may provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:

- I = Input
- O = Output
- OD = Output, with open-drain output function
- IO = Input, Output, or simultaneously Input and Output
- IOD = Input, Output, or simultaneously Input and Output with open-drain output function
- IOZ = Input, Output, or simultaneously Input and Output with three-state output function
- OZ = Output with three-state output function
- A = Analog
- PWR = Power
- GND = Ground
- CAP = LDO Capacitor

3. **DESCRIPTION:** Description of the signal

4. **BALL:** Ball number(s) associated with signal

For more information on the IO cell configurations, see the *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM.

### 5.3.1 ADC

#### 5.3.1.1 MCU Domain

**Table 5-2. MCU\_ADC Signal Descriptions**

| SIGNAL NAME [1]      | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4]   |
|----------------------|--------------|-------------------|---------------|
| MCU_ADC_EXT_TRIGGER0 | I            | ADC Trigger Input | C23, E22, F27 |
| MCU_ADC_EXT_TRIGGER1 | I            | ADC Trigger Input | E21, F25, F26 |

**Table 5-3. MCU\_ADC0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_ADC0_AIN0   | A            | ADC Input 0     | L25         |
| MCU_ADC0_AIN1   | A            | ADC Input 1     | K25         |
| MCU_ADC0_AIN2   | A            | ADC Input 2     | M24         |
| MCU_ADC0_AIN3   | A            | ADC Input 3     | L24         |
| MCU_ADC0_AIN4   | A            | ADC Input 4     | L27         |
| MCU_ADC0_AIN5   | A            | ADC Input 5     | K24         |
| MCU_ADC0_AIN6   | A            | ADC Input 6     | M27         |
| MCU_ADC0_AIN7   | A            | ADC Input 7     | M26         |

**Table 5-4. MCU\_ADC1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_ADC1_AIN0   | A            | ADC Input 0     | P25         |

**Table 5-4. MCU\_ADC1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_ADC1_AIN1   | A            | ADC Input 1     | R25         |
| MCU_ADC1_AIN2   | A            | ADC Input 2     | P28         |
| MCU_ADC1_AIN3   | A            | ADC Input 3     | P27         |
| MCU_ADC1_AIN4   | A            | ADC Input 4     | N25         |
| MCU_ADC1_AIN5   | A            | ADC Input 5     | P26         |
| MCU_ADC1_AIN6   | A            | ADC Input 6     | N26         |
| MCU_ADC1_AIN7   | A            | ADC Input 7     | N27         |

### 5.3.2 DDRSS

#### 5.3.2.1 MAIN Domain

**Table 5-5. DDRSS0 Signal Descriptions**

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                     | ALZ PIN [4] |
|--------------------------------|--------------|-------------------------------------|-------------|
| DDR0_CKN                       | IO           | DDRSS Differential Clock (negative) | R1          |
| DDR0_CKP                       | IO           | DDRSS Differential Clock (positive) | P1          |
| DDR0_RESETh                    | IO           | DDRSS Reset                         | R5          |
| DDR0_RET                       | I            | DDR Retention Enable                | T8          |
| DDR0_CA0                       | IO           | DDRSS Command Address               | P3          |
| DDR0_CA1                       | IO           | DDRSS Command Address               | P5          |
| DDR0_CA2                       | IO           | DDRSS Command Address               | N5          |
| DDR0_CA3                       | IO           | DDRSS Command Address               | P2          |
| DDR0_CA4                       | IO           | DDRSS Command Address               | P4          |
| DDR0_CA5                       | IO           | DDRSS Command Address               | R3          |
| DDR0_CAL0 <sup>(1)</sup>       | A            | IO Pad Calibration Resistor         | R8          |
| DDR0_CKE0                      | IO           | DDRSS Clock Enable                  | R2          |
| DDR0_CKE1                      | IO           | DDRSS Clock Enable                  | R4          |
| DDR0_CSn0_0                    | IO           | DDRSS Chip Select                   | V5          |
| DDR0_CSn0_1                    | IO           | DDRSS Chip Select                   | W5          |
| DDR0_CSn1_0                    | IO           | DDRSS Chip Select                   | T5          |
| DDR0_CSn1_1                    | IO           | DDRSS Chip Select                   | U6          |
| DDR0_DM0                       | IO           | DDRSS Data Mask                     | H5          |
| DDR0_DM1                       | IO           | DDRSS Data Mask                     | M3          |
| DDR0_DM2                       | IO           | DDRSS Data Mask                     | U4          |
| DDR0_DM3                       | IO           | DDRSS Data Mask                     | AD1         |
| DDR0_DQ0                       | IO           | DDRSS Data                          | F3          |
| DDR0_DQ1                       | IO           | DDRSS Data                          | G4          |
| DDR0_DQ2                       | IO           | DDRSS Data                          | F5          |
| DDR0_DQ3                       | IO           | DDRSS Data                          | F1          |
| DDR0_DQ4                       | IO           | DDRSS Data                          | J4          |
| DDR0_DQ5                       | IO           | DDRSS Data                          | H3          |
| DDR0_DQ6                       | IO           | DDRSS Data                          | J2          |
| DDR0_DQ7                       | IO           | DDRSS Data                          | G2          |
| DDR0_DQ8                       | IO           | DDRSS Data                          | K5          |
| DDR0_DQ9                       | IO           | DDRSS Data                          | M5          |
| DDR0_DQ10                      | IO           | DDRSS Data                          | K3          |
| DDR0_DQ11                      | IO           | DDRSS Data                          | K1          |

**Table 5-5. DDRSS0 Signal Descriptions (continued)**

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                 | ALZ PIN [4] |
|--------------------------------|--------------|---------------------------------|-------------|
| DDR0_DQ12                      | IO           | DDRSS Data                      | N4          |
| DDR0_DQ13                      | IO           | DDRSS Data                      | N2          |
| DDR0_DQ14                      | IO           | DDRSS Data                      | L4          |
| DDR0_DQ15                      | IO           | DDRSS Data                      | L2          |
| DDR0_DQ16                      | IO           | DDRSS Data                      | T1          |
| DDR0_DQ17                      | IO           | DDRSS Data                      | T3          |
| DDR0_DQ18                      | IO           | DDRSS Data                      | V3          |
| DDR0_DQ19                      | IO           | DDRSS Data                      | U2          |
| DDR0_DQ20                      | IO           | DDRSS Data                      | W2          |
| DDR0_DQ21                      | IO           | DDRSS Data                      | W4          |
| DDR0_DQ22                      | IO           | DDRSS Data                      | Y1          |
| DDR0_DQ23                      | IO           | DDRSS Data                      | Y3          |
| DDR0_DQ24                      | IO           | DDRSS Data                      | AB3         |
| DDR0_DQ25                      | IO           | DDRSS Data                      | AA2         |
| DDR0_DQ26                      | IO           | DDRSS Data                      | AA4         |
| DDR0_DQ27                      | IO           | DDRSS Data                      | Y5          |
| DDR0_DQ28                      | IO           | DDRSS Data                      | AC2         |
| DDR0_DQ29                      | IO           | DDRSS Data                      | AB5         |
| DDR0_DQ30                      | IO           | DDRSS Data                      | AD2         |
| DDR0_DQ31                      | IO           | DDRSS Data                      | AC4         |
| DDR0_QS0N                      | IO           | DDRSS Complimentary Data Strobe | H1          |
| DDR0_QS0P                      | IO           | DDRSS Data Strobe               | G1          |
| DDR0_QS1N                      | IO           | DDRSS Complimentary Data Strobe | M1          |
| DDR0_QS1P                      | IO           | DDRSS Data Strobe               | L1          |
| DDR0_QS2N                      | IO           | DDRSS Complimentary Data Strobe | U1          |
| DDR0_QS2P                      | IO           | DDRSS Data Strobe               | V1          |
| DDR0_QS3N                      | IO           | DDRSS Complimentary Data Strobe | AC1         |
| DDR0_QS3P                      | IO           | DDRSS Data Strobe               | AB1         |

(1) An external 240  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

(2) DDRSS0 and DDRSS1 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0\_\* interface. When using two LPDDR components, they must be connected to DDR0\_\* and DDR1\_\* interfaces.

**Table 5-6. DDRSS1 Signal Descriptions**

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                     | ALZ PIN [4] |
|--------------------------------|--------------|-------------------------------------|-------------|
| DDR1_CKN                       | IO           | DDRSS Differential Clock (negative) | A9          |
| DDR1_CKP                       | IO           | DDRSS Differential Clock (positive) | A10         |
| DDR1_RESETh                    | IO           | DDRSS Reset                         | F12         |
| DDR1_RET                       | I            | DDR Retention Enable                | J10         |
| DDR1_CA0                       | IO           | DDRSS Command Address               | C10         |
| DDR1_CA1                       | IO           | DDRSS Command Address               | E10         |
| DDR1_CA2                       | IO           | DDRSS Command Address               | E9          |
| DDR1_CA3                       | IO           | DDRSS Command Address               | B10         |
| DDR1_CA4                       | IO           | DDRSS Command Address               | D10         |
| DDR1_CA5                       | IO           | DDRSS Command Address               | C9          |
| DDR1_CAL0 <sup>(1)</sup>       | A            | IO Pad Calibration Resistor         | E8          |
| DDR1_CKE0                      | IO           | DDRSS Clock Enable                  | B9          |

**Table 5-6. DDRSS1 Signal Descriptions (continued)**

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                 | ALZ PIN [4] |
|--------------------------------|--------------|---------------------------------|-------------|
| DDR1_CKE1                      | IO           | DDRSS Clock Enable              | D9          |
| DDR1_CSn0_0                    | IO           | DDRSS Chip Select               | F9          |
| DDR1_CSn0_1                    | IO           | DDRSS Chip Select               | F8          |
| DDR1_CSn1_0                    | IO           | DDRSS Chip Select               | F11         |
| DDR1_CSn1_1                    | IO           | DDRSS Chip Select               | F10         |
| DDR1_DM0                       | IO           | DDRSS Data Mask                 | D16         |
| DDR1_DM1                       | IO           | DDRSS Data Mask                 | E13         |
| DDR1_DM2                       | IO           | DDRSS Data Mask                 | F7          |
| DDR1_DM3                       | IO           | DDRSS Data Mask                 | B3          |
| DDR1_DQ0                       | IO           | DDRSS Data                      | B18         |
| DDR1_DQ1                       | IO           | DDRSS Data                      | E17         |
| DDR1_DQ2                       | IO           | DDRSS Data                      | D18         |
| DDR1_DQ3                       | IO           | DDRSS Data                      | A17         |
| DDR1_DQ4                       | IO           | DDRSS Data                      | E15         |
| DDR1_DQ5                       | IO           | DDRSS Data                      | B16         |
| DDR1_DQ6                       | IO           | DDRSS Data                      | C15         |
| DDR1_DQ7                       | IO           | DDRSS Data                      | C17         |
| DDR1_DQ8                       | IO           | DDRSS Data                      | B14         |
| DDR1_DQ9                       | IO           | DDRSS Data                      | D14         |
| DDR1_DQ10                      | IO           | DDRSS Data                      | C13         |
| DDR1_DQ11                      | IO           | DDRSS Data                      | C11         |
| DDR1_DQ12                      | IO           | DDRSS Data                      | E11         |
| DDR1_DQ13                      | IO           | DDRSS Data                      | A11         |
| DDR1_DQ14                      | IO           | DDRSS Data                      | B12         |
| DDR1_DQ15                      | IO           | DDRSS Data                      | D12         |
| DDR1_DQ16                      | IO           | DDRSS Data                      | B7          |
| DDR1_DQ17                      | IO           | DDRSS Data                      | D7          |
| DDR1_DQ18                      | IO           | DDRSS Data                      | C8          |
| DDR1_DQ19                      | IO           | DDRSS Data                      | A8          |
| DDR1_DQ20                      | IO           | DDRSS Data                      | C6          |
| DDR1_DQ21                      | IO           | DDRSS Data                      | E6          |
| DDR1_DQ22                      | IO           | DDRSS Data                      | B5          |
| DDR1_DQ23                      | IO           | DDRSS Data                      | D5          |
| DDR1_DQ24                      | IO           | DDRSS Data                      | B1          |
| DDR1_DQ25                      | IO           | DDRSS Data                      | A4          |
| DDR1_DQ26                      | IO           | DDRSS Data                      | C4          |
| DDR1_DQ27                      | IO           | DDRSS Data                      | E4          |
| DDR1_DQ28                      | IO           | DDRSS Data                      | D1          |
| DDR1_DQ29                      | IO           | DDRSS Data                      | D3          |
| DDR1_DQ30                      | IO           | DDRSS Data                      | C2          |
| DDR1_DQ31                      | IO           | DDRSS Data                      | E2          |
| DDR1_DQS0N                     | IO           | DDRSS Complimentary Data Strobe | A15         |
| DDR1_DQS0P                     | IO           | DDRSS Data Strobe               | A16         |
| DDR1_DQS1N                     | IO           | DDRSS Complimentary Data Strobe | A12         |
| DDR1_DQS1P                     | IO           | DDRSS Data Strobe               | A13         |

**Table 5-6. DDRSS1 Signal Descriptions (continued)**

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                 | ALZ PIN [4] |
|--------------------------------|--------------|---------------------------------|-------------|
| DDR1_DQS2N                     | IO           | DDRSS Complimentary Data Strobe | A7          |
| DDR1_DQS2P                     | IO           | DDRSS Data Strobe               | A6          |
| DDR1_DQS3N                     | IO           | DDRSS Complimentary Data Strobe | A2          |
| DDR1_DQS3P                     | IO           | DDRSS Data Strobe               | A3          |

(1) An external 240  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

(2) DDRSS0 and DDRSS1 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0\_\* interface. When using two LPDDR components, they must be connected to DDR0\_\* and DDR1\_\* interfaces.

### 5.3.3 GPIO

#### 5.3.3.1 MAIN Domain

**Table 5-7. GPIO0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALZ PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO0_0         | IO           | General Purpose Input/Output | AG24        |
| GPIO0_1         | IO           | General Purpose Input/Output | W25         |
| GPIO0_2         | IO           | General Purpose Input/Output | AC24        |
| GPIO0_3         | IO           | General Purpose Input/Output | AE28        |
| GPIO0_4         | IO           | General Purpose Input/Output | AF28        |
| GPIO0_5         | IO           | General Purpose Input/Output | AD25        |
| GPIO0_6         | IO           | General Purpose Input/Output | W23         |
| GPIO0_7         | IO           | General Purpose Input/Output | Y24         |
| GPIO0_8         | IO           | General Purpose Input/Output | AA23        |
| GPIO0_9         | IO           | General Purpose Input/Output | Y28         |
| GPIO0_10        | IO           | General Purpose Input/Output | AB24        |
| GPIO0_11        | IO           | General Purpose Input/Output | V23         |
| GPIO0_12        | IO           | General Purpose Input/Output | T26         |
| GPIO0_13        | IO           | General Purpose Input/Output | AD24        |
| GPIO0_14        | IO           | General Purpose Input/Output | AB28        |
| GPIO0_15        | IO           | General Purpose Input/Output | U27         |
| GPIO0_16        | IO           | General Purpose Input/Output | AC28        |
| GPIO0_17        | IO           | General Purpose Input/Output | Y26         |
| GPIO0_18        | IO           | General Purpose Input/Output | AB27        |
| GPIO0_19        | IO           | General Purpose Input/Output | V27         |
| GPIO0_20        | IO           | General Purpose Input/Output | W27         |
| GPIO0_21        | IO           | General Purpose Input/Output | Y27         |
| GPIO0_22        | IO           | General Purpose Input/Output | AA27        |
| GPIO0_23        | IO           | General Purpose Input/Output | AA26        |
| GPIO0_24        | IO           | General Purpose Input/Output | AC27        |
| GPIO0_25        | IO           | General Purpose Input/Output | W28         |
| GPIO0_26        | IO           | General Purpose Input/Output | U28         |
| GPIO0_27        | IO           | General Purpose Input/Output | V26         |
| GPIO0_28        | IO           | General Purpose Input/Output | R27         |
| GPIO0_29        | IO           | General Purpose Input/Output | R28         |
| GPIO0_30        | IO           | General Purpose Input/Output | Y25         |
| GPIO0_31        | IO           | General Purpose Input/Output | T27         |
| GPIO0_32        | IO           | General Purpose Input/Output | U26         |
| GPIO0_33        | IO           | General Purpose Input/Output | AA28        |

**Table 5-7. GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALZ PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO0_34        | IO           | General Purpose Input/Output | AD27        |
| GPIO0_35        | IO           | General Purpose Input/Output | T25         |
| GPIO0_36        | IO           | General Purpose Input/Output | W24         |
| GPIO0_37        | IO           | General Purpose Input/Output | AA25        |
| GPIO0_38        | IO           | General Purpose Input/Output | V25         |
| GPIO0_39        | IO           | General Purpose Input/Output | T24         |
| GPIO0_40        | IO           | General Purpose Input/Output | AB25        |
| GPIO0_41        | IO           | General Purpose Input/Output | T23         |
| GPIO0_42        | IO           | General Purpose Input/Output | U24         |
| GPIO0_43        | IO           | General Purpose Input/Output | AC25        |
| GPIO0_44        | IO           | General Purpose Input/Output | AD26        |
| GPIO0_45        | IO           | General Purpose Input/Output | U25         |
| GPIO0_46        | IO           | General Purpose Input/Output | AA24        |
| GPIO0_47        | IO           | General Purpose Input/Output | V28         |
| GPIO0_48        | IO           | General Purpose Input/Output | T28         |
| GPIO0_49        | IO           | General Purpose Input/Output | AB26        |
| GPIO0_50        | IO           | General Purpose Input/Output | AD28        |
| GPIO0_51        | IO           | General Purpose Input/Output | AE27        |
| GPIO0_52        | IO           | General Purpose Input/Output | AF26        |
| GPIO0_53        | IO           | General Purpose Input/Output | AH27        |
| GPIO0_54        | IO           | General Purpose Input/Output | AG26        |
| GPIO0_55        | IO           | General Purpose Input/Output | AH26        |
| GPIO0_56        | IO           | General Purpose Input/Output | AH25        |
| GPIO0_57        | IO           | General Purpose Input/Output | AE24        |
| GPIO0_58        | IO           | General Purpose Input/Output | AE25        |
| GPIO0_59        | IO           | General Purpose Input/Output | AG25        |
| GPIO0_60        | IO           | General Purpose Input/Output | R22         |
| GPIO0_61        | IO           | General Purpose Input/Output | R24         |
| GPIO0_62        | IO           | General Purpose Input/Output | P24         |
| GPIO0_63        | IO           | General Purpose Input/Output | M23         |
| GPIO0_64        | IO           | General Purpose Input/Output | P23         |
| GPIO0_65        | IO           | General Purpose Input/Output | N24         |

### 5.3.3.2 WKUP Domain

**Table 5-8. WKUP\_GPIO0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALZ PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| WKUP_GPIO0_0    | IO           | General Purpose Input/Output | D26         |
| WKUP_GPIO0_1    | IO           | General Purpose Input/Output | E24         |
| WKUP_GPIO0_2    | IO           | General Purpose Input/Output | C28         |
| WKUP_GPIO0_3    | IO           | General Purpose Input/Output | C27         |
| WKUP_GPIO0_4    | IO           | General Purpose Input/Output | C23         |
| WKUP_GPIO0_5    | IO           | General Purpose Input/Output | F26         |
| WKUP_GPIO0_6    | IO           | General Purpose Input/Output | E25         |
| WKUP_GPIO0_7    | IO           | General Purpose Input/Output | F28         |
| WKUP_GPIO0_8    | IO           | General Purpose Input/Output | F24         |

**Table 5-8. WKUP\_GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALZ PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| WKUP_GPIO0_9    | IO           | General Purpose Input/Output | H26         |
| WKUP_GPIO0_10   | IO           | General Purpose Input/Output | F27         |
| WKUP_GPIO0_11   | IO           | General Purpose Input/Output | F25         |
| WKUP_GPIO0_12   | IO           | General Purpose Input/Output | C25         |
| WKUP_GPIO0_13   | IO           | General Purpose Input/Output | C24         |
| WKUP_GPIO0_14   | IO           | General Purpose Input/Output | B24         |
| WKUP_GPIO0_15   | IO           | General Purpose Input/Output | D25         |
| WKUP_GPIO0_16   | IO           | General Purpose Input/Output | D19         |
| WKUP_GPIO0_17   | IO           | General Purpose Input/Output | E20         |
| WKUP_GPIO0_18   | IO           | General Purpose Input/Output | E18         |
| WKUP_GPIO0_19   | IO           | General Purpose Input/Output | C19         |
| WKUP_GPIO0_20   | IO           | General Purpose Input/Output | F16         |
| WKUP_GPIO0_21   | IO           | General Purpose Input/Output | G15         |
| WKUP_GPIO0_22   | IO           | General Purpose Input/Output | F18         |
| WKUP_GPIO0_23   | IO           | General Purpose Input/Output | E19         |
| WKUP_GPIO0_24   | IO           | General Purpose Input/Output | G19         |
| WKUP_GPIO0_25   | IO           | General Purpose Input/Output | F19         |
| WKUP_GPIO0_26   | IO           | General Purpose Input/Output | F20         |
| WKUP_GPIO0_27   | IO           | General Purpose Input/Output | F15         |
| WKUP_GPIO0_28   | IO           | General Purpose Input/Output | G17         |
| WKUP_GPIO0_29   | IO           | General Purpose Input/Output | F14         |
| WKUP_GPIO0_30   | IO           | General Purpose Input/Output | F17         |
| WKUP_GPIO0_31   | IO           | General Purpose Input/Output | A19         |
| WKUP_GPIO0_32   | IO           | General Purpose Input/Output | B20         |
| WKUP_GPIO0_33   | IO           | General Purpose Input/Output | B19         |
| WKUP_GPIO0_34   | IO           | General Purpose Input/Output | D21         |
| WKUP_GPIO0_35   | IO           | General Purpose Input/Output | G20         |
| WKUP_GPIO0_36   | IO           | General Purpose Input/Output | C20         |
| WKUP_GPIO0_37   | IO           | General Purpose Input/Output | A20         |
| WKUP_GPIO0_38   | IO           | General Purpose Input/Output | D20         |
| WKUP_GPIO0_39   | IO           | General Purpose Input/Output | C21         |
| WKUP_GPIO0_40   | IO           | General Purpose Input/Output | F22         |
| WKUP_GPIO0_41   | IO           | General Purpose Input/Output | E23         |
| WKUP_GPIO0_42   | IO           | General Purpose Input/Output | E22         |
| WKUP_GPIO0_43   | IO           | General Purpose Input/Output | E21         |
| WKUP_GPIO0_44   | IO           | General Purpose Input/Output | G22         |
| WKUP_GPIO0_45   | IO           | General Purpose Input/Output | F23         |
| WKUP_GPIO0_46   | IO           | General Purpose Input/Output | F21         |
| WKUP_GPIO0_47   | IO           | General Purpose Input/Output | D22         |
| WKUP_GPIO0_48   | IO           | General Purpose Input/Output | D23         |
| WKUP_GPIO0_49   | IO           | General Purpose Input/Output | K26         |
| WKUP_GPIO0_50   | IO           | General Purpose Input/Output | B21         |
| WKUP_GPIO0_51   | IO           | General Purpose Input/Output | B22         |
| WKUP_GPIO0_52   | IO           | General Purpose Input/Output | A22         |
| WKUP_GPIO0_53   | IO           | General Purpose Input/Output | A21         |

**Table 5-8. WKUP\_GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALZ PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| WKUP_GPIO0_54   | IO           | General Purpose Input/Output | B27         |
| WKUP_GPIO0_55   | IO           | General Purpose Input/Output | D24         |
| WKUP_GPIO0_56   | IO           | General Purpose Input/Output | G27         |
| WKUP_GPIO0_57   | IO           | General Purpose Input/Output | J26         |
| WKUP_GPIO0_58   | IO           | General Purpose Input/Output | D28         |
| WKUP_GPIO0_59   | IO           | General Purpose Input/Output | D27         |
| WKUP_GPIO0_60   | IO           | General Purpose Input/Output | E27         |
| WKUP_GPIO0_61   | IO           | General Purpose Input/Output | E28         |
| WKUP_GPIO0_62   | IO           | General Purpose Input/Output | C22         |
| WKUP_GPIO0_63   | IO           | General Purpose Input/Output | H24         |
| WKUP_GPIO0_64   | IO           | General Purpose Input/Output | H27         |
| WKUP_GPIO0_65   | IO           | General Purpose Input/Output | G24         |
| WKUP_GPIO0_66   | IO           | General Purpose Input/Output | G25         |
| WKUP_GPIO0_67   | IO           | General Purpose Input/Output | J27         |
| WKUP_GPIO0_68   | IO           | General Purpose Input/Output | A23         |
| WKUP_GPIO0_69   | IO           | General Purpose Input/Output | B25         |
| WKUP_GPIO0_70   | IO           | General Purpose Input/Output | B26         |
| WKUP_GPIO0_71   | I            | General Purpose Input/Output | L25         |
| WKUP_GPIO0_72   | I            | General Purpose Input/Output | K25         |
| WKUP_GPIO0_73   | I            | General Purpose Input/Output | M24         |
| WKUP_GPIO0_74   | I            | General Purpose Input/Output | L24         |
| WKUP_GPIO0_75   | I            | General Purpose Input/Output | L27         |
| WKUP_GPIO0_76   | I            | General Purpose Input/Output | K24         |
| WKUP_GPIO0_77   | I            | General Purpose Input/Output | M27         |
| WKUP_GPIO0_78   | I            | General Purpose Input/Output | M26         |
| WKUP_GPIO0_79   | I            | General Purpose Input/Output | P25         |
| WKUP_GPIO0_80   | I            | General Purpose Input/Output | R25         |
| WKUP_GPIO0_81   | I            | General Purpose Input/Output | P28         |
| WKUP_GPIO0_82   | I            | General Purpose Input/Output | P27         |
| WKUP_GPIO0_83   | I            | General Purpose Input/Output | N25         |
| WKUP_GPIO0_84   | I            | General Purpose Input/Output | P26         |
| WKUP_GPIO0_85   | I            | General Purpose Input/Output | N26         |
| WKUP_GPIO0_86   | I            | General Purpose Input/Output | N27         |
| WKUP_GPIO0_87   | IO           | General Purpose Input/Output | J25         |
| WKUP_GPIO0_88   | IO           | General Purpose Input/Output | G26         |

### 5.3.4 I2C

#### 5.3.4.1 MAIN Domain

**Table 5-9. I2C0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C0_SCL        | IOD          | I2C Clock       | AH25        |
| I2C0_SDA        | IOD          | I2C Data        | AE24        |

**Table 5-10. I2C1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4]      |
|-----------------|--------------|-----------------|------------------|
| I2C1_SCL        | IOD          | I2C Clock       | AA23, AB26, AC25 |
| I2C1_SDA        | IOD          | I2C Data        | AD26, AD28, Y28  |

**Table 5-11. I2C2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C2_SCL        | IOD          | I2C Clock       | AH27, V27   |
| I2C2_SDA        | IOD          | I2C Data        | AG26, W27   |

**Table 5-12. I2C3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C3_SCL        | IOD          | I2C Clock       | R22, W28    |
| I2C3_SDA        | IOD          | I2C Data        | AC27, R24   |

**Table 5-13. I2C4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4]     |
|-----------------|--------------|-----------------|-----------------|
| I2C4_SCL        | IOD          | I2C Clock       | AA28, AD25, M23 |
| I2C4_SDA        | IOD          | I2C Data        | AF28, P24, U26  |

**Table 5-14. I2C5 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C5_SCL        | IOD          | I2C Clock       | R28, Y24    |
| I2C5_SDA        | IOD          | I2C Data        | W23, Y25    |

**Table 5-15. I2C6 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C6_SCL        | IOD          | I2C Clock       | AG25, N24   |
| I2C6_SDA        | IOD          | I2C Data        | AE25, P23   |

**5.3.4.2 MCU Domain****Table 5-16. MCU\_I2C0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_I2C0_SCL    | IOD          | I2C Clock       | G24         |
| MCU_I2C0_SDA    | IOD          | I2C Data        | J25         |

**Table 5-17. MCU\_I2C1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_I2C1_SCL    | IOD          | I2C Clock       | E25, F24    |
| MCU_I2C1_SDA    | IOD          | I2C Data        | F28, H26    |

**5.3.4.3 WKUP Domain****Table 5-18. WKUP\_I2C0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| WKUP_I2C0_SCL   | IOD          | I2C Clock       | H24         |
| WKUP_I2C0_SDA   | IOD          | I2C Data        | H27         |

### 5.3.5 I3C

#### 5.3.5.1 MCU Domain

**Table 5-19. MCU\_I3C0 Signal Descriptions**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]      | ALZ PIN [4] |
|--------------------|--------------|----------------------|-------------|
| MCU_I3C0_SCL       | IO           | I3C Clock            | F24         |
| MCU_I3C0_SDA       | IO           | I3C Data             | H26         |
| MCU_I3C0_SDAPULLEN | OD           | I3C Data Pull Enable | F25, G26    |

### 5.3.6 MCAN

#### 5.3.6.1 MAIN Domain

**Table 5-20. MCAN0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN0_RX        | I            | MCAN Receive Data  | U28         |
| MCAN0_TX        | O            | MCAN Transmit Data | W28         |

**Table 5-21. MCAN1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN1_RX        | I            | MCAN Receive Data  | AD28, R27   |
| MCAN1_TX        | O            | MCAN Transmit Data | V26         |

**Table 5-22. MCAN2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN2_RX        | I            | MCAN Receive Data  | Y25         |
| MCAN2_TX        | O            | MCAN Transmit Data | R28         |

**Table 5-23. MCAN3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN3_RX        | I            | MCAN Receive Data  | U26         |
| MCAN3_TX        | O            | MCAN Transmit Data | T27         |

**Table 5-24. MCAN4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN4_RX        | I            | MCAN Receive Data  | AD27        |
| MCAN4_TX        | O            | MCAN Transmit Data | AA28        |

**Table 5-25. MCAN5 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN5_RX        | I            | MCAN Receive Data  | U27, W24    |
| MCAN5_TX        | O            | MCAN Transmit Data | AB28, T25   |

**Table 5-26. MCAN6 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN6_RX        | I            | MCAN Receive Data  | V25, Y26    |
| MCAN6_TX        | O            | MCAN Transmit Data | AA25, AC28  |

**Table 5-27. MCAN7 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN7_RX        | I            | MCAN Receive Data  | AB25, V27   |
| MCAN7_TX        | O            | MCAN Transmit Data | AB27, T24   |

**Table 5-28. MCAN8 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN8_RX        | I            | MCAN Receive Data  | U24, Y27    |
| MCAN8_TX        | O            | MCAN Transmit Data | T23, W27    |

**Table 5-29. MCAN9 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN9_RX        | I            | MCAN Receive Data  | AA26, AD26  |
| MCAN9_TX        | O            | MCAN Transmit Data | AA27, AC25  |

**Table 5-30. MCAN10 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN10_RX       | I            | MCAN Receive Data  | AA24        |
| MCAN10_TX       | O            | MCAN Transmit Data | U25         |

**Table 5-31. MCAN11 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN11_RX       | I            | MCAN Receive Data  | T28         |
| MCAN11_TX       | O            | MCAN Transmit Data | V28         |

**Table 5-32. MCAN12 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN12_RX       | I            | MCAN Receive Data  | AC24, T26   |
| MCAN12_TX       | O            | MCAN Transmit Data | AB26, W25   |

**Table 5-33. MCAN13 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN13_RX       | I            | MCAN Receive Data  | AF28, AG25  |
| MCAN13_TX       | O            | MCAN Transmit Data | AE25, AE28  |

**Table 5-34. MCAN14 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN14_RX       | I            | MCAN Receive Data  | AF26, W23   |
| MCAN14_TX       | O            | MCAN Transmit Data | AD25, AE27  |

**Table 5-35. MCAN15 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN15_RX       | I            | MCAN Receive Data  | AA23, N24   |
| MCAN15_TX       | O            | MCAN Transmit Data | P23, Y24    |

**Table 5-36. MCAN16 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| MCAN16_RX       | I            | MCAN Receive Data | AB24        |

**Table 5-36. MCAN16 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN16_TX       | O            | MCAN Transmit Data | Y28         |

**Table 5-37. MCAN17 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN17_RX       | I            | MCAN Receive Data  | AC27, AD24  |
| MCAN17_TX       | O            | MCAN Transmit Data | V23         |

### 5.3.6.2 MCU Domain

**Table 5-38. MCU\_MCAN0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCU_MCAN0_RX    | I            | MCAN Receive Data  | E28         |
| MCU_MCAN0_TX    | O            | MCAN Transmit Data | E27         |

**Table 5-39. MCU\_MCAN1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCU_MCAN1_RX    | I            | MCAN Receive Data  | F26         |
| MCU_MCAN1_TX    | O            | MCAN Transmit Data | C23         |

### 5.3.7 MCSPI

#### 5.3.7.1 MAIN Domain

**Table 5-40. MCSPI0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI0_CLK        | IO           | SPI Clock         | AH27        |
| SPI0_CS0        | IO           | SPI Chip Select 0 | AE27        |
| SPI0_CS1        | IO           | SPI Chip Select 1 | AF26        |
| SPI0_CS2        | IO           | SPI Chip Select 2 | AA23        |
| SPI0_CS3        | IO           | SPI Chip Select 3 | AB24        |
| SPI0_D0         | IO           | SPI Data 0        | AG26        |
| SPI0_D1         | IO           | SPI Data 1        | AH26        |

**Table 5-41. MCSPI1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI1_CLK        | IO           | SPI Clock         | P23         |
| SPI1_CS0        | IO           | SPI Chip Select 0 | R22         |
| SPI1_CS1        | IO           | SPI Chip Select 1 | R24         |
| SPI1_CS2        | IO           | SPI Chip Select 2 | P24         |
| SPI1_CS3        | IO           | SPI Chip Select 3 | Y28         |
| SPI1_D0         | IO           | SPI Data 0        | M23         |
| SPI1_D1         | IO           | SPI Data 1        | N24         |

**Table 5-42. MCSPI2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI2_CLK        | IO           | SPI Clock         | AB25        |
| SPI2_CS0        | IO           | SPI Chip Select 0 | T23         |
| SPI2_CS1        | IO           | SPI Chip Select 1 | T24         |

**Table 5-42. MCSPI2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI2_CS2        | IO           | SPI Chip Select 2 | AC28        |
| SPI2_CS3        | IO           | SPI Chip Select 3 | Y26         |
| SPI2_D0         | IO           | SPI Data 0        | U24         |
| SPI2_D1         | IO           | SPI Data 1        | AC25        |

**Table 5-43. MCSPI3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI3_CLK        | IO           | SPI Clock         | T28         |
| SPI3_CS0        | IO           | SPI Chip Select 0 | V28         |
| SPI3_CS1        | IO           | SPI Chip Select 1 | T27         |
| SPI3_CS2        | IO           | SPI Chip Select 2 | AD27        |
| SPI3_CS3        | IO           | SPI Chip Select 3 | AA24        |
| SPI3_D0         | IO           | SPI Data 0        | V27         |
| SPI3_D1         | IO           | SPI Data 1        | W27         |

**Table 5-44. MCSPI5 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI5_CLK        | IO           | SPI Clock         | T27         |
| SPI5_CS0        | IO           | SPI Chip Select 0 | U28         |
| SPI5_CS1        | IO           | SPI Chip Select 1 | W28         |
| SPI5_CS2        | IO           | SPI Chip Select 2 | Y27         |
| SPI5_CS3        | IO           | SPI Chip Select 3 | AA27        |
| SPI5_D0         | IO           | SPI Data 0        | R27         |
| SPI5_D1         | IO           | SPI Data 1        | AD27        |

**Table 5-45. MCSPI6 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI6_CLK        | IO           | SPI Clock         | T26         |
| SPI6_CS0        | IO           | SPI Chip Select 0 | AD24        |
| SPI6_CS1        | IO           | SPI Chip Select 1 | Y25         |
| SPI6_CS2        | IO           | SPI Chip Select 2 | U26         |
| SPI6_CS3        | IO           | SPI Chip Select 3 | AA28        |
| SPI6_D0         | IO           | SPI Data 0        | AB26        |
| SPI6_D1         | IO           | SPI Data 1        | R28         |

**Table 5-46. MCSPI7 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI7_CLK        | IO           | SPI Clock         | AC28        |
| SPI7_CS0        | IO           | SPI Chip Select 0 | Y26         |
| SPI7_CS1        | IO           | SPI Chip Select 1 | Y27         |
| SPI7_CS2        | IO           | SPI Chip Select 2 | AA27        |
| SPI7_CS3        | IO           | SPI Chip Select 3 | V23         |
| SPI7_D0         | IO           | SPI Data 0        | U28         |
| SPI7_D1         | IO           | SPI Data 1        | T27         |

### 5.3.7.2 MCU Domain

**Table 5-47. MCU\_MCSPI0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| MCU_SPI0_CLK    | IO           | SPI Clock         | B27         |
| MCU_SPI0_CS0    | IO           | SPI Chip Select 0 | B26         |
| MCU_SPI0_CS1    | IO           | SPI Chip Select 1 | A20, C25    |
| MCU_SPI0_CS2    | IO           | SPI Chip Select 2 | B24, C21    |
| MCU_SPI0_CS3    | IO           | SPI Chip Select 3 | C23         |
| MCU_SPI0_D0     | IO           | SPI Data 0        | D24         |
| MCU_SPI0_D1     | IO           | SPI Data 1        | B25         |

**Table 5-48. MCU\_MCSPI1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| MCU_SPI1_CLK    | IO           | SPI Clock         | D26         |
| MCU_SPI1_CS0    | IO           | SPI Chip Select 0 | C27         |
| MCU_SPI1_CS1    | IO           | SPI Chip Select 1 | C24, G20    |
| MCU_SPI1_CS2    | IO           | SPI Chip Select 2 | C20, D25    |
| MCU_SPI1_CS3    | IO           | SPI Chip Select 3 | F26         |
| MCU_SPI1_D0     | IO           | SPI Data 0        | E24         |
| MCU_SPI1_D1     | IO           | SPI Data 1        | C28         |

### 5.3.8 UART

#### 5.3.8.1 MAIN Domain

**Table 5-49. UART0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                       | ALZ PIN [4]    |
|-----------------|--------------|---------------------------------------|----------------|
| UART0_CTSn      | I            | UART Clear to Send (active low)       | R22, V27       |
| UART0_DCDn      | I            | UART Data Carrier Detect (active low) | AC24           |
| UART0_DSRn      | I            | UART Data Set Ready (active low)      | AE28           |
| UART0_DTRn      | O            | UART Data Terminal Ready (active low) | AF28           |
| UART0_RIn       | I            | UART Ring Indicator                   | AD25           |
| UART0_RTSn      | O            | UART Request to Send (active low)     | AF26, P23, W27 |
| UART0_RXD       | I            | UART Receive Data                     | V28            |
| UART0_TXD       | O            | UART Transmit Data                    | T28            |

**Table 5-50. UART1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| UART1_CTSn      | I            | UART Clear to Send (active low)   | AA26, AH27  |
| UART1_RTSn      | O            | UART Request to Send (active low) | AC27, AG26  |
| UART1_RXD       | I            | UART Receive Data                 | Y27         |
| UART1_TXD       | O            | UART Transmit Data                | AA27        |

**Table 5-51. UART2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4]    |
|-----------------|--------------|-----------------------------------|----------------|
| UART2_CTSn      | I            | UART Clear to Send (active low)   | AB26           |
| UART2_RTSn      | O            | UART Request to Send (active low) | AD28           |
| UART2_RXD       | I            | UART Receive Data                 | AG26, P24, W28 |

**Table 5-51. UART2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4]    |
|-----------------|--------------|--------------------|----------------|
| UART2_TXD       | O            | UART Transmit Data | AH26, M23, U28 |

**Table 5-52. UART3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4]     |
|-----------------|--------------|-----------------------------------|-----------------|
| UART3_CTSn      | I            | UART Clear to Send (active low)   | T27             |
| UART3_RTSn      | O            | UART Request to Send (active low) | R27             |
| UART3_RXD       | I            | UART Receive Data                 | AB26, AE25, R28 |
| UART3_TXD       | O            | UART Transmit Data                | AD28, AG25, Y25 |

**Table 5-53. UART4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4]         |
|-----------------|--------------|-----------------------------------|---------------------|
| UART4_CTSn      | I            | UART Clear to Send (active low)   | AA25, AB27, P23     |
| UART4_RTSn      | O            | UART Request to Send (active low) | AA24, N24, V25      |
| UART4_RXD       | I            | UART Receive Data                 | AC28, P24, T25, U25 |
| UART4_TXD       | O            | UART Transmit Data                | AE28, M23, W24, Y26 |

**Table 5-54. UART5 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4]    |
|-----------------|--------------|-----------------------------------|----------------|
| UART5_CTSn      | I            | UART Clear to Send (active low)   | P24, T23       |
| UART5_RTSn      | O            | UART Request to Send (active low) | M23, U24       |
| UART5_RXD       | I            | UART Receive Data                 | AC24, R22, T24 |
| UART5_TXD       | O            | UART Transmit Data                | AB25, R24, W25 |

**Table 5-55. UART6 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4]     |
|-----------------|--------------|-----------------------------------|-----------------|
| UART6_CTSn      | I            | UART Clear to Send (active low)   | W28             |
| UART6_RTSn      | O            | UART Request to Send (active low) | U28             |
| UART6_RXD       | I            | UART Receive Data                 | AA26, AD25, T26 |
| UART6_TXD       | O            | UART Transmit Data                | AC27, AF28, V26 |

**Table 5-56. UART7 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4]    |
|-----------------|--------------|-----------------------------------|----------------|
| UART7_CTSn      | I            | UART Clear to Send (active low)   | P24            |
| UART7_RTSn      | O            | UART Request to Send (active low) | M23            |
| UART7_RXD       | I            | UART Receive Data                 | R22, T23, V23  |
| UART7_TXD       | O            | UART Transmit Data                | AD24, R24, U24 |

**Table 5-57. UART8 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4]           |
|-----------------|--------------|-----------------------------------|-----------------------|
| UART8_CTSn      | I            | UART Clear to Send (active low)   | AC28                  |
| UART8_RTSn      | O            | UART Request to Send (active low) | Y26                   |
| UART8_RXD       | I            | UART Receive Data                 | AB28, AC25, AF26, P23 |
| UART8_TXD       | O            | UART Transmit Data                | AD26, AH27, N24, U27  |

**Table 5-58. UART9 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| UART9_CTSn      | I            | UART Clear to Send (active low)   | AB27, T26   |
| UART9_RTSn      | O            | UART Request to Send (active low) | AA24, AD24  |
| UART9_RXD       | I            | UART Receive Data                 | V27, Y24    |
| UART9_TXD       | O            | UART Transmit Data                | W23, W27    |

### 5.3.8.2 MCU Domain

**Table 5-59. MCU\_UART0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4]   |
|-----------------|--------------|-----------------------------------|---------------|
| MCU_UART0_CTSn  | I            | UART Clear to Send (active low)   | A20, B24      |
| MCU_UART0_RTSn  | O            | UART Request to Send (active low) | C21, D25      |
| MCU_UART0_RXD   | I            | UART Receive Data                 | C24, F25, G20 |
| MCU_UART0_TXD   | O            | UART Transmit Data                | C20, C25, F27 |

### 5.3.8.3 WKUP Domain

**Table 5-60. WKUP\_UART0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| WKUP_UART0_CTSn | I            | UART Clear to Send (active low)   | E25         |
| WKUP_UART0_RTSn | O            | UART Request to Send (active low) | F28         |
| WKUP_UART0_RXD  | I            | UART Receive Data                 | D28         |
| WKUP_UART0_TXD  | O            | UART Transmit Data                | D27         |

### 5.3.9 MDIO

#### 5.3.9.1 MAIN Domain

**Table 5-61. MDIO0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MDIO0_MDC       | O            | MDIO Clock      | T28         |
| MDIO0_MDIO      | IO           | MDIO Data       | V28         |

#### 5.3.9.2 MCU Domain

**Table 5-62. MCU\_MDIO0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_MDIO0_MDC   | O            | MDIO Clock      | A21         |
| MCU_MDIO0_MDIO  | IO           | MDIO Data       | A22         |

### 5.3.10 CPSW2G

#### 5.3.10.1 MAIN Domain

**Table 5-63. CPSW2G0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]        | ALZ PIN [4] |
|-----------------|--------------|------------------------|-------------|
| CLKOUT          | IO           | RMII Clock Output      | U24         |
| RGMII1_RXC      | I            | RGMII Receive Clock    | AD26        |
| RGMII1_RX_CTL   | I            | RGMII Receive Control  | AC25        |
| RGMII1_TXC      | O            | RGMII Transmit Clock   | U25         |
| RGMII1_TX_CTL   | O            | RGMII Transmit Control | T24         |
| RGMII1_RD0      | I            | RGMII Receive Data 0   | AA24        |
| RGMII1_RD1      | I            | RGMII Receive Data 1   | AB25        |

**Table 5-63. CPSW2G0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                 | ALZ PIN [4] |
|-----------------|--------------|---------------------------------|-------------|
| RGMII1_RD2      | I            | RGMII Receive Data 2            | T23         |
| RGMII1_RD3      | I            | RGMII Receive Data 3            | U24         |
| RGMII1_TD0      | O            | RGMII Transmit Data 0           | T25         |
| RGMII1_TD1      | O            | RGMII Transmit Data 1           | W24         |
| RGMII1_TD2      | O            | RGMII Transmit Data 2           | AA25        |
| RGMII1_TD3      | O            | RGMII Transmit Data 3           | V25         |
| RMII1_CRS_DV    | I            | RMII Carrier Sense / Data Valid | V25         |
| RMII1_RX_ER     | I            | RMII Receive Data Error         | T24         |
| RMII1_TX_EN     | O            | RMII Transmit Enable            | AC25        |
| RMII1_RXD0      | I            | RMII Receive Data 0             | W24         |
| RMII1_RXD1      | I            | RMII Receive Data 1             | AA25        |
| RMII1_TXD0      | O            | RMII Transmit Data 0            | AB25        |
| RMII1_TXD1      | O            | RMII Transmit Data 1            | AD26        |
| RMII_REF_CLK    | I            | RMII Reference Clock            | T23         |

**5.3.10.2 MCU Domain****Table 5-64. MCU\_CPSW2G0 Signal Descriptions**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                 | ALZ PIN [4] |
|-------------------|--------------|---------------------------------|-------------|
| MCU_RGMII1_RXC    | I            | RGMII Receive Clock             | D22         |
| MCU_RGMII1_RX_CTL | I            | RGMII Receive Control           | E23         |
| MCU_RGMII1_TXC    | O            | RGMII Transmit Clock            | F21         |
| MCU_RGMII1_TX_CTL | O            | RGMII Transmit Control          | F22         |
| MCU_RGMII1_RD0    | I            | RGMII Receive Data 0            | B22         |
| MCU_RGMII1_RD1    | I            | RGMII Receive Data 1            | B21         |
| MCU_RGMII1_RD2    | I            | RGMII Receive Data 2            | C22         |
| MCU_RGMII1_RD3    | I            | RGMII Receive Data 3            | D23         |
| MCU_RGMII1_TD0    | O            | RGMII Transmit Data 0           | F23         |
| MCU_RGMII1_TD1    | O            | RGMII Transmit Data 1           | G22         |
| MCU_RGMII1_TD2    | O            | RGMII Transmit Data 2           | E21         |
| MCU_RGMII1_TD3    | O            | RGMII Transmit Data 3           | E22         |
| MCU_RMII1_CRS_DV  | I            | RMII Carrier Sense / Data Valid | F22         |
| MCU_RMII1_REF_CLK | I            | RMII Reference Clock            | D22         |
| MCU_RMII1_RX_ER   | I            | RMII Receive Data Error         | E23         |
| MCU_RMII1_TX_EN   | O            | RMII Transmit Enable            | F21         |
| MCU_RMII1_RXD0    | I            | RMII Receive Data 0             | B22         |
| MCU_RMII1_RXD1    | I            | RMII Receive Data 1             | B21         |
| MCU_RMII1_TXD0    | O            | RMII Transmit Data 0            | F23         |
| MCU_RMII1_TXD1    | O            | RMII Transmit Data 1            | G22         |

**5.3.11 ECAP****5.3.11.1 MAIN Domain****Table 5-65. ECAP0 Signal Descriptions**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                              | ALZ PIN [4] |
|-------------------|--------------|--------------------------------------------------------------|-------------|
| ECAP0_IN_APWM_OUT | IO           | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | AB26, P24   |

**Table 5-66. ECAP1 Signal Descriptions**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                              | ALZ PIN [4] |
|-------------------|--------------|--------------------------------------------------------------|-------------|
| ECAP1_IN_APWM_OUT | IO           | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | AE25, M23   |

**Table 5-67. ECAP2 Signal Descriptions**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                              | ALZ PIN [4] |
|-------------------|--------------|--------------------------------------------------------------|-------------|
| ECAP2_IN_APWM_OUT | IO           | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | AG25        |

### 5.3.12 EQEP

#### 5.3.12.1 MAIN Domain

**Table 5-68. EQEP0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ALZ PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| EQEP0_A         | I            | EQEP Quadrature Input A | U24         |
| EQEP0_B         | I            | EQEP Quadrature Input B | AC25        |
| EQEP0_I         | IO           | EQEP Index              | V28         |
| EQEP0_S         | IO           | EQEP Strobe             | AA24        |

**Table 5-69. EQEP1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ALZ PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| EQEP1_A         | I            | EQEP Quadrature Input A | AD26        |
| EQEP1_B         | I            | EQEP Quadrature Input B | U25         |
| EQEP1_I         | IO           | EQEP Index              | T26         |
| EQEP1_S         | IO           | EQEP Strobe             | T28         |

**Table 5-70. EQEP2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ALZ PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| EQEP2_A         | I            | EQEP Quadrature Input A | AB27        |
| EQEP2_B         | I            | EQEP Quadrature Input B | W27         |
| EQEP2_I         | IO           | EQEP Index              | AA26        |
| EQEP2_S         | IO           | EQEP Strobe             | Y27         |

### 5.3.13 EPWM

#### 5.3.13.1 MAIN Domain

**Table 5-71. EPWM Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                       | ALZ PIN [4] |
|-----------------|--------------|---------------------------------------|-------------|
| EHRPWM_SOCA     | O            | EHRPWM Start of Conversion A          | AA27        |
| EHRPWM_SOCB     | O            | EHRPWM Start of Conversion B          | AB25        |
| EHRPWM_TZn_IN0  | I            | EHRPWM Trip Zone Input 0 (active low) | T27         |
| EHRPWM_TZn_IN1  | I            | EHRPWM Trip Zone Input 1 (active low) | V27         |
| EHRPWM_TZn_IN2  | I            | EHRPWM Trip Zone Input 2 (active low) | AB28        |
| EHRPWM_TZn_IN3  | I            | EHRPWM Trip Zone Input 3 (active low) | W24         |
| EHRPWM_TZn_IN4  | I            | EHRPWM Trip Zone Input 4 (active low) | AD27        |
| EHRPWM_TZn_IN5  | I            | EHRPWM Trip Zone Input 5 (active low) | V26         |

**Table 5-72. EPWM0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                  | ALZ PIN [4]    |
|-----------------|--------------|--------------------------------------------------|----------------|
| EHRPWM0_A       | IO           | EHRPWM Output A                                  | AE27, R24, U28 |
| EHRPWM0_B       | IO           | EHRPWM Output B                                  | R22, W28       |
| EHRPWM0_SYNCI   | I            | Sync Input to EHRPWM module from an external pin | R27            |
| EHRPWM0_SYNCO   | O            | Sync Output to EHRPWM module to an external pin  | Y26            |

**Table 5-73. EPWM1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4]     |
|-----------------|--------------|-----------------|-----------------|
| EHRPWM1_A       | IO           | EHRPWM Output A | AC27, AF26, M23 |
| EHRPWM1_B       | IO           | EHRPWM Output B | P24, R28        |

**Table 5-74. EPWM2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4]     |
|-----------------|--------------|-----------------|-----------------|
| EHRPWM2_A       | IO           | EHRPWM Output A | AC28, AH27, N24 |
| EHRPWM2_B       | IO           | EHRPWM Output B | P23, U27        |

**Table 5-75. EPWM3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                  | ALZ PIN [4]    |
|-----------------|--------------|--------------------------------------------------|----------------|
| EHRPWM3_A       | IO           | EHRPWM Output A                                  | AG26, R22, T25 |
| EHRPWM3_B       | IO           | EHRPWM Output B                                  | T24            |
| EHRPWM3_SYNCI   | I            | Sync Input to EHRPWM module from an external pin | V25            |
| EHRPWM3_SYNCO   | O            | Sync Output to EHRPWM module to an external pin  | AA25           |

**Table 5-76. EPWM4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4]    |
|-----------------|--------------|-----------------|----------------|
| EHRPWM4_A       | IO           | EHRPWM Output A | AH26, P24, T23 |
| EHRPWM4_B       | IO           | EHRPWM Output B | Y25            |

**Table 5-77. EPWM5 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EHRPWM5_A       | IO           | EHRPWM Output A | AA28, P23   |
| EHRPWM5_B       | IO           | EHRPWM Output B | U26         |

### 5.3.14 USB

#### 5.3.14.1 MAIN Domain

**Table 5-78. USB0 Signal Descriptions**

| SIGNAL NAME [1]            | PIN TYPE [2] | DESCRIPTION [3]                                 | ALZ PIN [4]    |
|----------------------------|--------------|-------------------------------------------------|----------------|
| USB0_DM                    | IO           | USB 2.0 Differential Data (negative)            | AG2            |
| USB0_DP                    | IO           | USB 2.0 Differential Data (positive)            | AH2            |
| USB0_DRVVBUS               | O            | USB VBUS Control Output (active high)           | AG25, T25, V23 |
| USB0_ID                    | A            | USB 2.0 Dual-Role Device Role Select            | AC9            |
| USB0_RCALIB <sup>(1)</sup> | A            | Pin to connect to calibration resistor          | AA6            |
| USB0_VBUS <sup>(2)</sup>   | A            | USB Level-shifted VBUS Detector                 | AA8            |
| USB0_SSRX1N                | I            | SERDES_USB Differential Receive Data (negative) | AF6, AF9       |
| USB0_SSRX1P                | I            | SERDES_USB Differential Receive Data (positive) | AF10, AF7      |
| USB0_SSRX2N                | I            | SERDES_USB Differential Receive Data (negative) | AE5, AE8       |

**Table 5-78. USB0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                  | ALZ PIN [4] |
|-----------------|--------------|--------------------------------------------------|-------------|
| USB0_SSRX2P     | I            | SERDES_USB Differential Receive Data (positive)  | AE6, AE9    |
| USB0_SSTX1N     | O            | SERDES_USB Differential Transmit Data (negative) | AG5, AH7    |
| USB0_SSTX1P     | O            | SERDES_USB Differential Transmit Data (positive) | AG6, AH8    |
| USB0_SSTX2N     | O            | SERDES_USB Differential Transmit Data (negative) | AD7, AG8    |
| USB0_SSTX2P     | O            | SERDES_USB Differential Transmit Data (positive) | AD8, AG9    |

- (1) An external 500  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS, even when the pin is unused  
(2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see [Optional text USB VBUS Design Guidelines](#).

### 5.3.15 Display Port

#### 5.3.15.1 MAIN Domain

**Table 5-79. DP0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                     | ALZ PIN [4] |
|-----------------|--------------|-----------------------------------------------------|-------------|
| DP0_AUXN        | IO           | Display Port Differential Auxiliary Data (negative) | AG11        |
| DP0_AUXP        | IO           | Display Port Differential Auxiliary Data (positive) | AF11        |
| DP0_HPD         | I            | Display Port Hot Plug Detection                     | AA24        |
| DP0_TXN0        | O            | Display Port Differential Transmit (negative)       | AG5, AH7    |
| DP0_TXN1        | O            | Display Port Differential Transmit (negative)       | AD7, AG8    |
| DP0_TXN2        | O            | Display Port Differential Transmit (negative)       | AG5         |
| DP0_TXN3        | O            | Display Port Differential Transmit (negative)       | AD7         |
| DP0_TXP0        | O            | Display Port Differential Transmit (positive)       | AG6, AH8    |
| DP0_TXP1        | O            | Display Port Differential Transmit (positive)       | AD8, AG9    |
| DP0_TXP2        | O            | Display Port Differential Transmit (positive)       | AG6         |
| DP0_TXP3        | O            | Display Port Differential Transmit (positive)       | AD8         |

### 5.3.16 Hyperlink

#### 5.3.16.1 MAIN Domain

**Table 5-80. Hyperlink Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]          | ALZ PIN [4] |
|-----------------|--------------|--------------------------|-------------|
| HYP_RXN0        | I            | Hyperlink RX (negative)  | AF9         |
| HYP_RXN1        | I            | Hyperlink RX (negative)  | AE8         |
| HYP_RXN2        | I            | Hyperlink RX (negative)  | AF6         |
| HYP_RXN3        | I            | Hyperlink RX (negative)  | AE5         |
| HYP_RXP0        | I            | Hyperlink RX (positive)  | AF10        |
| HYP_RXP1        | I            | Hyperlink RX (positive)  | AE9         |
| HYP_RXP2        | I            | Hyperlink RX (positive)  | AF7         |
| HYP_RXP3        | I            | Hyperlink RX (positive)  | AE6         |
| HYP_TXN0        | O            | Hyperlink TX0 (negative) | AH7         |
| HYP_TXN1        | O            | Hyperlink TX0 (negative) | AG8         |
| HYP_TXN2        | O            | Hyperlink TX0 (negative) | AG5         |
| HYP_TXN3        | O            | Hyperlink TX0 (negative) | AD7         |
| HYP_TXP0        | O            | Hyperlink TX0 (positive) | AH8         |
| HYP_TXP1        | O            | Hyperlink TX0 (positive) | AG9         |
| HYP_TXP2        | O            | Hyperlink TX0 (positive) | AG6         |
| HYP_TXP3        | O            | Hyperlink TX0 (positive) | AD8         |

**Table 5-81. Hyperlink0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                           | ALZ PIN [4] |
|-----------------|--------------|-------------------------------------------|-------------|
| HYP0_RXFLCLK    | O            | Hyperlink Flow Management Receive Clock   | AB28        |
| HYP0_RXFLDAT    | O            | Hyperlink Flow Management Receive Data    | U27         |
| HYP0_RXPMCLK    | I            | Hyperlink Power Management Receive Clock  | AA26        |
| HYP0_RXPMDAT    | I            | Hyperlink Power Management Receive Data   | AC27        |
| HYP0_TXFLCLK    | I            | Hyperlink Flow Management Transmit Clock  | AC28        |
| HYP0_TXFLDAT    | I            | Hyperlink Flow Management Transmit Data   | Y26         |
| HYP0_TXPMCLK    | O            | Hyperlink Power Management Transmit Clock | Y27         |
| HYP0_TXPMDAT    | O            | Hyperlink Power Management Transmit Data  | AA27        |

**Table 5-82. Hyperlink1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                           | ALZ PIN [4] |
|-----------------|--------------|-------------------------------------------|-------------|
| HYP1_RXFLCLK    | O            | Hyperlink Flow Management Receive Clock   | AB27        |
| HYP1_RXFLDAT    | O            | Hyperlink Flow Management Receive Data    | T26         |
| HYP1_RXPMCLK    | I            | Hyperlink Power Management Receive Clock  | V27         |
| HYP1_RXPMDAT    | I            | Hyperlink Power Management Receive Data   | W27         |
| HYP1_TXFLCLK    | I            | Hyperlink Flow Management Transmit Clock  | AB26        |
| HYP1_TXFLDAT    | I            | Hyperlink Flow Management Transmit Data   | AD28        |
| HYP1_TXPMCLK    | O            | Hyperlink Power Management Transmit Clock | V26         |
| HYP1_TXPMDAT    | O            | Hyperlink Power Management Transmit Data  | U26         |

**5.3.17 PCIE****5.3.17.1 MAIN Domain****Table 5-83. PCIE Signal Descriptions**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]                                   | ALZ PIN [4] |
|--------------------|--------------|---------------------------------------------------|-------------|
| PCIE1_CLKREQn      | IO           | PCIE Clock Request Signal                         | AE25, R22   |
| PCIE1_RXN0         | I            | SERDES_PCIE Differential Receive Data (negative)  | AF9         |
| PCIE1_RXN1         | I            | SERDES_PCIE Differential Receive Data (negative)  | AE8         |
| PCIE1_RXN2         | I            | SERDES_PCIE Differential Receive Data (negative)  | AF6         |
| PCIE1_RXN3         | I            | SERDES_PCIE Differential Receive Data (negative)  | AE5         |
| PCIE1_RXP0         | I            | SERDES_PCIE Differential Receive Data (positive)  | AF10        |
| PCIE1_RXP1         | I            | SERDES_PCIE Differential Receive Data (positive)  | AE9         |
| PCIE1_RXP2         | I            | SERDES_PCIE Differential Receive Data (positive)  | AF7         |
| PCIE1_RXP3         | I            | SERDES_PCIE Differential Receive Data (positive)  | AE6         |
| PCIE1_TXN0         | O            | SERDES_PCIE Differential Transmit Data (negative) | AH7         |
| PCIE1_TXN1         | O            | SERDES_PCIE Differential Transmit Data (negative) | AG8         |
| PCIE1_TXN2         | O            | SERDES_PCIE Differential Transmit Data (negative) | AG5         |
| PCIE1_TXN3         | O            | SERDES_PCIE Differential Transmit Data (negative) | AD7         |
| PCIE1_TXP0         | O            | SERDES_PCIE Differential Transmit Data (positive) | AH8         |
| PCIE1_TXP1         | O            | SERDES_PCIE Differential Transmit Data (positive) | AG9         |
| PCIE1_TXP2         | O            | SERDES_PCIE Differential Transmit Data (positive) | AG6         |
| PCIE1_TXP3         | O            | SERDES_PCIE Differential Transmit Data (positive) | AD8         |
| PCIE_REFCLK1_N_OUT | O            | SERDES_PCIE Reference Clock Out Negative          | AH10        |
| PCIE_REFCLK1_P_OUT | O            | SERDES_PCIE Reference Clock Out Positive          | AH11        |

### 5.3.18 SERDES

#### 5.3.18.1 MAIN Domain

**Table 5-84. SERDES0 Signal Descriptions**

| SIGNAL NAME [1]             | PIN TYPE [2] | DESCRIPTION [3]                                | ALZ PIN [4] |
|-----------------------------|--------------|------------------------------------------------|-------------|
| SERDES0_REFCLK_N            | IO           | Serdes Reference Clock Input/Output (negative) | AH4         |
| SERDES0_REFCLK_P            | IO           | Serdes Reference Clock Input/Output (positive) | AH5         |
| SERDES0_REXT <sup>(1)</sup> | I            | External Calibration Resistor                  | AC10        |

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

### 5.3.19 DSI

#### 5.3.19.1 MAIN Domain

**Table 5-85. DSI0 Signal Descriptions**

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4] |
|------------------------------|--------------|-----------------------------------|-------------|
| DSI0_TXCLKN                  | O            | DSI Transmit clock (negative)     | AH13        |
| DSI0_TXCLKP                  | O            | DSI Transmit clock (positive)     | AH14        |
| DSI0_TXRCALIB <sup>(1)</sup> | A            | DSI Transmit Calibration Resistor | AC13        |
| DSI0_TXN0                    | IO           | DSI Transmit (negative)           | AG12        |
| DSI0_TXN1                    | O            | DSI Transmit (negative)           | AF13        |
| DSI0_TXN2                    | O            | DSI Transmit (negative)           | AE12        |
| DSI0_TXN3                    | O            | DSI Transmit (negative)           | AD13        |
| DSI0_TXP0                    | IO           | DSI Transmit (positive)           | AG13        |
| DSI0_TXP1                    | O            | DSI Transmit (positive)           | AF14        |
| DSI0_TXP2                    | O            | DSI Transmit (positive)           | AE13        |
| DSI0_TXP3                    | O            | DSI Transmit (positive)           | AD14        |

(1) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

**Table 5-86. DSI1 Signal Descriptions**

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4] |
|------------------------------|--------------|-----------------------------------|-------------|
| DSI1_TXCLKN                  | O            | DSI Transmit clock (negative)     | AH16        |
| DSI1_TXCLKP                  | O            | DSI Transmit clock (positive)     | AH17        |
| DSI1_TXRCALIB <sup>(1)</sup> | A            | DSI Transmit Calibration Resistor | AC15        |
| DSI1_TXN0                    | IO           | DSI Transmit (negative)           | AG15        |
| DSI1_TXN1                    | O            | DSI Transmit (negative)           | AF16        |
| DSI1_TXN2                    | O            | DSI Transmit (negative)           | AE15        |
| DSI1_TXN3                    | O            | DSI Transmit (negative)           | AD16        |
| DSI1_TXP0                    | IO           | DSI Transmit (positive)           | AG16        |
| DSI1_TXP1                    | O            | DSI Transmit (positive)           | AF17        |
| DSI1_TXP2                    | O            | DSI Transmit (positive)           | AE16        |
| DSI1_TXP3                    | O            | DSI Transmit (positive)           | AD17        |

(1) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

### 5.3.20 CSI

#### 5.3.20.1 MAIN Domain

**Table 5-87. CSI0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                 | ALZ PIN [4] |
|-----------------|--------------|-------------------------------------------------|-------------|
| CSI0_RXCLKN     | I            | CSI Differential Receive Clock Input (negative) | AH19        |
| CSI0_RXCLKP     | I            | CSI Differential Receive Clock Input (positive) | AH20        |

**Table 5-87. CSI0 Signal Descriptions (continued)**

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                                         | ALZ PIN [4] |
|------------------------------|--------------|-------------------------------------------------------------------------|-------------|
| CSI0_RXRCALIB <sup>(1)</sup> | A            | CSI Pin connected to external resistor for on-chip resistor calibration | AC18        |
| CSI0_TXCLKN                  | O            | CSI Differential Transmit Clock Output (negative)                       | AH13        |
| CSI0_TXCLKP                  | O            | CSI Differential Transmit Clock Output (positive)                       | AH14        |
| CSI0_RXN0                    | I            | CSI Differential Receive Input (negative)                               | AG18        |
| CSI0_RXN1                    | I            | CSI Differential Receive Input (negative)                               | AF19        |
| CSI0_RXN2                    | I            | CSI Differential Receive Input (negative)                               | AE18        |
| CSI0_RXN3                    | I            | CSI Differential Receive Input (negative)                               | AD19        |
| CSI0_RXP0                    | I            | CSI Differential Receive Input (positive)                               | AG19        |
| CSI0_RXP1                    | I            | CSI Differential Receive Input (positive)                               | AF20        |
| CSI0_RXP2                    | I            | CSI Differential Receive Input (positive)                               | AE19        |
| CSI0_RXP3                    | I            | CSI Differential Receive Input (positive)                               | AD20        |
| CSI0_TXN0                    | O            | CSI Differential Transmit Output (negative)                             | AG12        |
| CSI0_TXN1                    | O            | CSI Differential Transmit Output (negative)                             | AF13        |
| CSI0_TXN2                    | O            | CSI Differential Transmit Output (negative)                             | AE12        |
| CSI0_TXN3                    | O            | CSI Differential Transmit Output (negative)                             | AD13        |
| CSI0_TXP0                    | O            | CSI Differential Transmit Output (positive)                             | AG13        |
| CSI0_TXP1                    | O            | CSI Differential Transmit Output (positive)                             | AF14        |
| CSI0_TXP2                    | O            | CSI Differential Transmit Output (positive)                             | AE13        |
| CSI0_TXP3                    | O            | CSI Differential Transmit Output (positive)                             | AD14        |

(1) An external 500  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS, even when the pin is unused.

**Table 5-88. CSI1 Signal Descriptions**

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                                         | ALZ PIN [4] |
|------------------------------|--------------|-------------------------------------------------------------------------|-------------|
| CSI1_RXCLKN                  | I            | CSI Differential Receive Clock Input (negative)                         | AH22        |
| CSI1_RXCLKP                  | I            | CSI Differential Receive Clock Input (positive)                         | AH23        |
| CSI1_RXRCALIB <sup>(1)</sup> | A            | CSI pin connected to external resistor for on-chip resistor calibration | AC21        |
| CSI1_TXCLKN                  | O            | CSI Differential Transmit Clock Output (negative)                       | AH16        |
| CSI1_TXCLKP                  | O            | CSI Differential Transmit Clock Output (positive)                       | AH17        |
| CSI1_RXN0                    | I            | CSI Differential Receive Input (negative)                               | AG21        |
| CSI1_RXN1                    | I            | CSI Differential Receive Input (negative)                               | AF22        |
| CSI1_RXN2                    | I            | CSI Differential Receive Input (negative)                               | AE21        |
| CSI1_RXN3                    | I            | CSI Differential Receive Input (negative)                               | AD22        |
| CSI1_RXP0                    | I            | CSI Differential Receive Input (positive)                               | AG22        |
| CSI1_RXP1                    | I            | CSI Differential Receive Input (positive)                               | AF23        |
| CSI1_RXP2                    | I            | CSI Differential Receive Input (positive)                               | AE22        |
| CSI1_RXP3                    | I            | CSI Differential Receive Input (positive)                               | AD23        |
| CSI1_TXN0                    | O            | CSI Differential Transmit Output (negative)                             | AG15        |
| CSI1_TXN1                    | O            | CSI Differential Transmit Output (negative)                             | AF16        |
| CSI1_TXN2                    | O            | CSI Differential Transmit Output (negative)                             | AE15        |
| CSI1_TXN3                    | O            | CSI Differential Transmit Output (negative)                             | AD16        |
| CSI1_TXP0                    | O            | CSI Differential Transmit Output (positive)                             | AG16        |
| CSI1_TXP1                    | O            | CSI Differential Transmit Output (positive)                             | AF17        |
| CSI1_TXP2                    | O            | CSI Differential Transmit Output (positive)                             | AE16        |

**Table 5-88. CSI1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                             | ALZ PIN [4] |
|-----------------|--------------|---------------------------------------------|-------------|
| CSI1_TXP3       | O            | CSI Differential Transmit Output (positive) | AD17        |

(1) An external 500  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS, even when the pin is unused.

### 5.3.21 MCASP

#### 5.3.21.1 MAIN Domain

**Table 5-89. MCASP0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALZ PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCASP0_ACLKR    | IO           | MCASP Receive Bit Clock          | U24         |
| MCASP0_ACLKX    | IO           | MCASP Transmit Bit Clock         | AB28        |
| MCASP0_AFSR     | IO           | MCASP Receive Frame Sync         | AC25        |
| MCASP0_AFSX     | IO           | MCASP Transmit Frame Sync        | U27         |
| MCASP0_AXR0     | IO           | MCASP Serial Data (Input/Output) | AC28        |
| MCASP0_AXR1     | IO           | MCASP Serial Data (Input/Output) | Y26         |
| MCASP0_AXR2     | IO           | MCASP Serial Data (Input/Output) | AB27        |
| MCASP0_AXR3     | IO           | MCASP Serial Data (Input/Output) | T27         |
| MCASP0_AXR4     | IO           | MCASP Serial Data (Input/Output) | U26         |
| MCASP0_AXR5     | IO           | MCASP Serial Data (Input/Output) | AA28        |
| MCASP0_AXR6     | IO           | MCASP Serial Data (Input/Output) | AD27        |
| MCASP0_AXR7     | IO           | MCASP Serial Data (Input/Output) | T25         |
| MCASP0_AXR8     | IO           | MCASP Serial Data (Input/Output) | W24         |
| MCASP0_AXR9     | IO           | MCASP Serial Data (Input/Output) | AA25        |
| MCASP0_AXR10    | IO           | MCASP Serial Data (Input/Output) | V25         |
| MCASP0_AXR11    | IO           | MCASP Serial Data (Input/Output) | T24         |
| MCASP0_AXR12    | IO           | MCASP Serial Data (Input/Output) | AB25        |
| MCASP0_AXR13    | IO           | MCASP Serial Data (Input/Output) | T23         |
| MCASP0_AXR14    | IO           | MCASP Serial Data (Input/Output) | U24         |
| MCASP0_AXR15    | IO           | MCASP Serial Data (Input/Output) | AC25        |

**Table 5-90. MCASP1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALZ PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCASP1_ACLKR    | IO           | MCASP Receive Bit Clock          | AA28        |
| MCASP1_ACLKX    | IO           | MCASP Transmit Bit Clock         | AA24        |
| MCASP1_AFSR     | IO           | MCASP Receive Frame Sync         | AD27        |
| MCASP1_AFSX     | IO           | MCASP Transmit Frame Sync        | V28         |
| MCASP1_AXR0     | IO           | MCASP Serial Data (Input/Output) | T28         |
| MCASP1_AXR1     | IO           | MCASP Serial Data (Input/Output) | V27         |
| MCASP1_AXR2     | IO           | MCASP Serial Data (Input/Output) | W27         |
| MCASP1_AXR3     | IO           | MCASP Serial Data (Input/Output) | AD26        |
| MCASP1_AXR4     | IO           | MCASP Serial Data (Input/Output) | U25         |

**Table 5-91. MCASP2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]           | ALZ PIN [4] |
|-----------------|--------------|---------------------------|-------------|
| MCASP2_ACLKR    | IO           | MCASP Receive Bit Clock   | AB25        |
| MCASP2_ACLKX    | IO           | MCASP Transmit Bit Clock  | Y27         |
| MCASP2_AFSR     | IO           | MCASP Receive Frame Sync  | T23         |
| MCASP2_AFSX     | IO           | MCASP Transmit Frame Sync | AA27        |

**Table 5-91. MCASP2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALZ PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCASP2_AXR0     | IO           | MCASP Serial Data (Input/Output) | AA26        |
| MCASP2_AXR1     | IO           | MCASP Serial Data (Input/Output) | AC27        |
| MCASP2_AXR2     | IO           | MCASP Serial Data (Input/Output) | W28         |
| MCASP2_AXR3     | IO           | MCASP Serial Data (Input/Output) | R28         |
| MCASP2_AXR4     | IO           | MCASP Serial Data (Input/Output) | U24         |

**Table 5-92. MCASP3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALZ PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCASP3_ACLKR    | IO           | MCASP Receive Bit Clock          | AE27        |
| MCASP3_ACLKX    | IO           | MCASP Transmit Bit Clock         | AE27        |
| MCASP3_AFSR     | IO           | MCASP Receive Frame Sync         | AF26        |
| MCASP3_AFSX     | IO           | MCASP Transmit Frame Sync        | AF26        |
| MCASP3_AXR0     | IO           | MCASP Serial Data (Input/Output) | AH27        |
| MCASP3_AXR1     | IO           | MCASP Serial Data (Input/Output) | AG26        |
| MCASP3_AXR2     | IO           | MCASP Serial Data (Input/Output) | AH26        |

**Table 5-93. MCASP4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALZ PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| MCASP4_ACLKR    | IO           | MCASP Receive Bit Clock           | T25         |
| MCASP4_ACLKX    | IO           | MCASP Transmit Bit Clock          | AD28        |
| MCASP4_AFSR     | IO           | MCASP Receive Frame Sync          | W24         |
| MCASP4_AFSX     | IO           | MCASP Transmit Frame Sync         | V26         |
| MCASP4_AXR0     | IO           | MCASP Serial Data (Input/Output)  | AD24        |
| MCASP4_AXR1     | IO           | MCASP Serial Data (Input/Output)  | U28         |
| MCASP4_AXR2     | IO           | MCASP Serial Data (Input/Output)  | AB26        |
| MCASP4_AXR3     | IO           | MCASP Serial Data (Input/Output)  | R27         |
| MCASP4_AXR4     | IO           | MCASPI Serial Data (Input/Output) | AA25        |

**5.3.22 DMTIMER****5.3.22.1 MAIN Domain****Table 5-94. DMTIMER Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                            | ALZ PIN [4] |
|-----------------|--------------|----------------------------------------------------------------------------|-------------|
| TIMER_IO0       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AE25        |
| TIMER_IO1       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AG25        |
| TIMER_IO2       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | R22         |
| TIMER_IO3       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | R24         |
| TIMER_IO4       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | P24         |
| TIMER_IO5       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | M23         |
| TIMER_IO6       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | P23         |

**Table 5-94. DMTIMER Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                            | ALZ PIN [4] |
|-----------------|--------------|----------------------------------------------------------------------------|-------------|
| TIMER_IO7       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | N24         |

### 5.3.22.2 MCU Domain

**Table 5-95. MCU\_DMTIMER Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                            | ALZ PIN [4] |
|-----------------|--------------|----------------------------------------------------------------------------|-------------|
| MCU_TIMER_IO0   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | B25, C21    |
| MCU_TIMER_IO1   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | B26, F25    |
| MCU_TIMER_IO2   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | E22         |
| MCU_TIMER_IO3   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | E21         |
| MCU_TIMER_IO4   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | D23         |
| MCU_TIMER_IO5   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | C22         |
| MCU_TIMER_IO6   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | F24, G27    |
| MCU_TIMER_IO7   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | H26, J26    |
| MCU_TIMER_IO8   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | B24         |
| MCU_TIMER_IO9   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | D25         |

### 5.3.23 CPTS

#### 5.3.23.1 MAIN Domain

**Table 5-96. CPTS0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                 | ALZ PIN [4] |
|-----------------|--------------|---------------------------------|-------------|
| CPTS0_RFT_CLK   | I            | CPTS Reference Clock            | AB26        |
| CPTS0_TS_COMP   | O            | CPTS Time Stamp Counter Compare | AF26        |
| CPTS0_TS_SYNC   | O            | CPTS Time Stamp Counter Bit     | R24         |
| CPTS0_HW1TSPUSH | I            | CPTS Hardware Time Stamp Push 1 | AB26        |
| CPTS0_HW2TSPUSH | I            | CPTS Hardware Time Stamp Push 2 | AD28        |

#### 5.3.23.2 MCU Domain

**Table 5-97. MCU\_CPTS0 Signal Descriptions**

| SIGNAL NAME [1]     | PIN TYPE [2] | DESCRIPTION [3]                 | ALZ PIN [4] |
|---------------------|--------------|---------------------------------|-------------|
| MCU_CPTS0_RFT_CLK   | I            | CPTS Reference Clock            | F27, K26    |
| MCU_CPTS0_TS_COMP   | O            | CPTS Time Stamp Counter Compare | H26         |
| MCU_CPTS0_TS_SYNC   | O            | CPTS Time Stamp Counter Bit     | F24         |
| MCU_CPTS0_HW1TSPUSH | I            | CPTS Hardware Time Stamp Push 1 | E25         |
| MCU_CPTS0_HW2TSPUSH | I            | CPTS Hardware Time Stamp Push 2 | F28         |

### 5.3.24 DSS

#### 5.3.24.1 MAIN Domain

**Table 5-98. DSS0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                         | ALZ PIN [4] |
|-----------------|--------------|-----------------------------------------|-------------|
| DSS_FSYNC0      | O            | Video Output Frame Sync                 | V26, W25    |
| DSS_FSYNC1      | O            | Video Output Frame Sync                 | AC24, AD24  |
| DSS_FSYNC2      | O            | Video Output Frame Sync                 | AE28        |
| DSS_FSYNC3      | O            | Video Output Frame Sync                 | AF28        |
| VOUT0_DE        | O            | Video Output Data Enable                | AA28        |
| VOUT0_EXTCLKIN  | I            | Video Output External Pixel Clock Input | V26         |
| VOUT0_HSYNC     | O            | Video Output Horizontal Sync            | U26         |
| VOUT0_PCLK      | O            | Video Output Pixel Clock Output         | Y25         |
| VOUT0_VSYNC     | O            | Video Output Vertical Sync              | AD27        |
| VOUT0_DATA0     | O            | Video Output Data 0                     | R28         |
| VOUT0_DATA1     | O            | Video Output Data 1                     | R27         |
| VOUT0_DATA2     | O            | Video Output Data 2                     | T27         |
| VOUT0_DATA3     | O            | Video Output Data 3                     | U28         |
| VOUT0_DATA4     | O            | Video Output Data 4                     | W28         |
| VOUT0_DATA5     | O            | Video Output Data 5                     | AC27        |
| VOUT0_DATA6     | O            | Video Output Data 6                     | AA26        |
| VOUT0_DATA7     | O            | Video Output Data 7                     | AA27        |
| VOUT0_DATA8     | O            | Video Output Data 8                     | Y27         |
| VOUT0_DATA9     | O            | Video Output Data 9                     | W27         |
| VOUT0_DATA10    | O            | Video Output Data 10                    | V27         |
| VOUT0_DATA11    | O            | Video Output Data 11                    | AB27        |
| VOUT0_DATA12    | O            | Video Output Data 12                    | Y26         |
| VOUT0_DATA13    | O            | Video Output Data 13                    | AC28        |
| VOUT0_DATA14    | O            | Video Output Data 14                    | U27         |
| VOUT0_DATA15    | O            | Video Output Data 15                    | AB28        |
| VOUT0_DATA16    | O            | Video Output Data 16                    | AD28        |
| VOUT0_DATA17    | O            | Video Output Data 17                    | T26         |
| VOUT0_DATA18    | O            | Video Output Data 18                    | R28, V23    |
| VOUT0_DATA19    | O            | Video Output Data 19                    | AB24, R27   |
| VOUT0_DATA20    | O            | Video Output Data 20                    | Y27, Y28    |
| VOUT0_DATA21    | O            | Video Output Data 21                    | AA23, W27   |
| VOUT0_DATA22    | O            | Video Output Data 22                    | T26, Y24    |
| VOUT0_DATA23    | O            | Video Output Data 23                    | AB26, W23   |
| VOUT0_VP0_DE    | O            | Alternative Output Data Enable          | AA28        |
| VOUT0_VP0_HSYNC | O            | Alternative Output Horizontal Sync      | U26         |
| VOUT0_VP0_VSYNC | O            | Alternative Output Vertical Sync        | AD27        |
| VOUT0_VP2_DE    | O            | Alternative Output Data Enable          | AA28        |
| VOUT0_VP2_HSYNC | O            | Alternative Output Horizontal Sync      | U26         |
| VOUT0_VP2_VSYNC | O            | Alternative Output Vertical Sync        | AD27        |

### 5.3.25 GPMC

#### 5.3.25.1 MAIN Domain

**Table 5-99. GPMC0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                             | ALZ PIN [4] |
|-----------------|--------------|---------------------------------------------------------------------------------------------|-------------|
| GPMC0_ADVn_ALE  | O            | GPMC Address Valid (active low) or Address Latch Enable                                     | AB27        |
| GPMC0_CLK       | IO           | GPMC clock                                                                                  | W25         |
| GPMC0_CLKOUT    | O            | GPMC clock generated for external synchronization                                           | AD27        |
| GPMC0_DIR       | O            | GPMC Data Bus Signal Direction Control                                                      | R28, Y25    |
| GPMC0_OEn_REn   | O            | GPMC Output Enable (active low) or Read Enable (active low)                                 | U26         |
| GPMC0_WEn       | O            | GPMC Write Enable (active low)                                                              | AD24        |
| GPMC0_WPn       | O            | GPMC Flash Write Protect (active low)                                                       | AB27        |
| GPMC0_A0        | OZ           | GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories | T25         |
| GPMC0_A1        | OZ           | GPMC Address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode    | W24         |
| GPMC0_A2        | OZ           | GPMC Address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode    | AA25        |
| GPMC0_A3        | OZ           | GPMC Address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode    | V25         |
| GPMC0_A4        | OZ           | GPMC Address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode    | T24         |
| GPMC0_A5        | OZ           | GPMC Address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode    | AB25        |
| GPMC0_A6        | OZ           | GPMC Address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode    | T23         |
| GPMC0_A7        | OZ           | GPMC Address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode    | U24         |
| GPMC0_A8        | OZ           | GPMC Address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode    | AC25        |
| GPMC0_A9        | OZ           | GPMC Address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode    | AD26        |
| GPMC0_A10       | OZ           | GPMC Address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode   | U25         |
| GPMC0_A11       | OZ           | GPMC Address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | AA24        |
| GPMC0_A12       | OZ           | GPMC Address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | V28         |
| GPMC0_A13       | OZ           | GPMC Address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | T28         |
| GPMC0_A14       | OZ           | GPMC Address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | T25, V23    |
| GPMC0_A15       | OZ           | GPMC Address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | AB24        |
| GPMC0_A16       | OZ           | GPMC Address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | Y28         |
| GPMC0_A17       | OZ           | GPMC Address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | AA23        |
| GPMC0_A18       | OZ           | GPMC Address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | Y24         |
| GPMC0_A19       | OZ           | GPMC Address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | W23         |

**Table 5-99. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                  | ALZ PIN [4] |
|-----------------|--------------|------------------------------------------------------------------------------------------------------------------|-------------|
| GPMC0_A20       | OZ           | GPMC Address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                            | AD25        |
| GPMC0_A21       | OZ           | GPMC Address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                            | AF28        |
| GPMC0_A22       | OZ           | GPMC Address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                            | AE28        |
| GPMC0_A23       | OZ           | GPMC Address 23 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                            | AC24        |
| GPMC0_A24       | OZ           | GPMC Address 24 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                            | W25         |
| GPMC0_AD0       | IO           | GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode   | AB28        |
| GPMC0_AD1       | IO           | GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode   | U27         |
| GPMC0_AD2       | IO           | GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode   | AC28        |
| GPMC0_AD3       | IO           | GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode   | Y26         |
| GPMC0_AD4       | IO           | GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode   | T26         |
| GPMC0_AD5       | IO           | GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode   | AB26        |
| GPMC0_AD6       | IO           | GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode   | AD28        |
| GPMC0_AD7       | IO           | GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode   | V26         |
| GPMC0_AD8       | IO           | GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode   | V27         |
| GPMC0_AD9       | IO           | GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode  | W27         |
| GPMC0_AD10      | IO           | GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode | Y27         |
| GPMC0_AD11      | IO           | GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode | AA27        |
| GPMC0_AD12      | IO           | GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode | AA26        |
| GPMC0_AD13      | IO           | GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode | AC27        |
| GPMC0_AD14      | IO           | GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode | W28         |

**Table 5-99. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                  | ALZ PIN [4] |
|-----------------|--------------|------------------------------------------------------------------------------------------------------------------|-------------|
| GPMC0_AD15      | IO           | GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode | U28         |
| GPMC0_BE0n_CLE  | O            | GPMC Lower-Byte Enable (active low) or Command Latch Enable                                                      | R27         |
| GPMC0_BE1n      | O            | GPMC Upper-Byte Enable (active low)                                                                              | T27         |
| GPMC0_CS0       | O            | GPMC Chip Select 0 (active low)                                                                                  | AA28        |
| GPMC0_CS1       | O            | GPMC Chip Select 1 (active low)                                                                                  | Y25         |
| GPMC0_CS2       | O            | GPMC Chip Select 2 (active low)                                                                                  | T25, V23    |
| GPMC0_CS3       | O            | GPMC Chip Select 3 (active low)                                                                                  | AC24        |
| GPMC0_WAIT0     | I            | GPMC External Indication of Wait                                                                                 | R28         |
| GPMC0_WAIT1     | I            | GPMC External Indication of Wait                                                                                 | AB24        |
| GPMC0_WAIT2     | I            | GPMC External Indication of Wait                                                                                 | AE28        |
| GPMC0_WAIT3     | I            | GPMC External Indication of Wait                                                                                 | T28         |

### 5.3.26 MMC

#### 5.3.26.1 MAIN Domain

**Table 5-100. MMC0 Signal Descriptions**

| SIGNAL NAME [1]            | PIN TYPE [2] | DESCRIPTION [3]                  | ALZ PIN [4] |
|----------------------------|--------------|----------------------------------|-------------|
| MMC0_CALPAD <sup>(1)</sup> | A            | MMC/SD/SDIO Calibration Resistor | AF1         |
| MMC0_CLK                   | O            | MMC/SD/SDIO Clock                | AC6         |
| MMC0_CMD                   | IO           | MMC/SD/SDIO Command              | AF2         |
| MMC0_DS                    | IO           | MMC Data Strobe                  | AE3         |
| MMC0_DAT0                  | IO           | MMC/SD/SDIO Data                 | AF4         |
| MMC0_DAT1                  | IO           | MMC/SD/SDIO Data                 | AD3         |
| MMC0_DAT2                  | IO           | MMC/SD/SDIO Data                 | AD4         |
| MMC0_DAT3                  | IO           | MMC/SD/SDIO Data                 | AF3         |
| MMC0_DAT4                  | IO           | MMC/SD/SDIO Data                 | AE2         |
| MMC0_DAT5                  | IO           | MMC/SD/SDIO Data                 | AG3         |
| MMC0_DAT6                  | IO           | MMC/SD/SDIO Data                 | AE1         |
| MMC0_DAT7                  | IO           | MMC/SD/SDIO Data                 | AG1         |

(1) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

**Table 5-101. MMC1 Signal Descriptions**

| SIGNAL NAME [1]          | PIN TYPE [2] | DESCRIPTION [3]     | ALZ PIN [4] |
|--------------------------|--------------|---------------------|-------------|
| MMC1_CLK <sup>(2)</sup>  | IO           | MMC/SD/SDIO Clock   | P23         |
| MMC1_CMD                 | IO           | MMC/SD/SDIO Command | N24         |
| MMC1_SDCD <sup>(1)</sup> | I            | SD Card Detect      | AE25        |
| MMC1_SDWP                | I            | SD Write Protect    | AG25        |
| MMC1_DAT0                | IO           | MMC/SD/SDIO Data    | M23         |
| MMC1_DAT1                | IO           | MMC/SD/SDIO Data    | P24         |
| MMC1_DAT2                | IO           | MMC/SD/SDIO Data    | R24         |
| MMC1_DAT3                | IO           | MMC/SD/SDIO Data    | R22         |

- (1) For ROM boot from MMC1 interface to work properly, the MMC1\_SDCD pin should be pulled low externally with a resistor to indicate an SD Card/Memory device is present.
- (2) For MMC1\_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR\_PADCONFIG64 register should be set to 0x1 because of retiming purposes.

### 5.3.27 OSPI

#### 5.3.27.1 MCU Domain

**Table 5-102. MCU\_OSPI0 Signal Descriptions**

| SIGNAL NAME [1]      | PIN TYPE [2] | DESCRIPTION [3]                                | ALZ PIN [4] |
|----------------------|--------------|------------------------------------------------|-------------|
| MCU_OSPI0_CLK        | O            | OSPI Clock                                     | D19         |
| MCU_OSPI0_DQS        | I            | OSPI Data Strobe (DQS) or Loopback Clock Input | E18         |
| MCU_OSPI0_ECC_FAIL   | I            | OSPI ECC Status                                | B19, F17    |
| MCU_OSPI0_LBCLKO     | IO           | OSPI Loopback Clock Output                     | E20         |
| MCU_OSPI0_CSn0       | O            | OSPI Chip Select 0 (active low)                | F15         |
| MCU_OSPI0_CSn1       | O            | OSPI Chip Select 1 (active low)                | G17         |
| MCU_OSPI0_CSn2       | O            | OSPI Chip Select 2 (active low)                | B20, F14    |
| MCU_OSPI0_CSn3       | O            | OSPI Chip Select 3 (active low)                | B19, F17    |
| MCU_OSPI0_D0         | IO           | OSPI Data 0                                    | C19         |
| MCU_OSPI0_D1         | IO           | OSPI Data 1                                    | F16         |
| MCU_OSPI0_D2         | IO           | OSPI Data 2                                    | G15         |
| MCU_OSPI0_D3         | IO           | OSPI Data 3                                    | F18         |
| MCU_OSPI0_D4         | IO           | OSPI Data 4                                    | E19         |
| MCU_OSPI0_D5         | IO           | OSPI Data 5                                    | G19         |
| MCU_OSPI0_D6         | IO           | OSPI Data 6                                    | F19         |
| MCU_OSPI0_D7         | IO           | OSPI Data 7                                    | F20         |
| MCU_OSPI0_RESET_OUT0 | O            | OSPI Reset                                     | B20, F14    |
| MCU_OSPI0_RESET_OUT1 | O            | OSPI Reset                                     | C21, F17    |

**Table 5-103. MCU\_OSPI1 Signal Descriptions**

| SIGNAL NAME [1]  | PIN TYPE [2] | DESCRIPTION [3]                                | ALZ PIN [4] |
|------------------|--------------|------------------------------------------------|-------------|
| MCU_OSPI1_CLK    | O            | OSPI Clock                                     | A19         |
| MCU_OSPI1_DQS    | I            | OSPI Data Strobe (DQS) or Loopback Clock Input | B19         |
| MCU_OSPI1_LBCLKO | IO           | OSPI Loopback Clock Output                     | B20         |
| MCU_OSPI1_CSn0   | O            | OSPI Chip Select 0 (active low)                | D20         |
| MCU_OSPI1_CSn1   | O            | OSPI Chip Select 1 (active low)                | C21         |
| MCU_OSPI1_D0     | IO           | OSPI Data 0                                    | D21         |
| MCU_OSPI1_D1     | IO           | OSPI Data 1                                    | G20         |
| MCU_OSPI1_D2     | IO           | OSPI Data 2                                    | C20         |
| MCU_OSPI1_D3     | IO           | OSPI Data 3                                    | A20         |

### 5.3.28 Hyperbus

#### 5.3.28.1 MCU Domain

**Table 5-104. MCU\_HYPERBUS0 Signal Descriptions**

| SIGNAL NAME [1]       | PIN TYPE [2] | DESCRIPTION [3]                                                   | ALZ PIN [4]   |
|-----------------------|--------------|-------------------------------------------------------------------|---------------|
| MCU_HYPERBUS0_CK      | O            | Hyperbus Differential Clock (positive)                            | D19           |
| MCU_HYPERBUS0_CKn     | O            | Hyperbus Differential Clock (negative)                            | E20           |
| MCU_HYPERBUS0_INTn    | I            | Hyperbus Interrupt (active low)                                   | B19, F17      |
| MCU_HYPERBUS0_RESETn  | O            | Hyperbus Reset (active low) Output                                | G17           |
| MCU_HYPERBUS0_RESETOn | I            | Hyperbus Reset Status Indicator (active low) from Hyperbus Memory | B20, F14      |
| MCU_HYPERBUS0_RWDS    | IO           | Hyperbus Read-Write Data Strobe                                   | E18           |
| MCU_HYPERBUS0_WPn     | O            | Hyperbus Write Protect (Not in use)                               | C21, F14, F17 |

**Table 5-104. MCU\_HYPERBUS0 Signal Descriptions (continued)**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]        | ALZ PIN [4] |
|-------------------|--------------|------------------------|-------------|
| MCU_HYPERBUS0_CS0 | O            | Hyperbus Chip Select 0 | F15         |
| MCU_HYPERBUS0_CS1 | O            | Hyperbus Chip Select 1 | C21, F14    |
| MCU_HYPERBUS0_DQ0 | IO           | Hyperbus Data 0        | C19         |
| MCU_HYPERBUS0_DQ1 | IO           | Hyperbus Data 1        | F16         |
| MCU_HYPERBUS0_DQ2 | IO           | Hyperbus Data 2        | G15         |
| MCU_HYPERBUS0_DQ3 | IO           | Hyperbus Data 3        | F18         |
| MCU_HYPERBUS0_DQ4 | IO           | Hyperbus Data 4        | E19         |
| MCU_HYPERBUS0_DQ5 | IO           | Hyperbus Data 5        | G19         |
| MCU_HYPERBUS0_DQ6 | IO           | Hyperbus Data 6        | F19         |
| MCU_HYPERBUS0_DQ7 | IO           | Hyperbus Data 7        | F20         |

### 5.3.29 Emulation and Debug

#### 5.3.29.1 MAIN Domain

**Table 5-105. JTAG Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]             | ALZ PIN [4] |
|-----------------|--------------|-----------------------------|-------------|
| EMU0            | IO           | Emulation Control 0         | A27         |
| EMU1            | IO           | Emulation Control 1         | C26         |
| TCK             | I            | JTAG Test Clock Input       | A25         |
| TDI             | I            | JTAG Test Data Input        | AG28        |
| TDO             | OZ           | JTAG Test Data Output       | AE26        |
| TMS             | I            | JTAG Test Mode Select Input | AG27        |
| TRSTn           | I            | JTAG Reset                  | B28         |

**Table 5-106. Trace Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| TRC_CLK         | O            | Trace Clock     | AD28, W25   |
| TRC_CTL         | O            | Trace Control   | AC24, V26   |
| TRC_DATA0       | O            | Trace Data 0    | AD24, AE28  |
| TRC_DATA1       | O            | Trace Data 1    | AB26, AF28  |
| TRC_DATA2       | O            | Trace Data 2    | AD25, T26   |
| TRC_DATA3       | O            | Trace Data 3    | R28, W23    |
| TRC_DATA4       | O            | Trace Data 4    | Y27         |
| TRC_DATA5       | O            | Trace Data 5    | R27         |
| TRC_DATA6       | O            | Trace Data 6    | W27         |
| TRC_DATA7       | O            | Trace Data 7    | T27         |
| TRC_DATA8       | O            | Trace Data 8    | V27         |
| TRC_DATA9       | O            | Trace Data 9    | AA27        |
| TRC_DATA10      | O            | Trace Data 10   | AB27        |
| TRC_DATA11      | O            | Trace Data 11   | W28         |
| TRC_DATA12      | O            | Trace Data 12   | Y26         |
| TRC_DATA13      | O            | Trace Data 13   | AC27        |
| TRC_DATA14      | O            | Trace Data 14   | AC28        |
| TRC_DATA15      | O            | Trace Data 15   | AA26        |
| TRC_DATA16      | O            | Trace Data 16   | U28         |
| TRC_DATA17      | O            | Trace Data 17   | Y25         |

**Table 5-106. Trace Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| TRC_DATA18      | O            | Trace Data 18   | U26         |
| TRC_DATA19      | O            | Trace Data 19   | AA28        |
| TRC_DATA20      | O            | Trace Data 20   | AD27        |
| TRC_DATA21      | O            | Trace Data 21   | Y24         |
| TRC_DATA22      | O            | Trace Data 22   | AA23        |
| TRC_DATA23      | O            | Trace Data 23   | Y28         |
| TRC_DATA24      | O            | Trace Data 24   | AB24        |
| TRC_DATA25      | O            | Trace Data 25   | V23         |

### 5.3.30 System and Miscellaneous

#### 5.3.30.1 Boot Mode configuration

**Table 5-107. Sysboot Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| BOOTMODE00      | I            | Bootmode Pin 0     | C19         |
| BOOTMODE01      | I            | Bootmode Pin 1     | F16         |
| BOOTMODE02      | I            | Bootmode Pin 2     | E19         |
| BOOTMODE03      | I            | Bootmode Pin 3     | G19         |
| BOOTMODE04      | I            | Bootmode Pin 4     | G27         |
| BOOTMODE05      | I            | Bootmode Pin 5     | J26         |
| BOOTMODE06      | I            | Bootmode Pin 6     | G25         |
| BOOTMODE07      | I            | Bootmode Pin 7     | J27         |
| MCU_BOOTMODE00  | I            | MCU Bootmode Pin 0 | B27         |
| MCU_BOOTMODE01  | I            | MCU Bootmode Pin 1 | D24         |
| MCU_BOOTMODE02  | I            | MCU Bootmode Pin 2 | B25         |
| MCU_BOOTMODE03  | I            | MCU Bootmode Pin 3 | D26         |
| MCU_BOOTMODE04  | I            | MCU Bootmode Pin 4 | E24         |
| MCU_BOOTMODE05  | I            | MCU Bootmode Pin 5 | C28         |
| MCU_BOOTMODE06  | I            | MCU Bootmode Pin 6 | B24         |
| MCU_BOOTMODE07  | I            | MCU Bootmode Pin 7 | D25         |
| MCU_BOOTMODE08  | I            | MCU Bootmode Pin 8 | C25         |
| MCU_BOOTMODE09  | I            | MCU Bootmode Pin 9 | C24         |

#### 5.3.30.2 Clock

**Table 5-108. Clock0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                             | ALZ PIN [4] |
|-----------------|--------------|---------------------------------------------|-------------|
| WKUP_LF_CLKIN   | I            | Low Frequency (32.768 KHz) Oscillator Input | J27         |
| WKUP_OSC0_XI    | I            | High Frequency Oscillator Input             | H28         |
| WKUP_OSC0_XO    | O            | High Frequency Oscillator Output            | J28         |

**Table 5-109. Clock1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALZ PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| OSC1_XI         | I            | High Frequency Oscillator Input  | M28         |
| OSC1_XO         | O            | High Frequency Oscillator Output | L28         |

### 5.3.30.3 System

**Table 5-110. MCU System Signal Descriptions**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                                 | ALZ PIN [4] |
|-------------------|--------------|-----------------------------------------------------------------|-------------|
| MCU_CLKOUT0       | OZ           | Reference clock output for Ethernet PHYs (50MHz or 25MHz)       | F25         |
| MCU_EXT_REFCLK0   | I            | External system clock input                                     | F27, K26    |
| MCU_OBSCLK0       | O            | Observation clock output for test and debug purposes only       | C26, F25    |
| MCU_PORz          | I            | MCU Domain Cold Reset                                           | G23         |
| MCU_RESETSTATz    | O            | MCU Domain Warm Reset status output                             | A23         |
| MCU_RESETz        | I            | MCU Domain Warm Reset                                           | A26         |
| MCU_SAFETY_ERRORn | IO           | Error signal output from MCU Domain ESM                         | J23         |
| MCU_SYSCLKOUT0    | O            | MCU Domain system clock output for test and debug purposes only | F27         |

**Table 5-111. System Signal Descriptions**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                                                                                                                                                    | ALZ PIN [4] |
|-------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| AUDIO_EXT_REFCLK0 | IO           | External clock routed to ATL or McASP as one of the selectable input clock sources, or as a output clock output for ATL or McASP                                                   | AD24        |
| AUDIO_EXT_REFCLK1 | IO           | External clock routed to ATL or McASP as one of the selectable input clock sources, or as a output clock output for ATL or McASP                                                   | Y25         |
| EXTINTn           | I            | External Interrupt                                                                                                                                                                 | AG24        |
| EXT_REFCLK1       | I            | External clock input to Main Domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL) | AD28        |
| GPMC0_FCLK_MUX    | O            | GPMC functional clock output selected through a mux logic                                                                                                                          | AD27        |
| OBSCLK0           | O            | Observation clock output for test and debug purposes only                                                                                                                          | AG25        |
| OBSCLK1           | O            | Observation clock output for test and debug purposes only                                                                                                                          | Y26         |
| PMIC_POWER_EN1    | O            | Power enable output for MAIN Domain supplies                                                                                                                                       | G26         |
| PMIC_WAKE0        | O            | PMIC WakeUp (active low)                                                                                                                                                           | AD24        |
| PMIC_WAKE1        | O            | PMIC WakeUp (active low)                                                                                                                                                           | K26         |
| PORz              | I            | SoC PORz Reset Signal                                                                                                                                                              | K23         |
| RESETSTATz        | O            | Main Domain Warm Reset status output                                                                                                                                               | AF27        |
| RESET_REQz        | I            | Main Domain external Warm Reset request input                                                                                                                                      | A24         |
| SOC_SAFETY_ERRORn | IO           | Error signal output from Main Domain ESM                                                                                                                                           | AF25        |
| SYNC0_OUT         | O            | CPTS Time Stamp Generator Bit 0                                                                                                                                                    | AB26        |
| SYNC1_OUT         | O            | CPTS Time Stamp Generator Bit 1                                                                                                                                                    | AD28        |
| SYNC2_OUT         | O            | CPTS Time Stamp Generator Bit 2                                                                                                                                                    | T28         |
| SYNC3_OUT         | O            | CPTS Time Stamp Generator Bit 3                                                                                                                                                    | Y27         |
| SYSCLKOUT0        | O            | SYSCLK0 output from Main PLL controller (divided by 6) for test and debug purposes only                                                                                            | AE25        |

## 5.3.30.4 EFUSE

Table 5-112. EFUSE Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                            | ALZ PIN [4] |
|-----------------|--------------|--------------------------------------------|-------------|
| VPP_CORE        | PWR          | Programming Voltage for MAIN Domain Efuses | V22         |
| VPP_MCU         | PWR          | Programming Voltage for MCU Domain Efuses  | H22         |

## 5.3.30.5 VMON

Table 5-113. VMON Signal Descriptions

| SIGNAL NAME [1]  | PIN TYPE [2] | DESCRIPTION [3]                                                                                                                                             | ALZ PIN [4] |
|------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| VMON1_ER_VSYS    | A            | Voltage Monitor, fixed 0.45V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply. | H23         |
| VMON2_IR_VCPU    | A            | Recommended to be externally connected directly to VDD_CPU                                                                                                  | M18         |
| VMON3_IR_VEXT1P8 | A            | General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor divider.                                                      | L22         |
| VMON4_IR_VEXT1P8 | A            | General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor divider.                                                      | N19         |
| VMON5_IR_VEXT3P3 | A            | General purpose voltage monitor for external supplies, 3.3V threshold. With internal resistor divider.                                                      | N20         |
| VMON6_IR_VEXT0P8 | A            | General purpose voltage monitor for external supplies, 0.8V threshold. With internal resistor divider.                                                      | L18         |

## 5.3.31 Power

Table 5-114. Power Supply Signal Descriptions

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]               | ALZ PIN [4]            |
|------------------------------|--------------|-------------------------------|------------------------|
| CAP_VDDS0 <sup>(1)</sup>     | CAP          | External Capacitor Connection | T21                    |
| CAP_VDDS0_MCU <sup>(1)</sup> | CAP          | External Capacitor Connection | J20                    |
| CAP_VDDS1_MCU <sup>(1)</sup> | CAP          | External Capacitor Connection | G16                    |
| CAP_VDDS2 <sup>(1)</sup>     | CAP          | External Capacitor Connection | P21                    |
| CAP_VDDS2_MCU <sup>(1)</sup> | CAP          | External Capacitor Connection | H17                    |
| CAP_VDDS5 <sup>(1)</sup>     | CAP          | External Capacitor Connection | M22                    |
| VDDAR_CORE                   | PWR          | Core RAM Supply               | N17, V11, V16, Y20     |
| VDDAR_CPU                    | PWR          | CPU RAM Supply                | H9, K14, P11, P14, V13 |
| VDDAR_MCU                    | PWR          | MCU RAM Supply                | K17, K19               |
| VDDA_0P8_DSITX               | PWR          | Analog Supply for DSITX       | AB14                   |
| VDDA_0P8_DSITX_C             | PWR          | DSITX Clock Supply            | AB15                   |
| VDDA_0P8_USB                 | PWR          | USB 0.8V Supply               | AB8                    |
| VDDA_0P8_CSIRX0_1            | PWR          | Analog Supply for CSIRX       | AB17, AB18             |
| VDDA_0P8_DLL_MMC0            | PWR          | MMC DLL Analog Supply         | W7                     |
| VDDA_0P8_PLL_DDR0            | PWR          | DDR de-skew PLL Analog Supply | P10                    |
| VDDA_0P8_PLL_DDR1            | PWR          | DDR de-skew PLL Analog Supply | J14                    |
| VDDA_0P8_SERDES0_1           | PWR          | SERDES 0.8V Supply            | AB10, AB11             |
| VDDA_0P8_SERDES_C0_1         | PWR          | SERDES 0.8V Clock Supply      | AA10, AA11             |
| VDDA_1P8_DSITX               | PWR          | Analog Supply for DSITX       | AA14, AA15             |
| VDDA_1P8_USB                 | PWR          | USB 1.8V Supply               | AB7                    |
| VDDA_1P8_CSIRX0_1            | PWR          | Analog Supply for CSIRX       | AA17, AA19             |
| VDDA_1P8_SERDES0_1           | PWR          | SERDES 1.8V Supply            | AA12                   |
| VDDA_1P8_SERDES2_4           | PWR          | SERDES 1.8V Supply            | AB13                   |

**Table 5-114. Power Supply Signal Descriptions (continued)**

| SIGNAL NAME [1]  | PIN TYPE [2] | DESCRIPTION [3]                          | ALZ PIN [4]                                                                                                                                       |
|------------------|--------------|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| VDDA_3P3_USB     | PWR          | USB 3.3V Supply                          | AB9                                                                                                                                               |
| VDDA_ADC0        | PWR          | ADC0 Analog Supply                       | J21                                                                                                                                               |
| VDDA_ADC1        | PWR          | ADC1 Analog Supply                       | K21                                                                                                                                               |
| VDDA_MCU_PLLGRP0 | PWR          | Analog Supply for MCU PLL Group 0        | K22                                                                                                                                               |
| VDDA_MCU_TEMP    | PWR          | Analog Supply for MCU temperature sensor | J17                                                                                                                                               |
| VDDA_OSC1        | PWR          | HFOSC1 Supply                            | L21                                                                                                                                               |
| VDDA_PLLGRP0     | PWR          | Analog Supply for MAIN PLL Group 0       | U18                                                                                                                                               |
| VDDA_PLLGRP1     | PWR          | Analog Supply for MAIN PLL Group 1       | V19                                                                                                                                               |
| VDDA_PLLGRP2     | PWR          | Analog Supply for MAIN PLL Group 2       | Y11                                                                                                                                               |
| VDDA_PLLGRP5     | PWR          | Analog Supply for MAIN PLL Group 5       | N14                                                                                                                                               |
| VDDA_PLLGRP6     | PWR          | Analog Supply for MAIN PLL Group 6       | R12                                                                                                                                               |
| VDDA_PLLGRP7     | PWR          | Analog Supply for MAIN PLL Group 7       | R11                                                                                                                                               |
| VDDA_PLLGRP8     | PWR          | Analog Supply for MAIN PLL Group 8       | K12                                                                                                                                               |
| VDDA_PLLGRP9     | PWR          | Analog Supply for MAIN PLL Group 9       | T18                                                                                                                                               |
| VDDA_PLLGRP10    | PWR          | Analog Supply for MAIN PLL Group 10      | Y16                                                                                                                                               |
| VDDA_PLLGRP12    | PWR          | Analog Supply for MAIN PLL Group 12      | Y18                                                                                                                                               |
| VDDA_PLLGRP13    | PWR          | Analog Supply for MAIN PLL Group 13      | V12                                                                                                                                               |
| VDDA_POR_WKUP    | PWR          | WKUP domain Analog Supply                | L20                                                                                                                                               |
| VDDA_TEMP0       | PWR          | Analog Supply for temperature sensor 0   | U19                                                                                                                                               |
| VDDA_TEMP1       | PWR          | Analog Supply for temperature sensor 1   | K10                                                                                                                                               |
| VDDA_TEMP2       | PWR          | Analog Supply for temperature sensor 2   | T16                                                                                                                                               |
| VDDA_TEMP3       | PWR          | Analog Supply for temperature sensor 3   | U10                                                                                                                                               |
| VDDA_TEMP4       | PWR          | Analog Supply for temperature sensor 4   | Y14                                                                                                                                               |
| VDDA_WKUP        | PWR          | Oscillator Supply for WKUP domain        | J22                                                                                                                                               |
| VDDSHV0          | PWR          | IO Power Supply                          | R21, U21, U22                                                                                                                                     |
| VDDSHV0_MCU      | PWR          | IO Power Supply                          | H19, H20                                                                                                                                          |
| VDDSHV1_MCU      | PWR          | IO Power Supply                          | H16, J16                                                                                                                                          |
| VDDSHV2          | PWR          | IO Power Supply                          | M20, R20                                                                                                                                          |
| VDDSHV2_MCU      | PWR          | IO Power Supply                          | G18, H18                                                                                                                                          |
| VDDSHV5          | PWR          | IO Power Supply                          | M21, N22                                                                                                                                          |
| VDDS_DDR         | PWR          | DDR PHY IO Supply                        | A1, A18, AA1, G10, G12, G14, G6, H11, H13, H15, J6, L6, N6, N9, P7, P8, R6, U9                                                                    |
| VDDS_DDR_C0      | PWR          | IO Power Supply for DDR Clock            | R9                                                                                                                                                |
| VDDS_DDR_C1      | PWR          | IO Power Supply for DDR Clock            | J12                                                                                                                                               |
| VDDS_MMC0        | PWR          | MMC0 PHY IO Supply                       | Y7, Y8                                                                                                                                            |
| VDD_CORE         | PWR          | MAIN domain core Supply                  | AA21, AB20, J13, J15, M16, M19, N10, P18, R17, R19, T10, T20, U15, U17, U8, V14, V18, V20, V7, V9, W10, W13, W15, W17, W19, W21, W8, Y12, Y22, Y9 |
| VDD_CPU          | PWR          | CPU core Supply                          | G8, H7, J8, K11, K13, K7, K9, L8, M14, M7, M9, N11, N15, P16, R13, R15, T12, T14, U11, U13                                                        |
| VDD_MCU          | PWR          | MCU core Supply                          | K16, K18, L15, L17, L19                                                                                                                           |

**Table 5-114. Power Supply Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                         | ALZ PIN [4]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----------------|--------------|-----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD_MCU_WAKE1   | PWR          | Core Supply for MCU daisy chain         | J19                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| VDD_WAKE0       | PWR          | Core Supply for MAIN domain daisy chain | P20                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| VSS             | GND          | Ground                                  | A14, A5, AA13, AA16, AA18, AA20, AA22, AA3, AA5, AA7, AA9, AB12, AB16, AB19, AB2, AB21, AB23, AB4, AB6, AC11, AC22, AC26, AC3, AC5, AC7, AC8, AD15, AD18, AD21, AD6, AD9, AE10, AE14, AE17, AE20, AE23, AE4, AE7, AF12, AF15, AF18, AF21, AF24, AF5, AF8, AG10, AG14, AG17, AG20, AG23, AG4, AG7, AH1, AH12, AH15, AH18, AH21, AH24, AH3, AH6, AH9, B11, B13, B15, B17, B2, B23, B4, B6, B8, C1, C12, C14, C16, C18, C3, C5, C7, D11, D13, D15, D17, D2, D4, D6, D8, E1, E12, E14, E16, E26, E3, E5, E7, F2, F4, F6, G13, G28, G3, G5, G7, G9, H10, H12, H14, H2, H21, H4, H6, H8, J1, J11, J18, J24, J3, J5, J7, J9, K15, K2, K20, K27, K4, K6, K8, L14, L16, L3, L5, L7, L9, M15, M17, M2, M25, M4, M6, M8, N1, N16, N18, N21, N23, N3, N7, P15, P17, P19, P22, P6 |
| VSS (continued) | GND          | Ground                                  | P9, R10, R14, R16, R18, R23, R26, R7, T11, T13, T15, T17, T19, T2, T22, T4, T6, T9, U12, U14, U16, U20, U23, U3, U5, U7, V10, V15, V17, V2, V21, V24, V4, V6, V8, W1, W11, W12, W14, W16, W18, W20, W22, W26, W3, W6, W9, Y10, Y13, Y15, Y17, Y19, Y2, Y21, Y23, Y4, Y6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

(1) This pin must always be connected via a 1- $\mu$ F  $\pm$ 10% capacitor to VSS.

## 5.4 Connection for Unused Pins

This section describes connectivity requirements for package balls that have specific connectivity requirements and unused package balls.

### Note

All power balls must be supplied with the voltages specified in the [Recommended Operating Conditions](#) section, unless otherwise specified in [Signal Descriptions](#).

### Note

For additional clarification, "left unconnected" or "no connect" (NC) means no signal traces can be connected to these device ball number.

Table 5-115 shows the connectivity requirements for specific signals by ball name and ball number.

**Table 5-115. Connectivity Requirements**

| BALL<br>NUMBER | BALL NAME        | CONNECTION REQUIREMENT                                                                                                                                                                          |
|----------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H28            | WKUP_OSC0_XI     | Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level, if unused.                                    |
| M28            | OSC1_XI          |                                                                                                                                                                                                 |
| B28            | TRSTN            |                                                                                                                                                                                                 |
| G1             | DDR0_DQS0P       |                                                                                                                                                                                                 |
| L1             | DDR0_DQS1P       |                                                                                                                                                                                                 |
| V1             | DDR0_DQS2P       |                                                                                                                                                                                                 |
| AB1            | DDR0_DQS3P       |                                                                                                                                                                                                 |
| A16            | DDR1_DQS0P       |                                                                                                                                                                                                 |
| A13            | DDR1_DQS1P       |                                                                                                                                                                                                 |
| A6             | DDR1_DQS2P       |                                                                                                                                                                                                 |
| A3             | DDR1_DQS3P       |                                                                                                                                                                                                 |
| T8             | DDR0_RET         |                                                                                                                                                                                                 |
| J10            | DDR1_RET         |                                                                                                                                                                                                 |
| H23            | VMON1_ER_VSYS    |                                                                                                                                                                                                 |
| L18            | VMON6_IR_VEXT0P8 |                                                                                                                                                                                                 |
| L22            | VMON3_IR_VEXT1P8 |                                                                                                                                                                                                 |
| M18            | VMON2_IR_VCPU    |                                                                                                                                                                                                 |
| N19            | VMON4_IR_VEXT1P8 |                                                                                                                                                                                                 |
| N20            | VMON5_IR_VEXT3P3 |                                                                                                                                                                                                 |
| L25            | MCU_ADC0_AIN0    | Each of these balls can be connected to VSS through a separate external pull resistor or can be connected directly to VSS to ensure these balls are held to a valid logic low-level, if unused. |
| K25            | MCU_ADC0_AIN1    |                                                                                                                                                                                                 |
| M24            | MCU_ADC0_AIN2    |                                                                                                                                                                                                 |
| L24            | MCU_ADC0_AIN3    |                                                                                                                                                                                                 |
| L27            | MCU_ADC0_AIN4    |                                                                                                                                                                                                 |
| K24            | MCU_ADC0_AIN5    |                                                                                                                                                                                                 |
| M27            | MCU_ADC0_AIN6    |                                                                                                                                                                                                 |
| M26            | MCU_ADC0_AIN7    |                                                                                                                                                                                                 |
| P25            | MCU_ADC1_AIN0    |                                                                                                                                                                                                 |
| R25            | MCU_ADC1_AIN1    |                                                                                                                                                                                                 |
| P28            | MCU_ADC1_AIN2    |                                                                                                                                                                                                 |
| P27            | MCU_ADC1_AIN3    |                                                                                                                                                                                                 |
| N25            | MCU_ADC1_AIN4    |                                                                                                                                                                                                 |
| P26            | MCU_ADC1_AIN5    |                                                                                                                                                                                                 |
| N26            | MCU_ADC1_AIN6    |                                                                                                                                                                                                 |
| N27            | MCU_ADC1_AIN7    |                                                                                                                                                                                                 |

**Table 5-115. Connectivity Requirements (continued)**

| BALL NUMBER | BALL NAME     | CONNECTION REQUIREMENT                                                                                                                                                                                                                                                     |
|-------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AC10        | SERDES0_REXT  | Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level, if unused. Refer to <a href="#">Signal Descriptions</a> footnote for appropriate value of pull-resistor for each signal. |
| AC18        | CSI0_RXRCALIB |                                                                                                                                                                                                                                                                            |
| AC21        | CSI1_RXRCALIB |                                                                                                                                                                                                                                                                            |
| R8          | DDR0_CAL0     |                                                                                                                                                                                                                                                                            |
| E8          | DDR1_CAL0     |                                                                                                                                                                                                                                                                            |
| AC13        | DSI0_TXRCALIB |                                                                                                                                                                                                                                                                            |
| AC15        | DSI1_TXRCALIB |                                                                                                                                                                                                                                                                            |
| AA6         | USB0_RCALIB   |                                                                                                                                                                                                                                                                            |
| A26         | MCU_RESETZ    | Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to ensure these balls are held to a valid logic high level, if unused.                                                                                   |
| G23         | MCU_PORZ      |                                                                                                                                                                                                                                                                            |
| K23         | PORZ          |                                                                                                                                                                                                                                                                            |
| A24         | RESET_REQZ    |                                                                                                                                                                                                                                                                            |
| A25         | TCK           |                                                                                                                                                                                                                                                                            |
| AG27        | TMS           |                                                                                                                                                                                                                                                                            |
| G24         | MCU_I2C0_SCL  |                                                                                                                                                                                                                                                                            |
| H24         | WKUP_I2C0_SCL |                                                                                                                                                                                                                                                                            |
| H27         | WKUP_I2C0_SDA |                                                                                                                                                                                                                                                                            |
| J25         | MCU_I2C0_SDA  |                                                                                                                                                                                                                                                                            |
| AE24        | I2C0_SDA      |                                                                                                                                                                                                                                                                            |
| AH25        | I2C0_SCL      |                                                                                                                                                                                                                                                                            |
| AG24        | EXTINTN       |                                                                                                                                                                                                                                                                            |
| AG28        | TDI           |                                                                                                                                                                                                                                                                            |
| AE26        | TDO           |                                                                                                                                                                                                                                                                            |
| A27         | EMU0          |                                                                                                                                                                                                                                                                            |
| C26         | EMU1          |                                                                                                                                                                                                                                                                            |
| H1          | DDR0_DQS0N    |                                                                                                                                                                                                                                                                            |
| M1          | DDR0_DQS1N    |                                                                                                                                                                                                                                                                            |
| U1          | DDR0_DQS2N    |                                                                                                                                                                                                                                                                            |
| AC1         | DDR0_DQS3N    |                                                                                                                                                                                                                                                                            |
| A15         | DDR1_DQS0N    |                                                                                                                                                                                                                                                                            |
| A12         | DDR1_DQS1N    |                                                                                                                                                                                                                                                                            |
| A7          | DDR1_DQS2N    |                                                                                                                                                                                                                                                                            |
| A2          | DDR1_DQS3N    |                                                                                                                                                                                                                                                                            |
| H22         | VPP_MCU       | Each of these balls must be left unconnected, if unused.                                                                                                                                                                                                                   |
| V22         | VPP_CORE      |                                                                                                                                                                                                                                                                            |
| AF1         | MMC0_CALPAD   |                                                                                                                                                                                                                                                                            |
|             | DDR0_*        | DDRSS0 and DDRSS1 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0_* interface. When using two LPDDR components, they must be connected to DDR0_* and DDR1_* interfaces.                      |
|             | DDR1_*        |                                                                                                                                                                                                                                                                            |

Table 5-116 shows the specific connection requirements for the RESERVED ball numbers on the device.

### Note

For additional clarification, "left unconnected" or "no connect" (NC) means **no** signal traces can be connected to these device ball numbers.

**Table 5-116. Reserved Balls Specific Connection Requirements**

| BALL NUMBERS                                                                                                                                      | CONNECTION REQUIREMENTS                            |
|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|
| AB22 / AC12 / AC14 / AC16 / AC17 / AC19 / AC20 / AC23 / AD10 / AD11 / AD12 / AD5 / AE11 / F13 / G11 / G21 / H25 / K28 / L23 / L26 / N28 / N8 / T7 | RESERVED.<br>These balls must be left unconnected. |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

| PARAMETER            |                                                      | MIN  | MAX  | UNIT |
|----------------------|------------------------------------------------------|------|------|------|
| VDD_CORE             | MAIN domain core supply                              | −0.3 | 1.05 | V    |
| VDD_MCU              | MCUSS core supply                                    | −0.3 | 1.05 | V    |
| VDD_CPU              | CPU core supply                                      | −0.3 | 1.05 | V    |
| VDD_MCU_WAKE1        | Core supply for MCU WAKE function                    | −0.3 | 1.05 | V    |
| VDD_WAKE0            | Core supply for MAIN domain WAKE function            | −0.3 | 1.05 | V    |
| VDDA_0P8_DLL_MMC0    | MMC0 DLL analog supply                               | −0.3 | 1.05 | V    |
| VDDAR_CORE           | MAIN domain RAM supply                               | −0.3 | 1.05 | V    |
| VDDAR_MCU            | MCUSS RAM supply                                     | −0.3 | 1.05 | V    |
| VDDAR_CPU            | CPU RAM supply                                       | −0.3 | 1.05 | V    |
| VDDA_0P8_DSITX       | DSITX clock supply                                   | −0.3 | 1.05 | V    |
| VDDA_0P8_DSITX_C     | DSITX clock supply                                   | −0.3 | 1.05 | V    |
| VDDA_0P8_CSIRX0_1    | CSIRX analog supply low                              | −0.3 | 1.05 | V    |
| VDDA_0P8_SERDES0_1   | SERDES0-1 analog supply low                          | −0.3 | 1.05 | V    |
| VDDA_0P8_SERDES_C0_1 | SERDES0-1 clock supply                               | −0.3 | 1.05 | V    |
| VDDA_0P8_USB         | USB0-1 0.8 V analog supply                           | −0.3 | 1.05 | V    |
| VDDA_0P8_PLL_DDR0    | DDR0 PLL analog supply                               | −0.3 | 1.05 | V    |
| VDDA_0P8_PLL_DDR1    | DDR1 PLL analog supply                               | −0.3 | 1.05 | V    |
| VDDA_1P8_USB         | USB0-1 1.8 V analog supply                           | −0.3 | 2.2  | V    |
| VDDA_1P8_DSITX       | DSITX analog supply high                             | −0.3 | 2.2  | V    |
| VDDA_1P8_CSIRX0_1    | CSIRX analog supply high                             | −0.3 | 2.2  | V    |
| VDDA_1P8_SERDES0_1   | SERDES0-1 analog supply high                         | −0.3 | 2.2  | V    |
| VDDA_1P8_SERDES2_4   | SERDES2-4 analog supply high                         | −0.3 | 2.2  | V    |
| VDDA_3P3_USB         | USB0-1 3.3 V analog supply                           | −0.3 | 3.8  | V    |
| VDDA_MCU_PLLGRP0     | Analog supply for MCU PLL Group 0                    | −0.3 | 2.2  | V    |
| VDDA_PLLGRP0         | Analog supply for Main PLL Group 0                   | −0.3 | 2.2  | V    |
| VDDA_PLLGRP1         | Analog supply for Main PLL Group 1                   | −0.3 | 2.2  | V    |
| VDDA_PLLGRP2         | Analog supply for Main PLL Group 2                   | −0.3 | 2.2  | V    |
| VDDA_PLLGRP5         | Analog supply for MAIN PLL Group 5 (DDR)             | −0.3 | 2.2  | V    |
| VDDA_PLLGRP6         | Analog supply for MAIN PLL Group 6                   | −0.3 | 2.2  | V    |
| VDDA_PLLGRP7         | Analog supply for MAIN PLL Group 7                   | −0.3 | 2.2  | V    |
| VDDA_PLLGRP8         | Analog supply for MAIN PLL Group 8                   | −0.3 | 2.2  | V    |
| VDDA_PLLGRP9         | Analog supply for MAIN PLL Group 9                   | −0.3 | 2.2  | V    |
| VDDA_PLLGRP10        | Analog supply for MAIN PLL Group 10                  | −0.3 | 2.2  | V    |
| VDDA_PLLGRP12        | Analog supply for MAIN PLL Group 12                  | −0.3 | 2.2  | V    |
| VDDA_PLLGRP13        | Analog supply for MAIN PLL Group 13                  | −0.3 | 2.2  | V    |
| VDDA_WKUP            | Oscillator supply for WKUP domain                    | −0.3 | 2.2  | V    |
| VDDA_ADC0            | ADC analog supply                                    | −0.3 | 2.2  | V    |
| VDDA_ADC1            | ADC analog supply                                    | −0.3 | 2.2  | V    |
| VDDA_MCU_TEMP        | Analog supply for temperature sensor 0 in MCU domain | −0.3 | 2.2  | V    |
| VDDA_POR_WKUP        | WKUP domain analog supply                            | −0.3 | 2.2  | V    |
| VDDA_TEMP_0          | Analog supply for temperature sensor 0               | −0.3 | 2.2  | V    |
| VDDA_TEMP_1          | Analog supply for temperature sensor 1               | −0.3 | 2.2  | V    |

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

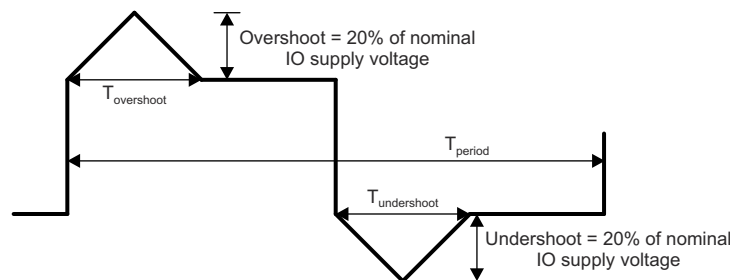
| PARAMETER                                                     |                                                                           |                                                                                                                        | MIN  | MAX                      | UNIT |
|---------------------------------------------------------------|---------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|------|--------------------------|------|
| VDDA_TEMP_2                                                   | Analog supply for temperature sensor 2                                    |                                                                                                                        | -0.3 | 2.2                      | V    |
| VDDA_TEMP_3                                                   | Analog supply for temperature sensor 3                                    |                                                                                                                        | -0.3 | 2.2                      | V    |
| VDDA_TEMP_4                                                   | Analog supply for temperature sensor 4                                    |                                                                                                                        | -0.3 | 2.2                      | V    |
| VDDA_OSC1                                                     | HFOSC1 supply                                                             |                                                                                                                        | -0.3 | 2.2                      | V    |
| VDDS_DDR                                                      | DDR interface power supply                                                |                                                                                                                        | -0.3 | 1.2                      | V    |
| VDDS_DDR_C0                                                   | IO power for DDR0 Memory Clock Bit (MCB) macro                            |                                                                                                                        | -0.3 | 1.2                      | V    |
| VDDS_DDR_C1                                                   | IO power for DDR1 Memory Clock Bit (MCB) macro                            |                                                                                                                        | -0.3 | 1.2                      | V    |
| VDDS_MMC0                                                     | MMC0 IO supply                                                            |                                                                                                                        | -0.3 | 2.2                      | V    |
| VDDSHV0_MCU                                                   | IO supply MCUSS general IO group, and MCU and MAIN domain warm reset pins | 1.8 V                                                                                                                  | -0.3 | 2.2                      | V    |
|                                                               |                                                                           | 3.3 V                                                                                                                  | -0.3 | 3.8                      |      |
| VDDSHV0                                                       | IO supply for MAIN domain general                                         | 1.8 V                                                                                                                  | -0.3 | 2.2                      | V    |
|                                                               |                                                                           | 3.3 V                                                                                                                  | -0.3 | 3.8                      |      |
| VDDSHV1_MCU                                                   | IO supply for MCUSS IO group 1                                            | 1.8 V                                                                                                                  | -0.3 | 2.2                      | V    |
|                                                               |                                                                           | 3.3 V                                                                                                                  | -0.3 | 3.8                      |      |
| VDDSHV2_MCU                                                   | IO supply for MCUSS IO group 2                                            | 1.8 V                                                                                                                  | -0.3 | 2.2                      | V    |
|                                                               |                                                                           | 3.3 V                                                                                                                  | -0.3 | 3.8                      |      |
| VDDSHV2                                                       | IO supply for MAIN domain IO group 2                                      | 1.8 V                                                                                                                  | -0.3 | 2.2                      | V    |
|                                                               |                                                                           | 3.3 V                                                                                                                  | -0.3 | 3.8                      |      |
| VDDSHV5                                                       | IO supply for MAIN domain IO group 5                                      | 1.8 V                                                                                                                  | -0.3 | 2.2                      | V    |
|                                                               |                                                                           | 3.3 V                                                                                                                  | -0.3 | 3.8                      |      |
| VPP_CORE                                                      | Supply voltage range for CORE EFUSE domain                                |                                                                                                                        | -0.3 | 1.89                     | V    |
| VPP_MCU                                                       | Supply voltage range for MCU EFUSE domain                                 |                                                                                                                        | -0.3 | 1.89                     | V    |
| USB0_VBUS <sup>(8)</sup>                                      | Voltage range for USB VBUS comparator input                               |                                                                                                                        | -0.3 | 3.6                      | V    |
| Steady State Max. Voltage at all fail-safe IO pins            |                                                                           | I2C0_SCL, I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, MCU_I2C0_SCL, MCU_I2C0_SDA, EXTINTn                                  | -0.3 | 3.8                      | V    |
|                                                               |                                                                           | MCU_PORz, PORz                                                                                                         | -0.3 | 3.8                      | V    |
| Steady State Max. Voltage at all other IO pins <sup>(3)</sup> |                                                                           | VMON1_ER_VSYS, VMON3_IR_VEXT1P8, VMON4_IR_VEXT1P8,                                                                     | -0.3 | 2.2                      | V    |
|                                                               |                                                                           | VMON2_IR_VCPU, VMON6_IR_VEXT0P8 <sup>(7)</sup>                                                                         | -0.3 | 1.05                     |      |
|                                                               |                                                                           | VMON5_IR_VEXT3P3 <sup>(7)</sup>                                                                                        | -0.3 | 3.8                      |      |
|                                                               |                                                                           | All other IO pins                                                                                                      | -0.3 | IO supply voltage + 0.3  | V    |
|                                                               |                                                                           |                                                                                                                        |      |                          |      |
| Transient Overshoot and Undershoot specification at IO pin    |                                                                           | 20% of IO supply voltage for up to 20% of signal period (see <a href="#">Figure 6-1, IO Transient Voltage Ranges</a> ) |      | 0.2 × VDD <sup>(6)</sup> | V    |
| Latch-up Performance, Class II (125°C) <sup>(4)</sup>         |                                                                           | I-Test                                                                                                                 | -100 | 100                      | mA   |
|                                                               |                                                                           | Over-Voltage (OV) Test                                                                                                 | NA   | 1.5 × VDD <sup>(6)</sup> | V    |

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

| PARAMETER                       |                     | MIN | MAX  | UNIT |
|---------------------------------|---------------------|-----|------|------|
| T <sub>STG</sub> <sup>(5)</sup> | Storage temperature | –55 | +150 | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the [Recommended Operating Conditions](#) but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to their associated VSS or VSSA\_x, unless otherwise noted.
- (3) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
- (4) For current pulse injection:  
Pins stressed per JEDEC JESD78E (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.  
For overvoltage performance:  
Supplies stressed per JEDEC JESD78E (Class II) and passed specified voltage injection.
- (5) For tape and reel the storage temperature range is [–10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.
- (6) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
- (7) The VMON pins provides a way to monitor the system power supply. For more information, see [System Power Supply Monitor Design Guidelines using VMON/POK](#).
- (8) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [USB VBUS Design Guidelines](#).

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The specific signals that are fail safe are highlighted in the parameter "Steady State Max. Voltage at all fail-safe IO pins". All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the "Steady State Max. Voltage at all other IO pins" parameter in [Absolute Maximum Ratings](#).



A.  $T_{\text{overshoot}} + T_{\text{undershoot}} < 20\% \text{ of } T_{\text{period}}$

**Figure 6-1. IO Transient Voltage Ranges**

## 6.2 ESD Ratings

|                    |                         |                                                         |                        | VALUE | UNIT |
|--------------------|-------------------------|---------------------------------------------------------|------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> |                        | ±1000 | V    |
|                    |                         | Charged-device model (CDM), per AEC Q100-011            | All pins               | ±250  |      |
|                    |                         |                                                         | Corner pins (A1, AJ29) | ±750  |      |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| SUPPLY NAME <sup>(2)</sup> | DESCRIPTION                                     | MIN <sup>(1)</sup>  | NOM | MAX <sup>(1)</sup>  | UNIT |
|----------------------------|-------------------------------------------------|---------------------|-----|---------------------|------|
| VDD_CORE                   | Boot/Active voltage for MAIN domain core supply | 0.76 <sup>(1)</sup> | 0.8 | 0.84 <sup>(1)</sup> | V    |

over operating free-air temperature range (unless otherwise noted)

| SUPPLY NAME <sup>(2)</sup> | DESCRIPTION                                                            | MIN <sup>(1)</sup>            | NOM                | MAX <sup>(1)</sup>            | UNIT |
|----------------------------|------------------------------------------------------------------------|-------------------------------|--------------------|-------------------------------|------|
| VDD_MCU                    | Boot/Active voltage for MCUSS core supply                              | 0.76 <sup>(1)</sup>           | 0.8                | 0.89 <sup>(1)</sup>           | V    |
| VDD_CPU                    | Boot voltage for CPU core supply, applied at cold power up event       | 0.76 <sup>(1)</sup>           | 0.8                | 0.84 <sup>(1)</sup>           | V    |
|                            | Active voltage for CPU core supply, after AVS mode enabled in software | AVS <sup>(5)</sup> -5%<br>(1) | AVS <sup>(5)</sup> | AVS <sup>(5)</sup> +5%<br>(1) | V    |
| VDD_CPU AVS Range          | AVS valid voltage range for VDD_CPU                                    | 0.6                           |                    | 0.9                           | V    |
| VDD_MCU_WAKE1              | Core supply for MCU WAKE function                                      | 0.76                          | 0.8                | 0.89                          | V    |
| VDD_WAKE0                  | Core supply for MAIN domain WAKE function                              | 0.76                          | 0.8                | 0.89                          | V    |
| VDDA_0P8_DLL_MMC0          | MMC PLL analog supply                                                  | 0.76                          | 0.8                | 0.84                          | V    |
| VDDAR_CORE                 | Main domain RAM supply                                                 | 0.81                          | 0.85               | 0.89                          | V    |
| VDDAR_MCU                  | MCUSS RAM supply                                                       | 0.81                          | 0.85               | 0.89                          | V    |
| VDDAR_CPU                  | CPU RAM supply                                                         | 0.81                          | 0.85               | 0.89                          | V    |
| VDDA_0P8_DSITX             | DSITX clock supply                                                     | 0.76                          | 0.8                | 0.84                          | V    |
| VDDA_0P8_DSITX_C           | DSITX clock supply                                                     | 0.76                          | 0.8                | 0.84                          | V    |
| VDDA_0P8_CSIRX0_1          | CSIRX analog supply low                                                | 0.76                          | 0.8                | 0.84                          | V    |
| VDDA_0P8_SERDES0_1         | SERDES0-1 analog supply low                                            | 0.76                          | 0.8                | 0.84                          | V    |
| VDDA_0P8_SERDES_C0_1       | SERDES0-1 clock supply                                                 | 0.76                          | 0.8                | 0.84                          | V    |
| VDDA_0P8_USB               | USB0-1 0.8v analog supply                                              | 0.76                          | 0.8                | 0.84                          | V    |
| VDDA_0P8_PLL_DDR0          | DDR0 PLL analog supply low                                             | 0.76                          | 0.8                | 0.84                          | V    |
| VDDA_0P8_PLL_DDR1          | DDR1 PLL analog supply low                                             | 0.76                          | 0.8                | 0.84                          | V    |
| VDDA_1P8_USB               | USB0-1 1.8v analog supply                                              | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_1P8_DSITX             | DSITX analog supply high                                               | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_1P8_CSIRX0_1          | CSIRX analog supply high                                               | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_1P8_SERDES0_1         | SERDES0-1 analog supply high                                           | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_1P8_SERDES2_4         | SERDES2-4 analog supply high                                           | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_3P3_USB               | USB0-1 3.3v analog supply                                              | 3.14                          | 3.3                | 3.46                          | V    |
| VDDA_MCU_PLLGRP0           | Analog supply for MCU PLL Group 0                                      | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP0               | Analog supply for Main PLL Group 0                                     | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP1               | Analog supply for MAIN PLL Group 1                                     | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP2               | Analog supply for MAIN PLL Group 2                                     | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP5               | Analog supply for MAIN PLL Group 5 (DDR)                               | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP6               | Analog supply for MAIN PLL Group 6                                     | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP7               | Analog supply for MAIN PLL Group 7                                     | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP8               | Analog supply for MAIN PLL Group 8                                     | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP9               | Analog supply for MAIN PLL Group 9                                     | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP10              | Analog supply for MAIN PLL Group 10                                    | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP12              | Analog supply for MAIN PLL Group 12                                    | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_PLLGRP13              | Analog supply for MAIN PLL Group 13                                    | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_WKUP                  | Oscillator supply for wkup domain                                      | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_ADC0                  | ADC analog supply                                                      | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_ADC1                  | ADC analog supply                                                      | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_MCU_TEMP              | Analog supply for temperature sensor 0 in MCU domain                   | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_POR_WKUP              | WKUP domain analog supply                                              | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_1P8_MLB               | MLB IO supply (6-pin interface)                                        | 1.71                          | 1.8                | 1.89                          | V    |
| VDDA_TEMP_0                | Analog supply for temperature sensor 0                                 | 1.71                          | 1.8                | 1.89                          | V    |

over operating free-air temperature range (unless otherwise noted)

| SUPPLY NAME <sup>(2)</sup> | DESCRIPTION                                                               |                 | MIN <sup>(1)</sup> | NOM                | MAX <sup>(1)</sup> | UNIT |
|----------------------------|---------------------------------------------------------------------------|-----------------|--------------------|--------------------|--------------------|------|
| VDDA_TEMP_1                | Analog supply for temperature sensor 1                                    |                 | 1.71               | 1.8                | 1.89               | V    |
| VDDA_TEMP_2                | Analog supply for temperature sensor 2                                    |                 | 1.71               | 1.8                | 1.89               | V    |
| VDDA_TEMP_3                | Analog supply for temperature sensor 3                                    |                 | 1.71               | 1.8                | 1.89               | V    |
| VDDA_TEMP_4                | Analog supply for temperature sensor 4                                    |                 | 1.71               | 1.8                | 1.89               | V    |
| VDDA_OSC1                  | Analog supply for HFOSC1                                                  |                 | 1.71               | 1.8                | 1.89               | V    |
| VDDA_*                     | Peak to Peak Noise for all VDDA inputs                                    |                 |                    |                    | 25                 | mV   |
| VDDS_DDR <sup>(3)</sup>    | DDR interface power supply                                                |                 | 1.06               | 1.1                | 1.15               | V    |
| VDDS_DDR_C0                | IO power for DDR0 Memory Clock Bit (MCB) macro                            |                 | 1.06               | 1.1                | 1.15               | V    |
| VDDS_DDR_C1                | IO power for DDR1 Memory Clock Bit (MCB) macro                            |                 | 1.06               | 1.1                | 1.15               | V    |
| VDDS_MMC0                  | MMC0 IO supply                                                            |                 | 1.71               | 1.8                | 1.89               | V    |
| VDDSHV0                    | IO supply for main domain general                                         | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                            |                                                                           | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV0_MCU                | IO supply MCUSS general IO group, and MCU and Main domain warm reset pins | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                            |                                                                           | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV1_MCU <sup>(6)</sup> | IO supply for MCUSS IO group 1                                            | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                            |                                                                           | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV2                    | IO supply for main domain IO group 2                                      | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                            |                                                                           | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV2_MCU                | IO supply for MCUSS IO group 2                                            | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                            |                                                                           | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV5                    | IO supply for main domain IO group 5                                      | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                            |                                                                           | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| USB0_VBUS                  | Voltage range for USB VBUS comparator input                               |                 | 0                  | See <sup>(7)</sup> | 3.46               | V    |
| USB0_ID                    | Voltage range for the USB ID input                                        |                 |                    | See <sup>(4)</sup> |                    | V    |
| VSS                        | Ground                                                                    |                 |                    | 0                  |                    | V    |
| T <sub>J</sub>             | Operating junction temperature range                                      | Automotive      | -40                |                    | 125                | °C   |
|                            |                                                                           | Extended        | -40                |                    | 105                | °C   |
|                            |                                                                           | Commercial      | 0                  |                    | 90                 | °C   |

- (1) For all VDD\* supply inputs, the voltage at the device ball must never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth. This is required for all supply inputs, but special care should be given to the VDD\_CORE, VDD\_MCU, and VDD\_CPU domains which have higher transient current demand compared to other rails.
- (2) Refer to *Power-On-Hour (POH) Limits* for limitations.
- (3) VDDS\_DDR is required to still be powered with LPDDR4 voltage ranges, even if DDR interface is unused.
- (4) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSS with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.
- (5) The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the VTM\_DEVINFO\_VDn. For information about VTM\_DEVINFO\_VDn Registers address, please refer to Voltage and Thermal Manager section in the device TRM. The power supply should be adjustable over the ranges shown in the VDD\_CPU AVS Range entry.
- (6) When DDR1 is used concurrently with either OSPI0 or Hyperbus, VDDSHV1\_MCU is limited to 1.8V (3.3V mode not supported if DDR1 is used in the system.)
- (7) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [USB VBUS Design Guidelines](#).

## 6.4 Power-On-Hour (POH) Limits

| IP <sup>(1)</sup> (2) (3) | VOLTAGE DOMAIN | VOLTAGE (V) (MAX) | FREQUENCY (MHz) (MAX) | T <sub>J</sub> (°C)                      | POH   |
|---------------------------|----------------|-------------------|-----------------------|------------------------------------------|-------|
| All                       | 100%           | All               | All Supported OPPs    | Automotive -40°C to 125°C <sup>(4)</sup> | 20000 |

| IP <sup>(1)</sup> (2) (3) | VOLTAGE DOMAIN | VOLTAGE (V)<br>(MAX) | FREQUENCY<br>(MHz) (MAX) | T <sub>j</sub> (°C)     | POH    |
|---------------------------|----------------|----------------------|--------------------------|-------------------------|--------|
| All                       | 100%           | All                  | All Supported OPPs       | Extended -40°C to 105°C | 100000 |
| All                       | 100%           | All                  | All Supported OPPs       | Commercial 0°C to 90°C  | 100000 |

- (1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
- (2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
- (3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.
- (4) Automotive profile is defined as 20000 power on hours with a junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, and 10%@125°C.

## 6.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks.

[Table 6-1](#) describes the maximum supported frequency per speed grade for the device.

**Table 6-1. Speed Grade Maximum Frequency**

| DEVICE | MAXIMUM FREQUENCY (MHz) |          |          |               |     |        |                    |                   |      |                          |
|--------|-------------------------|----------|----------|---------------|-----|--------|--------------------|-------------------|------|--------------------------|
|        | A72SS0                  | C71SS0/1 | R5FSS0/1 | MCU_<br>R5SS0 | GPU | CBASS0 | VPAC               | VENCDEC           | DMSC | LPDDR4                   |
| T      | 2000                    | 1000     | 1000     | 1000          | 800 | 500    | 720 <sup>(1)</sup> | 550<br>(480MP/s)  | 333  | 4266 MT/s <sup>(2)</sup> |
| H      | 1200                    | 500      | 1000     | 1000          | 800 | 500    | 600 <sup>(1)</sup> | 150 (120<br>MP/s) | 333  | 3200 MT/s <sup>(2)</sup> |

- (1) Max VPAC and DMPAC speeds not available concurrently due to PLL sharing (max combinations are 720/480 and 650/520 for VPAC/DMPAC, respectively).
- (2) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. TI strongly recommends all designs to follow the TI LPDDR4 EVM PCB layout exactly in every detail (routing, spacing, vias/backdrill, PCB material, etc.) in order to achieve the full specified clock frequency. Refer to the Jacinto 7 [LPDDR Board Design and Layout Guidelines](#) for details.

## 6.6 Electrical Characteristics

### Note

The interfaces or signals described in [Section 6.6.1](#) through [Section 6.6.8](#) correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

### 6.6.1 I2C, Open-Drain, Fail-Safe (I2C OD FS) Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                                         | TEST CONDITIONS               | MIN                          | TYP | MAX                          | UNIT |
|-------------------|-----------------------------------------|-------------------------------|------------------------------|-----|------------------------------|------|
| 1.8-V MODE        |                                         |                               |                              |     |                              |      |
| V <sub>IL</sub>   | Input low-level threshold               |                               |                              |     | 0.3 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state  |                               |                              |     | 0.3 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>IH</sub>   | Input high-level threshold              |                               | 0.7 × VDDSHV <sup>(1)</sup>  |     |                              | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state |                               | 0.7 × VDDSHV <sup>(1)</sup>  |     |                              | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                |                               | 0.1 × VDDSHV <sup>(1)</sup>  |     |                              | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V |                              |     | ±10                          | μA   |
| V <sub>OL</sub>   | Output low-level voltage                |                               |                              |     | 0.2 × VDDSHV <sup>(1)</sup>  | V    |
| I <sub>OL</sub>   | Low Level Output Current                | V <sub>OL(MAX)</sub>          | 6                            |     |                              | mA   |
| 3.3-V MODE        |                                         |                               |                              |     |                              |      |
| V <sub>IL</sub>   | Input low-level threshold               |                               |                              |     | 0.3 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state  |                               |                              |     | 0.25 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>IH</sub>   | Input high-level threshold              |                               | 0.7 × VDDSHV <sup>(1)</sup>  |     |                              | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state |                               | 0.7 × VDDSHV <sup>(1)</sup>  |     |                              | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                |                               | 0.05 × VDDSHV <sup>(1)</sup> |     |                              | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 3.3 V or 0 V |                              |     | ±10                          | μA   |
| V <sub>OL</sub>   | Output low-level voltage                |                               |                              |     | 0.4                          | V    |
| I <sub>OL</sub>   | Low Level Output Current                | V <sub>OL(MAX)</sub>          | 6                            |     |                              | mA   |

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the [Pin Attributes](#), POWER column.

### 6.6.2 Fail-Safe Reset (FS Reset) Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS                        | MIN | TYP | MAX                         | UNIT |
|-------------------|----------------------------------------|-----|-----|-----------------------------|------|
| V <sub>IL</sub>   | Input low-level threshold              |     |     | 0.3 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state |     |     | 0.3 × VDDSHV <sup>(1)</sup> | V    |

Over recommended operating conditions (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                         | MIN                                   | TYP | MAX      | UNIT          |
|------------|-----------------------------------------|---------------------------------------|-----|----------|---------------|
| $V_{IH}$   | Input high-level threshold              | $0.7 \times V_{DDSHV}^{(1)}$          |     |          | V             |
| $V_{IHSS}$ | Input high-level threshold steady state | $0.7 \times V_{DDSHV}^{(1)}$          |     |          | V             |
| $V_{HYS}$  | Input Hysteresis Voltage                | 200                                   |     |          | mV            |
| $I_{IN}$   | Input Leakage Current                   | $V_I = 1.8 \text{ V or } 0 \text{ V}$ |     | $\pm 10$ | $\mu\text{A}$ |

(1)  $V_{DDSHV}$  stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column.

### 6.6.3 HFOSC/LFOSC Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER                        | TEST CONDITIONS            | MIN                               | TYP | MAX                               | UNIT |
|----------------------------------|----------------------------|-----------------------------------|-----|-----------------------------------|------|
| <b>HIGH FREQUENCY OSCILLATOR</b> |                            |                                   |     |                                   |      |
| $V_{IH}$                         | Input high-level threshold | $0.65 \times V_{DDSHV}^{(1)}$     |     |                                   | V    |
| $V_{IL}$                         | Input low-level threshold  |                                   |     | $0.35 \times V_{DDSHV}^{(1)}$     | V    |
| $V_{HYS}$                        | Input Hysteresis Voltage   |                                   | 49  |                                   | mV   |
| <b>LOW FREQUENCY OSCILLATOR</b>  |                            |                                   |     |                                   |      |
| $V_{IH}$                         | Input high-level threshold | $0.65 \times V_{DDA\_WKUP}^{(1)}$ |     |                                   | V    |
| $V_{IL}$                         | Input low-level threshold  |                                   |     | $0.35 \times V_{DDA\_WKUP}^{(1)}$ | V    |
| $V_{HYS}$                        | Input Hysteresis Voltage   | Active Mode                       | 85  |                                   | mV   |
|                                  |                            | Bypass Mode                       | 324 |                                   | mV   |

(1)  $V_{DDSHV}$  stands for corresponding power supply. For WKUP\_OSC0, the corresponding power supply is  $V_{DDA\_WKUP}$ . For OSC1\_XI, the corresponding power supply is  $V_{DDS\_OSC1}$ .

### 6.6.4 eMMCPHY Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                         | MIN                                   | NOM | MAX                           | UNIT          |
|------------|-----------------------------------------|---------------------------------------|-----|-------------------------------|---------------|
| $V_{IL}$   | Input low-level threshold               |                                       |     | $0.35 \times V_{DDSHV}^{(1)}$ | V             |
| $V_{ILSS}$ | Input low-level threshold steady state  |                                       |     | 0.20                          | V             |
| $V_{IH}$   | Input high-level threshold              | $0.65 \times V_{DDSHV}^{(1)}$         |     |                               | V             |
| $V_{IHSS}$ | Input high-level threshold steady state | 1.4                                   |     |                               | V             |
| $I_{IN}$   | Input Leakage Current                   | $V_I = 1.8 \text{ V or } 0 \text{ V}$ |     | $\pm 10$                      | $\mu\text{A}$ |
| $I_{OZ}$   | Tri-state Output Leakage Current        | $V_O = 1.8 \text{ V or } 0 \text{ V}$ |     | $\pm 10$                      | $\mu\text{A}$ |
| $R_{PU}$   | Pull-up Resistor                        | 15                                    | 20  | 25                            | k $\Omega$    |
| $R_{PD}$   | Pull-down Resistor                      | 15                                    | 20  | 25                            | k $\Omega$    |
| $V_{OL}$   | Output low-level voltage                |                                       |     | 0.30                          | V             |
| $V_{OH}$   | Output high-level voltage               | $V_{DDSHV} - 0.30^{(1)}$              |     |                               | V             |
| $I_{OL}$   | Low Level Output Current                | $V_{OL(MAX)}$                         | 2   |                               | mA            |
| $I_{OH}$   | High Level Output Current               | $V_{OH(MAX)}$                         | 2   |                               | mA            |

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS | MIN   | NOM | MAX | UNIT |
|-----------------|-----------------|-------|-----|-----|------|
| SR <sub>I</sub> | Input Slew Rate | 5E +8 |     |     | V/s  |

(1) VDDSHV stands for corresponding power supply (vddshv8). For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column..

### 6.6.5 SDIO Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS                         | MIN                           | NOM | MAX                           | UNIT |
|-------------------|-----------------------------------------|-------------------------------|-----|-------------------------------|------|
| <b>1.8-V MODE</b> |                                         |                               |     |                               |      |
| V <sub>IL</sub>   | Input low-level threshold               |                               |     | 0.58                          | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state  |                               |     | 0.58                          | V    |
| V <sub>IH</sub>   | Input high-level threshold              | 1.27                          |     |                               | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state | 1.7                           |     |                               | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                | 150                           |     |                               | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V |     | ±10                           | μA   |
| R <sub>PU</sub>   | Pull-up Resistor                        | 40                            | 50  | 60                            | kΩ   |
| R <sub>PD</sub>   | Pull-down Resistor                      | 40                            | 50  | 60                            | kΩ   |
| V <sub>OL</sub>   | Output low-level voltage                |                               |     | 0.45                          | V    |
| V <sub>OH</sub>   | Output high-level voltage               | VDDSHV-0.45 <sup>(1)</sup>    |     |                               | V    |
| I <sub>OL</sub>   | Low Level Output Current                | V <sub>OL(MAX)</sub>          |     |                               | mA   |
| I <sub>OH</sub>   | High Level Output Current               | V <sub>OH(MAX)</sub>          |     |                               | mA   |
| <b>3.3-V Mode</b> |                                         |                               |     |                               |      |
| V <sub>IL</sub>   | Input low-level threshold               |                               |     | 0.25 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state  |                               |     | 0.15 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>IH</sub>   | Input high-level threshold              | 0.625 × VDDSHV <sup>(1)</sup> |     |                               | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state | 0.625 × VDDSHV <sup>(1)</sup> |     |                               | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                | 150                           |     |                               | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V |     | ±10                           | μA   |
| R <sub>PU</sub>   | Pull-up Resistor                        | 40                            | 50  | 60                            | kΩ   |
| R <sub>PD</sub>   | Pull-down Resistor                      | 40                            | 50  | 60                            | kΩ   |
| V <sub>OL</sub>   | Output low-level voltage                |                               |     | 0.125 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>OH</sub>   | Output high-level voltage               | 0.75 × VDDSHV <sup>(1)</sup>  |     |                               | V    |
| I <sub>OL</sub>   | Low Level Output Current                | V <sub>OL(MAX)</sub>          |     |                               | mA   |
| I <sub>OH</sub>   | High Level Output Current               | V <sub>OH(MAX)</sub>          |     |                               | mA   |

(1) VDDSHV stands for corresponding power supply (vddshv8). For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column.

### 6.6.6 CSI2/DSI D-PHY Electrical Characteristics

#### Note

The CSI2/DSI DPHY interfaces electrical characteristics are compliant with the MIPI D-PHY Specifications v1.2 (August 1, 2014) including ECNs and Errata, as applicable.

### 6.6.7 ADC12B Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER                                 |                                         | TEST CONDITIONS                                       | MIN                                                         | TYP                | MAX | UNIT                   |
|-------------------------------------------|-----------------------------------------|-------------------------------------------------------|-------------------------------------------------------------|--------------------|-----|------------------------|
| Analog Input                              |                                         |                                                       |                                                             |                    |     |                        |
| V <sub>MCU_ADC0/1_AIN[7:0]</sub>          | Full-scale Input Range                  |                                                       | VSS                                                         | VDDA_ADC0/1        |     | V                      |
| DNL                                       | Differential Non-Linearity              |                                                       | -1                                                          | 0.5                | 4   | LSB                    |
| INL                                       | Integral Non-Linearity                  |                                                       |                                                             | ±1                 | ±4  | LSB                    |
| LSB <sub>GAIN-ERROR</sub>                 | Gain Error                              |                                                       |                                                             | ±2                 |     | LSB                    |
| LSB <sub>OFFSE<br/>T-ERROR</sub>          | Offset Error                            |                                                       |                                                             | ±2                 |     | LSB                    |
| C <sub>IN</sub>                           | Input Sampling Capacitance              |                                                       |                                                             | 5.5                |     | pF                     |
| SNR                                       | Signal-to-Noise Ratio                   | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale |                                                             | 70                 |     | dB                     |
| THD                                       | Total Harmonic Distortion               | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale |                                                             | 73                 |     | dB                     |
| SFDR                                      | Spurious Free Dynamic Range             | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale |                                                             | 76                 |     | dB                     |
| SNR <sub>(PLUS)</sub>                     | Signal-to-Noise Plus Distortion         | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale |                                                             | 69                 |     | dB                     |
| R <sub>MCU_ADC0/1_AIN[0:7]</sub>          | Input Impedance of MCU_ADC0/1_AIN[7:0]  | f = input frequency                                   | [1/((65.97 × 10 <sup>-12</sup> ) × f <sub>SMPL_CLK</sub> )] |                    |     | Ω                      |
| I <sub>IN</sub>                           | Input Leakage                           | MCU_ADC0/1_AIN[7:0] = VSS                             |                                                             |                    | -10 | μA                     |
|                                           |                                         | MCU_ADC0/1_AIN[7:0] = VDDA_ADC0/1                     |                                                             |                    | 24  | μA                     |
| Sampling Dynamics                         |                                         |                                                       |                                                             |                    |     |                        |
| F <sub>SMPL_CLK</sub>                     | SMPL_CLK Frequency                      |                                                       |                                                             | 60                 |     | MHz                    |
| t <sub>C</sub>                            | Conversion Time                         |                                                       |                                                             | 13                 |     | ADC0/1 SMPL_CLK Cycles |
| t <sub>ACQ</sub>                          | Acquisition time                        |                                                       | 2                                                           |                    | 257 | ADC0/1 SMPL_CLK Cycles |
| T <sub>R</sub>                            | Sampling Rate                           | ADC0/1 SMPL_CLK = 60 MHz                              |                                                             | 4                  |     | MSPS                   |
| CCISO                                     | Channel to Channel Isolation            |                                                       |                                                             | 100                |     | dB                     |
| General Purpose Input Mode <sup>(1)</sup> |                                         |                                                       |                                                             |                    |     |                        |
| V <sub>IL</sub>                           | Input low-level threshold               |                                                       |                                                             | 0.35 × VDDA_ADC0/1 |     | V                      |
| V <sub>ILSS</sub>                         | Input high-level threshold steady state |                                                       |                                                             | 0.35 × VDDA_ADC0/1 |     | V                      |
| V <sub>IH</sub>                           | Input high-level threshold              |                                                       | 0.65 × VDDA_ADC0/1                                          |                    |     | V                      |

Over recommended operating conditions (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS                         | MIN                           | TYP | MAX | UNIT |
|-------------------|-----------------------------------------|-------------------------------|-----|-----|------|
| V <sub>IHSS</sub> | Input high-level threshold steady state | 0.65 × VDDA_ADC0/1            |     |     | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                | 200                           |     |     | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V |     | 6   | μA   |

- (1) MCU\_ADC0/1 can be configured to operate in General Purpose Input mode, where all MCU\_ADC0/1\_AIN[7:0] inputs are globally enabled to operate as digital inputs via the ADC0/1\_CTRL register (gpi\_mode\_en = 1).

### 6.6.8 LVC MOS Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS                 | MIN                           | TYP                       | MAX  | UNIT |
|-------------------|---------------------------------|-------------------------------|---------------------------|------|------|
| <b>1.8-V MODE</b> |                                 |                               |                           |      |      |
| V <sub>IL</sub>   | Input Low Voltage               |                               | 0.35 × VDD <sup>(1)</sup> |      | V    |
| V <sub>ILSS</sub> | Input Low Voltage Steady State  |                               | 0.3 × VDD <sup>(1)</sup>  |      | V    |
| V <sub>IH</sub>   | Input High Voltage              | 0.65 × VDD <sup>(1)</sup>     |                           |      | V    |
| V <sub>IHSS</sub> | Input High Voltage Steady State | 0.85 × VDD <sup>(1)</sup>     |                           |      | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage        | 150                           |                           |      | mV   |
| I <sub>IN</sub>   | Input Leakage Current.          | V <sub>I</sub> = 1.8 V or 0 V |                           | ±10  | μA   |
| R <sub>PU</sub>   | Pull-up Resistor                | 15                            | 22                        | 30   | kΩ   |
| R <sub>PD</sub>   | Pull-down Resistor              | 15                            | 22                        | 30   | kΩ   |
| V <sub>OL</sub>   | Output Low Voltage              |                               |                           | 0.45 | V    |
| V <sub>OH</sub>   | Output High Voltage             | VDD <sup>(1)</sup> - 0.45     |                           |      | V    |
| I <sub>OL</sub>   | Low Level Output Current        | V <sub>OL</sub> (MAX)         | 3                         |      | mA   |
| I <sub>OH</sub>   | High Level Output Current       | V <sub>OH</sub> (MIN)         | 3                         |      | mA   |
| <b>3.3-V MODE</b> |                                 |                               |                           |      |      |
| V <sub>IL</sub>   | Input Low Voltage               |                               |                           | 0.8  | V    |
| V <sub>ILSS</sub> | Input Low Voltage Steady State  |                               |                           | 0.6  | V    |
| V <sub>IH</sub>   | Input High Voltage              | 2.0                           |                           |      | V    |
| V <sub>IHSS</sub> | Input High Voltage Steady State | 2.0                           |                           |      | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage        | 150                           |                           |      | mV   |
| I <sub>IN</sub>   | Input Leakage Current.          | V <sub>I</sub> = 3.3 V or 0 V |                           | ±10  | μA   |
| R <sub>PU</sub>   | Pull-up Resistor                | 15                            | 22                        | 30   | kΩ   |
| R <sub>PD</sub>   | Pull-down Resistor              | 15                            | 22                        | 30   | kΩ   |
| V <sub>OL</sub>   | Output Low Voltage              |                               |                           | 0.4  | V    |
| V <sub>OH</sub>   | Output High Voltage             | 2.4                           |                           |      | V    |
| I <sub>OL</sub>   | Low Level Output Current        | V <sub>OL</sub> (MAX)         | 5                         |      | mA   |
| I <sub>OH</sub>   | High Level Output Current       | V <sub>OH</sub> (MIN)         | 6                         |      | mA   |

- (1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column.

### 6.6.9 USB2PHY Electrical Characteristics

#### Note

USB0 and USB1 Electrical Characteristics are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

### 6.6.10 SerDes 2-L-PHY/4-L-PHY Electrical Characteristics

#### Note

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 4.0, September 27, 2017.

This Device imposes an additional limit on SERDES REFCLK when used in Input mode with internal termination enabled, as described by parameter  $V_{\text{REFCLK\_TERM}}$  in [Table 6-2, 4-L-PHY SERDES REFCLK Electrical Characteristics](#). Internal termination is enabled by default and must be disabled before applying a reference clock signal that exceeds the limits defined by  $V_{\text{REFCLK\_TERM}}$ . External termination should always be enabled on the source side.

**Table 6-2. 4-L-PHY SERDES REFCLK Electrical Characteristics**

Only applies when internal termination is enabled. Over recommended operating conditions (unless otherwise noted)

| PARAMETER                 |                                                                                                | MIN | TYP | MAX  | UNIT     |
|---------------------------|------------------------------------------------------------------------------------------------|-----|-----|------|----------|
| $V_{\text{REFCLK\_TERM}}$ | Single ended voltage threshold at the reference clock pin when internal termination is enabled |     |     | 400  | mV       |
| $R_{\text{TERM}}$         | Internal termination                                                                           | 40  | 50  | 62.5 | $\Omega$ |

#### Note

The SerDes USB interfaces are compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0, July 26, 2013.

#### Note

The SGMII interfaces electrical characteristics are compliant with 1000BASE-KX per IEEE802.3 Clause 70.

#### Note

The SGMII 2.5G / XAUI interfaces electrical characteristics are compliant with IEEE802.3 Clause 47.

#### Note

The QSGMII interface electrical characteristics are compliant with QSGMII Specification revision 1.2.

#### Note

USXGMII supports IEEE 802.3 TX and RX electrical characteristics of Clause 72-7 and Annex 69B.

IEEE 802.3 Tables 72-7 and 72-8 are not required by USXGMII since these tables are associated with training (Clause 72-6), which is not a requirement of USXGMII.

The pre, main, and post cursors should be set by using BER sweeps.

#### Note

The UFS interface electrical characteristics are compliant with MIPI M-PHY Specification v3.1, February 17, 2014.

#### Note

The DP interface electrical characteristics are compliant with the VESA DisplayPort (DP) Standard v 1.4 February 23, 2016.

#### Note

The eDP interface electrical characteristics are compliant with the VESA Embedded DisplayPort (eDP) Standard v1.4b October 23, 2015.

### 6.6.13 DDR0 Electrical Characteristics

#### Note

The DDR interface is compatible with JESD209-4B standard compliant LPDDR4 SDRAM devices.

## 6.7 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for High-Security Devices.

### 6.7.1 Recommended Operating Conditions for OTP eFuse Programming

over operating free-air temperature range (unless otherwise noted)

| PARAMETER           | DESCRIPTION                                                                         | MIN                                                  | NOM | MAX    | UNIT |
|---------------------|-------------------------------------------------------------------------------------|------------------------------------------------------|-----|--------|------|
| VDD_CORE            | Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)       | See <a href="#">Recommended Operating Conditions</a> |     |        | V    |
| VDD_MCU             | Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)       | See <a href="#">Recommended Operating Conditions</a> |     |        | V    |
| VPP_CORE            | Supply voltage range for the eFuse ROM domain during normal operation               | N/A <sup>(2)</sup>                                   |     |        |      |
|                     | Supply voltage range for the eFuse ROM domain during OTP programming <sup>(1)</sup> | 1.71                                                 | 1.8 | 1.89   | V    |
| VPP_MCU             | Supply voltage range for the eFuse ROM domain during normal operation               | N/A <sup>(2)</sup>                                   |     |        |      |
|                     | Supply voltage range for the eFuse ROM domain during OTP programming <sup>(1)</sup> | 1.71                                                 | 1.8 | 1.89   | V    |
| SR <sub>(VPP)</sub> | VPP Power-up Slew Rate                                                              |                                                      |     | 6E + 4 | V/s  |

(1) Supply voltage range includes DC errors and peak-to-peak noise.

(2) N/A stands for Not Applicable.

### 6.7.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP\_CORE and VPP\_MCU power supplies must be disabled when not programming OTP registers.
- The VPP\_CORE and VPP\_MCU power supplies must be ramped up after the proper device power-up sequence (for more details, see [Power Supply Sequencing](#)).

### 6.7.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP\_CORE and VPP\_MCU terminals during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).

- Apply the voltage on the VPP\_CORE and VPP\_MCU terminals according to the specification in [Section 6.7.1](#).
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP\_CORE and VPP\_MCU terminals.

#### **6.7.4 Impact to Your Hardware Warranty**

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY FOR ANY TI DEVICES THAT HAVE BEEN eFUSED.

## 6.8 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the  $T_J$  value identified in [Recommended Operating Conditions](#).

### 6.8.1 Thermal Resistance Characteristics for ALZ Package

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

| NO. | PARAMETER      | DESCRIPTION             | ALZ PACKAGE                             |                                  |
|-----|----------------|-------------------------|-----------------------------------------|----------------------------------|
|     |                |                         | $^{\circ}\text{C/W}$ <sup>(1) (3)</sup> | AIR FLOW <sup>(2)</sup><br>(m/s) |
| T1  | $R\theta_{JC}$ | Junction-to-case        | 0.3                                     | N/A                              |
| T2  | $R\theta_{JB}$ | Junction-to-board       | 2.0                                     | N/A                              |
| T3  | $R\theta_{JA}$ | Junction-to-free air    | 10.4                                    | 0                                |
| T4  |                | Junction-to-moving air  | 6.1                                     | 1                                |
| T5  |                |                         | 5.3                                     | 2                                |
| T6  |                |                         | 4.8                                     | 3                                |
| T7  | $\psi_{JT}$    | Junction-to-package top | 0.16                                    | 0                                |
| T8  |                |                         | 0.17                                    | 1                                |
| T9  |                |                         | 0.17                                    | 2                                |
| T10 |                |                         | 0.17                                    | 3                                |
| T11 | $\psi_{JB}$    | Junction-to-board       | 1.8                                     | 0                                |
| T12 |                |                         | 1.5                                     | 1                                |
| T13 |                |                         | 1.4                                     | 2                                |
| T14 |                |                         | 1.4                                     | 3                                |

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [ $R\theta_{JC}$ ] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.

(3)  $^{\circ}\text{C/W}$  = degrees Celsius per watt.

## 6.9 Temperature Sensor Characteristics

This section summarizes the Voltage and Temperature Module (VTM) on die temperature sensor characteristics.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the  $T_J$  value identified in the [Recommended Operating Conditions](#).

**Table 6-3. VTM Die Temperature sensor Characteristics**

| PARAMETER |                                 | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---------------------------------|-----------------|-----|-----|-----|------|
| $T_{acc}$ | VTM temperature sensor accuracy | –40 to 110 °C   | –5  |     | 5   | °C   |
|           |                                 | 110 to 125 °C   | –2  |     | 2   | °C   |

## 6.10 Timing and Switching Characteristics

### Note

The timings presented in this section are valid when the DRV\_STR (Drive Strength) control in the associated PADCONFIG registers are set to the default “0h – Nominal (recommended)” value.

### 6.10.1 Timing Parameters and Information

The timing parameter symbols used in [Timing and Switching Characteristics](#) are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in [Table 6-4](#):

**Table 6-4. Timing Parameters Subscripts**

| SYMBOL | PARAMETER                              |
|--------|----------------------------------------|
| c      | Cycle time (period)                    |
| d      | Delay time                             |
| dis    | Disable time                           |
| en     | Enable time                            |
| h      | Hold time                              |
| su     | Setup time                             |
| START  | Start bit                              |
| t      | Transition time                        |
| v      | Valid time                             |
| w      | Pulse duration (width)                 |
| X      | Unknown, changing, or don't care level |
| F      | Fall time                              |
| H      | High                                   |
| L      | Low                                    |
| R      | Rise time                              |
| V      | Valid                                  |
| IV     | Invalid                                |
| AE     | Active Edge                            |
| FE     | First Edge                             |
| LE     | Last Edge                              |
| Z      | High impedance                         |

### 6.10.2 Power Supply Sequencing

This section describes power supply sequencing required to ensure proper device operation. The device can be operated using either an isolated or combined MCU & Main power distribution network (PDN). Two different primary power sequences are recommended based upon isolated and combined MCU & Main PDNs. In addition, the device can be operated in either MCU Only or DDR Retention or GPIO Retention low power modes. Two different desired device power supply sequences for entry and exit of low power modes are shown.

The power supply names used in this section are specific to this device and align to names given in the Signal Descriptions section. Common power supply names may be used across different devices within the Jacinto 7™ processor family. These common supply names will have very similar if not identical functions across devices.

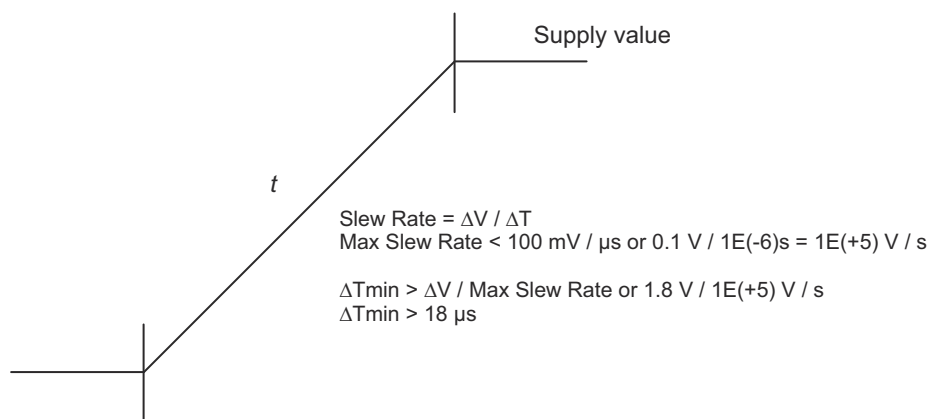
All power sequencing timing diagrams shown will use the following terminology:

- Primary = Essential power sequences of all voltage domains between off and full active states.
- $V_{OPR\ MIN}$  = Minimum operational voltage level that ensures functionality as specified in Recommended Operating Conditions
- Ramp-up = start of a voltage supply transition time from off condition to  $V_{opr\ min}$ .
- Ramp-down = start of a voltage supply transition time from  $V_{opr}$  to off condition
- Supply\_“n” = multiple instances of similar power supplies (i.e.  $VDDSHV_n = VDDSHV_0, VDDSHV_1, VDDSHV_2 \dots VDDSHV_6$ )
- Supply\_“xxx” = multiple instances of similar power supplies used for different signal types (i.e.  $VDDA\_1P8\_xxx = VDDA\_1P8\_DSITX, VDDA\_1P8\_USB, VDDA\_0P8\_DSITX, VDDA\_0P8\_USB, \text{etc.}$ )
- Time stamps = “T#” markers with descriptions and approximate elapsed times for general reference. Specific timing transitions are dependent upon PDN design (see PDN User Guide for details).

#### 6.10.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 100 mV/us, as shown in [Figure 6-2](#). For instance, a 1.8V supply should have a ramp time  $> 18\ \mu s$  to ensure the slew rate  $< 100\text{mV/us}$ .

[Figure 6-2](#) describes the Power Supply Slew Rate Requirement in the device.

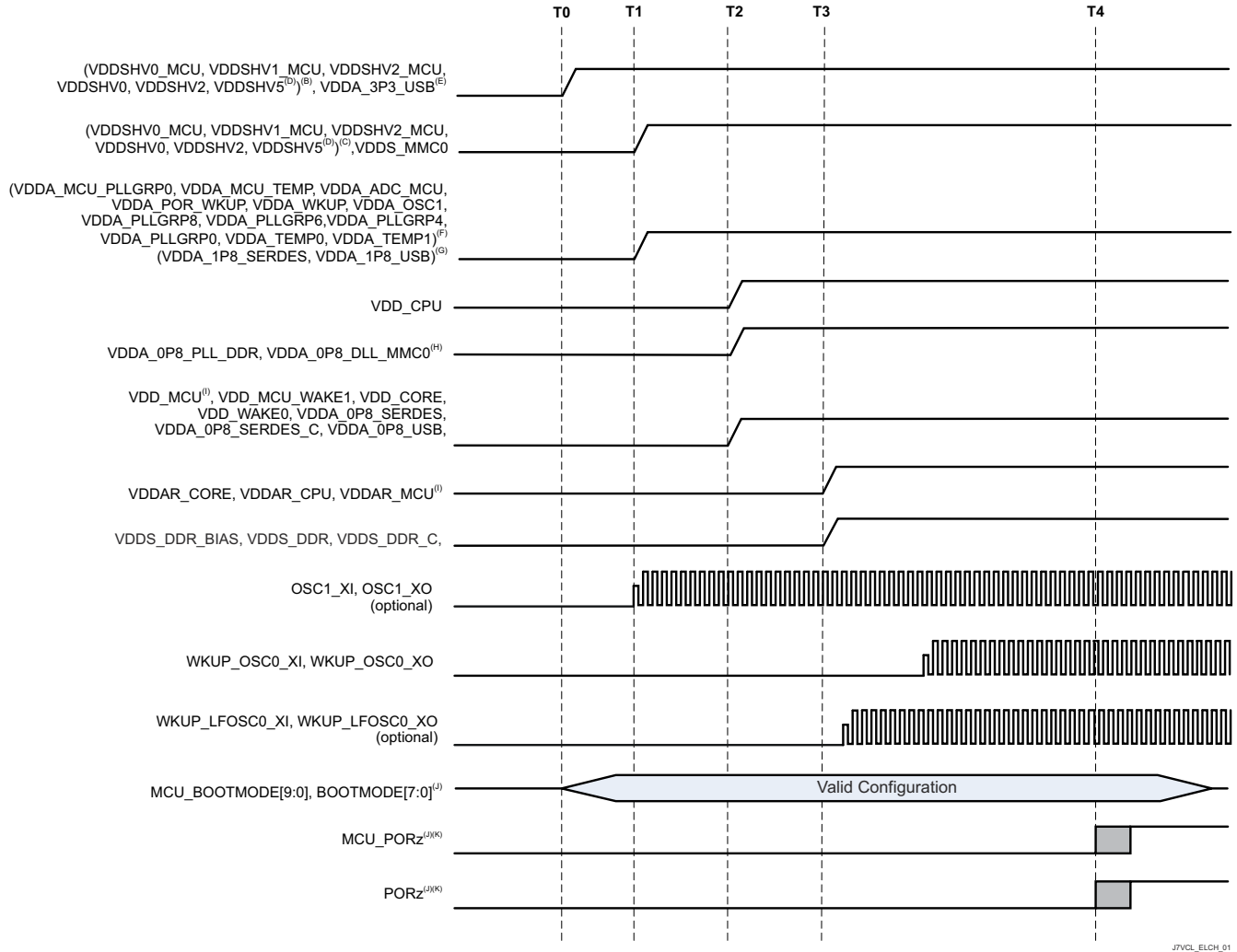


SPRSP08\_ELCH\_06

**Figure 6-2. Power Supply Slew and Slew Rate**

### 6.10.2.2 Combined MCU and Main Domains Power- Up Sequencing

Section 6.10.2.2 describes the primary power-up sequencing when similar MCU and Main voltage domains are combined into common power rails. Combining MCU and Main voltage domains simplifies PDN design by reducing total number of power rails and sources while making MCU and Main processor sub-systems operational dependent on common power rails.



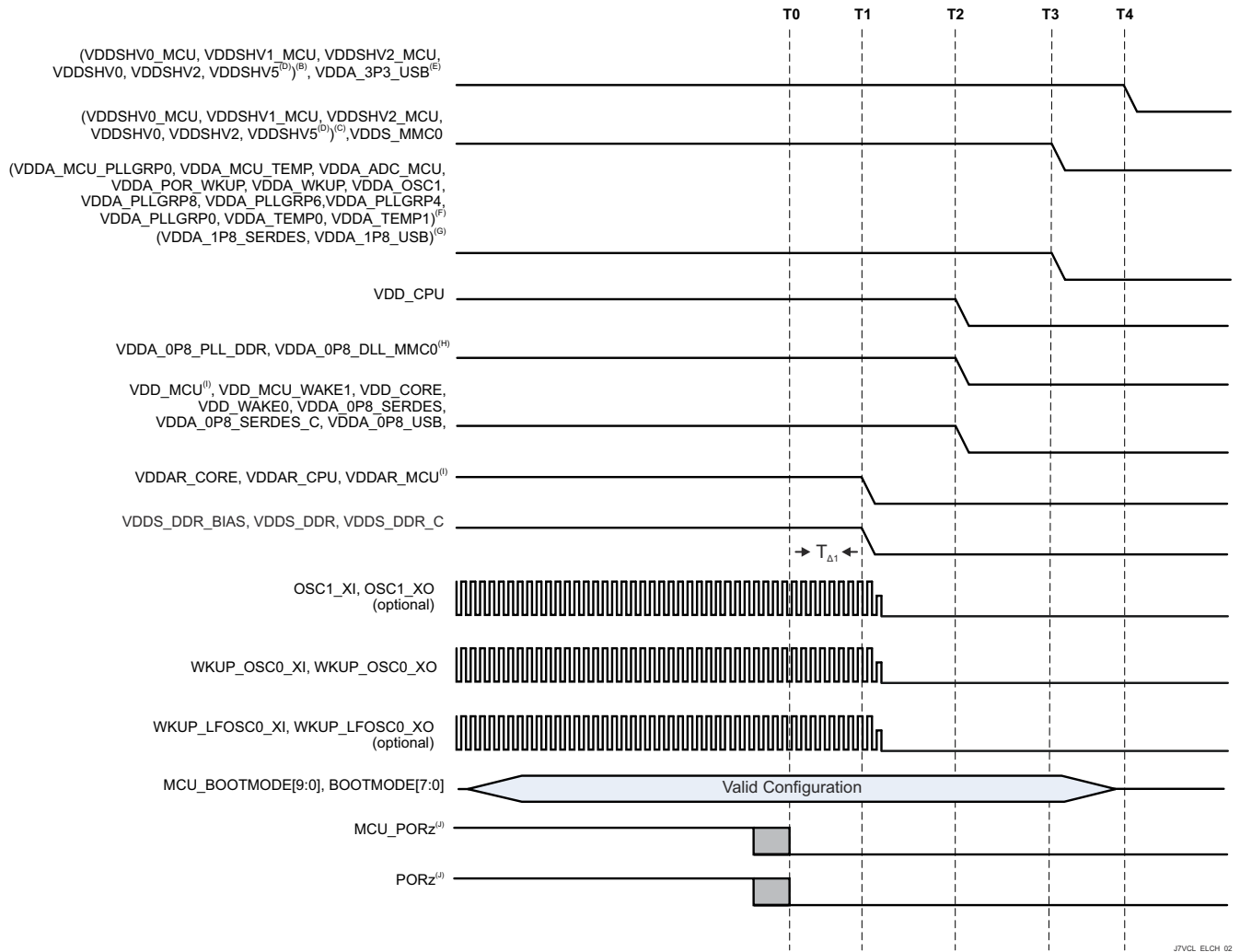
- A. Time stamp markers:
- T0 – 3.3V voltages start ramp-up to  $V_{OPR\ MIN}$ . (0 ms)
  - T1 – 1.8-V voltages start ramp-up to  $V_{OPR\ MIN}$ . (2 ms)
  - T2 – Low voltage core supplies start ramp-up to  $V_{OPR\ MIN}$ . (3 ms)
  - T3 – Low voltage RAM array voltages start ramp-up to  $V_{OPR\ MIN}$ . (4 ms)
  - T4 – OSC1 is stable and PORz/MCU\_PORz are de-asserted to release processor from reset. (13 ms)
- B. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces. A few supplies could have varying start times between T0 to T1 due to PDN designs using different power resources with varying turn-on & ramp-up time delays.
- C. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces. When eMMC memories are used, Main 1.8-V supplies could have a ramp-up aligned to T3 due to PDN designs grouping supplies with VDD\_MMC0.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. If compliant high-speed SD card operation is needed, then an independent, dual voltage (3.3 V/1.8 V) power source and rail are required. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If SD card is not needed or standard data rates with fixed 3.3 V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then domain can be grouped with digital IO 1.8-V power rail.

- E. VDDA\_3P3\_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- G. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. VDD\_MCU is a digital voltage domain with a wide operational voltage range enabling it to be grouped either with VDDAR\_MCU domain or with VDD\_CORE; for the “Combined MCU and Main Domains Power-Up Sequencing,” VDD\_MCU can be grouped with VDD\_CORE, and VDDAR\_MCU can be grouped with VDDAR\_CPU and VDDAR\_CORE. If VDD\_MCU is grouped with VDD\_CORE, VDD\_MCU must be ramped-up from a common voltage resource with 0.8-V VDD\_CORE at T2. If VDD\_MCU is not grouped with VDD\_CORE, VDD\_MCU must be ramped-up before T2. In either case, the VDDAR supplies must be ramped at T3.
- J. Minimum set-up and hold times shown with respect to MCU\_PORz and PORz asserting high to latch MCU\_BOOTMODEn (referenced to MCU\_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power up sequence.
- K. Minimum elapsed time from crystal oscillator circuitry being energized (VDDA\_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10 ms elapsed time defined by (T4 – T1) time stamps is shown. This could be reduced depending upon customer’s clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

**Figure 6-3. Combined MCU and Main Domains, Primary Power-Up Sequence**

### 6.10.2.3 Combined MCU and Main Domains Power- Down Sequencing

Figure 6-4 describes the device power-down sequencing.



#### A. Time stamp markers:

- T0 – MCU\_PORz & PORz assert low to put all processor resources in safe state. (0 ms)
- T1 – Main DDR, SRAM Core, and SRAM CPU power supplies start ramp-down. (0.5 ms)
- T2 – Low voltage core supplies start supply ramp-down. (2.5 ms)
- T3 – 1.8-V voltages start supply ramp-down. (3.0 ms)
- T4 – 3.3V voltages start supply ramp-down. (3.5 ms)

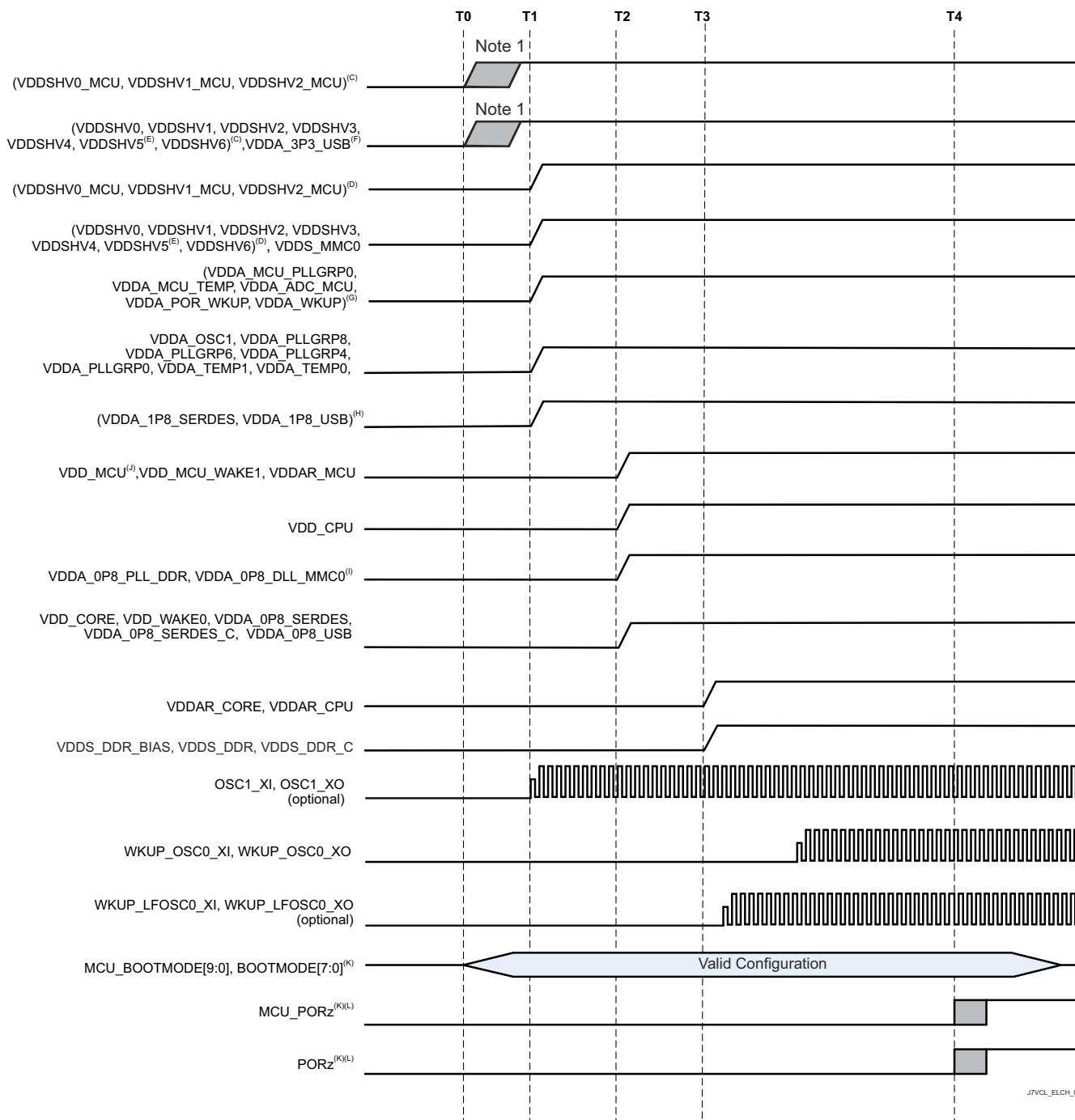
- B. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3 V to support 3.3-V digital interfaces.
- C. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3 V/1.8 V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then domain can be grouped with digital IO 1.8-V power rail.
- E. VDDA\_3P3\_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required .

- G. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. MCU\_PORz and PORz must be asserted low for  $T_{\Delta 1} = 200 \text{ us}$  MIN to ensure SoC resources enter into safe state before any voltage begins to ramp down.

**Figure 6-4. Combined MCU and Main Domains, Primary Power-Down Sequence**

#### 6.10.2.4 Isolated MCU and Main Domains Power- Up Sequencing

Isolated MCU and Main voltage domains enable an SoC's MCU and Main processor sub-systems to operate independently. There are 2 reasons an SoC's PDN design may need to support independent MCU and Main processor functionality. First is to provide flexibility to enable SoC low power modes that can significantly reduce SoC power dissipation when processor operations are not needed. Second is to enable robustness to gain freedom from interference (FFI) of a single fault impacting both MCU and Main processor sub-systems which is especially beneficial if using the SoC's MCU as the system safety monitoring processor. The number of additional PDN power rails needed is dependent upon number of different MCU IO signaling voltage levels. If only 1.8V IO signaling is used, then only 2 additional power rails could be required. If both 1.8 and 3.3V IO signaling is desired, then 4 additional power rails could be needed.



## A. T1 Time stamp markers:

- T0 – All 3.3-V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (0 ms)
- T1 – All 1.8-V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (2 ms)
- T2 – All core voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (3 ms)
- T3 – All RAM array voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (4 ms)
- T4 – OSC1 is stable and PORz/MCU\_PORz are de-asserted to release processor from reset. (13 ms)

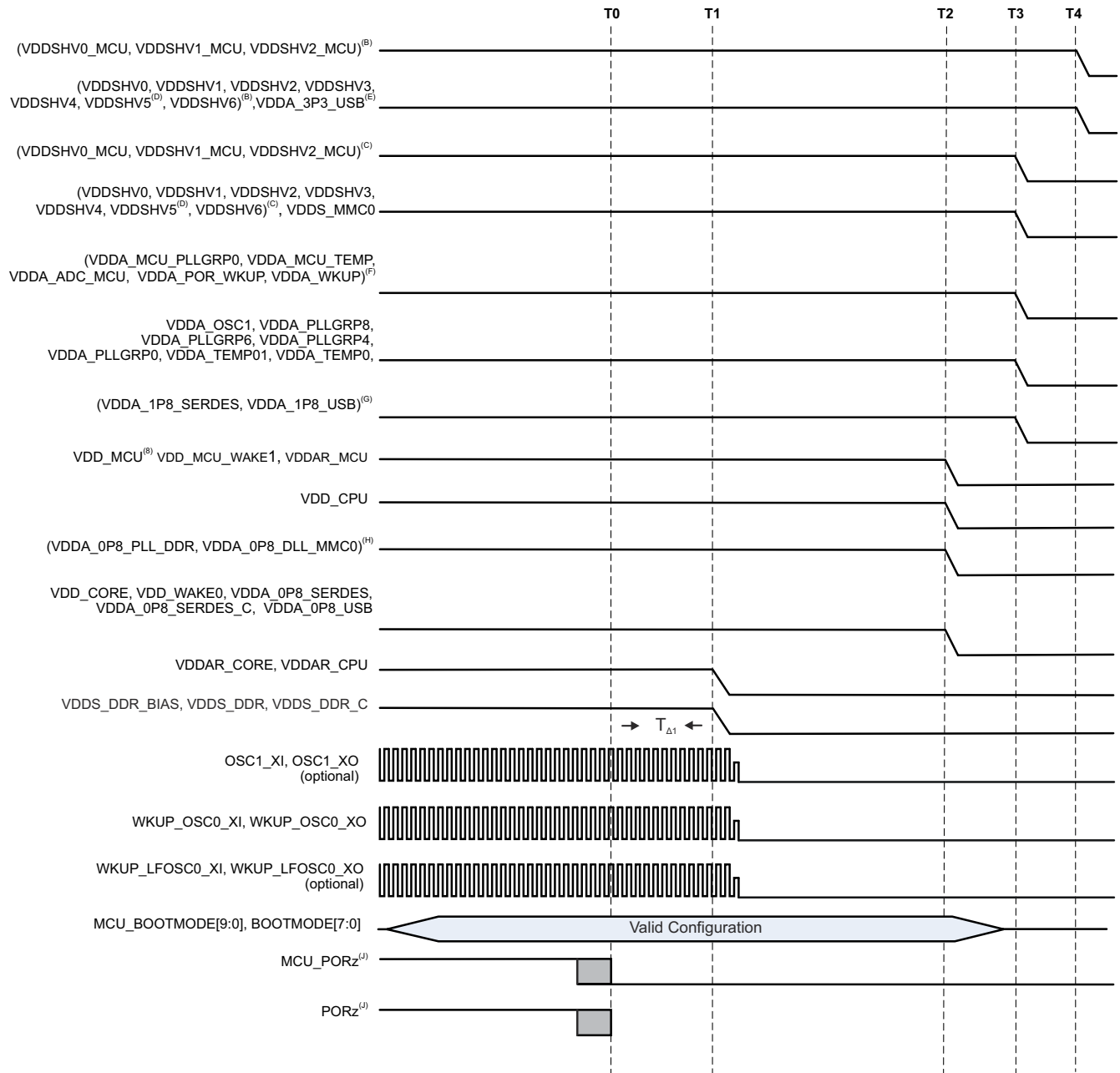
## B. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3 V to support 3.3-V digital interfaces. A few supplies could have varying start times between T0 to T1 due to PDN designs using different power resources with varying turn-on &amp; ramp-up time delays.

- C. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces. When eMMC memories are used, Main 1.8-V supplies could have delayed start times that aligns to T3 due to PDN designs grouping supplies with VDD\_MMC0.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. If compliant UHS-I SD card operation is needed, then an independent, dual voltage (3.3 V/1.8 V) power source and rail are required. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then supply can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then supply can be grouped with digital IO 1.8-V power rail.
- E. VDDA\_3P3\_USB is 3.3-V analog supply used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then supply can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- G. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. VDD\_MCU is a digital voltage domain with a wide operational voltage range enabling it to be grouped either with VDDAR\_MCU domain or with VDD\_CORE; for the "Isolated MCU and Main Domains Power-Up Sequencing," VDD\_MCU can be grouped with VDDAR\_MCU; VDD\_MCU must be ramped-up before T2. If VDDAR\_MCU is not grouped with VDD\_MCU, it must be ramped at T3.
- J. Minimum set-up and hold times shown with respect to MCU\_PORz and PORz asserting high to latch MCU\_BOOTMODEn (referenced to MCU\_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power up sequence.
- K. Minimum elapsed time from crystal oscillator circuitry being energized (VDDA\_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10 ms elapsed time defined by (T4 – T1) time stamps is shown. This could be reduced depending upon customer's clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

**Figure 6-5. Isolated MCU and Main Domains, Primary Power-Up Sequence**

### 6.10.2.5 Isolated MCU and Main Domains Power- Down Sequencing

Figure 6-6 describes the device power-down sequencing.



J7VCL\_ELCH\_04

A. Time stamp markers:

- T0 – MCU\_PORz and PORz assert low to put all processor resources in safe state. (0 ms)
- T1 – Main DDR, SRAM Core, and SRAM CPU power domains start ramp-down. (0.5 ms)
- T2 – All core voltages start supply ramp-down. (2.5 ms)
- T3 – All 1.8V voltages start supply ramp-down. (3.0 ms)
- T4 – All 3.3V voltages start supply ramp-down. (3.5 ms)

B. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3 V to support 3.3-V digital interfaces.

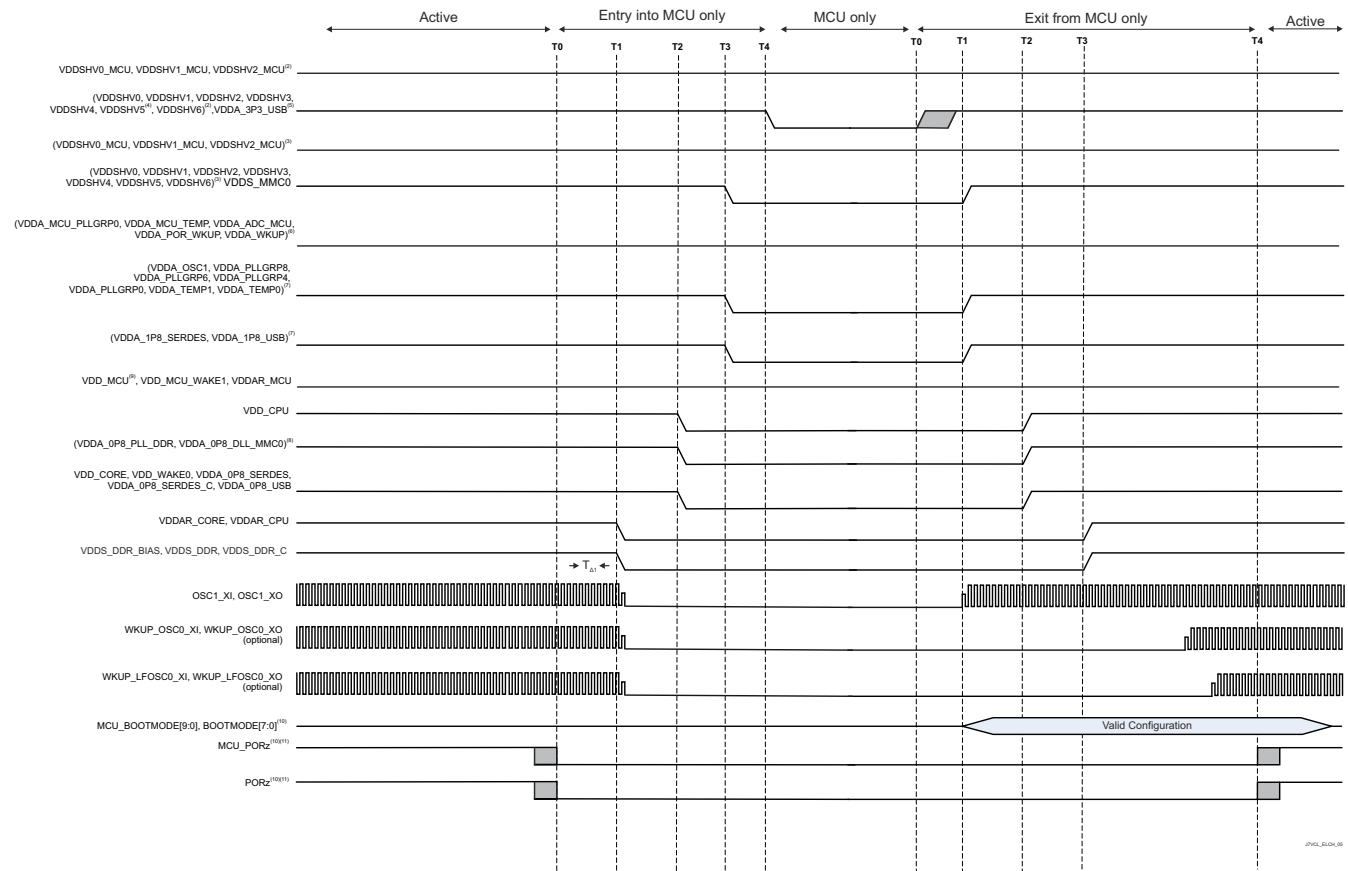
C. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces. When eMMC memories are used, Main 1.8-V supplies could have a ramp-down aligned to T1 due to PDN designs grouping supplies with VDD\_MMC0.

- D. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3 V/1.8 V) power rail is required for compliant, high-speed SD card operations. If compliant high-speed SD card operation is needed, then an independent, dual voltage (3.3 V/1.8 V) power source and rail are required. The start of ramp-down from 3.3 V/1.8 V will be same as other 3.3-V domains as shown. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then domain can be grouped with digital IO 1.8-V power rail.
- E. VDDA\_3P3\_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-down from 3.3 V will be same as other 3.3-V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- G. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. MCU\_PORz and PORz must be asserted low for  $T_{\Delta 1} = 200 \mu s$  MIN to ensure SoC resources enter into safe state before any voltage begins to ramp down.

**Figure 6-6. Isolated MCU and Main Domains, Primary Power- Down Sequencing**

#### 6.10.2.6 Independent MCU and Main Domains, Entry and Exit of MCU Only Sequencing

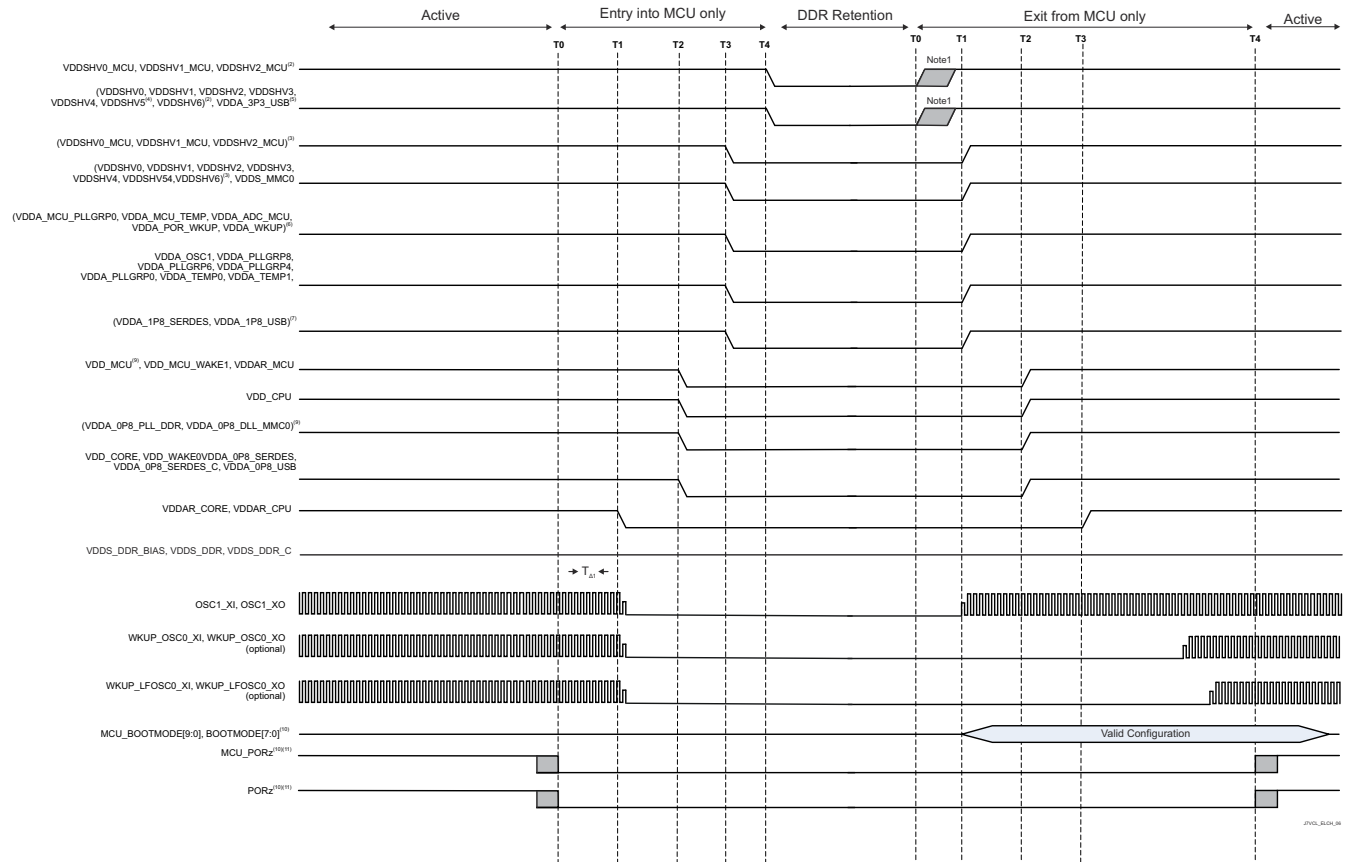
Entry into MCU Only state is accomplished by executing a power down sequence except for the 4 MCU domains that remain energized. Exit from MCU Only state is accomplished by executing a power up sequence with the 4 MCU domains remaining energized throughout the seque.



**Figure 6-7. Independent MCU and Main Domains, Entry and Exit of MCU Only Sequencing**

#### 6.10.2.7 Independent MCU and Main Domains, Entry and Exit of DDR Retention State

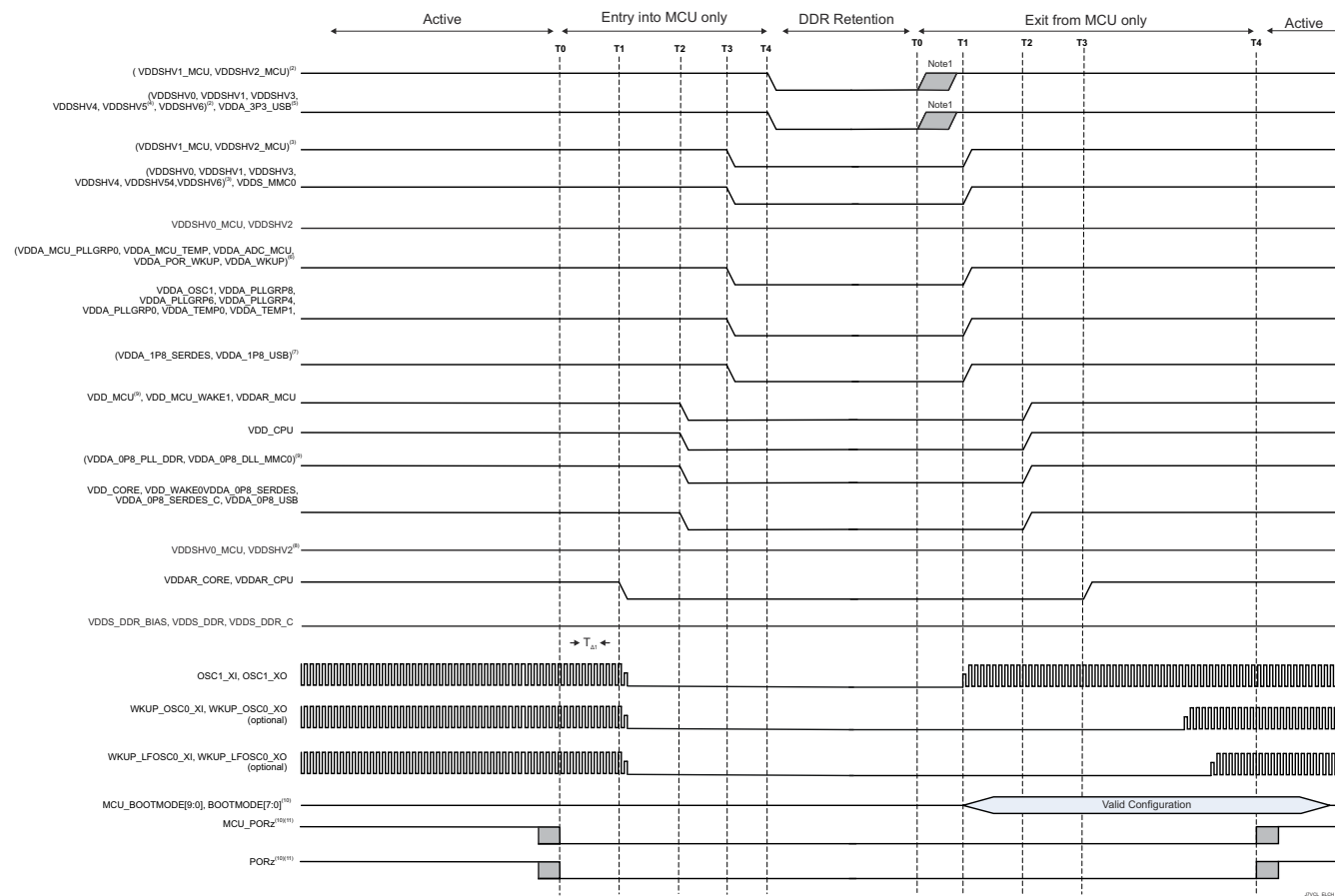
Entry into DDR Retention state is accomplished by executing a power down sequence except for the 4 DDR domains that remain energized. Exit from DDR Retention state is accomplished by executing a power up sequence with the 3 DDR domains remaining energized throughout the sequence.



**Figure 6-8. Independent MCU and Main Domains, Entry and Exit of DDR Retention State**

#### 6.10.2.8 Independent MCU and Main Domains, Entry and Exit of GPIO Retention Sequencing

Entry into GPIO Retention state is accomplished by executing a power down sequence except for the 2 or 4 wake domains that remain energized. Exit from GPIO Retention state is accomplished by executing a power up sequence with the 2 or 4 wake DDR domains remaining energized throughout the sequence.



**Figure 6-9. Independent MCU and Main Domains, Entry and Exit of GPIO Retention Sequencing**

### 6.10.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

**Table 6-5. System Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5 | 2   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 3   | 30  | pF   |

#### 6.10.3.1 Reset Timing

The tables and figures provided in this section define the timing requirements and switching characteristics for reset related signals.

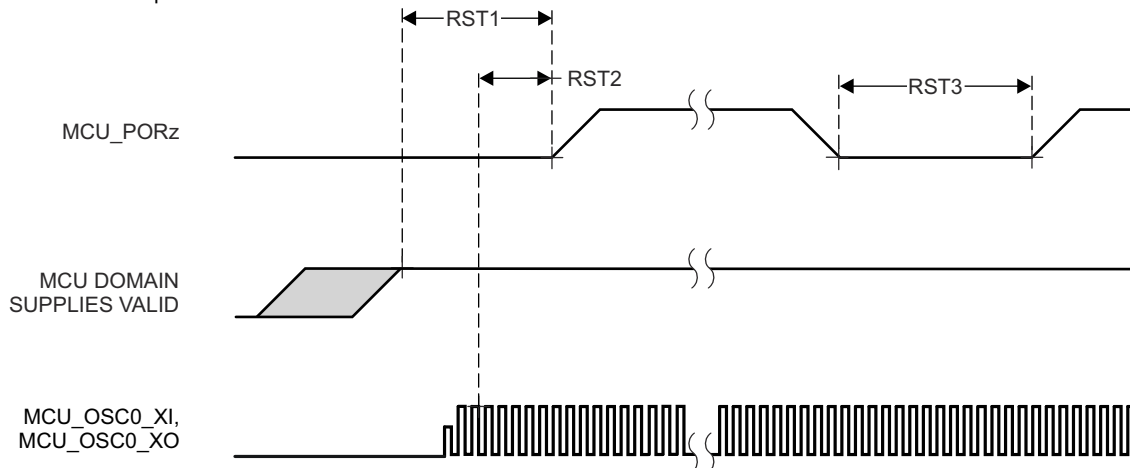
**Table 6-6. MCU\_PORz Timing Requirements**

see [Figure 6-10](#)

| NO.  |                                                 |                                                                                                                                                               | MIN                     | TYP     | MAX | UNIT |
|------|-------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|---------|-----|------|
| RST1 |                                                 | Hold time, MCU_PORz active (low) at Power-up after all MCU DOMAIN supplies valid (using external crystal)                                                     | N + 1200 <sup>(2)</sup> | 9500000 |     | ns   |
| RST2 | t <sub>h</sub> (MCUD_SUPPLIES_VALID - MCU_PORz) | Hold time, MCU_PORz active (low) at Power-up after all MCU DOMAIN supplies <sup>(1)</sup> valid and external clock stable (using external LVC MOS oscillator) | 1200                    |         |     | ns   |
| RST3 | t <sub>w</sub> (MCU_PORzL)                      | Pulse Width minimum, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)                                          | 1200                    |         |     | ns   |

(1) For the definition of the MCU DOMAIN supplies, see the [Section 6.10.2.2, Combined MCU and Main Domains Poewr-Up Sequencing](#).

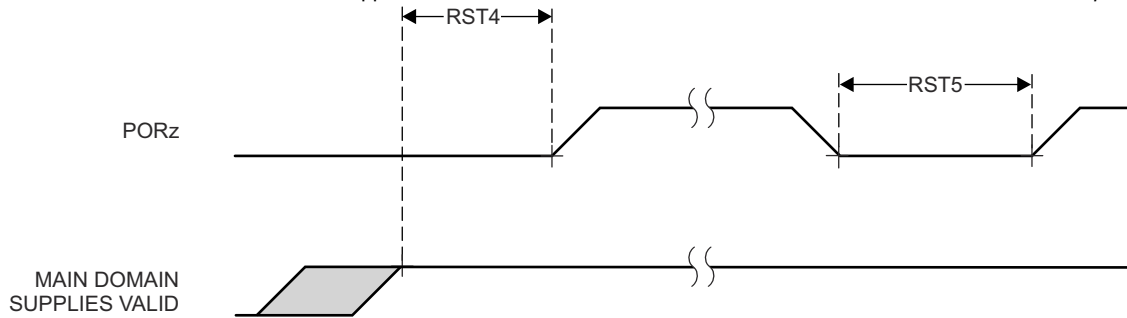
(2) N = oscillator start-up time



**Figure 6-10. MCU\_PORz Timing Requirements**

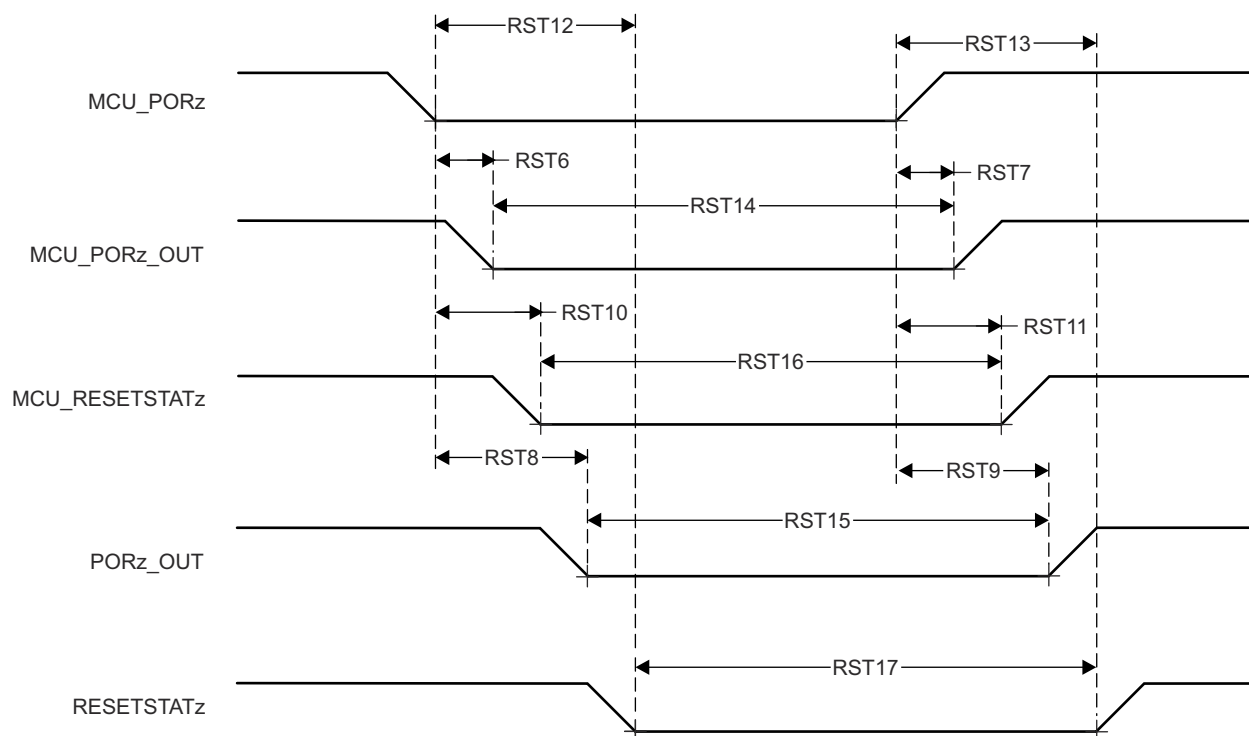
**Table 6-7. PORz Timing Requirements**see [Figure 6-11](#)

| NO.  |                                       |                                                                                              | MIN  | MAX | UNIT |
|------|---------------------------------------|----------------------------------------------------------------------------------------------|------|-----|------|
| RST4 | $t_{h(MAIN\_SUPPLIES\_VALID - PORz)}$ | Hold time, PORz active (low) at Power-up after all MAIN DOMAIN supplies <sup>(1)</sup> valid | 1200 |     | ns   |
| RST5 | $t_{w(PORzL)}$                        | Pulse Width minimum, PORz low after Power-up                                                 | 1200 |     | ns   |

(1) For the definition of the MAIN DOMAIN supplies, see the [Section 6.10.2.2, Combined MCU and Main Domains Power-Up Sequencing](#).**Figure 6-11. PORz Timing Requirements****Table 6-8. MCU\_PORz initiates; MCU\_PORz\_OUT, PORz\_OUT, MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**see [Figure 6-12](#)

| NO.   | PARAMETER                          |                                                                        | MODE        | MIN                   | MAX | UNIT |
|-------|------------------------------------|------------------------------------------------------------------------|-------------|-----------------------|-----|------|
| RST6  | $t_d(MCU\_PORzL-MCU\_PORz\_OUTL)$  | Delay time, MCU_PORz active (low) to MCU_PORz_OUT active (low)         |             | 0                     |     | ns   |
| RST7  | $t_d(MCU\_PORzH-MCU\_PORz\_OUTH)$  | Delay time, MCU_PORz inactive (high) to MCU_PORz_OUT inactive (high)   |             | 0                     |     | ns   |
| RST8  | $t_d(MCU\_PORzL-PORz\_OUTL)$       | Delay time, MCU_PORz active (low) to PORz_OUT active (low)             |             | 0                     |     | ns   |
| RST9  | $t_d(MCU\_PORzH-PORz\_OUTH)$       | Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)       |             | 1500                  |     | ns   |
| RST10 | $t_d(MCU\_PORzL-MCU\_RESETSTATzL)$ | Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)       |             | 0                     |     | ns   |
| RST11 | $t_d(MCU\_PORzH-MCU\_RESETSTATzH)$ | Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high) | POST bypass | $12000 \cdot S^{(1)}$ |     | ns   |
| RST12 | $t_d(MCU\_PORzL-RESETSTATzL)$      | Delay time, MCU_PORz active (low) to RESETSTATz active (low)           |             | 0                     |     | ns   |
| RST13 | $t_d(MCU\_PORzH-RESETSTATzH)$      | Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)     |             | $14500 \cdot S^{(1)}$ |     | ns   |
| RST14 | $t_w(MCU\_PORz\_OUTL)$             | Pulse width minimum, MCU_PORz_OUT active (low)                         |             | 1200                  |     | ns   |
| RST15 | $t_w(PORz\_OUTL)$                  | Pulse Width Minimum PORz_OUT low                                       |             | 2550                  |     | ns   |
| RST16 | $t_w(MCU\_RESETSTATzL)$            | Pulse Width Minimum MCU_RESETSTATz low                                 |             | $3900 \cdot S^{(1)}$  |     | ns   |
| RST17 | $t_w(RESETSTATzL)$                 | Pulse Width Minimum RESETSTATz low                                     |             | $2650 \cdot S^{(1)}$  |     | ns   |

(1)  $S = MCU\_OSC0\_XI/XO$  clock period.



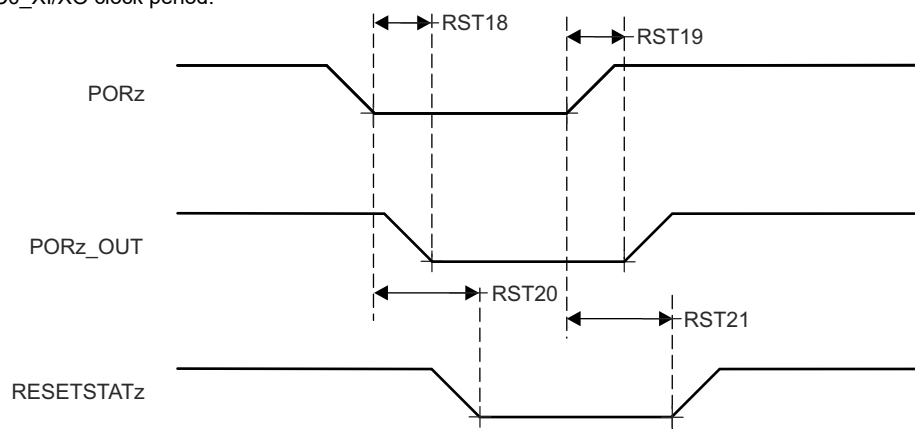
**Figure 6-12. MCU\_PORz initiates; MCU\_PORz\_OUT, PORz\_OUT, MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

**Table 6-9. PORz Initiates; PORz\_OUT and RESETSTATz Switching Characteristics**see [Figure 6-13](#)

| NO.   | PARAMETER                  |                                                            | MODE                                                | MIN                    | MAX | UNIT |
|-------|----------------------------|------------------------------------------------------------|-----------------------------------------------------|------------------------|-----|------|
| RST18 | $t_{d(PORzL-PORz\_OUTL)}$  | Delay time, PORz active (low) to PORz_OUT active (low)     | software control of POR_RST_ISO_DONE_Z              | $T^{(1)}$              |     |      |
|       |                            |                                                            | CTRLMMR_WKUP_POR_RST_CTRL[0].POR_RST_ISO_DONE_Z = 0 | 0                      |     | ns   |
| RST19 | $t_{d(PORzH-PORz\_OUTH)}$  | Delay time, PORz active (high) to PORz_OUT active (high)   |                                                     | 1300                   |     | ns   |
| RST20 | $t_{d(PORzL-RESETSTATzL)}$ | Delay time, PORz active (low) to RESETSTATz active (low)   |                                                     | $T^{(1)}$              |     |      |
|       |                            |                                                            | CTRLMMR_WKUP_POR_RST_CTRL[0].POR_RST_ISO_DONE_Z = 0 | 0                      |     | ns   |
| RST21 | $t_{d(PORzH-RESETSTATzH)}$ | Delay time, PORz active (high) to RESETSTATz active (high) |                                                     | 14500*S <sup>(2)</sup> |     | ns   |

(1) T = Reset Isolation Time (Software Dependent).

(2) S = MCU\_OSC0\_XI/XO clock period.

**Figure 6-13. PORz initiates; PORz\_OUT and RESETSTATz Switching Characteristics**

**Table 6-10. MCU\_RESETz Timing Requirements**

see [Figure 6-14](#)

| NO.   |                                      |                                              | MIN  | MAX | UNIT |
|-------|--------------------------------------|----------------------------------------------|------|-----|------|
| RST22 | $t_{w(MCU\_RESETzL)}$ <sup>(1)</sup> | Pulse Width minimum, MCU_RESETz active (low) | 1200 |     | ns   |

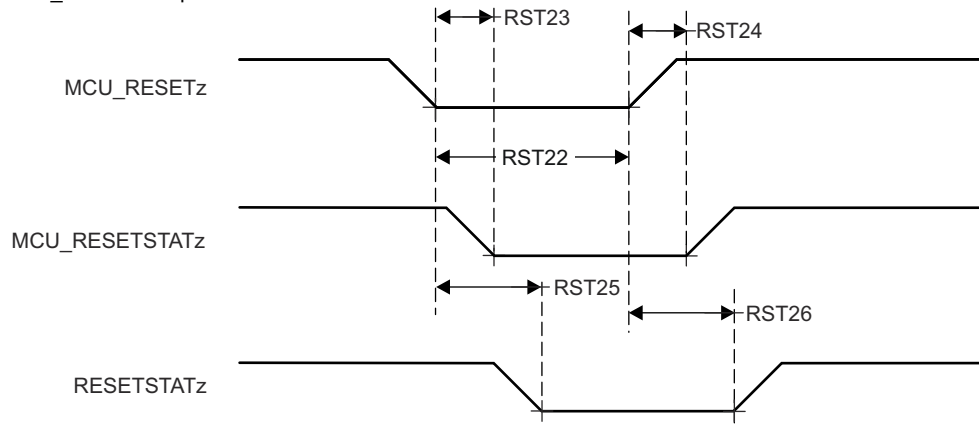
(1) Timing for MCU\_RESETz is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

**Table 6-11. MCU\_RESETz initiates; MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

see [Figure 6-14](#)

| NO.   |                                        | PARAMETER                                                                | MIN                   | MAX | UNIT |
|-------|----------------------------------------|--------------------------------------------------------------------------|-----------------------|-----|------|
| RST23 | $t_{d(MCU\_RESETzL-MCU\_RESETSTATzL)}$ | Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)       | 800                   |     | ns   |
| RST24 | $t_{d(MCU\_RESETzH-MCU\_RESETSTATzH)}$ | Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high) | 3900*S <sup>(1)</sup> |     | ns   |
| RST25 | $t_{d(MCU\_RESETzL-RESETSTATzL)}$      | Delay time, MCU_RESETz active (low) to RESETSTATz active (low)           | 800                   |     | ns   |
| RST26 | $t_{d(MCU\_RESETzH-RESETSTATzH)}$      | Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)     | 3900*S <sup>(1)</sup> |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.



**Figure 6-14. MCU\_RESETz initiates; MCU\_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics**

**Table 6-12. RESET\_REQz Timing Requirements**see [Figure 6-15](#)

| NO.   |                                    |                                              | MIN  | MAX | UNIT |
|-------|------------------------------------|----------------------------------------------|------|-----|------|
| RST27 | $t_{w(RES\_REQzL)}$ <sup>(1)</sup> | Pulse Width minimum, RESET_REQz active (low) | 1200 |     | ns   |

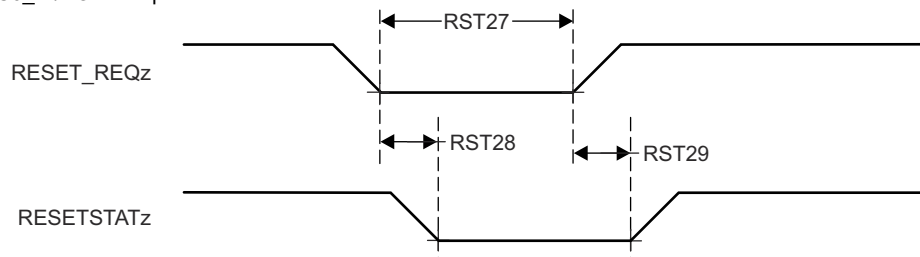
(1) Timing for RESET\_REQz is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

**Table 6-13. RESET\_REQz initiates; RESETSTATz Switching Characteristics**see [Figure 6-15](#)

| NO.   |                                 | PARAMETER                                                            | MODE                                                          | MIN                   | MAX | UNIT |
|-------|---------------------------------|----------------------------------------------------------------------|---------------------------------------------------------------|-----------------------|-----|------|
| RST28 | $t_{d(RES\_REQzL-RES\_STATzL)}$ | Delay time, RESET_REQz active (low) to RESETSTATz active (low)       | software control of SOC_WARMRST_ISO_DONE_Z                    | T <sup>(1)</sup>      |     |      |
|       |                                 |                                                                      | CTRLMMR_WKUP_MAIN_WARM_RST_CTRL[0].SOC_WARMRST_ISO_DONE_Z = 0 | 740                   |     | ns   |
| RST29 | $t_{d(RES\_REQzH-RES\_STATzH)}$ | Delay time, RESET_REQz inactive (high) to RESETSTATz inactive (high) |                                                               | 2650*S <sup>(2)</sup> |     | ns   |

(1) T = Reset Isolation Time (Software Dependent).

(2) S = MCU\_OSC0\_XI/XO clock period.

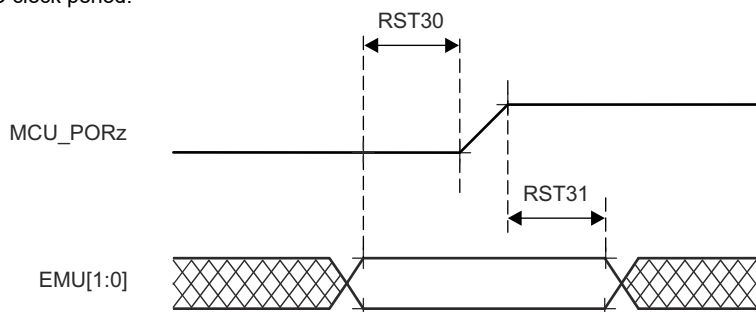
**Figure 6-15. RESET\_REQz initiates; RESETSTATz Timing Requirements and Switching Characteristics**

**Table 6-14. EMUx Timing Requirements**

see [Figure 6-16](#)

| NO.   |                          |                                                      | MIN               | MAX | UNIT |
|-------|--------------------------|------------------------------------------------------|-------------------|-----|------|
| RST30 | $t_{su}(EMUx-MCU\_PORz)$ | Setup time, EMU[1:0] before MCU_PORz inactive (high) | $3 \cdot S^{(1)}$ |     | ns   |
| RST31 | $t_h(MCU\_PORz - EMUx)$  | Hold time, EMU[1:0] after MCU_PORz inactive (high)   | 10                |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.



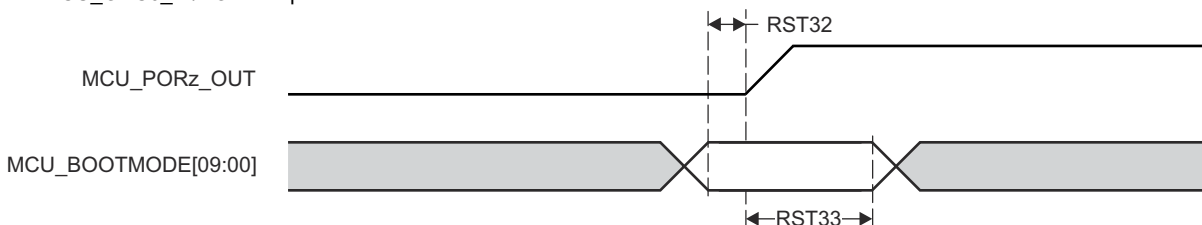
**Figure 6-16. EMUx Timing Requirements**

**Table 6-15. MCU\_BOOTMODE Timing Requirements**

see [Figure 6-17](#)

| NO.   |                                        |                                                          | MIN               | MAX | UNIT |
|-------|----------------------------------------|----------------------------------------------------------|-------------------|-----|------|
| RST32 | $t_{su}(MCU\_BOOTMODE-MCU\_PORz\_OUT)$ | Setup time, MCU_BOOTMODE[09:00] before MCU_PORz_OUT high | $3 \cdot S^{(1)}$ |     | ns   |
| RST33 | $t_h(MCU\_PORz\_OUT - MCU\_BOOTMODE)$  | Hold time, MCU_BOOTMODE[09:00] after MCU_PORz_OUT high   | 0                 |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.



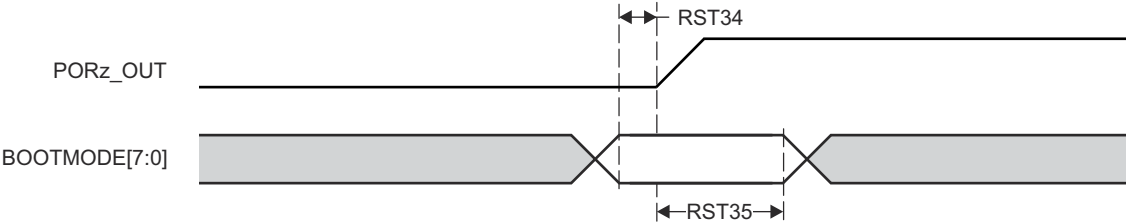
**Figure 6-17. MCU\_BOOTMODE Timing Requirements**

**Table 6-16. BOOTMODE Timing Requirements**

see [Figure 6-18](#)

| NO.   |                                     |                                                | MIN               | MAX | UNIT |
|-------|-------------------------------------|------------------------------------------------|-------------------|-----|------|
| RST34 | $t_{su}(\text{BOOTMODE-PORz\_OUT})$ | Setup time, BOOTMODE[7:0] before PORz_OUT high | $3 \cdot S^{(1)}$ |     | ns   |
| RST35 | $t_h(\text{PORz\_OUT - BOOTMODE})$  | Hold time, BOOTMODE[7:0] after PORz_OUT high   | 0                 |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.



**Figure 6-18. BOOTMODE Timing Requirements**

### 6.10.3.2 Safety Signal Timing

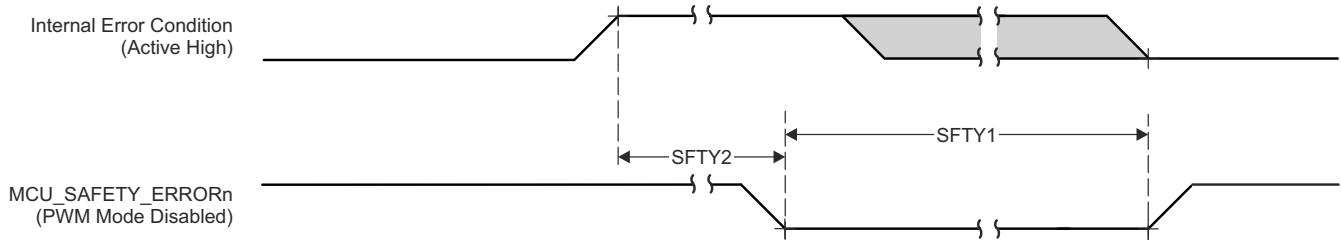
Tables and figures provided in this section define switching characteristics for MCU\_SAFETY\_ERRORn and SOC\_SAFETY\_ERRORn.

**Table 6-17. MCU\_SAFETY\_ERRORn Switching Characteristics**

see [Figure 6-19](#)

| NO.   | PARAMETER                                                                                                  | MIN                   | MAX | UNIT |
|-------|------------------------------------------------------------------------------------------------------------|-----------------------|-----|------|
| SFTY1 | $t_{w(MCU\_SAFETY\_ERRORn)}$<br>Pulse width minimum, MCU_SAFETY_ERRORn active (PWM mode disabled)          | $P \cdot R^{(1) (2)}$ |     | ns   |
| SFTY2 | $t_{d (ERROR\_CONDITION-MCU\_SAFETY\_ERRORnL)}$<br>Delay time, ERROR CONDITION to MCU_SAFETY_ERRORn active | $50 \cdot P^{(1)}$    |     | ns   |

- (1) P = ESM functional clock (MCU\_SYSCCLK0 /6).  
(2) R = Error Pin Counter Pre-Load Register count value.

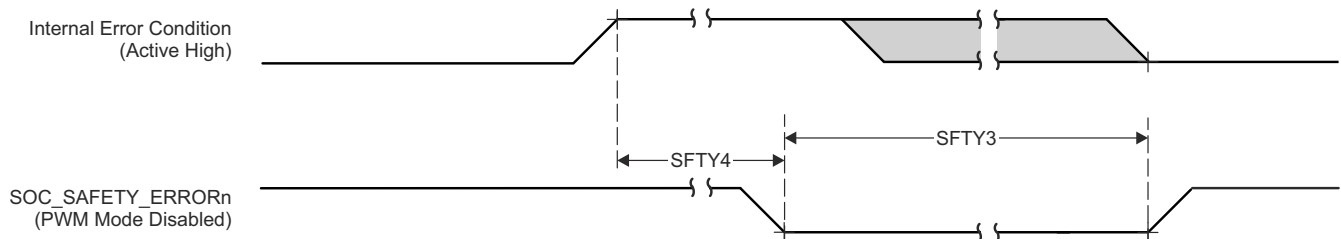


**Figure 6-19. MCU\_SAFETY\_ERRORn Switching Characteristics**

**Table 6-18. SOC\_SAFETY\_ERRORn Switching Characteristics**

see [Figure 6-20](#)

| NO.   | PARAMETER                                                                                                  | MIN                   | MAX | UNIT |
|-------|------------------------------------------------------------------------------------------------------------|-----------------------|-----|------|
| SFTY3 | $t_{w(SOC\_SAFETY\_ERRORn)}$<br>Pulse width minimum, SOC_SAFETY_ERRORn active (PWM mode disabled)          | $P \cdot R^{(1) (2)}$ |     | ns   |
| SFTY4 | $t_{d (ERROR\_CONDITION-SOC\_SAFETY\_ERRORnL)}$<br>Delay time, ERROR CONDITION to SOC_SAFETY_ERRORn active | $50 \cdot P^{(1)}$    |     | ns   |



**Figure 6-20. SOC\_SAFETY\_ERRORn Switching Characteristics**

### 6.10.3.3 Clock Timing

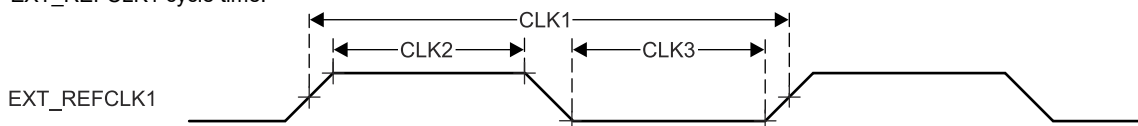
Tables and figures provided in this section define timing requirements and switching characteristics for clock signals.

**Table 6-19. Clock Timng Requiements**

see [Figure 6-21](#)

| NO.  |                        |                                          | MIN                  | MAX                  | UNIT |
|------|------------------------|------------------------------------------|----------------------|----------------------|------|
| CLK1 | $t_{c(EXT\_REFCLK1)}$  | Cycle time minimum, EXT_REFCLK1          | 10                   |                      | ns   |
| CLK2 | $t_{w(EXT\_REFCLK1H)}$ | Pulse Duration minimum, EXT_REFCLK1 high | $E \cdot 0.45^{(1)}$ | $E \cdot 0.55^{(1)}$ | ns   |
| CLK3 | $t_{w(EXT\_REFCLK1L)}$ | Pulse Duration minimum, EXT_REFCLK1 low  | $E \cdot 0.45^{(1)}$ | $E \cdot 0.55^{(1)}$ | ns   |

(1)  $E = EXT\_REFCLK1$  cycle time.



**Figure 6-21. Clock Timing Requirements**

**Table 6-20. Clock Switching Characteristics**

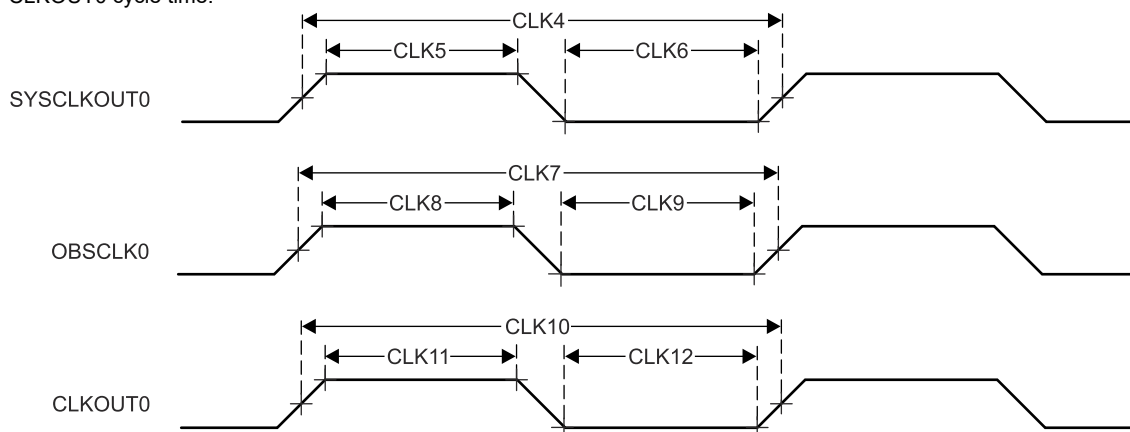
see [Figure 6-22](#)

| NO.   |                      | PARAMETER                               | MIN                 | MAX                 | UNIT |
|-------|----------------------|-----------------------------------------|---------------------|---------------------|------|
| CLK4  | $t_{c(SYSCLKOUT0)}$  | Cycle time minimum, SYSCLKOUT0          | 8                   |                     | ns   |
| CLK5  | $t_{w(SYSCLKOUT0H)}$ | Pulse Duration minimum, SYSCLKOUT0 high | $A \cdot 0.4^{(1)}$ | $A \cdot 0.6^{(1)}$ | ns   |
| CLK6  | $t_{w(SYSCLKOUT0L)}$ | Pulse Duration minimum, SYSCLKOUT0 low  | $A \cdot 0.4^{(1)}$ | $A \cdot 0.6^{(1)}$ | ns   |
| CLK7  | $t_{c(OBSCLK0)}$     | Cycle time minimum, OBSCLK0             | 5                   |                     | ns   |
| CLK8  | $t_{w(OBSCLK0H)}$    | Pulse Duration minimum, OBSCLK0 high    | $B \cdot 0.4^{(2)}$ | $B \cdot 0.6^{(2)}$ | ns   |
| CLK9  | $t_{w(OBSCLK0L)}$    | Pulse Duration minimum, OBSCLK0 low     | $B \cdot 0.4^{(2)}$ | $B \cdot 0.6^{(2)}$ | ns   |
| CLK10 | $t_{c(CLKOUT0)}$     | Cycle time minimum, CLKOUT0             | 20                  |                     | ns   |
| CLK11 | $t_{w(CLKOUT0H)}$    | Pulse Duration minimum, CLKOUT0 high    | $C \cdot 0.4^{(3)}$ | $C \cdot 0.6^{(3)}$ | ns   |
| CLK12 | $t_{w(CLKOUT0L)}$    | Pulse Duration minimum, CLKOUT0 low     | $C \cdot 0.4^{(3)}$ | $C \cdot 0.6^{(3)}$ | ns   |

(1)  $A = SYSCLKOUT0$  cycle time.

(2)  $B = OBSCLK0$  cycle time.

(3)  $C = CLKOUT0$  cycle time.



**Figure 6-22. Clock Switching Characteristics**

## 6.10.4 Clock Specifications

### 6.10.4.1 Input and Output Clocks / Oscillators

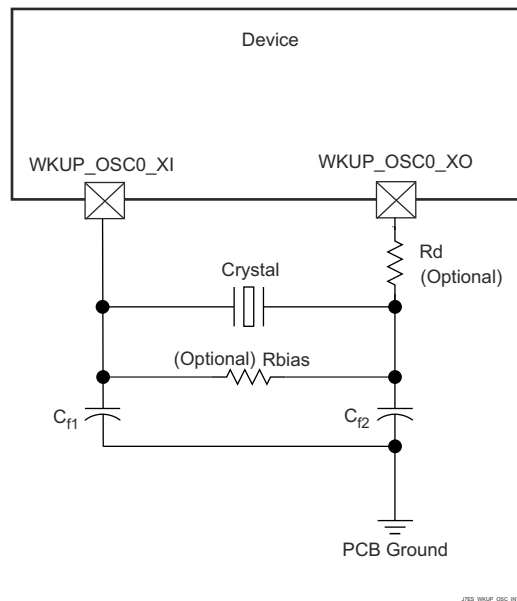
Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- High frequency oscillators inputs
  - OSC1\_XO/OSC1\_XI — external main crystal interface pins connected to internal oscillator which sources reference clock. Provides reference clock to PLLs within MCU domain and MAIN domain. This high-frequency oscillator is used to provide audio clock frequencies to MCASPs.
  - WKUP\_OSC0\_XO/WKUP\_OSC0\_XI — external main crystal interface pins connected to internal oscillator which sources reference clock. Provides reference clock to PLLs within WKUP and MAIN domain.
- Low frequency digital input
  - WKUP\_LF\_CLKIN - Low Frequency 32k digital clock input, optionally sourced from an external PMIC or other clock source. This SoC does not support a LFOSC crystal input.
- General purpose clock inputs
  - MCU\_EXT\_REFCLK0 - optional external System clock input (MCU domain).
  - EXT\_REFCLK1 — optional external System clock input (MAIN domain).
- Peripheral clocks - refer to the Signal Descriptions for peripheral specific clocks

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

#### 6.10.4.1.1 WKUP\_OSC0 Internal Oscillator Clock Source

Figure 6-23 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the WKUP\_OSC0\_XI and WKUP\_OSC0\_XO pins.



**Figure 6-23. WKUP\_OSC0 Crystal Implementation**

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-21 summarizes the required electrical constraints.

**Table 6-21. WKUP\_OSC0 Crystal Electrical Characteristics**

| PARAMETER             |                                                     |                 |                                             | MIN                      | TYP | MAX | UNIT |    |
|-----------------------|-----------------------------------------------------|-----------------|---------------------------------------------|--------------------------|-----|-----|------|----|
| F <sub>xtal</sub>     | Crystal Parallel Resonance Frequency                |                 |                                             | 19.2, 20, 24, 25, 26, 27 |     |     | MHz  |    |
| F <sub>xtal</sub>     | Crystal Frequency Stability and Tolerance           |                 | Ethernet RGMII and RMII not used            | ±100                     |     |     | ppm  |    |
|                       |                                                     |                 | Ethernet RGMII and RMII using derived clock | ±50                      |     |     |      |    |
| C <sub>L1+PCBXI</sub> | Capacitance of C <sub>L1</sub> + C <sub>PCBXI</sub> |                 |                                             | 12                       |     |     | 24   | pF |
| C <sub>L2+PCBXO</sub> | Capacitance of C <sub>L2</sub> + C <sub>PCBXO</sub> |                 |                                             | 12                       |     |     | 24   | pF |
| C <sub>L</sub>        | Crystal Load Capacitance                            |                 |                                             | 6                        |     |     | 12   | pF |
| C <sub>shunt</sub>    | Crystal Circuit Shunt Capacitance                   | 19.2 MHz, 20MHz | ESR <sub>xtal</sub> ≤ 30 Ω                  |                          |     |     | 7    | pF |
|                       |                                                     |                 | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 80 Ω           |                          |     |     | 5    | pF |
|                       |                                                     |                 | 80 Ω ≤ ESR <sub>xtal</sub> ≤ 100 Ω          |                          |     |     | 3    | pF |
|                       |                                                     | 24MHz           | ESR <sub>xtal</sub> ≤ 30 Ω                  |                          |     |     | 7    | pF |
|                       |                                                     |                 | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 60 Ω           |                          |     |     | 5    | pF |
|                       |                                                     |                 | 60 Ω ≤ ESR <sub>xtal</sub> ≤ 80 Ω           |                          |     |     | 3    | pF |
|                       |                                                     |                 | Not Supported: 80 Ω ≤ ESR <sub>xtal</sub>   |                          |     |     | —    |    |
|                       |                                                     | 25MHz           | ESR <sub>xtal</sub> ≤ 30 Ω                  |                          |     |     | 7    | pF |
|                       |                                                     |                 | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 50 Ω           |                          |     |     | 5    | pF |
|                       |                                                     |                 | 50 Ω ≤ ESR <sub>xtal</sub> ≤ 80 Ω           |                          |     |     | 3    | pF |
|                       |                                                     |                 | Not Supported: 80 Ω ≤ ESR <sub>xtal</sub>   |                          |     |     | —    |    |
|                       |                                                     | 26 MHz, 27 MHz  | ESR <sub>xtal</sub> ≤ 30 Ω                  |                          |     |     | 7    | pF |
|                       |                                                     |                 | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 50 Ω           |                          |     |     | 5    | pF |
|                       |                                                     |                 | Not Supported: 50 Ω ≤ ESR <sub>xtal</sub>   |                          |     |     | —    |    |
| ESR <sub>xtal</sub>   | Crystal Effective Series Resistance                 |                 |                                             | (1)                      |     |     | Ω    |    |

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C<sub>shunt</sub> parameter.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

Table 6-22 details the switching characteristics of the oscillator and the requirements of the input clock.

**Table  
6-22.  
WKUP\_O  
SC0  
Switchin  
g  
Characte  
ristics –  
Crystal  
Mode**

| PARAMETER       |                | PACKAGE | MIN | TYP | MAX   | UNIT |
|-----------------|----------------|---------|-----|-----|-------|------|
| PARAMETER       |                | PACKAGE | MIN | TYP | MAX   | UNIT |
| C <sub>XI</sub> | XI Capacitance | ALY     |     |     | 2.241 | pF   |
| C <sub>XO</sub> | XO Capacitance | ALY     |     |     | 2.210 | pF   |

**Table  
6-22.  
WKUP\_O  
SC0  
Switchin  
g  
Characte  
ristics –  
Crystal  
Mode  
(continue  
d)**

| PARAMETER         |                             | PACKAGE | MIN | TYP                | MAX  | UNIT |
|-------------------|-----------------------------|---------|-----|--------------------|------|------|
| PARAMETER         |                             | PACKAGE | MIN | TYP                | MAX  | UNIT |
| C <sub>XIXO</sub> | XI to XO Mutual Capacitance | ALY     |     |                    | 0.01 | pF   |
| t <sub>s</sub>    | Start-up Time               |         |     | 9.5 <sup>(1)</sup> |      | ms   |

**Table  
6-22.  
WKUP\_O  
SC0  
Switchin  
g  
Characte  
ristics –  
Crystal  
Mode**

| PARAMETER         |                             | PACKAGE | MIN | TYP                | MAX   | UNIT |
|-------------------|-----------------------------|---------|-----|--------------------|-------|------|
| PARAMETER         |                             | PACKAGE | MIN | TYP                | MAX   | UNIT |
| C <sub>XI</sub>   | XI Capacitance              | ALY     |     |                    | 2.241 | pF   |
|                   |                             | AND     |     |                    | 2.047 | pF   |
| C <sub>XO</sub>   | XO Capacitance              | ALY     |     |                    | 2.210 | pF   |
|                   |                             | AND     |     |                    | 1.972 | pF   |
| C <sub>XIXO</sub> | XI to XO Mutual Capacitance | ALY     |     |                    | 0.01  | pF   |
|                   |                             | AND     |     |                    | 0.01  | pF   |
| t <sub>s</sub>    | Start-up Time               |         |     | 9.5 <sup>(1)</sup> |       | ms   |

- (1) TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.

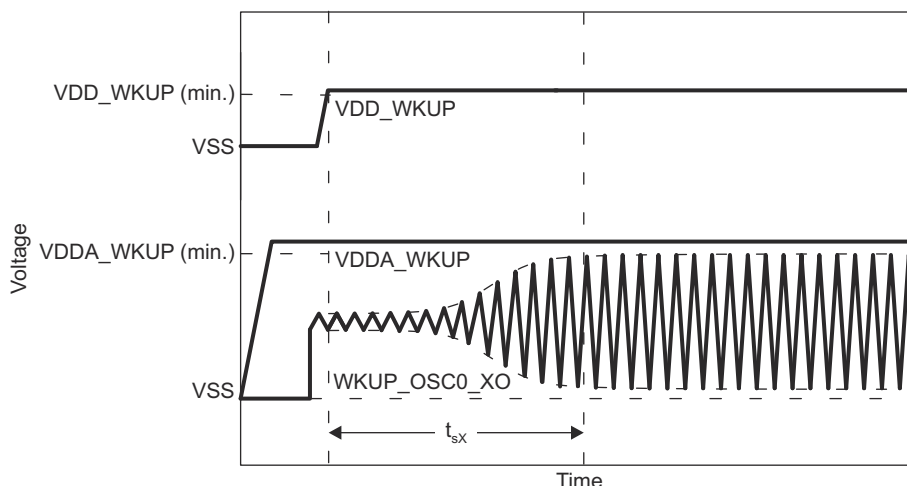


Figure 6-24. WKUP\_OSC0 Start-up Time

#### 6.10.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load,  $C_L$ , of this circuit is a combination of discrete capacitors  $C_{L1}$ ,  $C_{L2}$ , and several parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP\_OSC0\_XI and WKUP\_OSC0\_XO have parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where the PCB designer should be able to extract parasitic capacitance for each signal trace. The WKUP\_OSC0 circuits and device package have combined parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where these parasitic capacitance values are defined in Table 6-22.

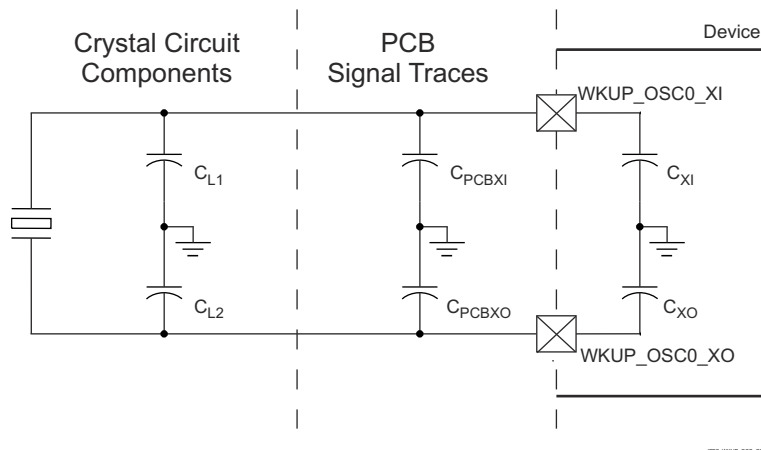


Figure 6-25. Load Capacitance

Load capacitors,  $C_{L1}$  and  $C_{L2}$  in Figure 6-23, should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer.

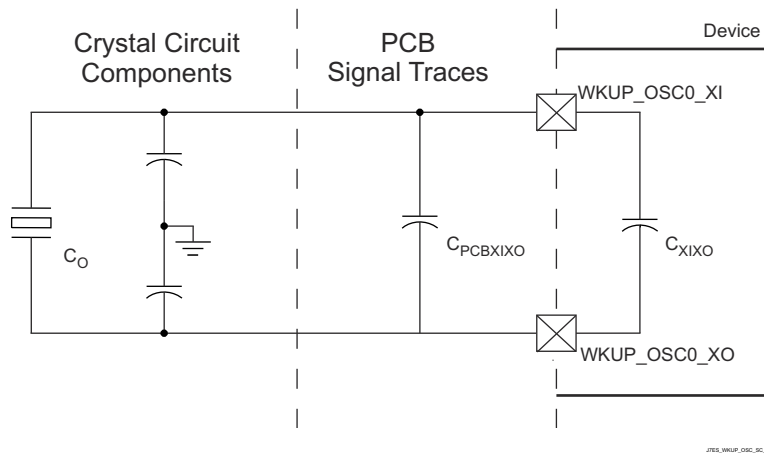
$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of  $C_{L1}$  and  $C_{L2}$ , multiply the capacitive load value  $C_L$  by 2. Using this result, subtract the combined values of  $C_{PCBXI} + C_{XI}$  to determine the value of  $C_{L1}$  and the combined values of  $C_{PCBXO} + C_{XO}$  to determine the value of  $C_{L2}$ . For example, if  $C_L = 10$  pF,  $C_{PCBXI} = 2.9$  pF,  $C_{XI} = 0.5$  pF,  $C_{PCBXO} = 3.7$  pF,  $C_{XO} = 0.5$  pF, the value of  $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10 \text{ pF}) - 2.9 \text{ pF} - 0.5 \text{ pF}] = 16.6$  pF and  $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10 \text{ pF}) - 3.7 \text{ pF} - 0.5 \text{ pF}] = 15.8$  pF

#### 6.10.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for WKUP\_OSC0 operating conditions defined in Table 6-21. Shunt capacitance,  $C_{shunt}$ , of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP\_OSC0 have mutual parasitic capacitance to each other,  $C_{PCBXIXO}$ , where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance,  $C_{XIXO}$ , where this mutual parasitic capacitance value is defined in Table 6-22.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.



**Figure 6-26. Shunt Capacitance**

A crystal should be chosen such that the below equation is satisfied.  $C_O$  in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$$

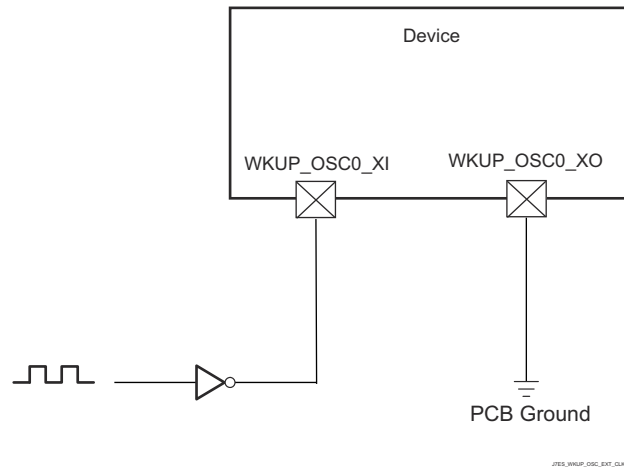
For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30  $\Omega$ ,  $C_{PCBXIXO}$  = 0.04 pF,  $C_{XIXO}$  = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

#### 6.10.4.1.2 WKUP\_OSC0 LVC MOS Digital Clock Source

Figure 6-27 shows the recommended oscillator connections when WKUP\_OSC0\_XI is connected to a 1.8-V LVC MOS square-wave digital clock source.

#### Note

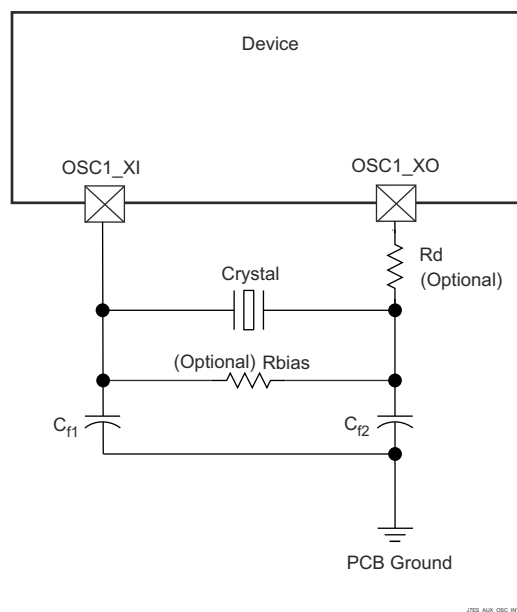
A DC steady-state condition is not allowed on WKUP\_OSC0\_XI when the oscillator is powered up. This is not allowed because WKUP\_OSC0\_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down WKUP\_OSC0 any time WKUP\_OSC0\_XI is not toggling between logic states.



**Figure 6-27. 1.8-V LVCMOS-Compatible Clock Input**

#### 6.10.4.1.3 Auxiliary OSC1 Internal Oscillator Clock Source

Figure 6-28 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the OSC1\_XI and OSC1\_XO pins.



**Figure 6-28. OSC1 Crystal Implementation**

The crystal must be in the fundamental mode of operation and parallel resonant. [Table 6-23](#) summarizes the required electrical constraints.

**Table 6-23. OSC1 Crystal Electrical Characteristics**

| PARAMETER             |                                                     |                                     |                                             | MIN  | TYP | MAX  | UNIT |
|-----------------------|-----------------------------------------------------|-------------------------------------|---------------------------------------------|------|-----|------|------|
| F <sub>xtal</sub>     | Crystal Parallel Resonance Frequency                |                                     |                                             | 19.2 |     | 27   | MHz  |
| F <sub>xtal</sub>     | Crystal Frequency Stability and Tolerance           |                                     | Ethernet RGMII and RMII not used            |      |     | ±100 | ppm  |
|                       |                                                     |                                     | Ethernet RGMII and RMII using derived clock |      |     | ±50  |      |
| C <sub>L1+PCBXI</sub> | Capacitance of C <sub>L1</sub> + C <sub>PCBXI</sub> |                                     |                                             | 12   |     | 24   | pF   |
| C <sub>L2+PCBXO</sub> | Capacitance of C <sub>L2</sub> + C <sub>PCBXO</sub> |                                     |                                             | 12   |     | 24   | pF   |
| C <sub>L</sub>        | Crystal Load Capacitance                            |                                     |                                             | 6    |     | 12   | pF   |
| C <sub>shunt</sub>    | Crystal Circuit Shunt Capacitance                   | 19.2MHz ≤ F <sub>xtal</sub> ≤ 20MHz | ESR <sub>xtal</sub> ≤ 30 Ω                  |      |     | 7    | pF   |
|                       |                                                     |                                     | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 80 Ω           |      |     | 5    | pF   |
|                       |                                                     |                                     | 80 Ω ≤ ESR <sub>xtal</sub> ≤ 100 Ω          |      |     | 3    | pF   |
|                       | 20MHz ≤ F <sub>xtal</sub> ≤ 24.576MHz               |                                     | ESR <sub>xtal</sub> ≤ 30 Ω                  |      |     | 7    | pF   |
|                       |                                                     |                                     | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 60 Ω           |      |     | 5    | pF   |
|                       |                                                     |                                     | 60 Ω ≤ ESR <sub>xtal</sub> ≤ 80 Ω           |      |     | 3    | pF   |
|                       |                                                     |                                     | Not Supported: 80 Ω ≤ ESR <sub>xtal</sub>   |      |     | –    |      |
|                       | 24.576MHz ≤ F <sub>xtal</sub> ≤ 25MHz               |                                     | ESR <sub>xtal</sub> ≤ 30 Ω                  |      |     | 7    | pF   |
|                       |                                                     |                                     | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 50 Ω           |      |     | 5    | pF   |
|                       |                                                     |                                     | 50 Ω ≤ ESR <sub>xtal</sub> ≤ 80 Ω           |      |     | 3    | pF   |
|                       |                                                     |                                     | Not Supported: 80 Ω ≤ ESR <sub>xtal</sub>   |      |     | –    |      |
|                       | 25MHz ≤ F <sub>xtal</sub> ≤ 27MHz                   |                                     | ESR <sub>xtal</sub> ≤ 30 Ω                  |      |     | 7    | pF   |
|                       |                                                     |                                     | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 50 Ω           |      |     | 5    | pF   |
|                       |                                                     |                                     | Not Supported: 50 Ω ≤ ESR <sub>xtal</sub>   |      |     | –    |      |
| ESR <sub>xtal</sub>   | Crystal Effective Series Resistance                 |                                     |                                             |      |     | 100  | Ω    |

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

[Table 6-24](#) details the switching characteristics of the oscillator and the requirements of the input clock.

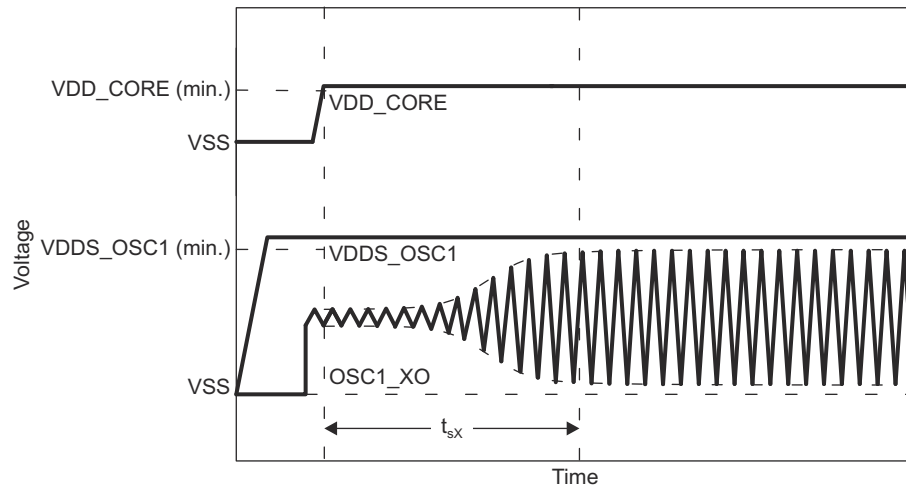
**Table  
6-24.  
OSC1  
Switchin  
g  
Characte  
ristics –  
Crystal  
Mode**

| PARAMETER         |                             | PACKAGE | MIN | TYP                | MAX   | UNIT |
|-------------------|-----------------------------|---------|-----|--------------------|-------|------|
| PARAMETER         |                             | PACKAGE | MIN | TYP                | MAX   | UNIT |
| C <sub>XI</sub>   | XI Capacitance              | ALY     |     |                    | 1.989 | pF   |
| C <sub>XO</sub>   | XO Capacitance              | ALY     |     |                    | 1.971 | pF   |
| C <sub>XIXO</sub> | XI to XO Mutual Capacitance | ALY     |     |                    | 0.01  | pF   |
| t <sub>s</sub>    | Start-up Time               |         |     | 9.5 <sup>(1)</sup> |       | ms   |

**Table  
6-24.  
OSC1  
Switchin  
g  
Characte  
ristics –  
Crystal  
Mode**

| PARAMETER         |                             | PACKAGE | MIN | TYP                | MAX   | UNIT |
|-------------------|-----------------------------|---------|-----|--------------------|-------|------|
| PARAMETER         |                             | PACKAGE | MIN | TYP                | MAX   | UNIT |
| C <sub>XI</sub>   | XI Capacitance              | ALY     |     |                    | 1.989 | pF   |
|                   |                             | AND     |     |                    | 2.548 | pF   |
| C <sub>XO</sub>   | XO Capacitance              | ALY     |     |                    | 1.971 | pF   |
|                   |                             | AND     |     |                    | 2.878 | pF   |
| C <sub>XIXO</sub> | XI to XO Mutual Capacitance | ALY     |     |                    | 0.01  | pF   |
|                   |                             | AND     |     |                    | 0.01  | pF   |
| t <sub>s</sub>    | Start-up Time               |         |     | 9.5 <sup>(1)</sup> |       | ms   |

- (1) TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.



**Figure 6-29. OSC1 Start-up Time**

#### 6.10.4.1.3.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load,  $C_L$ , of this circuit is a combination of discrete capacitors  $C_{L1}$ ,  $C_{L2}$ , and several parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1\_XI and OSC1\_XO have parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where the PCB designer should be able to extract parasitic capacitance for each signal trace. The OSC1 circuits and device package have combined parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where these parasitic capacitance values are defined in [Table 6-24](#).

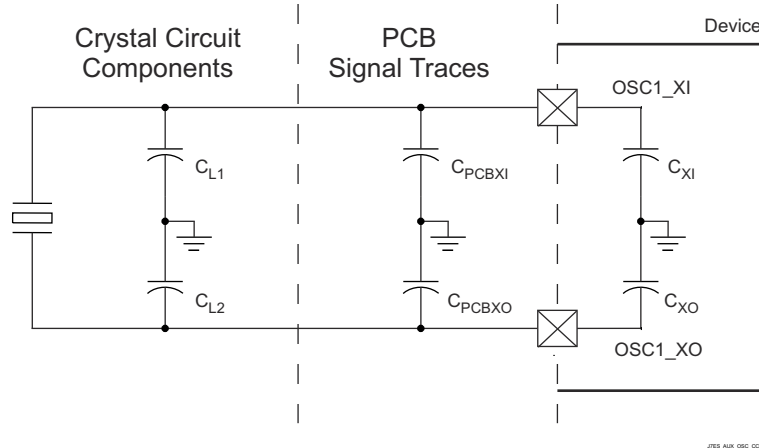


Figure 6-30. Load Capacitance

Load capacitors,  $C_{L1}$  and  $C_{L2}$  in Figure 6-28, should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of  $C_{L1}$  and  $C_{L2}$ , multiply the capacitive load value  $C_L$  by 2. Using this result, subtract the combined values of  $C_{PCBXI} + C_{XI}$  to determine the value of  $C_{L1}$  and the combined values of  $C_{PCBXO} + C_{XO}$  to determine the value of  $C_{L2}$ . For example, if  $C_L = 10$  pF,  $C_{PCBXI} = 2.9$  pF,  $C_{XI} = 0.5$  pF,  $C_{PCBXO} = 3.7$  pF,  $C_{XO} = 0.5$  pF, the value of  $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10 \text{ pF}) - 2.9 \text{ pF} - 0.5 \text{ pF}] = 16.6 \text{ pF}$  and  $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10 \text{ pF}) - 3.7 \text{ pF} - 0.5 \text{ pF}] = 15.8 \text{ pF}$

#### 6.10.4.1.3.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for OSC1 operating conditions defined in Table 6-23. Shunt capacitance,  $C_{shunt}$ , of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1 have mutual parasitic capacitance to each other,  $C_{PCBXIXO}$ , where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance,  $C_{XIXO}$ , where this mutual parasitic capacitance value is defined in Table 6-24.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

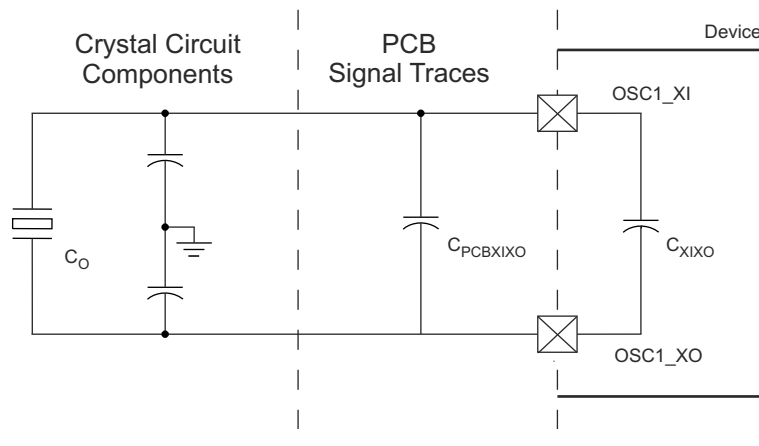


Figure 6-31. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied.  $C_O$  in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{\text{shunt}} \geq C_O + C_{\text{PCBXIXO}} + C_{\text{XIXO}}$$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30  $\Omega$ ,  $C_{\text{PCBXIXO}} = 0.04$  pF,  $C_{\text{XIXO}} = 0.01$  pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

#### 6.10.4.1.4 Auxiliary OSC1 LVC MOS Digital Clock Source

Figure 6-32 shows the recommended oscillator connections when OSC1 is connected to a 1.8-V LVC MOS square-wave digital clock source.

#### Note

A DC steady-state condition is not allowed on OSC1\_XI when the oscillator is powered up. This is not allowed because OSC1\_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down OSC1 any time OSC1\_XI is not toggling between logic states.

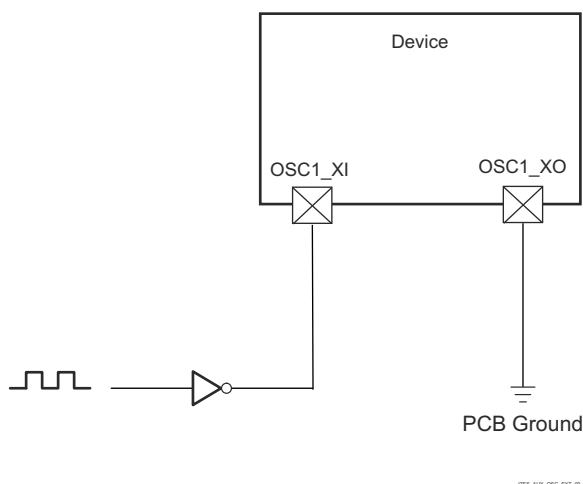


Figure 6-32. 1.8-V LVC MOS-Compatible Clock Input

#### 6.10.4.1.5 Auxiliary OSC1 Not Used

Figure 6-33 shows the recommended oscillator connections when OSC1 is not used. OSC1\_XI must be connected to VSS through an external pull resistor ( $R_{pd}$ ) to ensure this input is held to a valid low level when unused since the internal pull-down resistor is disabled by default.

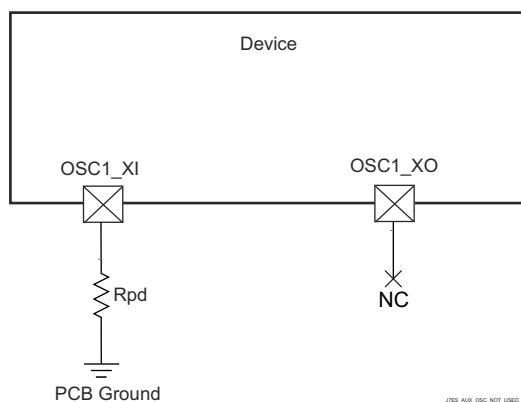


Figure 6-33. OSC1 Not Used

#### 6.10.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU\_CLKOUT0**
  - Reference clock output for Ethernet PHYs (50 MHz or 25 MHz)
- **MCU\_SYCLKOUT0**
  - MCU\_SYCLK0 is divided by 4 and then sent out of the device as a LVCMOS clock signal (MCU\_SYCLKOUT0). This signal can be used to test if the main chip clock is functioning or not. This signal should not be used as a clock source for external devices on a board.
- **MCU\_OBSCLK0**
  - On the clock output MCU\_OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug. This signal should not be used as a clock source for external devices on a board.
- **SYCLKOUT0**
  - SYCLK0 is divided by 4 and then sent out of the device as a LVCMOS clock signal (SYCLKOUT0). This signal can be used to test if the main chip clock is functioning or not. This signal should not be used as a clock source for external devices on a board.
- **CLKOUT**
  - Reference clock output for Ethernet PHYs (50 MHz)
- **OBSCLK[1:0]**
  - On the clock output OBSCLK0/1, oscillators and PLLs clocks can be observed for tests and debug.

#### 6.10.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuitries (PLLs) by internal regulators that derive power from the off-chip power-supply.

There are total of three PLLs in the device in WKUP and MCU domains:

- MCU\_PLL0 (MCU R5FSS PLL) with WKUP\_PLLCTRL0
- MCU\_PLL1 (MCU PERIPHERAL PLL)
- MCU\_PLL2 (MCU CPSW PLL)

There are total of twenty PLLs in the device in MAIN domain:

- PLL0 (MAIN PLL) with PLLCTRL0
- PLL1 (PER0 PLL)
- PLL2 (PER1 PLL)
- PLL3 (CPSW9G PLL)
- PLL4 (AUDIO0 PLL)
- PLL5 (VIDEO PLL)
- PLL6 (GPU PLL)
- PLL7 (C7x PLL)
- PLL8 (ARM0 PLL)
- PLL12 (DDR PLL)
- PLL13 (C66 PLL)
- PLL14 (R5F PLL)
- PLL15 (AUDIO1 PLL)
- PLL16 (DSS PLL0)
- PLL17 (DSS PLL1)
- PLL18 (DSS PLL2)
- PLL19 (DSS PLL3)
- PLL23 (DSS PLL7)
- PLL24 (MLB PLL)
- PLL25 (VISION PLL)

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#### Note

For more information, see:

- *Device Configuration / Clocking / PLLs* section in the device TRM.
  - *Peripherals / Display Subsystem Overview* section in the device TRM.
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#### Note

The input reference clock (OSC1\_XI/OSC1\_XO) is specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter in the device TRM.

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#### 6.10.4.4 Module and Peripheral Clocks Frequencies

[Section 6.10.5, Peripherals](#) section documents the maximum frequency associated with the peripheral clocks of the device.

For more details on the clocking structure of each module, reference *Device Configurations* chapter in the device TRM.

## 6.10.5 Peripherals

### 6.10.5.1 ATL

The device contains ATL module that can be used for asynchronous sample rate conversion of audio. The ATL calculates the error between two time bases, such as audio syncs, and optionally generates an averaged clock using cycle stealing via software.

#### Note

For more information about ATL, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

Table 6-25 represents ATL timing conditions.

**Table 6-25. ATL Timing Conditions**

| PARAMETER                |                         | MODE                   | MIN | MAX | UNIT |
|--------------------------|-------------------------|------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |                        |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | External reference CLK | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |                        |     |     |      |
| C <sub>L</sub>           | Output load capacitance | Internal reference CLK | 1   | 10  | pF   |

Section 6.10.5.1.1, Section 6.10.5.1.2, Section 6.10.5.1.3, and Section 6.10.5.1.4 present timing requirements and switching characteristics for ATL.

#### 6.10.5.1.1 ATL\_PCLK Timing Requirements

| NO. | PARAMETER             |                               | MODE                   | MIN                         | MAX | UNIT |
|-----|-----------------------|-------------------------------|------------------------|-----------------------------|-----|------|
| D1  | t <sub>c(pclk)</sub>  | Cycle time, ATL_PCLK          | External reference CLK | 5                           |     | ns   |
| D2  | t <sub>w(pclkL)</sub> | Pulse Duration, ATL_PCLK low  | External reference CLK | $0.45 \times M^{(1)} + 2.5$ |     | ns   |
| D3  | t <sub>w(pclkH)</sub> | Pulse Duration, ATL_PCLK high | External reference CLK | $0.45 \times M^{(1)} + 2.5$ |     | ns   |

(1) M = ATL\_CLK[x] period

#### 6.10.5.1.2 ATL\_AWS[x] Timing Requirements

| NO. | PARAMETER            |                                                | MODE                   | MIN                         | MAX | UNIT |
|-----|----------------------|------------------------------------------------|------------------------|-----------------------------|-----|------|
| D4  | t <sub>c(aws)</sub>  | Cycle Time, ATL_AWS[x] <sup>(3)</sup>          | External reference CLK | $2 \times M^{(1)}$          |     | ns   |
| D5  | t <sub>w(awsL)</sub> | Pulse Duration, ATL_AWS[x] <sup>(3)</sup> low  | External reference CLK | $0.45 \times A^{(2)} + 2.5$ |     | ns   |
| D6  | t <sub>w(awsH)</sub> | Pulse Duration, ATL_AWS[x] <sup>(3)</sup> high | External reference CLK | $0.45 \times A^{(2)} + 2.5$ |     | ns   |

(1) M = ATL\_CLK[x] period

(2) A = ATL\_AWS[x] period

(3) x = 0 to 3

#### 6.10.5.1.3 ATL\_BWS[x] Timing Requirements

| NO. | PARAMETER            |                                               | MODE                     | MIN                         | MAX | UNIT |
|-----|----------------------|-----------------------------------------------|--------------------------|-----------------------------|-----|------|
| D7  | t <sub>c(bws)</sub>  | Cycle Time, ATL_BWS[x] <sup>(3)</sup>         | External reference clock | $2 \times M^{(1)}$          |     | ns   |
| D8  | t <sub>w(bwsL)</sub> | Pulse Duration, ATL_BWS[x] low <sup>(3)</sup> | External reference clock | $0.45 \times B^{(2)} + 2.5$ |     | ns   |

| NO. |               |                                                | MODE                     | MIN                         | MAX | UNIT |
|-----|---------------|------------------------------------------------|--------------------------|-----------------------------|-----|------|
| D9  | $t_{w(bwsH)}$ | Pulse Duration, ATL_BWS[x] high <sup>(3)</sup> | External reference clock | $0.45 \times B^{(2)} + 2.5$ |     | ns   |

(1) M = ATL\_CLK[x] period

(2) B = ATL\_BWS[x] period

(3) x = 0 to 3

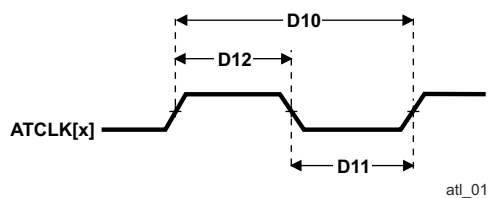
**6.10.5.1.4 ATCLK[x] Switching Characteristics**

| NO. |                 | PARAMETER                                    | MODE                   | MIN                                   | MAX | UNIT |
|-----|-----------------|----------------------------------------------|------------------------|---------------------------------------|-----|------|
| D10 | $t_{c(atclk)}$  | Cycle time, ATCLK[x] <sup>(3)</sup>          | Internal reference CLK | 20                                    |     | ns   |
| D11 | $t_{w(atclkL)}$ | Pulse Duration, ATCLK[x] low <sup>(3)</sup>  | Internal reference CLK | $0.45 \times P^{(2)} - M^{(1)} - 0.3$ |     | ns   |
| D12 | $t_{w(atclkH)}$ | Pulse Duration, ATCLK[x] high <sup>(3)</sup> | Internal reference CLK | $0.45 \times P^{(2)} - M^{(1)} - 0.3$ |     | ns   |

(1) M = ATL\_CLK[x] period

(2) P = ATCLK[x] period

(3) x = 0 to 3

**Figure 6-34. ATCLK[x] Timing**

### 6.10.5.2 CPSW2G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

#### 6.10.5.2.1 CPSW2G MDIO Interface Timings

Table 6-26 represents CPSW2G timing conditions.

**Table 6-26. CPSW2G MDIO Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input signal slew rate  | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 10  | 470 | pF   |

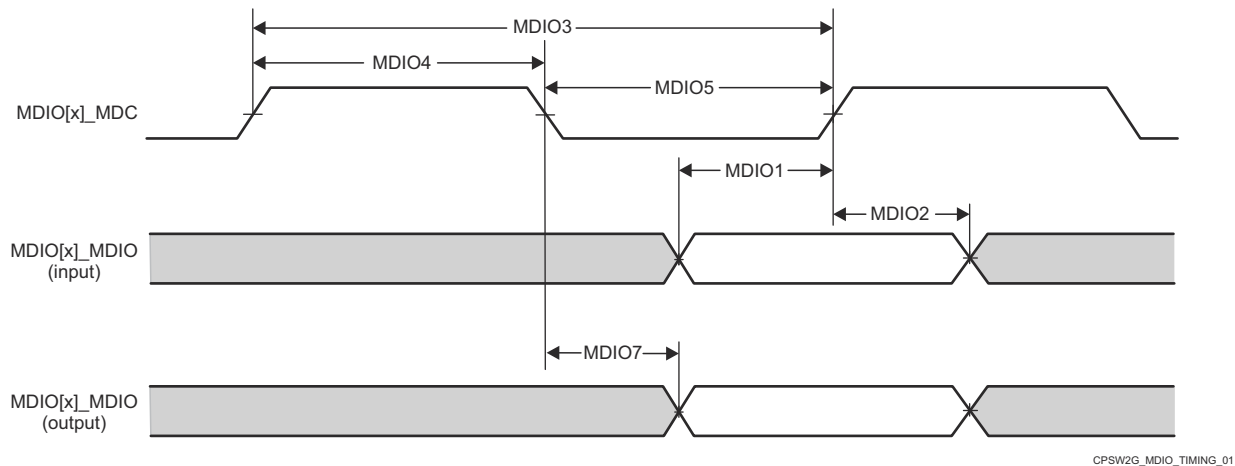
Table 6-27, Table 6-28, and Figure 6-35 present timing requirements for MDIO.

**Table 6-27. CPSW2G MDIO Timing Requirements**

| NO.   |                             |                                                        | MIN | MAX | UNIT |
|-------|-----------------------------|--------------------------------------------------------|-----|-----|------|
| MDIO1 | t <sub>su(mdioV-mdcH)</sub> | Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high | 90  |     | ns   |
| MDIO2 | t <sub>h(mdcH-mdioV)</sub>  | Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high   | 0   |     | ns   |

**Table 6-28. CPSW2G MDIO Switching Characteristics**

| NO.   | PARAMETER                  | MIN  | MAX | UNIT |
|-------|----------------------------|------|-----|------|
| MDIO3 | t <sub>c(mdc)</sub>        |      | 400 | ns   |
| MDIO4 | t <sub>w(mdcH)</sub>       |      | 160 | ns   |
| MDIO5 | t <sub>w(mdcL)</sub>       |      | 160 | ns   |
| MDIO7 | t <sub>d(mdcL-mdioV)</sub> | –150 | 150 | ns   |



#### Note

x = 0 in MCU domain

**Figure 6-35. CPSW2G MDIO Timing Requirements and Switching Characteristics**

### 6.10.5.2.2 CPSW2G RMII Timings

Table 6-29, Section 6.10.5.2.2.1, Section 6.10.5.2.2.2, and Section 6.10.5.2.2.3 present timing conditions, requirements, and switching characteristics for CPSW2G RMII.

**Table 6-29. CPSW2G RMII Timing Conditions**

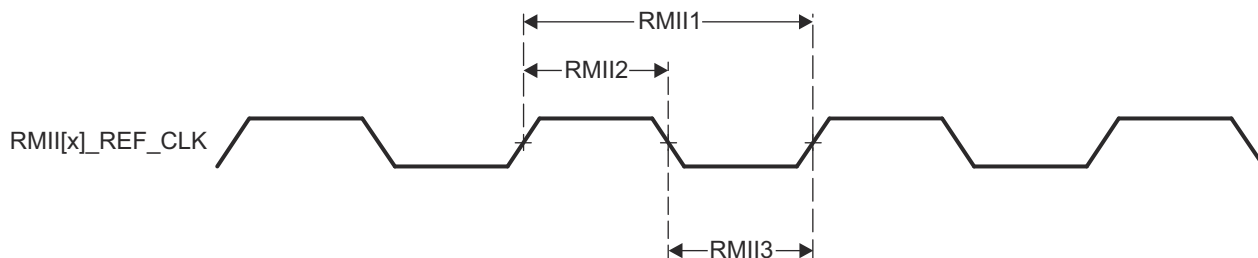
| PARAMETER         |                         |                            | MIN   | MAX  | UNIT |
|-------------------|-------------------------|----------------------------|-------|------|------|
| INPUT CONDITIONS  |                         |                            |       |      |      |
| SR <sub>I</sub>   | Input signal slew rate  | VDD <sup>(1)</sup> = 1.8 V | 0.108 | 0.54 | V/ns |
|                   |                         | VDD <sup>(1)</sup> = 3.3 V | 0.4   | 1.2  | V/ns |
| OUTPUT CONDITIONS |                         |                            |       |      |      |
| C <sub>L</sub>    | Output load capacitance |                            | 3     | 25   | pF   |

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the [Pin Attributes](#)

#### 6.10.5.2.2.1 CPSW2G RMII[x]\_REF\_CLK Timing Requirements – RMII Mode

see [Figure 6-36](#)

| NO.   |                          |                                      | MIN    | MAX | UNIT |
|-------|--------------------------|--------------------------------------|--------|-----|------|
| RMII1 | t <sub>c(ref_clk)</sub>  | Cycle time, RMII[x]_REF_CLK          | 19.999 | 20  | ns   |
| RMII2 | t <sub>w(ref_clkH)</sub> | Pulse Duration, RMII[x]_REF_CLK high | 7      | 13  | ns   |
| RMII3 | t <sub>w(ref_clkL)</sub> | Pulse Duration, RMII[x]_REF_CLK low  | 7      | 13  | ns   |

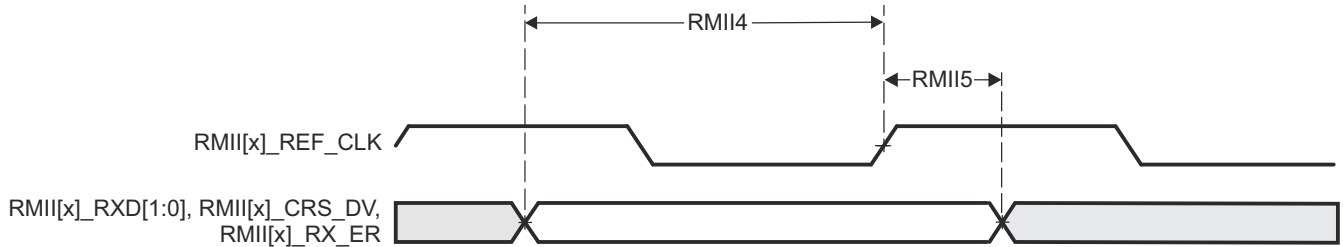


A. x = 1 in MCU domain.

**Figure 6-36. CPSW2G RMII[x]\_REFCLK Timing Requirements – RMII Mode**

#### 6.10.5.2.2.2 CPSW2G RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, and RMII[x]\_RX\_ER Timing Requirements – RMII Mode

| NO.   |                                   |                                                                       | MIN | MAX | UNIT |
|-------|-----------------------------------|-----------------------------------------------------------------------|-----|-----|------|
| RMII4 | t <sub>su(rxdV-ref_clkH)</sub>    | Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK rising edge | 4   |     | ns   |
|       | t <sub>su(crs_dvV-ref_clkH)</sub> | Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK rising edge   | 4   |     | ns   |
|       | t <sub>su(rx_erV-ref_clkH)</sub>  | Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK rising edge    | 4   |     | ns   |
| RMII5 | t <sub>h(ref_clkH-rxdV)</sub>     | Hold time, RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK rising edge   | 2   |     | ns   |
|       | t <sub>h(ref_clkH-crs_dvV)</sub>  | Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK rising edge     | 2   |     | ns   |
|       | t <sub>h(ref_clkH-rx_erV)</sub>   | Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK rising edge      | 2   |     | ns   |



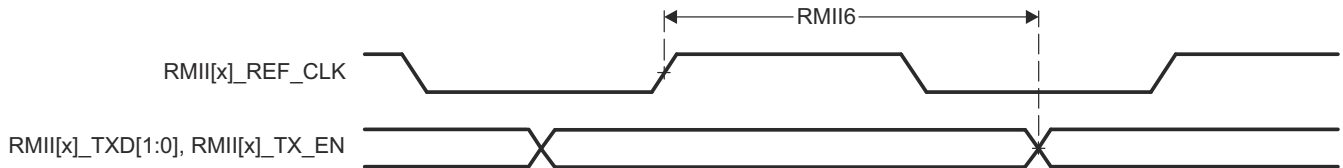
**Figure 6-37. CPSW2G RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, RMII[x]\_RX\_ER Timing Requirements – RMII Mode**

Section 6.10.5.2.2.3, and Figure 6-38 present switching characteristics for CPSW2G RMII Transmit.

#### 6.10.5.2.2.3 CPSW2G RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics – RMII Mode

see Figure 6-38

| NO.   | PARAMETER                         |                                                                   | MIN | MAX | UNIT |
|-------|-----------------------------------|-------------------------------------------------------------------|-----|-----|------|
| RMII6 | $t_{d(\text{ref\_clkH-txdV})}$    | Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TXD[1:0] valid | 2   | 10  | ns   |
|       | $t_{d(\text{ref\_clkH-tx\_enV})}$ | Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TX_EN valid    | 2   | 10  | ns   |



**Figure 6-38. RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics – RMII Mode**

#### 6.10.5.2.3 CPSW2G RGMII Timings

Section 6.10.5.2.3.1, Section 6.10.5.2.3.2, and Figure 6-40 present timing requirements for receive RGMII operation.

For more information, see *Gigabit Ethernet MAC (MCU\_CPSW0)* section in *Peripherals* chapter in the device TRM.

**Table 6-30. CPSW2G RGMII Timing Conditions**

| PARAMETER                             |                                              |                                                       | MIN  | MAX | UNIT |
|---------------------------------------|----------------------------------------------|-------------------------------------------------------|------|-----|------|
| INPUT CONDITIONS                      |                                              |                                                       |      |     |      |
| SR <sub>I</sub>                       | Input slew rate                              | VDD <sup>(1)</sup> = 1.8 V                            | 1.44 | 5   | V/ns |
|                                       |                                              | VDD <sup>(1)</sup> = 3.3 V                            | 2.64 | 5   | V/ns |
| OUTPUT CONDITIONS                     |                                              |                                                       |      |     |      |
| C <sub>L</sub>                        | Output load capacitance                      |                                                       | 2    | 20  | pF   |
| PCB CONNECTIVITY REQUIREMENTS         |                                              |                                                       |      |     |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | RGMII[x]_RXC,<br>RGMII[x]_RD[3:0],<br>RGMII[x]_RX_CTL |      | 50  | ps   |
|                                       |                                              | RGMII[x]_TXC,<br>RGMII[x]_TD[3:0],<br>RGMII[x]_TX_CTL |      | 50  | ps   |

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the [Pin Attributes](#).

### 6.10.5.2.3.1 RGMII[x]\_RXC Timing Requirements – RGMII Mode

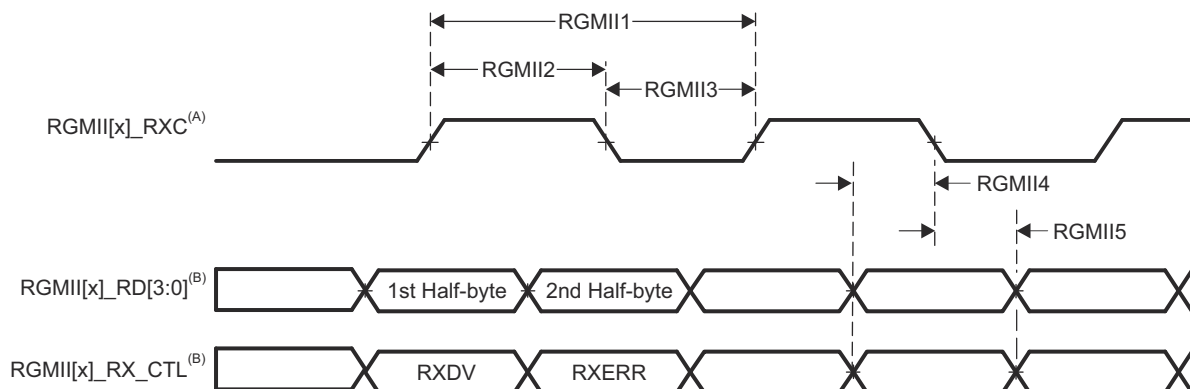
see [Figure 6-39](#)

| NO.    |               |                                   | MODE     | MIN | MAX | UNIT |
|--------|---------------|-----------------------------------|----------|-----|-----|------|
| RGMII1 | $t_{c(rxc)}$  | Cycle time, RGMII[x]_RXC          | 10Mbps   | 360 | 440 | ns   |
|        |               |                                   | 100Mbps  | 36  | 44  | ns   |
|        |               |                                   | 1000Mbps | 7.2 | 8.8 | ns   |
| RGMII2 | $t_{w(rxcH)}$ | Pulse duration, RGMII[x]_RXC high | 10Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000Mbps | 3.6 | 4.4 | ns   |
| RGMII3 | $t_{w(rxcL)}$ | Pulse duration, RGMII[x]_RXC low  | 10Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000Mbps | 3.6 | 4.4 | ns   |

### 6.10.5.2.3.2 CPSW2G Timing Requirements for RGMII[x]\_RD[3:0], and RGMII[x]\_RCTL – RGMII Mode

see [Figure 6-39](#)

| NO.    |                         |                                                                   | MODE     | MIN | MAX | UNIT |
|--------|-------------------------|-------------------------------------------------------------------|----------|-----|-----|------|
| RGMII4 | $t_{su(rdV-rxcV)}$      | Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC transition | 10Mbps   | 1   |     | ns   |
|        |                         |                                                                   | 100Mbps  | 1   |     | ns   |
|        |                         |                                                                   | 1000Mbps | 1   |     | ns   |
|        | $t_{su(rx\_ctlV-rxcV)}$ | Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC transition  | 10Mbps   | 1   |     | ns   |
|        |                         |                                                                   | 100Mbps  | 1   |     | ns   |
|        |                         |                                                                   | 1000Mbps | 1   |     | ns   |
| RGMII5 | $t_{h(rxcV-rdV)}$       | Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC transition   | 10Mbps   | 1   |     | ns   |
|        |                         |                                                                   | 100Mbps  | 1   |     | ns   |
|        |                         |                                                                   | 1000Mbps | 1   |     | ns   |
|        | $t_{h(rxcV-rx\_ctlV)}$  | Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC transition    | 10Mbps   | 1   |     | ns   |
|        |                         |                                                                   | 100Mbps  | 1   |     | ns   |
|        |                         |                                                                   | 1000Mbps | 1   |     | ns   |



- A. RGMII\_RXC must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. RGMII\_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII\_RXC and data bits 7-4 on the falling edge of RGMII\_RXC. Similarly, RGMII\_RXCTL carries RXDV on rising edge of RGMII\_RXC and RXERR on falling edge of RGMII\_RXC.

**Figure 6-39. CPSW2G Receive Interface Timing, RGMII Operation**

[Section 6.10.5.2.3.3](#), [Section 6.10.5.2.3.4](#) present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

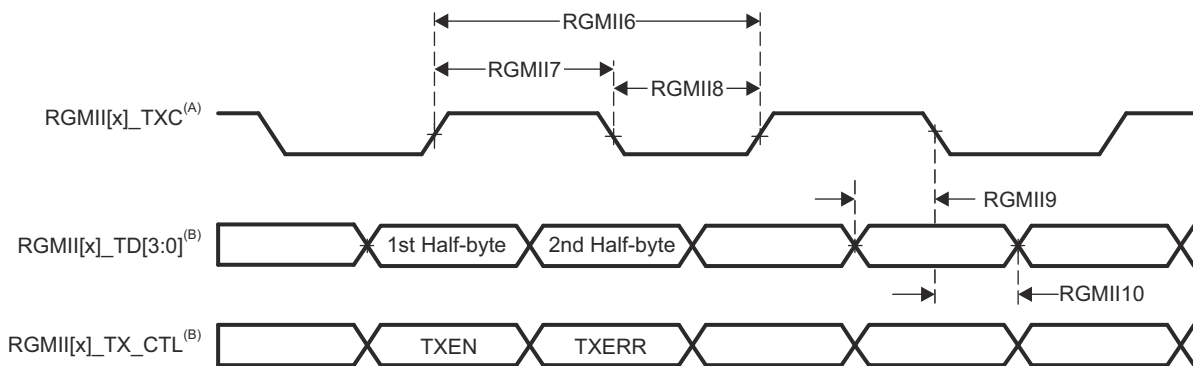
#### 6.10.5.2.3.3 CPSW2G RGMII[x]\_TXC Switching Characteristics – RGMII Mode

| NO.    | PARAMETER    |                                   | MODE     | MIN | MAX | UNIT |
|--------|--------------|-----------------------------------|----------|-----|-----|------|
| RGMII6 | $t_{c(tc)}$  | Cycle time, RGMII[x]_TXC          | 10Mbps   | 360 | 440 | ns   |
|        |              |                                   | 100Mbps  | 36  | 44  | ns   |
|        |              |                                   | 1000Mbps | 7.2 | 8.8 | ns   |
| RGMII7 | $t_{w(tcH)}$ | Pulse duration, RGMII[x]_TXC high | 10Mbps   | 160 | 240 | ns   |
|        |              |                                   | 100Mbps  | 16  | 24  | ns   |
|        |              |                                   | 1000Mbps | 3.6 | 4.4 | ns   |
| RGMII8 | $t_{w(tcL)}$ | Pulse duration, RGMII[x]_TXC low  | 10Mbps   | 160 | 240 | ns   |
|        |              |                                   | 100Mbps  | 16  | 24  | ns   |
|        |              |                                   | 1000Mbps | 3.6 | 4.4 | ns   |

#### 6.10.5.2.3.4 RGMII[x]\_TD[3:0], and RGMII[x]\_TX\_CTL Switching Characteristics – RGMII Mode

see Figure 6-40

| NO.     | PARAMETER               |                                                                        | MODE     | MIN | MAX | UNIT |
|---------|-------------------------|------------------------------------------------------------------------|----------|-----|-----|------|
| RGMII9  | $t_{osu(tdV-txcV)}$     | Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC transition   | 10Mbps   | 1.2 |     | ns   |
|         |                         |                                                                        | 100Mbps  | 1.2 |     | ns   |
|         |                         |                                                                        | 1000Mbps | 1.2 |     | ns   |
|         | $t_{osu(tx_cIIV-txcV)}$ | Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC transition    | 10Mbps   | 1.2 |     | ns   |
|         |                         |                                                                        | 100Mbps  | 1.2 |     | ns   |
|         |                         |                                                                        | 1000Mbps | 1.2 |     | ns   |
| RGMII10 | $t_{oh(tdV-txcV)}$      | Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC transition | 10Mbps   | 1.2 |     | ns   |
|         |                         |                                                                        | 100Mbps  | 1.2 |     | ns   |
|         |                         |                                                                        | 1000Mbps | 1.2 |     | ns   |
|         | $t_{oh(tx_cIIV-txcV)}$  | Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC transition  | 10Mbps   | 1.2 |     | ns   |
|         |                         |                                                                        | 100Mbps  | 1.2 |     | ns   |
|         |                         |                                                                        | 1000Mbps | 1.2 |     | ns   |



- A. TxC is delayed internally before being driven to the RGMII[x]\_TxC pin. This internal delay is always enabled.
- B. Data and control information is received using both edges of the clocks. RGMII\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII\_TxC and data bits 7-4 on the falling edge of RGMII\_TxC. Similarly, RGMII\_TX\_CTL carries TXDV on rising edge of RGMII\_TxC and RTXERR on falling edge of RGMII\_TxC.

**Figure 6-40. CPSW2G Transmit Interface Timing RGMII Mode**

### 6.10.5.3 CSI-2

#### Note

For more information, see the Camera Streaming Interface Receiver (CSI\_RX\_IF) chapter in the device TRM.

The CSI\_RX\_IF deals with the processing of the pixel data coming from an external image sensor and data from memory. It is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture.

The CSI\_RX\_IF has a primary serial interface (CSI-2 port) compliant with the MIPI D-PHY RX specification v1.2 and the MIPI CSI-2 specification v1.3, with 4 differential data lanes plus 1 differential clock lane in synchronous mode, double data rate. Refer to the specification for timing details.

- 2.5 Gbps (1.25 GHz) for each lane.

### 6.10.5.4 DDRSS

For more details about features and additional description information on the device LPDDR4 Memory Interfaces, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

The device has dedicated interface to LPDDR4. It supports JEDEC JESD209-4B standard compliant LPDDR4 SDRAM devices with the following features:

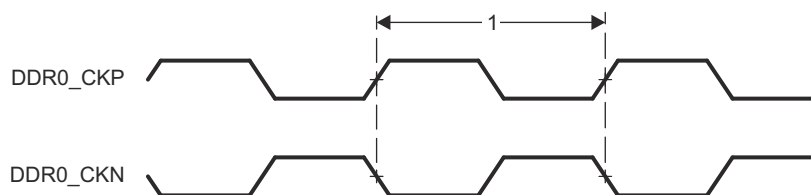
- 32-bit data path to external SDRAM memory
- Memory device capacity: Up to 8GB address space available over two chip selects (4GB per rank)
- No support for byte mode LPDDR4 memories, or memories with more than 17 row address bits

[Table 6-31](#) and [Figure 6-41](#) present switching characteristics for DDRSS.

**Table 6-31. Switching Characteristics for DDRSS**

| NO. | PARAMETER                                                    | DDR TYPE | MIN                | MAX   | UNIT |
|-----|--------------------------------------------------------------|----------|--------------------|-------|------|
| 1   | $t_{C(DDR\_CKP/DDR\_CKN)}$ Cycle time, DDR0_CKP and DDR0_CKN | LPDDR4   | 0.468 <sup>1</sup> | 3.003 | ns   |

1. Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. TI strongly recommends all designs to follow the TI LPDDR4 EVM PCB layout exactly in every detail (routing, spacing, vias/backdrill, PCB material, etc.) in order to achieve the full specified clock frequency. Refer to the Jacinto 7 DDR Board Design and Layout Guidelines for details.



**Figure 6-41. DDRSS Memory Interface Clock Timing**

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

### 6.10.5.5 DSS

For more details about features and additional description information on the device Display Subsystem – Video Output Ports, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

[Table 6-32](#) represents DPI timing conditions.

**Table 6-32. DPI Timing Conditions**

| PARAMETER               | MIN  | MAX  | UNIT |
|-------------------------|------|------|------|
| <b>INPUT CONDITIONS</b> |      |      |      |
| $SR_i$ Input slew rate  | 1.44 | 26.4 | V/ns |

**Table 6-32. DPI Timing Conditions (continued)**

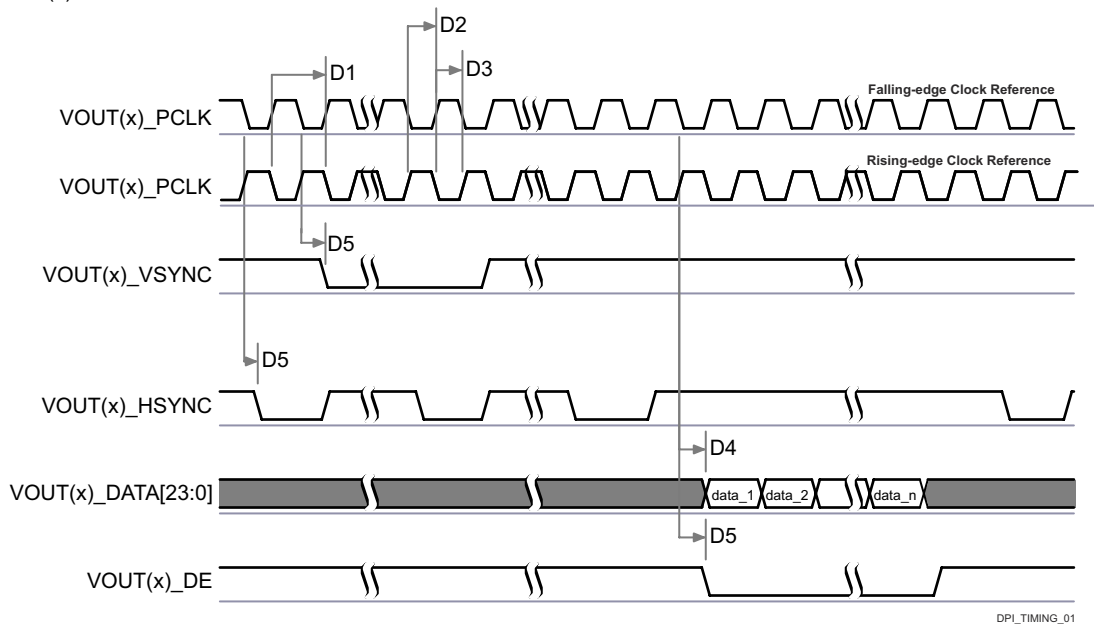
| PARAMETER                            |                                              | MIN | MAX | UNIT |
|--------------------------------------|----------------------------------------------|-----|-----|------|
| <b>OUTPUT CONDITIONS</b>             |                                              |     |     |      |
| $C_L$                                | Output load capacitance                      | 1.5 | 5   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |                                              |     |     |      |
| $t_d$ (Trace Mismatch Delay)         | Propagation delay mismatch across all traces |     | 100 | ps   |

Table 6-33, Table 6-34, Figure 6-42 and Figure 6-43 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-33. DPI Video Output Switching Characteristics**

| NO.(2) | PARAMETER            |                                                                                                              | MIN                    | MAX  | UNIT |
|--------|----------------------|--------------------------------------------------------------------------------------------------------------|------------------------|------|------|
| D1     | $t_{c(pclk)}$        | Cycle time, VOUT(x)_PCLK                                                                                     | 6.06                   |      | ns   |
| D2     | $t_{w(pclkL)}$       | Pulse duration, VOUT(x)_PCLK low                                                                             | $0.475 \times P^{(1)}$ |      | ns   |
| D3     | $t_{w(pclkH)}$       | Pulse duration, VOUT(x)_PCLK high                                                                            | $0.475 \times P^{(1)}$ |      | ns   |
| D4     | $t_{d(pclkV-dataV)}$ | Delay time, VOUT(x)_PCLK transition to VOUT(x)_DATA[23:0] transition                                         | -0.68                  | 1.78 | ns   |
| D5     | $t_{d(pclkV-ctrlL)}$ | Delay time, VOUT(x)_PCLK transition to control signals VOUT(x)_VSYNC, VOUT(x)_HSYNC, VOUT(x)_DE falling edge | -0.68                  | 1.78 | ns   |

- (1) P = output VOUT(x)\_PCLK period in ns.  
(2) x in VOUT(x) = 1 or 2



- A. The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.  
B. The polarity and the pulse width of VOUT(x)\_HSYNC and VOUT(x)\_VSYNC are programmable, refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.  
C. The VOUT(x)\_PCLK frequency can be configured, refer to *Display Subsystem* section in *Peripherals* chapter in the device TRM.  
D. x in VOUT(x) = 1 or 2.

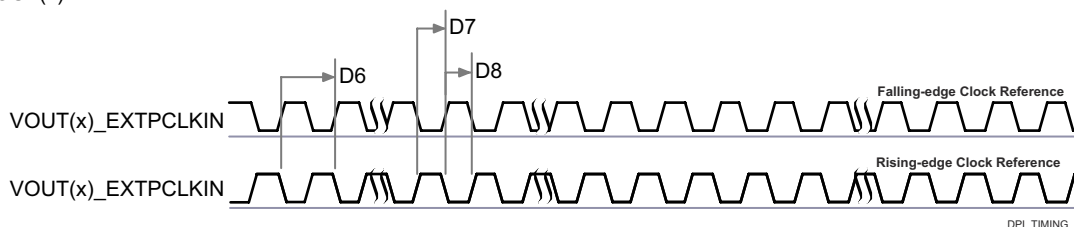
**Figure 6-42. DPI Video Output**

**Table 6-34. DPI External Pixel Clock Timing Requirements**

| NO.(2) |                     |                                        | MIN                   | MAX | UNIT |
|--------|---------------------|----------------------------------------|-----------------------|-----|------|
| D6     | $t_{c(extpclkin)}$  | Cycle time, VOUT(x)_EXTPCLKIN          | 6.06                  |     | ns   |
| D7     | $t_{w(extpclkinL)}$ | Pulse duration, VOUT(x)_EXTPCLKIN low  | $0.45 \times P^{(1)}$ |     | ns   |
| D8     | $t_{w(extpclkinH)}$ | Pulse duration, VOUT(x)_EXTPCLKIN high | $0.45 \times P^{(1)}$ |     | ns   |

(1) P = output VOUT(x)\_PCLK period in ns.

(2) x in VOUT(x) = 1 or 2

**Figure 6-43. DPI External Pixel Clock Input**

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter in the device TRM.

**6.10.5.6 eCAP**

The supported features by the device ECAP are:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt capabilities on any of the four capture events
- Input capture signal pre-scaling (from 1 to 16)
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or difference mode time-stamp capture)

Table 6-35 represents ECAP timing conditions.

**Table 6-35. ECAP Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>i</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

Section 6.10.5.6.1 and Section 6.10.5.6.2 present timing and switching characteristics for eCAP (see Figure 6-44 and Figure 6-45).

**6.10.5.6.1 Timing Requirements for eCAP**

| NO.  | PARAMETER    | DESCRIPTION                        | MIN            | MAX | UNIT |
|------|--------------|------------------------------------|----------------|-----|------|
| CAP1 | $t_{w(cap)}$ | Pulse duration, CAP (asynchronous) | $2 + 2P^{(1)}$ |     | ns   |

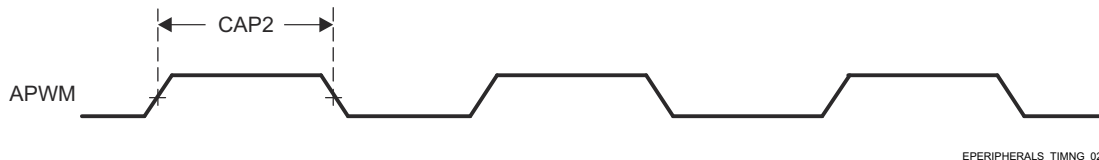
(1) P = sysclk

**Figure 6-44. eCAP Input Timings**

#### 6.10.5.6.2 Switching Characteristics for eCAP

| NO.  | PARAMETER     | DESCRIPTION          | MIN             | MAX | UNIT |
|------|---------------|----------------------|-----------------|-----|------|
| CAP2 | $t_{w(apwm)}$ | Pulse duration, APWM | $-2 + 2P^{(1)}$ |     | ns   |

(1)  $P = \text{sysclk}$



**Figure 6-45. eCAP Output Timings**

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.7 EPWM

The supported features by the device EPWM are:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs which can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

Table 6-36 represents EPWM timing conditions.

**Table 6-36. EPWM Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| $SR_i$                   | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| $C_L$                    | Output load capacitance | 2   | 7   | pF   |

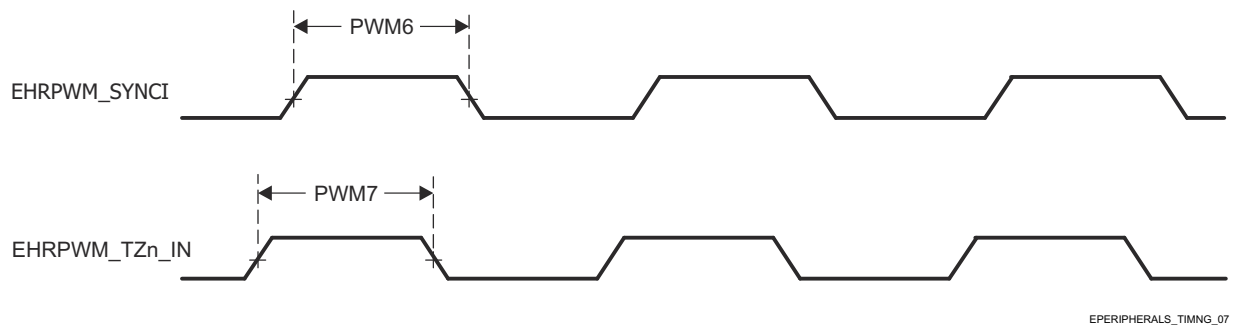
Section 6.10.5.7.2, Section 6.10.5.7.1 and present timing and switching characteristics for eHRPWM (see Figure 6-47, Figure 6-48, Figure 6-49, and Figure 6-46).

#### 6.10.5.7.1 Timing Requirements for eHRPWM

| NO.  | PARAMETER      | DESCRIPTION                  | MIN            | MAX | UNIT |
|------|----------------|------------------------------|----------------|-----|------|
| PWM6 | $t_{w(synci)}$ | Pulse duration, EHRPWM_SYNCI | $2 + 2P^{(1)}$ |     | ns   |

| NO.  | PARAMETER   | DESCRIPTION                       | MIN                   | MAX | UNIT |
|------|-------------|-----------------------------------|-----------------------|-----|------|
| PWM7 | $t_{w(tz)}$ | Pulse duration, EHRPWM_TZn_IN low | 2 + 3P <sup>(1)</sup> |     | ns   |

(1) P = sysclk



**Figure 6-46. ePWM\_SYNCI and ePWM\_TZn\_IN Output Timings**

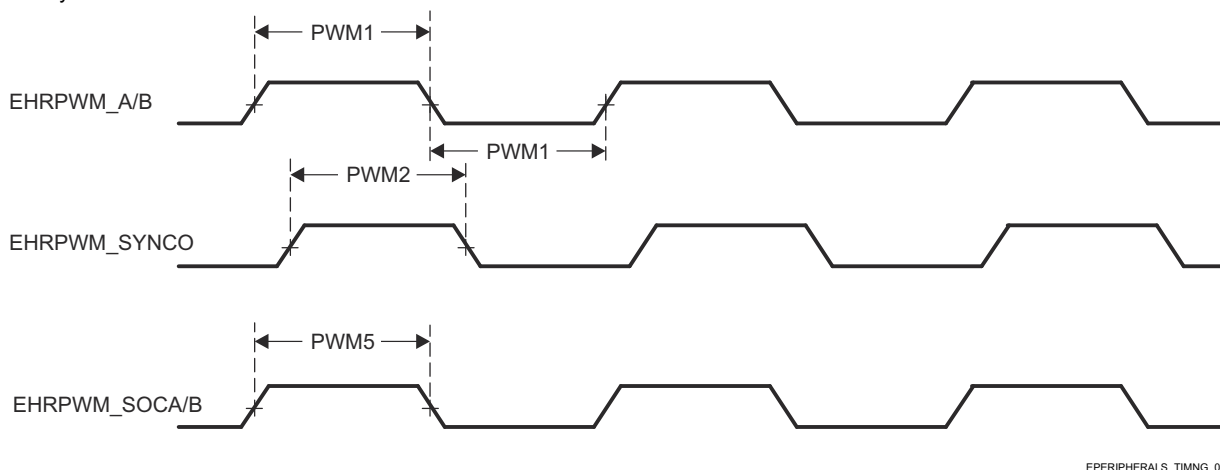
For more information, see *Camera Subsystem* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.7.2 Switching Characteristics for eHRPWM

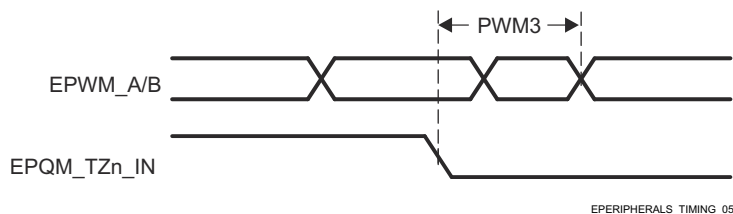
| NO.  | PARAMETER         | DESCRIPTION                                                | MIN                | MAX | UNIT |
|------|-------------------|------------------------------------------------------------|--------------------|-----|------|
| PWM1 | $t_{w(pwm)}$      | Pulse duration, EHRPWM_A/B, high or low                    | P-3 <sup>(1)</sup> |     | ns   |
| PWM2 | $t_{w(syncout)}$  | Pulse duration, EHRPWM_SYNCO                               | P-3 <sup>(1)</sup> |     | ns   |
| PWM3 | $t_{d(tzL-pwmV)}$ | Delay time, EHRPWM_TZn_IN falling edge to EHRPWM_A/B valid |                    | 11  | ns   |
| PWM4 | $t_{d(tzL-pwmZ)}$ | Delay time, EHRPWM_TZn_IN falling edge to EHRPWM_A/B Hi-Z  |                    | 11  | ns   |

| NO.  | PARAMETER    | DESCRIPTION                    | MIN                | MAX | UNIT |
|------|--------------|--------------------------------|--------------------|-----|------|
| PWM5 | $t_{w(soc)}$ | Pulse duration, EHRPWM_SOC/A/B | P-3 <sup>(1)</sup> |     | ns   |

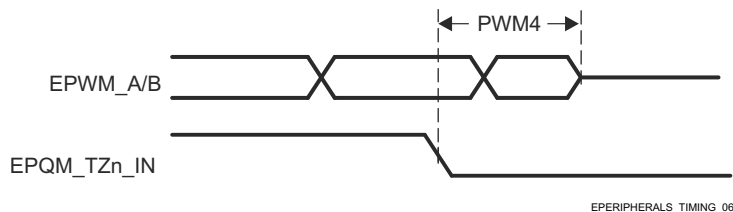
(1) P = sysclk



**Figure 6-47. EPWM\_A/B\_out, ePWM\_SYNCO, and ePWM\_SOC/A/B Input Timings**



**Figure 6-48. EPWM\_A/B and ePWM\_TZn\_IN Forced High/Low Input Timings**



**Figure 6-49. EPWM\_A/B and ePWM\_TZn\_IN Hi-Z Input Timings**

#### 6.10.5.8 eQEP

The supported features by the device eQEP are:

- Input Synchronization
- Three Stage/Six Stage Digital Noise Filter
- Quadrature Decoder Unit
- Position Counter and Control unit for position measurement
- Quadrature Edge Capture unit for low speed measurement
- Unit Time base for speed/frequency measurement
- Watchdog Timer for detecting stalls

Table 6-37 represents EQEP timing conditions.

**Table 6-37. EQEP Timing Conditions**

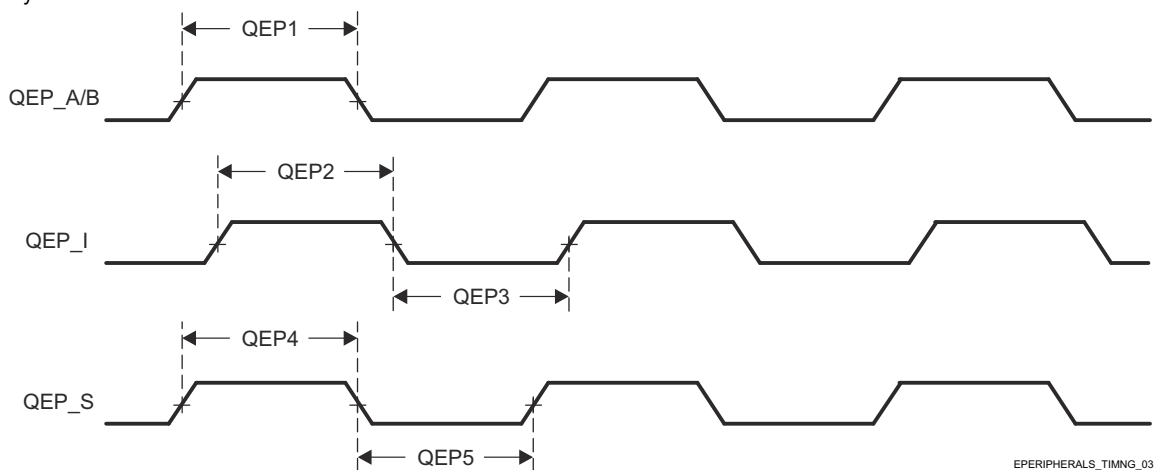
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

Section 6.10.5.8.1 and Section 6.10.5.8.2 present timing requirements and switching characteristics for eQEP (see Figure 6-50).

#### 6.10.5.8.1 Timing Requirements for eQEP

| NO.  |                |                            | MIN            | MAX | UNIT |
|------|----------------|----------------------------|----------------|-----|------|
| QEP1 | $t_{w(qep)}$   | Pulse duration, QEP_A/B    | $2 + 2P^{(1)}$ |     | ns   |
| QEP2 | $t_{w(qepiH)}$ | Pulse duration, QEP_I high | $2 + 2P^{(1)}$ |     | ns   |
| QEP3 | $t_{w(qepiL)}$ | Pulse duration, QEP_I low  | $2 + 2P^{(1)}$ |     | ns   |
| QEP4 | $t_{w(qepsH)}$ | Pulse duration, QEP_S high | $2 + 2P^{(1)}$ |     | ns   |
| QEP5 | $t_{w(qepsL)}$ | Pulse duration, QEP_S low  | $2 + 2P^{(1)}$ |     | ns   |

(1)  $P = \text{sysclk}$

**Figure 6-50. eQEP Input Timings**

#### 6.10.5.8.2 Switching Characteristics for eQEP

| NO.  |                   | PARAMETER                                       | MIN | MAX | UNIT |
|------|-------------------|-------------------------------------------------|-----|-----|------|
| QEP6 | $t_{d(QEP-CNTR)}$ | Delay time, external clock to counter increment |     | 24  | ns   |

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.9 GPIO

For more details about features and additional description information on the device GPIO, see the device-specific Technical Reference Manual (TRM) and the corresponding sections within [Signal Descriptions](#) of this data sheet.

[Table 6-38](#), [Section 6.10.5.9.1](#), and [Section 6.10.5.9.2](#) present timing conditions, requirements, and switching characteristics for GPIO.

**Table 6-38. GPIO Timing Conditions**

| PARAMETER         |                         | BUFFER TYPE | MIN | MAX  | UNIT |
|-------------------|-------------------------|-------------|-----|------|------|
| INPUT CONDITIONS  |                         |             |     |      |      |
| SR <sub>I</sub>   | Input slew rate         | LVC MOS     | 0.2 | 6.6  | V/ns |
|                   |                         | I2C OD FS   | 0.2 | 0.08 | V/ns |
| OUTPUT CONDITIONS |                         |             |     |      |      |
| C <sub>L</sub>    | Output load capacitance | LVC MOS     | 3   | 10   | pF   |
|                   |                         | I2C OD FS   | 3   | 100  | pF   |

#### 6.10.5.9.1 GPIO Timing Requirements

| NO.   |                         |                                   | BUFFER TYPE | MIN                     | MAX | UNIT |
|-------|-------------------------|-----------------------------------|-------------|-------------------------|-----|------|
| GPIO1 | t <sub>w(gpio_in)</sub> | Pulse width, GPIO <sub>n</sub> _x | 1.8 V       | 2P + 2.6 <sup>(1)</sup> |     | ns   |
|       |                         |                                   | 3.3 V       | 2P + 3.4 <sup>(1)</sup> |     | ns   |

(1) P = functional clock period in ns.

#### 6.10.5.9.2 GPIO Switching Characteristics

| NO.   | PARAMETER                |                                 | BUFFER TYPE    | MIN                          | MAX | UNIT |
|-------|--------------------------|---------------------------------|----------------|------------------------------|-----|------|
| GPIO3 | t <sub>w(GPIO_OUT)</sub> | Minimum Output Pulse Width      | LVC MOS        | –3.6 + 0.975P <sup>(1)</sup> |     | ns   |
| GPIO4 | t <sub>w(GPIO_OUT)</sub> | Minimum Output Pulse Width Low  | I2C Open Drain | 160                          |     | ns   |
| GPIO5 | t <sub>w(GPIO_OUT)</sub> | Minimum Output Pulse Width High | I2C Open Drain | 60                           |     | ns   |

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.10 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

[Table 6-39](#) represents GPMC timing conditions.

#### Note

The IO timings provided in this section are applicable for all combinations of signals for GPMC0. However, the timings are only valid for GPMC0 if signals within a single IOSET are used. The IOSETs are defined in the [GPMC0\\_IOSET](#), [GPMC0\\_IOSET](#) table.

**Table 6-39. GPMC Timing Conditions**

| PARAMETER                             | DESCRIPTION                            |                          | MIN  | MAX | UNIT |
|---------------------------------------|----------------------------------------|--------------------------|------|-----|------|
| Input Conditions                      |                                        |                          |      |     |      |
| SR <sub>I</sub>                       | Input slew rate                        |                          | 1.65 | 4   | V/ns |
| Output Conditions                     |                                        |                          |      |     |      |
| C <sub>L</sub>                        | Output load capacitance                |                          | 5    | 20  | pF   |
| PCB Connectivity Requirements         |                                        |                          |      |     |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace        | 133 MHz Synchronous Mode | 140  | 360 | ps   |
|                                       |                                        | All other modes          | 140  | 720 |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation mismatch across all traces |                          |      | 200 | ps   |

#### 6.10.5.10.1 GPMC and NOR Flash — Synchronous Mode

[Section 6.10.5.10.1.1](#) and [Section 6.10.5.10.1.2](#) assume testing over the recommended operating conditions and electrical characteristic conditions below (see [Figure 6-51](#) through [Figure 6-55](#)).

### 6.10.5.10.1.1 GPMC and NOR Flash Timing Requirements — Synchronous Mode

| NO. | PARAMETER                    | DESCRIPTION <sup>(2)</sup>                                                                 | MODE <sup>(3)</sup>                                            | MIN                    | MAX | MIN                    | MAX | UNIT |
|-----|------------------------------|--------------------------------------------------------------------------------------------|----------------------------------------------------------------|------------------------|-----|------------------------|-----|------|
|     |                              |                                                                                            |                                                                | 100 MHz <sup>(4)</sup> |     | 133 MHz <sup>(4)</sup> |     |      |
| F12 | t <sub>su</sub> (dV-clkH)    | Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high               | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.81                   |     | 1.11                   |     | ns   |
|     |                              |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.06                   |     |                        | ns  |      |
| F13 | t <sub>h</sub> (clkH-dV)     | Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high                 | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.78                   |     | 2.28                   |     | ns   |
|     |                              |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.78                   |     |                        | ns  |      |
| F21 | t <sub>su</sub> (waitV-clkH) | Setup time, input wait GPMC_WAIT[j] valid before output clock GPMC_CLK high <sup>(1)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.81                   |     | 1.11                   |     | ns   |
|     |                              |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.06                   |     |                        | ns  |      |
| F22 | t <sub>h</sub> (clkH-waitV)  | Hold time, input wait GPMC_WAIT[j] valid after output clock GPMC_CLK high <sup>(1)</sup>   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.78                   |     | 2.28                   |     | ns   |
|     |                              |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.78                   |     |                        | ns  |      |

(1) In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

(2) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.

(3) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency / (2 to 4)
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100 MHz
- For TIMEPARAGRANULARITY\_X1:
  - GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

(4) For 100 MHz:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = MAIN\_PLL2\_HSDIV1\_CLKOUT / 3

For 133 MHz:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = MAIN\_PLL0\_HSDIV3\_CLKOUT

### 6.10.5.10.1.2 GPMC and NOR Flash Switching Characteristics – Synchronous Mode

| NO. <sup>(2)</sup> | PARAMETER | DESCRIPTION                                   | MODE <sup>(19)</sup>                                         | MIN                     | MAX | MIN                     | MAX | UNIT |
|--------------------|-----------|-----------------------------------------------|--------------------------------------------------------------|-------------------------|-----|-------------------------|-----|------|
|                    |           |                                               |                                                              | 100 MHz <sup>(20)</sup> |     | 133 MHz <sup>(20)</sup> |     |      |
| F0                 | tc(clk)   | Period, output clock GPMC_CLK <sup>(18)</sup> | div_by_1_mode;<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 10                      |     | 7.52                    |     | ns   |

| NO. <sup>(2)</sup> | PARAMETER                      | DESCRIPTION                                                                                                                                                                  | MODE <sup>(19)</sup>                                                          | MIN                     | MAX                     | MIN                     | MAX                     | UNIT |
|--------------------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
|                    |                                |                                                                                                                                                                              |                                                                               | 100 MHz <sup>(20)</sup> |                         | 133 MHz <sup>(20)</sup> |                         |      |
| F1                 | t <sub>w</sub> (clkH)          | Typical pulse duration, output clock GPMC_CLK high                                                                                                                           | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | 0.475*P<br>(15)- 0.3    |                         | 0.475*P<br>(15)- 0.3    |                         | ns   |
| F1                 | t <sub>w</sub> (clkL)          | Typical pulse duration, output clock GPMC_CLK low                                                                                                                            | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | 0.475*P<br>(15)- 0.3    |                         | 0.475*P<br>(15)- 0.3    |                         | ns   |
| F2                 | t <sub>d</sub> (clkH-csnV)     | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS[n] transition <sup>(14)</sup>                                                                    | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | F <sup>(6)</sup> - 2.2  | F+3.75                  | F <sup>(6)</sup> - 2.2  | F <sup>(6)</sup> + 3.75 | ns   |
| F3                 | t <sub>d</sub> (clkH-CSn[i]V)  | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS[n] invalid <sup>(14)</sup>                                                                       | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | E <sup>(5)</sup> - 2.2  | E <sup>(5)</sup> + 3.75 | E <sup>(5)</sup> - 2.2  | E <sup>(5)</sup> + 3.75 | ns   |
| F4                 | t <sub>d</sub> (aV-clk)        | Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge                                                                                            | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | B <sup>(2)</sup> -2.3   | B <sup>(2)</sup> +4.5   | B <sup>(2)</sup> -2.3   | B <sup>(2)</sup> +4.5   | ns   |
| F5                 | t <sub>d</sub> (clkH-aIV)      | Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid                                                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3                    | 4.5                     | -2.3                    | 4.5                     | ns   |
| F6                 | t <sub>d</sub> (be[x]nV-clk)   | Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge                    | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | B <sup>(2)</sup> -2.3   | B <sup>(2)</sup> +1.9   | B <sup>(2)</sup> -2.3   | B <sup>(2)</sup> +1.9   | ns   |
| F7                 | t <sub>d</sub> (clkH-be[x]nIV) | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid <sup>(11)</sup> | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +1.9   | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +1.9   | ns   |
| F7                 | t <sub>d</sub> (clkL-be[x]nIV) | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(12)</sup>                                                                                        | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +1.9   | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +1.9   | ns   |
| F7                 | t <sub>d</sub> (clkL-be[x]nIV) | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(13)</sup>                                                                                        | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +1.9   | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +1.9   | ns   |
| F8                 | t <sub>d</sub> (clkH-advn)     | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition                                                      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | G <sup>(7)</sup> -2.3   | G <sup>(7)</sup> +4.5   | G <sup>(7)</sup> -2.3   | G <sup>(7)</sup> +4.5   | ns   |
| F9                 | t <sub>d</sub> (clkH-advnIV)   | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay  | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +4.5   | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +4.5   | ns   |
| F10                | t <sub>d</sub> (clkH-oen)      | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition                                                                                       | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | H <sup>(8)</sup> -2.3   | H <sup>(8)</sup> +3.5   | H <sup>(8)</sup> -2.3   | H <sup>(8)</sup> +3.5   | ns   |

| NO. <sup>(2)</sup> | PARAMETER                   | DESCRIPTION                                                                                                                                 | MODE <sup>(19)</sup>                                                          | MIN                     | MAX                    | MIN                     | MAX                    | UNIT |
|--------------------|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-------------------------|------------------------|-------------------------|------------------------|------|
|                    |                             |                                                                                                                                             |                                                                               | 100 MHz <sup>(20)</sup> |                        | 133 MHz <sup>(20)</sup> |                        |      |
| F11                | $t_{d(\text{clkH-oenIV})}$  | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_Ren invalid                                                         | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | E <sup>(8)</sup> -2.3   | E <sup>(8)</sup> +3.5  | E <sup>(8)</sup> -2.3   | E <sup>(8)</sup> +3.5  | ns   |
| F14                | $t_{d(\text{clkH-wen})}$    | Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition                                                    | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | I <sup>(9)</sup> -2.3   | I <sup>(9)</sup> +4.5  | I <sup>(9)</sup> -2.3   | I <sup>(9)</sup> +4.5  | ns   |
| F15                | $t_{d(\text{clkH-do})}$     | Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition <sup>(11)</sup>                                       | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | ns   |
| F15                | $t_{d(\text{clkL-do})}$     | Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(12)</sup>                                                      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | ns   |
| F15                | $t_{d(\text{clkL-do})}$     | Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(13)</sup>                                                      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | ns   |
| F17                | $t_{d(\text{clkH-be[x]n})}$ | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition <sup>(11)</sup> | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | ns   |
| F17                | $t_{d(\text{clkL-be[x]n})}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(12)</sup>                                                    | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | ns   |
| F17                | $t_{d(\text{clkL-be[x]n})}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(13)</sup>                                                    | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | ns   |
| F18                | $t_{w(\text{csnV})}$        | Pulse duration, output chip select GPMC_CSn[i] low <sup>(14)</sup>                                                                          | Read                                                                          | A <sup>(1)</sup>        |                        | A <sup>(1)</sup>        |                        | ns   |
|                    |                             |                                                                                                                                             | Write                                                                         | A <sup>(1)</sup>        |                        | A <sup>(1)</sup>        |                        | ns   |
| F19                | $t_{w(\text{be[x]nV})}$     | Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low                     | Read                                                                          | C <sup>(3)</sup>        |                        | C <sup>(3)</sup>        |                        | ns   |
|                    |                             |                                                                                                                                             | Write                                                                         | C <sup>(3)</sup>        |                        | C <sup>(3)</sup>        |                        | ns   |
| F20                | $t_{w(\text{advnV})}$       | Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low                                                             | Read                                                                          | K <sup>(16)</sup>       |                        | K <sup>(16)</sup>       |                        | ns   |
|                    |                             |                                                                                                                                             | Write                                                                         | K <sup>(16)</sup>       |                        | K <sup>(16)</sup>       |                        | ns   |

- (1) For single read:  $A = (\text{CSRdOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst read:  $A = (\text{CSRdOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst write:  $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 With n being the page burst access number.
- (2)  $B = \text{ClkActivationTime} \times \text{GPMC\_FCLK}^{(17)}$
- (3) For single read:  $C = \text{RdCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst read:  $C = (\text{RdCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst write:  $C = (\text{WrCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 With n being the page burst access number.
- (4) For single read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst write:  $D = (\text{WrCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$
- (5) For single read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst write:  $E = (\text{CSWrOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$
- (6) For csn falling edge (CS activated):

- Case GPMCFCLKDIVIDER = 0:
  - $F = 0.5 \times \text{CSEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $F = 0.5 \times \text{CSEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and CSONTime are odd) or (ClkActivationTime and CSONTime are even)
  - $F = (1 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $F = 0.5 \times \text{CSEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((CSONTime - ClkActivationTime) is a multiple of 3)
  - $F = (1 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((CSONTime - ClkActivationTime - 1) is a multiple of 3)
  - $F = (2 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((CSONTime - ClkActivationTime - 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOnTime - ClkActivationTime) is a multiple of 3)

- $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOnTime} - \text{ClkActivationTime} - 1))$  is a multiple of 3
- $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOnTime} - \text{ClkActivationTime} - 2))$  is a multiple of 3

For OE rising edge (OE deactivated):

- Case GPMCFCCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ClkActivationTime}$  and  $\text{OEOffTime}$  are odd) or  $((\text{ClkActivationTime}$  and  $\text{OEOffTime}$  are even)
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOffTime} - \text{ClkActivationTime}))$  is a multiple of 3
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOffTime} - \text{ClkActivationTime} - 1))$  is a multiple of 3
  - $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOffTime} - \text{ClkActivationTime} - 2))$  is a multiple of 3

(9) For WE falling edge (WE activated):

- Case GPMCFCCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCCLKDIVIDER = 1:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ClkActivationTime}$  and  $\text{WEOnTime}$  are odd) or  $((\text{ClkActivationTime}$  and  $\text{WEOnTime}$  are even)
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCCLKDIVIDER = 2:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{WEOnTime} - \text{ClkActivationTime}))$  is a multiple of 3
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{WEOnTime} - \text{ClkActivationTime} - 1))$  is a multiple of 3
  - $I = (2 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{WEOnTime} - \text{ClkActivationTime} - 2))$  is a multiple of 3

For WE rising edge (WE deactivated):

- Case GPMCFCCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCCLKDIVIDER = 1:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ClkActivationTime}$  and  $\text{WEOffTime}$  are odd) or  $((\text{ClkActivationTime}$  and  $\text{WEOffTime}$  are even)
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCCLKDIVIDER = 2:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{WEOffTime} - \text{ClkActivationTime}))$  is a multiple of 3
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 1))$  is a multiple of 3
  - $I = (2 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 2))$  is a multiple of 3

(10)  $J = \text{GPMC\_FCLK}^{(17)}$

(11) First transfer only for CLK DIV 1 mode.

(12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.

(13) Half cycle of GPMC\_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC\_CLKOUT divide down from GPMC\_FCLK.

(14) In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2, or 3. In GPMC\_WAIT[j], *j* is equal to 0, 1, 2, or 3.

(15)  $P = \text{GPMC\_CLK}$  period in ns

(16) For read:  $K = (\text{ADVrdOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$

For write:  $K = (\text{ADVWrOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$

(17) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

(18) Related to the GPMC\_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC\_CONFIG1\_i configuration register bit field GPMCFCCLKDIVIDER.

(19) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i register: GPMCFCCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency
- CTRLMMR\_GPMC\_CLKSEL[1:0] CLK\_SEL = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100 MHz
- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOffTIME, WEONTIME, WEOffTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

For no extra\_delay:

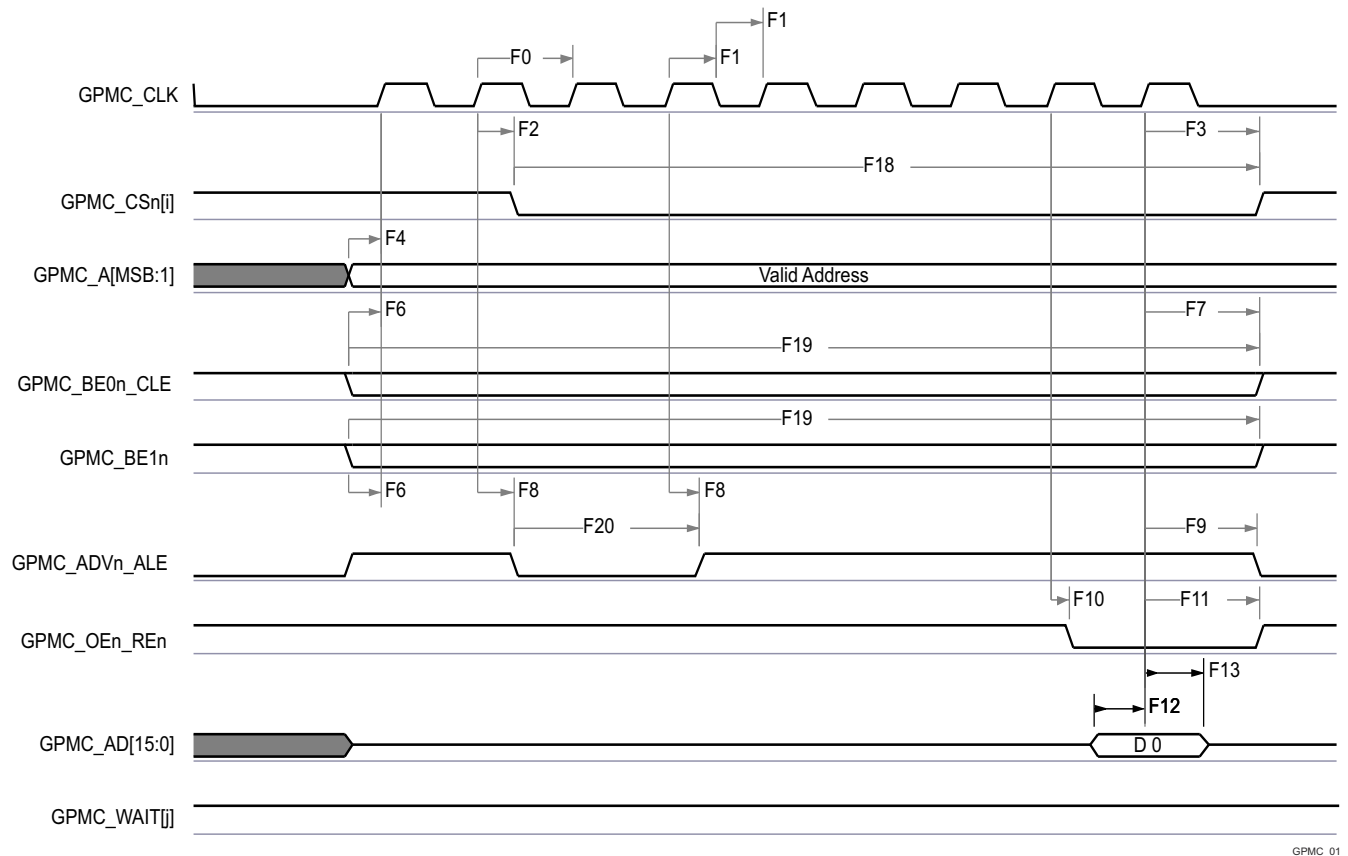
- GPMC\_CONFIG2\_i Register: CSEXTRADELAY = 0h = CSn Timing control signal is not delayed
- GPMC\_CONFIG4\_i Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC\_CONFIG4\_i Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC\_CONFIG3\_i Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed

(20) For 100 MHz:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = MAIN\_PLL2\_HSDIV1\_CLKOUT / 3

For 133 MHz:

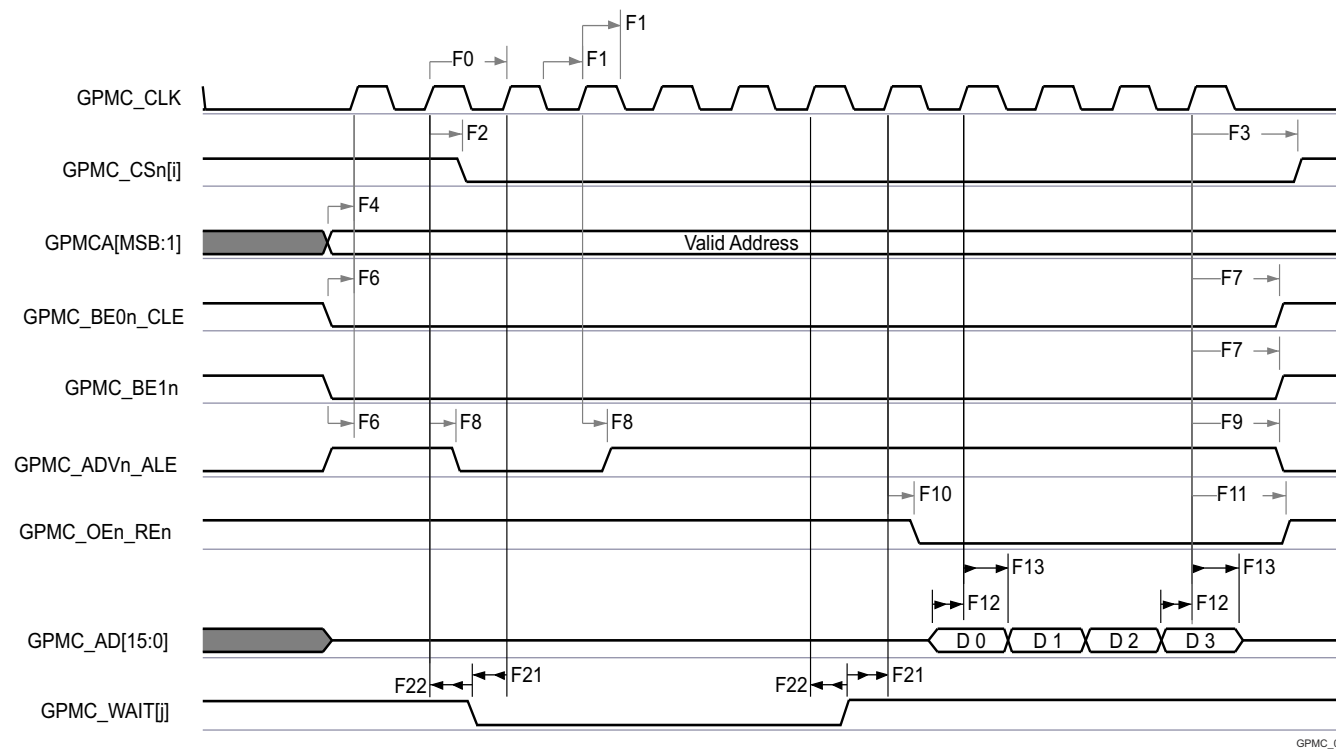
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = MAIN\_PLL0\_HSDIV3\_CLKOUT



GPMC\_01

- A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3.  
B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

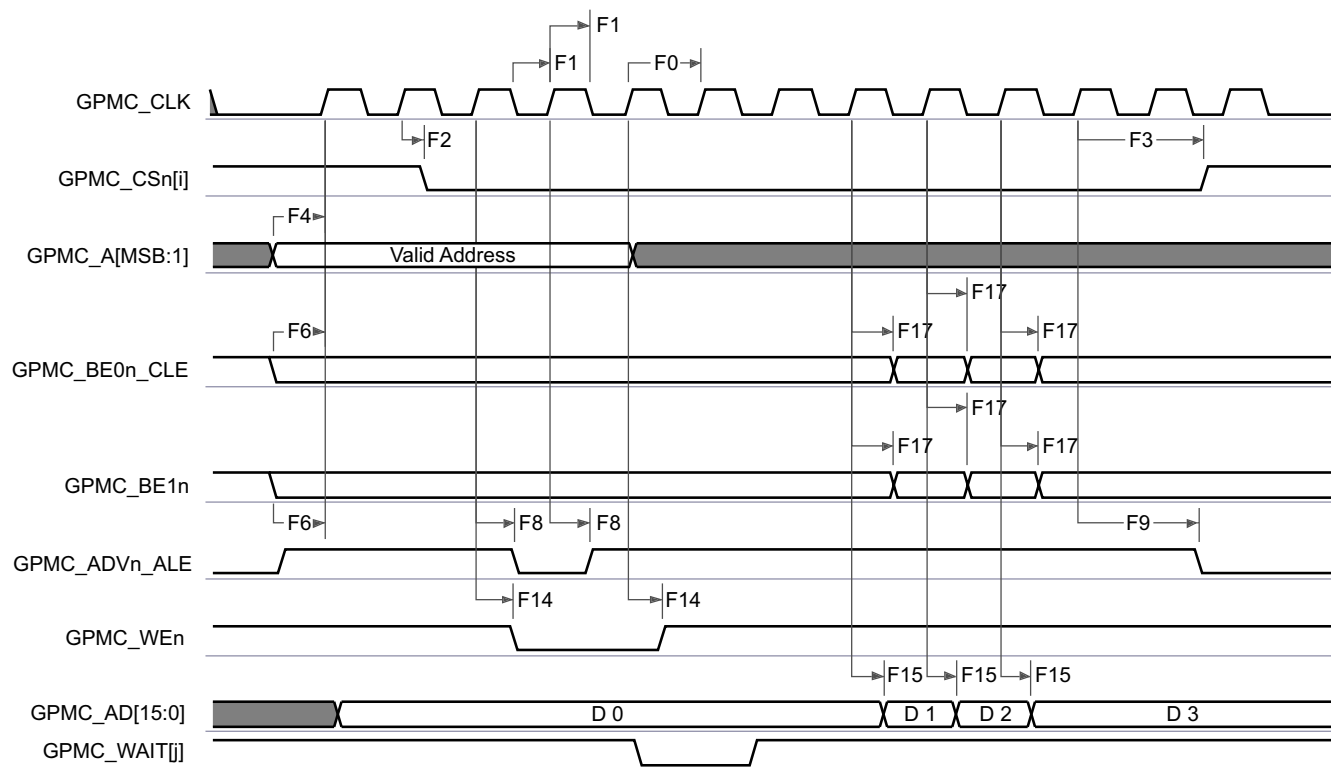
**Figure 6-51. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)**



GPMC\_02

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.  
 B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

**Figure 6-52. GPMC and NOR Flash — Synchronous Burst Read — 4x16-bit (GPMCCLKDIVIDER = 0)**

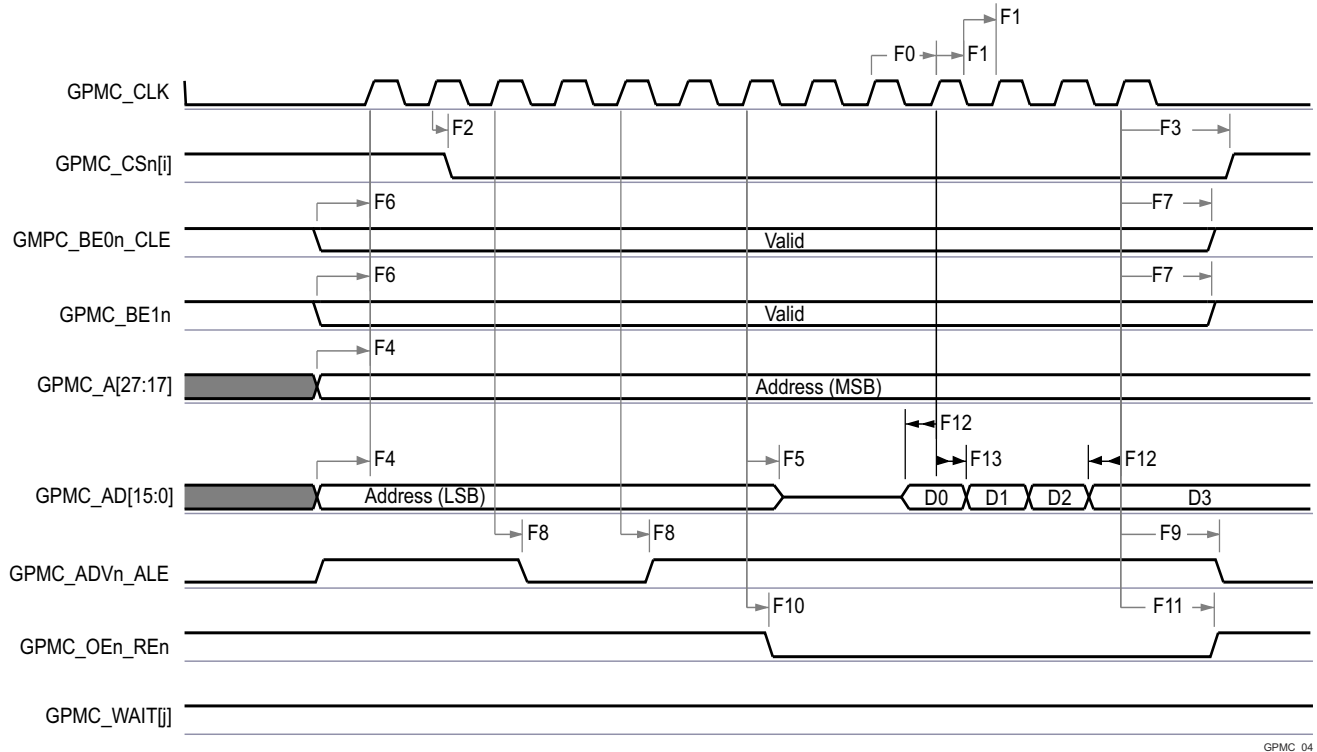


GPMC\_03

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

**Figure 6-53. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)**

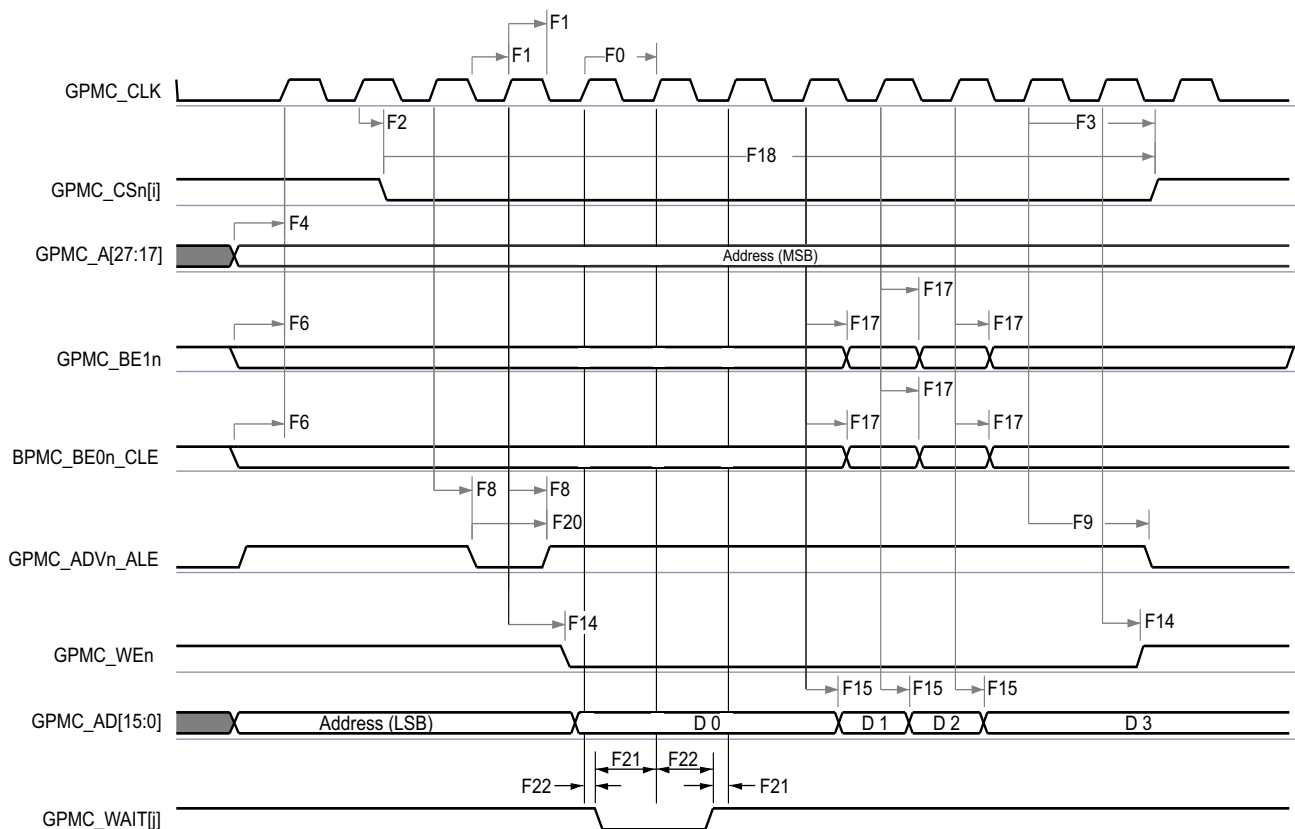


GPMC\_04

A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

**Figure 6-54. GPMC and Multiplexed NOR Flash — Synchronous Burst Read**



GPMC\_05

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.  
 B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

**Figure 6-55. GPMC and Multiplexed NOR Flash — Synchronous Burst Write**

#### 6.10.5.10.2 GPMC and NOR Flash — Asynchronous Mode

Section 6.10.5.10.2.1 and Section 6.10.5.10.2.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-56 through Figure 6-61).

##### 6.10.5.10.2.1 GPMC and NOR Flash Timing Requirements – Asynchronous Mode

| NO.                 |                      |                                       | MODE <sup>(7)</sup>                                             | MIN | MAX              | UNIT |
|---------------------|----------------------|---------------------------------------|-----------------------------------------------------------------|-----|------------------|------|
| FA5 <sup>(1)</sup>  | $t_{acc(d)}$         | Data access time                      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X<br>1 |     | H <sup>(5)</sup> | ns   |
| FA20 <sup>(2)</sup> | $t_{acc1-pgmode(d)}$ | Page mode successive data access time | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X<br>1 |     | P <sup>(4)</sup> | ns   |
| FA21 <sup>(3)</sup> | $t_{acc2-pgmode(d)}$ | Page mode first data access time      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X<br>1 |     | H <sup>(5)</sup> | ns   |

- (1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
- (2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.

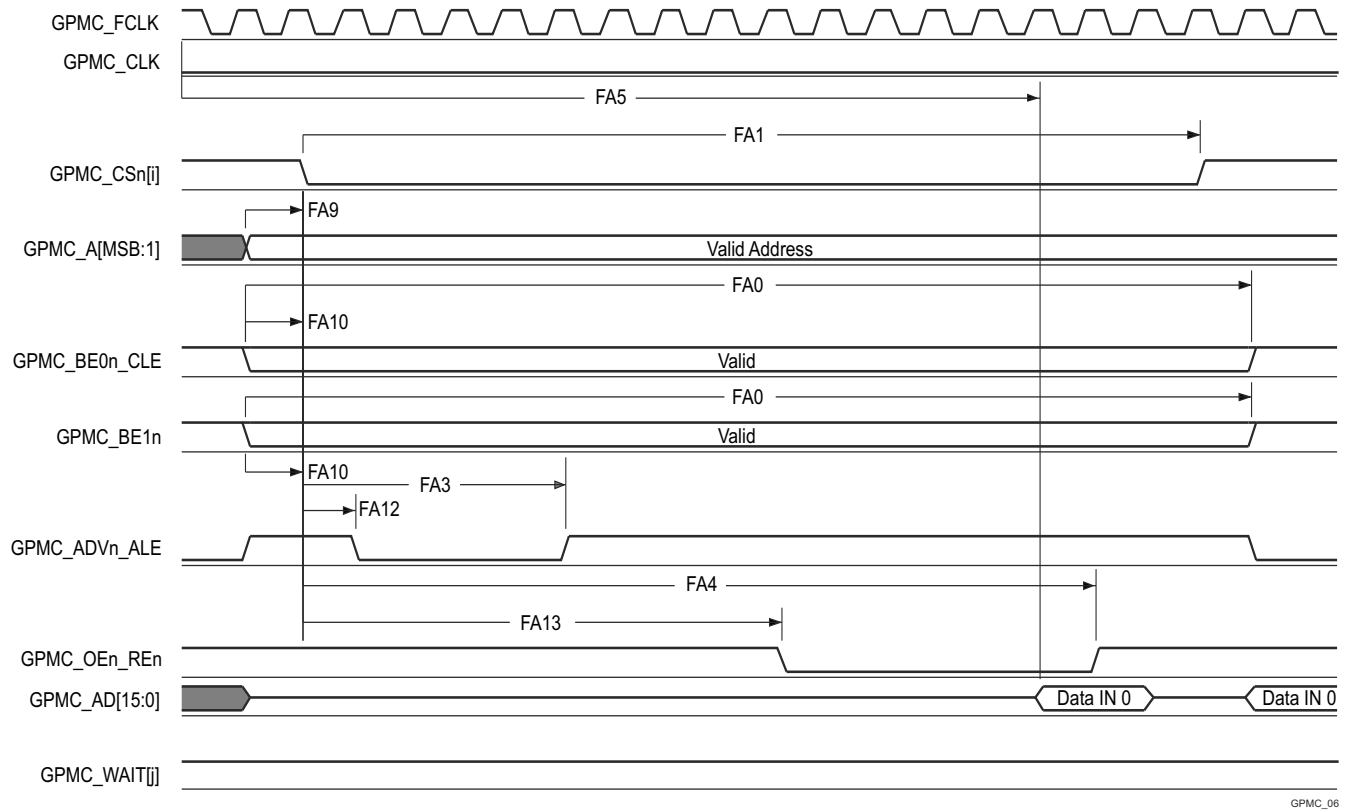
- (3) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.
- (4)  $P = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(6)}$
- (5)  $H = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(6)}$
- (6) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (7) For div\_by\_1\_mode:
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
    - GPMC\_CLK frequency = GPMC\_FCLK frequency
  - CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz
  - GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

#### 6.10.5.10.2.2 GPMC and NOR Flash Switching Characteristics – Asynchronous Mode

| NO.  | PARAMETER                           | DESCRIPTION                                                                                                                                                                                     | MODE <sup>(15)</sup>                                       | MIN                                             | MAX                      | UNIT |
|------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------|--------------------------|------|
|      |                                     |                                                                                                                                                                                                 |                                                            | 133 MHz <sup>(16)</sup>                         |                          |      |
| FA0  | $t_{w(\text{be}[x]nV)}$             | Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time                                                                  | Read                                                       | N <sup>(12)</sup>                               |                          | ns   |
|      |                                     |                                                                                                                                                                                                 | Write                                                      | N <sup>(12)</sup>                               |                          |      |
| FA1  | $t_{w(\text{csn}V)}$                | Pulse duration, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> low                                                                                                            | Read                                                       | A <sup>(1)</sup>                                |                          | ns   |
|      |                                     |                                                                                                                                                                                                 | Write                                                      | A <sup>(1)</sup>                                |                          |      |
| FA3  | $t_{d(\text{csn}V\text{-}advnIV)}$  | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADV <i>n</i> _ALE invalid                              | Read                                                       | B <sup>(2)</sup> - 2.55                         | B <sup>(2)</sup> + 2.65  | ns   |
|      |                                     |                                                                                                                                                                                                 | Write                                                      | B <sup>(2)</sup> - 2.55                         | B <sup>(2)</sup> + 2.65  |      |
| FA4  | $t_{d(\text{csn}V\text{-}oenIV)}$   | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output enable GPMC_OEn_RE <i>n</i> invalid (Single read)                                                  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | C <sup>(3)</sup> - 2.55 C <sup>(3)</sup> + 2.65 |                          | ns   |
| FA9  | $t_{d(aV\text{-}csnV)}$             | Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid                                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J <sup>(9)</sup> - 2.55 J <sup>(9)</sup> + 2.65 |                          | ns   |
| FA10 | $t_{d(\text{be}[x]nV\text{-}csnV)}$ | Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J <sup>(9)</sup> - 2.55 J <sup>(9)</sup> + 2.65 |                          | ns   |
| FA12 | $t_{d(\text{csn}V\text{-}advnV)}$   | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADV <i>n</i> _ALE valid                                | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | K <sup>(10)</sup> - 2.55                        | K <sup>(10)</sup> + 2.65 | ns   |
| FA13 | $t_{d(\text{csn}V\text{-}oenV)}$    | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output enable GPMC_OEn_RE <i>n</i> valid                                                                  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | L <sup>(11)</sup> - 2.55                        | L <sup>(11)</sup> + 2.65 | ns   |
| FA16 | $t_{w(aIV)}$                        | Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses                                                                                                 | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | G <sup>(7)</sup>                                |                          | ns   |
| FA18 | $t_{d(\text{csn}V\text{-}oenIV)}$   | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output enable GPMC_OEn_RE <i>n</i> invalid (Burst read)                                                   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | I <sup>(8)</sup> - 2.55                         | I <sup>(8)</sup> + 2.65  | ns   |
| FA20 | $t_{w(aV)}$                         | Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses                                                                                                                  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | D <sup>(4)</sup>                                |                          | ns   |

| NO.  | PARAMETER                  | DESCRIPTION                                                                                                                | MODE <sup>(15)</sup>                                       | MIN                     | MAX                     | UNIT |
|------|----------------------------|----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------|-------------------------|------|
|      |                            |                                                                                                                            |                                                            | 133 MHz <sup>(16)</sup> |                         |      |
| FA25 | t <sub>d(csnV-wenV)</sub>  | Delay time, output chip select GPMC_CS <i>n</i> [ <i>i</i> ] <sup>(13)</sup> valid to output write enable GPMC_WEn valid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | E <sup>(5)</sup> - 2.55 | E <sup>(5)</sup> + 2.65 | ns   |
| FA27 | t <sub>d(csnV-wenIV)</sub> | Delay time, output chip select GPMC_CS <i>n</i> [ <i>i</i> ] <sup>(13)</sup> valid to output write enable GPMC_WEn invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | F <sup>(6)</sup> - 2.55 | F <sup>(6)</sup> + 2.65 | ns   |
| FA28 | t <sub>d(wenV-dV)</sub>    | Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                         | 2.65                    | ns   |
| FA29 | t <sub>d(dV-csnV)</sub>    | Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CS <i>n</i> [ <i>i</i> ] <sup>(13)</sup> valid      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J <sup>(9)</sup> - 2.55 | J <sup>(9)</sup> + 2.65 | ns   |
| FA37 | t <sub>d(oenV-alV)</sub>   | Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end                                     | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                         | 2.65                    | ns   |

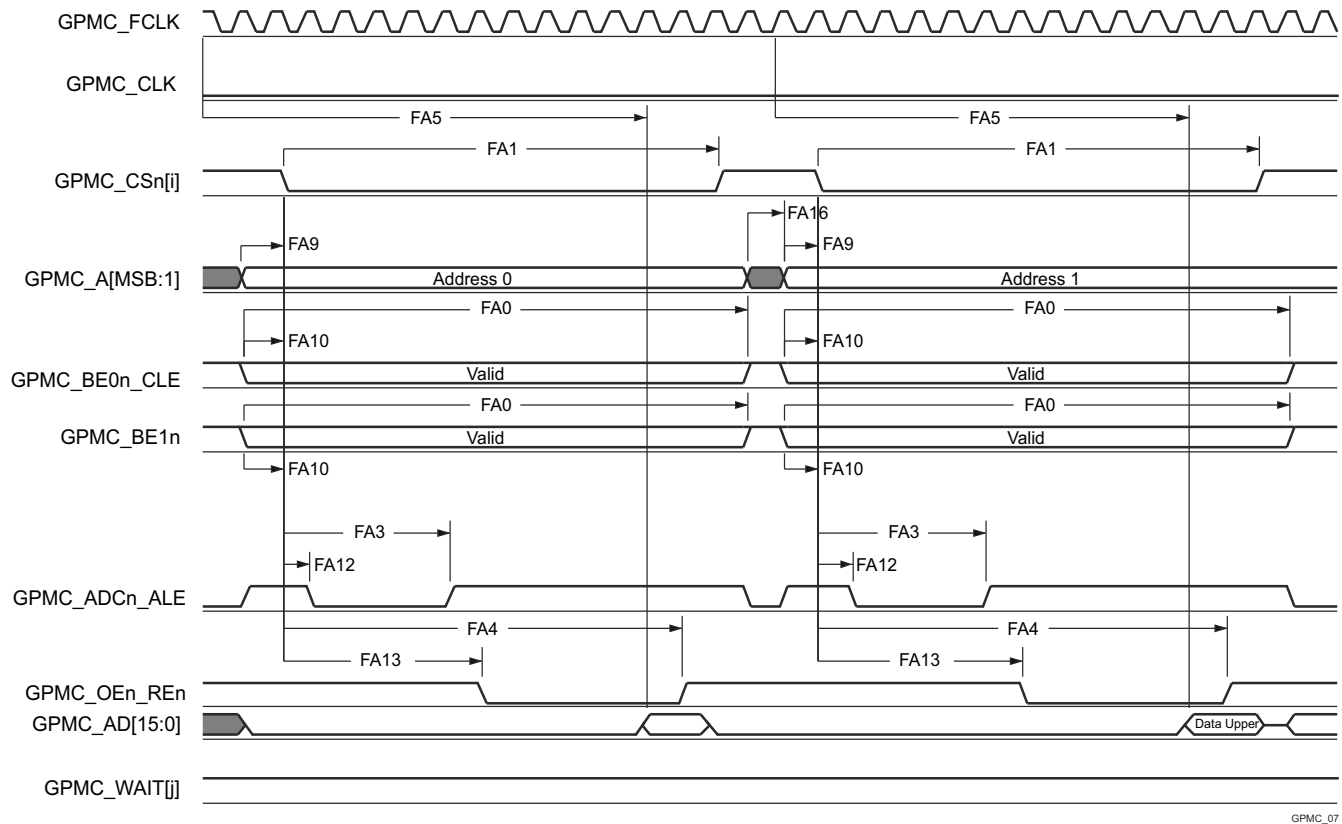
- (1) For single read:  $A = (CSRdOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For single write:  $A = (CSWrOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst read:  $A = (CSRdOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst write:  $A = (CSWrOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
with *n* being the page burst access number
- (2) For reading:  $B = ((ADVrOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
For writing:  $B = ((ADVwOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (3)  $C = ((OEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (4)  $D = PageBurstAccessTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (5)  $E = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (6)  $F = ((WEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (7)  $G = Cycle2CycleDelay \times GPMC\_FCLK^{(14)}$
- (8)  $I = ((OEOffTime + (n - 1) \times PageBurstAccessTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (9)  $J = (CSOnTime \times (TimeParaGranularity + 1) + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK^{(14)}$
- (10)  $K = ((ADVOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (11)  $L = ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (12) For single read:  $N = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For single write:  $N = WrCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst read:  $N = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst write:  $N = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (13) In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.
- (14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (15) For div\_by\_1\_mode:
  - GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
    - GPMC\_CLK frequency = GPMC\_FCLK frequency
  - CTRLMMR\_GPMC\_CLKSEL[1:0] CLK\_SEL = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz
  - GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOffTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)
- (16) For 133 MHz:
  - CTRLMMR\_GPMC\_CLKSEL[1:0] CLK\_SEL = 00 = MAIN\_PLL0\_HSDIV3\_CLKOUT



GPMC\_06

- In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

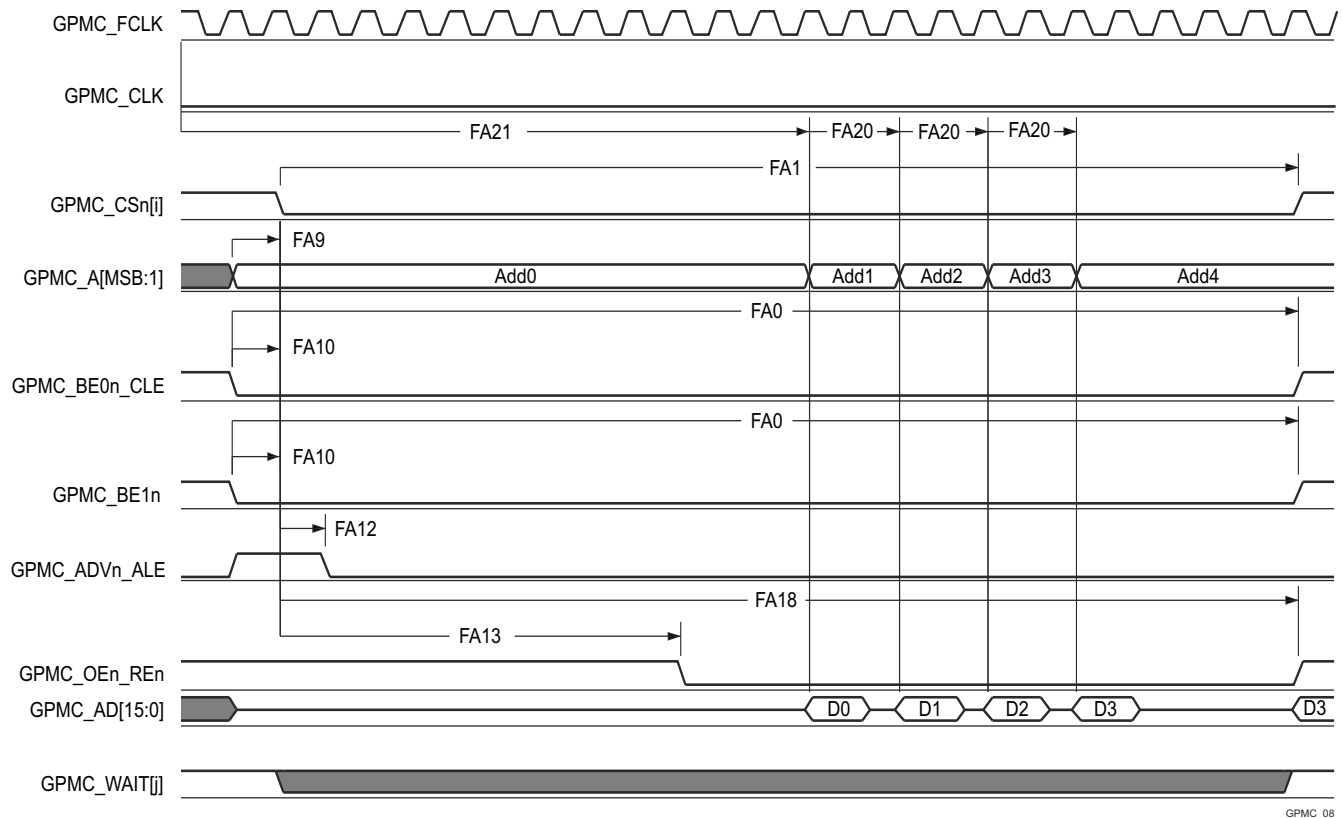
**Figure 6-56. GPMC and NOR Flash — Asynchronous Read — Single Word**



GPMC\_07

- A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

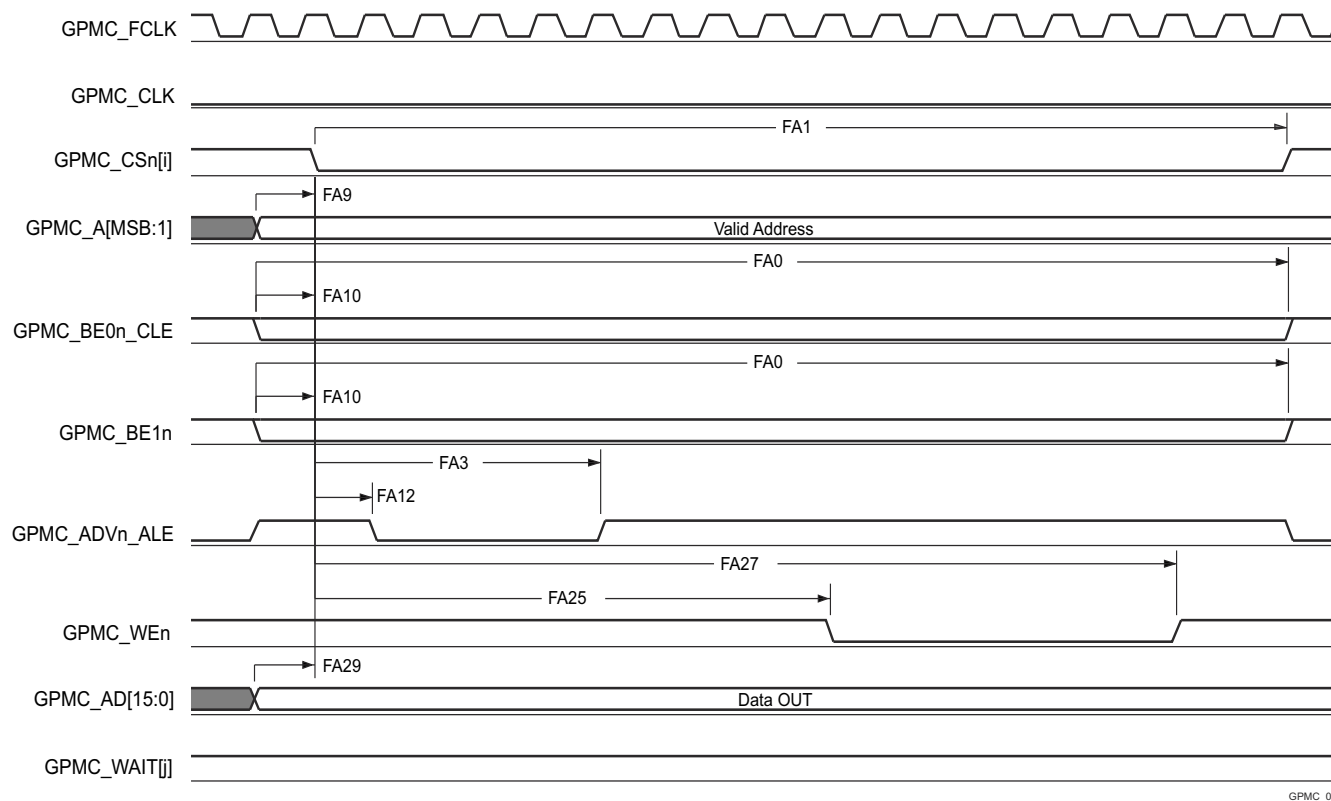
**Figure 6-57. GPMC and NOR Flash — Asynchronous Read — 32-Bit**



GPMC\_08

- In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.
- FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
- FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

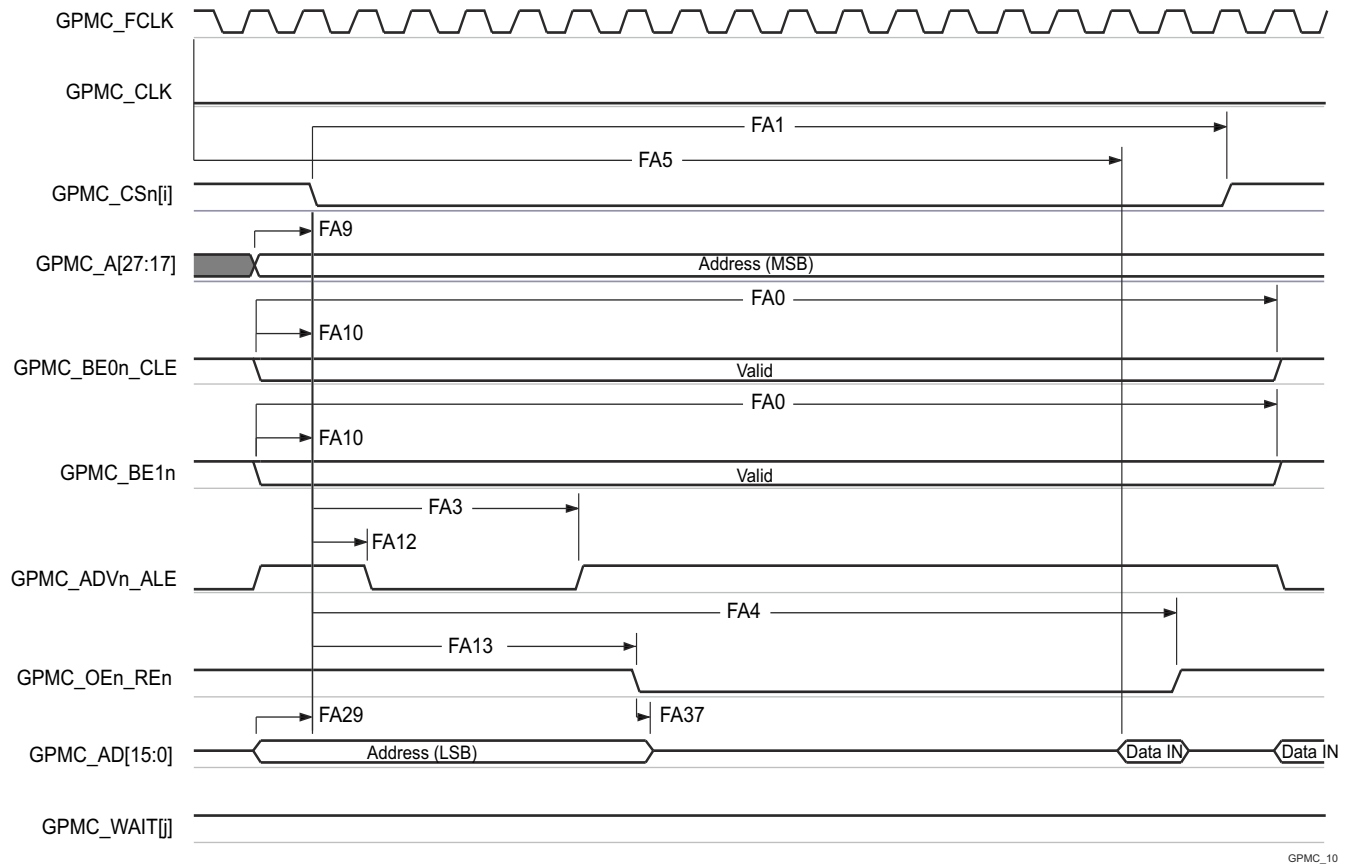
**Figure 6-58. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16-Bit**



GPMC\_09

A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

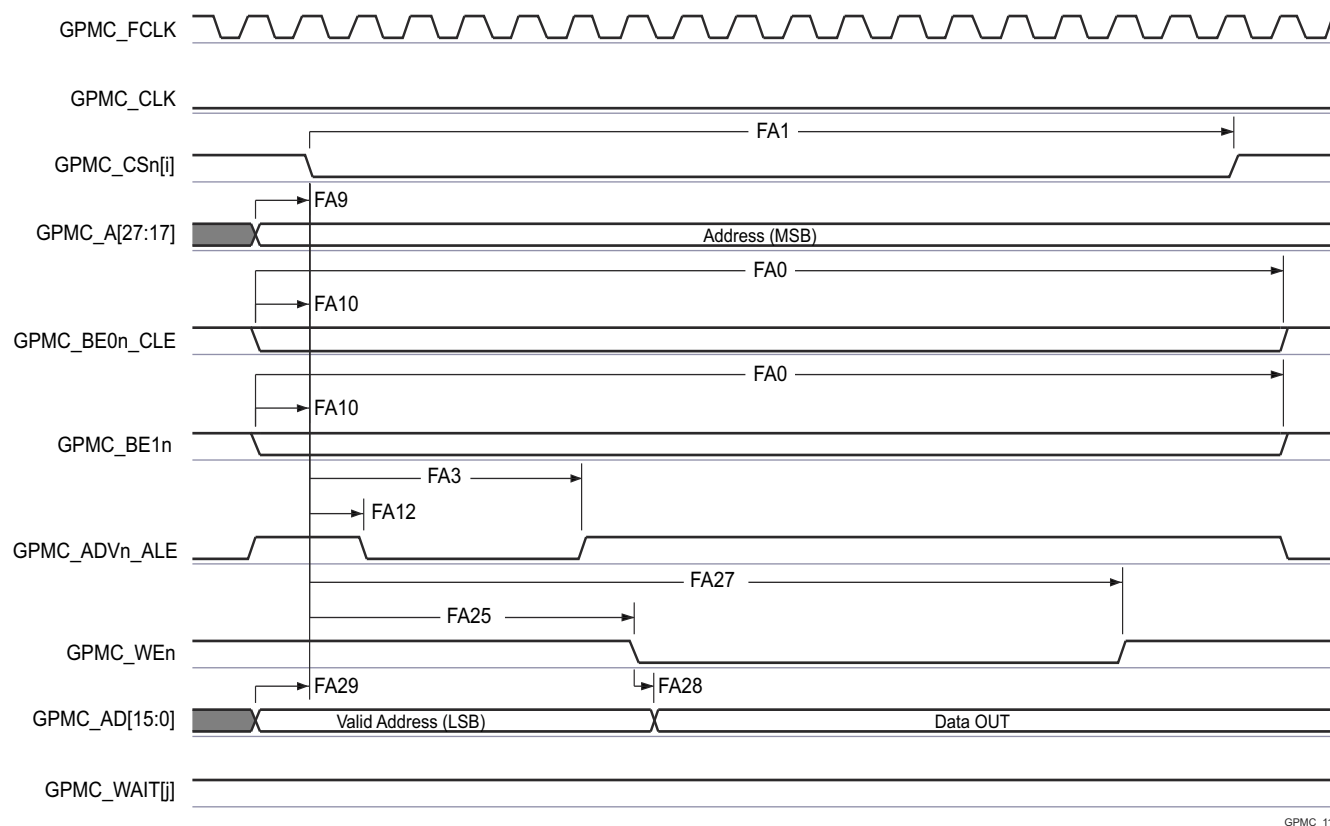
**Figure 6-59. GPMC and NOR Flash — Asynchronous Write — Single Word**



GPMC\_10

- In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-60. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word**



GPMC\_11

A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

**Figure 6-61. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word**

### 6.10.5.10.3 GPMC and NAND Flash — Asynchronous Mode

Section 6.10.5.10.3.1 and Section 6.10.5.10.3.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-62 through Figure 6-65).

#### 6.10.5.10.3.1 GPMC and NAND Flash Timing Requirements – Asynchronous Mode

| NO.                  |                                                                          | MODE <sup>(4)</sup>                                        | MIN                    | MAX              | UNIT |
|----------------------|--------------------------------------------------------------------------|------------------------------------------------------------|------------------------|------------------|------|
|                      |                                                                          |                                                            | 133 MHz <sup>(5)</sup> |                  |      |
| GNF12 <sup>(1)</sup> | t <sub>acc(d)</sub> Access time, input data GPMC_AD[15:0] <sup>(3)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                        | J <sup>(2)</sup> | ns   |

- (1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
- (2)  $J = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$ <sup>(3)</sup>
- (3) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (4) For div\_by\_1\_mode:
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
    - GPMC\_CLK frequency = GPMC\_FCLK frequency
  - CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHSIDIV\_CLKOUT3 = 2000/15 = 133.33 MHz
  - GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)
- (5) For 133 MHz:
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = MAIN\_PLL0\_HSDIV3\_CLKOUT

#### 6.10.5.10.3.2 GPMC and NAND Flash Switching Characteristics – Asynchronous Mode

| NO.  | PARAMETER                   |                                                                                                                             | MODE <sup>(15)</sup>                                       | MIN                     | MAX                     | UNIT |
|------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------|-------------------------|------|
|      |                             |                                                                                                                             |                                                            | 133 MHz <sup>(16)</sup> |                         |      |
| GNF0 | t <sub>w(wenV)</sub>        | Pulse duration, output write enable GPMC_WEn valid                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | A <sup>(1)</sup>        |                         | ns   |
| GNF1 | t <sub>d(csnV-wenV)</sub>   | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output write enable GPMC_WEn valid                       | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | B <sup>(2)</sup> - 2.55 | B <sup>(2)</sup> + 2.65 | ns   |
| GNF2 | t <sub>w(cleH-wenV)</sub>   | Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | C <sup>(3)</sup> - 2.55 | C <sup>(3)</sup> + 2.65 | ns   |
| GNF3 | t <sub>w(wenV-dV)</sub>     | Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid                                           | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | D <sup>(4)</sup> - 2.55 | D <sup>(4)</sup> + 2.65 | ns   |
| GNF4 | t <sub>w(wenIV-dIV)</sub>   | Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid                                       | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | E <sup>(5)</sup> - 2.55 | E <sup>(5)</sup> + 2.65 | ns   |
| GNF5 | t <sub>w(wenIV-cleIV)</sub> | Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | F <sup>(6)</sup> - 2.55 | F <sup>(6)</sup> + 2.65 | ns   |

| NO.   | PARAMETER                     |                                                                                                                         | MODE <sup>(15)</sup>                                       | MIN                      | MAX                      | UNIT |
|-------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|--------------------------|--------------------------|------|
|       |                               |                                                                                                                         |                                                            | 133 MHz <sup>(16)</sup>  |                          |      |
| GNF6  | t <sub>w(wenIV-CSn[i]V)</sub> | Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CSn[i] <sup>(13)</sup> invalid              | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | G <sup>(7)</sup> - 2.55  | G <sup>(7)</sup> + 2.65  | ns   |
| GNF7  | t <sub>w(aleH-wenV)</sub>     | Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | C <sup>(3)</sup> - 2.55  | C <sup>(3)</sup> + 2.65  | ns   |
| GNF8  | t <sub>w(wenIV-aleIV)</sub>   | Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | F <sup>(6)</sup> - 2.55  | F <sup>(6)</sup> + 2.65  | ns   |
| GNF9  | t <sub>c(wen)</sub>           | Cycle time, write                                                                                                       | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                          | H <sup>(8)</sup>         | ns   |
| GNF10 | t <sub>d(csnV-oenV)</sub>     | Delay time, output chip select GPMC_CSn[i] <sup>(13)</sup> valid to output enable GPMC_OEn_REn valid                    | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | I <sup>(9)</sup> - 2.55  | I <sup>(9)</sup> + 2.65  | ns   |
| GNF13 | t <sub>w(oenV)</sub>          | Pulse duration, output enable GPMC_OEn_REn valid                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                          | K <sup>(10)</sup>        | ns   |
| GNF14 | t <sub>c(oen)</sub>           | Cycle time, read                                                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | L <sup>(11)</sup>        |                          | ns   |
| GNF15 | t <sub>w(oenIV-CSn[i]V)</sub> | Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CSn[i] <sup>(13)</sup> invalid                | div_by_1_mode;                                             | M <sup>(12)</sup> - 2.55 | M <sup>(12)</sup> + 2.65 | ns   |

- (1)  $A = (WEOffTime - WEOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
 (2)  $B = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
 (3)  $C = ((WEOnTime - ADVOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - ADVExtraDelay)) \times GPMC\_FCLK^{(14)}$   
 (4)  $D = (WEOnTime \times (TimeParaGranularity + 1) + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK^{(14)}$   
 (5)  $E = ((WrCycleTime - WEOffTime) \times (TimeParaGranularity + 1) - 0.5 \times WEEExtraDelay) \times GPMC\_FCLK^{(14)}$   
 (6)  $F = ((ADVWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
 (7)  $G = ((CSWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
 (8)  $H = WrCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
 (9)  $I = ((OEOntime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
 (10)  $K = (OEOffTime - OEOntime) \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
 (11)  $L = RdCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
 (12)  $M = ((CSRdOffTime - OEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - OEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
 (13) In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.  
 (14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.  
 (15) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
 – GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

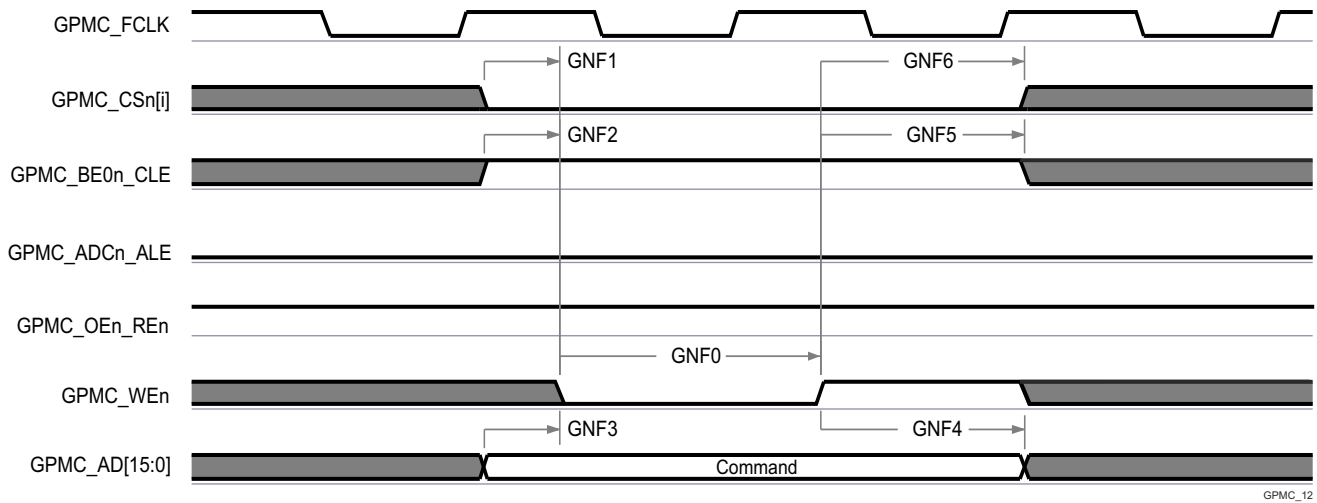
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHSIDIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRd/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

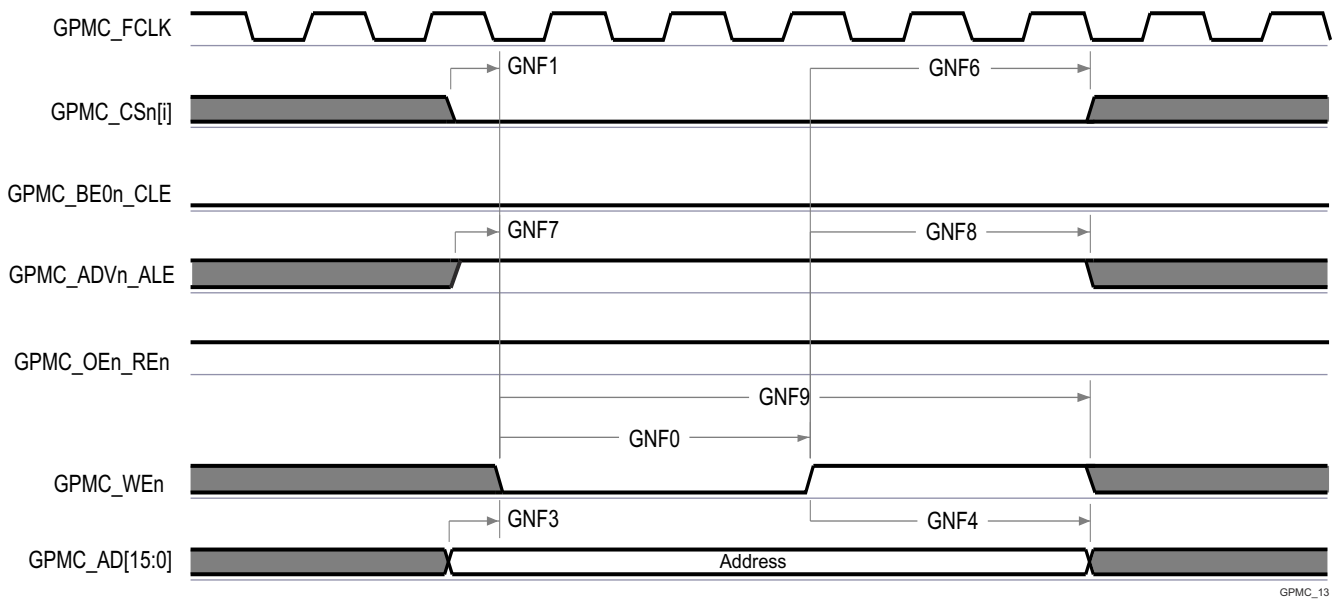
(16) For 133 MHz:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = MAIN\_PLL0\_HSDIV3\_CLKOUT



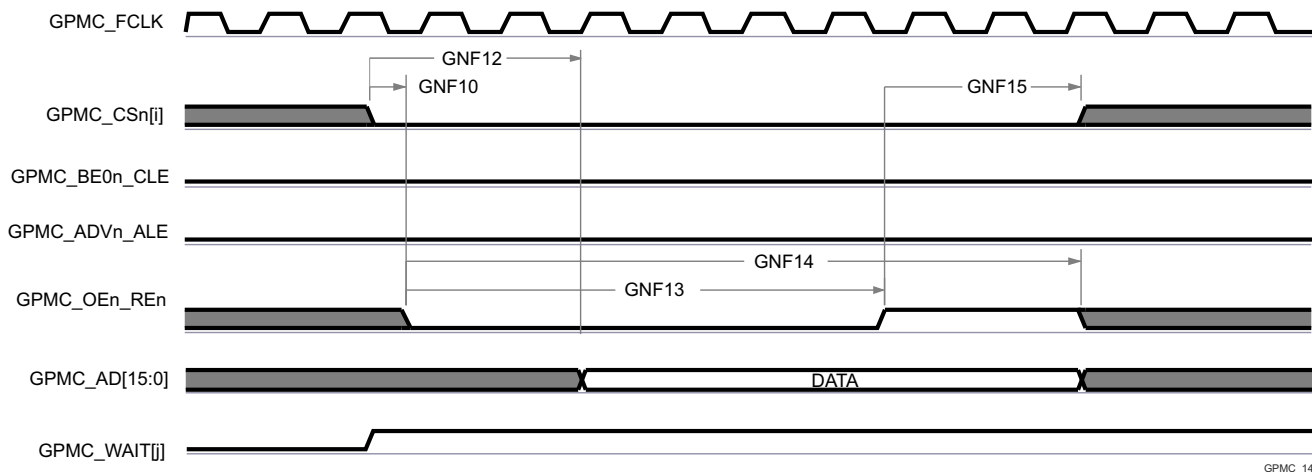
A. In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.

**Figure 6-62. GPMC and NAND Flash — Command Latch Cycle**



A. In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.

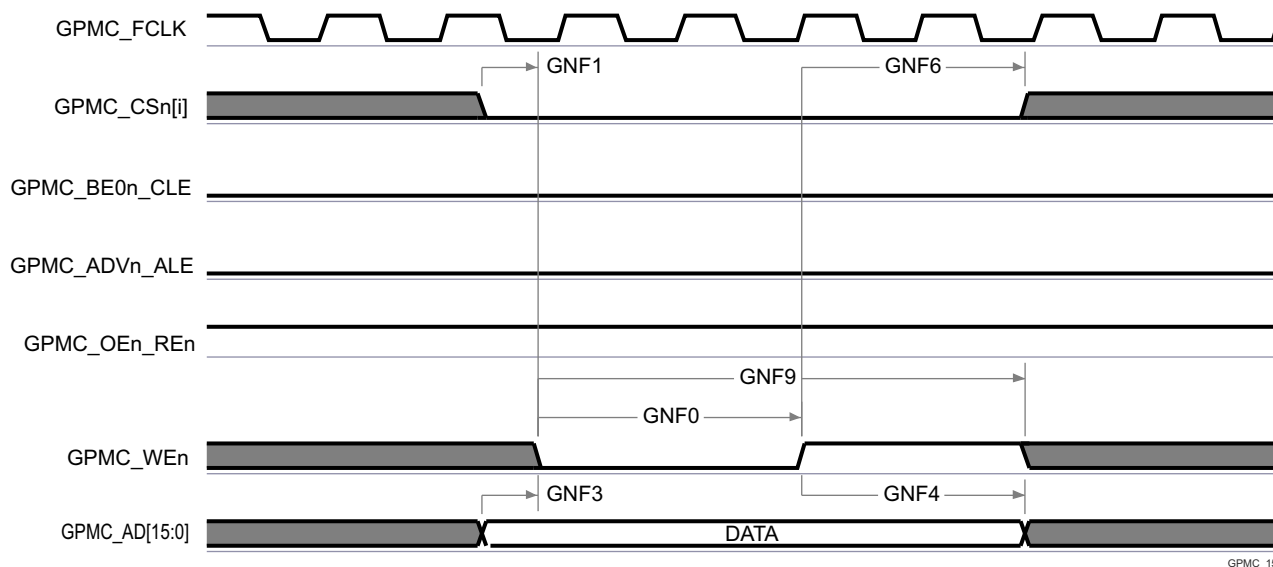
**Figure 6-63. GPMC and NAND Flash — Address Latch Cycle**



GPMC\_14

- A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- B. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- C. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

**Figure 6-64. GPMC and NAND Flash — Data Read Cycle**



GPMC\_15

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

**Figure 6-65. GPMC and NAND Flash — Data Write Cycle**

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.10.4 GPMC0 IOSET

Table 6-40 present the specific groupings of signals (IOSET) for use with GPMC0.

**Table 6-40. GPMC0 IOSET**

| Signals     | IOSET1         |     | IOSET2     |     |
|-------------|----------------|-----|------------|-----|
|             | BALL NAME      | MUX | BALL NAME  | MUX |
| GPMC0_WAIT2 | MDIO0_MDC      | 8   | MDIO0_MDC  | 8   |
| GPMC0_BE1n  | PRG1_PRU0_GPO0 | 8   | RGMII6_RD1 | 8   |

**Table 6-40. GPMC0 IOSET (continued)**

| Signals        | IOSET1          |     | IOSET2          |     |
|----------------|-----------------|-----|-----------------|-----|
|                | BALL NAME       | MUX | BALL NAME       | MUX |
| GPMC0_WAIT0    | PRG1_PRU0_GPO1  | 8   | PRG1_PRU0_GPO1  | 8   |
| GPMC0_WAIT1    | PRG1_PRU0_GPO2  | 8   | PRG1_PRU0_GPO2  | 8   |
| GPMC0_DIR      | PRG1_PRU0_GPO3  | 8   | PRG1_PRU0_GPO3  | 8   |
| GPMC0_CSn2     | PRG1_PRU0_GPO4  | 8   | PRG1_PRU0_GPO4  | 8   |
| GPMC0_WEn      | PRG1_PRU0_GPO5  | 8   | PRG1_PRU0_GPO5  | 8   |
| GPMC0_CSn3     | PRG1_PRU0_GPO6  | 8   | PRG1_PRU0_GPO6  | 8   |
| GPMC0_OEn_REn  | PRG1_PRU0_GPO8  | 8   | PRG1_PRU0_GPO8  | 8   |
| GPMC0_ADVh_ALE | PRG1_PRU0_GPO9  | 8   | PRG1_PRU0_GPO9  | 8   |
| GPMC0_BE0n_CLE | PRG1_PRU0_GPO10 | 8   | PRG1_PRU0_GPO10 | 8   |
| GPMC0_WPn      | PRG1_PRU1_GPO5  | 8   | PRG1_PRU1_GPO5  | 8   |
| GPMC0_CSn1     | PRG1_PRU1_GPO8  | 8   | PRG1_PRU1_GPO8  | 8   |
| GPMC0_CSn0     | PRG1_PRU1_GPO9  | 8   | PRG1_PRU1_GPO9  | 8   |
| GPMC0_CLKOUT   | PRG1_PRU1_GPO10 | 8   | PRG1_PRU1_GPO10 | 8   |
| GPMC0_AD0      | PRG0_PRU0_GPO5  | 8   | PRG0_PRU0_GPO5  | 8   |
| GPMC0_AD1      | PRG0_PRU0_GPO7  | 8   | PRG0_PRU0_GPO7  | 8   |
| GPMC0_AD2      | PRG0_PRU0_GPO8  | 8   | PRG0_PRU0_GPO8  | 8   |
| GPMC0_AD3      | PRG0_PRU0_GPO9  | 8   | PRG0_PRU0_GPO9  | 8   |
| GPMC0_AD4      | PRG0_PRU0_GPO10 | 8   | PRG0_PRU0_GPO10 | 8   |
| GPMC0_AD5      | PRG0_PRU0_GPO17 | 8   | PRG0_PRU0_GPO17 | 8   |
| GPMC0_AD6      | PRG0_PRU0_GPO18 | 8   | PRG0_PRU0_GPO18 | 8   |
| GPMC0_AD7      | PRG0_PRU0_GPO19 | 8   | PRG0_PRU0_GPO19 | 8   |
| GPMC0_AD8      | PRG0_PRU1_GPO5  | 8   | PRG0_PRU1_GPO5  | 8   |
| GPMC0_AD9      | PRG0_PRU1_GPO7  | 8   | PRG0_PRU1_GPO7  | 8   |
| GPMC0_AD10     | PRG0_PRU1_GPO8  | 8   | PRG0_PRU1_GPO8  | 8   |
| GPMC0_AD11     | PRG0_PRU1_GPO9  | 8   | PRG0_PRU1_GPO9  | 8   |
| GPMC0_AD12     | PRG0_PRU1_GPO10 | 8   | PRG0_PRU1_GPO10 | 8   |
| GPMC0_AD13     | PRG0_PRU1_GPO17 | 8   | PRG0_PRU1_GPO17 | 8   |
| GPMC0_AD14     | PRG0_PRU1_GPO18 | 8   | PRG0_PRU1_GPO18 | 8   |
| GPMC0_AD15     | PRG0_PRU1_GPO19 | 8   | PRG0_PRU1_GPO19 | 8   |
| GPMC0_A0       | PRG0_MDIO0_MDC  | 8   | PRG0_MDIO0_MDC  | 8   |
| GPMC0_A1       | RGMII5_TX_CTL   | 8   | RGMII5_TX_CTL   | 8   |
| GPMC0_A2       | RGMII5_RX_CTL   | 8   | RGMII5_RX_CTL   | 8   |
| GPMC0_A3       | RGMII5_TD3      | 8   | RGMII5_TD3      | 8   |
| GPMC0_A4       | RGMII5_TD2      | 8   | RGMII5_TD2      | 8   |
| GPMC0_A5       | RGMII5_TD1      | 8   | RGMII5_TD1      | 8   |
| GPMC0_A6       | RGMII5_TD0      | 8   | RGMII5_TD0      | 8   |
| GPMC0_A7       | RGMII5_TXC      | 8   | RGMII5_TXC      | 8   |
| GPMC0_A8       | RGMII5_RXC      | 8   | RGMII5_RXC      | 8   |
| GPMC0_A9       | RGMII5_RD3      | 8   | RGMII5_RD3      | 8   |
| GPMC0_A10      | RGMII5_RD2      | 8   | RGMII5_RD2      | 8   |
| GPMC0_A11      | RGMII5_RD1      | 8   | RGMII5_RD1      | 8   |
| GPMC0_A12      | RGMII5_RD0      | 8   | RGMII5_RD0      | 8   |
| GPMC0_A13      | RGMII6_TX_CTL   | 8   | RGMII6_TX_CTL   | 8   |
| GPMC0_A14      | RGMII6_RX_CTL   | 8   | RGMII6_RX_CTL   | 8   |

**Table 6-40. GPMC0 IOSET (continued)**

| Signals     | IOSET1          |     | IOSET2          |     |
|-------------|-----------------|-----|-----------------|-----|
|             | BALL NAME       | MUX | BALL NAME       | MUX |
| GPMC0_A15   | RGMII6_TD3      | 8   | RGMII6_TD3      | 8   |
| GPMC0_A16   | RGMII6_TD2      | 8   | RGMII6_TD2      | 8   |
| GPMC0_A17   | RGMII6_TD1      | 8   | RGMII6_TD1      | 8   |
| GPMC0_A18   | RGMII6_TD0      | 8   | RGMII6_TD0      | 8   |
| GPMC0_A19   | RGMII6_TXC      | 8   | RGMII6_TXC      | 8   |
| GPMC0_A20   | RGMII6_RXC      | 8   | RGMII6_RXC      | 8   |
| GPMC0_A21   | RGMII6_RD3      | 8   | RGMII6_RD3      | 8   |
| GPMC0_A22   | RGMII6_RD2      | 8   | RGMII6_RD2      | 8   |
| GPMC0_A23   | PRG0_PRU1_GPO2  | 8   | PRG0_PRU1_GPO2  | 8   |
| GPMC0_A24   | PRG0_PRU1_GPO4  | 8   | PRG0_PRU1_GPO4  | 8   |
| GPMC0_A25   | PRG0_PRU1_GPO6  | 8   | PRG0_PRU1_GPO6  | 8   |
| GPMC0_A26   | PRG0_PRU1_GPO11 | 8   | PRG0_PRU1_GPO11 | 8   |
| GPMC0_A27   | PRG0_MDIO0_MDIO | 8   | PRG0_MDIO0_MDIO | 8   |
| GPMC0_WAIT3 | MDIO0_MDIO      | 8   | MDIO0_MDIO      | 8   |

**6.10.5.11 HyperBus**

For more details about features and additional description information on the device HyperBus, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

[Section 6.10.5.11](#), [Section 6.10.5.11.2](#), and [Section 6.10.5.11.3](#) assume testing over the recommended operating conditions and electrical characteristic conditions (see [Figure 6-66](#), [Figure 6-67](#), and [Figure 6-68](#)).

[Table 6-41](#) represents HyperBus timing conditions.

**Table 6-41. HyperBus Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 2   | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 1.5 | 8   | pF   |

**6.10.5.11.1 Timing Requirements for HyperBus**

| NO. | PARAMETER                    | DESCRIPTION                               | MIN    | MAX | UNIT |
|-----|------------------------------|-------------------------------------------|--------|-----|------|
| D1  | t <sub>w</sub> (RESETn)      | Pulse width, RESETn                       | 200    |     | ns   |
| D2  | t <sub>w</sub> (csL)         | Pulse width, Chip Select                  | 1000   |     | ns   |
| D3  | t <sub>d</sub> (RESETnH-csL) | Delay time, RESETn inactive to CSn active | 200.34 |     | ns   |
| D4  | t <sub>d</sub> (csL-RWDSL)   | Delay time, CSn active to RWDS falling    | 115    |     | ns   |

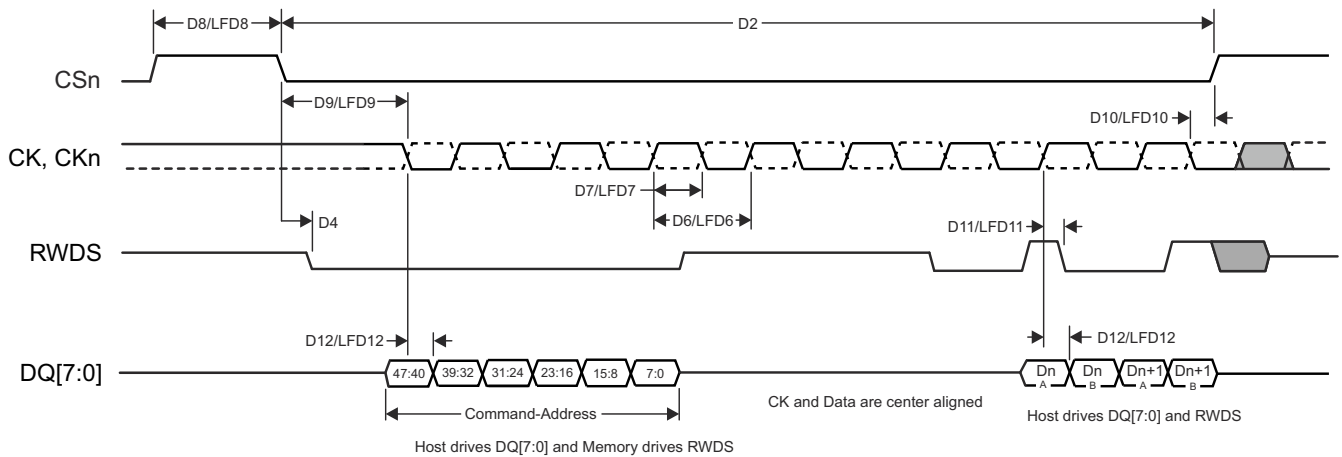
**6.10.5.11.2 HyperBus 166 MHz Switching Characteristics**

| NO. | PARAMETER                     | DESCRIPTION                                                    | MIN   | MAX   | UNIT |
|-----|-------------------------------|----------------------------------------------------------------|-------|-------|------|
| D5  | t <sub>skn</sub> (rwdsX-dV)   | Input skew, RWDS transitioning to D0:D7 valid                  | -0.46 | 0.46  | ns   |
| D6  | t <sub>c</sub> (clk/clkn)     | CLK period, CLK/CLKn                                           | 6     |       | ns   |
| D7  | t <sub>w</sub> (clk/clkn)     | Pulse width, CLK/CLKn                                          | 2.7   |       | ns   |
| D8  | t <sub>w</sub> (csIV)         | Pulse width, CS0 invalid between operations                    | 6     |       | ns   |
| D9  | t <sub>d</sub> (clkH-csL)     | Delay time, CS0 active to CLK rising/ CLKn falling             |       | -3.34 | ns   |
| D10 | t <sub>d</sub> (clkL[LE]-csH) | Delay time, last falling CLK/ rising CLKn edge to CS0 inactive | 0.41  |       | ns   |
| D11 | t <sub>d</sub> (clkX-rwdsV)   | Delay time, CLK transition to RWDS valid                       | 1.01  | 2.08  | ns   |

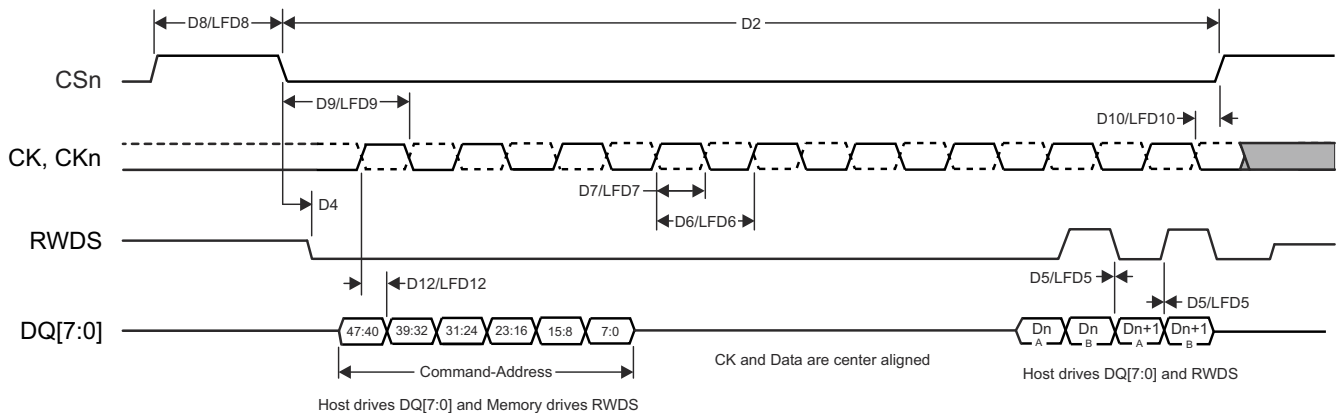
| NO. | PARAMETER                           | DESCRIPTION                                  | MIN  | MAX  | UNIT |
|-----|-------------------------------------|----------------------------------------------|------|------|------|
| D12 | $t_{d(\text{clkX-d}[0:7]\text{V})}$ | Delay time, CLK transitioning to D0:D7 valid | 0.84 | 2.17 | ns   |

### 6.10.5.11.3 HyperBus 100 MHz Switching Characteristics

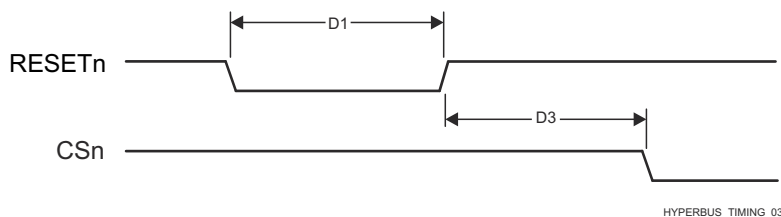
| NO.   | PARAMETER                           | DESCRIPTION                                       | MIN   | MAX   | UNIT |
|-------|-------------------------------------|---------------------------------------------------|-------|-------|------|
| LFD5  | $t_{\text{skn}(\text{rwdsX-dV})}$   | Input skew, RWDS transitioning to D0:D7 valid     | -0.81 | 0.81  | ns   |
| LFD6  | $t_{c(\text{clk})}$                 | CLK period, CLK                                   | 10    |       | ns   |
| LFD7  | $t_{w(\text{clk})}$                 | Pulse width, CLK                                  | 4.75  |       | ns   |
| LFD8  | $t_{w(\text{csIV})}$                | Pulse width, CS0 invalid between operations       | 10    |       | ns   |
| LFD9  | $t_{d(\text{clkH-csL})}$            | Delay time, CS0 active to CLK rising              |       | -3.51 | ns   |
| LFD10 | $t_{d(\text{clkL[LE]-csH})}$        | Delay time, last falling CLK edge to CS0 inactive | 0.51  |       | ns   |
| LFD11 | $t_{d(\text{clkX-rwdsV})}$          | Delay time, CLK transition to RWDS valid          | 1.51  | 3.49  | ns   |
| LFD12 | $t_{d(\text{clkX-d}[0:7]\text{V})}$ | Delay time, CLK transitioning to D0:D7 valid      | 1.34  | 3.66  | ns   |



**Figure 6-66. HyperBus Timing Diagrams – Transmitter Mode**



**Figure 6-67. HyperBus Timing Diagrams – Receiver Mode**



**Figure 6-68. HyperBus Timing Diagrams – Reset**

For more information, see *HyperBus Interface* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.12 I2C

The device contains **several** multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I2C-bus™ specification version 2.1. However, the device **IO Buffers** are not fully compliant to the I2C electrical specification. **Some I2C instances use the LVCMOS Buffer Type, while other instances use the I2S OD FS Buffer type. See the Pin Attributes table to determine the IO Buffer Type used for each I2C instance on this device.** The I2C speeds supported and exceptions are described per **IO Buffer Type** below:

- I2C instances that use the LVCMOS buffer type
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 1.8V
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 1.8V
      - 3.3V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5V)$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the [Absolute Maximum Ratings](#) section of this data sheet.
- I2C instances that use the I2C OD FS buffer type
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 1.8V
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 1.8V
      - 3.3V
    - Hs-mode (up to 3.4Mbit/s)
      - 1.8V
  - Exceptions:
    - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3V. So Hs-mode is limited to 1.8-V operation.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.08V/ns (or 8E+7V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C

specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.08V/ns.

- The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5V)$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the [Absolute Maximum Ratings](#) section of this data sheet.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within [Section 5.3](#) and *Detailed Description*.

#### 6.10.5.13 I3C

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

[Table 6-42](#), [Table 6-43](#), [Figure 6-69](#), [Table 6-44](#), and [Figure 6-70](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-42. I3C Open Drain Timing Conditions**

| PARAMETER                     | MIN    | MAX | UNIT |
|-------------------------------|--------|-----|------|
| <b>INPUT CONDITIONS</b>       |        |     |      |
| $SR_I$ Input slew rate        | 0.2276 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b>      |        |     |      |
| $C_L$ Output load capacitance |        | 50  | pF   |

**Table 6-43. I3C Open Drain Timing Parameters**

| NO. | PARAMETER        | DESCRIPTION                                                            | MODE               | MIN                                   | MAX      | UNIT |
|-----|------------------|------------------------------------------------------------------------|--------------------|---------------------------------------|----------|------|
| D1  | $t_{LOW\_OD}$    | Low Period of SCL Clock                                                | Controller         | 200                                   |          | ns   |
|     | $t_{DIG\_OD\_L}$ |                                                                        |                    | $t_{LOW\_OD\ MIN} + t_{FDA\_OD\ MIN}$ |          | ns   |
| D2  | $t_{HIGH}$       | High Period of SCL Clock                                               | Controller         |                                       | 41       | ns   |
|     | $t_{DIG\_H}$     |                                                                        |                    | $t_{HIGH} + t_{CF}$                   |          | ns   |
| D3  | $t_{FDA\_OD}$    | Fall Time of SDA Signal                                                | Controller, Target | $t_{CF}$                              | 12       | ns   |
| D4  | $t_{SU\_OD}$     | SDA Data Setup Time During Open Drain Mode                             | Controller, Target | 3                                     |          | ns   |
| D5  | $t_{CAS}$        | Clock After START (S) Condition                                        | Controller, ENTAS0 | 38.4                                  | 1000     | ns   |
|     |                  |                                                                        | Controller, ENTAS1 | 38.4                                  | 100000   | ns   |
|     |                  |                                                                        | Controller, ENTAS2 | 38.4                                  | 2000000  | ns   |
|     |                  |                                                                        | Controller, ENTAS3 | 38.4                                  | 50000000 | ns   |
| D6  | $t_{CBP}$        | Clock Before STOP (P) Condition                                        | Controller         | $t_{CAS\ MIN} / 2$                    |          | ns   |
| D7  | $t_{MMOVERLAP}$  | Current Controller to Secondary Controller Overlap time during handoff | Controller         | $t_{DIG\_OD\_L\ min}$                 |          | ns   |
| D8  | $t_{AVAL}$       | Bus Available Condition                                                | Controller         | 1000                                  |          | ns   |
| D9  | $t_{IDLE}$       | Bus Idle Condition                                                     | Controller         | 1000000                               |          | ns   |
| D10 | $t_{MMLOCK}$     | Time Interval Where New Controller Not Driving SDA Low                 | Controller         | $t_{AVAL\ min}$                       |          | ns   |

- This is approximately equal to  $t_{LOW\ min} + t_{DS\_OD\ min} + t_{rDA\_OD\ typ} + t_{SU\_OD\ min}$ .

- The Controller may use a shorter Low period if the Controller knows that this is safe, when SDA is already above  $V_{IH}$ .
- Based on  $t_{SPIKE}$ , rise and fall times, and interconnect.
- This maximum High period may be exceeded when the signals can be safely seen by Legacy I2C Devices, and/or in consideration of the interconnect (for example: a short Bus).
- On a Legacy Bus where I2C Devices need to see Start, the  $t_{CAS}$  Min value is further constrained.
- Targets that do not support the optional ENTASx CCCs shall use the  $t_{CAS}$  Max value shown for ENTAS3.
- On a Mixed Bus with Fm Legacy I2C Devices,  $t_{AVAL}$  is 300ns shorter than the Fm Bus Free Condition time ( $t_{BUF}$ ).

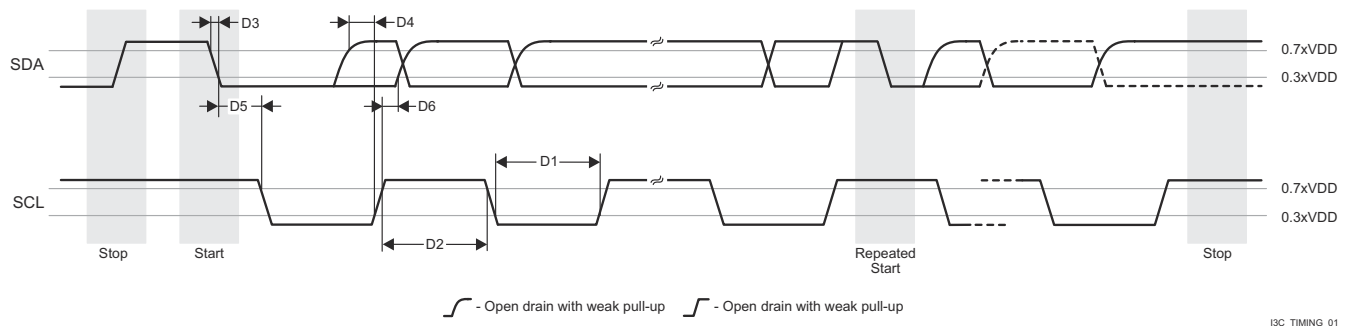


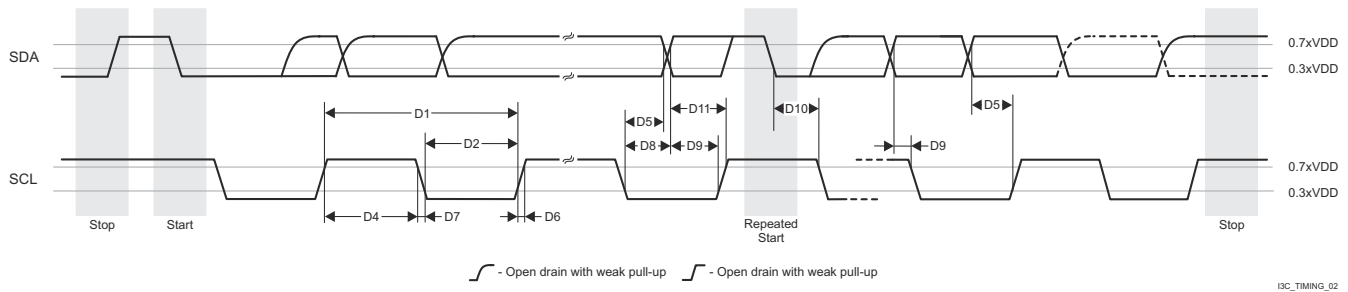
Figure 6-69. I3C Open Drain Timing

Table 6-44. I3C Push-Pull Timing Parameters for SDR and HDR-DDR Modes

| NO. | PARAMETER           | DESCRIPTION                                                           | MODE               | MIN                              | MAX    | UNIT |
|-----|---------------------|-----------------------------------------------------------------------|--------------------|----------------------------------|--------|------|
| D1  | $f_{SCL}$           | SCL Clock Period                                                      | Controller         | 80                               | 100000 | ns   |
| D2  | $t_{LOW}$           | SCL Clock Low Period                                                  | Controller         | 24                               |        | ns   |
|     | $t_{DIG\_L}$        |                                                                       |                    | 32                               |        | ns   |
| D3  | $t_{HIGH\_MIXED}$   | SCL Clock High Period of Mixed Bus (Mixed Bus Topology Not Supported) | Controller         | 24                               |        | ns   |
|     | $t_{DIG\_H\_MIXED}$ |                                                                       |                    | 32                               | 45     | ns   |
| D4  | $t_{HIGH}$          | SCL Clock High Period                                                 | Controller         | 24                               |        | ns   |
|     | $t_{DIG\_H}$        |                                                                       |                    | 32                               |        | ns   |
| D5  | $t_{SCO}$           | Clock in to Data Out for Target                                       | Target             | 12                               |        | ns   |
| D6  | $t_{CR}$            | SCL Clock Rise Time                                                   | Controller         | $150 \times 1 / f_{SCL}$         | 60     | ns   |
| D7  | $t_{CF}$            | SCL Clock Fall Time                                                   | Controller         | $150 \times 1 / f_{SCL}$         | 60     | ns   |
| D8  | $t_{HD\_PP}$        | SDA Signal Data Hold in Push Pull Mode                                | Controller         | $t_{CR} + 3$<br>and $t_{CF} + 3$ |        | ns   |
|     |                     |                                                                       | Target             | 0                                |        | ns   |
| D9  | $t_{SU\_PP}$        | SDA Signal Data Setup In Push-Pull Mode                               | Controller, Target | 3                                |        | ns   |
| D10 | $t_{CASr}$          | Clock After Repeated START (Sr)                                       | Controller         | $t_{CAS}$ MIN                    |        | ns   |
| D11 | $t_{CBSr}$          | Clock Before Repeated START (Sr)                                      | Controller         | $t_{CAS}$ MIN / 2                |        | ns   |

- $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$
- $t_{DIG\_L}$  and  $t_{DIG\_H}$  are the clock Low and High periods as seen at the receiver end of the I3C Bus using  $V_{IL}$  and  $V_{IH}$ .
- When communicating with an I3C Device on a mixed Bus, the  $t_{DIG\_H\_MIXED}$  period must be constrained to make sure that I2C Devices do not interpret I3C signaling as valid I2C signaling.
- As both edges are used, the hold time needs to be satisfied for the respective edges;  $t_{CF} + 3$  for falling edge clocks, and  $t_{CR} + 3$  for rising edge clocks.

5. Clock Frequency Minimum 0.01 MHz, Maximum 12.5 MHz



**Figure 6-70. I3C Push-Pull Timing (SDR and HDR-DDR Modes)**

**6.10.5.14 MCAN**

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

**Note**

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

**Table 6-45. MCAN Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 2   | 15  | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 5   | 20  | pF   |

**Table 6-46. MCAN Switching Characteristics**

| NO.   | PARAMETER               |                                                                    | MIN | MAX | UNIT |
|-------|-------------------------|--------------------------------------------------------------------|-----|-----|------|
| MCAN1 | t <sub>d(MCAN_TX)</sub> | Delay time, transmit shift register to MCANn_TX pin <sup>(1)</sup> |     | 10  | ns   |
| MCAN2 | t <sub>d(MCAN_RX)</sub> | Delay time, MCANn_RX pin to receive shift register <sup>(1)</sup>  |     | 10  | ns   |

(1) n is [0:13] in MCANn\_\* or [0:1] in MCU\_MCANn\_\*

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

### 6.10.5.15 MCASP

For more details about features and additional description information on the device Multichannel Audio Serial Port, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

[Table 6-48](#) and [Figure 6-71](#) present timing requirements for MCASP0 to MCASP11.

[Table 6-47](#) represents MCASP timing conditions.

**Table 6-47. MCASP Timing Conditions**

| PARAMETER                             |                                              | MIN | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|-----|------|------|
| <b>INPUT CONDITIONS</b>               |                                              |     |      |      |
| SR <sub>I</sub>                       | Input slew rate                              | 0.7 | 5    | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |     |      |      |
| C <sub>L</sub>                        | Output load capacitance                      | 1   | 10   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |     |      |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | 100 | 1100 | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |     | 100  | ps   |

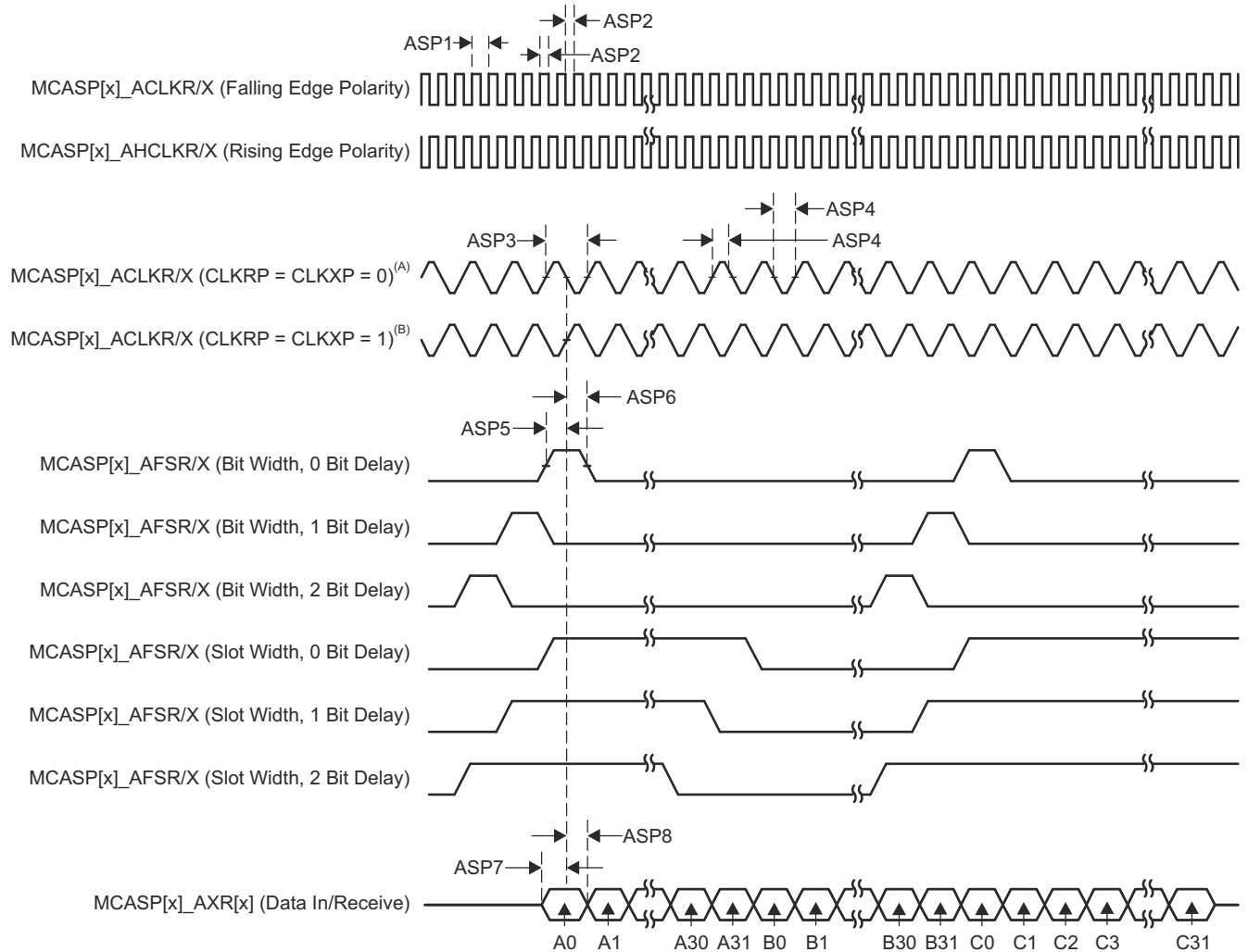
**Table 6-48. MCASP Timing Requirements**

| NO.  |                                 |                                                                 | MODE <sup>(1)</sup> | MIN                        | MAX | UNIT |
|------|---------------------------------|-----------------------------------------------------------------|---------------------|----------------------------|-----|------|
| ASP1 | t <sub>c</sub> (AHCLKRX)        | Cycle time, MCASP[x]_AHCLKR/X                                   |                     | 15.26                      |     | ns   |
| ASP2 | t <sub>w</sub> (AHCLKRX)        | Pulse duration, MCASP[x]_AHCLKR/X high or low                   |                     | 0.5P <sup>(2)</sup> - 1.53 |     | ns   |
| ASP3 | t <sub>c</sub> (ACLKRX)         | Cycle time, MCASP[x]_ACLKR/X                                    |                     | 15.26                      |     | ns   |
| ASP4 | t <sub>w</sub> (ACLKRX)         | Pulse duration, MCASP[x]_ACLKR/X high or low                    |                     | 0.5R <sup>(3)</sup> - 1.53 |     | ns   |
| ASP5 | t <sub>su</sub> (AFSRX-ACLKR/X) | Setup time, MCASP[x]_AFSR/X input valid before MCASP[x]_ACLKR/X | ACLKR/X int         | 12.3                       |     | ns   |
|      |                                 |                                                                 | ACLKR/X ext in/out  | 4                          |     |      |
| ASP6 | t <sub>h</sub> (ACLKR/X-AFSRX)  | Hold time, MCASP[x]_AFSR/X input valid after MCASP[x]_ACLKR/X   | ACLKR/X int         | -1                         |     | ns   |
|      |                                 |                                                                 | ACLKR/X ext in/out  | 1.6                        |     |      |
| ASP7 | t <sub>su</sub> (AXR-ACLKR/X)   | Setup time, MCASP[x]_AXR input valid before MCASP[x]_ACLKR/X    | ACLKR/X int         | 12.3                       |     | ns   |
|      |                                 |                                                                 | ACLKR/X ext in/out  | 4                          |     |      |
| ASP8 | t <sub>h</sub> (ACLKR/X-AXR)    | Hold time, MCASP[x]_AXR input valid after MCASP[x]_ACLKR/X      | ACLKR/X int         | -1                         |     | ns   |
|      |                                 |                                                                 | ACLKR/X ext in/out  | 1.6                        |     |      |

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.



- A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).
- B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

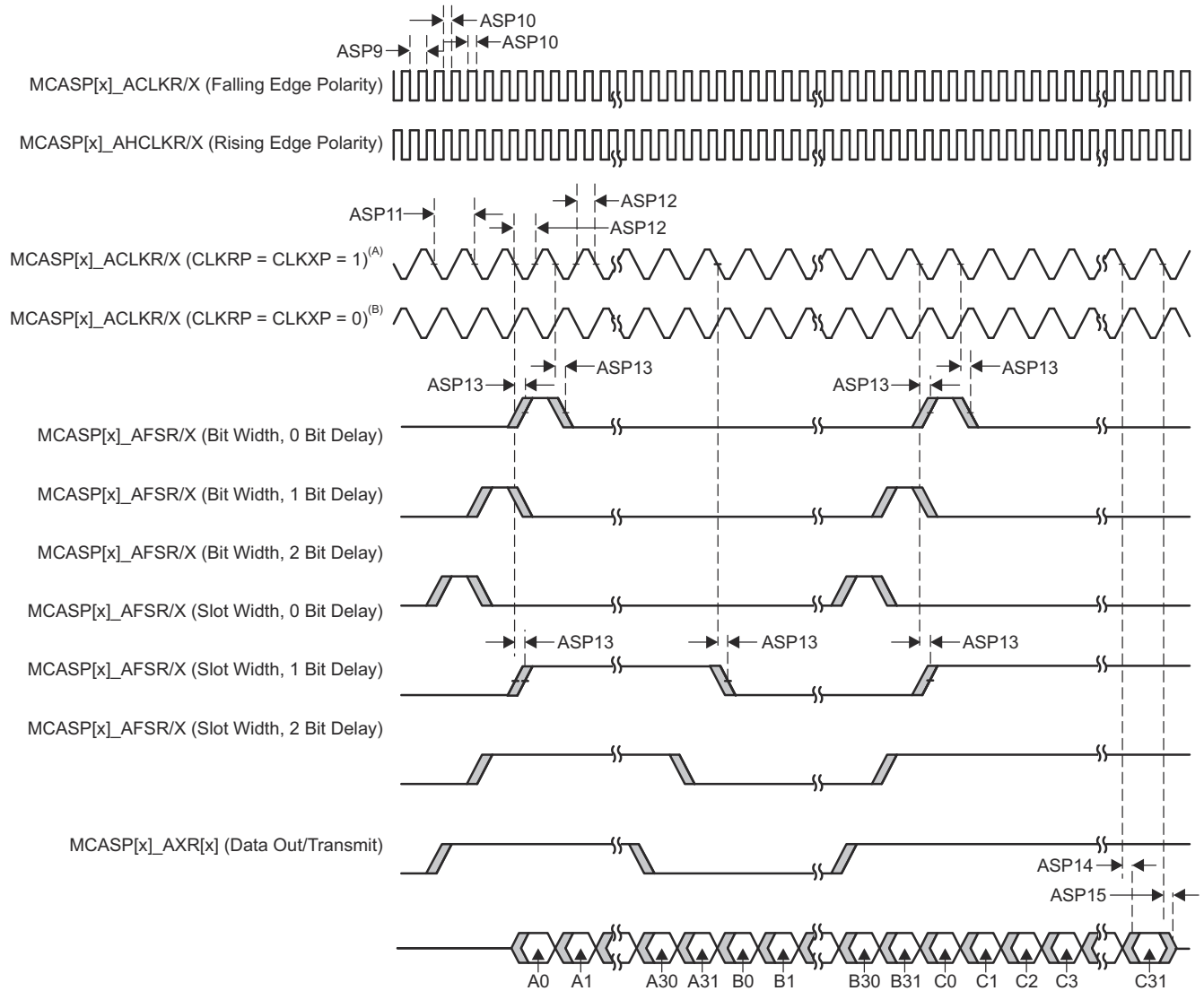
**Figure 6-71. MCASP Input Timing**

Table 6-49 and Figure 6-72 present switching characteristics over recommended operating conditions for MCASP0 to MCASP11.

**Table 6-49. MCASP Switching Characteristics**

| NO.   | PARAMETER             | DESCRIPTION                                                                      | MODE <sup>(1)</sup> | MIN                     | MAX   | UNIT |
|-------|-----------------------|----------------------------------------------------------------------------------|---------------------|-------------------------|-------|------|
| ASP9  | $t_{c(AHCLKRX)}$      | Cycle time, MCASP[x]_AHCLKR/X                                                    |                     | 20                      |       | ns   |
| ASP10 | $t_{w(AHCLKRX)}$      | Pulse duration, MCASP[x]_AHCLKR/X high or low                                    |                     | 0.5P <sup>(2)</sup> - 2 |       | ns   |
| ASP11 | $t_{c(ACLKRX)}$       | Cycle time, MCASP[x]_ACLKR/X                                                     |                     | 20                      |       | ns   |
| ASP12 | $t_{w(ACLKRX)}$       | Pulse duration, MCASP[x]_ACLKR/X high or low                                     |                     | 0.5R <sup>(3)</sup> - 2 |       | ns   |
| ASP13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, MCASP[x]_ACLKR/X transmit edge to MCASP[x]_AFSR/X output valid       | ACLKR/X int         | 0                       | 7.25  | ns   |
|       |                       |                                                                                  | ACLKR/X ext in/out  | -15.28                  | 12.84 |      |
| ASP14 | $t_{d(ACLKX-AXR)}$    | Delay time, MCASP[x]_ACLKX transmit edge to MCASP[x]_AXR output valid            | ACLKR/X int         | 0                       | 7.25  | ns   |
|       |                       |                                                                                  | ACLKR/X ext in/out  | -15.28                  | 12.84 |      |
| ASP15 | $t_{dis(ACLKX-AXR)}$  | Disable time, MCASP[x]_ACLKX transmit edge to MCASP[x]_AXR output high impedance | ACLKR/X int         | 0                       | 7.25  | ns   |
|       |                       |                                                                                  | ACLKR/X ext in/out  | -14.9                   | 14    |      |

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
- (2) P = AHCLKR/X period in ns.
- (3) R = ACLKR/X period in ns.



- A. For  $\text{CLKRP} = \text{CLKXP} = 1$ , the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).
- B. For  $\text{CLKRP} = \text{CLKXP} = 0$ , the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

**Figure 6-72. MCASP Output Timing**

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

### 6.10.5.16 MCSPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

[Table 6-50](#) represents MCSPI timing conditions.

#### Note

The IO timings provided in this section are applicable for all combinations of signals for MCU\_SPI0 and MCU\_SPI1. However, the timings are only valid for MCU\_SPI0 and MCU\_SPI1 if signals within a single IOSET are used. The IOSETs are defined in the [Table 6-55](#) and [Table 6-56](#) tables.

**Table 6-50. MCSPI Timing Conditions**

| PARAMETER                |                         |           | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |           |     |     |      |
| SR <sub>I</sub>          | Input slew rate         |           | 2   | 8.5 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |           |     |     |      |
| C <sub>L</sub>           | Output load capacitance | CLK       | 6   | 24  | pF   |
|                          |                         | D[x], CSi | 6   | 12  | pF   |

#### 6.10.5.16.1 MCSPI — Controller Mode

[Table 6-51](#), [Figure 6-73](#), [Table 6-52](#), and [Figure 6-74](#) present timing requirements and switching characteristics for MCSPI – Controller Mode.

**Table 6-51. MCSPI Timing Requirements - Controller Mode**

see [Figure 6-73](#)

| NO. |                               |                                                       | MIN | MAX | UNIT |
|-----|-------------------------------|-------------------------------------------------------|-----|-----|------|
| SM4 | t <sub>su(misoV-spickV)</sub> | Setup time, SPI_D[x] valid before SPI_CLK active edge | 2.9 |     | ns   |
| SM5 | t <sub>h(spickV-misoV)</sub>  | Hold time, SPI_D[x] valid after SPI_CLK active edge   | 2   |     | ns   |

**Table 6-52. MCSPI Switching Characteristics - Controller Mode**

see [Figure 6-74](#)

| NO. | PARAMETER                    |                                                        | MODE                   | MIN                     | MAX | UNIT |
|-----|------------------------------|--------------------------------------------------------|------------------------|-------------------------|-----|------|
| SM1 | t <sub>c(spick)</sub>        | Cycle time, SPI_CLK                                    |                        | 20                      |     | ns   |
| SM2 | t <sub>w(spickL)</sub>       | Pulse duration, SPI_CLK low                            |                        | 0.5P - 1 <sup>(1)</sup> |     | ns   |
| SM3 | t <sub>w(spickH)</sub>       | Pulse duration, SPI_CLK high                           |                        | 0.5P - 1 <sup>(1)</sup> |     | ns   |
| SM6 | t <sub>d(spickV-simoV)</sub> | Delay time, SPI_CLK active edge to SPI_D[x] transition |                        | -2                      | 2   | ns   |
| SM7 | t <sub>d(csV-simoV)</sub>    | Delay time, SPI_CSi active edge to SPI_D[x] transition |                        | 5                       |     | ns   |
| SM8 | t <sub>d(csV-spick)</sub>    | Delay time, SPI_CSi active to SPI_CLK first edge       | PHA = 0 <sup>(2)</sup> | B - 4 <sup>(3)</sup>    |     | ns   |
|     |                              |                                                        | PHA = 1 <sup>(2)</sup> | A - 4 <sup>(4)</sup>    |     | ns   |
| SM9 | t <sub>d(spickV-csV)</sub>   | Delay time, SPI_CLK last edge to SPI_CSi inactive      | PHA = 0 <sup>(2)</sup> | A - 4 <sup>(4)</sup>    |     | ns   |
|     |                              |                                                        | PHA = 1 <sup>(2)</sup> | B - 4 <sup>(3)</sup>    |     | ns   |

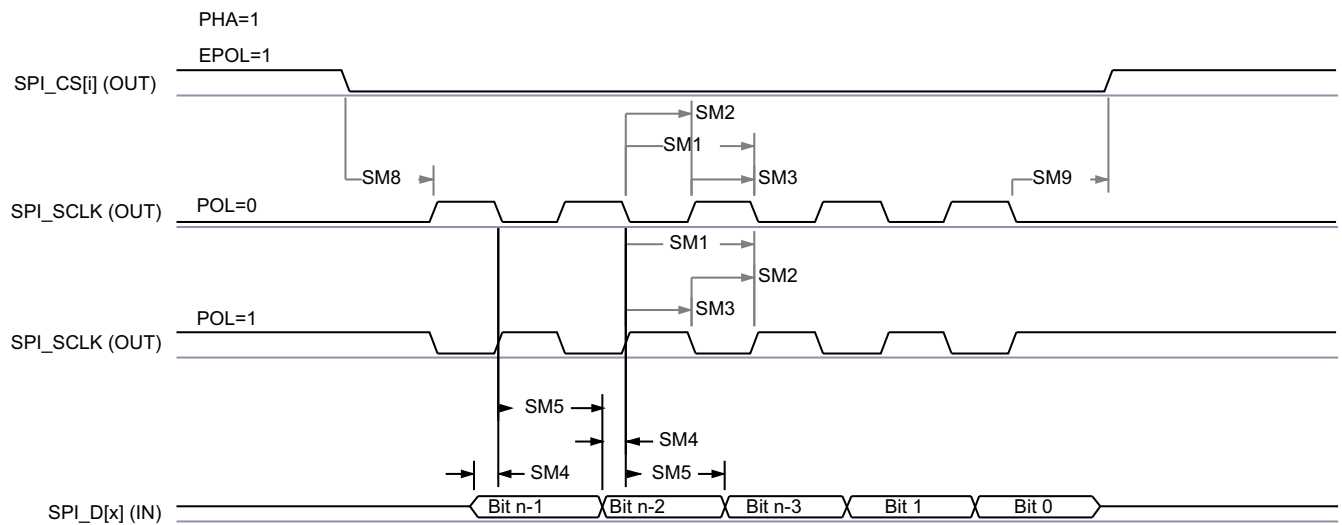
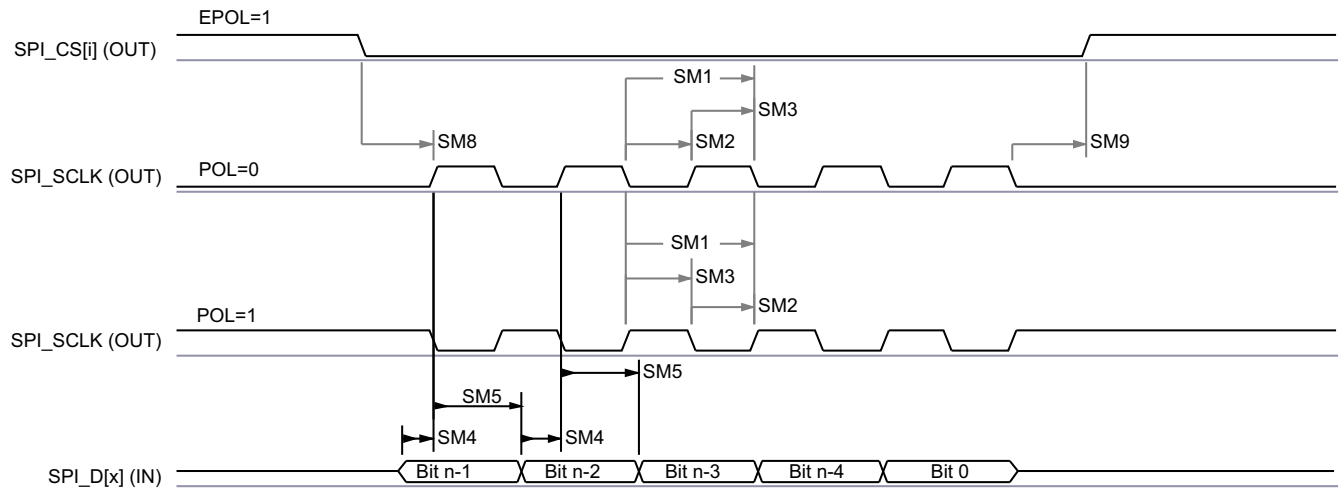
(1) P = SPI\_CLK period in ns

(2) SPI\_CLK phase is programmable with the PHA bit of the MCSPI\_CHCONF\_0/1/2/3 register

(3) B = (TCS + .5) \* TSPICKREF, where TCSns a bit field of the MCSPI\_CHCONF\_0/1/2/3 register and Fratio = Even >= 2.

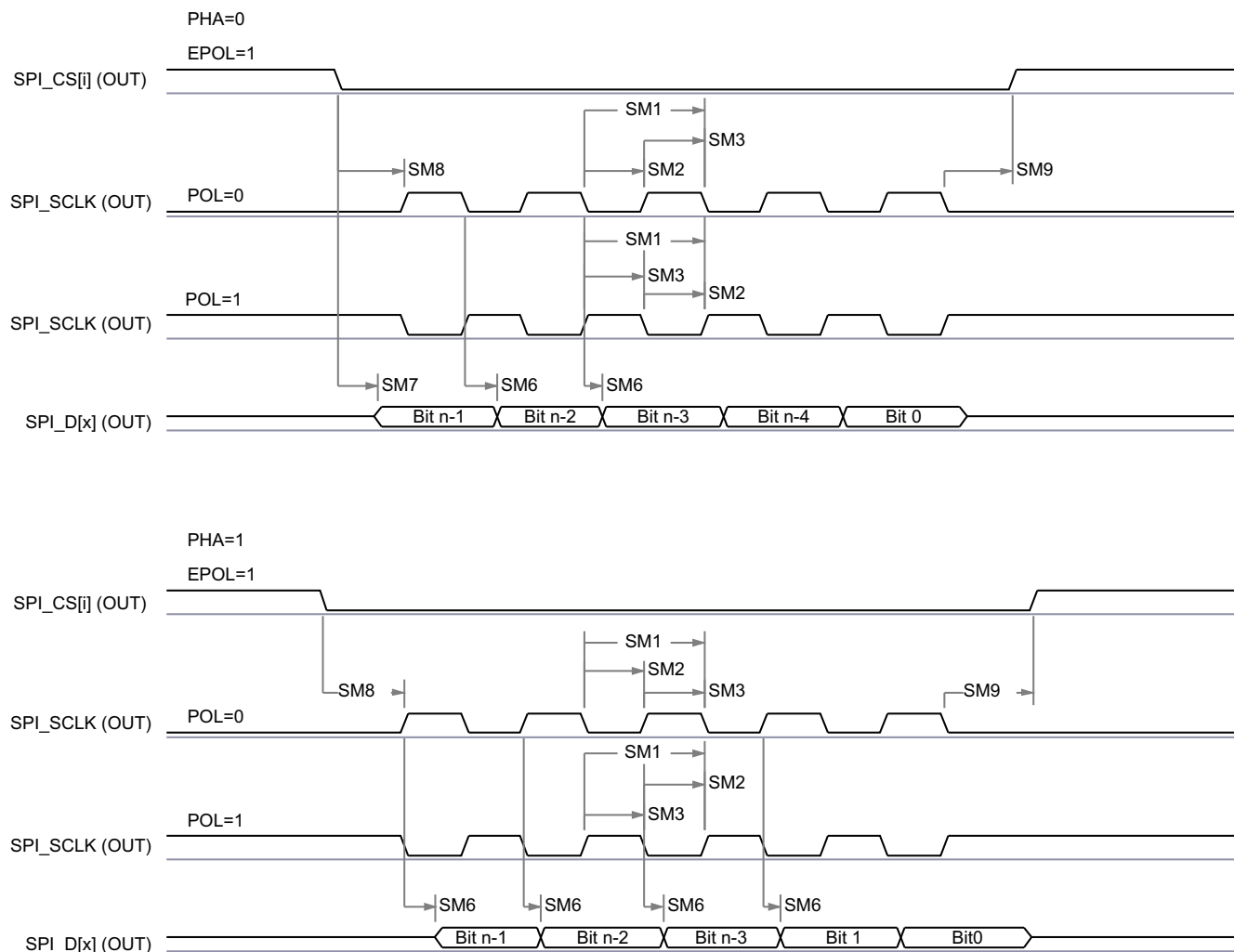
(4) When P = 20.8 ns, A = (TCS + 1) \* TSPICKREF, where TCSns a bit field of the MCSPI\_CHCONF\_0/1/2/3 register.

When  $P > 20.8 \text{ ns}$ ,  $A = (TCS + 0.5) * Fratio * TSPICLKREF$ , where TCSns a bit field of the MCSPI\_CHCONF\_0/1/2/3 register.  
PHA=0



SPRSP08\_TIMING\_McSPI\_02

**Figure 6-73. SPI Controller Mode Receive Timing**



SPRSP08\_TIMING\_McSPI\_01

**Figure 6-74. MCSPI Controller Mode Transmit Timing****6.10.5.16.2 MCSPI — Peripheral Mode**

Table 6-53, Table 6-54, Figure 6-75, and Figure 6-76 present timing requirements and switching characteristics for MCSPI – Peripheral Mode.

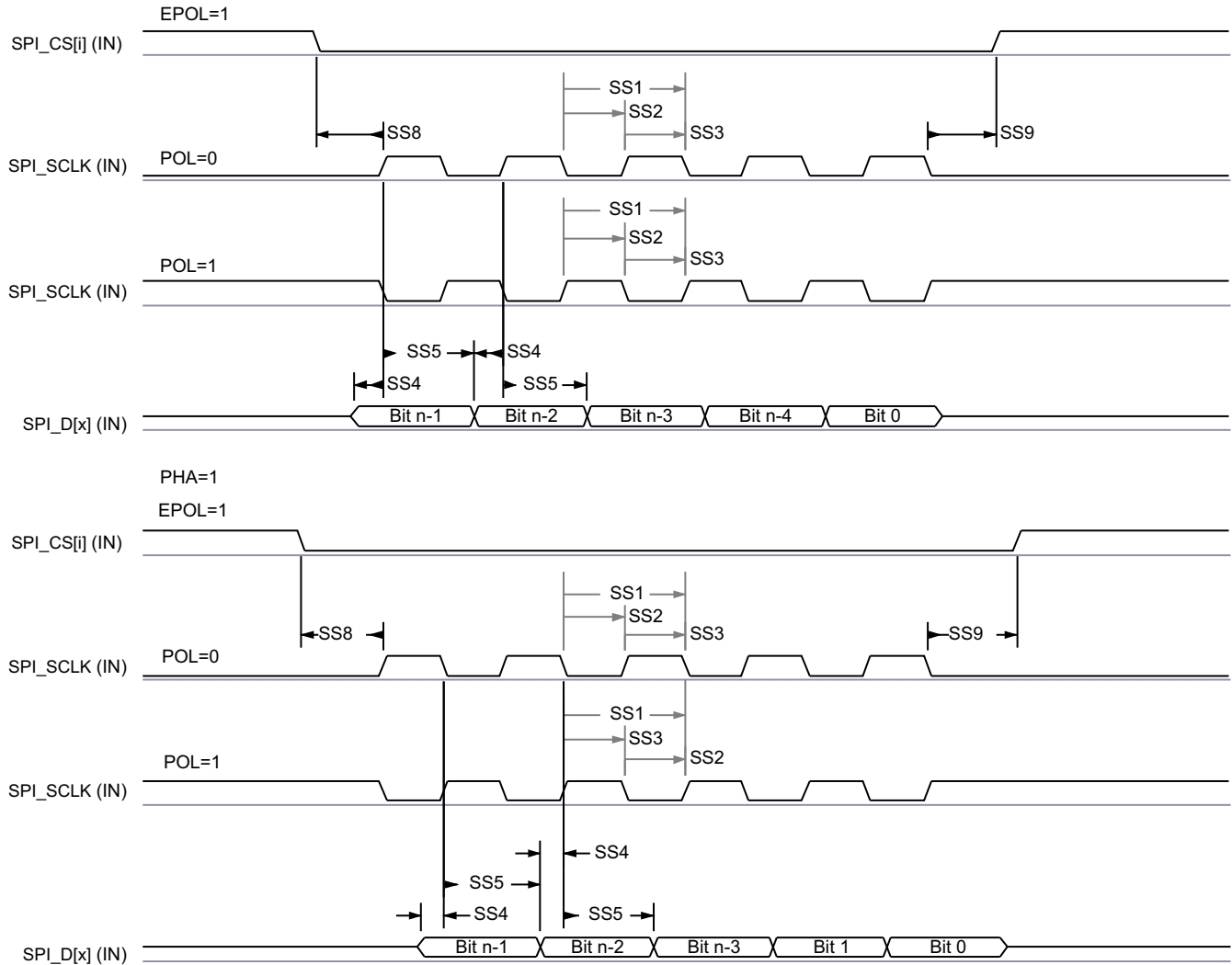
**Table 6-53. MCSPI Timing Requirements - Peripheral Mode**

| NO. | PARAMETER              | DESCRIPTION                                           | MODE | MIN                  | MAX | UNIT |
|-----|------------------------|-------------------------------------------------------|------|----------------------|-----|------|
| SS1 | $t_{c(spclk)}$         | Cycle time, SPI_CLK                                   |      | 20                   |     | ns   |
| SS2 | $t_{w(spclkL)}$        | Pulse duration, SPI_CLK low                           |      | 0.45P <sup>(1)</sup> |     | ns   |
| SS3 | $t_{w(spclkH)}$        | Pulse duration, SPI_CLK high                          |      | 0.45P <sup>(1)</sup> |     | ns   |
| SS4 | $t_{su(simoV-spclkV)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge |      | 5                    |     | ns   |
| SS5 | $t_{h(spclkV-simoV)}$  | Hold time, SPI_D[x] valid after SPI_CLK active edge   |      | 5                    |     | ns   |
| SS8 | $t_{su(csV-spclkV)}$   | Setup time, SPI_CSi valid before SPI_CLK first edge   |      | 5                    |     | ns   |
| SS9 | $t_{h(spclkV-csV)}$    | Hold time, SPI_CSi valid after SPI_CLK last edge      |      | 5                    |     | ns   |

**Table 6-54. MCSPI Switching Characteristics - Peripheral Mode**

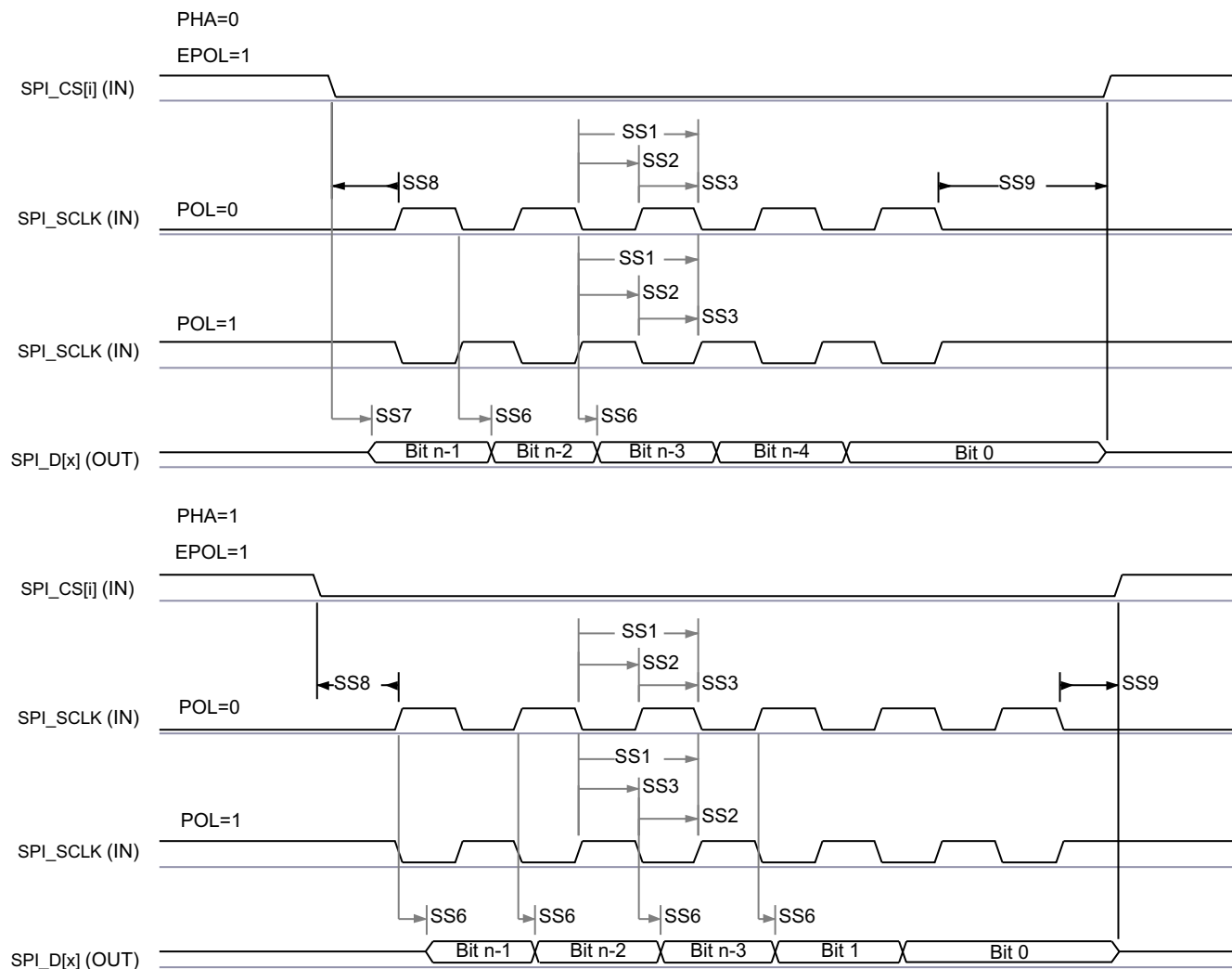
| NO. | PARAMETER              | DESCRIPTION                                            | MIN   | MAX   | UNIT |
|-----|------------------------|--------------------------------------------------------|-------|-------|------|
| SS6 | $t_{d(spiclkV-somIV)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition | 2     | 17.12 | ns   |
| SS7 | $t_{sk(csV-somIV)}$    | Delay time, SPI_CSi active edge to SPI_D[x] transition | 20.95 |       | ns   |

(1) P = SPI\_CLK period in ns.  
PHA=0  
EPOL=1



SPRSP08\_TIMING\_McSPI\_04

**Figure 6-75. SPI Peripheral Mode Receive Timing**



SPRSP08\_TIMING\_McSPI\_03

**Figure 6-76. MCSPI Peripheral Mode Transmit Timing**

Table 6-55 and Table 6-56 present the specific groupings of signals (IOSET) for use with MCU\_SPI0 and MCU\_SPI1.

**Table 6-55. MCU\_SPI0 IOSETs**

| Signals      | IOSET1         |     | IOSET2        |     |
|--------------|----------------|-----|---------------|-----|
|              | BALL NAME      | MUX | BALL NAME     | MUX |
| MCU_SPI0_CLK | MCU_SPI0_CLK   | 0   | MCU_SPI0_CLK  | 0   |
| MCU_SPI0_D0  | MCU_SPI0_D0    | 0   | MCU_SPI0_D0   | 0   |
| MCU_SPI0_D1  | MCU_SPI0_D1    | 0   | MCU_SPI0_D1   | 0   |
| MCU_SPI0_CS0 | MCU_SPI0_CS0   | 0   | MCU_SPI0_CS0  | 0   |
| MCU_SPI0_CS1 | MCU_OSP11_D3   | 5   | WKUP_GPIO0_12 | 1   |
| MCU_SPI0_CS2 | MCU_OSP11_CSn1 | 5   | WKUP_GPIO0_14 | 1   |

**Table 6-56. MCU\_SPI1 IOSET**

| Signals      | IOSET1       |     | IOSET2        |     |
|--------------|--------------|-----|---------------|-----|
|              | BALL NAME    | MUX | BALL NAME     | MUX |
| MCU_SPI1_CLK | MCU_SPI1_CLK | 0   | MCU_SPI1_CLK  | 0   |
| MCU_SPI1_D0  | MCU_SPI1_D0  | 0   | MCU_SPI1_D0   | 0   |
| MCU_SPI1_D1  | MCU_SPI1_D1  | 0   | MCU_SPI1_D1   | 0   |
| MCU_SPI1_CS0 | MCU_SPI1_CS0 | 0   | MCU_SPI1_CS0  | 0   |
| MCU_SPI1_CS1 | MCU_OSPI1_D1 | 5   | WKUP_GPIO0_13 | 1   |
| MCU_SPI1_CS2 | MCU_OSPI1_D2 | 5   | WKUP_GPIO0_15 | 1   |

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.17 MMCSd

The MMCSd Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSd Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSd interfaces, see the corresponding MMC0, MMC1, and MMC2 sections within [Signal Descriptions](#) and *Detailed Description*.

#### Note

Some operating modes require software configuration of the MMC DLL delay settings, as shown in [Table 6-57](#) and [Table 6-68](#).

For more information, see *Multi-Media Card/Secure Digital (MMCSd) Interface* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.17.1 MMC0 - eMMC Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and it supports the following eMMC applications:

- Legacy speed
- High speed SDR
- High speed DDR
- High Speed HS200
- High Speed HS400

[Table 6-57](#) presents the required DLL software configuration settings for MMC0 timing modes.

**Table 6-57. MMC0 DLL Delay Mapping for All Timing Modes**

| REGISTER NAME        |                                         | MMCSd0_SS_PHY_CTRL_4_REG |                           |                          |                          |                         | MMCSd0_SS_PHY_CTRL_5_REG      |                      |                             |
|----------------------|-----------------------------------------|--------------------------|---------------------------|--------------------------|--------------------------|-------------------------|-------------------------------|----------------------|-----------------------------|
| BIT FIELD            |                                         | [31:24]                  | [20]                      | [15:12]                  | [8]                      | [4:0]                   | [17:16]                       | [10:8]               | [2:0]                       |
| BIT FIELD NAME       |                                         | STRBSEL                  | OTAPDLYENA                | OTAPDLYSEL               | ITAPDLYENA               | ITAPDLYSEL              | SELDLYTXCLK<br>SELDLYRXCLK    | FRQSEL               | CLKBUFSEL                   |
| MODE                 | DESCRIPTION                             | STROBE<br>DELAY          | OUTPUT<br>DELAY<br>ENABLE | OUTPUT<br>DELAY<br>VALUE | INPUT<br>DELAY<br>ENABLE | INPUT<br>DELAY<br>VALUE | DLL/<br>DELAY CHAIN<br>SELECT | DLL REF<br>FREQUENCY | DELAY<br>BUFFER<br>DURATION |
| Legacy<br>SDR        | 8-bit PHY<br>operating 1.8 V,<br>25 MHz | 0x0                      | 0x0                       | NA                       | 0x1                      | 0x10                    | 0x1                           | 0x0                  | 0x7                         |
| High<br>Speed<br>SDR | 8-bit PHY<br>operating 1.8 V,<br>50 MHz | 0x0                      | 0x0                       | NA                       | 0x1                      | 0xA                     | 0x1                           | 0x0                  | 0x7                         |

**Table 6-57. MMC0 DLL Delay Mapping for All Timing Modes (continued)**

| REGISTER NAME        |                                          | MMCS0_SS_PHY_CTRL_4_REG |                           |                          |                          |                         | MMCS0_SS_PHY_CTRL_5_REG       |                      |                             |
|----------------------|------------------------------------------|-------------------------|---------------------------|--------------------------|--------------------------|-------------------------|-------------------------------|----------------------|-----------------------------|
| BIT FIELD            |                                          | [31:24]                 | [20]                      | [15:12]                  | [8]                      | [4:0]                   | [17:16]                       | [10:8]               | [2:0]                       |
| BIT FIELD NAME       |                                          | STRBSEL                 | OTAPDLYENA                | OTAPDLYSEL               | ITAPDLYENA               | ITAPDLYSEL              | SELDLYTXCLK<br>SELDLYRXCLK    | FRQSEL               | CLKBUFSEL                   |
| MODE                 | DESCRIPTION                              | STROBE<br>DELAY         | OUTPUT<br>DELAY<br>ENABLE | OUTPUT<br>DELAY<br>VALUE | INPUT<br>DELAY<br>ENABLE | INPUT<br>DELAY<br>VALUE | DLL/<br>DELAY CHAIN<br>SELECT | DLL REF<br>FREQUENCY | DELAY<br>BUFFER<br>DURATION |
| High<br>Speed<br>DDR | 8-bit PHY<br>operating 1.8 V,<br>50 MHz  | 0x0                     | 0x1                       | 0x6                      | 0x1                      | Tuning                  | 0x0                           | 0x4                  | 0x7                         |
| HS200                | 8-bit PHY<br>operating 1.8 V,<br>200 MHz | 0x0                     | 0x1                       | 0x8                      | 0x1                      | Tuning                  | 0x0                           | 0x0                  | 0x7                         |
| HS400                | 8-bit PHY<br>operating 1.8 V,<br>200 MHz | 0x66                    | 0x1                       | 0x5                      | 0x1                      | Tuning                  | 0x0                           | 0x0                  | 0x7                         |

Table 6-58 presents timing conditions for MMC0.

**Table 6-58. MMC0 Timing Conditions**

| PARAMETER                             |                                              |                                            | MIN  | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|--------------------------------------------|------|------|------|
| INPUT CONDITIONS                      |                                              |                                            |      |      |      |
| SR <sub>I</sub>                       | Input slew rate                              | Legacy SDR                                 | 0.14 | 1.44 | V/ns |
|                                       |                                              | High Speed SDR                             | 0.3  | 0.90 | V/ns |
|                                       |                                              | High Speed DDR (CMD)                       | 0.3  | 0.90 | V/ns |
|                                       |                                              | High Speed DDR (DAT[7:0])                  | 0.45 | 0.90 | V/ns |
| OUTPUT CONDITIONS                     |                                              |                                            |      |      |      |
| C <sub>L</sub>                        | Output load capacitance                      | HS200, HS400                               | 1    | 6    | pF   |
|                                       |                                              | All other modes                            | 1    | 12   | pF   |
| PCB CONNECTIVITY REQUIREMENTS         |                                              |                                            |      |      |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | All modes                                  | 134  | 756  | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | Legacy SDR, High Speed SDR, High Speed DDR |      | 100  | ps   |
|                                       |                                              | HS200, HS400                               |      | 8    | ps   |

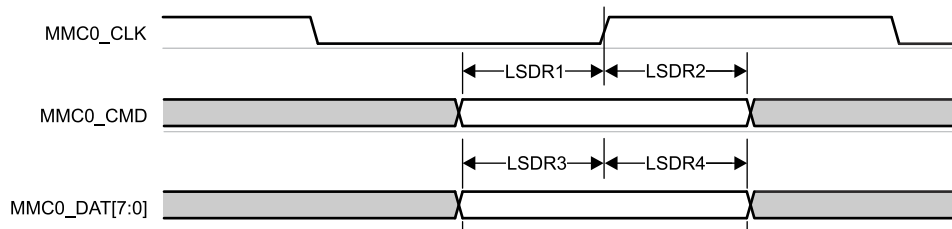
#### 6.10.5.17.1.1 Legacy SDR Mode

Table 6-59, Figure 6-77, Table 6-60, and Figure 6-78 present timing requirements and switching characteristics for MMC0 – Legacy SDR Mode.

**Table 6-59. MMC0 Timing Requirements – Legacy SDR Mode**

see Figure 6-77

| NO.   |                     |                                                             | MIN | MAX | UNIT |
|-------|---------------------|-------------------------------------------------------------|-----|-----|------|
| LSDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge      | 2.5 |     | ns   |
| LSDR2 | $t_{h(clkH-cmdV)}$  | Hold time, MMC0_CMD valid after MMC0_CLK rising edge        | 6.5 |     | ns   |
| LSDR3 | $t_{su(dV-clkH)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge | 2.5 |     | ns   |
| LSDR4 | $t_{h(clkH-dV)}$    | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge   | 6.5 |     | ns   |

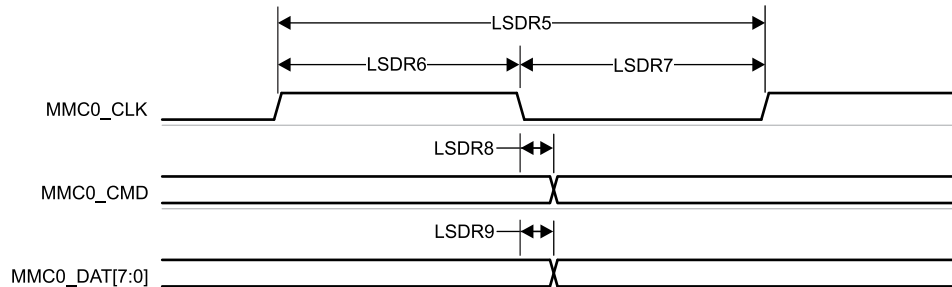


**Figure 6-77. MMC0 – Legacy SDR – Receive Mode**

**Table 6-60. MMC0 Switching Characteristics – Legacy SDR Mode**

see Figure 6-78

| NO.   |                    | PARAMETER                                                     | MIN  | MAX | UNIT |
|-------|--------------------|---------------------------------------------------------------|------|-----|------|
|       | $f_{op(clk)}$      | Operating frequency, MMC0_CLK                                 |      | 25  | MHz  |
| LSDR5 | $t_{c(clk)}$       | Cycle time, MMC0_CLK                                          | 40   |     | ns   |
| LSDR6 | $t_{w(clkH)}$      | Pulse duration, MMC0_CLK high                                 | 18.7 |     | ns   |
| LSDR7 | $t_{w(clkL)}$      | Pulse duration, MMC0_CLK low                                  | 18.7 |     | ns   |
| LSDR8 | $t_{d(clkL-cmdV)}$ | Delay time, MMC0_CLK falling edge to MMC0_CMD transition      | –3.2 | 3.8 | ns   |
| LSDR9 | $t_{d(clkL-dV)}$   | Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition | –3.2 | 3.8 | ns   |



**Figure 6-78. MMC0 – Legacy SDR – Transmit Mode**

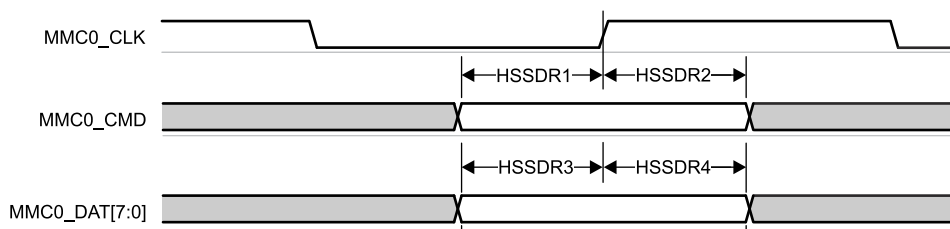
### 6.10.5.17.1.2 High Speed SDR Mode

Table 6-61, Figure 6-79, Table 6-62, and Figure 6-80 present timing requirements and switching characteristics for MMC0 – High Speed SDR Mode.

**Table 6-61. MMC0 Timing Requirements – High Speed SDR Mode**

see Figure 6-79

| NO.    |                     |                                                             | MIN  | MAX | UNIT |
|--------|---------------------|-------------------------------------------------------------|------|-----|------|
| HSSDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge      | 2.99 |     | ns   |
| HSSDR2 | $t_h(clkH-cmdV)$    | Hold time, MMC0_CMD valid after MMC0_CLK rising edge        | 2.67 |     | ns   |
| HSSDR3 | $t_{su(dV-clkH)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge | 2.99 |     | ns   |
| HSSDR4 | $t_h(clkH-dV)$      | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge   | 2.67 |     | ns   |

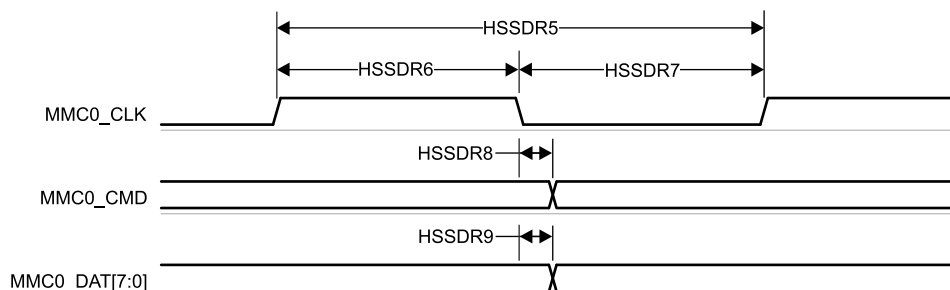


**Figure 6-79. MMC0 – High Speed SDR Mode – Receive Mode**

**Table 6-62. MMC0 Switching Characteristics – High Speed SDR Mode**

see Figure 6-80

| NO.    |                  | PARAMETER                                                     | MIN  | MAX | UNIT |
|--------|------------------|---------------------------------------------------------------|------|-----|------|
|        | $f_{op(clk)}$    | Operating frequency, MMC0_CLK                                 |      | 50  | MHz  |
| HSSDR5 | $t_c(clk)$       | Cycle time, MMC0_CLK                                          | 20   |     | ns   |
| HSSDR6 | $t_w(clkH)$      | Pulse duration, MMC0_CLK high                                 | 9.2  |     | ns   |
| HSSDR7 | $t_w(clkL)$      | Pulse duration, MMC0_CLK low                                  | 9.2  |     | ns   |
| HSSDR8 | $t_d(clkL-cmdV)$ | Delay time, MMC0_CLK falling edge to MMC0_CMD transition      | –3.2 | 3.8 | ns   |
| HSSDR9 | $t_d(clkL-dV)$   | Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition | –3.2 | 3.8 | ns   |



**Figure 6-80. MMC0 – High Speed SDR Mode – Transmit Mode**

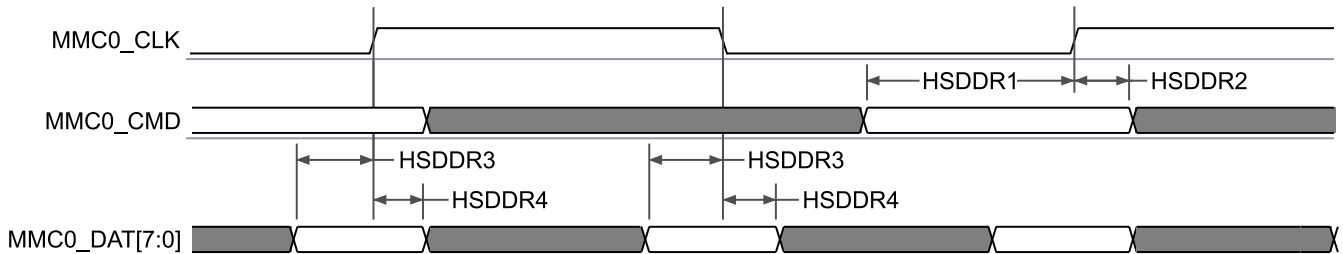
### 6.10.5.17.1.3 High Speed DDR Mode

Table 6-63, Figure 6-81, Table 6-64, and Figure 6-82 present timing requirements and switching characteristics for MMC0 – High Speed DDR Mode.

**Table 6-63. MMC0 Timing Requirements – High Speed DDR Mode**

see Figure 6-81

| NO.    |                     |                                                            | MIN  | MAX | UNIT |
|--------|---------------------|------------------------------------------------------------|------|-----|------|
| HSDDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge     | 3.79 |     | ns   |
| HSDDR2 | $t_h(clkH-cmdV)$    | Hold time, MMC0_CMD valid after MMC0_CLK rising edge       | 2.67 |     | ns   |
| HSDDR3 | $t_{su(dV-clkV)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition | 0.74 |     | ns   |
| HSDDR4 | $t_h(clkV-dV)$      | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition   | 1.67 |     | ns   |

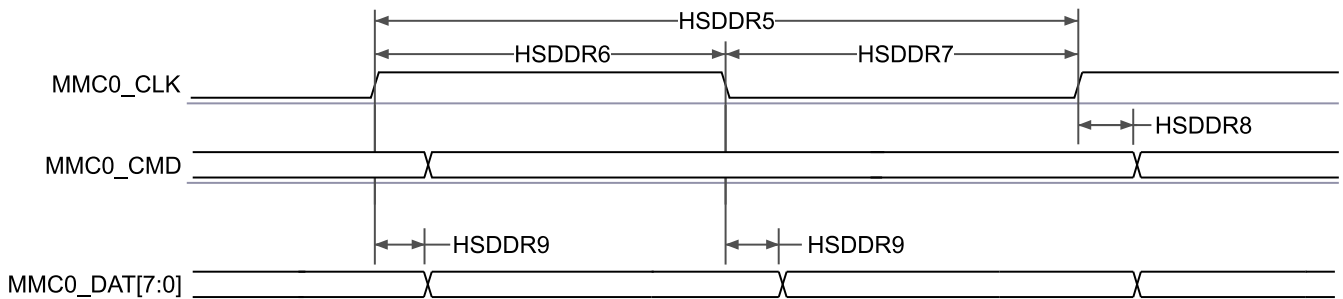


**Figure 6-81. MMC0 – High Speed DDR Mode – Receive Mode**

**Table 6-64. MMC0 Switching Characteristics – High Speed DDR Mode**

see Figure 6-82

| NO.    |                  | PARAMETER                                                   | MIN | MAX  | UNIT |
|--------|------------------|-------------------------------------------------------------|-----|------|------|
|        | $f_{op(clk)}$    | Operating frequency, MMC0_CLK                               |     | 50   | MHz  |
| HSDDR5 | $t_c(clk)$       | Cycle time, MMC0_CLK                                        | 20  |      | ns   |
| HSDDR6 | $t_w(clkH)$      | Pulse duration, MMC0_CLK high                               | 9.2 |      | ns   |
| HSDDR7 | $t_w(clkL)$      | Pulse duration, MMC0_CLK low                                | 9.2 |      | ns   |
| HSDDR8 | $t_d(clkH-cmdV)$ | Delay time, MMC0_CLK rising edge to MMC0_CMD transition     | 3.4 | 9.8  | ns   |
| HSDDR9 | $t_d(clkV-dV)$   | Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition | 2.9 | 6.85 | ns   |



**Figure 6-82. MMC0 – High Speed DDR Mode – Transmit Mode**

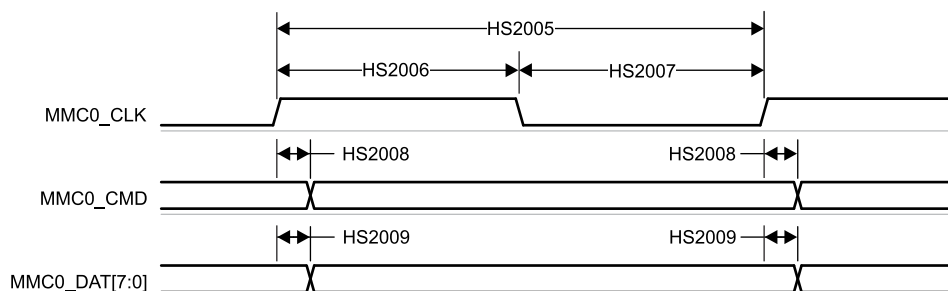
#### 6.10.5.17.1.4 HS200 Mode

Table 6-65 and Figure 6-83 present switching characteristics for MMC0 – HS200 Mode.

**Table 6-65. MMC0 Switching Characteristics – HS200 Mode**

see Figure 6-83

| NO.    | PARAMETER        |                                                              | MIN  | MAX  | UNIT |
|--------|------------------|--------------------------------------------------------------|------|------|------|
|        | $f_{op}(clk)$    | Operating frequency, MMC0_CLK                                |      | 200  | MHz  |
| HS2005 | $t_c(clk)$       | Cycle time, MMC0_CLK                                         | 5    |      | ns   |
| HS2006 | $t_w(clkH)$      | Pulse duration, MMC0_CLK high                                | 2.08 |      | ns   |
| HS2007 | $t_w(clkL)$      | Pulse duration, MMC0_CLK low                                 | 2.08 |      | ns   |
| HS2008 | $t_d(clkL-cmdV)$ | Delay time, MMC0_CLK rising edge to MMC0_CMD transition      | 0.99 | 3.16 | ns   |
| HS2009 | $t_d(clkL-dV)$   | Delay time, MMC0_CLK rising edge to MMC0_DAT[7:0] transition | 0.99 | 3.16 | ns   |



**Figure 6-83. MMC0 – HS200 Mode – Transmit Mode**

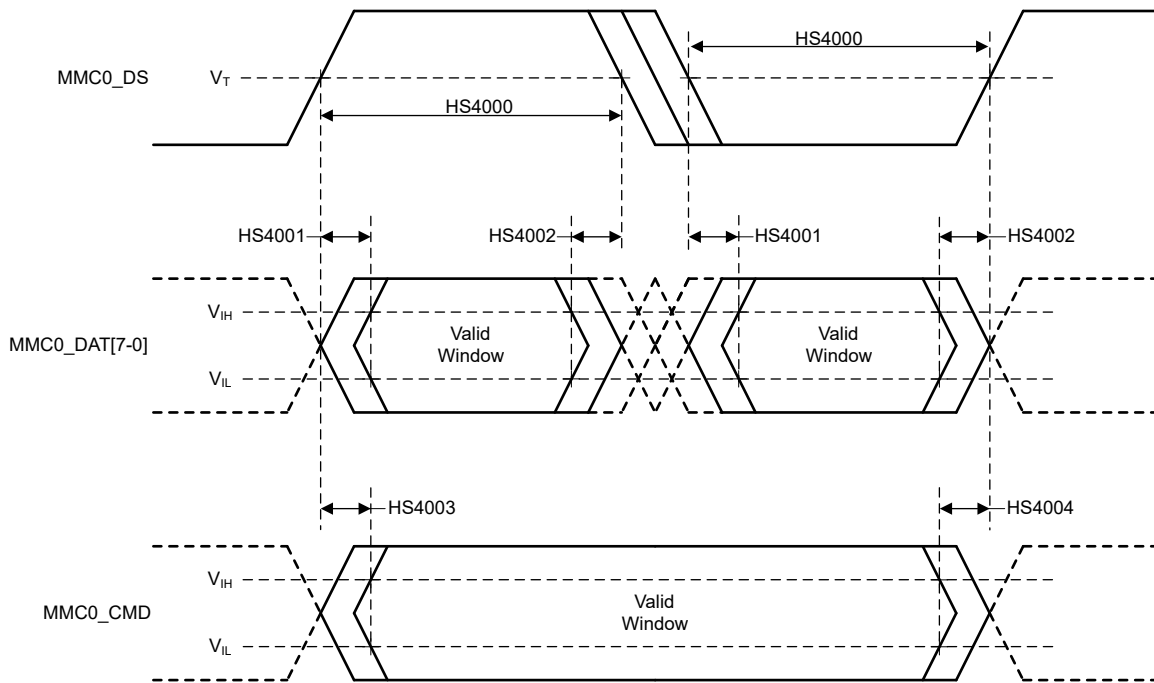
#### 6.10.5.17.1.5 HS400 Mode

Table 6-66, Figure 6-84, Table 6-67, and Figure 6-85 present switching characteristics for MMC0 – HS400 Mode.

**Table 6-66. MMC0 Timing Requirements – HS400 Mode**

see Figure 6-84

| NO.    | PARAMETER      |                                              | MIN  | MAX | UNIT |
|--------|----------------|----------------------------------------------|------|-----|------|
| HS4000 | $t_{DSMPW}$    | Pulse width, MMC0_DS                         | 1.95 |     | ns   |
| HS4001 | $t_{RQ\_DAT}$  | Input skew, MMC0_DS to MMC0_DAT valid        |      | 475 | ps   |
| HS4002 | $t_{RQH\_DAT}$ | Input skew hold, MMC0_DAT invalid to MMC0_DS |      | 475 | ps   |
| HS4003 | $t_{RQ\_CMD}$  | Input skew, MMC0_DS to MMC0_CMD valid        |      | 475 | ps   |
| HS4004 | $t_{RQH\_CMD}$ | Input skew hold, MMC0_CMD invalid to MMC0_DS |      | 475 | ps   |



**Figure 6-84. MMC0 – HS400 – Receive Mode**

**Table 6-67. MMC0 Switching Characteristics – HS400 Mode**

see [Figure 6-85](#)

| NO.    | PARAMETER            | DESCRIPTION                                                                               | MIN  | MAX | UNIT |
|--------|----------------------|-------------------------------------------------------------------------------------------|------|-----|------|
|        | $f_{op}(clk)$        | Operating frequency, MMC0_CLK                                                             |      | 200 | MHz  |
| HS4005 | $t_{c}(clk)$         | Cycle time, MMC0_CLK                                                                      | 5    |     | ns   |
| HS4006 | $t_{w}(clkH)$        | Pulse duration, MMC0_CLK high                                                             | 2.23 |     | ns   |
| HS4007 | $t_{w}(clkL)$        | Pulse duration, MMC0_CLK low                                                              | 2.23 |     | ns   |
| HS4008 | $t_{osu}(cmdV-clkH)$ | Output setup time, MMC0_CMD valid to MMC0_CLK rising edge <sup>(1)</sup>                  | 2.54 |     | ns   |
| HS4009 | $t_{osu}(dV-clk)$    | Output setup time, MMC0_DAT[7:0] valid to MMC0_CLK rising or falling edge <sup>(1)</sup>  | 0.63 |     | ns   |
| HS4010 | $t_{oh}(clkH-cmdIV)$ | Output hold time, MMC0_CLK rising edge to MMC0_CMD invalid <sup>(2)</sup>                 | 0.98 |     | ns   |
| HS4011 | $t_{oh}(clk-dIV)$    | Output hold time, MMC0_CLK rising or falling edge to MMC0_DAT[7:0] invalid <sup>(2)</sup> | 0.72 |     | ns   |

- (1) This parameter defines the output setup time provided to the attached device. This time is relative to the next capture clock edge. The timing references for this parameter are from mid-supply of the DAT or CMD signal transition to mid-supply of the CLK signal transition. The eMMC standard defines the setup timing references from VIL or VIH of the DAT or CMD signal transition to mid-supply of the CLK signal transition. Therefore, the system designer must consider the impact of the DAT signal slew rate when designing the PCB, and ensure the time it takes for the DAT signal to slew from mid-supply to VIL or VIH does not erode the setup time margin.
- (2) This parameter defines the output hold time provided to the attached device. This time is relative to the previous launch clock edge. The timing references for this parameter are from mid-supply of the CLK signal transition to mid-supply of the DAT or CMD signal transition. The eMMC standard defines the hold timing references from mid-supply of the CLK signal transition to VIL or VIH of the DAT or CMD signal transition. Therefore, the system designer must consider the impact of the DAT signal slew rate when designing the PCB, and ensure the time it takes for the DAT signal to slew from VIL or VIH to mid-supply does not erode the hold time margin.

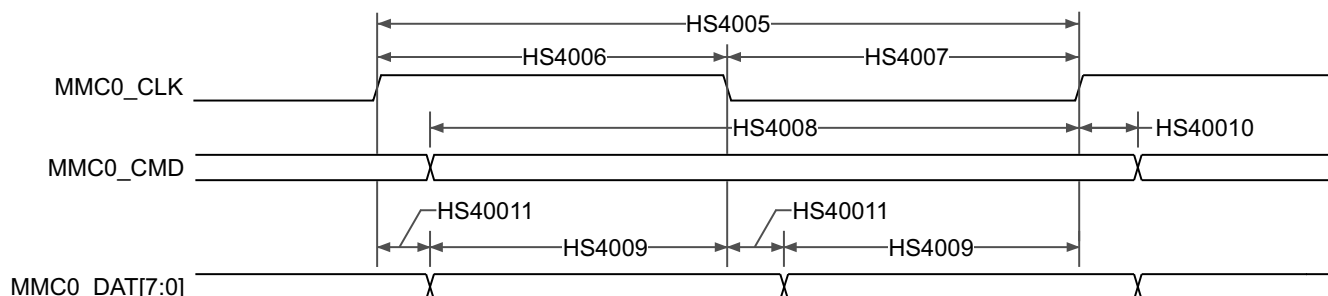


Figure 6-85. eMMC in – HS400 Mode – Transmitter Mode

#### 6.10.5.17.2 MMC1/2 - SD/SDIO Interface

MMC1 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and they support the following SD Card applications:

- Default speed
- High speed
- UHS-I SDR12
- UHS-I SDR25
- UHS-I SDR50
- UHS-I SDR104
- UHS-I DDR50

Table 6-68 presents the required DLL software configuration settings for MMC1 timing modes.

Table 6-68. MMC1 DLL Delay Mapping for All Timing Modes

| REGISTER NAME  |                                    | MMCSD12_SS_PHY_CTRL_4_REG |             |                    |                   | MMCSD12_SS_PHY_CTRL_5_REG |
|----------------|------------------------------------|---------------------------|-------------|--------------------|-------------------|---------------------------|
| BIT FIELD      |                                    | [20]                      | [15:12]     | [8]                | [4:0]             | [2:0]                     |
| BIT FIELD NAME |                                    | OTAPDLYENA                | OTAPDLYSEL  | ITAPDLYENA         | ITAPDLYSEL        | CLKBUFSEL                 |
| MODE           | DESCRIPTION                        | DELAY ENABLE              | DELAY VALUE | INPUT DELAY ENABLE | INPUT DELAY VALUE | DELAY BUFFER DURATION     |
| Default Speed  | 4-bit PHY operating 3.3 V, 25 MHz  | 0x0                       | 0x0         | 0x0                | 0x0               | 0x7                       |
| High Speed     | 4-bit PHY operating 3.3 V, 50 MHz  | 0x0                       | 0x0         | 0x0                | 0x0               | 0x7                       |
| UHS-I SDR12    | 4-bit PHY operating 1.8 V, 25 MHz  | 0x1                       | 0xF         | 0x0                | 0x0               | 0x7                       |
| UHS-I SDR25    | 4-bit PHY operating 1.8 V, 50 MHz  | 0x1                       | 0xF         | 0x0                | 0x0               | 0x7                       |
| UHS-I SDR50    | 4-bit PHY operating 1.8 V, 100 MHz | 0x1                       | 0xC         | 0x1                | Tuning            | 0x7                       |
| UHS-I DR50     | 4-bit PHY operating 1.8 V, 50 MHz  | 0x1                       | 0xC         | 0x1                | 0x2               | 0x7                       |
| UHS-I SDR104   | 4-bit PHY operating 1.8 V, 200 MHz | 0x1                       | 0x5         | 0x1                | Tuning            | 0x7                       |

Table 6-69 presents timing conditions for MMC1.

Table 6-69. MMC1 Timing Conditions

| PARAMETER               |                 |                           | MIN  | MAX  | UNIT |
|-------------------------|-----------------|---------------------------|------|------|------|
| <b>INPUT CONDITIONS</b> |                 |                           |      |      |      |
| SR <sub>I</sub>         | Input slew rate | Default Speed, High Speed | 0.69 | 2.06 | V/ns |
|                         |                 | UHS-I SDR12, UHS-I SDR25  | 0.34 | 1.34 | V/ns |
|                         |                 | UHS-I DDR50               | 1.00 | 2.00 | V/ns |

**Table 6-69. MMC1 Timing Conditions (continued)**

| PARAMETER                            |                                              |                 | MIN    | MAX  | UNIT |
|--------------------------------------|----------------------------------------------|-----------------|--------|------|------|
| <b>OUTPUT CONDITIONS</b>             |                                              |                 |        |      |      |
| $C_L$                                | Output load capacitance                      | All modes       | 1      | 10   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |                                              |                 |        |      |      |
| $t_d$ (Trace Delay)                  | Propagation delay of each trace              | UHS-I DDR50     | 240.03 | 1134 | ps   |
|                                      |                                              | All other modes | 126    | 1386 | ps   |
| $t_d$ (Trace Mismatch Delay)         | Propagation delay mismatch across all traces | UHS-I DDR50     |        | 20   | ps   |
|                                      |                                              | UHS-I SDR104    |        | 8    | ps   |
|                                      |                                              | All other modes |        | 100  | ps   |

### 6.10.5.17.2.1 Default Speed Mode

Table 6-70, Figure 6-86, Table 6-71, and Figure 6-87 present timing requirements and switching characteristics for MMC1/2 – Default Speed Mode.

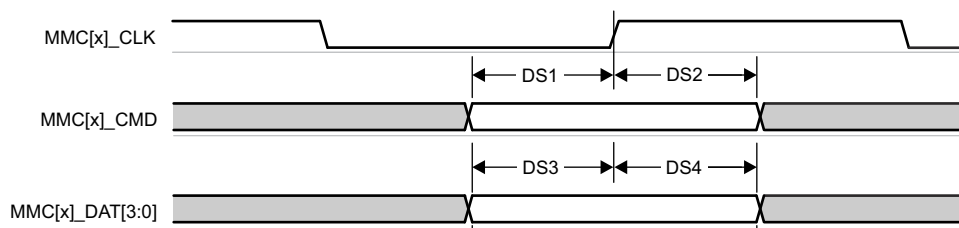
**Table 6-70. MMC1/2 Timing Requirements – Default Speed Mode**

see Figure 6-86

| NO. |                     |                                                                 | MIN  | MAX | UNIT |
|-----|---------------------|-----------------------------------------------------------------|------|-----|------|
| DS1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 2.15 |     | ns   |
| DS2 | $t_h(clkH-cmdV)$    | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 4.56 |     | ns   |
| DS3 | $t_{su(dV-clkH)}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 2.15 |     | ns   |
| DS4 | $t_h(clkH-dV)$      | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 4.56 |     | ns   |

A. x = 1, 2 for MMC1 and MMC2

B. x = 1, 2 for MMC1 and MMC2



**Figure 6-86. MMC1/2 – Default Speed – Receive Mode**

**Table 6-71. MMC1/2 Switching Characteristics – Default Speed Mode**

see Figure 6-87

| NO. |                  | PARAMETER                                                         | MIN   | MAX  | UNIT |
|-----|------------------|-------------------------------------------------------------------|-------|------|------|
|     | $f_{op(clk)}$    | Operating frequency, MMC[x]_CLK                                   |       | 25   | MHz  |
| DS5 | $t_c(clk)$       | Cycle time, MMC[x]_CLK                                            | 40    |      | ns   |
| DS6 | $t_w(clkH)$      | Pulse duration, MMC[x]_CLK high                                   | 18.7  |      | ns   |
| DS7 | $t_w(clkL)$      | Pulse duration, MMC[x]_CLK low                                    | 18.7  |      | ns   |
| DS8 | $t_d(clkL-cmdV)$ | Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition      | –3.53 | 3.53 | ns   |
| DS9 | $t_d(clkL-dV)$   | Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition | –3.53 | 3.53 | ns   |



**Figure 6-87. MMC1/2 – Default Speed – Transmit Mode**

#### 6.10.5.17.2.2 High Speed Mode

Table 6-72, Figure 6-88, Table 6-73, and Figure 6-89 present timing requirements and switching characteristics for MMC1/2 – High Speed Mode.

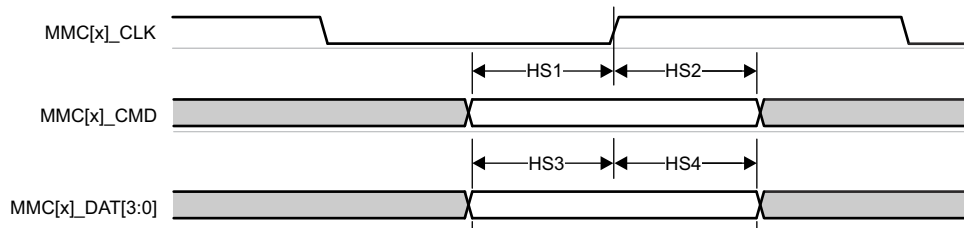
**Table 6-72. MMC1/2 Timing Requirements – High Speed Mode**

see Figure 6-88

| NO. |                     |                                                                 | MIN  | MAX | UNIT |
|-----|---------------------|-----------------------------------------------------------------|------|-----|------|
| HS1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 2.15 |     | ns   |
| HS2 | $t_{h(clkH-cmdV)}$  | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 2.26 |     | ns   |
| HS3 | $t_{su(dV-clkH)}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 2.15 |     | ns   |
| HS4 | $t_{h(clkH-dV)}$    | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 2.26 |     | ns   |

A. x = 1, 2 for MMC1 and MMC2

B. x = 1, 2 for MMC1 and MMC2

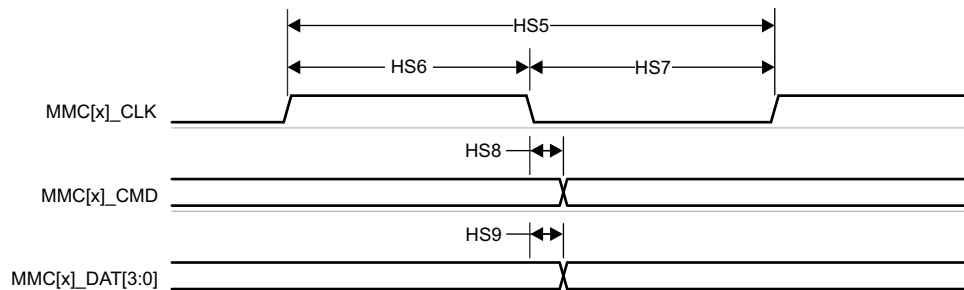


**Figure 6-88. MMC1 /2– High Speed – Receive Mode**

**Table 6-73. MMC1/2 Switching Characteristics – High Speed Mode**

see Figure 6-89

| NO. |                    | PARAMETER                                                         | MIN   | MAX  | UNIT |
|-----|--------------------|-------------------------------------------------------------------|-------|------|------|
|     | $f_{op(clk)}$      | Operating frequency, MMC[x]_CLK                                   |       | 50   | MHz  |
| HS5 | $t_{c(clk)}$       | Cycle time, MMC[x]_CLK                                            | 20    |      | ns   |
| HS6 | $t_{w(clkH)}$      | Pulse duration, MMC[x]_CLK high                                   | 9.2   |      | ns   |
| HS7 | $t_{w(clkL)}$      | Pulse duration, MMC[x]_CLK low                                    | 9.2   |      | ns   |
| HS8 | $t_{d(clkL-cmdV)}$ | Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition      | –2.07 | 2.07 | ns   |
| HS9 | $t_{d(clkL-dV)}$   | Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition | –2.07 | 2.07 | ns   |



**Figure 6-89. MMC1/2 – High Speed – Transmit Mode**

### 6.10.5.17.2.3 UHS-I SDR12 Mode

Table 6-74, Figure 6-90, Table 6-75, and Figure 6-91 present timing requirements and switching characteristics for MMC1/2 – UHS-I SDR12 Mode.

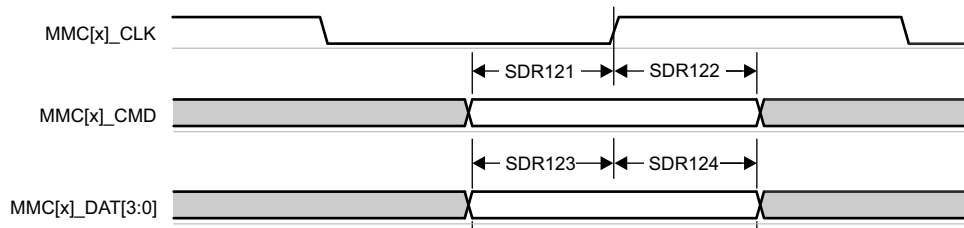
**Table 6-74. MMC1/2 Timing Requirements – UHS-I SDR12 Mode**

see Figure 6-90

| NO.    |                     |                                                                 | MIN  | MAX | UNIT |
|--------|---------------------|-----------------------------------------------------------------|------|-----|------|
| SDR121 | $t_{su(cmdV-clkH)}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 5.46 |     | ns   |
| SDR122 | $t_{h(clkH-cmdV)}$  | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 1.67 |     | ns   |
| SDR123 | $t_{su(dV-clkH)}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 5.46 |     | ns   |
| SDR124 | $t_{h(clkH-dV)}$    | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 1.67 |     | ns   |

A. x = 1, 2 for MMC1 and MMC2

B. x = 1, 2 for MMC1 and MMC2

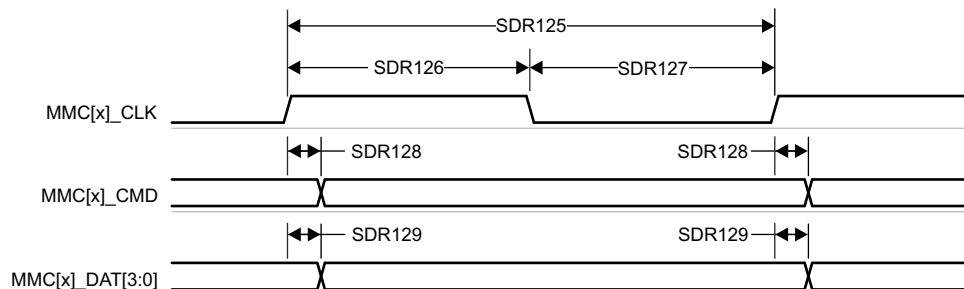


**Figure 6-90. MMC1/2 – UHS-I SDR12 – Receive Mode**

**Table 6-75. MMC1/2 Switching Characteristics – UHS-I SDR12 Mode**

see Figure 6-91

| NO.    |                    | PARAMETER                                                        | MIN  | MAX   | UNIT |
|--------|--------------------|------------------------------------------------------------------|------|-------|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC[x]_CLK                                  |      | 25    | MHz  |
| SDR125 | $t_{c(clk)}$       | Cycle time, MMC[x]_CLK                                           | 40   |       | ns   |
| SDR126 | $t_{w(clkH)}$      | Pulse duration, MMC[x]_CLK high                                  | 18.7 |       | ns   |
| SDR127 | $t_{w(clkL)}$      | Pulse duration, MMC[x]_CLK low                                   | 18.7 |       | ns   |
| SDR128 | $t_{d(clkH-cmdV)}$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 1.2  | 13.55 | ns   |
| SDR129 | $t_{d(clkH-dV)}$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 1.2  | 13.55 | ns   |



**Figure 6-91. MMC1/2 – UHS-I SDR12 – Transmit Mode**

#### 6.10.5.17.2.4 UHS-I SDR25 Mode

Table 6-76, Figure 6-92, Table 6-77, and Figure 6-93 present timing requirements and switching characteristics for MMC1/2 – UHS-I SDR25 Mode.

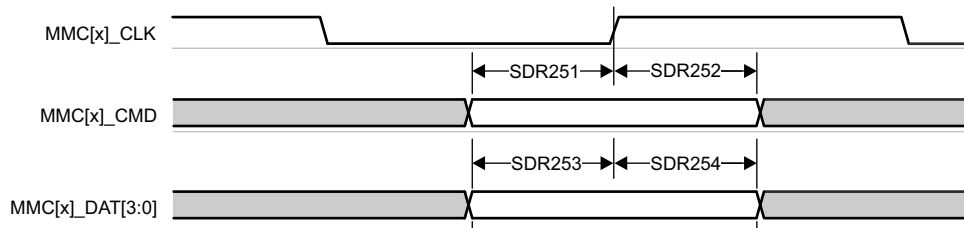
**Table 6-76. MMC1/2 Timing Requirements – UHS-I SDR25 Mode**

see Figure 6-92

| NO.    |                     |                                                                 | MIN  | MAX | UNIT |
|--------|---------------------|-----------------------------------------------------------------|------|-----|------|
| SDR251 | $t_{su(cmdV-clkH)}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 2.1  |     | ns   |
| SDR252 | $t_{h(clkH-cmdV)}$  | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 1.67 |     | ns   |
| SDR253 | $t_{su(dV-clkH)}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 2.1  |     | ns   |
| SDR254 | $t_{h(clkH-dV)}$    | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 1.67 |     | ns   |

A. x = 1, 2 for MMC1 and MMC2

B. x = 1, 2 for MMC1 and MMC2

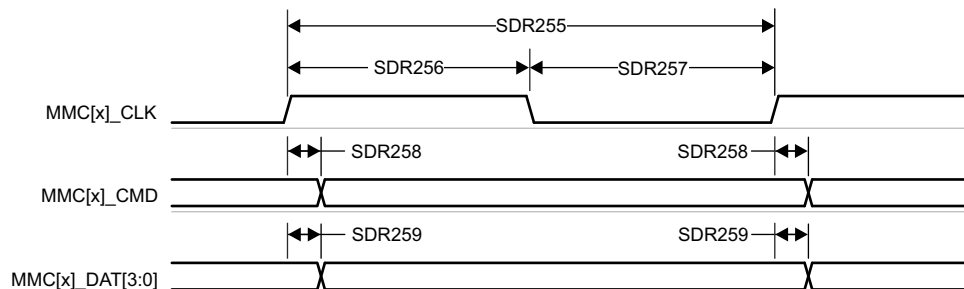


**Figure 6-92. MMC1/2 – UHS-I SDR25 – Receive Mode**

**Table 6-77. MMC1/2 Switching Characteristics – UHS-I SDR25 Mode**

see Figure 6-93

| NO.    |                    | PARAMETER                                                        | MIN | MAX  | UNIT |
|--------|--------------------|------------------------------------------------------------------|-----|------|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC[x]_CLK                                  |     | 50   | MHz  |
| SDR255 | $t_{c(clk)}$       | Cycle time, MMC[x]_CLK                                           | 20  |      | ns   |
| SDR256 | $t_{w(clkH)}$      | Pulse duration, MMC[x]_CLK high                                  | 9.2 |      | ns   |
| SDR257 | $t_{w(clkL)}$      | Pulse duration, MMC[x]_CLK low                                   | 9.2 |      | ns   |
| SDR258 | $t_{d(clkH-cmdV)}$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 2.4 | 9.37 | ns   |
| SDR259 | $t_{d(clkH-dV)}$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 2.4 | 9.37 | ns   |



**Figure 6-93. MMC1/2 – UHS-I SDR25 – Transmit Mode**

### 6.10.5.17.2.5 UHS-I SDR50 Mode

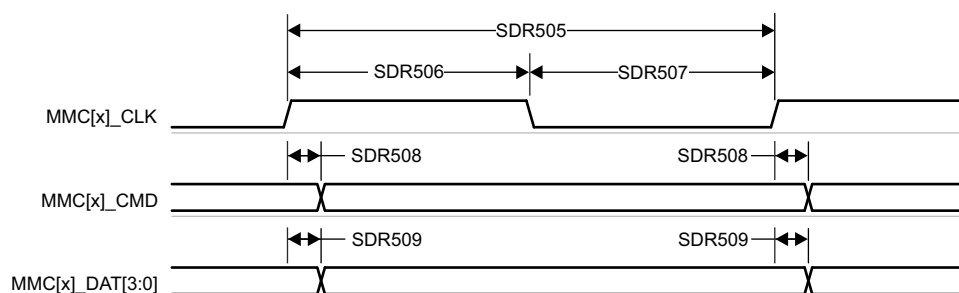
Table 6-78, and Figure 6-94 presents switching characteristics for MMC1/2 – UHS-I SDR50 Mode.

**Table 6-78. MMC1/2 Switching Characteristics – UHS-I SDR50 Mode**

see Figure 6-94

| NO.    | PARAMETER          |                                                                  | MIN  | MAX  | UNIT |
|--------|--------------------|------------------------------------------------------------------|------|------|------|
|        | $f_{op}(clk)$      | Operating frequency, MMC[x]_CLK                                  |      | 100  | MHz  |
| SDR505 | $t_{c}(clk)$       | Cycle time, MMC[x]_CLK                                           | 10   |      | ns   |
| SDR506 | $t_{w}(clkH)$      | Pulse duration, MMC[x]_CLK high                                  | 4.45 |      | ns   |
| SDR507 | $t_{w}(clkL)$      | Pulse duration, MMC[x]_CLK low                                   | 4.45 |      | ns   |
| SDR508 | $t_{d}(clkH-cmdV)$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 1.2  | 6.35 | ns   |
| SDR509 | $t_{d}(clkH-dV)$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 1.2  | 6.35 | ns   |

A.  $x = 1, 2$  for MMC1 and MMC2



**Figure 6-94. MMC1/2 – UHS-I SDR50 – Transmit Mode**

#### 6.10.5.17.2.6 UHS-I DDR50 Mode

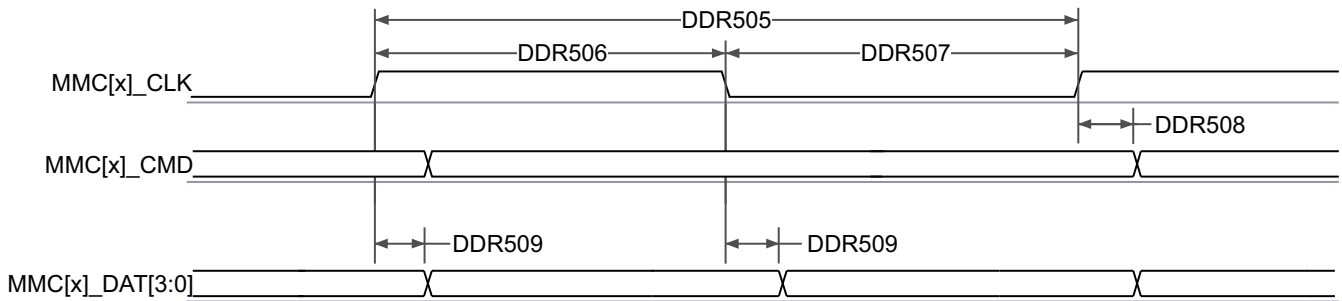
Table 6-79 and Figure 6-95 present switching characteristics for MMC1/2 – UHS-I DDR50 Mode.

**Table 6-79. MMC1/2 Switching Characteristics – UHS-I DDR50 Mode**

see Figure 6-95

| NO.    | PARAMETER          |                                                                 | MIN  | MAX  | UNIT |
|--------|--------------------|-----------------------------------------------------------------|------|------|------|
|        | $f_{op}(clk)$      | Operating frequency, MMC[x]_CLK                                 |      | 50   | MHz  |
| DDR505 | $t_{c}(clk)$       | Cycle time, MMC[x]_CLK                                          | 20   |      | ns   |
| DDR506 | $t_{w}(clkH)$      | Pulse duration, MMC[x]_CLK high                                 | 9.2  |      | ns   |
| DDR507 | $t_{w}(clkL)$      | Pulse duration, MMC[x]_CLK low                                  | 9.2  |      | ns   |
| DDR508 | $t_{d}(clkH-cmdV)$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition     | 1.12 | 3.46 | ns   |
| DDR509 | $t_{d}(clk-dV)$    | Delay time, MMC[x]_CLK transition to MMC[x]_DAT[3:0] transition | 1.12 | 6.12 | ns   |

A. x = 1, 2 for MMC1 and MMC2



**Figure 6-95. MMC1/2 – UHS-I DDR50 – Transmit Mode**

#### 6.10.5.17.2.7 UHS-I SDR104 Mode

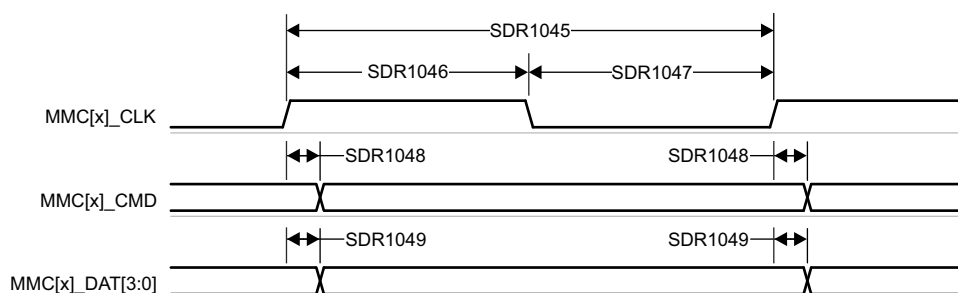
Table 6-80, and Figure 6-96 present switching characteristics for MMC1/2 – UHS-I SDR104 Mode.

**Table 6-80. MMC1/2 Switching Characteristics – UHS-I SDR104 Mode**

see Figure 6-96

| NO.     | PARAMETER          | MIN  | MAX  | UNIT |
|---------|--------------------|------|------|------|
|         | $f_{op}(clk)$      |      | 200  | MHz  |
| SDR1045 | $t_{c}(clk)$       | 5    |      | ns   |
| SDR1046 | $t_{w}(clkH)$      | 2.12 |      | ns   |
| SDR1047 | $t_{w}(clkL)$      | 2.12 |      | ns   |
| SDR1048 | $t_{d}(clkH-cmdV)$ | 1.07 | 3.21 | ns   |
| SDR1049 | $t_{d}(clkH-dV)$   | 1.07 | 3.21 | ns   |

A.  $x = 1, 2$  for MMC1 and MMC2



**Figure 6-96. MMC1/2 – UHS-I SDR104 – Transmit Mode**

#### 6.10.5.18 CPTS

Table 6-81 represents CPTS timing conditions.

**Table 6-81. CPTS Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| $SR_i$                   | Input slew rate         | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| $C_L$                    | Output load capacitance | 2   | 10  | pF   |

Section 6.10.5.18.1, Section 6.10.5.18.2, Figure 6-97, and Figure 6-98 present timing requirements and switching characteristics of the CPTS interface.

#### 6.10.5.18.1 CPTS Timing Requirements

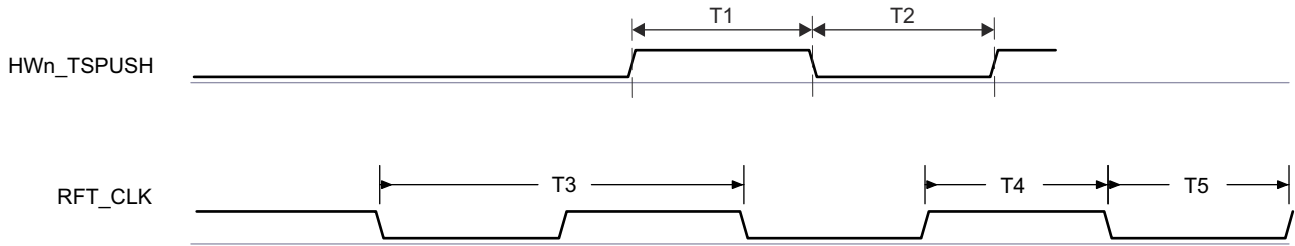
see Figure 6-97

| NO. | PARAMETER           | DESCRIPTION                                   | MIN              | MAX | UNIT |
|-----|---------------------|-----------------------------------------------|------------------|-----|------|
| T1  | $t_{w}(HWnTSPUSH)$  | Pulse duration, HWnTSPUSH <sup>(2)</sup> high | $12P + 2^{(1)}$  |     | ns   |
| T2  | $t_{w}(HWnTSPUSHL)$ | Pulse duration, HWnTSPUSH <sup>(2)</sup> low  | $12P + 2^{(1)}$  |     | ns   |
| T3  | $t_{c}(RFT\_CLK)$   | Cycle time, RFT_CLK                           | 5                | 8   | ns   |
| T4  | $t_{w}(RFT\_CLKH)$  | Pulse duration, RFT_CLK high                  | $0.45 * T^{(3)}$ |     | ns   |
| T5  | $t_{w}(RFT\_CLKL)$  | Pulse duration, RFT_CLK low                   | $0.45 * T^{(3)}$ |     | ns   |

(1) P = functional clock period in ns.

(2) In HWnTSPUSH, n = 1 to 2.

(3) T = RFT\_CLK period in ns.



**Figure 6-97. CPTS Timing Requirements**

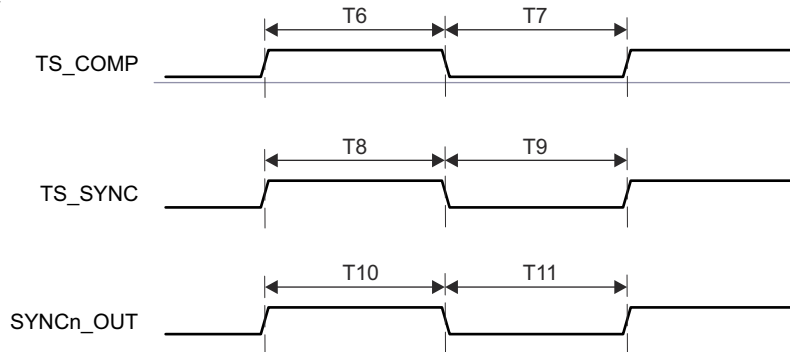
#### 6.10.5.18.2 CPTS Switching Characteristics

see [Figure 6-98](#)

| NO. | PARAMETER            |                                               | SOURCE  | MIN             | MAX | UNIT |
|-----|----------------------|-----------------------------------------------|---------|-----------------|-----|------|
| T6  | $t_{w(TS\_COMPH)}$   | Pulse duration, TS_COMP high                  |         | $36P - 2^{(1)}$ |     | ns   |
| T7  | $t_{w(TS\_COMPL)}$   | Pulse duration, TS_COMP low                   |         | $36P - 2^{(1)}$ |     | ns   |
| T8  | $t_{w(TS\_SYNCH)}$   | Pulse duration, TS_SYNC high                  |         | $36P - 2^{(1)}$ |     | ns   |
| T9  | $t_{w(TS\_SYNCL)}$   | Pulse duration, TS_SYNC low                   |         | $36P - 2^{(1)}$ |     | ns   |
| T10 | $t_{w(SYNcN\_OUTH)}$ | Pulse duration, SYNcN_OUT <sup>(2)</sup> high | TS_SYNC | $36P - 2^{(1)}$ |     | ns   |
|     |                      |                                               | TS_GENF | $5P - 2^{(1)}$  |     | ns   |
| T11 | $t_{w(SYNcN\_OUTL)}$ | Pulse duration, SYNcN_OUT <sup>(2)</sup> low  | TS_SYNC | $36P - 2^{(1)}$ |     | ns   |
|     |                      |                                               | TS_GENF | $5P - 2^{(1)}$  |     | ns   |

(1) P = functional clock period in ns.

(2) n = 0 to 3 in SYNcN\_OUT



**Figure 6-98. CPTS Switching Characteristics**

For more information, see *Navigator Subsystem (NAVSS)* section in *Data Movement Architecture (DMA)* chapter in the device TRM.

#### 6.10.5.19 OSPI

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

[Table 6-82](#) represents OSPI timing conditions.

**Table 6-82. OSPI Timing Conditions**

| PARAMETER         |                 |                                      | MIN  | MAX | UNIT |
|-------------------|-----------------|--------------------------------------|------|-----|------|
| INPUT CONDITIONS  |                 |                                      |      |     |      |
| SR <sub>I</sub>   | Input slew rate | 3.3V, all modes                      | 2    | 6   | V/ns |
|                   |                 | 1.8V, PHY Data Training DDR with DQS | 0.75 | 6   | V/ns |
|                   |                 | 1.8V, all other modes                | 1    | 6   | V/ns |
| OUTPUT CONDITIONS |                 |                                      |      |     |      |

**Table 6-82. OSPI Timing Conditions (continued)**

| PARAMETER                            |                                                                                                     |                                       | MIN            | MAX            | UNIT |
|--------------------------------------|-----------------------------------------------------------------------------------------------------|---------------------------------------|----------------|----------------|------|
| $C_L$                                | Output load capacitance                                                                             | All modes                             | 3              | 10             | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |                                                                                                     |                                       |                |                |      |
| $t_d$ (Trace Delay)                  | Propagation delay<br>OSPI_CLK trace                                                                 | No Loopback;<br>Internal Pad Loopback |                | 450            | ps   |
|                                      | Propagation delay<br>OSPI_LBCLKO trace                                                              | External Board<br>Loopback            | $2*L-30^{(2)}$ | $2*L+30^{(2)}$ | ps   |
|                                      | Propagation delay<br>OSPI_DQS trace                                                                 | DQS                                   | $L-30^{(2)}$   | $L+30^{(2)}$   | ps   |
| $t_d$ (Trace Mismatch Delay)         | Propagation delay mismatch<br>OSPI_D[i:0] <sup>(1)</sup> , OSPI_CS <i>n</i><br>relative to OSPI_CLK | All modes                             |                | 60             | ps   |

(1)  $i$  in D[i:0] = 0 to 7 for OSPI0;  $i$  in [i:0] = 3 for OSPI1(2)  $L$  = Propagation delay of OSPI\_CLK trace

### 6.10.5.19.1 OSPI0/1 PHY Mode

#### 6.10.5.19.1.1 OSPI0/1 With PHY Data Training

Read and write data valid windows will shift due to variation in process, voltage, temperature, and operating frequency. A data training method may be implemented to dynamically configure optimal read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

Data transmit and receive timing parameters are not defined for the data training use case since they are dynamically adjusted based on the operating condition.

Table 6-83 defines DLL delays required for OSPI0/1 with Data Training. Table 6-84, Figure 6-99, Figure 6-100, Table 6-85, Figure 6-101, and Figure 6-102 present timing requirements and switching characteristics for OSPI0/1 with Data Training.

**Table 6-83. OSPI0/1 DLL Delay Mapping for PHY Data Training**

| MODE            | OSPI_PHY_CONFIGURATION_REG BIT FIELD | DELAY VALUE |
|-----------------|--------------------------------------|-------------|
| <b>Transmit</b> |                                      |             |
| All modes       | PHY_CONFIG_TX_DLL_DELAY_FLD          | (1)         |
| <b>Receive</b>  |                                      |             |
| All modes       | PHY_CONFIG_RX_DLL_DELAY_FLD          | (2)         |

(1) Transmit DLL delay value determined by training software

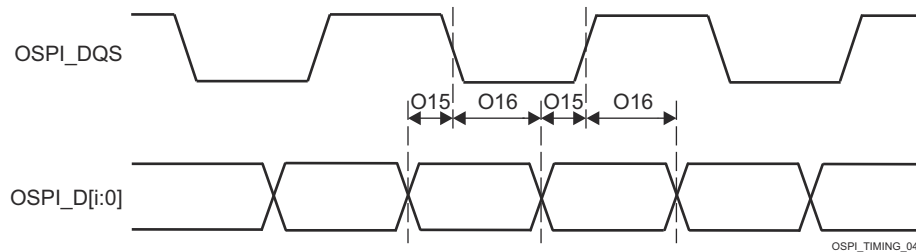
(2) Receive DLL delay value determined by training software

**Table 6-84. OSPI0 Timing Requirements – PHY Data Training**

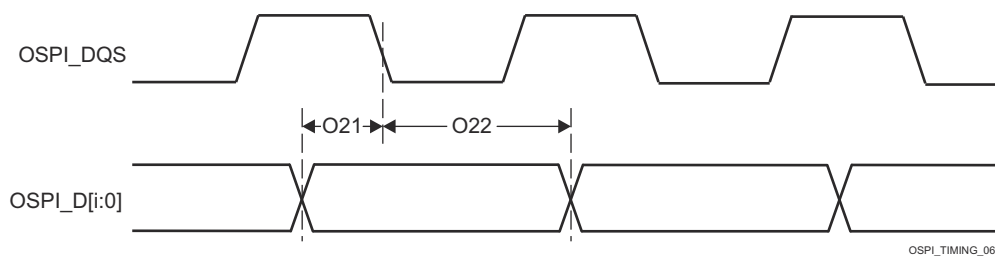
see Figure 6-99, and Figure 6-100

| NO. |                   |                                                             | MODE                                 | MIN | MAX | UNIT |
|-----|-------------------|-------------------------------------------------------------|--------------------------------------|-----|-----|------|
| O15 | $t_{su(D-LBCLK)}$ | Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge | DDR with DQS                         | (1) |     | ns   |
| O16 | $t_h(LBCLK-D)$    | Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge   | DDR with DQS                         | (1) |     | ns   |
| O21 | $t_{su(D-LBCLK)}$ | Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge | SDR with Internal PHY Loopback       | (1) |     | ns   |
| O22 | $t_h(LBCLK-D)$    | Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge   | SDR with Internal PHY Loopback       | (1) |     | ns   |
|     | $t_{DVW}$         | Data valid window (O15 + O16)                               | 1.8V, DDR with DQS                   | 1.4 |     | ns   |
|     |                   | Data valid window (O21 + O22)                               | 1.8V, SDR with Internal PHY Loopback | 1.7 |     | ns   |

(1) Minimum setup and hold time requirements for OSPI0/1\_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window. The  $t_{DVW}$  parameter defines the minimum data invalid window required. This parameter is provided in lieu of minimum setup and minimum hold times, where it must be used to check compatibility with the data valid window provided by an attached device.



**Figure 6-99. OSPI0/1 Timing Requirements – PHY Data Training, DDR with DQS**



**Figure 6-100. OSPI0/1 Timing Requirements – PHY Data Training, SDR with Internal PHY Loopback**

**Table 6-85. OSPI0/1 Switching Characteristics – PHY Data Training**

See [Figure 6-101](#) and [Figure 6-102](#)

| NO. | PARAMETER        | MODE      | MIN                                                              | MAX                                                              | UNIT |
|-----|------------------|-----------|------------------------------------------------------------------|------------------------------------------------------------------|------|
| O1  | $t_{c(CLK)}$     | 1.8V, DDR | 6.0                                                              | 6.0                                                              | ns   |
| O7  |                  | 1.8V, SDR | 6.0                                                              | 6.0                                                              | ns   |
| O2  | $t_{w(CLKL)}$    | DDR       | $((0.475P^{(1)}) - 0.3)$                                         |                                                                  | ns   |
| O8  |                  | SDR       |                                                                  |                                                                  |      |
| O3  | $t_{w(CLKH)}$    | DDR       | $((0.475P^{(1)}) - 0.3)$                                         |                                                                  | ns   |
| O9  |                  | SDR       |                                                                  |                                                                  |      |
| O4  | $t_{d(CSn-CLK)}$ | DDR       | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)}) + (0.028TD^{(5)} - 1))$ | $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + (0.055TD^{(5)} + 1))$ | ns   |
| O10 |                  | SDR       |                                                                  |                                                                  |      |
| O5  | $t_{d(CLK-CSn)}$ | DDR       | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - (0.055TD^{(5)} - 1))$ | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}) - (0.028TD^{(5)} + 1))$ | ns   |
| O11 |                  | SDR       |                                                                  |                                                                  |      |
| O6  | $t_{d(CLK-D)}$   | DDR       | (6)                                                              |                                                                  | ns   |
| O12 |                  | SDR       |                                                                  |                                                                  |      |
|     | $t_{DIVW}$       | DDR       | 1                                                                |                                                                  | ns   |
|     |                  | SDR       |                                                                  |                                                                  |      |

(1) P = SCLK cycle time in ns = OSPI0\_CLK cycle time in ns

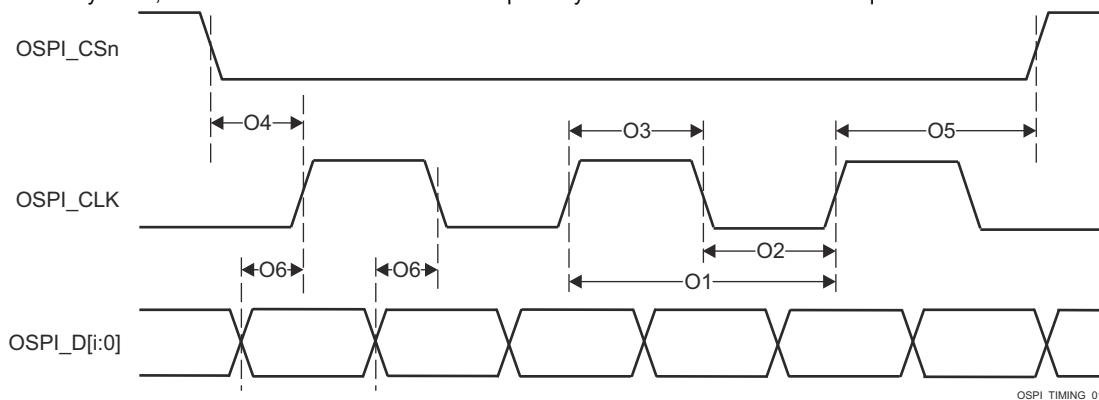
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]

(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]

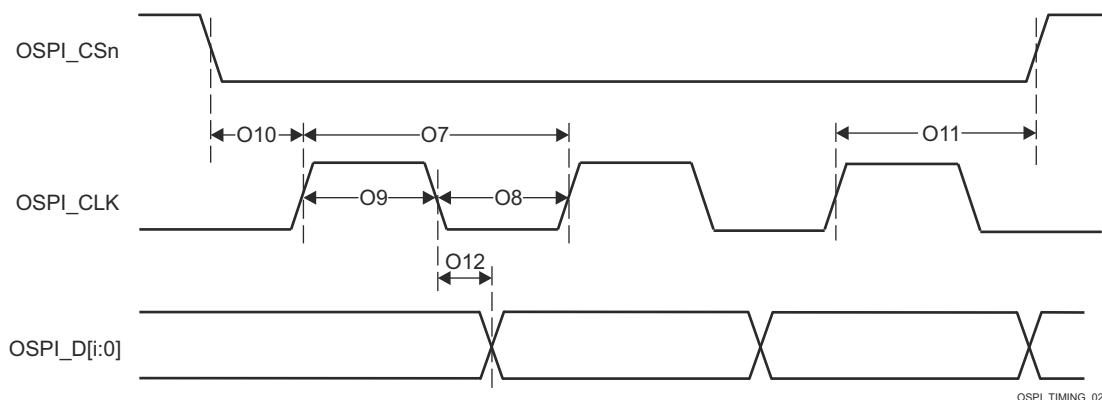
(4) R = reference clock cycle time in ns

(5) TD = PHY\_CONFIG\_TX\_DLL\_DELAY\_FLD

(6) Minimum and maximum delay times for OSPI0\_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window. The  $t_{DIVW}$  parameter defines the maximum data invalid window. This parameter is provided in lieu of minimum and maximum delay times, where it must be used to check compatibility with the data valid window requirements of an attached device.



**Figure 6-101. OSPI0/1 Switching Characteristics – PHY DDR Data Training**



**Figure 6-102. OSPI0/1 Switching Characteristics – PHY SDR Data Training**

#### 6.10.5.19.1.2 OSPI Without Data Training

##### Note

The I/O Timings provided in this section are only applicable when data training is not implemented. Additionally, the I/O Timings are valid only for some OSPI usage modes when the corresponding DLL Delays are configured as described in [Table 6-86](#) found in this section.

[Section 6.10.5.19.1.2.4](#), [Section 6.10.5.19.1.2.2](#), [Section 6.10.5.19.1.2](#), and [Section 6.10.5.19.1.2](#) present switching characteristics for OSPI DDR and SDR Mode.

#### 6.10.5.19.1.2.1 OSPI Timing Requirements – SDR Mode

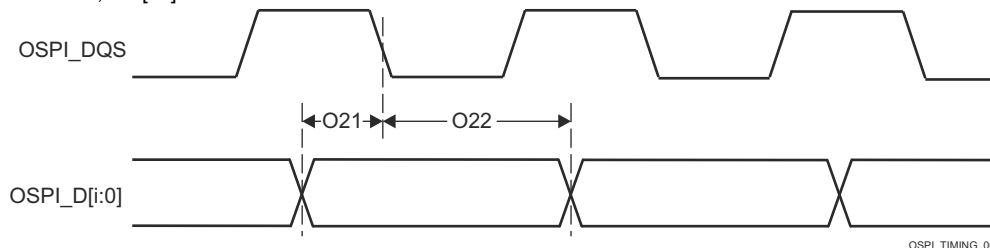
**Table 6-86. OSPI DLL Delay Mapping - SDR Timing Modes**

| MODE      | OSPI_PHY_CONFIGURATION_REG BIT FIELD | DELAY VALUE |
|-----------|--------------------------------------|-------------|
| All modes | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x0         |
|           | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x0         |

**Table 6-87. OSPI Timing Requirements – SDR Mode**

| NO. | PARAMETER         | DESCRIPTION                                                                  | MODE                          | MIN | MAX | UNIT |
|-----|-------------------|------------------------------------------------------------------------------|-------------------------------|-----|-----|------|
| O21 | $t_{su}(D-LBCLK)$ | Setup time, D[i:0] valid before active LBCLK input (DQS) edge <sup>(1)</sup> | 1.8V, External Board Loopback | 0.6 |     | ns   |
|     |                   |                                                                              | 3.3V, External Board Loopback | 0.9 |     | ns   |
| O22 | $t_h(LBCLK-D)$    | Hold time, D[i:0] valid after active LBCLK input (DQS) edge <sup>(1)</sup>   | 1.8V, External Board Loopback | 1.7 |     | ns   |
|     |                   |                                                                              | 3.3V, External Board Loopback | 2   |     | ns   |

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1



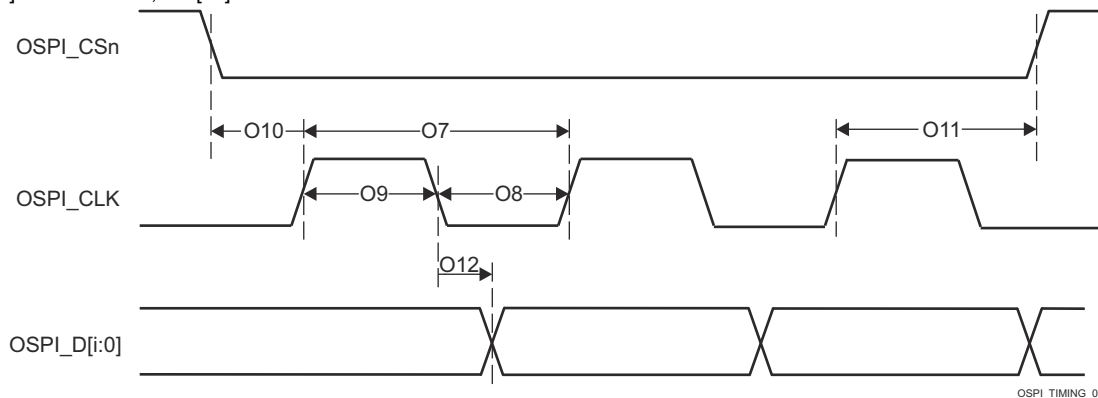
**Figure 6-103. OSPI Timing Requirements – SDR, External Loopback Clock**

#### 6.10.5.19.1.2.2 OSPI Switching Characteristics – SDR Mode

| NO. | PARAMETER    | DESCRIPTION     | MODE | MIN | MAX | UNIT |
|-----|--------------|-----------------|------|-----|-----|------|
| O7  | $t_{c(CLK)}$ | Cycle time, CLK | 1.8V | 7   |     | ns   |
|     |              |                 | 3.3V | 7.5 |     | ns   |

| NO. | PARAMETER         | DESCRIPTION                                                     | MODE | MIN                                                                                                                               | MAX  | UNIT |
|-----|-------------------|-----------------------------------------------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------|------|------|
| O8  | $t_{w(CLKL)}$     | Pulse duration, CLK low                                         |      | $((0.475P^{(1)}) - 0.3)$                                                                                                          |      | ns   |
| O9  |                   | Pulse duration, CLK high                                        |      | $((0.475P^{(1)}) - 0.3)$                                                                                                          |      | ns   |
| O10 | $t_{id(CSn-CLK)}$ | Delay time, CSn active edge to CLK rising edge                  | 1.8V | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)}) + (0.028TD^{(5)} - 1)) + ((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + (0.055TD^{(5)} - 1))$ |      | ns   |
|     |                   |                                                                 | 3.3V | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)}) + (0.028TD^{(5)} - 1)) + ((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + (0.055TD^{(5)} - 1))$ |      | ns   |
| O11 | $t_{d(CLK-CSn)}$  | Delay time, CLK rising edge to CSn inactive edge                | 1.8V | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - (0.055TD^{(5)} - 1)) + ((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}) - (0.028TD^{(5)} - 1))$ |      | ns   |
|     |                   |                                                                 | 3.3V | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - (0.055TD^{(5)} - 1)) + ((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}) - (0.028TD^{(5)} - 1))$ |      | ns   |
| O12 | $t_{d(CLK-D)}$    | Delay time, CLK active edge to D[i:0] transition <sup>(6)</sup> | 1.8V | -1.16                                                                                                                             | 1.25 | ns   |
|     |                   |                                                                 | 3.3V | -1.33                                                                                                                             | 1.51 | ns   |

- (1) P = CLK cycle time = SCLK period  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = refclk  
(5) TD = PHY\_CONFIG\_TX\_DLL\_DELAY\_FLD  
(6) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1



**Figure 6-104. OSPI Switching Characteristics – SDR**

Section 6.10.5.19.1.2.3, Section 6.10.5.19.1.2.1, Section 6.10.5.19.1.2.2, Section 6.10.5.19.1.2.2, and Figure 6-103 presents timing requirements for OSPI DDR and SDR Mode.

#### 6.10.5.19.1.2.3 OSPI Timing Requirements – DDR Mode

**Table 6-88. OSPI DLL Delay Mapping - DDR Timing Modes**

| MODE     | OSPI_PHY_CONFIGURATION_REG<br>BIT FIELD | OSPI0       | OSPI1 |
|----------|-----------------------------------------|-------------|-------|
|          |                                         | DELAY VALUE |       |
| TRANSMIT |                                         |             |       |
| 1.8V     | PHY_CONFIG_TX_DLL_DELAY_FLD             | 0x54        | 0x54  |

**Table 6-88. OSPI DLL Delay Mapping - DDR Timing Modes (continued)**

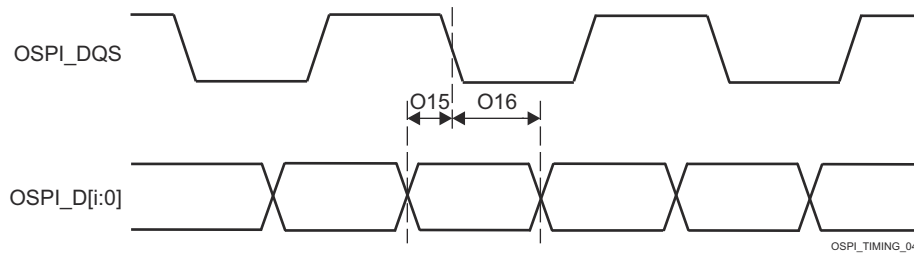
| MODE            | OSPI_PHY_CONFIGURATION_REG<br>BIT FIELD | OSPI0       | OSPI1 |
|-----------------|-----------------------------------------|-------------|-------|
|                 |                                         | DELAY VALUE |       |
| 3.3V            | PHY_CONFIG_TX_DLL_DELAY_FLD             | 0x55        | 0x5C  |
| <b>RECEIVE</b>  |                                         |             |       |
| 1.8V, DQS       | PHY_CONFIG_RX_DLL_DELAY_FLD             | 0x23        | 0x29  |
| 3.3V, DQS       | PHY_CONFIG_RX_DLL_DELAY_FLD             | 0x47        | 0x42  |
| All other modes | PHY_CONFIG_RX_DLL_DELAY_FLD             | 0x0         | 0x0   |

**Table 6-89. OSPI Timing Requirements – DDR Mode**

| NO. | PARAMETER         | DESCRIPTION                                                            | MODE                          | MIN                 | MAX | UNIT |
|-----|-------------------|------------------------------------------------------------------------|-------------------------------|---------------------|-----|------|
| O15 | $t_{su}(D-LBCLK)$ | Setup time, D[i:0] valid before active LBCLK (DQS) edge <sup>(1)</sup> | 1.8V, External Board Loopback | 0.52                |     | ns   |
|     |                   |                                                                        | 3.3V, External Board Loopback | 1.97                |     | ns   |
| O16 | $t_h(LBCLK-D)$    | Hold time, D[i:0] valid after active LBCLK (DQS) edge <sup>(1)</sup>   | 1.8V, External Board Loopback | 1.24 <sup>(2)</sup> |     | ns   |
|     |                   |                                                                        | 3.3V, External Board Loopback | 1.44 <sup>(2)</sup> |     | ns   |
| O17 | $t_{su}(D-DQS)$   | Setup time, DQS edge to D[i:0] transition <sup>(1)</sup>               | 1.8V, DQS                     | –0.46               |     | ns   |
|     |                   |                                                                        | 3.3V, DQS                     | –0.66               |     | ns   |
| O18 | $t_h(DQS-D)$      | Hold time, DQS edge to D[i:0] transition <sup>(1)</sup>                | 1.8V, DQS                     | 3.59                |     | ns   |
|     |                   |                                                                        | 3.3V, DQS                     | 8.89                |     | ns   |

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

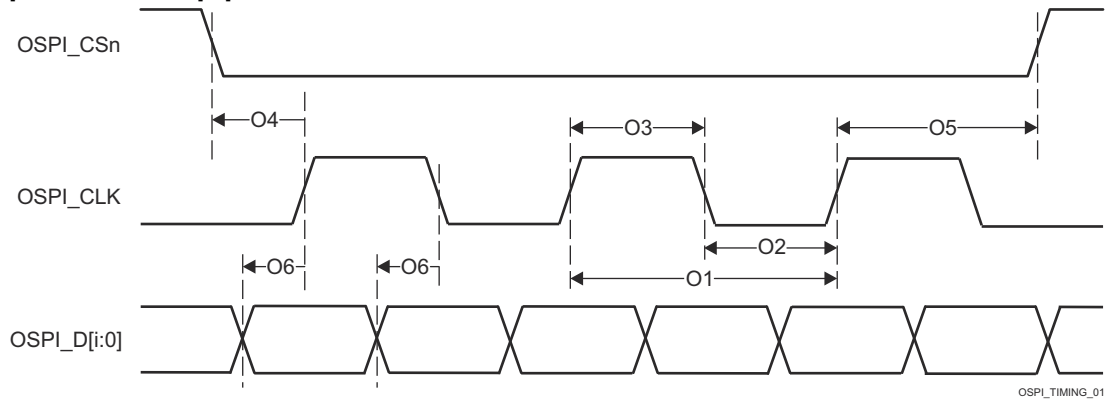
(2) This Hold time requirement is larger than the Hold time provided by a typical flash device. Therefore, the trace length between the SoC and flash device must be sufficiently long enough to ensure that the Hold time is met at the SoC. Refer to [OSPI and QSPI Board Design and Layout Guidelines](#) for more details.

**Figure 6-105. OSPI Timing Requirements – DDR, External Loopback Clock and DQS****6.10.5.19.1.2.4 OSPI Switching Characteristics – PHY DDR Mode**

| NO. | PARAMETER       | DESCRIPTION                                    | MODE | MIN                                                                                                                               | MAX | UNIT |
|-----|-----------------|------------------------------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------|-----|------|
| O1  | $t_c(CLK)$      | Cycle time, CLK                                | 1.8V | 19                                                                                                                                |     | ns   |
|     |                 |                                                | 3.3V | 19                                                                                                                                |     | ns   |
| O2  | $t_w(CCLKL)$    | Pulse duration, CLK low                        |      | $((0.475P^{(1)}) - 0.3)$                                                                                                          |     | ns   |
| O3  | $t_w(CCLKH)$    | Pulse duration, CLK high                       |      | $((0.475P^{(1)}) - 0.3)$                                                                                                          |     | ns   |
| O4  | $t_d(CCLK-CSn)$ | Delay time, CSn active edge to CLK rising edge | 1.8V | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)}) + (0.028TD^{(5)}) - 1)$ $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + (0.055TD^{(5)}) - 1)$ |     | ns   |
|     |                 |                                                | 3.3V | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)}) + (0.028TD^{(5)}) - 1)$ $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + (0.055TD^{(5)}) - 1)$ |     | ns   |

| NO. | PARAMETER                | DESCRIPTION                                                     | MODE                                      | MIN                                                                                                    | MAX                                                                                                    | UNIT |
|-----|--------------------------|-----------------------------------------------------------------|-------------------------------------------|--------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|------|
| O5  | t <sub>d</sub> (CLK-CSn) | Delay time, CLK rising edge to CSn inactive edge                | 1.8V                                      | ((0.475P <sup>(1)</sup> ) + (0.975N <sup>(3)</sup> R <sup>(4)</sup> ) + (0.055TD <sup>(5)</sup> ) - 1) | ((0.525P <sup>(1)</sup> ) + (1.025N <sup>(3)</sup> R <sup>(4)</sup> ) + (0.028TD <sup>(5)</sup> ) + 1) | ns   |
|     |                          |                                                                 | 3.3V, OSPI0 DDR TX;<br>3.3V, OSPI1 DDR TX | ((0.475P <sup>(1)</sup> ) + (0.975N <sup>(3)</sup> R <sup>(4)</sup> ) + (0.055TD <sup>(5)</sup> ) - 1) | ((0.525P <sup>(1)</sup> ) + (1.025N <sup>(3)</sup> R <sup>(4)</sup> ) + (0.028TD <sup>(5)</sup> ) + 1) | ns   |
| O6  | t <sub>d</sub> (CLK-D)   | Delay time, CLK active edge to D[i:0] transition <sup>(6)</sup> | 1.8V, OSPI0 DDR TX;<br>1.8V, OSPI1 DDR TX | −7.71                                                                                                  | −1.56                                                                                                  | ns   |
|     |                          |                                                                 | 3.3V, OSPI0 DDR TX;<br>3.3V, OSPI1 DDR TX | −7.71                                                                                                  | −1.56                                                                                                  | ns   |

- (1) P = CLK cycle time = SCLK period  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = reference clock cycle time in ns  
(5) TD = PHY\_CONFIG\_TX\_DLL\_DELAY\_FLD  
(6) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1



**Figure 6-106. OSPI Switching Characteristics – DDR**

### 6.10.5.19.2 OSPI0/1 Tap Mode

#### 6.10.5.19.2.1 OSPI0 Tap SDR Timing

Table 6-90, Figure 6-107, Table 6-91, and Figure 6-108 present timing requirements and switching characteristics for OSPI0 Tap SDR Mode.

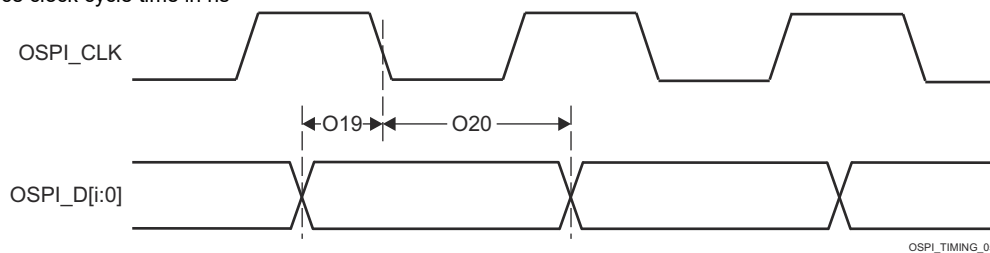
**Table 6-90. OSPI0/1 Timing Requirements – Tap SDR Mode**

see Figure 6-107

| NO. |                 |                                                                 | MODE        | MIN                               | MAX | UNIT |
|-----|-----------------|-----------------------------------------------------------------|-------------|-----------------------------------|-----|------|
| O19 | $t_{su(D-CLK)}$ | Setup time, OSPI0/1_D[7:0] valid before active OSPI0/1_CLK edge | No Loopback | (15.4 - $(0.975T^{(1)}R^{(2)})$ ) |     | ns   |
| O20 | $t_{h(CLK-D)}$  | Hold time, OSPI0/1_D[7:0] valid after active OSPI0/1_CLK edge   | No Loopback | (-5.2 + $(0.975T^{(1)}R^{(2)})$ ) |     | ns   |

(1) T = OSPI\_RD\_DATA\_CAPTURE\_REG[DELAY\_FLD]

(2) R = reference clock cycle time in ns



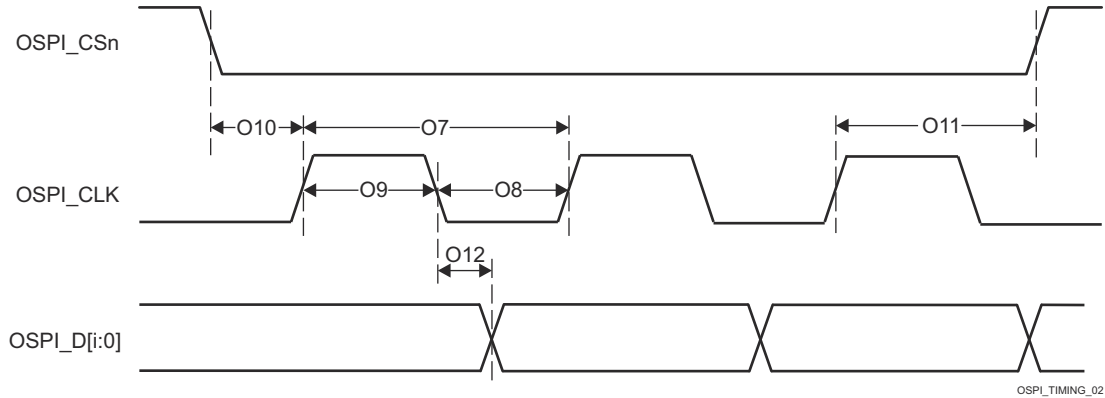
**Figure 6-107. OSPI0/1 Timing Requirements – Tap SDR, No Loopback**

**Table 6-91. OSPI0/1 Switching Characteristics – Tap SDR Mode**

see [Figure 6-108](#)

| NO. | PARAMETER        | MODE                                                                  | MIN                                            | MAX                                            | UNIT |
|-----|------------------|-----------------------------------------------------------------------|------------------------------------------------|------------------------------------------------|------|
| O7  | $t_{c(CLK)}$     | Cycle time, OSPI0/1_CLK                                               | 20                                             |                                                | ns   |
| O8  | $t_{w(CLKL)}$    | Pulse duration, OSPI0/1_CLK low                                       | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O9  | $t_{w(CLKH)}$    | Pulse duration, OSPI0/1_CLK high                                      | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O10 | $t_{d(CSn-CLK)}$ | Delay time, OSPI0/1_CSn[3:0] active edge to OSPI0/1_CLK rising edge   | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)}) - 1)$ | $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + 1)$ | ns   |
| O11 | $t_{d(CLK-CSn)}$ | Delay time, OSPI0/1_CLK rising edge to OSPI0/1_CSn[3:0] inactive edge | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - 1)$ | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}) + 1)$ | ns   |
| O12 | $t_{d(CLK-D)}$   | Delay time, OSPI0/1_CLK active edge to OSPI0/1_D[7:0] transition      | -2                                             | 2                                              | ns   |

- (1) P = CLK cycle time = SCLK period in ns  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = reference clock cycle time in ns



**Figure 6-108. OSPI0/1 Switching Characteristics – Tap SDR, No Loopback**

### 6.10.5.19.2.2 OSPI0 Tap DDR Timing

Table 6-92, Figure 6-109, Table 6-93, and Figure 6-110 present timing requirements and switching characteristics for OSPI0 Tap DDR Mode.

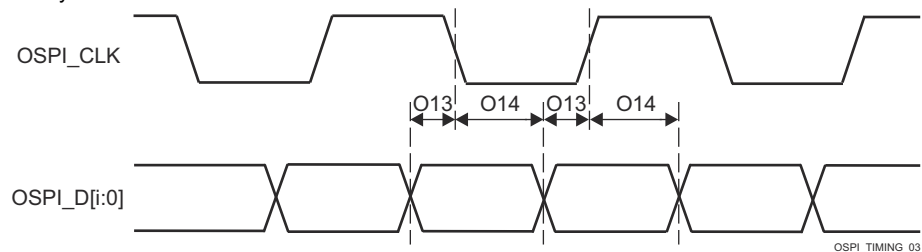
**Table 6-92. OSPI0/1 Timing Requirements – Tap DDR Mode**

see Figure 6-109

| NO. |                 |                                                                 | MODE        | MIN                                                    | MAX | UNIT |
|-----|-----------------|-----------------------------------------------------------------|-------------|--------------------------------------------------------|-----|------|
| O13 | $t_{su}(D-CLK)$ | Setup time, OSPI0/1_D[7:0] valid before active OSPI0/1_CLK edge | No Loopback | (17.04 -<br>(0.975T <sup>(1)</sup> R <sup>(2)</sup> )) |     | ns   |
| O14 | $t_h(CLK-D)$    | Hold time, OSPI0/1_D[7:0] valid after active OSPI0/1_CLK edge   | No Loopback | (-3.16 +<br>(0.975T <sup>(1)</sup> R <sup>(2)</sup> )) |     | ns   |

(1) T = OSPI\_RD\_DATA\_CAPTURE\_REG[DELAY\_FLD]

(2) R = reference clock cycle time in ns



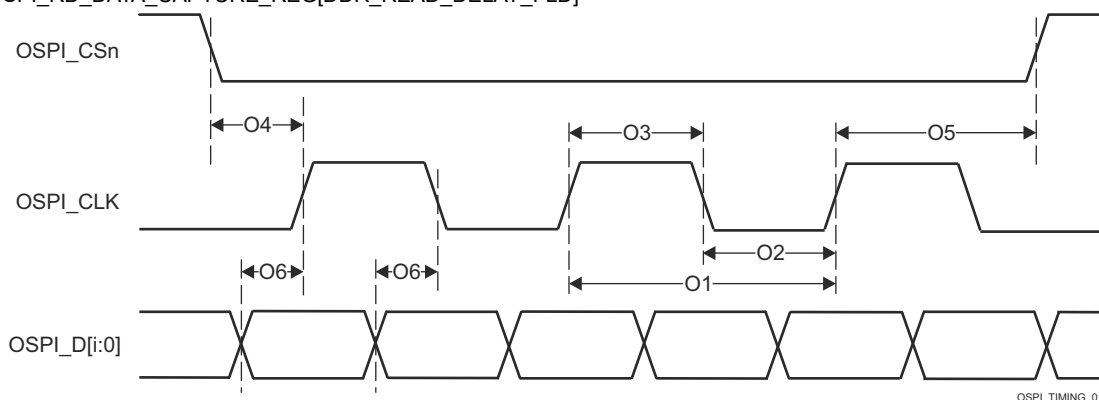
**Figure 6-109. OSPI0/1 Timing Requirements – Tap DDR, No Loopback**

**Table 6-93. OSPI0/1 Switching Characteristics – Tap DDR Mode**

see [Figure 6-110](#)

| NO. | PARAMETER        | MODE                                                                  | MIN                                                      | MAX                                                     | UNIT |
|-----|------------------|-----------------------------------------------------------------------|----------------------------------------------------------|---------------------------------------------------------|------|
| O1  | $t_{c(CLK)}$     | Cycle time, OSPI0/1_CLK                                               | 40                                                       |                                                         | ns   |
| O2  | $t_{w(CLKL)}$    | Pulse duration, OSPI0/1_CLK low                                       | $((0.475P^{(1)}) - 0.3)$                                 |                                                         | ns   |
| O3  | $t_{w(CLKH)}$    | Pulse duration, OSPI0/1_CLK high                                      | $((0.475P^{(1)}) - 0.3)$                                 |                                                         | ns   |
| O4  | $t_{d(CSn-CLK)}$ | Delay time, OSPI0/1_CSn[3:0] active edge to OSPI0/1_CLK rising edge   | $((0.475P^{(1)}) + ((0.975M^{(2)}R^{(4)}) - 1)$          | $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + 1)$          | ns   |
| O5  | $t_{d(CLK-CSn)}$ | Delay time, OSPI0/1_CLK rising edge to OSPI0/1_CSn[3:0] inactive edge | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - 1)$           | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}) + 1)$          | ns   |
| O6  | $t_{d(CLK-D)}$   | Delay time, OSPI0/1_CLK active edge to OSPI0/1_D[7:0] transition      | $(-5.04 + (0.975(T^{(5)} + 1)R^{(4)}) - (0.525P^{(1)}))$ | $(3.64 + (1.025(T^{(5)} + 1)R^{(4)}) - (0.475P^{(1)}))$ | ns   |

- (1) P = CLK cycle time = SCLK period in ns  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = reference clock cycle time in ns  
(5) T = OSPI\_RD\_DATA\_CAPTURE\_REG[DDR\_READ\_DELAY\_FLD]



**Figure 6-110. OSPI0/1 Switching Characteristics – Tap DDR, No Loopback**

#### 6.10.5.20 PCIE

The PCI-Express Subsystem is compliant with the PCIe® Base Specification, Revision 4.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.21 Timers

For more details about features and additional description information on the device Timers, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

[Table 6-94](#) represents Timers timing conditions.

**Table 6-94. Timers Timing Conditions**

| PARAMETER                | DESCRIPTION             | MODE    | MIN | MAX | UNIT |
|--------------------------|-------------------------|---------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | CAPTURE | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | PWM     | 2   | 10  | pF   |

Section 6.10.5.21.1, Section 6.10.5.21.2 and Figure 6-111 present timings and switching characteristics of the Timers.

#### 6.10.5.21.1 Timing Requirements for Timers

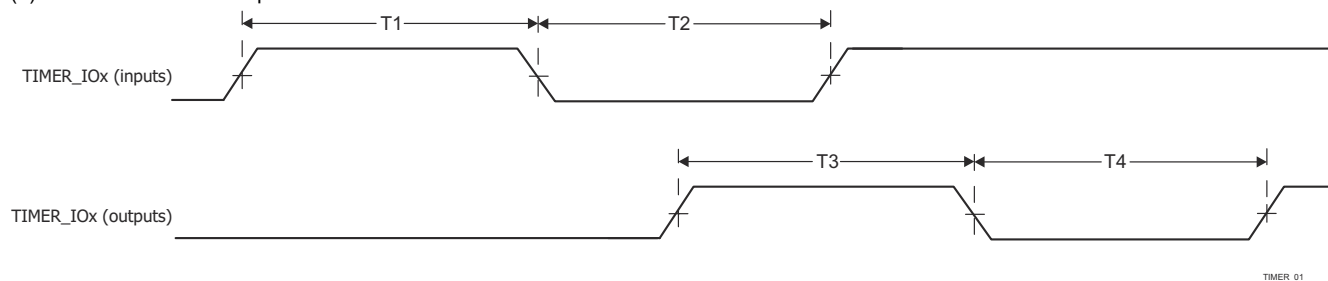
| NO. | PARAMETER      | DESCRIPTION          | MODE    | MIN              | MAX | UNIT |
|-----|----------------|----------------------|---------|------------------|-----|------|
| T1  | $t_{w(TINPH)}$ | Pulse duration, high | CAPTURE | $2.5 + 4P^{(1)}$ |     | ns   |
| T2  | $t_{w(TINPL)}$ | Pulse duration, low  | CAPTURE | $2.5 + 4P^{(1)}$ |     | ns   |

(1) P = functional clock period in ns.

#### 6.10.5.21.2 Switching Characteristics for Timers

| NO. | PARAMETER      | DESCRIPTION          | MODE | MIN               | MAX | UNIT |
|-----|----------------|----------------------|------|-------------------|-----|------|
| T3  | $t_{w(TOUTH)}$ | Pulse duration, high | PWM  | $-2.5 + 4P^{(1)}$ |     | ns   |
| T4  | $t_{w(TOUTL)}$ | Pulse duration, low  | PWM  | $-2.5 + 4P^{(1)}$ |     | ns   |

(1) P = functional clock period in ns.



**Figure 6-111. Timer Timing**

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.22 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding sections within , [Signal Descriptions](#) and *Detailed Description*.

Table 6-95 represents UART timing conditions.

**Table 6-95. UART Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX        | UNIT |
|--------------------------|-------------------------|-----|------------|------|
| <b>INPUT CONDITIONS</b>  |                         |     |            |      |
| $SR_I$                   | Input slew rate         | 0.5 | 5          | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |            |      |
| $C_L$                    | Output load capacitance | 1   | $30^{(1)}$ | pF   |

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

Section 6.10.5.22.1, Section 6.10.5.22.2, and Figure 6-112 present timing requirements and switching characteristics for UART interface.

#### 6.10.5.22.1 Timing Requirements for UART

| NO. | PARAMETER       | DESCRIPTION                                | MODE | MIN                         | MAX                         | UNIT |
|-----|-----------------|--------------------------------------------|------|-----------------------------|-----------------------------|------|
| 4   | $t_{w( rxd )}$  | Pulse width, receive data bit, high or low |      | 0.95U <sup>(1)</sup><br>(2) | 1.05U <sup>(1)</sup><br>(2) | ns   |
| 5   | $t_{w( rxdS )}$ | Pulse width, receive start bit, low        |      | 0.95U <sup>(1)</sup><br>(2) |                             | ns   |

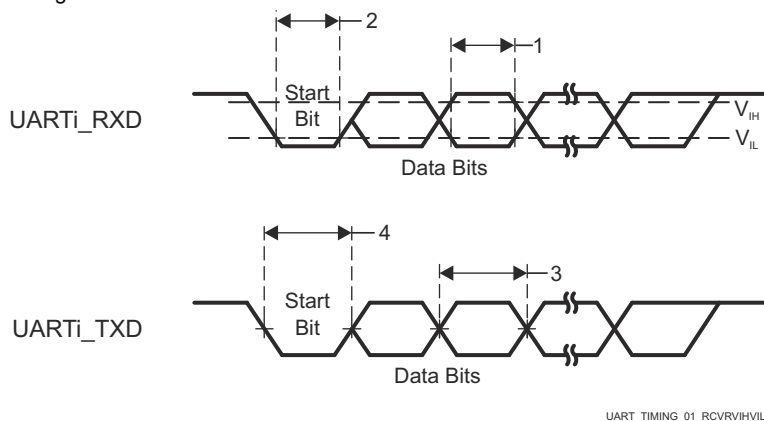
(1) U = UART baud time = 1/Programmed baud rate

(2) This value defines the data valid time, where the input voltage is required to be above  $V_{IH}$  or below  $V_{IL}$ .

#### 6.10.5.22.2 UART Switching Characteristics

| NO. | PARAMETER    | DESCRIPTION                                  | MIN                  | MAX                  | UNIT |
|-----|--------------|----------------------------------------------|----------------------|----------------------|------|
|     | $f_{(baud)}$ | Maximum programmable baud rate               |                      | 12                   | Mbps |
| 2   | $t_{w(TX)}$  | Pulse width, transmit data bit, high or low  | U - 2 <sup>(1)</sup> | U + 2 <sup>(1)</sup> | ns   |
| 3   | $t_{w(RTS)}$ | Pulse width, transmit start bit, high or low | U - 2 <sup>(1)</sup> |                      | ns   |

(1) U = UART baud time = 1/Programmed baud rate



**Figure 6-112. UART Timing**

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.23 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 Dual-Role Device Subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

### 6.10.6 Emulation and Debug

#### 6.10.6.1 Trace

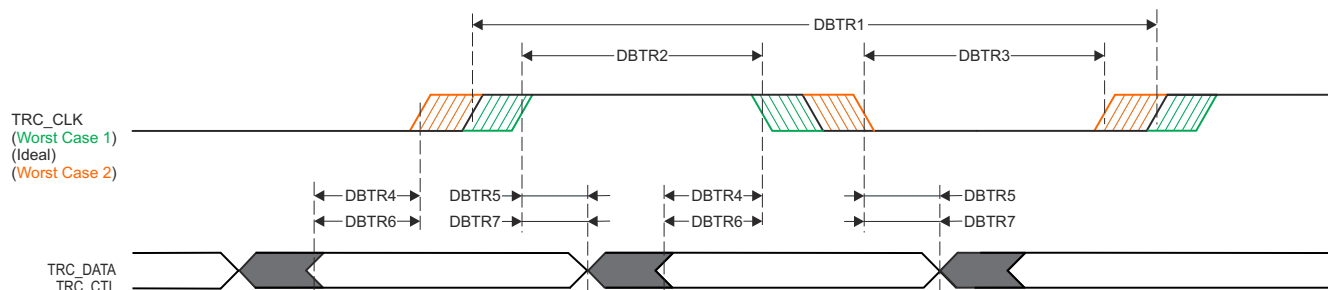
**Table 6-96. Trace Timing Conditions**

| PARAMETER                            |                                              | MIN | MAX | UNIT |
|--------------------------------------|----------------------------------------------|-----|-----|------|
| <b>OUTPUT CONDITIONS</b>             |                                              |     |     |      |
| $C_L$                                | Output load capacitance                      | 2   | 5   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |                                              |     |     |      |
| $t_d(\text{Trace Mismatch})$         | Propagation delay mismatch across all traces |     | 200 | ps   |

Table 6-97 and Figure 6-113 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-97. Trace Switching Characteristics**

| NO.        | PARAMETER                            |                                                    | MIN  | MAX | UNIT |
|------------|--------------------------------------|----------------------------------------------------|------|-----|------|
| 1.8 V Mode |                                      |                                                    |      |     |      |
| DBTR1      | t <sub>c</sub> (TRC_CLK)             | Cycle time, TRC_CLK                                | 6.50 |     | ns   |
| DBTR2      | t <sub>w</sub> (TRC_CLKH)            | Pulse width, TRC_CLK high                          | 2.50 |     | ns   |
| DBTR3      | t <sub>w</sub> (TRC_CLKL)            | Pulse width, TRC_CLK low                           | 2.50 |     | ns   |
| DBTR4      | t <sub>osu</sub> (TRC_DATAV-TRC_CLK) | Output setup time, TRC_DATA valid to TRC_CLK edge  | 0.81 |     | ns   |
| DBTR5      | t <sub>oh</sub> (TRC_CLK-TRC_DATAI)  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 0.81 |     | ns   |
| DBTR6      | t <sub>osu</sub> (TRC_CTLV-TRC_CLK)  | Output setup time, TRC_CTL valid to TRC_CLK edge   | 0.81 |     | ns   |
| DBTR7      | t <sub>oh</sub> (TRC_CLK-TRC_CTLI)   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 0.81 |     | ns   |
| 3.3 V Mode |                                      |                                                    |      |     |      |
| DBTR1      | t <sub>c</sub> (TRC_CLK)             | Cycle time, TRC_CLK                                | 9.75 |     | ns   |
| DBTR2      | t <sub>w</sub> (TRC_CLKH)            | Pulse width, TRC_CLK high                          | 4.13 |     | ns   |
| DBTR3      | t <sub>w</sub> (TRC_CLKL)            | Pulse width, TRC_CLK low                           | 4.13 |     | ns   |
| DBTR4      | t <sub>osu</sub> (TRC_DATAV-TRC_CLK) | Output setup time, TRC_DATA valid to TRC_CLK edge  | 1.22 |     | ns   |
| DBTR5      | t <sub>oh</sub> (TRC_CLK-TRC_DATAI)  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 1.22 |     | ns   |
| DBTR6      | t <sub>osu</sub> (TRC_CTLV-TRC_CLK)  | Output setup time, TRC_CTL valid to TRC_CLK edge   | 1.22 |     | ns   |
| DBTR7      | t <sub>oh</sub> (TRC_CLK-TRC_CTLI)   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 1.22 |     | ns   |



SPRSP08\_Debug\_01

**Figure 6-113. Trace Switching Characteristics**

#### 6.10.6.2 JTAG

For more details about features and additional description information on the device IEEE 1149.1 Standard–Test–Access Port, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

#### Note

The JTAG signals are split across two IO power domains on the device. Timings parameters defined in this section only apply when the two IO power domains are operating at the same voltage and level-shifters are not inserted into the signal path. Values for the following timing parameters are not defined when operating the two IO power domains at different voltages since propagation delay through the device IO buffers differ when some are operating at 1.8 V while others are operating at 3.3 V. This effectively reduces timing margin beyond the values defined in this section. The JTAG interface is still expected to function when the two IO power domains are operated at different voltages, assuming the system designer has implemented appropriate level-shifters and the operating frequency is reduced to accommodate additional delay inserted by the level-shifters and IO buffers operating at different voltages.

**Table 6-98. JTAG Timing Conditions**

| PARAMETER                             |                                              | MIN  | MAX                 | UNIT |
|---------------------------------------|----------------------------------------------|------|---------------------|------|
| <b>Input Conditions</b>               |                                              |      |                     |      |
| SR <sub>I</sub>                       | Input slew rate                              | 0.50 | 2.00                | V/ns |
| <b>Output Conditions</b>              |                                              |      |                     |      |
| C <sub>L</sub>                        | Output load capacitance                      | 5    | 15                  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |      |                     |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | 83.5 | 1000 <sup>(1)</sup> | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |      | 100                 | ps   |

- (1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

#### 6.10.6.2.1 JTAG Electrical Data and Timing

Section 6.10.6.2.1.1, Section 6.10.6.2.1.2, and Figure 6-114 assume testing over the recommended operating conditions and electrical characteristic conditions.

##### 6.10.6.2.1.1 JTAG Timing Requirements

See Figure 6-114

| NO. |                           |                                                  | MIN                 | MAX | UNIT |
|-----|---------------------------|--------------------------------------------------|---------------------|-----|------|
| J1  | t <sub>c</sub> (TCK)      | Cycle time minimum, TCK                          | 46.5 <sup>(1)</sup> |     | ns   |
| J2  | t <sub>w</sub> (TCKH)     | Pulse width minimum, TCK high                    | 18.6 <sup>(2)</sup> |     | ns   |
| J3  | t <sub>w</sub> (TCKL)     | Pulse width minimum, TCK low                     | 18.6 <sup>(2)</sup> |     | ns   |
| J4  | t <sub>su</sub> (TDI-TCK) | Input setup time minimum, TDI valid to TCK high  | 4.5                 |     | ns   |
|     | t <sub>su</sub> (TMS-TCK) | Input setup time minimum, TMS valid to TCK high  | 4.5                 |     | ns   |
| J5  | t <sub>h</sub> (TCK-TDI)  | Input hold time minimum, TDI valid from TCK high | 2                   |     | ns   |
|     | t <sub>h</sub> (TCK-TMS)  | Input hold time minimum, TMS valid from TCK high | 2                   |     | ns   |

- (1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristics for the attached debugger. The operating frequency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.
- Minimum TDO setup time of 4.6 ns relative to the rising edge of TCK
  - TDI and TMS output delay in the range of –16.5 ns to 14.0 ns relative to the falling edge of TCK

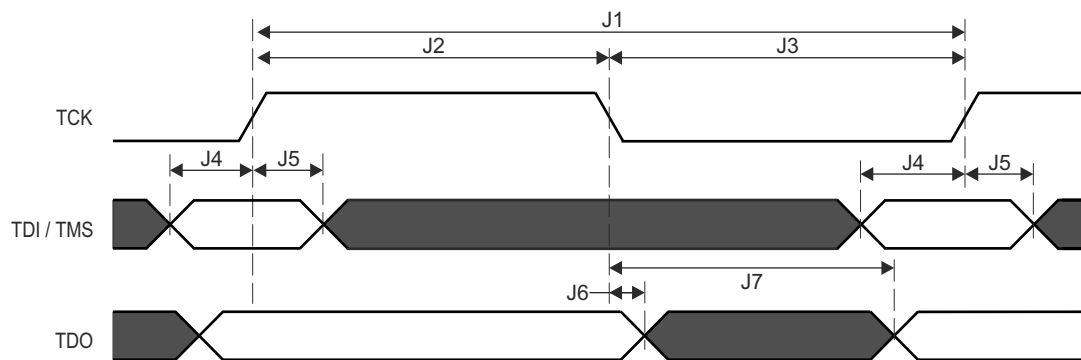
- (2) P = TCK cycle time in ns

##### 6.10.6.2.1.2 JTAG Switching Characteristics

See Figure 6-114

| NO. | PARAMETER                  |                                            | MIN | MAX | UNIT |
|-----|----------------------------|--------------------------------------------|-----|-----|------|
| J6  | t <sub>d</sub> (TCKL-TDOI) | Delay time minimum, TCK low to TDO invalid | 0   |     | ns   |
| J7  | t <sub>d</sub> (TCKL-TDOV) | Delay time maximum, TCK low to TDO valid   |     | 12  | ns   |

- The JTAG signals are split across two IO power domains on the device. Timings parameters defined in this table only apply when the two IO power domains are operating at the same voltage. Values for these timing parameters are not defined when operating the two IO power domains at different voltages since propagation delay through the device IO buffers differ when some are operating at 1.8V while others are operating at 3.3V. This effectively reduces timing margin beyond the values defined in this table. The JTAG interface is still expected to function when the two IO power domains are operated at different voltages, assuming the system designer has implemented appropriate level shifters and the operating frequency is reduced to accommodate additional delay inserted by the level-shifters and IO buffers operating at different voltages.



**Figure 6-114. JTAG Timing Requirements and Switching Characteristics**

## 7 Detailed Description

## 8 Applications, Implementation, and Layout

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

### 8.1 Device Connection and Layout Fundamentals

#### 8.1.1 Power Supply Decoupling and Bulk Capacitors

##### 8.1.1.1 Power Distribution Network Implementation Guidance

The [Powering Jacinto™ J7 SoC Family For Isolated Power Groups With TPS6594133A-Q1 PMIC and Dual HCPS Converters](#) User's Guide provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports *only* designs that follow the board design guidelines contained in the application report.

#### 8.1.2 External Oscillator

For more information about External Oscillators, see [Clock Specifications](#).

#### 8.1.3 JTAG and EMU

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the [XDS Target Connection Guide](#).

For more recommendations on EMU routing, see [Emulation and Trace Headers Technical Reference Manual](#)

#### 8.1.4 Reset

The device incorporates four external reset pins (MCU\_PORz, MCU\_RESETz, PORz, and RESET\_REQz) and two reset status pins (MCU\_RESETSTATz and RESETSTATz). These pins can be driven by an external power good circuitry or Power Management IC (PMIC). MCU\_PORz and Main PORz pins should be held active low during the entire power-up phase, and until all power supplies as well as the HFOSC0 clock are stable.

All MCU domain resets act as master resets to the whole device, whereas Main domain resets only reset Main domain (MCU domain is reset isolated from all Main domain resets).

#### 8.1.5 Unused Pins

For more information about Unused Pins, see [Pin Connectivity Requirements](#).

#### 8.1.6 Hardware Design Guide for Jacinto™ 7 Devices

The Hardware Design Guide for Jacinto™ 7 Devices document describes hardware system design considerations for the Jacinto™ 7 family of processors. This design guide is intended to be used as an aid during the development of application hardware.

### 8.2 Peripheral- and Interface-Specific Design Information

#### 8.2.1 LPDDR4 Board Design and Layout Guidelines

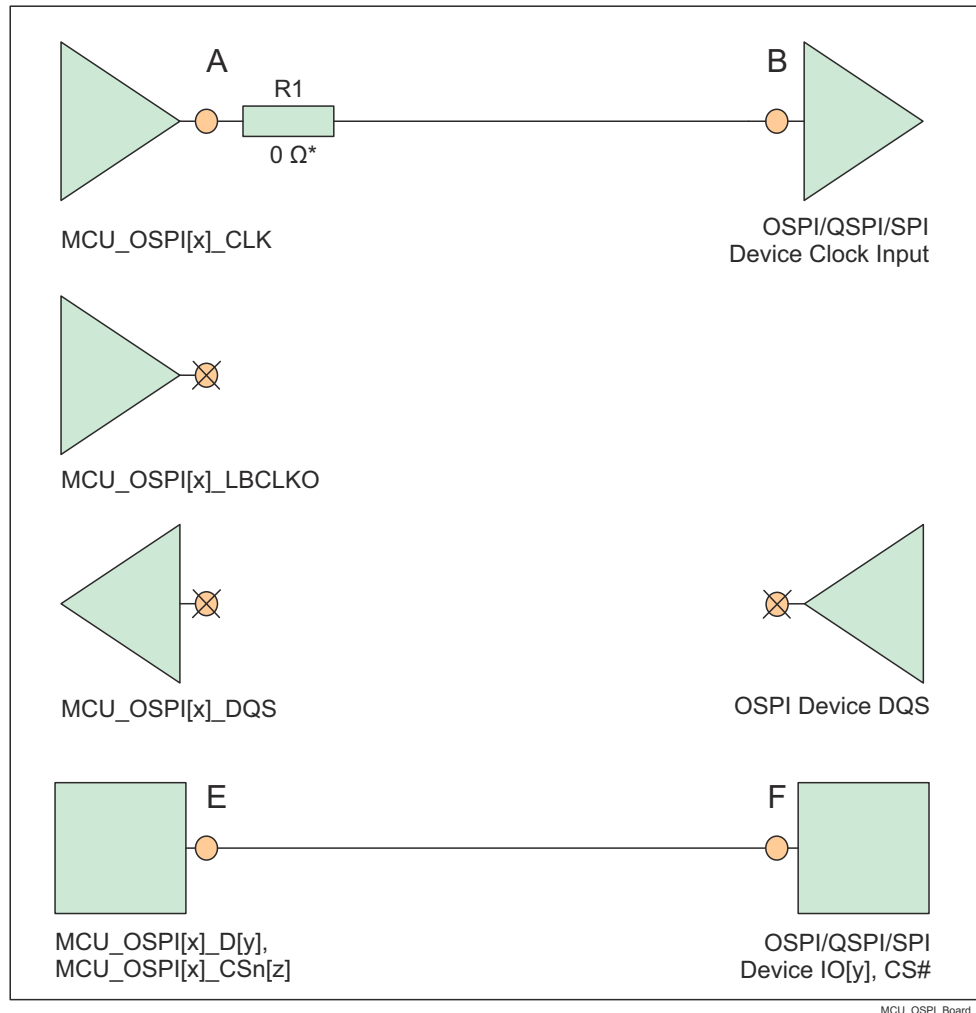
The goal of the [Jacinto 7 DDR Board Design and Layout Guidelines](#) is to make the LPDDR4 system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using LPDDR4 memories that follow the guidelines in this document.

## 8.2.2 OSPI and QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the OSPI and QSPI interfaces.

### 8.2.2.1 No Loopback and Internal Pad Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The signal propagation delay from the MCU\_OSPI[x]\_CLK signal to the flash device must be  $< 450$  ps ( $\sim 7$ cm as stripline or  $\sim 8$ cm as microstrip)
- $50\ \Omega$  PCB routing is recommended along with series terminations, as shown in [Figure 8-1](#)
- Propagation delays and matching:
  - A to B  $< 450$  ps
  - Matching skew:  $< 60$  ps



\*  $0\ \Omega$  resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK pin, is placeholder for fine tuning, if needed.

**Figure 8-1. OSPI Interface High Level Schematic**

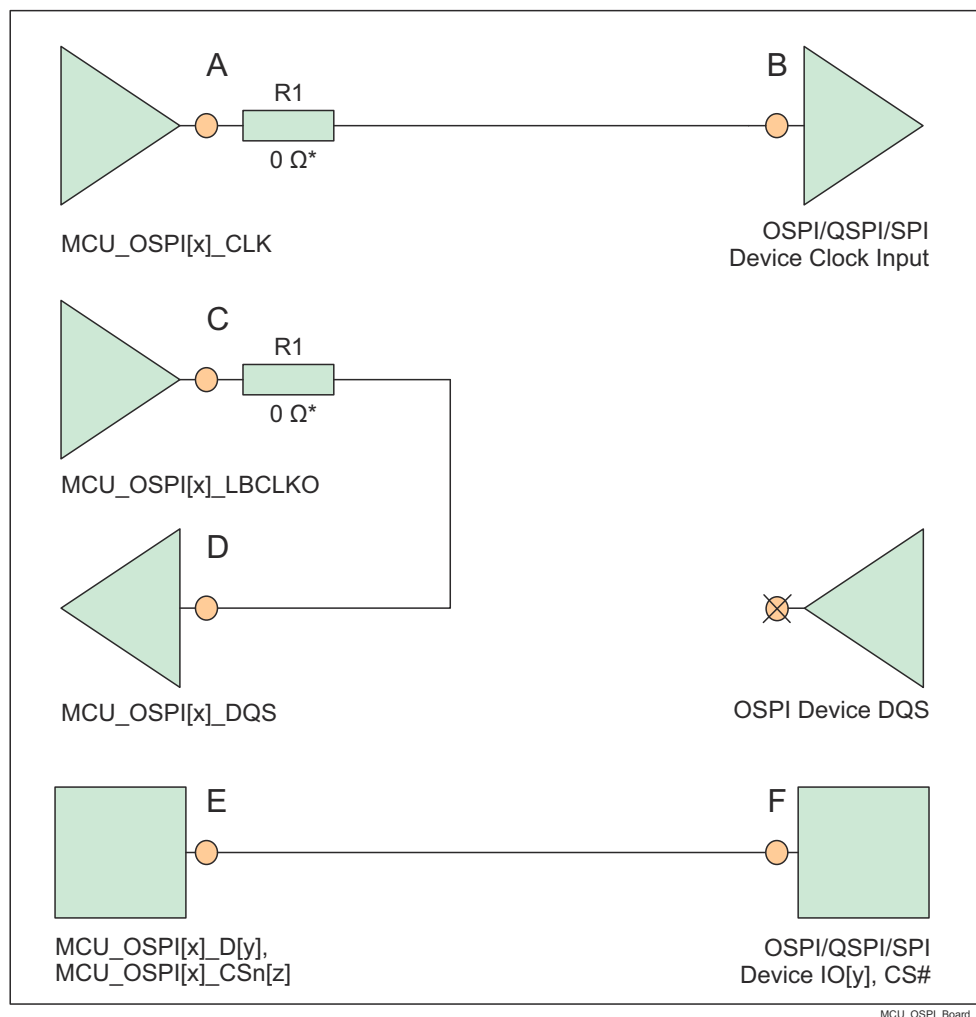
### 8.2.2.2 External Board Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The MCU\_OSPI[x]\_LBCLKO output signal must be looped back into the MCU\_OSPI[x]\_DQS input
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to half of the signal propagation delay from the MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin ((C to D)/2). See the note below.

- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) must be approximately equal to the signal propagation delay of the control and data signals between the flash device and the SoC device (E to F, or F to E)
- 50  $\Omega$  PCB routing is recommended along with series terminations, as shown in [Figure 8-2](#)
- Propagation delays and matching:
  - A to B = E to F = (C to D) / 2
  - Matching skew: < 60 ps

#### Note

The OSPI Board Loopback Hold time requirement (described in [OSPI](#)) is larger than the Hold time provided by a typical flash device. Therefore, the length of MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin (C to D) can be shortened to compensate.



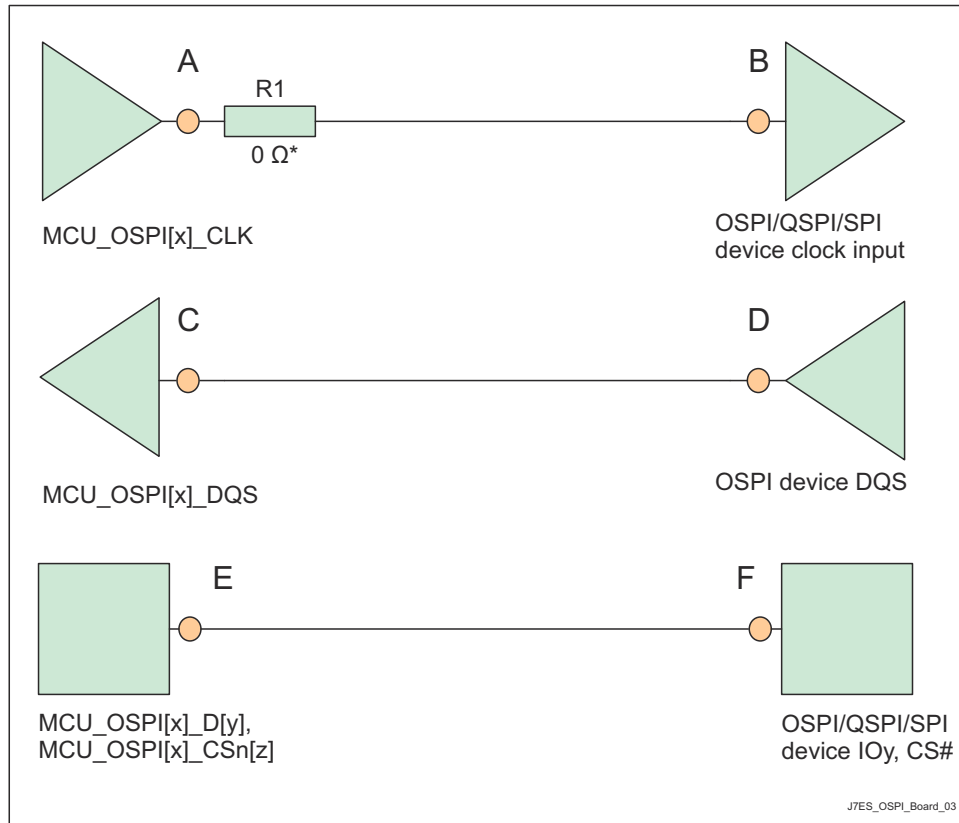
\* 0  $\Omega$  resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK and MCU\_OSPI[x]\_LBCLKO pins, is a placeholder for fine tuning, if needed.

**Figure 8-2. OSPI Interface High Level Schematic**

#### 8.2.2.3 DQS (only available in Octal Flash devices)

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The DQS pin of the flash devices must be connected to MCU\_OSPI[x]\_DQS signal

- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to the signal propagation delay from the MCU\_OSPI[x]\_DQS pin to the DQS output pin (C to D)
- 50  $\Omega$  PCB routing is recommended along with series terminations, as shown in [Figure 8-3](#)
- Propagation delays and matching:
  - A to B = C to D
  - Matching skew: < 60 ps



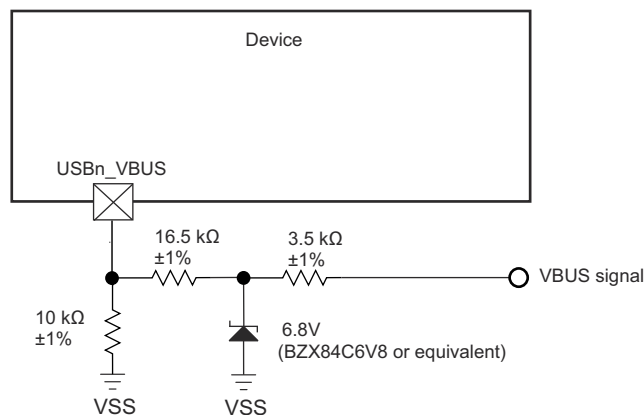
\* 0  $\Omega$  resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK pin, is a placeholder for fine tuning, if needed.

**Figure 8-3. OSPI Interface High Level Schematic**

### 8.2.3 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the [Figure 8-4](#)), which limits the voltage applied to the actual device pin (USB0\_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of zener diode at 5 V should be less than 100 nA.<sup>(1)</sup>



J7ES\_USB\_VBUS\_01

**Figure 8-4. USB VBUS Detect Voltage Divider / Clamp Circuit**

The USB0\_VBUS pin can be considered to be fail-safe because the external circuit in [Figure 8-4](#) limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

#### 8.2.4 System Power Supply Monitor Design Guidelines using VMON/POK

The VMON1\_ER\_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system. This supply is monitored by comparing the output of an external voltage divider circuit sourced by this supply with an internal voltage reference, with a power fail event being triggered when the voltage applied to VMON1\_ER\_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit. When designing the resistor divider circuit it is important to understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON1\_ER\_VSYS input threshold which has a nominal value of 0.45 V, with a variation of  $\pm 3\%$ . Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON1\_ER\_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON1\_ER\_VSYS input leakage current may be in the range of 10 nA to 2.5  $\mu$ A when applying 0.45 V.

#### Note

The resistor voltage divider shall be designed such that its output voltage never exceeds the maximum value defined in [Recommended Operating Conditions](#) during normal operating conditions.

[Figure 8-5](#) presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

For this example, it is important to understand which variables effect the maximum trigger threshold when selecting resistor values. It is obvious a device which has a VMON1\_ER\_VSYS input threshold of 0.45 V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but how these contributions effect the maximum trigger point may not be obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON1\_ER\_VSYS pin is 2.5  $\mu$ A. When implementing a resistor divider where R1 = 4.81 K $\Omega$  and R2 = 40.2 K $\Omega$ , the result is a maximum trigger threshold of 4.523 V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45 V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input

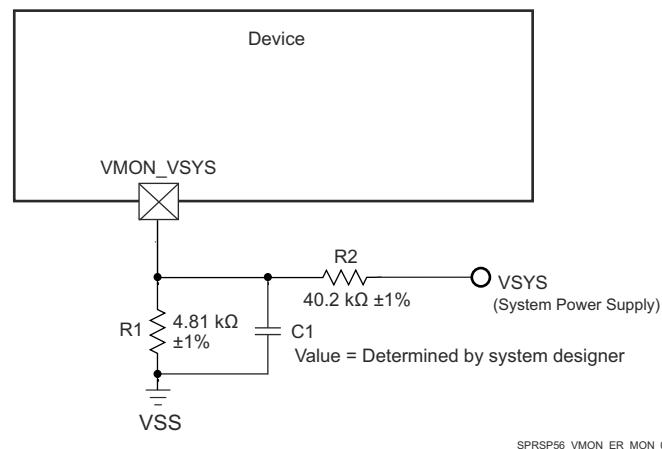
leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.008 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.008 V to 4.523 V. Approximately 250 mV of this range is introduced by VMON1\_ER\_VSYS input threshold accuracy of  $\pm 3\%$ , approximately 150 mV of this range is introduced by resistor tolerance of  $\pm 1\%$ , and approximately 100 mV of this range is introduced by loading error when VMON1\_ER\_VSYS input leakage current is 2.5  $\mu\text{A}$ .

The resistor values selected in this example produces approximately 100  $\mu\text{A}$  of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above could be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer should also consider implementing a noise filter on the voltage divider output since VMON1\_ER\_VSYS has minimum hysteresis and a high-bandwidth response to transients. This could be done by installing a capacitor across R1 as shown in Figure 8-5. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

Figure 8-5 presents an example, when the system power supply voltage is nominally 5 V and the desired trigger threshold is -10% or 4.5 V.



**Figure 8-5. System Supply Monitor Voltage Divider Circuit**

The **VMON2\_IR\_VCPU** pin provides a way to monitor VDD\_CPU power supply. TI recommends that **VMON2\_IR\_VCPU** pin be externally connected as close as possible to VDD\_CPU pin on the board. SoCs that have a **VMON6\_IR\_VEXT0P8** can optionally monitor other domains such as VDD\_CORE or VDD\_MCU. Similarly, those signals should be as close as possible to VDD\_CORE or VDD\_MCU pin on the board.

The **VMON3\_IR\_VEXT1P8** and **VMON4\_IR\_VEXT1P8** pins provide a way to monitor an external 1.8-V power supply. The **VMON5\_IR\_VEXT3P3** pin provides a way to monitor an external 3.3-V power supply. An internal resistor divider with software control is implemented inside the SoC. Software can program the internal resistor divider to create appropriate under voltage and over voltage interrupts. These pins should not be sourced from an external resistor divider. If the monitored voltage requires adjustment, be sure to buffer the divided voltage prior connecting to monitor pin.

### 8.2.5 High Speed Differential Signal Routing Guidance

The [High Speed Interface Layout Guidelines](#) provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

### 8.2.6 Thermal Solution Guidance

The [Thermal Design Guide for DSP and ARM Application Processors](#) provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers, see the Package Option Addendum of this document, the TI website ([ti.com](https://www.ti.com)), or contact your TI sales representative.

### 9.1.1 Standard Package Symbolization

#### Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

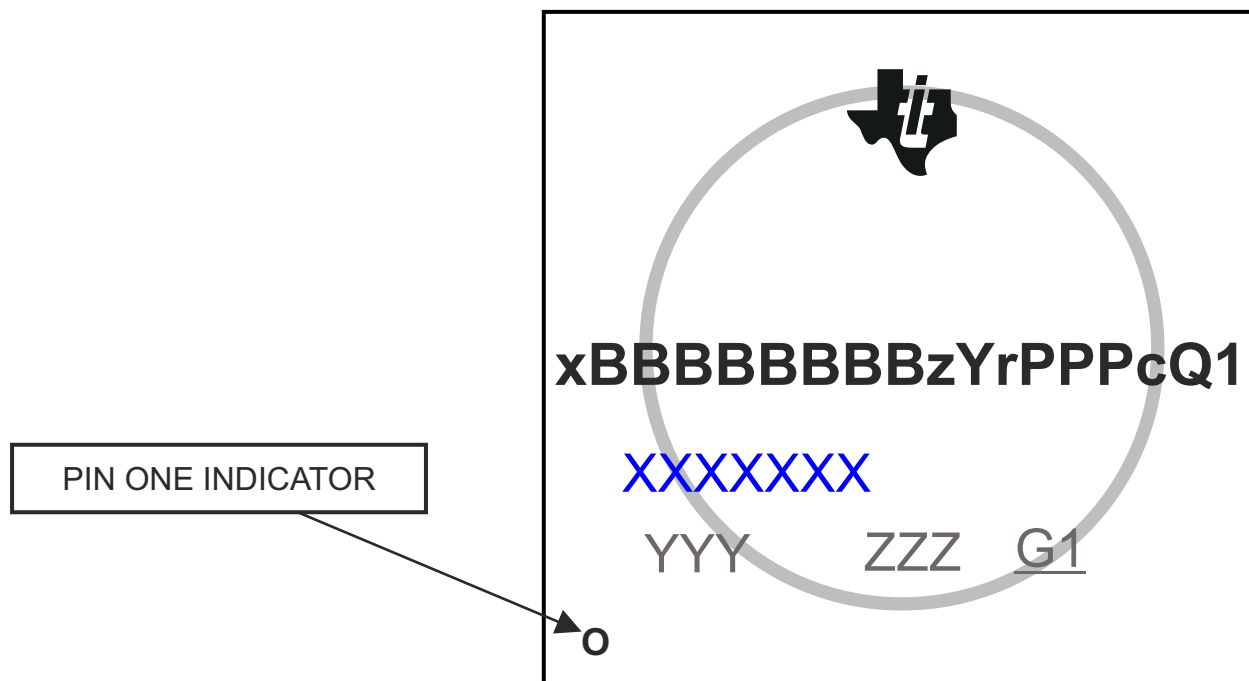


Figure 9-1. Printed Device Reference

## 9.1.2 Device Naming Convention

### Note

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

**Table 9-1. Nomenclature Description**

| FIELD PARAMETER | FIELD DESCRIPTION                                 | VALUE                | DESCRIPTION                                                                                  |
|-----------------|---------------------------------------------------|----------------------|----------------------------------------------------------------------------------------------|
| a               | Device evolution stage                            | X                    | Prototype                                                                                    |
|                 |                                                   | P                    | Preproduction (production test flow, no reliability data)                                    |
|                 |                                                   | BLANK <sup>(1)</sup> | Production                                                                                   |
| BBBBBB          | Base production part number                       | AM68A9               | See <a href="#">Device Comparison</a> ,                                                      |
|                 |                                                   | AM68A7               |                                                                                              |
|                 |                                                   | AM685                |                                                                                              |
|                 |                                                   | AM683                |                                                                                              |
| r               | Device revision                                   | A                    | SR1.0                                                                                        |
| Z               | Device Speed Grade                                | T                    | See <a href="#">Speed Grade Maximum Frequency</a> .                                          |
|                 |                                                   | H                    |                                                                                              |
|                 |                                                   | OTHER                | Alternate speed grade                                                                        |
| f               | Features (see <a href="#">Device Comparison</a> ) | G                    | Base, no additional Features                                                                 |
| Y               | Functional Safety <sup>(3)</sup>                  | G                    | Non-Functional Safety                                                                        |
| y               | Security                                          | G                    | Non-Secure                                                                                   |
|                 |                                                   | Other                | Secure                                                                                       |
| t               | Temperature <sup>(2)</sup>                        | A                    | –40°C to 105°C - Extended Industrial (see <a href="#">Recommended Operation Conditions</a> ) |
|                 |                                                   | H                    | 0°C to 95°C - Commercial (see <a href="#">Recommended Operation Conditions</a> )             |
|                 |                                                   | I                    | –40°C to 125°C - Automotive (see <a href="#">Recommended Operation Conditions</a> )          |
| PPP             | Package Designator                                | ALZ                  | FCBGA (770-pin; 23 mm x 23 mm)                                                               |
| Q1              | Automotive Designator                             | Q1                   | Auto Qualified (Q100)                                                                        |
|                 |                                                   | BLANK <sup>(1)</sup> | Standard                                                                                     |
| xxxxxxx         | Lot Trace Code (LTC)                              |                      |                                                                                              |
| YYY             | Production Code, For TI use only                  |                      |                                                                                              |
| ZZZ             | Production Code, For TI use only                  |                      |                                                                                              |
| O               | Pin one designator                                |                      |                                                                                              |
| G1              | ECAT - Green package designator                   |                      |                                                                                              |

(1) BLANK in the symbol or part number is collapsed so there are no gaps between characters.

(2) Applies to device max junction temperature.

(3) Functional Safety is not supported on this device family, if interested in this feature, please see the [TDA4VE device family](#).

## 9.2 Tools and Software

The following products support development for TDA4VM platforms:

### Development Tools

**Code Composer Studio™ Integrated Development Environment** Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever

before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

**SYSCONFIG Tool** System Configuration Tool To help simplify configuration challenges and accelerate software development, TI created SysConfig, an intuitive and comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose, and resolve conflicts visually so that you have more time to create differentiated applications. The SysConfig tool is integrated in Code Composer Studio™ (CCS) IDE, as a standalone installer, or can be used via the [dev.ti.com](https://dev.ti.com) cloud tools portal.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at [ti.com](https://ti.com). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

### 9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the TDA4x/AM69A devices.

#### Technical Reference Manual

**TDA4AL, TDA4VL, TDA4VE, AM68A Technical Reference Manual** Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the TDA4VM family of devices.

#### Errata

**J721S2, TDA4VE, TDA4AL, TDA4VL, AM68A Processor Silicon Revision 1.0, Silicon Errata** Describes the known exceptions to the functional specifications for the device.

### 9.4 Trademarks

eMMC™ is a trademark of MultiMediaCard Association.

Jacinto™, C7000™, and TI E2E™ are trademarks of Texas Instruments.

Code Composer Studio™ is a trademark of TI.

Arm® and Cortex® are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

PCI-Express® is a registered trademark of PCI-SIG.

Secure Digital® is a registered trademark of SD Card Association.

All trademarks are the property of their respective owners.

### 9.5 Support Resources

**TI E2E™ support forums** are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.7 Glossary

#### TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

### Changes from August 18, 2023 to December 13, 2024 (from Revision A (August 2023) to Revision B (DECEMBER 2024))

|                                                                                                                                                                                                                                                 | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • (Features): Deleted the "OLDI/LVDS (4 lanes - 2x) and 24-bit RGB parallel interface" bullet under the <i>Display subsystem supports</i> : .....                                                                                               | 1    |
| • <b>Global</b> :: Added "(active-low)" and verified "O" Pin Type for the PMIC_WAKE0 and PMIC_WAKE1 signals, where applicable. Deleted the "n" suffix from the Signal and Ball Names.....                                                       | 1    |
| • (Features): Updated/Changed the CSI2.0 bullet and added sub-bullets.....                                                                                                                                                                      | 1    |
| • (Pin Attributes): Added more description for each column header in Pin Attributes Header List.....                                                                                                                                            | 10   |
| • (Pin Attributes): Added Ball State DURING Reset and Ball State AFTER Reset information for MMC0_* pins in the <i>Pin Attributes (ALZ Package)</i> table.....                                                                                  | 13   |
| • (VMON Signal Descriptions): Updated/Changed the <b>DESCRIPTION</b> for the VMON2_IR_VCPU signal name.....                                                                                                                                     | 98   |
| • (CSI2/DSI D-PHY Electrical Characteristics): Delete the table and added a compliance specifications Note.....                                                                                                                                 | 113  |
| • (SERDES Electrical Characteristics): Added USXGMII Note to show compliance with IEEE 802.3 Clause 72-7 and Annex 69B.....                                                                                                                     | 116  |
| • (ROC for OTP eFuse Programming): Removed legacy PMIC part number from footnote.....                                                                                                                                                           | 117  |
| • (Recommended Operating Conditions for OTP eFuse Programming): Added the SR <sub>(VPP)</sub> , VPP Power-up Slew Rate parameter to clarify the limit associated with this parameter only applies during power-up.....                          | 117  |
| • (Combined MCU and Main Domains Power- Up Sequencing): Updated note that starts with "VDD_MCU is a digital voltage domain ..." to clarify VDD_MCU grouping and sequence constraints.....                                                       | 123  |
| • (Isolated MCU and Main Domains Power-Up Sequencing): Updated note that starts with "VDD_MCU is a digital voltage domain ..." to clarify VDD_MCU grouping and sequence constraints.....                                                        | 127  |
| • (WKUP_OSC0 Internal Oscillator Clock Source): Updated/Changed the C <sub>shunt</sub> , Crystal Circuit Shunt Capacitance content in the <i>WKUP_OSC0 Crystal Electrical Characteristics</i> table.....                                        | 145  |
| • (WKUP_OSC0 Internal Oscillator Clock Source): Added a footnote to define the MAX ESR <sub>xtal</sub> , Crystal Effective Series Resistance value based on the C <sub>shunt</sub> , Crystal Circuit Shunt Capacitance parameter selection..... | 145  |
| • (WKUP_OSC0 Switching Characteristics – Crystal Mode [Table]): Updated/Changed the XI, XO, and XI to XO capacitance MAX values.....                                                                                                            | 145  |
| • (Auxiliary OSC1 Internal Oscillator Clock Source): Updated/Changed the C <sub>shunt</sub> , Crystal Circuit Shunt Capacitance content in the <i>OSC1 Crystal Electrical Characteristics</i> table.....                                        | 150  |
| • (OSC1 Switching Characteristics – Crystal Mode [Table]): Updated/Changed the XI, XO, and XI to XO capacitance MAX table values.....                                                                                                           | 150  |
| • (GPIO): Updated/Changed the lead-in content with just TRM and Signal Descriptions references.....                                                                                                                                             | 170  |
| • (GPIO): Updated/Changed the SR <sub>I</sub> , Input slew rate, I2C OD FS MAX value from "0.8" to "0.08" V/ns in the <i>GPIO Timing Conditions</i> table.....                                                                                  | 170  |
| • (HyperBus): Added the MIN and MAX values for C <sub>L</sub> , Output load capacitance in the HyperBus Timing Conditions table, under OUTPUT CONDITIONS.....                                                                                   | 194  |
| • (I2C Timing): Updated/Changed the typo on the slew rate from "0.8" to "0.08" V/ns ( <i>which is equivalent to the stated value of 8E+7</i> ) on the rise and fall times of the I2C signals bullet.....                                        | 196  |
| • (MCSPI Timing Requirements - Controller Mode): Updated/Changed the MIN value of SM1, t <sub>c(spiclk)</sub> , Cycle time, SPI_CLK from "20.8" to "20" ns.....                                                                                 | 204  |
| • (MCSPI Switching Characteristics - Peripheral Mode): Updated/Changed the MIN value of SS1, t <sub>c(spiclk)</sub> , Cycle time, SPI_CLK from "20.8" to "20" ns.....                                                                           | 206  |
| • (MMC0 Timing Requirements – HS400 Mode): Added new table and associated timing image.....                                                                                                                                                     | 214  |
| • (MMC0 Switching Characteristics – HS400 Mode): Replaced the Delay time parameters HS4008 and HS4009 with Output setup and Output hold parameters HS4008, HS4009, HS40010, and HS40011.....                                                    | 214  |
| • (eMMC in – HS400 Mode – Transmitter Mode): Updated the timing diagram to match the new definitions associated with parameters HS4008, HS4009, HS40010, and HS40011.....                                                                       | 214  |

|                                                                                                                                                                                          |     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| • (MMC1/2 - SD/SDIO Interface/ UHS-I DDR50 Mode): Updated/Changed the $f_{op(clk)}$ , Operating frequency, MMC[x]_CLK MAX value from "40" to "50" MHz.....                               | 223 |
| • (MMC1/2 - SD/SDIO Interface/ UHS-I DDR50 Mode): Updated/Changed the DDR505, $t_{c(clk)}$ , Cycle time, MMC[x]_CLK MIN value from "25" to "20" ns.....                                  | 223 |
| • (OSPI Timing Conditions): Added Input slew rate 1.8V, PHY Data Training DDR with DQS row to table.....                                                                                 | 225 |
| • (OSPI Timing Conditions): Updated "3.3V" and "All other modes" mode description.....                                                                                                   | 225 |
| • (OSPI0/1 With PHY Data Training): Added new section.....                                                                                                                               | 227 |
| • (OSPI Switching Characteristics – PHY SDR Mode): Corrected the formulas associated with timing parameters O10 and O11.....                                                             | 230 |
| • (OSPI Switching Characteristics – PHY DDR Mode): Corrected the formulas associated with timing parameters O4 and O5.....                                                               | 232 |
| • (OSPI0/1 Timing Requirements – Tap SDR Mode): Updated/Changed the constant values associated with the Setup time and Hold time MIN formulas in the O19 and O20 parameters.....         | 234 |
| • (OSPI0/1 Timing Requirements – Tap SDR Mode): Updated/Changed the R= footnotes "refclk" to "reference clock" to match the clock name used in the Technical Reference Manual (TRM)..... | 234 |
| • (OSPI0/1 Timing Requirements – Tap DDR Mode): Updated/Changed the constant values associated with the Setup time and Hold time MIN formulas in the O13 and O14 parameters.....         | 236 |
| • (OSPI0/1 Timing Requirements – Tap DDR Mode): Updated/Changed the R= footnotes "refclk" to "reference clock" to match the clock name used in the Technical Reference Manual (TRM)..... | 236 |
| • (OSPI0/1 Switching Characteristics – Tap DDR Mode): Updated/Changed the data output delay MIN and MAX formulas in the O6 parameter.....                                                | 236 |
| • (Power Distribution Network Implementation Guidance): Updated/Changed the user's guide doc title and ulink association.....                                                            | 244 |
| • (System Power Supply Monitor Design Guidelines using VMON/POK): Updated/Changed "The VMON2_IR_VCPU pin ..." paragraph.....                                                             | 248 |

## 11 Mechanical, Packaging, and Orderable Information

### 11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)         |
|-----------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-----------------------------|
| AM6852ATGGHAALZR      | Active        | Production           | FCBGA (ALZ)   770 | 250   LARGE T&R       | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM6852A<br>TGGHAALZ<br>206  |
| AM68A92ATGGHAALZF     | Active        | Production           | FCBGA (ALZ)   770 | 250   LARGE T&R       | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM68A92A<br>TGGHAALZ<br>206 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "--" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

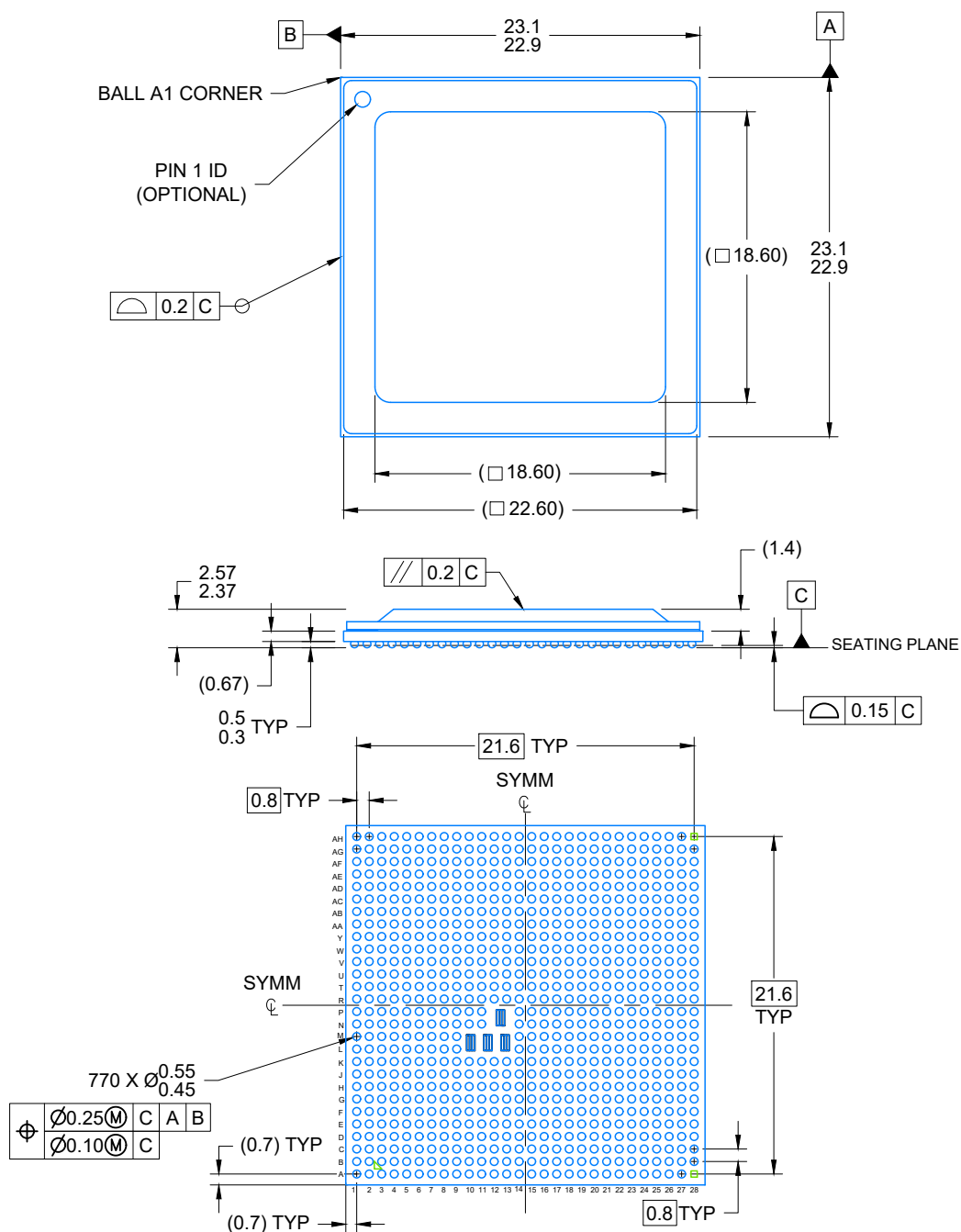
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## PACKAGE OUTLINE

### FCBGA - 2.57 mm max height

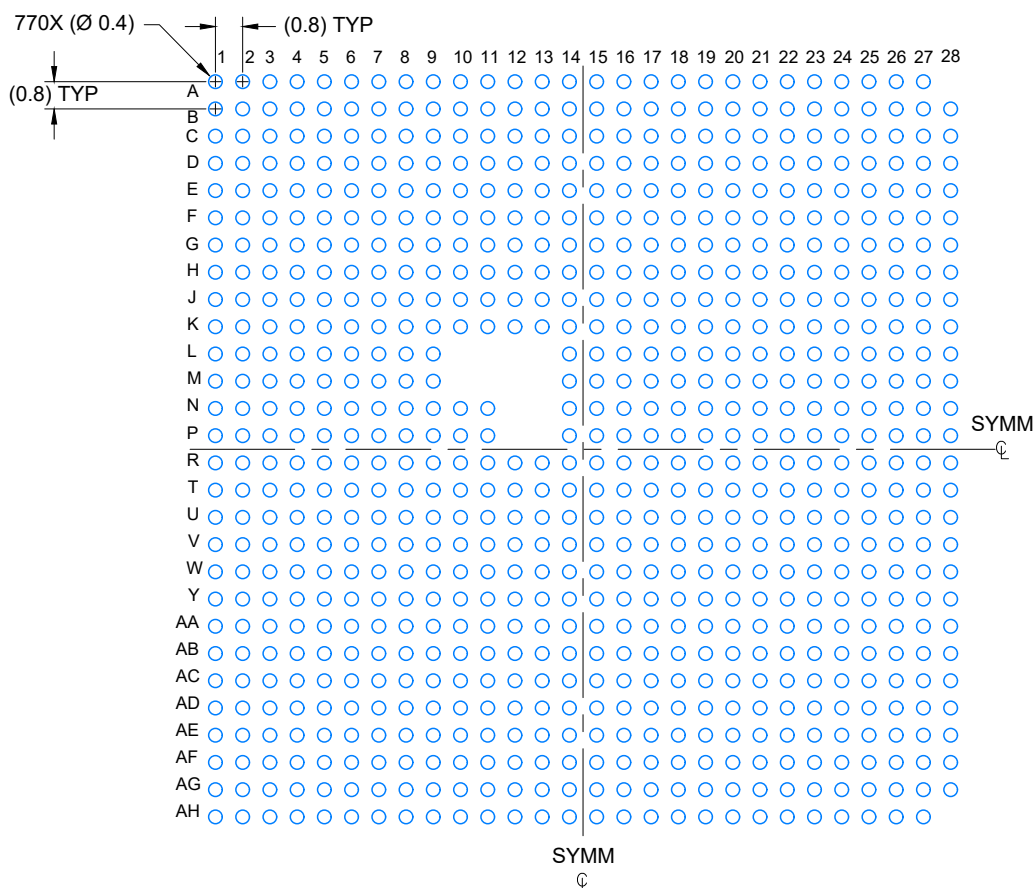
## BALL GRID ARRAY



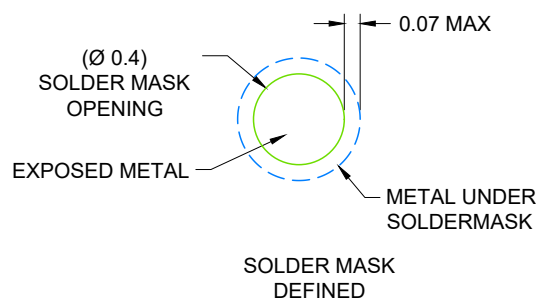
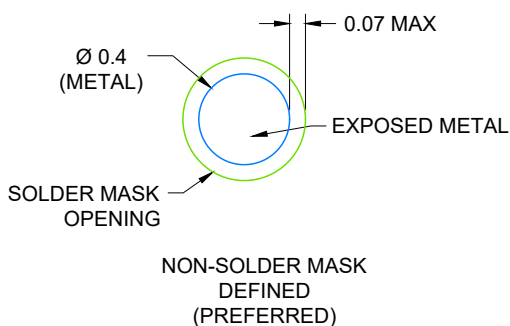
4226636/B 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 0.225X



SOLDER MASK DETAILS  
NOT TO SCALE

4226636/B 03/2024

## NOTES: (continued)

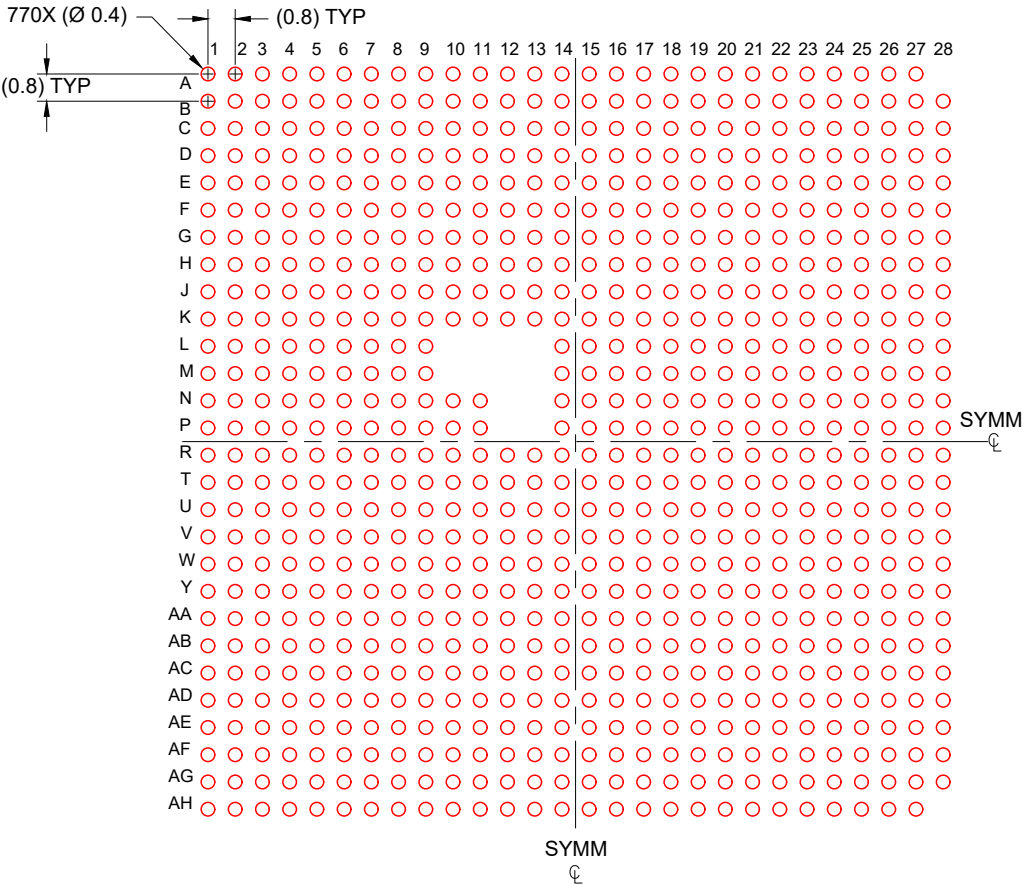
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

ALZ0770A

FCBGA - 2.57 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE: 0.225X

4226636/B 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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