MIXED SIGNAL MICROCONTROLLER

Check for Samples: AFE4110

FEATURES

- **Ultra Low Supply-Voltage (ULV) Range**
  - **1.1V - 1.55V Unregulated Single Cell Battery Operation (CPU, System Core, and Timers)**
  - **3mA 1.85V Internal Charge Pump for External EEPROM (R/W), VDDIO, and Internal LCD Controller**
  - **60µA 3.3V Regulated Charge Pump for LCD Drive Pads**
- **Low Power Consumption**
  - **Active Mode (AM): 45µA/MHz (1.55V)**
  - **Standby Mode (LPM3, LCD): < 25µA**
  - **Deep Sleep Mode (LPM5):<0.4µA**
  - **8-Bytes Battery Backed RAM for Calibration Retention**
  - **Wakeup From Periodic Timer or External Interrupt**
  - **Wake-Up from LPM5 in 10ms, Wake-Up from LPM4 in 5µs**
- **16-Bit RISC Architecture**
  - **Extended Instructions**
  - **125ns Instruction Cycle Time**
- **Compact Clock System**
  - **Internal Trimmable High Frequency Clock Oscillator with Discrete Frequency Selections Between 1MHz and 5.4MHz**
  - **20kHz Internal low Frequency Clock Oscillator**
  - **External Clock Input (Upto 8MHz)**
  - **32kHz Crystal Oscillator**
- **Internal High Frequency Oscillator Frequency Correction**
  - **Facilitates Generation and Measurement of Real Time Intervals Without a Clock Crystal**
  - **Utilizes Factory Calibration (E-Fuse), S/W, and a Single External 1MΩ Resistor**
- **Integrated LCD Controller**
  - **Drives 4-Mux, 3-Mux, 2-Mux, or Static Mode LCDs**
  - **Up to 48 (4x12) LCD Segments**
- **Two 16-Bit Timer0_A3 with Three Capture/Compare Registers**

- **Extended Input Multiplexer for High Accuracy RC Discharge Measurement**
- **ULV Analog Pool**
  - **8-Bit Analog-to-Digital Converter (ADC)**
  - **8-Bit Digital-to-Analog Converter (DAC)**
  - **Programmable Comparator (COMP)**
  - **Supply-Voltage-Monitoring (SVM)**
  - **Internal Temperature Sensor**
  - **Internal Voltage Reference**
  - **1V Regulated (LDO) Outputs**
- **32-Bit Watch-Dog-Timer (WDT-A)**
- **21-Configurable Analog I/O or Digital GPIO Pads,**
  - **2-Power GPIO for 10mA V_{DD}/1.85/3.6V Buzzer Load**
  - **10-GPIO for VDDIO Operation with V_{DD}/1.85/3.6V Internal Level Shifting**
  - **11-GPIO for VDD Operation (1.1V - 1.55V)**
  - **4-Regulated 1V (LDO) Analog Outputs**
  - **1-250mV DAC Analog Output**
  - **6-Analog Comparator/ADC Inputs**
- **SPI EEPROM Bootstrap Loader (AFE4110A)**
- **Full Four Wire JTAG Debug Interface**
- **Family Members Include:**
  - *AFE4110B*:
    - **512B RAM Memory**
    - **16KB ROM (TI PSUC, Custom)**
    AFE4110A:
    - **14KB RAM + 512B RAM**
    - **16KB ROM (TI DSUC,TI Bootloader)**
- **55-Bonding Pads Available as Tested Wafers, See the Ordering Information for Other Options**

APPLICATIONS

- **For any application requiring a full analog signal chain and an LCD display driver such as digital thermometers, pedometers, thermostats, and other portable single alkaline battery devices.**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The Texas Instruments MSP430 family of low-power mixed signal ASSPs consists of many devices featuring different sets of peripherals targeted for various consumer medical applications. The AFE4110 CPU architecture is based on the popular ultra low power Texas Instruments MSP430 RISC processor.
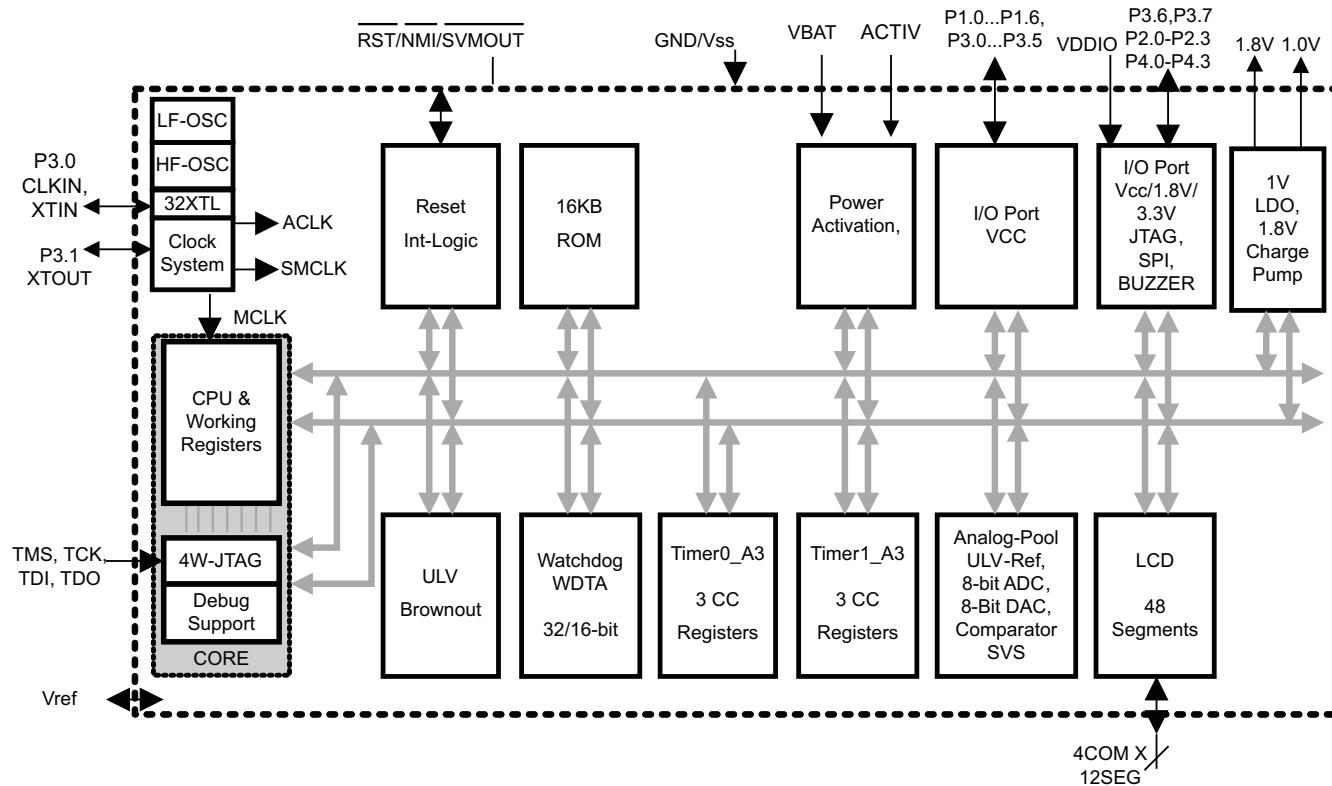
The AFE4110 configuration with two 16-bit timers, integrated 48-segment LCD driver, programmable Analog Pool, supply voltage monitor and internal reference voltage source is particularly well suited for implementation of low cost digital thermometers operating from a single cell SR60 battery. The capability to correct the on chip high frequency oscillator output facilitates the generation and measurement of real time intervals. For many applications, this capability allows system designers to eliminate a clock crystal from the system BOM.

ORDERING INFORMATION[1]

T_A	ORDERABLE PART
0ºC to 70ºC	AFE4110B000YS

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTIONAL BLOCK DIAGRAM, AFE4110

ABSOLUTE MAXIMUM RATINGS[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	VALUE		UNIT
	MIN	**MAX**	
Voltage applied at V_{DD} referenced to V_{SS} (V_{AMR})	–0.3	1.8	V
Voltage applied to any pin (references to V_{SS})	–0.3	V_{DD} + 0.3	V
	–0.3	1.8	V
Diode current at any device pin[2]		± 2.5	mA
Storage temparature range[3]	–55	150	°C
ESD tolerance HBM		2000	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

RECOMMENDED OPERATING CONDITIONS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage during program execution	1.1		1.55	V
V_{SS}	Supply voltage (GND reference)		0		V
T_A	Operating free-air temperature	0		70	°C
CV_{DD}	Capacitor on V_{DD}		470		nF
f_{SYSTEM}[1][2]	V_{DD} > 1.1 V			1	MHz
	V_{DD} > 1.5 V			4	

(1) The AFE4110 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulsewidth of the specified maximum frequency.
(2) Modules may have a different maximum input clock specification.See the specification of the respective module in this data sheet.

Active Mode Supply Current (Into V$_{CC}$) [1][2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V$_{DD}$	T$_A$	MIN	TYP	MAX	UNIT
I$_{AM,1MHz}$	f$_{MCLK}$ = f$_{SMCLK}$ = 1 MHz, f$_{ACLK}$ = 20 kHz, Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	1.3 V	30°C		72		µA
		1.55 V			86		
	f$_{MCLK}$ = f$_{SMCLK}$ = 1 MHz, f$_{ACLK}$ = 20 kHz, Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	1.3 V	70°C		74		µA
		1.55 V			88		
I$_{AM,125kHz}$	f$_{MCLK}$ = f$_{SMCLK}$ = 125 kHz, f$_{ACLK}$ = 20 kHz Program executes in RAM CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	1.3 V	30°C		33		µA
		1.55 V			37		
	f$_{MCLK}$ = f$_{SMCLK}$ = 125 kHz, f$_{ACLK}$ = 20 kHz, Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	1.3 V	70°C		35		µA
		1.55 V			40		
I$_{AM}$/MHz	f$_{MCLK}$ = f$_{SMCLK}$: 1 to 5 MHz, f$_{ACLK}$ = 20 kHz Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	1.3 V	30°C		45		µA/ MHz

(1)   All inputs are tied to 0 V or to V$_{DD}$. Outputs do not source or sink any current.
(2)   Characterized with program executing typical data processing "Type2".

Low-Power Mode Supply Current (Into V$_{CC}$) [1][2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V$_{DD}$	T$_A$	MIN	TYP	MAX	UNIT
I$_{LPM0}$	f$_{MCLK}$ = f$_{SMCLK}$ = 1 MHz, f$_{ACLK}$ = 20 kHz CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	1.3 V	30°C		8.3	11	µA
		1.55 V			9.5	12	
		1.3 V	70°C		11	14	
		1.55 V			12	17	
I$_{LPM1}$	f$_{MCLK}$ = f$_{SMCLK}$ = 1 MHz, f$_{ACLK}$ = 20 kHz CPUOFF = 1, SCG0 = 1, SCG1 = 0, OSCOFF = 0	1.3 V	30°C		8.3	11	µA
		1.55 V			9.5	12	
		1.3 V	70°C		11	14	
		1.55 V			12	17	
I$_{LPM2,1MHz}$	f$_{MCLK}$ = f$_{SMCLK}$ = 1MHz, f$_{ACLK}$ = 1MHz CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	1.3 V	30°C		28	32	µA
		1.55 V			29	33	
		1.3 V	70°C		30	35	
		1.55 V			32	38	
I$_{LPM2,20kHz}$	f$_{MCLK}$ = f$_{SMCLK}$ = f$_{ACLK}$ = 20 kHz CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	1.3 V	30°C		8.3	12	µA
		1.55 V			9.5	13	
		1.3 V	70°C		11	15	
		1.55 V			12	17	
I$_{LPM3}$	f$_{MCLK}$ = f$_{SMCLK}$ = f$_{ACLK}$ = 20 kHz CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	1.3 V	30°C		8.3	11	µA
		1.55 V			9.5	12	
		1.3 V	70°C		11	14	
		1.55 V			12	17	
I$_{LPM4}$	f$_{MCLK}$ = f$_{SMCLK}$ = f$_{ACLK}$ = 20 kHz CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	1.3 V	30°C		6	7.9	µA
		1.55 V			7.8	10	
		1.3 V	70°C		8.6	12	
		1.55 V			11	16	

(1)   Current for WDT clocked by ACLK included.
(2)   Current for Brownout included.

Product Folder Link(s) :*AFE4110*

Ports P1, P3 (except for P3.6, P3.7), $\overline{\text{RST}}$, $\overline{\text{NMI}}$, $\overline{\text{SVMOUT}}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	V_{DD} = 1.1 V, I_{OH} = −1 mA[1] for ports P1, P3	V_{DD}-0.25			V
	V_{DD} = 1.55 V, I_{OH} = −1 mA[1] for ports P1, P3	V_{DD}-0.15			
	V_{DD} = 1.1 V, I_{OH} = −300 µA[1] for ports P1, P3	V_{DD}-0.15			
V_{OL}	V_{DD} = 1.1 V, I_{OL} = 2.5 mA[2] for ports P1, P3			0.2	V
	V_{DD} = 1.55 V, I_{OL} = 2.5 mA[2] for ports P1, P3			0.15	
	V_{DD} = 1.1 V, I_{OL} = 300 µA[2] for ports P1, P3			0.07	
V_{IL}	V_{DD} = 1.55 V			0.3 x V_{DD}	V
	V_{DD} = 1.1 V			0.25 x V_{DD}	V
V_{IH}	V_{DD} = 1.55 V	0.7 x V_{DD}			V
	V_{DD} = 1.55 V	0.75 x V_{DD}			V
V_{HYS}	Intrinsic Hysteresis		150		mV
$\Delta t/\Delta v$	V_{DD} = 1.1V, C_L = 15 pF || R_L = 750Ω to Vss on V_{OH} for ports P1, P3			75	ns/V
	V_{DD} = 1.1 V, C_L = 15 pF || R_L = 320Ω to Vcc on V_{OL} for ports P1, P3			75	
	V_{DD} = 1.55 V, C_L = 25 pF || R_L= 1600Ω to Vss on V_{OH} for ports P1, P3			75	
	V_{DD} = 1.55 V, C_L = 25 pF || R_L= 600Ω to Vss on V_{OL} for ports P1, P3			75	
I_{OH}	V_{DD} = 1.1 V – 1.55 V for ports P1, P3	−1			mA
I_{OL}	V_{DD} = 1.1 V – 1.55 V for ports P1, P3	2.5			mA
I_{LKG}	V_{DD} = 1.1 V – 1.55 V			±100	nA
t_{INT}	P0.x; V_{DD} = 1.1 V – 1.55 V		200		ns
R_{PULL}	For pullup:V_{IN} = V_{SS}; For pulldown: V_{IN} = V_{DD} for ports P1, P3	30	35	40	kΩ
R_{RST}	Pullup on $\overline{\text{RST}}$, $\overline{\text{NMI}}$, $\overline{\text{SVMOUT}}$	30	35	40	kΩ
R_{EXT}	External pull up resistor on RST terminal (optional)	680			kΩ
C_I	V_{IN} = V_{SS} or V_{DD}		7		pF

(1) The maximum total current I_{OH}, for all outputs combined should not exceed 5mA to hold the maximum voltage drop specified
(2) The maximum total current I_{OL}, for all outputs combined should not exceed 15mA to hold the maximum voltage drop specified

Ports P2, P4 and Port 3.7, Port 3.6

1.1V < VDDIO < 3.3V over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	VDDIO = 1.1 V, I_{OH} = –1 mA[1]	VDDIO - 0.25			V
	VDDIO = 3.3 V, I_{OH} = –1 mA[1]	VDDIO - 0.15			
	VDDIO = 1.1 V, I_{OH} = –300 µA[1]	VDDIO - 0.15			
V_{OL}	VDDIO = 1.1 V, I_{OL} = 2.5 mA[2]			0.2	V
	VDDIO = 3.3 V, I_{OL} = 2.5 mA[2]			0.15	
	VDDIO = 1.1 V, I_{OL} = 300 µA[2]			0.07	
V_{IL}	VDDIO = 3.3 V			0.3 x VDDIO	V
	VDDIO = 1.1 V			0.25 x VDDIO	V
V_{IH}	VDDIO = 3.3 V	0.7 x VDDIO			V
	VDDIO = 1.1 V	0.75 x VDDIO			V
V_{IT+}	VDDIO = 1.1 V – 3.3 V (positive going input threshold)	V_{ILmax}+V_{HYS}		V_{IHmin}	V
V_{IT-}	VDDIO = 1.1 V – 3.3 V (negative going input threshold)	V_{ILmax}		V_{IHmin}- V_{HYS}	V
V_{HYS}	Intrinsic Hysteresis		150		mV
$\Delta t/\Delta v$	VDDIO = 1.1 V, C_L = 15 pF || R_L = 750Ω to V_{SS} on V_{OH} for ports P1,P2,P3			75	ns/V
	VDDIO = 1.1 V, C_L = 15 pF || R_L = 320Ω to V_{DD} on V_{OL} for ports P1,P2,P3			75	
	VDDIO = 3.3 V, C_L = 25 pF || R_L= 1600Ω to V_{SS} on V_{OH} for ports P1,P2,P3			75	
	VDDIO = 3.3 V, C_L = 25 pF || R_L= 600Ω to V_{SS} on V_{OL} for ports P1,P2,P3			75	
I_{OH}	VDDIO = 1.1 V – 3.3 V for ports P1,P2,P3	–1			mA
I_{OL}	VDDIO = 1.1 V – 3.3 V for ports P1,P2,P3	2.5			mA
I_{LKG}	VDDIO = 1.1 V – 3.3 V			±100	nA
t_{INT}	P0.x; V_{DD} = 1.1 V – 3.3 V			200	ns
R_{PULL}	For pullup:V_{IN} = V_{SS}; For pulldown: V_{IN} = VDDIO for ports P1,P2,P3	30	35	40	kΩ
R_{RST}	Pullup on RST/NMI/SVMOUT	30	35	40	kΩ
C_I	V_{IN} = V_{SS} or VDDIO		7		pF

(1) The maximum total current I_{OH}, for all outputs combined should not exceed 5mA to hold the maximum voltage drop specified
(2) The maximum total current I_{OL}, for all outputs combined should not exceed 15mA to hold the maximum voltage drop specified

Ports P3.6, P3.7 (High Current Buzzer)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	VDDIO = 1.1 V, I_{OH} = –10 mA	VDDIO-0.15			V
	VDDIO = 3.3 V, I_{OH} = –10 mA	VDDIO-0.15			
V_{OL}	VDDIO = 1.1 V, I_{OL} = 10 mA			0.2	V
	VDDIO = 3.3 V, I_{OL} = 10 mA			0.15	
$\Delta t/\Delta v$	VDDIO = 1.1V, C_L = 15 pF || R_L = 750Ω to V_{SS} on V_{OH}			75	ns/V
	VDDIO = 1.1 V, C_L = 15 pF || R_L = 320Ω to V_{DD} on V_{OL}			75	
	VDDIO = 1.55 V, C_L = 25 pF || R_L= 1600Ω to V_{SS} on			75	
	VDDIO = 1.55 V, C_L = 25 pF || R_L= 600Ω to V_{SS} on			75	
I_{OH}	VDDIO = 1.1 V – 3.3 V	–10			mA
I_{OL}	VDDIO = 1.1 V – 3.3 V	10			mA
I_{LKG}	VDDIO = 1.1 V – 3.3 V			±100	nA
t_{INT}	P0.x; V_{DD} = 1.1 V – 3.3 V		200		ns
R_{PULL}	Only pulldown implemented: V_{IN} = VDDIO	30	35	40	kΩ
C_I	V_{IN} = V_{SS} or V_{DD}		7		pF

Product Folder Link(s) :AFE4110

High Frequency – OSCILLATOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{HFOSC}	V_{DD} = 1.1 V – 1.55 V (untrimmed)	4	5	7	MHz
f_{HFOSC}	V_{DD} = 1.1 V – 1.55 V (trimmed)	4.1	4.5	4.8	MHz
Duty Cycle	V_{DD} = 1.1 V – 1.55 V	45%	50%	55%	
t_{START}	V_{DDC} = 1.1 V – 1.55 V			20	µs
$\Delta f_{DCO}/\Delta T$	V_{DD} = 1.1 V – 1.55 V; f_{DCO} = 4 MHz		±0.07		%/°C
$\Delta f_{DCO}/V_{DD}$	V_{DD} = 1.1 V – 1.55 V; f_{DCO} = 4 MHz		±1		%/V
$\Delta f_{DCO}/CALSTEP$	V_{DD} = 1.1 V – 1.55 V; f_{DCO} = 4 MHz; ±64 calibration steps	0.1	1	4	%/Step
I_{OP}	V_{DD} = 1.1 V – 1.55 V; f_{DCO} = 4 MHz		25		µA
I_{OP}	V_{DD} = 1.1 V – 1.55 V; f_{DCO} = 1 MHz		22		µA

Low Frequency – OSCILLATOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFO}	V_{DD} = 1.1 V – 1.55 V	6	20	45	kHz
Duty Cycle	V_{DD} = 1.1 V – 1.55 V	45%	50%	55%	
t_{START}	V_{DD} = 1.1 V – 1.55 V			500	µs
I_{OP}	V_{DDC} = 1.1 V – 1.55 V; f_{LFO} = 20 kHz		600		nA

32 kHz Crystal – OSCILLATOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFO}	V_{DD} = 1.1 V – 1.55 V		32		kHz
Duty Cycle	V_{DD} = 1.1 V – 1.55 V	45%	50%	55%	
t_{START}	V_{DDC} = 1.1 V – 1.55 V		200		mS
I_{OP}	V_{DD} = 1.1 V – 1.55 V		2		µA

CP_1P8 Specifications

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time			5mS		
Supply voltage battery input		1.1		1.55	V
Output voltage, V_O			1.8 x V_{BAT}		
No load voltage	V_{BAT} = 1.55 V			3	V
Max load voltage	V_{BAT} = 1.2 V	1.85			V
Max load	CP18 = 10 nF	0.01		3	mA
Charge pump efficiency			70%		
Clocking frequency			4		MHz

Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR(Start)}$		490			mV
$V_{(BOR\_IT+)}$	V_{DD} rising; $dV_{DD} / d_t < 3V/s$	1095		1150	mV
$V_{(BOR\_IT-)}$	V_{DD} falling; $dV_{DD} / d_t < 3V/s$	860		900	mV
Vhys(BOR)			200		mV
V_{MARGIN}	$V_{MARGIN} = V_{(BOR-IT-)} - V_{CRIT}$; T = 0-70°C	40			mV
td$_{BOR}$				3000[1]	µs
I_{OP}	V_{DD} = 1.1 V – 1.55 V		500		nA

(1) Depends on the voltage ramp in the system (actually a maximum typical value).

A-POOL, External Reference Source

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	V_{DD} = 1.1 V – 1.55 V for ADC / DAC operation	100		475	mV
	V_{DD} = 1.1 V – 1.55 V ADC / DAC not operational	0		V_{DD}	V
I_{REF}	V_{DD} = 1.1 V – 1.55 V			3	µA
C_{REF}	REFON = 0	20		50	pF

A-POOL, Built-In Reference Source

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	V_{DD} = 1.1 V – 1.55 V (±1.5%; overall 3%)		256 ±3%		mV
I_{REF}	V_{DD} = 1.1 V – 1.55 V		10		µA
C_{REF}	REFON = 1	20		50	pF
T_{REF}	V_{DD} = 1.1 V – 1.55 V ($\Delta V/\Delta T \times V_{REF}$ referenced to 25°C)		±250		ppm/°C
t_{settle}	V_{DD} = 1.1 V – 1.55 V; REFON = 1; $C_{REF} = C_{REF}$(max)		900		µs
I_{OP}	V_{DD} = 1.1 V – 1.55 V; REFON = 1; $C_{REF} = C_{REF}$(max)	50			µA

A-POOL, Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{SENSOR}	V_{CC} = 1.1 V – 1.55 V		2		µA
TC_{SENSOR}	V_{CC} = 1.1 V – 1.55 V; 0-70°C ($\Delta V/\Delta T$ referenced to 30°C)		464		µV/°C
$V_{OFFSET25}$	V_{CC} = 1.1 V – 1.55 V at T_A = 30°C		179		mV
t_{SETTLE}	V_{CC} = 1.1 V – 1.55 V (before start of conversion)			15	µs
V_{SENSOR}[1]	V_{CC} = 1.1 V – 1.55 V; 0-70°C		179		mV

(1) The following formula can be used to calculate the temperature sensor output voltage
$V_{SENSOR} = V_{OFFSET25} + TC_{SENSOR} \times (T_A = 30°C)$

Product Folder Link(s) :*AFE4110*

A-POOL, Input Voltage Dividers

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta Rx/Rx$	any Rx in dividers		±1.5%		
	any Rx across switches and internal supply voltage divider (by 4, by 8)		±2%		
R_{IN}	on A0/A1 ; V_{A0}/V_{A1} = 0.5 V; ADIV0/ADIV1 = 1 (500 mV range)	120	200	300	kΩ
	on A2/A3 ; V_{A2}/V_{A3} = 0.5 V; ADIV2/ADIV4 = 1 (1 V range)	80	133	190	
	on A2/A3 ; V_{A2}/V_{A3} = 0.5 V; ADIV2 + ADIV3/ADIV4 + ADIV5 = 1 (2 V range)	70	114	150	
ΔI_{VDD}	ADIV7 = 1 (supply voltage divider on)		2		µA

A-POOL, DAC-8

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REFEXT}	V_{DD} = 1.1 V – 1.55 V		256		mV
t_{SETTLE}	On ±1 LSB steps (6τ); V_{DD} = 1.1 V – 1.55 V; V_{REFEXT}(typ); C_{VREF}(min)		2		µs
	Between all codes >20 on A_{OUT} (6τ); V_{DD} = 1.1 V – 1.55 V; V_{REFEXT}(typ); C_{VREF}(min)		14		µs
E_I	V_{DD} = 1.1 V – 1.55 V; V_{REFEXT}(typ); C_{VREF}(min); (add ±7 mV			±3	LSB
E_D	for V_{OUT} offset[1])			±1	LSB

(1) This offset can be compensated using proper software.

A-POOL, Comparator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	V_{DD} = 1.1 V – 1.55 V	0		275	mV
t_{pd}	Overdrive = 20 mV			0.5	µs
	Overdrive = 5 mV			0.5	
	Overdrive = 1 mV			1	

A-POOL, AOUT Pin

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
| I_{LOAD} |	V_{DD} = 1.1 V – 1.55 V; C_{LOAD} = 25 pF; V_{OUT} >50mV	5			µA
| I_{LOAD} |	V_{DD} = 1.1 V – 1.55 V; C_{LOAD} = 25 pF; V_{OUT} >20mV	2			µA
t_{SETTLE}	V_{DD} = 1.1 V – 1.55 V; C_{LOAD} = 25 pF; ±1% (6τ) (for A_{OUT} 20-256 mV)			4	µs

A-POOL, ADC-8 Counter
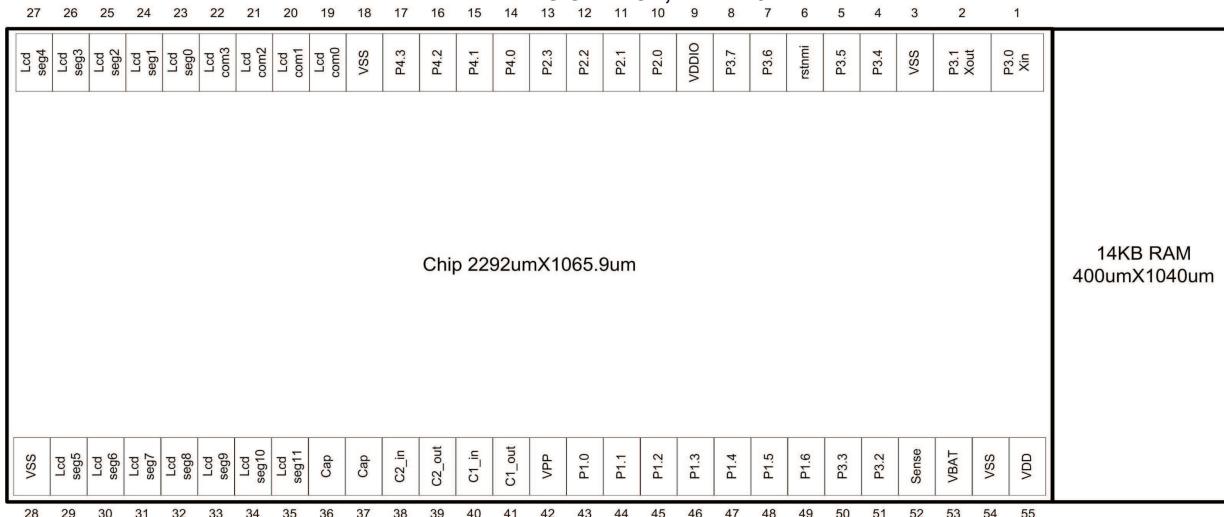
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CNT}	V_{DD} = 1.1 V – 1.55 V				1	MHz
t_{CONV}	Full conversion (all codes) at f_{CNT} = 1MHz			256		µs
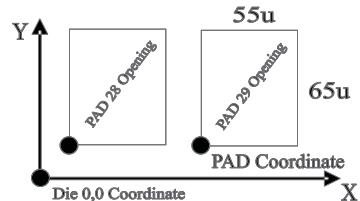
RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OP}	Operating temperature 0-70°C, f_{CPU} = 1MHz	1.1			V
V_{RET}	Operating temperature 0-70°C (tracks BOL level)	700			mV

PIN DESIGNATION, AFE4110

Top row pins (left to right), pins 27 to 1:

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Lcd seg4	Lcd seg3	Lcd seg2	Lcd seg1	Lcd seg0	Lcd com3	Lcd com2	Lcd com1	Lcd com0	VSS	P4.3	P4.2	P4.1	P4.0	P2.3	P2.2	P2.1	P2.0	VDDIO	P3.7	P3.6	rstnmi	P3.5	P3.4	VSS	P3.1 Xout	P3.0 Xin

Chip 2292umX1065.9um

14KB RAM 400umX1040um

Bottom row pins (left to right), pins 28 to 55:

28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55
VSS	Lcd seg5	Lcd seg6	Lcd seg7	Lcd seg8	Lcd seg9	Lcd seg10	Lcd seg11	Cap	Cap	C2_in	C2_out	C1_in	C1_out	VPP	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P3.3	P3.2	Sense	VBAT	VSS	VDD

PAD#	PAD X [μ]	PAD Y [μ]	PAD#	PAD X [μ]	PAD Y [μ]
1	2108.3	987.3	28	96.0	23.6
2	1994.6	987.3	29	171.0	23.6
3	1908.6	987.3	30	246.0	23.6
4	1824.2	987.3	31	321.0	23.6
5	1749.2	987.3	32	396.0	23.6
6	1674.2	987.3	33	471.0	23.6
7	1599.2	987.3	34	546.0	23.6
8	1521.8	987.3	35	621.0	23.6
9	1446.8	987.3	36	696.0	23.6
10	1371.8	987.3	37	771.0	23.6
11	1296.8	987.3	38	846.0	23.6
12	1221.8	987.3	39	921.0	23.6
13	1146.8	987.3	40	996.0	23.6
14	1071.8	987.3	41	1071.0	23.6
15	996.8	987.3	42	1146.0	23.6
16	921.8	987.3	43	1221.0	23.6
17	846.8	987.3	44	1296.0	23.6
18	771.8	987.3	45	1371.0	23.6
19	696.8	987.3	46	1446.0	23.6
20	621.8	987.3	47	1521.0	23.6
21	546.8	987.3	48	1596.0	23.6
22	471.8	987.3	49	1671.0	23.6
23	396.8	987.3	50	1746.0	23.6
24	321.8	987.3	51	1821.0	23.6
25	246.8	987.3	52	1896.0	23.6
26	171.8	987.3	53	1971.0	23.6
27	96.8	987.3	54	2046.0	23.6
			55	2121.0	23.6

Y

55u

PAD 28 Opening   PAD 29 Opening

65u

PAD Coordinate

Die 0,0 Coordinate   X

Product Folder Link(s) :AFE4110

PIN FUNCTIONS

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
P3.0/XTI/EXCLK/TA1.CCI1A1	1	I/O	General-purpose digital I/O 32 kHz Crystal Input External Clock Input Timer1_A3 CCR1A1 capture: CCI1A1 input, compare
P3.1/XTO/TSCLK/TA1.CCI1A2/ ACTSEN/CMP	2	I/O	General-purpose digital I/O 32 kHz Crystal Out Test Clock Input Timer1_A3 CCR1A2 capture: CCI1A2 input, compare Activation Sense Output Comparator Out
VSS/GND	3	Power	Analog and Digital Power Supply Ground Reference
P3.4/TA0.1/TA1.1/TA1.0/TA1.CCI2A2	4	I/O	General-purpose digital I/O Timer0_A3 Out1 output Timer1_A3 Out1 output Timer1_A3 Out0 output Timer1_A3 CCR2A2 capture: CCI2A2 input, compare
P3.5/TA0.1/TA1.1/TA1.0/TA1.CCI2A3	5	I/O	General-purpose digital I/O Timer0_A3 Out1 output Timer1_A3 Out1 output Timer1_A3 Out0 output Timer1_A3 CCR2A3 capture: CCI2A3 input, compare
RST/NMI/SVMOUT	6	I/O	Reset input active low Non-maskable interrupt input SVM Output
P3.6/ TA0.0/TA0.1/TA0.2/TA0.0N/TA0.1N/TA0.2N/ TA1.CCI1A3/ TA1.1/BOR/ACTSEN/LFOSC/CP18OK	7	I/O	10mA General-purpose digital I/O Timer0_A3 Out0 output Timer0_A3 Out1 output Timer0_A3 Out2 output Timer0_A3 Out0# output Timer0_A3 Out1# output Timer0_A3 Out2# output Timer1_A3 CCR1A3 capture: CCI1A3 input, compare Timer1_A3 Out1 output BOR Out Activation Sense Output LFOSC Out CP 1.8V OK Out
P3.7/ TA0.0/TA0.1/TA0.2/TA0.0N/TA0.1N/TA0.2N/ TA1.CCI2A1/HFOSC/LCDCPCLK/ LCDFCLK/ 1KCLK/LCDCMP	8	I/O	10mA General-purpose digital I/O Timer0_A3 Out0 output Timer0_A3 Out1 output Timer0_A3 Out2 output Timer0_A3 Out0# output Timer0_A3 Out1# output Timer0_A3 Out2# output Timer1_A3 CCR2A1 capture: CCI2A1 input, compare LCD Charge Pump Clock Out LCD Frame Clock Out 1 kHz Activation Clock Out LCD Voltage Comparator Out
VDDIO	9	Power	Port2.x, Port4.x, Port3.6 and Port3.7 Positive Power supply 1.1V-3.3V
TCK/P2.0/TA1.2/TA1.1/CxOUT	10	I/O	JTAG Test clock General-purpose digital I/O Timer1_A3 Out2 output Timer1_A3 Out1 output CxOUT digital out from A-Pool

(1)   I = input, O = output, N/A = not available on this package offering.

PIN FUNCTIONS (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
TMS/P2.1/ EXT_CLK/TA0.1/TA0.2	11	I/O	JTAG Test mode selec1 General-purpose digital I/O Timer0_A3 Out2 output Timer0_A3 Out1 output XTAL_CLK or EXT_CLK monitor out
TDI/P2.2/HF_CLK/CxOUT/TA1.0/	12	I/O	JTAG Test data input General-purpose digital I/O Timer1_A3 Out0 output CxOUT digital out from A-Pool HF_CLK out
TDO/P2.3/LF_CLK/TA0.2	13	I/O	JTAG Test data output General-purpose digital I/O Timer0_A3 Out2 output LF_CLK Out
P4.0/TA0.2/TA1.2/ACLK/ATEST/SPI_CS	14	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output ACLK output Analog Test Multiplexer Out SPI Chip Select
P4.1/TA0.2/TA1.2/SMCLK/SPI_MOSI	15	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output SMCLK output SPI Serial IN
P4.2/ TA0.2/TA1.2/MCLK/SPI_CLK	16	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output MCLK output SPI Clock Out
P4.3/ TA0.2/TA1.2/1KOSC//SPI_MISO	17	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output 1 kHz Activation Oscillator Out SPI Serial Out
GNDIO	18	Power	PX.X GND
LCD_ECOM.0	19	Analog	LCD_E Common-0 , 0V – 3.4V
LCD_ECOM.1	20	Analog	LCD_E Common-1 , 0V – 3.4V
LCD_ECOM.2	21	Analog	LCD_E Common-2 , 0V – 3.4V
LCD_ECOM.3	22	Analog	LCD_E Common-3 , 0V – 3.4V
LCD_ESEG.0	23	Analog	LCD_E Segment-0 , 0V – 3.4V
LCD_ESEG.1	24	Analog	LCD_E Segment-1 , 0V – 3.4V
LCD_ESEG.2	25	Analog	LCD_E Segment-2 , 0V – 3.4V
LCD_ESEG.3	26	Analog	LCD_E Segment-3 , 0V – 3.4V
LCD_ESEG.4	27	Analog	LCD_E Segment-4 , 0V – 3.4V
VSS/GND	28	Power	Analog and Digital Power Supply Ground Reference
LCD_ESEG.5	29	Analog	LCD_E Segment-5 , 0V – 3.4V
LCD_ESEG.6	30	Analog	LCD_E Segment-6 , 0V – 3.4V
LCD_ESEG.7	31	Analog	LCD_E Segment-7 , 0V – 3.4V
LCD_ESEG.8	32	Analog	LCD_E Segment-8 , 0V – 3.4V
LCD_ESEG.9	33	Analog	LCD_E Segment-9 , 0V – 3.4V
LCD_ESEG.10	34	Analog	LCD_E Segment-10 , 0V – 3.4V
LCD_ESEG.11	35	Analog	LCD_E Segment-11 , 0V – 3.4V

Product Folder Link(s) :AFE4110

PIN FUNCTIONS (continued)
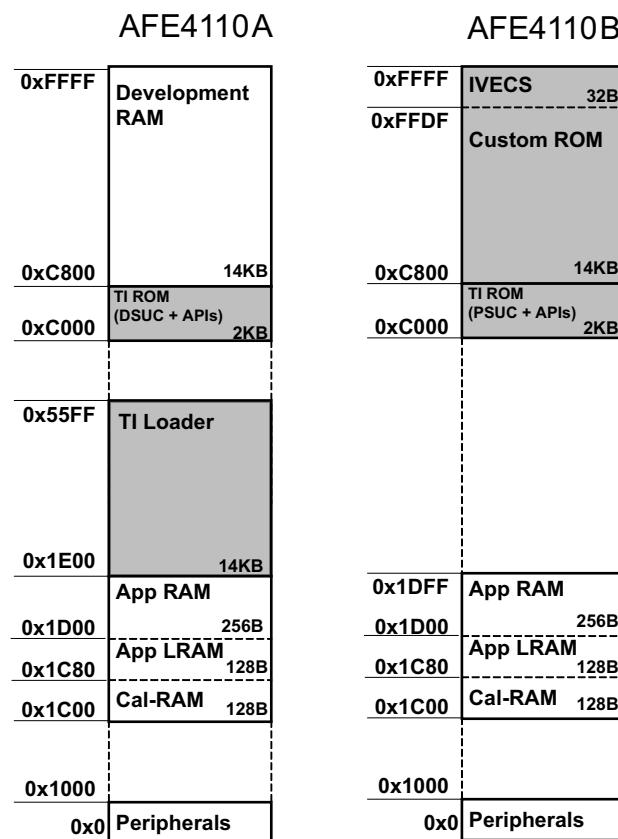
PIN		I/O[1]	DESCRIPTION
NAME	NO.		
LCD_EHVCAP	36	Analog	LCD_E HV Charge Pump Ext Capacitor to GND, 3.4V
CP18CAP	37	Analog	Minimum 1.8V Charge pump Ext capacitor C to VSS
CP1P8_C2_IN	38	Analog	1.8V Charge pump Ext capacitor B for 2mA drive
CP1P8_C2_OUT	39	Analog	1.8V Charge pump Ext capacitor B for 2mA drive
CP1P8_C1_IN	40	Analog	1.8V Charge pump Ext capacitor A for 2mA drive
CP1P8_C1_OUT	41	Analog	1.8V Charge pump Ext capacitor A for 2mA drive
VPP	42	Power	Factory programming voltage. VPP must be tied to VDD in normal use mode.
P1.0/TA0.2/TA0.1/TA1.2/LDO1/TA0.CCI1B0/ TA0.CCI2B0/A2	43	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer0_A3 Out1 output Timer1_A3 Out2 output LDO 1V Out Timer0_A3 CCR1B0 capture: CCI1B0 input, compare Timer0_A3 CCR2B0 capture: CCI2B0 input, compare Analog input A2 – A-Pool
P1.1/TA0.2/TA0.1/TA1.2/LDO1/TA0.CCI1A1/ TA0.CCI2A1/A1	44	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer0_A3 Out1 output Timer1_A3 Out2 output LDO 1V Out Timer0_A3 CCR1A1 capture: CCI1A1 input, compare Timer0_A3 CCR2A1 capture: CCI2A1 input, compare Analog input A1 – A-Pool
P1.2/TA0.2/TA0.1/TA1.2/AOUT/ TA0.CCI1A2/TA0.CCI2A2/A3	45	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer0_A3 Out1 output Timer1_A3 Out2 output Analog Out - A-Pool Timer0_A3 CCR1A2 capture: CCI1A2 input, compare Timer0_A3 CCR2A2 capture: CCI2A2 input, compare Analog input A3 – A-Pool
P1.3/TA0.2/TA0.1/TA1.2/REFOUT/ TA0.CCI1A3/TA0.CCI2A3/A3	46	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer0_A3 Out1 output Timer1_A3 Out2 output Vref Out – A-Pool Timer0_A3 CCR1A3 capture: CCI1A3 input, compare Timer0_A3 CCR2A3 capture: CCI2A3 input, compare Analog input A3 – A-Pool
P1.4/TA0.2/TA0.1/TA1.2/LDO1/ TA0.CCI1B1/TA0.CCI2B1/A0	47	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer0_A3 Out1 output Timer1_A3 Out2 output LDO 1V Out Timer0_A3 CCR1B1 capture: CCI1B1 input, compare Timer0_A3 CCR2B1 capture: CCI2B1 input, compare Analog input A0 – A-Pool
P1.5/TA0.2/TA0.1/TA1.2/LDO1/TA0.CCI1B2/ TA0.CCI2B2	48	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer0_A3 Out1 output Timer1_A3 Out2 output Timer0_A3 CCR1B2 capture: CCI1B2 input, compare Timer0_A3 CCR2B2 capture: CCI2B2 input, compare

PIN FUNCTIONS (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
P1.6/TA0.2/TA0.1/TA1.2/TA1.CCI1B0/ TA1.CCI2B0	49	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer0_A3 Out1 output Timer1_A3 Out2 output Timer1_A3 CCR1B0 capture: CCI1B0 input, compare Timer1_A3 CCR2B0 capture: CCI2B0 input, compare
P3.3/ TA0.1/TA1.1/TA1.0/A0/LDO1	50	I/O	General-purpose digital I/O Timer0_A3 Out1 output Timer1_A3 Out1 output Timer1_A3 Out0 output LDO 1V Out Analog input A0 – A-Pool
P3.2/ TA0.1/TA1.1/TA1.0	51	I/O	General-purpose digital I/O Timer0_A3 Out1 output Timer1_A3 Out1 output Timer1_A3 Out0 output
ACTIVE	52	I	Sleep Mode (LPM5) activation pin
VBAT	53	Power	Battery Power, Switched from VDD
VSS/GND	54	Power	Analog and Digital Power Supply Ground Reference
VDD	55	Power	Analog and Digital Power Supply

Product Folder Link(s) :*AFE4110*

Memory Organization

- AFE4110 manufactured in 2 memory configurations
- AFE4110A – Application Development Device
    - 14KB Development RAM
    - 512B Application RAM
    - 2KB Development Start Up Code ROM
    - 14KB Boot Loader ROM
- AFE4110B – Custom Masked ROM Device
    - 512B Application RAM
    - 2KB Production Start Up Code ROM
    - 14KB Custom Masked ROM

AFE4110A		AFE4110B	
0xFFFF	**Development RAM**	0xFFFF	**IVECS** 32B
		0xFFDF	**Custom ROM**
0xC800	14KB	0xC800	14KB
0xC000	TI ROM (DSUC + APIs) 2KB	0xC000	TI ROM (PSUC + APIs) 2KB
0x55FF	**TI Loader**		
0x1E00	14KB		
	App RAM	0x1DFF	**App RAM**
0x1D00	256B	0x1D00	256B
0x1C80	**App LRAM** 128B	0x1C80	**App LRAM** 128B
0x1C00	**Cal-RAM** 128B	0x1C00	**Cal-RAM** 128B
0x1000		0x1000	
0x0	**Peripherals**	0x0	**Peripherals**

SHORT-FORM DESCRIPTION

CPU

The AFE4110 is based on an MSP430 CPU core with a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

INSTRUCTION SET

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD	R4, R5	R4 + R5 → R5
Single operands, destination only	e.g. CALL	R8	PC → (TOS), R8 → PC
Relative jump, un/conditional			Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S[1]	D[2]	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10, R11	R10 → R11
Indexed	●	●	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE, TONI		M(EDE) → M(TONI)
Absolute	●	●	MOV & MEM, and TCDAT		M(MEM) → M(TCDAT)
Indirect	●		MOV at Rn, Y(Rm)	MOV at R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	●		MOV at Rn+,Rm	MOV at R10+, R11	M(R10) → R11 R10 + 2 → R10
Immediate	●		MOV at 45,TONI	MOV #45, TONI	#45 → M(TONI)

(1) S = source
(2) D = destination

Product Folder Link(s) :*AFE4110*

Operation Modes

The AFE4110 has one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
  - ACLK and SMCLK remain active for all sources
  - MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled
  - ACLK and SMCLK remain active (for LF-Osc and CLKIN as source; HF-Osc is mapped to LF-Osc as source)
  - MCLK is disabled
- Low-power mode 2 (LPM2);
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is disabled
  - ACLK remains active for all sources
- Low-power mode 3 (LPM3);
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is disabled
  - ACLK remains active (for LF-Osc and CLKIN as source; HF-Osc is mapped to LF-Osc as source)
- Low-power mode 4 (LPM4);
  - CPU is disabled
  - ACLK is disabled
  - MCLK is disabled
  - Oscillators are stopped (exclude Activation Block 1kHz local oscillator)
- Low-power mode 5 (LPM5);
  - CPU core and peripherials are powered off (Application and Calibration RAM contents are not retained.)
  - Activation Block, 1kHz local oscillator, and 8 bytes RAM remain active

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 3. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog	WDTIFG(1)	Reset	0x0FFFE	14, highest
System NMI Vacant memory access	SVMIFG, VMAIFG[1]	(Non)maskable	0x0FFFC	13
User NMI NMI	NMIIFG[1] [2]	(Non)maskable	0x0FFFA	12
Timer1_A3 Timer1_A3	TA1CCR0 CCIFG[3] TA1CCR1 CCIFG TA1CCR2 CCIFG TA1IFG[1] [3]	Maskable Maskable	0x0FFF8 0x0FFF6	11 10
Watchdog Timer_A Interval Timer Mode	WDTIFG	Maskable	0x0FFF4	9
A-Pool	CxIFG	Maskable	0x0FFF2	8
I/O Port P1	P1IFG.0 to P1IFG.6[1] [3]	Maskable	0x0FFF0	7
Timer0_A3	TA0CCR0 CCIFG[3]	Maskable	0x0FFEE	6
Timer0_A3	TA0CCR1 CCIFG TA0CCR1 CCIFG TA0IFG[1] [3]	Maskable	0x0FFEC	5
I/O Port P2	P2IFG.0 to P2IFG.3[1] [3]	Maskable	0x0FFEA	4
I/O Port P3	P3IFG.0 to P3IFG.7[1][3]	Maskable	0x0FFE8	3
I/O Port P4	P4IFG.0 to P4IFG.3[1] [3]	Maskable	0x0FFE6	2
LCD Controller	LCDFRMIFG, LCDBLKOFFIFG, LCDBLKONIFG, LCDNOCAPIFG	Maskable	0x0FFE4	1
The Following Interrupts are multiplexed on I/O Port P3 interrupts				
Activation Sense[4] [5]	Muxed with P3.6	Maskable	0x0FFE8	3
CP 1p8 Valid[4] [5]	Muxed with P3.7	Maskable	0x0FFE8	3
Activation sleep counter timeout [4] [5]	Muxed with P3.4	Maskable	0x0FFE8	3
CP 1p8 comparator out[4][5]	Muxed with P3.5	Maskable	0x0FFE8	3
LCD CP comparator out [4][5]	Muxed with P3.2	Maskable	0x0FFE8	3
APOOL comparator out[4]	Muxed with P3.3	Maskable	0x0FFE8	3

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) No additional synchronization mechanisms beyond standard MSP430 interrupt synchronization
(5) Interrupt Signal is directly connoted without a de-glitcher mechanism.

Product Folder Link(s) :*AFE4110*

Special Function Registers (SFRs)

The AFE4110 SFRs are located in the lowest address space and can be accessed via word or byte formats. Other SFR registers documented in Texas Instruments MSP430x5xx "**Compact SYS Module User's Guide**" (SLAU321).

Legend	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
	rw-[0,1]:	Bit can be read and written. It is reset or set by BOR.
		SFR bit is not present in device

SFRIE1, SFRIE1_L, SFRIE1_H, Interrupt Enable Register

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	SVMIE
r0	r0	r0	r0	r0	r0	r0	rw-0

7	6	5	4	3	2	1	0
JMBOUTIE	JMBINIE	–	NMIIE	VMAIE	–	OFIE	WDTIE
rw-0	rw-0	r0	rw-0	rw-0	r0	rw-0	rw-0

Reserved	Bits 15 – 9	Reserved. Read back as 0
SVMIE	Bit 8	SVM interrupt enable flag. 0 interrupts disabled 1 interrupts enabled
JMBOUTIE	Bit 7	JTAG mailbox output interrupt enable flag. 0 interrupts disabled 1 interrupts enabled
JMBINIE	Bit 6	JTAG mailbox input interrupt enable flag. 0 interrupts disabled 1 interrupts enabled
Reserved	Bit 5	Reserved. Reads back as 0
NMIIE	Bit 4	NMI pin interrupt enable flag. 0 interrupts disabled 1 interrupts enabled
VMAIE	Bit 3	Vacant memory access interrupt enable flag. 0 interrupts disabled 1 interrupts enabled
Reserved	Bit 2	Reserved. Reads back as 0
OFIE	Bit 1	Oscillator fault interrupt enable flag. 0 interrupts disabled 1 interrupts enabled
WDTIE	Bit 0	Watchdog timer interrupt enable. This bit enables the WDTIFG interrupt for interval timer mode. It is not necessary to set this bit for watchdog mode. Because other bits in ~IE1 may be used for other modules, it is recommended to set or clear this bit using BIS.B or BIC.B instructions, rather than MOV.B or CLR.B instruction 0 interrupts disabled 1 interrupts enabled

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SFRIFG1, SFRIFG1_L, SFRIFG1_H, Interrupt Flag Register

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	SVMIFG
r0	r0	r0	r0	r0	r0	r0	rw-0

7	6	5	4	3	2	1	0
JMBOUTIFG	JMBINIFG	–	NMIIFG	VMAIFG	–	OFIFG	WDTIFG
rw-0	rw-0	r0	rw-0	rw-0	r0	rw-0	rw-0

Reserved	Bits 15 – 9	Reserved. Read back as 0
SVMIFG	Bit 8	SVM interrupt flag. This bit signals that the A-POOL comparator signaled an SVM event either low voltage or high voltage depending on setup 0 no interrupt pending 1 interrupt pending
JMBOUTIFG	Bit 7	JTAG mailbox output interrupt flag 0 no interrupt pending. When in 16-bit mode (JMBMODE = 0), this bit is cleared automatically when JMBO0 has been written by the CPU. When in 32-bit mode (JMBMODE = 1), this bit is cleared automatically when both JMBO0 and JMBO1 have been written by the CPU. This bit is also cleared when the associated vector in SYSSNIV has been read 1 interrupt pending, JMBO registers are ready for new messages. In 16-bit mode (JMBMODE=0) JMBO0 has been received by JTAG. In 32-bit mode (JMBMODE=1) , JMBO0 and JMBO1 have been received by JTAG
JMBINIFG	Bit 6	JTAG mailbox input interrupt flag 0 no interrupt pending. When in 16-bit mode (JMBMODE = 0), this bit is cleared automatically when JMBI0 is read by the CPU. When in 32-bit mode (JMBMODE = 1), this bit is cleared automatically when both JMBI0 and JMBI1 have been read by the CPU. This bit is also cleared when the associated vector in SYSSNIV has been read 1 interrupt pending, a message is waiting in the JMBIN registers. In 16-bit mode (JMBMODE = 0) when JMBI0 has been written by JTAG. In 32 bit mode (JMBMODE = 1) when JMBI0 and JMBI1 have been written by JTAG
Reserved	Bit 5	Reserved. Reads back as 0
NMIIFG	Bit 4	NMI pin interrupt flag 0 no interrupt pending 1 interrupt pending
VMAIFG	Bit 3	Vacant memory access interrupt flag 0 no interrupt pending 1 interrupt pending
Reserved	Bit 2	Reserved. Reads back as 0
OFIFG		Oscillator fault interrupt flag 0 no interrupt pending 1 interrupt pending
WDTIFG	Bit 0	Watchdog timer interrupt flag. In watchdog mode, WDTIFG remains set until reset by software. In interval mode, WDTIFG is reset automatically by servicing the interrupt, or can be reset by software. Because other bits in ~IFG1 may be used for other modules, it is recommended to clear WDTIFG by using BIS.B or BIC.B instructions, rather than MOV.B or CLR.B instructions. 0 no interrupt pending 1 interrupt pending

SFRRPCR, SFRRPCR_H, SFRRPCR_L, Reset Pin Control Register

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
–	–	–	–	SYSRSTRE	SYSRSTUP	SYSNMIES	SYSNMI
r0	r0	r0	r0	r1	r1	r1	rw-0

Reserved	Bits 15–9	Reserved. Read back as 0
SYSRSTRE	Bit 3	Reset Pin resistor enable 0 Pullup / pulldown resistor at the RST/NMI pin is disabled 1 Pullup / pulldown resistor at the RST/NMI pin is enabled
SYSRSTUP	Bit 2	Reset resistor pin pullup / pulldown 0 Pulldown is selected 1 Pullup is selected
SYSNMIES	Bit 1	NMI edge select. This bit selects the interrupt edge for the NMI interrupt when SYSNMI = 1. Modifying this bit can trigger an NMI. Modify this bit when SYSNMI = 0 to avoid triggering an accidental NMI 0 NMI on rising edge 1 NMI on falling edge
SYSNMI	Bit 0	NMI select. This bit selects the function for the RST/NMI pin 0 Reset function 1 NMI function

Table 4. Memory Organization

	TYPE	AFE4110A (Dev RAM)	Type	AFE4110B (Custom ROM)
Interrupt Vectors	RAM	32 B 0xFFE0[1] – 0xFFFF	ROM	32 B 0xFFE0[1] – 0xFFFF
Development RAM	RAM	14KB 0xC800 – 0xFFFF	—	—
Application ROM	—	—	ROM	14KB 0xC800 – 0xFFFF
TI Start Up Code (DSUC/PSUC)	ROM	2KB 0xC000 – 0xC7FF	ROM	2KB 0xC000 – 0xC7FF
TI Boot Loader Code	ROM	14KB 0x1E0 – 0x55FF	—	—
Application RAM	RAM	256B 0x1D00 – 0x1DFF	RAM	256B 0x1D00 – 0x1DFF
Application LRAM (lockable)	RAM	128B 0x1C80 – 0x1CFF	RAM	128B 0x1C80 – 0x1CFF
Calibration RAM (lockable)	RAM	128B 0x1C00 – 0x1C7F	RAM	128B 0x1C00 – 0x1C7F
Peripherals	Registers	4 kB 0x0000 – 0x0FFF	Registers	4 kB 0x0000 – 0x0FFF

(1)   not the whole interrupt vector range of CSYS is used on AFE4110 devices

Start-Up Code (SUC)

The AFE4110A Development Start-Up Code (DSUC) supports system debug via a JTAG connection to an external emulator. After the release of RST/NMI, the DSUC checks for the presence of a JTAG emulator by reading the contents of the JTAG Mailbox Register. If the emulation password is present in the JTAG Mailbox, the DSUC unlocks full access to the on chip emulation features, then enters LPM4 while waiting for to enter the debug session. If the emulation password is not present in the JTAG Mailbox, the DSUC initiates execution of the Loader Code.

The AFE4110B Production Start-Up Code (PSUC) also supports system debug via a JTAG connection to an external emulator. The difference is that the PSUC checks for the contents of the JTAG Mailbox Register for a confidential password. If the confidential password is present in the JTAG Mailbox, the PSUC unlocks full access to the on chip emulation features, then enters LPM4 while waiting for to enter the debug session. If the confidential password is not present in the JTAG Mailbox when RST/NMI is released, the PSUC initates execution of the custom ROM code.

Loader Code (Loader)

The AFE4110A Loader checks for the presence of an external SPI memory device containing a valid data/code package. The Loader transfers a validated data/code package into Development RAM. During validation and transfer, the on chip 1.85V charge pump is enabled to supply power to VDDIO and the external SPI memory device. (PCB level connections are required.) Once the transfer of the data/code package is complete, the charge pump is disabled, the AFE4110 registers are returned to their default contents, and execution of the code loaded in Development RAM is initiated.

RAM Memory

The RAM memory is split into three ranges for different purposes: Application memory, lockable application memory and calibration memory.

Lockable application memory and calibration memory can be protected against accidental erasure by setting a dedicated lock bit in the special functions register (System Maintenance Register).

Note: The lockable memory is locked by default after release of RST/NMI or exit from LPM5. The user code must clear the lock bits in the Special Function Register after release of RST/NMI or exit from LPM5 to enable writing lockable memory.

Peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the MSP430x5xx Family User's Guide (SLAU208) and the MSP430x09x Family User's Guide (SLAU321).

Digital I/O

There are 4 I/O ports implemented: P1 (7 I/O lines), P2 (4 I/O lines), P3 (6 I/O lines) and P4 (4 I/O lines)
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on P1 and P3(0-5) ports.
- Programmable pullup on P2, P4 and P3(6,7) ports.
- External VDD (VDDIO) supply (1.1-3.3V range) to P2, P4 and P3(6,7) ports.
- Edge-selectable interrupt input capability for all ports.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1, P2, P3 and P4) or word-wise in pairs (P1/P2 combo).

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Oscillator and System Clock

The clock system in the AFE4110 family of devices is supported by the Compact Clock System (CCS) module that includes an internal 20kHz current controlled low frequency oscillator (LF-OSC), an internal adjustable (1-5.4MHz) current controlled high frequency oscillator (HF-OSC), a 1KHz ultra low power oscillator for the activation block, an external clock input from CLKIN, and a 32kHz crystal oscillator. The CCS module is designed to meet the requirements of both low system cost and low-power consumption. The CCS provides a fast turn-on of the oscillators in less than 1 ms.

The CCS module provides the following clock signals:

- Auxiliary clock (ACLK) is software selectable for individual peripheral modules. ACLK is sourced from the internal LF-OSC, the internal HF-OSC, an external source via CLKIN, or the crystal oscillator.
- Main clock (MCLK) is the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem master clock is software selectable by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- VLOCLK this is a low frequency clock sourced by LF-OSC that is constantly available.
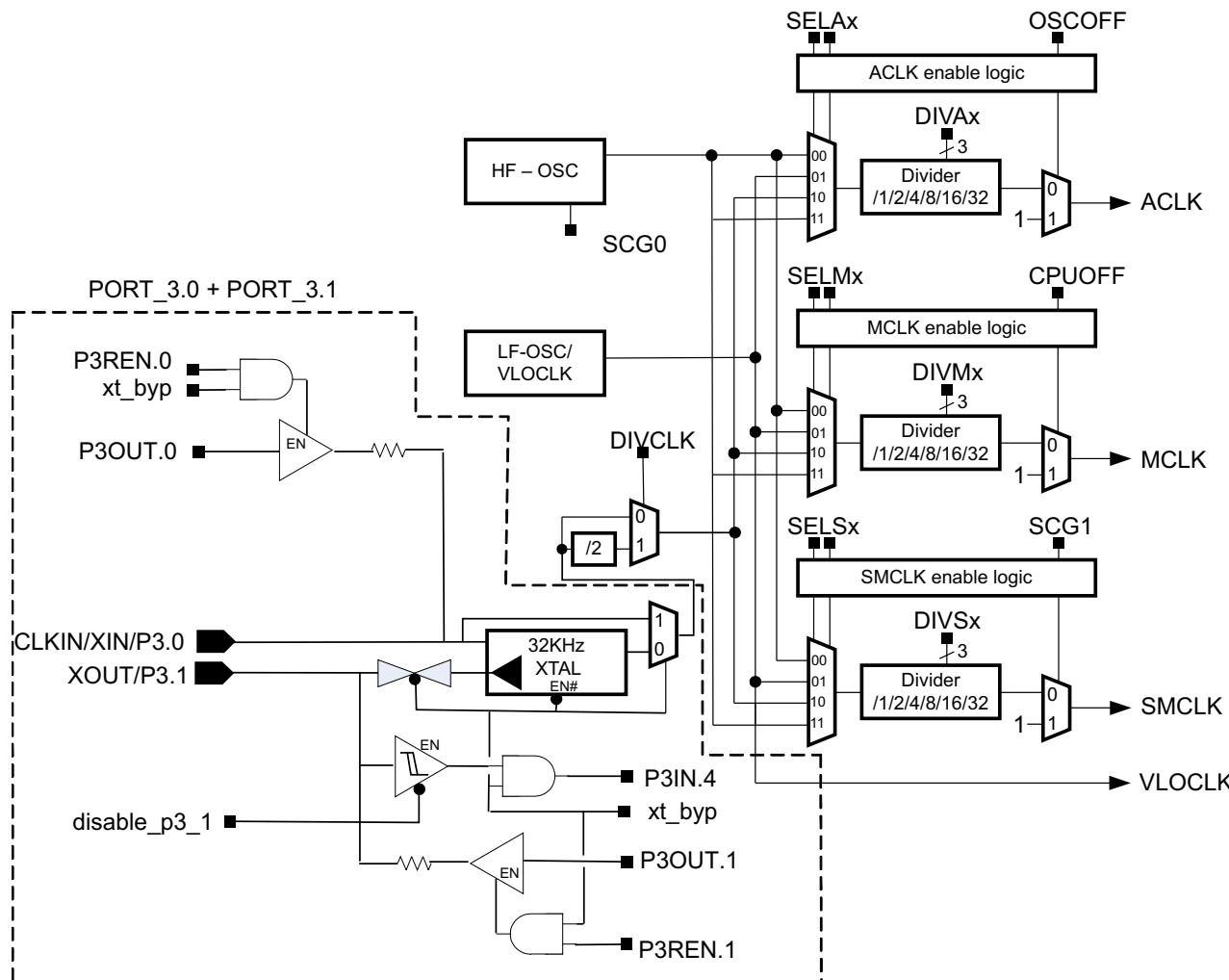
Figure 1. Block Diagram of Compact Clock System (CCS)

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Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. For a complete description of WDT_A, see the Watchdog Timer (WDT_A) section of the MSP430x09x Family Users Guide (SLAU321).

Table 5. WDT_A Signal Connections

DEVICE CLOCK SIGNAL	MODULE CLOCK SIGNAL
ACLK	ACLK
SMCLK	SMCLK
LF-OSC-CLK	VLOCLK
HF-OSC-CLK	X-CLK

Compact System Module (C-SYS)

The Compact SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, as well as, configuration management. It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application. For a complete description of C-SYS, see the Compact System chapter of the MSP430x09x Family Users Guide (SLAU321).

Reset/NMI/SVMOUT System

The Reset system of the MSP430x09x family features the function Reset input, Reset output, NMI input, SVM output and SVS input.
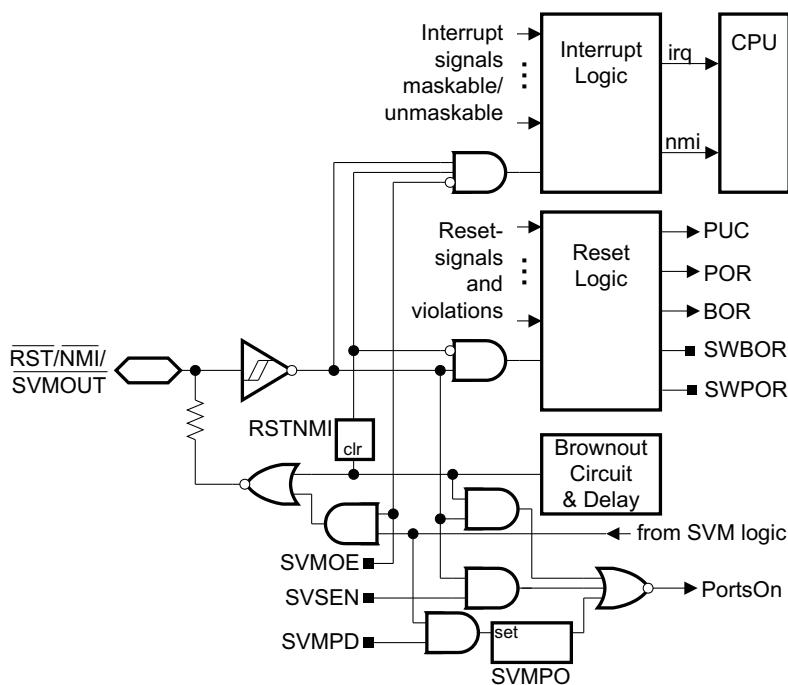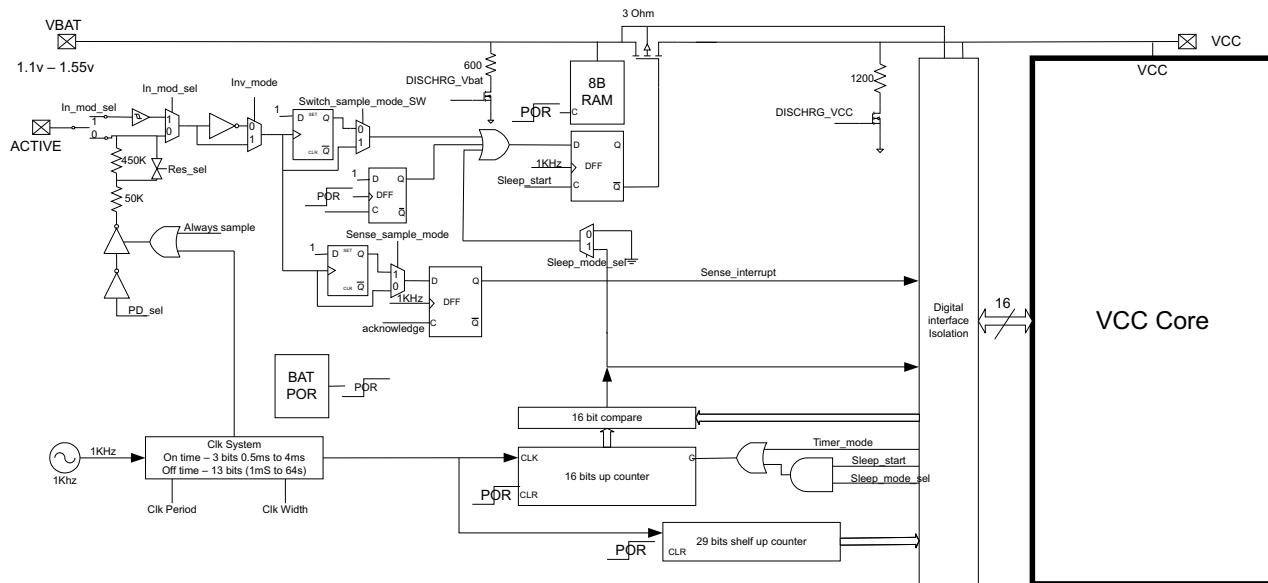
Figure 2. Block Diagram of Reset/NMI/SVM and PortsOn logic

Product Folder Link(s) :*AFE4110*

Table 6. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	INTERRUPT VECTOR	WORD ADDRESS	OFFSET	PRIORITY
SYSRSTIV, System Reset	No interrupt pending	019Eh	00h	
	Brownout (BOR)		02h	Highest
	SVMBOR (BOR)		04h	
	RST/NMI (BOR)		06h	
	DoBOR (BOR)		08h	
	Security violation (BOR)		0Ah	
	DoPOR(POR)		0Ch	
	WDT timeout (PUC)		0Eh	
	WDT key violation (PUC)		10h	
	CCS key violation		12h	
	PMM key violation		14h	
	Peripheral area fetch (PUC)		16h	
	Reserved		18h-3Eh	Lowest
SYSSNIV, System NMI	No interrupt pending	019Ch	00h	
	SVMIFG		02h	Highest
	VMAIFG		04h	
	JMBINIFG		06h	
	JMBOUTIFG		08h	
	Reserved		0Ah-3Eh	Lowest
SYSUNIV, User NMI	No interrupt pending	019Ah	00h	
	NMIFG		02h	Highest
	OFIFG		04h	
	BERR		06h	
	Reserved		08h-3Eh	Lowest
SYSBERRIV, Bus Error	No interrupt pending	0198h	00h	
	Reserved		02h-3Eh	Lowest

Activation Block

The AFE4110 Activation Block controls entry and exit from "deep-sleep" (LPM5) mode. When the device is in LPM5, power is disconnected from AFE4110 CPU and all peripherals (including RAM, LCD and I/O) other than the Activation block. When exiting LPM5, power is reapplied to the CPU core and peripherals. Exiting "deep-sleep" (LPM5) mode is termed "wake up". The Activation block wakes up the CPU core and peripherals based on how it was configured prior to entering LPM5. Wake up takes place based either on a transition on the Activation Sense (ACTIVE) input or after a number of Activation Clock cycles have been counted. The ACTIVE input can be configured to respond to either LOW-to-HIGH or HIGH-to-LOW transitions. The number of Activation clock cycles to be counted prior to exiting LPM5 is configurable.

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Activation Block Hardware Status and Control Registers:

The Activation Block hardware registers control the method of entry and exit from deep sleep (LPM5) mode. Additional features of the Activation Block registers include the following:

- VBAT Power On Reset (POR) Circuit – The VBAT POR is designed to reset the Activation block during initial system power up that is typical of installation of a battery into the final product.
- 4-16bit words (8B) RAM – This RAM is implemented in hardware registers. The contents of these registers is cleared at inital system power up by VBAT POR. The fact that these registers are cleared at initial system power up allow them to be used to determine whether the CPU is being powered up by battery insertion or exit from LPM5.
- 16bit Sleep Counter – The Activation block can be configured to exit LPM5 after the number of Activation clock cycles that are selected. The counter can also be used as a general purpose down counter without entering LPM5.
- 28bit Shelf Counter – This counter starts incrementing after the first time the device enters LPM5. After the first exit from LPM5 this counter stops and its outputs remain static until VBAT power is removed. The intent is for this counter to record number of Activation clock periods between initial insertion of a battery in to the final product and the first usage of the final product. In other words, this counter indicates the length of time that the final product is on the shelf prior to being used by a consumer.
- ACTIVE Sample Clock – To minimize the power required for determining transitions on the ACTIVE pad, the state of the ACTIVE pad is sampled only at intervals which are set by the duty cycle of the ACTIVE Sample Clock. The period between samples and the duration of the sample interval are configurable.

The Activation Block 'strobe' registers are not memory mapped and require a multi-step procedure for Reads and Writes of their contents from the CPU. The Activation register strobe refers to the hardware signal used to capture data into the bank of hardware registers. The strobe number (strobe address) indicates the bank of 16-hardware registers to be accessed. Only 16-bit (word) accesses are supported.

Activation Strobe Register Read Procedure:

The steps to Read a particular Activation strobe register follows:

1. Write the strobe address of the Activation register to be Read to the ACTIVATION_RD_ADDR register
2. Wait 10-MCLK clock cycles for the transfer of selected data to the ACTIVATION_DATAIN register
3. Read to contents of the ACTIVATION_DATAIN register

Activation Strobe Register Write Procedure:

The steps to Write Activation strobe registers follows:

1. Write to data value to be transferred to the Activation hardware register to the ACTIVATION_DATAOUT register
2. Wait 10-MCLK clock cycles for data to transfer to the Activation block
3. Write a '1' to the bit corresponding to the Activation hardware register to be written into the ACTIVATION_STROBES register.

   Note: If multiple bits are written in the ACTIVATION_STROBES register, multiple Activation hardware registers will be written

The table below describes the function of the Activation strobe registers.

Table 7. Activation Strobe Register Function Table

data in #	strobe0	strobe1	strobe2	strobe3	strobe4	strobe5	strobe6	strobe 7
data in 0	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**Res_sel**	ACTCLK_Freq_Sel<2:0>
data in 1	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**PD_sel**	
data in 2	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**Always_sample**	
data in 3	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**Inv_mode**	Reserved
data in 4	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**Switch_sample_mode_SW**	Reserved
data in 5	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**Switch_sample_mode**	Reserved
data in 6	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**In_mod_sel**	Reserved
data in 7	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**Sleep_mode_sel**	Reserved
data in 8	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	Reserved	Reserved
data in 9	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**Sleep_start**	Reserved
data in 10	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	**Timer_mode**	Reserved
data in 11	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	Reserved	Reserved
data in 12	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Period	Reserved	Reserved
data in 13	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Width	**DISCHRG_Vbat**	Reserved
data in 14	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Width	**DISCHRG_VCC**	Reserved
data in 15	RAM reg 0	RAM reg 1	RAM reg 2	RAM reg 3	sleep counter	ACTIVE Sample Clk Width	Reserved	Reserved

Strobe0 - Strobe3: Activation Block RAM Registers

RAM Reg0 - RAM Reg3 - Bits 15 - 0 - Constantly powered registers for used as RAM (Cleared by assertion of VBAT POR)

Strobe4: Sleep Counter Register

Sleep_counter - Bits 15 - 0 - Sleep counter output value

Strobe5: ACTIVE Sample Clock Configuration Register

ACTIVE_Sample_Clock_Period - Bits 12 - 0 - Number of ACTCLK cycles per period of the ACTIVE sample clock
0x0000 sets the sampling period to ~8192ms
0x0001 sets the sampling period to ~1ms...
0x0009 sets the sampling period to ~9ms ...
0x1FFF sets the sampling frequency to ~8192ms

ACTIVE_Sample_Clock_Width - Bits 15 - 13 - Number of ACTCLK half-cycles per sample interval of the ACTIVE sample clock

Strobe6: LPM5 Configuration Register

Res_sel - Bit 0 - PU/PD Resistor Select
1 - 500KΩ resister selected
0 - 50KΩ resister selected

PD_sel - Bit 1 - Pull Down Select
1 - PMOS sensing - internal PU is connected
0 - NMOS sensing – internal PD is connected

Always_sample - Bit 1 ACTIVE Sampling Select
1 - Continuous ACTIVE input sensing
0 - ACTIVE input sensing at sampled intervals

Inv_mode - Bit 3 - Inverted Mode
1 - Low to high transition sensing
0 - High to low transition sensing

Switch_sample_mode_SW - Bit 4 - Switch Sample Mode Switch
1 - Edge sensing for external switch closure selected
0 - Level sensing for external switch closure selected

Switch_sample_mode - Bit 5 - Switch Sample Mode
1 - Edge sensing for the sense_interrupt
0 - Level sensing for the sense_interrupt

In_mod_sel - Bit 6 - Input Mode Select
1 - Low current hysteresis sense inverter selected
0 - Standard input selected

Sleep_mode_sel - Bit 7 - Sense Mode Select
1 - high selects power down with counter;
0 - low selects power down without counter

Sleep_start - Bit 9 - Sleep Start
1 - Start power down
0 - Normal operating mode (This bit must be cleared by TI start up code.)

Timer_mode - Bit 10 - Timer Mode
1- Start sleep counter without entering LPM5
0 - Sleep counter is starting when entering LPM5 if sleep counter mode is selected

DISCHRG_Vbat - Bit 13 - Dischanrge VBAT Power
1 - Discharge Vbat voltage through 600 Ω resister
0 - No VBAT discharing selected

DISCHRG_VCC - Bit 14 - Discharge VCC Core
1- Discharge Vcc voltage through 1200 Ω resister
0 - No discharge of VCC Core voltage select

Strobe7: Activation Clock Frequency Select Register
ACTCLK_Freq_Sel - Bits 2 - 0 - Trims the ACT oscillator to set the frequency

Table 8. ACTIVE Sample Clock Width

SETTING	ACTIVE Sample Clock Interval
000	0.5 ACTCLK Period
001	1 ACTCLK Period
010	1.5 Clock Period
011	2 Clock Period
100	2.5 Clock Period
101	3 Clock Period
110	3.5 Clock Period
111	4 Clock Period

Table 9. Activation Clock Frequency Selections

SETTING	CAP SETTING	FREQUENCY
000	60 fF	1 kHz
001	120 fF	0.75 kHz
010	180 fF	0.35 kHz
011	240 fF	250 Hz
100	150 fF	400 kHz
101	210 fF	280 Hz
110	270 fF	220 Hz

Activation Registers

SHELF_CNT_LO: Shelf counter low

15	14	13	12	11	10	9	8
s_cnt_low (cont.)							
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
s_cnt_low							
r0	r0	r0	r0	r0	r0	r0	r0

s_cnt_low	Bits 0-15	Lower 16 bits of Shelf counter

This is a read only Register

SHELF_CNT_HI: Shelf counter high

15	14	13	12	11	10	9	8
–	–	–	s_cnt_high (cont.)				
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
s_cnt_high							
r0	r0	r0	r0	r0	r0	r0	r0

s_cnt_high	Bits 0-12	Upper 13 bits of Shelf counter

This is a read only Register

ACTIVATION_DATAIN: Activation data in

15	14	13	12	11	10	9	8
act_d_in (cont.)							

7	6	5	4	3	2	1	0
act_d_in							

act_d_in	Bits 0-15	Activation Data In - Value of the Strobe7-0 register which is selected by the ACTIVATION_RD_ADDR register

This is a read only Register

ACTIVATION_DATAOUT: Activation data out

15	14	13	12	11	10	9	8
act_d_out (cont.)							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
act_d_out							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

act_d_out	Bits 0-15	Activation Data Out - The data value to be written into the Strob1-0 register which is selected by the ACTIVATION_STROBES register

ACTIVATION_STROBES: Activation strobes

15	14	13	12	11	10	9	8
Password							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0
7	6	5	4	3	2	1	0
strb7	**strb6**	**strb5**	**strb4**	**strb3**	**strb2**	**strb1**	**strb0**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

strbx	Bits 0-15	Activation Strobe - These bits are 'one-hot' coded to select the Strob7-0 register to be written with the contents of the ACTIVATION_DATAOUT register

strb0	Bit 0	Activation strobe 0
strb1	Bit 1	Activation strobe 1
strb2	Bit 2	Activation strobe 2
strb3	Bit 3	Activation strobe 3
strb4	Bit 4	Activation strobe 4
strb5	Bit 5	Activation strobe 5
strb6	Bit 6	Activation strobe 6
strb7	Bit 7	Activation strobe 7
Password	Bits 8-15	Write 0xA5 to initiate Strobex register Write - Always reads back 0x96

Strb0-7 are self clearing bits

ACTIVATION_RD_ADDR: Activation read address

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
–	–	–	–	–	read_add		
r-0	r-0	r-0	r-0	r-0	rw-0	rw-0	rw-0

read_add	Bits 0-2	Register Read Address - Decimal coded index of Strobe7-0 register to be read back in ACTIVATION_DATAIN register

ACTIVATION_STATUS: Activation Status

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
–	–	–	–	–	**act_test**	**act_sleep**	**act_sense**
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

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This is a read only register.

act_sense   Bit 0   Logic high signal indicate sense button changed state (pushed)

act_sleep   Bit 1   Sleep Comparator OUT. Can be configured like MSP Timer_0 out (INT_rise, INT fall, Level Latch High, Level latch Low)

act_test   Bit 2   Counter out for testing

ACTIVATION_SENSE: Activation Sense

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	**Act_sense_cir**
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

This is a self clearing register

activation_sense_cir   Bit 0   Acknowledge for clearing the sense_interrupt signal (should be a high pulse that can comes from SW or HW)

Timer0_A3

Timer0_A3 is a 16-bit timer/counter with three capture/compare registers. Timer0_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer0_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. AFE4110 Timer-0 has different Clocks Sources and CCx input multiplexing, compared to MSP430x5 documentation. Timer-0 Clock sources and the CCx input signals described in this document.

Product Folder Link(s) :*AFE4110*

Timer0_A3 Signal Connections and Block Diagrams
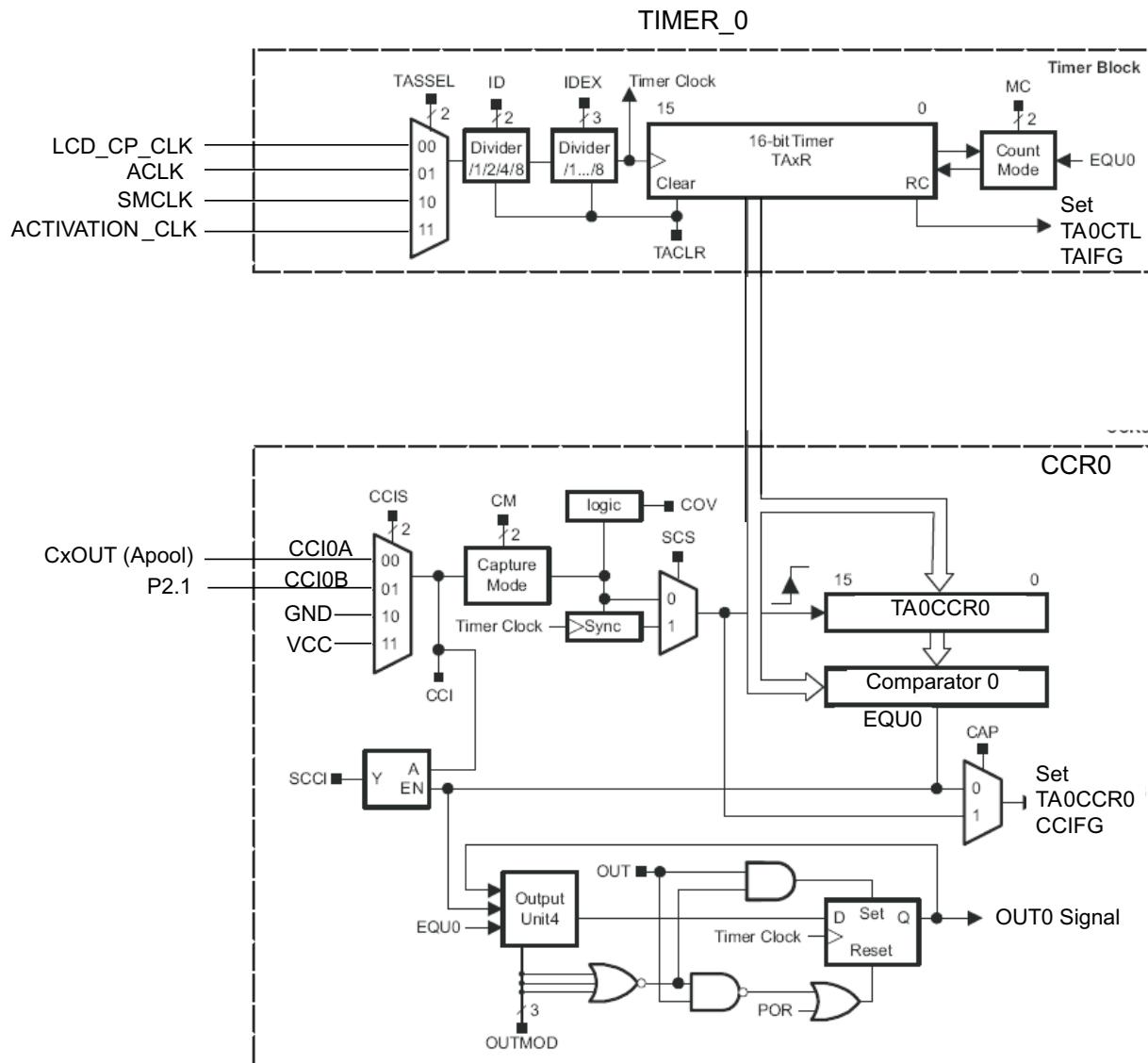
Figure 3. Timer0_CCR0 Block Diagram
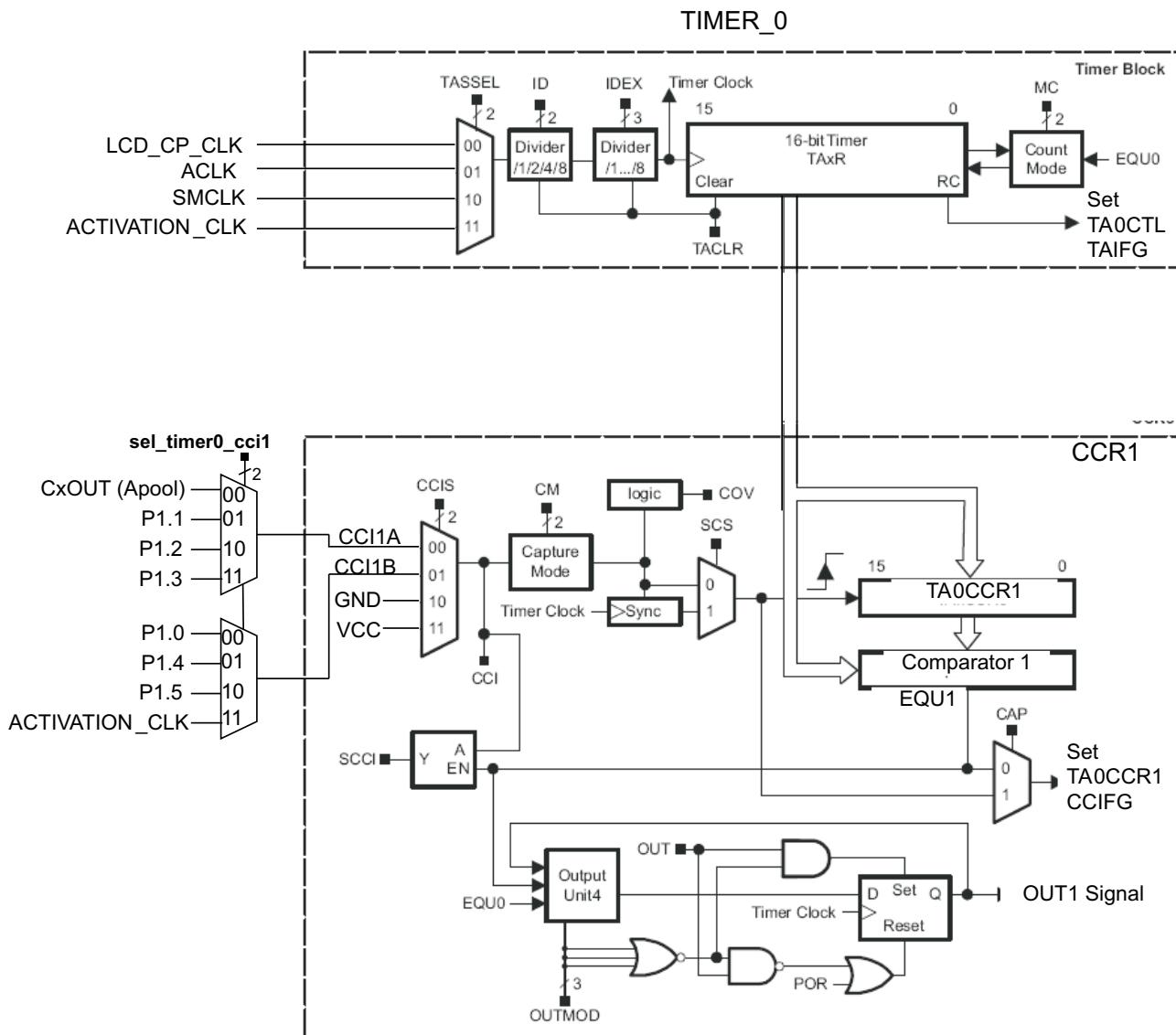
TIMER_0

Figure 4. Timer0_CCR1 Block Diagram
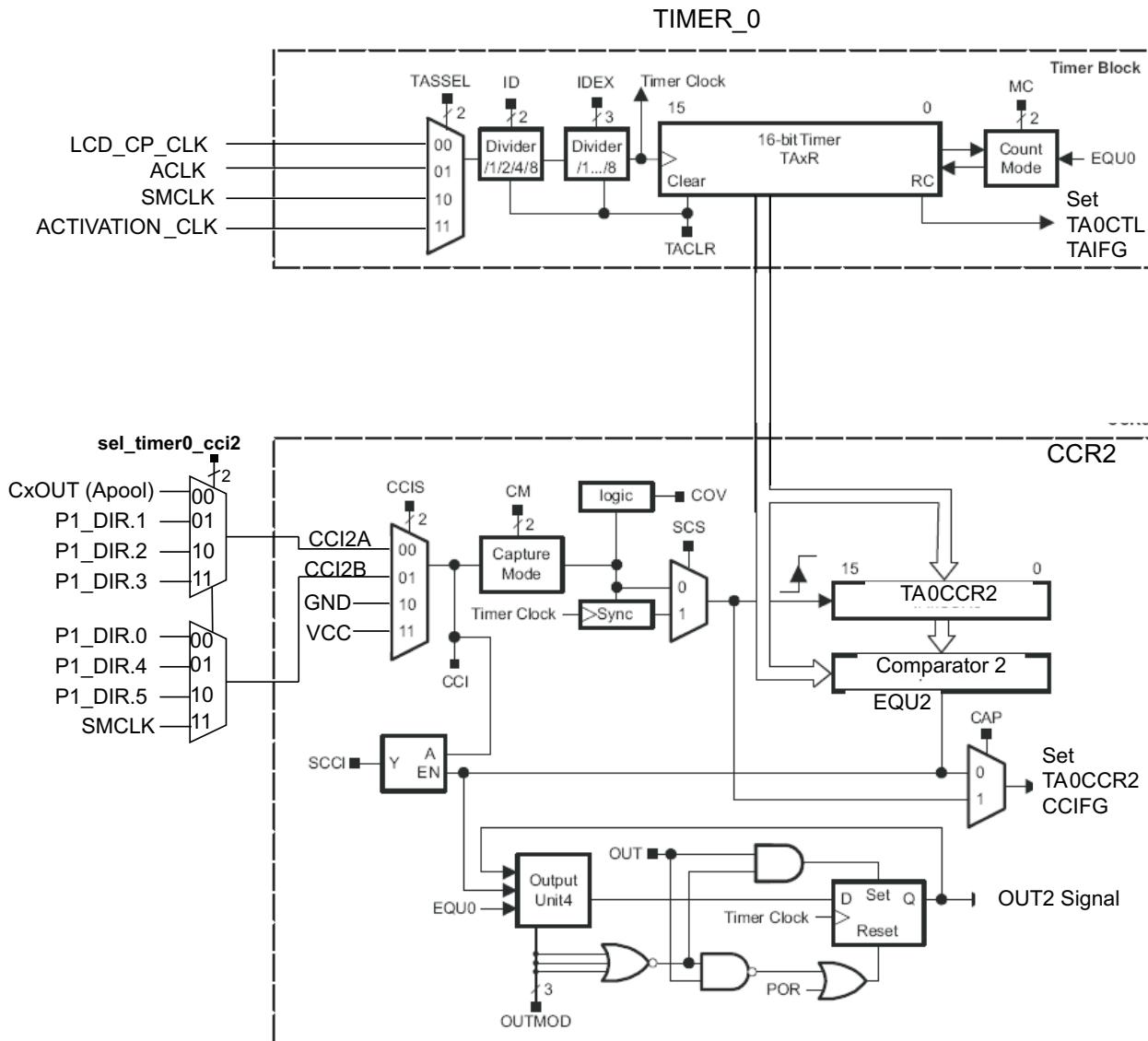
Figure 5. Timer0_CCR2 Block Diagram

Timer1_A3

Timer1_A3 is a 16-bit timer/counter with three capture/compare registers. Timer1_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer1_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. AFE4110 Timer-1 has different Clocks Sources and CCx input multiplexing, compared to MSP430x5 documentation. Timer-1 Clock sources and the CCx input signals described in this document.

Timer1_A3 Signal Connections and Block Diagrams
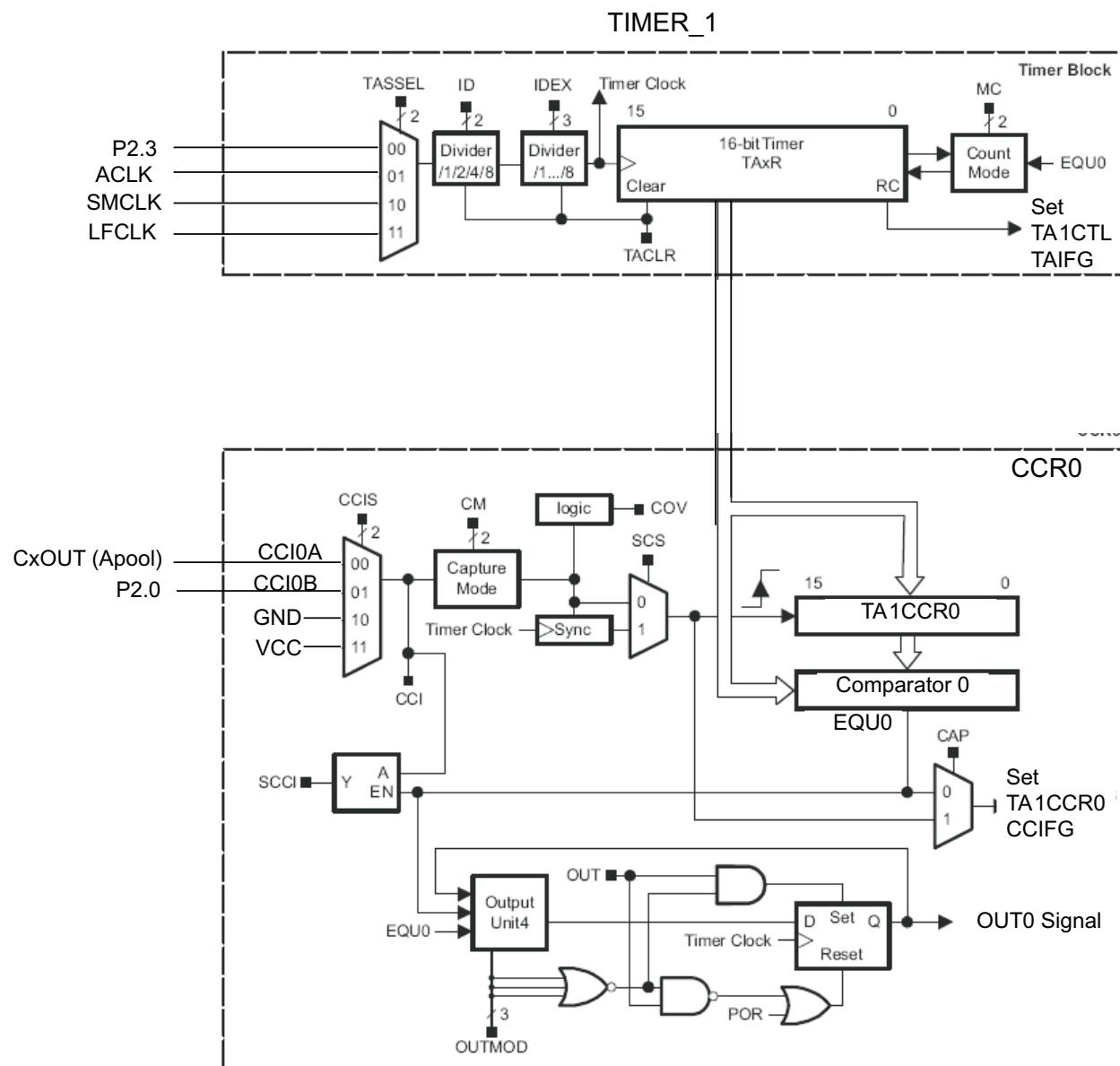
TIMER_1

Figure 6. Timer1_CCR0 Block Diagram
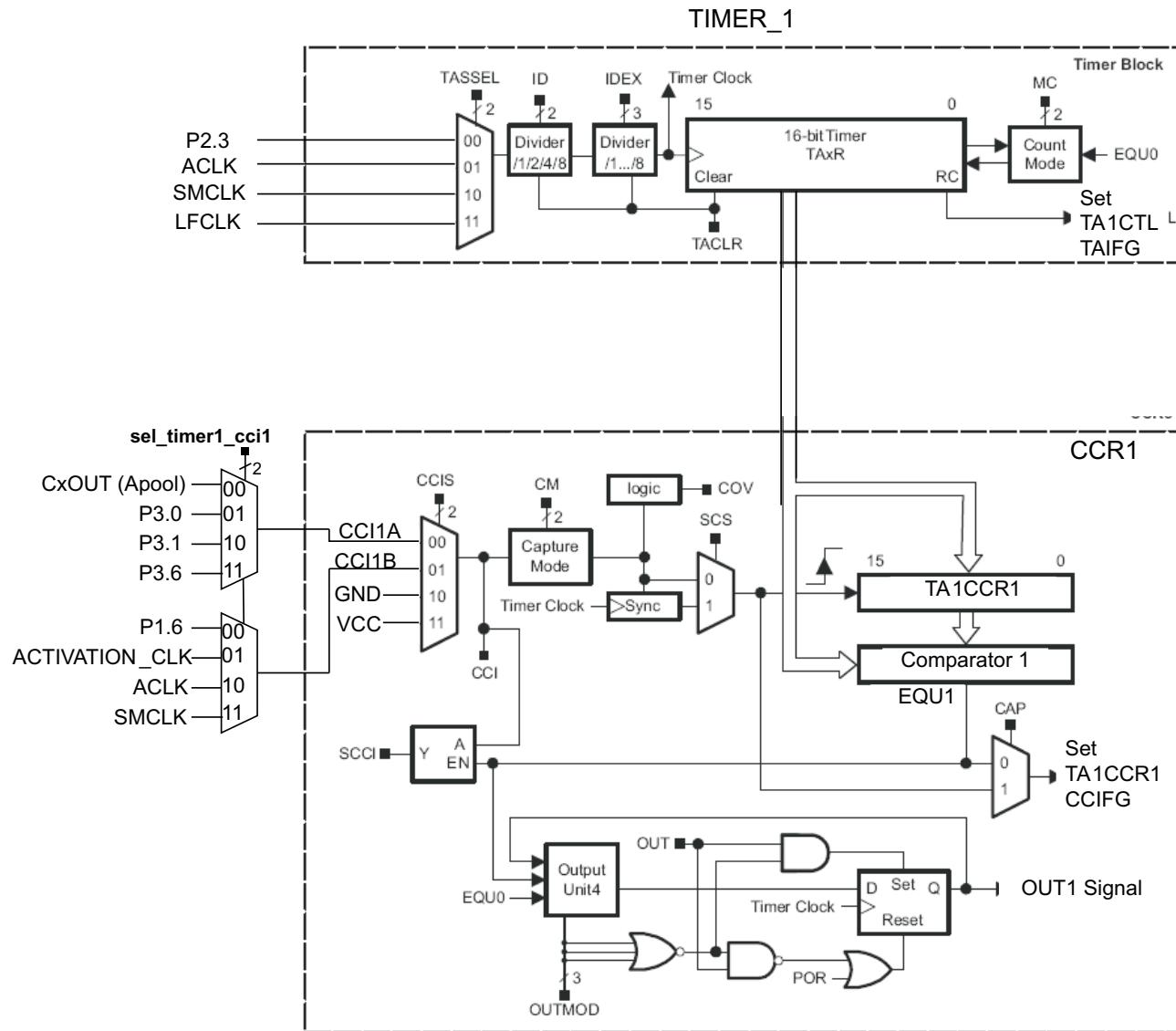
TIMER_1

Figure 7. Timer1_CCR1 Block Diagram
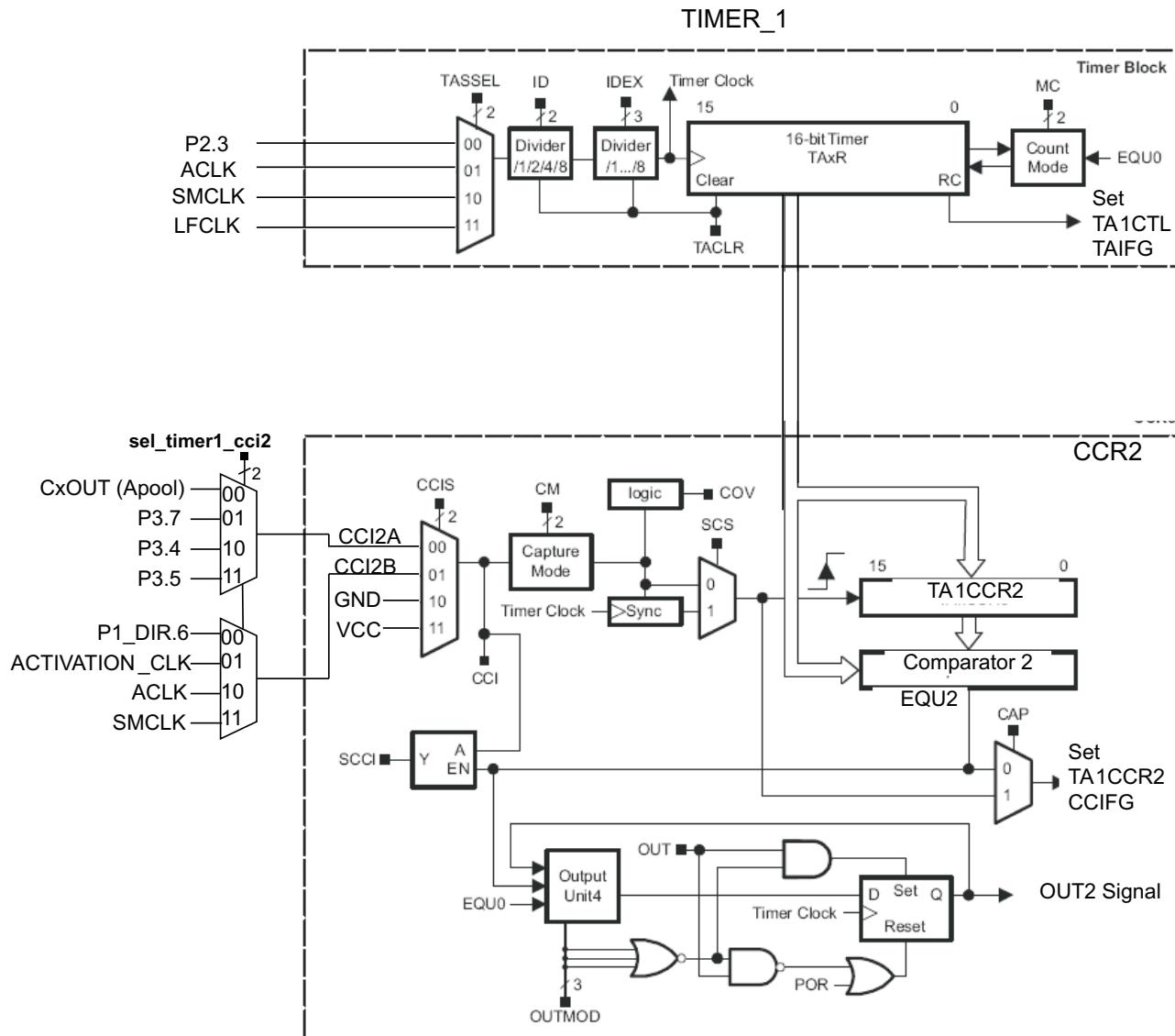
TIMER_1

Figure 8. Timer1_CCR2 Block Diagram

LCD_E

The LCD_E is equivalent to TI LCD-B (MSP430x4 family) driver that generates the segment and common signals required to drive an LCD display. The LCD_E controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump.

Furthermore it is possible to control the level of the LCD voltage and, thus, contrast by software.

The LCD_E operating voltage is minimum 2V, therefore the user must verify a 2V voltage is available on pin 37 either by activating the CP_1P8 or using external power supply.

The LCD_CP is using the CP_OSC as the reference oscillator for boosting the 2V to LCD operating voltage. The CP_OSC is working from battery voltage (minimum 1.1V) and is shared with CP_1P8 which also using it for generating the 2V from the battery voltage internally.

A-Pool

The analog functions pool (A-Pool) provides a series of function that can be configured to a Digital to Analog converter (DAC), multi channel Analog to Digital converter (ADC), Supply voltage supervisor SVS and Comparator, input voltage dividers and an internal reference source allow wide range of combined analog functions. For a complete description of A-Pool, see the Analog Pool chapter of the MSP430x09x Family Users Guide (SLAU321)
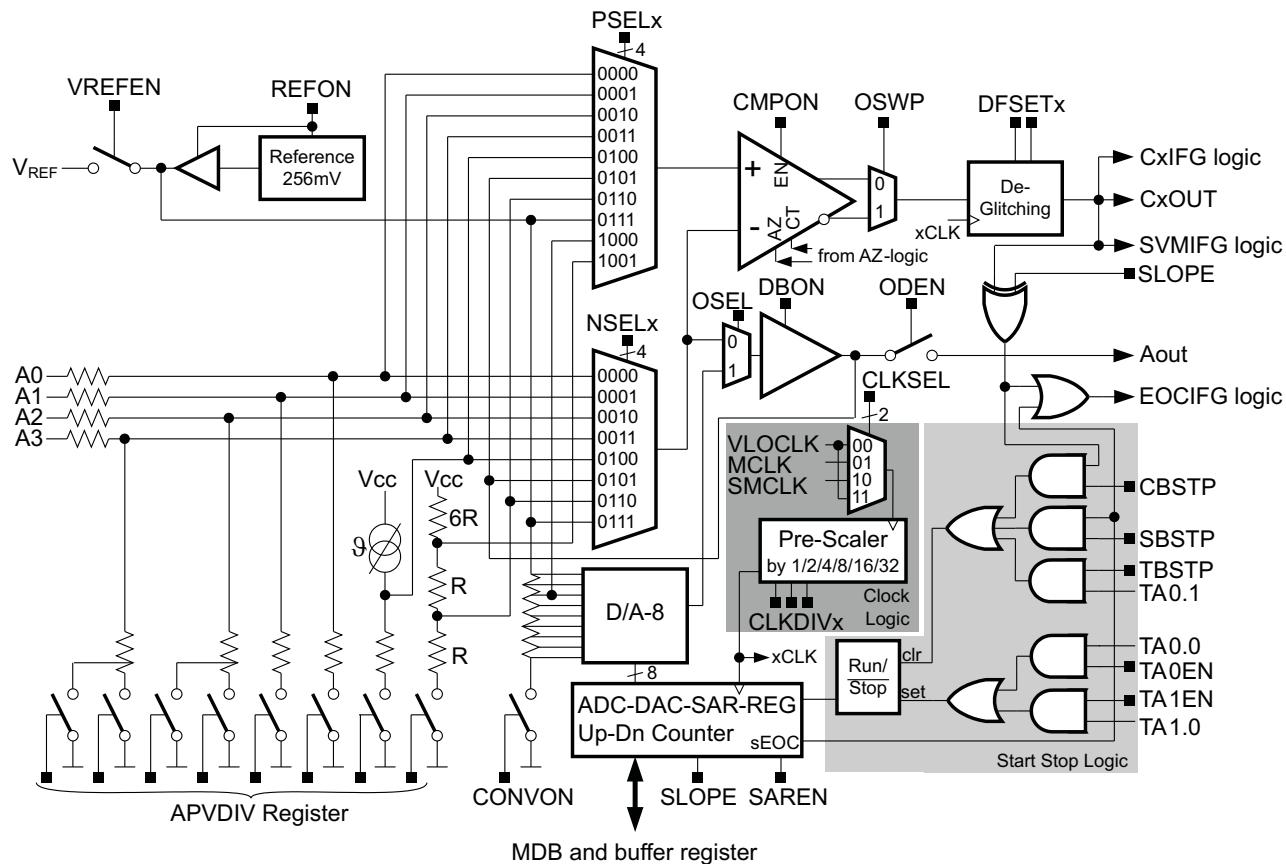
Figure 9. Block Diagram of A-Pool

Table 10. A-Pool Analog inputs Connection Table

A-POOL ANALOG INPUT	PAD	PSEL	NSEL	A3PSEL	A0_port_sel
A3a	P1.2	0011	0011	0	X
A3b	P1.3	0011	0011	1	X
A2	P1.0	0010	0010	X	X
A1	P1.1	0001	0001	X	X
A0a	P1.4	0000	0000	X	0
A0b	P3.3	0000	0000	X	1

Versatile I/O Port P1, P2, P3, P4

The versatile I/O ports P1, P2, P3 and P4 feature device dependent reset values. The reset values for the AFE4110 devices are shown in below.

Table 11. Versatile Port Reset Values

PORT NUMBER	PxOUT	PxDIR	PxREN	PxSEL0	PxSEL1	RESET	Ports ON	COMMENT	I/O POWER DOMAIN
P1.0	0	0	0	0	0	PUC	yes	P1.0, input	V_{DD}
P1.1	0	0	0	0	0	PUC	yes	P1.1, input	V_{DD}
P1.2	0	0	0	0	0	PUC	yes	P1.2, input	V_{DD}
P1.3	0	0	0	0	0	PUC	yes	P1.3, input	V_{DD}
P1.4	0	0	0	0	0	PUC	yes	P1.4, input	V_{DD}
P1.5	0	0	0	0	0	PUC	yes	P1.5, input	V_{DD}
P1.6	0	0	0	0	0	PUC	yes	P1.6, input	V_{DD}
P1.7	–	–	–	–	–	–	–	–	
P2.0	1	0	1	1	1	BOR	no	JTAG TCK	VDDIO
P2.1	1	0	1	1	1	BOR	no	JTAG TMS	VDDIO
P2.2	1	0	1	1	1	BOR	no	JTAG TDI	VDDIO
P2.3	0	1	0	1	1	BOR	no	JTAG TDO	VDDIO
P3.0	0	0	0	0	0	PUC	yes	P3.0, input	V_{DD}
P3.1	0	0	0	0	0	PUC	yes	P3.1, input	V_{DD}
P3.2	0	0	0	0	0	PUC	yes	P3.2, input	V_{DD}
P3.3	0	0	0	0	0	PUC	yes	P3.3, input	V_{DD}
P3.4	0	0	0	0	0	PUC	yes	P3.4, input	V_{DD}
P3.5	0	0	0	0	0	PUC	yes	P3.5, input	V_{DD}
P3.6	0	0	0	0	0	PUC	yes	P3.6, input	VDDIO
P3.7	0	0	0	0	0	PUC	yes	P3.7, input	VDDIO
P4.0	0	0	0	0	0	PUC	Yes	P4.0, input	VDDIO
P4.1	0	0	0	0	0	PUC	Yes	P4.1, input	VDDIO
P4.2	0	0	0	0	0	PUC	Yes	P4.2, input	VDDIO
P4.3	0	1	0	0	0	PUC	yes	P4.3, input	VDDIO

Product Folder Link(s) :*AFE4110*

Table 12. Peripherals

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
AREGS	Analog e-fuse	ANALOG_FUSETRIM	04A0h	16h
	Analog timer control	ANALOG_TIMERCTL		14h
	Analog port control 2	ANALOG_PORTCTL2		12h
	Analog port control 1	ANALOG_PORTCTL1		10h
	Analog ana control	ANALOG_ANACTL		0Eh
	Analog bias current control	ANALOG_IBIASCTL		0Ch
	Analog LDO control	ANALOG_LDOCTL		0Ah
	Analog LDO configuration	ANALOG_LDOCFG		08h
	Analog LCDP control	ANALOG_LCDPCTL		06h
	Analog LCD charge pump control	ANALOG_LCDCPCFG		04h
	Analog charge pump 1.8V control	ANALOG_CP1P8CTL		02h
	Analog charge pump 1.8V configuration	ANALOG_CP1P8CFG		00h
Activation	Activation Sense	ACTIVATION_SENSE	0480h	0Eh
	Activation Status	ACTIVATION_STATUS		0Ch
	Activation read address	ACTIVATION_RD_ADDR		0Ah
	Activation strobes	ACTIVATION_STROBES		08h
	Activation data out	ACTIVATION_DATAOUT		06h
	Activation data in	ACTIVATION_DATAIN		04h
	Shelf counter high	SHELF_CNT_HI		02h
	Shelf counter low	SHELF_CNT_LO		00h
LCD	Reserved		0400h	46h-5Fh
	LCD Blinking 1–6[1]	LCDB1-6		40h-45h
	Reserved			26h-3Fh
	LCD memory 1–6[1]	LCDM1-6		20h-25h
	LCD_B interrupt vector	LCDBIV		1Eh
	Reserved			14h-1Ch
	LCD_B charge pump control	LCDBCPCTL		12h
	Reserved			0Ah-11h
	LCD_B voltage control register	LCDBVCTL		08h
	LCD_B memory control register	LCDBMEMCTL		06h
	LCD_B blinking control register	LCDBBLKCTL		04h
	LCD B control register 1	LCDBCTL1		02h
	LCD B control register 0	LCDBCTL0		00h
Timer1_A3	Timer1_A interrupt vector	TA1IV	0380h	2Eh
	Capture/compare register 2	TA1CCR2		16h
	Capture/compare register 1	TA1CCR1		14h
	Capture/compare register 0	TA1CCR0		12h
	Timer1_A register	TA1R		10h
	Capture/compare control 2	TA1CCTL2		06h
	Capture/compare control 1	TA1CCTL1		04h
	Capture/compare control 0	TA1CCTL0		02h
	Timer1_A control	TA1CTL		00h

(1) Six 8 bit registers, but the LCD blinking and memory registers can also be accessed as word

Table 12. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
Timer0_A3	Timer0_A interrupt vector	TA0IV	0340h	2Eh
	Capture/compare register 2	TA0CCR2		16h
	Capture/compare register 1	TA0CCR1		14h
	Capture/compare register 0	TA0CCR0		12h
	Timer1_A register	TA0R		10h
	Capture/compare control 2	TA0CCTL2		06h
	Capture/compare control 1	TA0CCTL1		04h
	Capture/compare control 0	TA0CCTL0		02h
	Timer1_A control	TA0CTL		00h
Port P4	Port P4 interrupt Flag	P4IFG	0220h	1Dh
	Port P4 interrupt enable	P4IE		1Bh
	Port P4 interrupt edge select	P4IES		19h
	Port P4 interrupt vector word	P4IV		1Eh
	Port P4 selection 1	P4SEL1		0Dh
	Port P4 selection 0	P4SEL0		0Bh
	Port P4 pullup/pulldown enable	P4REN		07h
	Port P4 direction	P4DIR		05h
	Port P4 outout	P4OUT		03h
	Port P4 input	P4IN		01h
Port P3	Port P3 interrupt Flag	P3IFG	0220h	1Ch
	Port P3 interrupt enable	P3IE		1Ah
	Port P3 interrupt edge select	P3IES		18h
	Port P3 interrupt vector word	P3IV		0Eh
	Port P3 selection 1	P3SEL1		0Ch
	Port P3 selection 0	P3SEL0		0Ah
	Port P3 pullup/pulldown enable	P3REN		06h
	Port P3 direction	P3DIR		04h
	Port P3 outout	P3OUT		02h
	Port P3 input	P3IN		00h
Port P2	Port P2 interrupt Flag	P2IFG	0200h	1Dh
	Port P2 interrupt enable	P2IE		1Bh
	Port P2 interrupt edge select	P2IES		19h
	Port P2 interrupt vector word	P2IV		0Eh
	Port P2 selection 1	P2SEL1		0Dh
	Port P2 selection 0	P2SEL0		0Bh
	Port P2 pullup/pulldown enable	P2REN		07h
	Port P2 direction	P2DIR		05h
	Port P2 outout	P2OUT		03h
	Port P2 input	P2IN		01h
Port P1	Port P1 interrupt Flag	P1IFG	0200h	1Ch
	Port P1 interrupt enable	P1IE		1Ah
	Port P1 interrupt edge select	P1IES		18h
	Port P1 interrupt vector word	P1IV		0Eh
	Port P1 selection 1	P1SEL1		0Ch
	Port P1 selection 0	P1SEL0		0Ah
	Port P1 pullup/pulldown enable	P1REN		06h
	Port P1 direction	P1DIR		04h

Table 12. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
	Port P1 outout	P1OUT		02h
	Port P1 input	P1IN		00h
A-POOL	Analog pool interrupt vector register	APIV	01A0h	1Eh
	Analog pool interrupt enable register register	APIE		1Ch
	Analog pool interrupt flag register	APIFG		1Ah
	Analog pool fractional value buffer	APFRACTB		16h
	Analog pool fractional value register	APFRACT		14h
	Analog pool integer value buffer	APINTB		12h
	Analog pool integer value register	APINT		10h
	Analog pool voltage divider register	APVDIV		06h
	Analog pool operation mode register	APOMR		04h
	Analog pool control register	APCTL		02h
	Analog pool configuration register	APCNF		00h
CSYS	Reset vector generator	SYSRSTIV	0180h	1Eh
	System NMI vector generator	SYSSNIV		1Ch
	User NMI vector generator	SYSUNIV		1Ah
	Bus error vector generator	SYSBERRIV		18h
	System Configuration register	SYSCNF		10h
	JTAG mailbox output register #1	SYSJMBO1		0Eh
	JTAG mailbox output register #0	SYSJMBO0		0Ch
	JTAG mailbox input register #1	SYSJMBI1		0Ah
	JTAG mailbox input register #0	SYSJMBI0		08h
	JTAG mailbox control register	SYSJMBC		06h
	System control register	SYSCTL		00h
CCS	CCS control 8 register	CCSCTL8	0160h	10h
	CCS control 7 register	CCSCTL7		0Eh
	CCS control 6 register	CCSCTL6		0Ch
	CCS control 5 register	CCSCTL5		0Ah
	CCS control 4 register	CCSCTL4		08h
	CCS control 2 register	CCSCTL2		04h
	CCS control 1 register	CCSCTL1		02h
	CCS control 0 register	CCSCTL0		00h
WDT_A	WDT_A Watchdog timer control	WDTCTL	0150h	0Ch
PMM	PMM PMM control 0	PMMCTL0	0120h	00h
ET-WRAPPER	ET-Wrapper ET Key and select	ETKEYSEL	0110h	00h
Special Functions	Special Functions SFR Reset pin control register	SFRRPCR	0100h	04h
	SFR interrupt flag register	SFRIFG1		02h
	SFR interrupt enable register	SFRIE1		00h

Legend

rw: Bit can be read and written.

> **rw-0,1:** Bit can be read and written. It is reset or set by PUC. [1]
>
> **rw-(0,1):** Bit can be read and written. It is reset or set by POR [2]
>
> **rw-[0,1]:** Bit can be read and written. It is reset or set by BOR. [3]

–   bit is not present in device

(1)   PUC is for "normal" registers which should be reset at all time
(2)   POR is used for registers, which should not be reset by a WDT event (like status information)
(3)   BOR is used for registers, which are configured during boot code execution and should not be reset during normal reset events

Analog Control Registers

ANALOG_CP1P8CFG: Analog charge pump 1.8V configuration

15	14	13	12	11	10	9	8
–	–	–	1p8_valid	clk_sel	force_clk	mode_sel	cp_1p8_pd
r-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-1

7	6	5	4	3	2	1	0
cp_1p8_hyst_set		cp_1p8_out_level			cp_1p8_clk_div		
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

cp_1p8_clk_div	Bits 2-0	Select the clock divider (see table below)
cp_1p8_out_level	Bits 5-3	Set the CP valid threshold voltage (see table below)
cp_1p8_hyst_set	Bits 7-6	Set the comparator hysteresis (inside the CP loop) – 000 means close hysteresis, and 111 means wide hysteresis. When using fast clock (high current) the user must use close hysteresis 000.
cp_1p8_pd	Bit 8	Powers Down the charge pump circuitries
cp_1p8_clk_mode_sel	Bit 9	Test mode of the CP loop, break the loop to control by the signal fram_force_clk
cp_1p8_force_clk	Bit 10	Force a continuous clock to the Charge Pump (in test mode)
cp_1p8_clk_sel	Bit 11	Select which clock to use (internal or external)
cp_1p8_valid	Bit 12	Valid 1.8v indication output

ANALOG_CP1P8CTL: Analog charge pump 1.8V control

15	14	13	12	11	10	9	8
Reserved							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

7	6	5	4	3	2	1	0
cp_1p8_valid_level		clk_refresh_freq		ext_cap_en	clamp	clamp_en	quiet_mode
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1	rw-0

cp_1p8_quiet_mode	Bit 0	Inhibits charge pump clocking
cp_1p8_force_out_clamp_en	Bit 1	Controls the output clamp switch to AVDD_BAT (0 - clamp according to control; 1- clamp according to PD control)
cp_1p8_force_out_clamp	Bit 2	Force the output clamp to AVDD_BAT
cp_1p8_ext_cap_en	Bit 3	Set to high when high current is required
cp_1p8_clk_refresh_freq	Bits 4-5	Set the frequency for refreshing the rdiv cap (see table below)
cp_1p8_valid_level	Bits 6-7	Set the CP valid threshold voltage (see table below)
Reserved	Bits 8 - 15	

cp_1p8_out_level			cp_1p8_clk_div table:	
Setting	**Freq**		**Setting**	**Freq**
000	2.075 V		000	FS (4MHz)
001	2.05 V		001	001 FS/2
010	2.025 V		010	FS/4
011	2 V		011	FS/8
100	1.975 V		100	FS/16
101	1.95 V		101	FS/32
110	1.925 V		110	FS/64
111	1.9 V		111	FS/128

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cp_1p8_clk_refresh_freq table:			cp_1p8_clk_valid_level table:	
Setting	**Freq**		**Setting**	**Freq**
00	156.25 Hz		00	1.75 V
01	312.5 Hz		01	1.8 V
10	312.5 Hz		10	1.85 V
11	625 Hz		11	1.9 V

The clock output is a single 50 µs pulse

ANALOG_LCDCPCFG: Analog LCD charge pump controlR

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

7	6	5	4	3	2	1	0
–	–	–	Force_clk	–	–	–	clk_sel
r-0	r-0	r-0	rw-0	r-0	r-0	r-0	rw-0

lcd_cp_clk_sel	Bit 0	NC (Not connected)
lcd_cp_force_clk	Bit 4	NC

ANALOG_LCDPCTL: Analog LCDP control

15	14	13	12	11	10	9	8
seg11_en	seg10_en	seg9_en	seg8_en	seg7_en	seg6_en	seg5_en	seg4_en
rw-1	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1

7	6	5	4	3	2	1	0
seg3_en	seg2_en	seg1_en	seg0_en	com3_en	com2_en	com1_en	com0_en
rw-1	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1

com0_en	Bit 0	Enable LCD pin common 0. "1" – enable, "0" – disable
com1_en	Bit 1	Enable LCD pin common 1. "1" – enable, "0" – disable
com2_en	Bit 2	Enable LCD pin common 2. "1" – enable, "0" – disable
com3_en	Bit 3	Enable LCD pin common 3. "1" – enable, "0" – disable
seg0_en	Bit 4	Enable LCD pin segment 0. "1" – enable, "0" – disable
seg1_en	Bit 5	Enable LCD pin segment 1. "1" – enable, "0" – disable
seg2_en	Bit 6	Enable LCD pin segment 2. "1" – enable, "0" – disable
seg3_en	Bit 7	Enable LCD pin segment 3. "1" – enable, "0" – disable
seg4_en	Bit 8	Enable LCD pin segment 4. "1" – enable, "0" – disable
seg5_en	Bit 9	Enable LCD pin segment 5. "1" – enable, "0" – disable
seg6_en	Bit 10	Enable LCD pin segment 6. "1" – enable, "0" – disable
seg7_en	Bit 11	Enable LCD pin segment 7. "1" – enable, "0" – disable
seg8_en	Bit 12	Enable LCD pin segment 8. "1" – enable, "0" – disable
seg9_en	Bit 13	Enable LCD pin segment 9. "1" – enable, "0" – disable
seg10_en	Bit 14	Enable LCD pin segment 10. "1" – enable, "0" – disable
seg11_en	Bit 15	Enable LCD pin segment 11. "1" – enable, "0" – disable

To enable the LCD both the relevant ANALOG_LCDPCTL bit should be set to 1 and the LCDON bit in LCD register LCDBCTL0 should be set to 1.

ANALOG_LDOCFG: Analog LDO configuration

15	14	13	12	11	10	9	8
–	–	ldo_out_mux		–	–	cap_sw_general	
r-0	r-0	rw-0	rw-0	r-0	r-0	rw-0	rw-0

7	6	5	4	3	2	1	0
high_cap_sw	low_cap_sw	ldo_bypass	ldo_pd	–	ldo_trim_bits		
rw-0	rw-0	rw-0	rw-1	r-0	rw-0	rw-0	rw-0

ldo_trim_bits	Bits 0-2	LDO voltage trimming (see table below)
ldo_pd	Bit 4	"1" LDO Shut down. Vout=open
ldo_bypass	Bits 5	"1" Bypass the LDO, shorts LDO Vout to VDD
low_cap_sw	Bit 6	"1" Connect the low calibration capacitor (20pF)
high_cap_sw	Bit 7	"1" Connect the high calibration capacitor (40pF)
cap_sw_general	Bit 8-9	NC
ldo_out_mux	Bit 12-13	"00" set the LDO output switch to "off". "11" set LDO output switch to "on"

ldo_trim_bits table:	
Setting	Vout[V]
000	1.045
001	10.72
010	1.1
011	1.125
100	0.96
101	0.98
110	1
111	1.02

ANALOG_LDOCTL Analog LDO control

15	14	13	12	11	10	9	8
ldo_ctl (cont.)							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

7	6	5	4	3	2	1	0
ldo_ctl			a0_port_sel	LDO_IO_sel			
rw-0	rw-0	rw-0	rw-1	r-0	rw-0	rw-0	rw-0

LDO_IO_sel	Bit 0-3	Used to mux the LDO to IOs in the following order: <0> – port 1.0; <1> – port 1.1; <2> – port 1.4; <3> – port 3.3;
a0_port_sel	Bit 4	Select which IO goes to A0 input of the A-Pool – ,0. selects port 1.4
ldo_ctl	Bits 5-15	NC

ANALOG_IBIASCTL: Analog bias current control

15	14	13	12	11	10	9	8
spare		lf_force_mode	hfos_current	osc_6m current		ctl_ref_current	
rw-0	rw-0	rw-0	rw-1	rw-0	rw-0	rw-0	rw-0

7	6	5	4	3	2	1	0
ibias_pd							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

lbias_pd	Bits 0-7	Powering down the bias currents Not used
ctl_ref_current	Bits 8-9	Select main reference current: 00 – 10nA (Deafult) 01 – 6nA 10 – 12nA 11 – 8nA
osc_6m current	Bits 10-11	Controls the HF_OSC current setting: 00 – 1 µA 01 – 3 µA 10 – 2 µA 11 – 4 µA
hfos_current	Bit 12	1 – Setting the HF_OSC to low frequency/low current mode (1MHz/10µA)
lf_mode_force	Bit 13	0 – lf_mode is forced on hf_osc ; 1 – lf_mode is working only of I_trim is 00
spare	Bits 14-15	Not Used

HF_OSC LF Mode - Typical frequency after HF-OSC calibrated to 4.4MHz

hfos_current<12>	lf_mode_force<13>	osc_6m current<11,10>	HF-OSC Frq [MHz]
0	x	00	1.87
		01	4.44
		10	3.27
		11	5.4
1	0	00	1
		01	
		10	
		11	
1	1	00	1
		01	3.9
		10	2.6
		11	5

ANALOG_ANACTL: Analog ana control

15	14	13	12	11	10	9	8
ana_ctl (not used)					lpm5_en_lcd_ana_shell	Cp_osc_trim	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-1	rw-0	rw-0

7	6	5	4	3	2	1	0
Reserved							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Reserved	Bits 0-7	
Ana_ctl_cp_osc_trim	Bits 8-9	Course trimming of the 2 charge pumps oscillator (current trimming)
lpm5_lcd_ana_shell	Bit 10	"1" powers down (~40nA) the max_detect block inside the LCD Block
ana_ctl	Bits 11-15	Not used

ANALOG_PORTCTL1: Analog Analog port control 1

15	14	13	12	11	10	9	8
bp_dir_sync		irq_on_p3_7	irq_on_p3_6	irq_on_p3_5	irq_on_p3_4	irq_on_p3_3	irq_on_p3_2
rw-0	r-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

7	6	5	4	3	2	1	0
		sel_port3_7		–	–	sel_port3_6	
r-0	r-0	rw-0	rw-0	r-0	r-0	rw-0	rw-0

sel_port3_6, sel_port3_7: PORT3.6 and PORT3.7 Input multiplexer control

sel_port3_6	**Bits 1,0**	**0,0**	**0,1**	**1,0**	**1,1**
	P3SEL1/0 = 01	TA0.0	TA0.1	TA0.2	TA1.1
	P3SEL1/0 = 10	NEG(TA0.0)	NEG(TA0.1)	NEG(TA0.2)	NEG(TA1.1)
	P3SEL1/0 = 11	BROWNOUT	ACTIVATION_SENSE	LFCLK	CP_1P8_COMP
sel_port3_7	**Bits 5,4**	**0,0**	**0,1**	**1,0**	**1,1**
	P3SEL1/0 = 01	TA0.0	TA0.1	TA0.2	LCD_COMP
	P3SEL1/0 = 10	NEG(TA0.0)	NEG(TA0.1)	NEG(TA0.2)	NEG(LCD_COMP)
	P3SEL1/0 = 11	LCD_CP_CLK	LCD_FCLK	HFCLK	ACTIVATION_OSC_1KHZ
sel_irq_on_p3_2	Bit 8	force '0' when test_atpg_en_i = '1'			
sel_irq_on_p3_3	Bit 9				
sel_irq_on_p3_4	Bit 10				
sel_irq_on_p3_5	Bit 11				
sel_irq_on_p3_6	Bit 12				
sel_irq_on_p3_7	Bit 13				
bypass_dir_sync	Bit 15	"1" Enable Portx.y direct DIR signal connection to TiIMERx CCx (No Dithering). "0" Enable Portx.y DIR signal (sync to LFCLK) connection to TiIMERx CCx .Dithering enabled when HF-CLK or EXCLK selected as Timer Clock source.[1]			

(1)   force '1' when test_atpg_en_i = '1'

ANALOG_PORTCTL2: Analog Analog port control 2

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

7	6	5	4	3	2	1	0
dp1_6	**dp1_5**	**dp3_5**	**dp3_4**	**dp3_3**	**dp3_2**	**dp3_1**	**dp3_0**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

disable_p3_0	Bit 0	"1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage[1]
disable_p3_1	Bit 1	"1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage[1]
disable_p3_2	Bit 2	"1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage [1]
disable_p3_3	Bit 3	"1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage [1]
disable_p3_4	Bit 4	"1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage [1]
disable_p3_5	Bit 5	"1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage[1]
disable_p1_5	Bit 6	"1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage [1]
disable_p1_6	Bit 7	"1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage [1]

(1) force '0' when test_atpg_en_i = '1'

ANALOG_TIMERCTL: Analog timer CCx input mux control

15	14	13	12	11	10	9	8
–	–	**sel_timer1_cci2**		–	–	**sel_timer1_cci1**	
r-0	r-0	rw-0	rw-0	r-0	r-0	rw-0	rw-0

7	6	5	4	3	2	1	0
–	–	**sel_timer0_cci2**		–	–	**sel_timer0_cci1**	
r-0	r-0	rw-0	rw-0	r-0	r-0	rw-0	rw-0

sel_port3_6, sel_port3_7: PORT3.6 and PORT3.7 Input multiplexer control

sel_timer0_cci1	**Bits 1,0**	**0,0**	**0,1**	**1,0**	**1,1**
	Timer0 CCI1A Input Select	CxOUT from APOOL	Port P1.1	Port P1.2	Port P1.3
	Timer0 CCI1B Input Select	Port P1.0	Port P1.4	Port P1.5	ACTIVATION_OSC_1KHZ
sel_timer0_cci2	**Bits 5,4**	**0,0**	**0,1**	**1,0**	**1,1**
	Timer0 CCI2A Input Select	CxOUT from APOOL	Port P1.1DIR	Port P1.2DIR	Port P1.3DIR
	Timer0 CCI2B Input Select	Port P1.0DIR	Port P1.4DIR	Port P1.5DIR	SMCLK
sel_timer1_cci1	**Bits 9,8**	**0,0**	**0,1**	**1,0**	**1,1**
	Timer1 CCI1A Input Select	CxOUT from APOOL	Port P3.0	Port P3.1	Port P3.6
	Timer1 CCI1B Input Select	Port P1.6	ACTIVATION_OSC_1KHZ	ACLK	SMCLK
sel_timer1_cci2	**Bits 13,12**	**0,0**	**0,1**	**1,0**	**1,1**
	Timer1 CCI2A Input Select	CxOUT from APOOL	Port P3.7	Port P3.4	Port P3.5
	Timer1 CCI2B Input Select	Port P1.6DIR	ACTIVATION_OSC_1KHZ	ACLK	SMCLK

ANALOG_FUSETRIM: Analog e-fuse

15	14	13	12	11	10	9	8
–	–	–	cal-fact (cont.)				
r-0	r-0	r-0	r-f*	r-f*	r-f*	r-f*	r-f*

7	6	5	4	3	2	1	0
cal-fact					HF-Osc_trim		
r-f*	r-f*	r-f*	r-f*	r-f*	r-f*	r-f*	r-f*

HF-Osc_trim	Bits 2-0	HF-Oscillator trimming. Bits 7-9 of effuse module.
cal_fact	Bits 12-3	Discharge calibration factor. Bits 10-19 of e-fuse module.

- Bits 6-0 of e-fuse module can be read via bits 0-6 of APOOL APTRIM register.
- Some e-fuse bits can also be read via top level register ETTOPCTL0
- This is a read only register.

Additional LCD Registers

LCD registers are described in the LCD_B chapter of the CC430 Family Users Guide (slau259b). The only exceptions:

1. Bit 15 of register LCDBCPCTL (LCDCPCLKEXT bit) has a new functionality as described below.
2. Bit 10 of register ANALOG_ANACTL (lpm5_lcd_ana_shell bit) has a new functionality as described below.

1. LCDBCPCTL, LCD_B Charge Pump Control Register

LCDCPCLKEXT	Bit 15	Selects between internal and external clock source for the LCD Charge Pump	'0' – internal clock source '1' – external clock source

Default value of this bit is rw-0

2. ANALOG_ANACTL

lpm5_lcd_ana_shell	Bit 10	"1" powers down (~40nA) the max_detect block inside the LCD Block

Default value of this bit is rw-1

Additional Timer Registers

Timer registers are described in Timer_A chapter of the MSP430x09x Family Users Guide (SLAU321).

Additional Ports Registers

Port registers are described in Versatile I/O Port chapter of the MSP430x09x Family Users Guide (SLAU321)

Additional APOOL Registers

Analog Functions Pool Module chapter of the MSP430x09x Family Users Guide (SLAU321).

Additional CSYS Registers

Compact System Control Module chapter of the MSP430x09x Family Users Guide (SLAU321). The only exceptions are:

MEMSWP BIT 11

1 - Selects the EMU/Loader memory configuration

0 - Selects the custom ROM memory configuration

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CCS Registers

Compact Clock System chapter of the MSP430x09x Family Users Guide (SLAU321). The only exception is different functionality of register CCSCTL6 as described below:

CCSCTL6: CCS control 6

15	14	13	12	11	10	9	8
–	–	–	Reserved				xt_off
r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0	rw-1

7	6	5	4	3	2	1	0
–	xt_sw				xt_byp	xt_clken2	xt_clken1
r-0	rw-1	r-0	rw-1	rw-1	rw-1	r-0	r-0

xt_clken1	Bit 0	Enable 1 of 32Khz XTAL clock synchronization sequence
xt_clken2	Bit 1	Enable 2 of 32Khz XTAL clock synchronization sequence
xt_byp	Bit 2	32Khz XTAL Bypass
xt_sw	Bits 3-6	32Khz XTAL switch See table below for recommended switch values
xt_off	Bit 8	32Khz XTAL off
Reserved	Bits 9-12	

Recommended control switch settings:

XTL Oscillator Performance	SW4	SW3	SW2	SW1
Least current	1	0	0	0
Fast startup	1	0	1	1

CCS CTL6 enables the external clock/XTAL clock:

> **xt_clken1**, bit 0 and **xt_clken2**, bit 1

1. Enable EXT/XTL Clock by setting the xt_clken2 and xt_clken1 bits.
2. After sufficient delay for XTAL or external clock source to become stable, the user can switch the CCS clock source to EXT/XTL Clock
3. To stop the clock, clear the two bits in the following sequence:
   (a) Switch the CCS clock source to other clock source
   (b) Clear bit xt_clken2
   (c) Wait for at least 3 period of XTAL (or external clock)
   (d) Clear bit xt_clken1

CCSCTL2, Compact Clock System Control 2 Register

15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

7	6	5	4	3	2	1	0
Reserved	FSELx						
r-0	rw-0	rw-1	rw-0	rw-1	rw-0	rw-0	rw-0

Reserved	Bits 15 – 7	Reserved. Read back as 0.
FSELx	Bits 6 – 0	Frequency trimming of the HF-OSC Value HF-OSC 0000000 highest adjustable frequency … … 0101000 center frequency … … 1111111 lowest adjustable frequency

WDT_A Registers

WDT_A registers are described in the Watch Dog Timer (WDT_A) chapter of the MSP430x09x Family Users Guide (SLAU321).

PMM Registers

Compact System Control chapter of the MSP430x09x Family Users Guide (SLAU321).

Peripherals Continued

LDO1V

The Low Droop Out (LDO) is 1Volt (200µA max) voltage regulator that capable to drive 4 GPIO ports. The regulated 1V output is recommended to use for external RC charge, in order to minimize the effect of battery voltage changes between consecutive RC charges, durring Termistor and reference Resistor discharge time measurement.
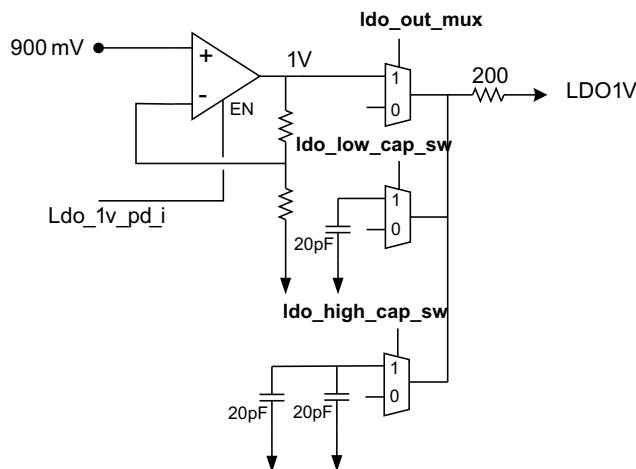
Figure 10. LDO1V Block Diagram

CP_1P8

The CP_1P8 is an internal charge pump module which is used to boost the battery voltage to ~2V. **The voltage boost is mandatory for the LCD operation.**

The CP_1P8 is sharing the CP_OSC with the LCD_CP as the reference clock for the boosting and also using the LF_clk for voltage feedback sensing.

The CP_1P8 requires 3 external capacitors for operation which are connected as following:
- 1nF capacitor connected between pads 41 (C1_out) and 40 (C1_in)
- 1nF capacitor connected between pads 39 (C2_out) and 38 (C2_in)
- 4.7nF capacitor connected between pads 37 and ground – load capacitor.

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The CP_1P8 has a valid signal which indicates when the voltage of the CP_1P8 has reached a 1.8V (Configurable) to allow operation of the LCD_CP or of other peripherals.
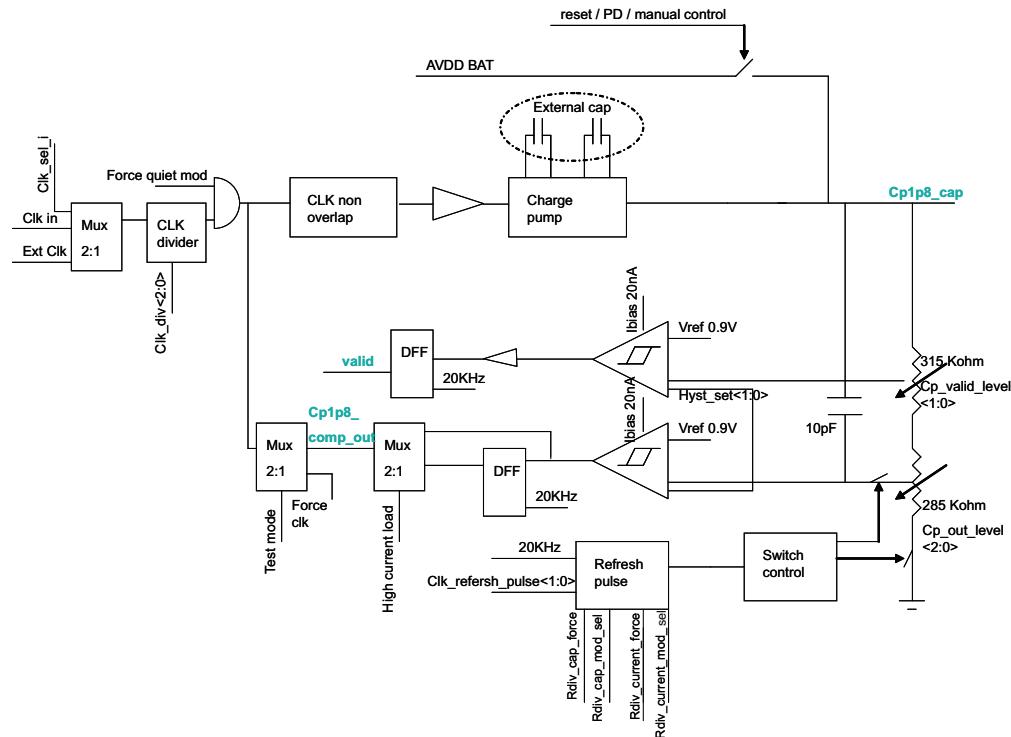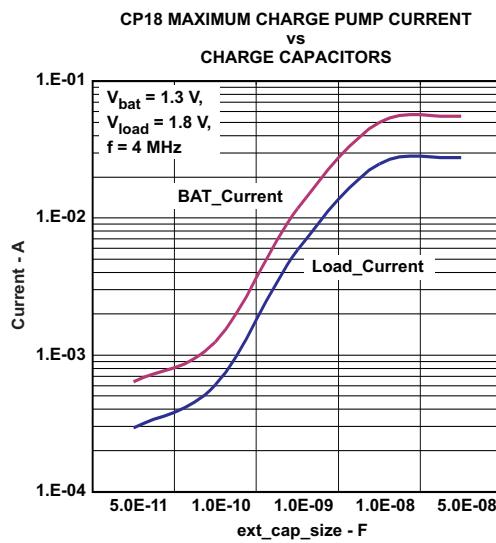
Figure 11. CP_1P8 Block Diagram

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PARAMETER MEASUREMENT INFORMATION
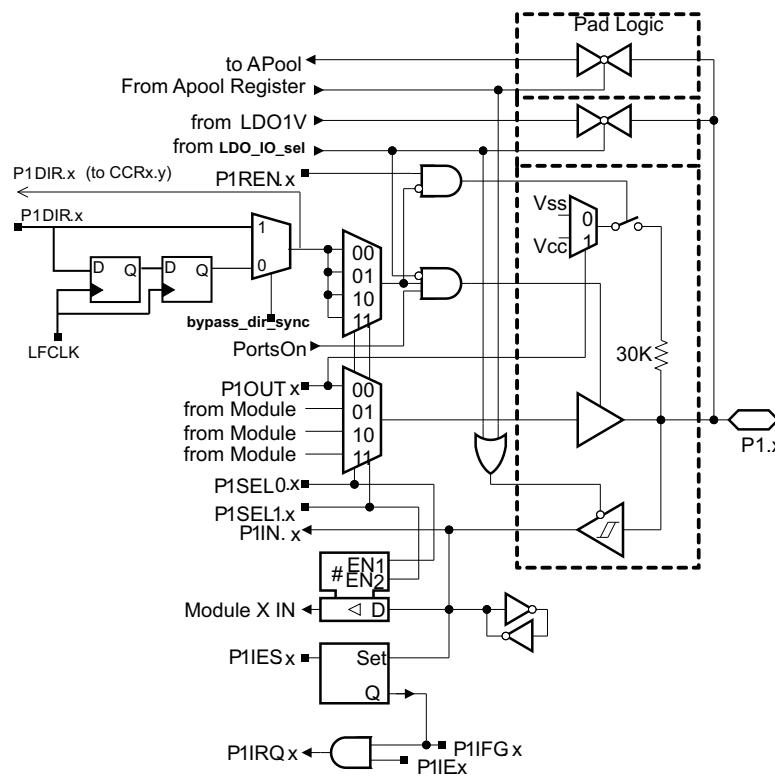
Figure 12. Port P1, P1.0, P1.1, P1.4 Input/Output

Table 13. Port P1 (P1.0, P1.1, P1.4) Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]				
			P1DIR.x	P1SEL1.x	P1SEL0.x	NSELx/PSELx	LDO_IO_sel <3-0>
P1.0/TA0.2/TA0.1/TA1.2/LDO1/TA0.CCI1B0/TA0.CCI2B0/A2	0	General-purpose digital I/O	In:0; Out:1	0	0	0	XXX0
		Timer0_A3 Out2 output	1	0	1	0	XXX0
		Timer1_A3 Out2 output	1	1	0	0	XXX0
		Timer0_A3 Out1 output	1	1	1	0	XXX0
		Analog in A2 or Atest1 Out – A Pool	X	X	X	2	XXXX
		LDO 1V Out	1	X	X	X	XXX1
P1.1/TA0.2/TA0.1/TA1.2/LDO1/TA0.CCI1A1/TA0.CCI2A1/A1	1	General-purpose digital I/O	In:0; Out:1	0	0	0	XX0X
		Timer0_A3 Out2 output	1	0	1	0	XX0X
		Timer1_A3 Out2 output	1	1	0	0	XX0X
		Timer0_A3 Out1 output	1	1	1	0	XX0X
		Analog in A1 – A-Pool	X	X	X	1	XXXX
		LDO 1V Out	1	X	X	X	XX1X
P1.4/TA0.2/TA0.1/TA1.2/LDO1/TA0.CCI1B1/TA0.CCI2B1/A0	4	General-purpose digital I/O	In:0; Out:1	0	0	0	X0XX
		Timer0_A3 Out2 output	1	0	1	0	X0XX
		Timer1_A3 Out2 output	1	1	0	0	X0XX
		Timer0_A3 Out1 output	1	1	1	0	X0XX
		Analog in A0 – A-Pool	X	X	X	0	XXXX
		LDO 1V Out	1	X	X	X	X1XX

(1) X = Don't care

Product Folder Link(s) :*AFE4110*
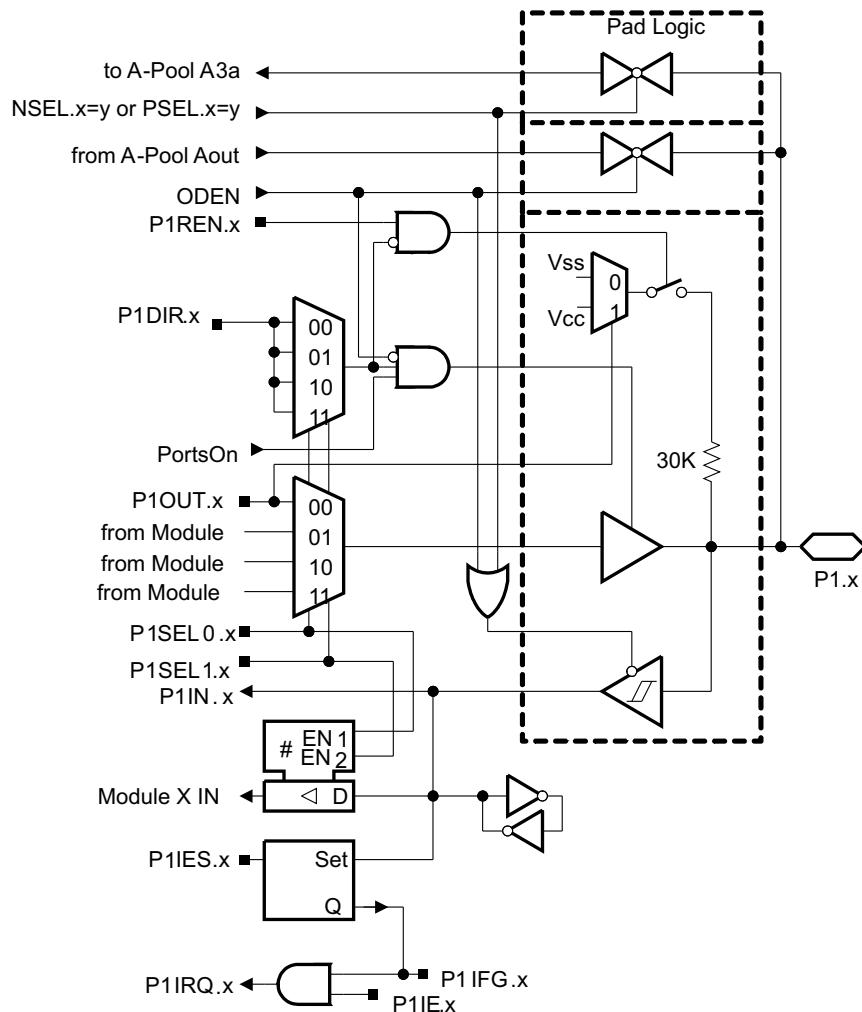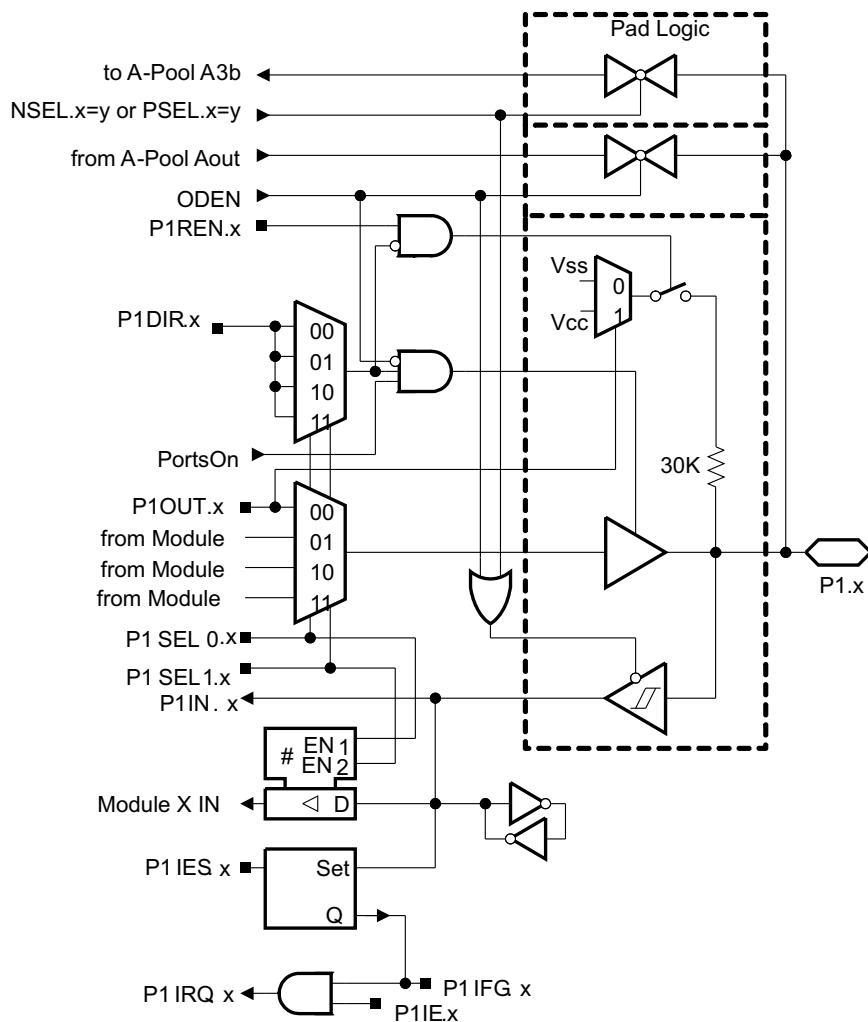
Figure 13. Port P1, P1.2 Input/Output

Table 14. Port P1 (P1.2) Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNAL [1]					
			P1DIR.x	P1SEL1.x	P1SEL0.x	NSELx/PSELx	ODEN	A3PSEL
P1.2/TA0.2/TA0.1/TA1.2/ AOUT/TA0.CCI1A2/TA0. CCI2A2/A3	2	General-purpose digital I/O	In:0; Out:1	0	0	≠3	0	X
		Timer0_A3 Out2	1	0	1	≠3	0	X
		Timer1_A3 Out2	1	1	0	≠3	0	X
		Timer0_A3 Out1	1	1	1	≠3	0	X
		Analog Input - A3a	X	X	X	3	0	0
		A-pool Aout	1	X	X	X	1	0

(1)   X = Don't care

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Figure 14. Port P1, P1.3 Input/Output

Table 15. Port P1 (P1.3) Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS [1]					
			P1DIR.x	P1SEL1.x	P1SEL0.x	NSELx/PSELx	VREFEN	A3PSEL
P1.3/TA0.2/TA0.1/TA1.2/ REFOUT/TA0.CCI1A3/T A0.CCI2A3/A3	3	General-purpose digital I/O	In:0; Out:1	0	0	≠2	0	X
		Timer0_A3 Out2	1	0	1	≠2	0	X
		Timer1_A3 Out1	1	1	0	≠2	0	X
		Timer0_A3 Out2	1	1	1	≠2	0	X
		Timer0_A3 CCR1A3						
		Timer0_A3 CCR2A3						
		A-Pool Analog Input - A3b	X	X	X	2	0	0
		A-Pool Vref	X	X	X	X	1	X

(1)   X = Don't care
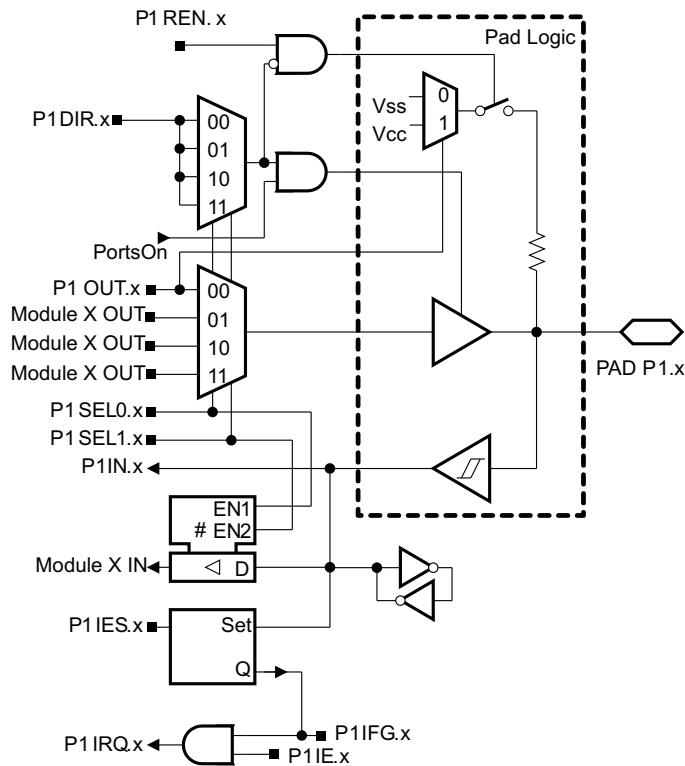
Figure 15. Port P1, P1.5 to P1.6 Input/Output

Table 16. Port P1 (P1.5 to P1.6) Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.5/TA0.2/TA1.2/TA0.1	5	General-purpose digital I/O	I:0; O:1	0	0
		Timer0_A3 Out2	1	0	1
		Timer1_A3 Out2	1	1	0
		Timer0_A3 Out1	1	1	1
		Timer0_A3 CCR1A3	0	≠0	≠0
P1.6/TA0.2/TA1.2/TA0.1	6	General-purpose digital I/O	I:0; O:1	0	0
		Timer0_A3 Out2	1	0	1
		Timer1_A3 Out2	1	1	0
		Timer1_A3 Out1	1	1	1
		Timer1_A2 CCR1B0	0	≠0	≠0

(1)   X = Don't care
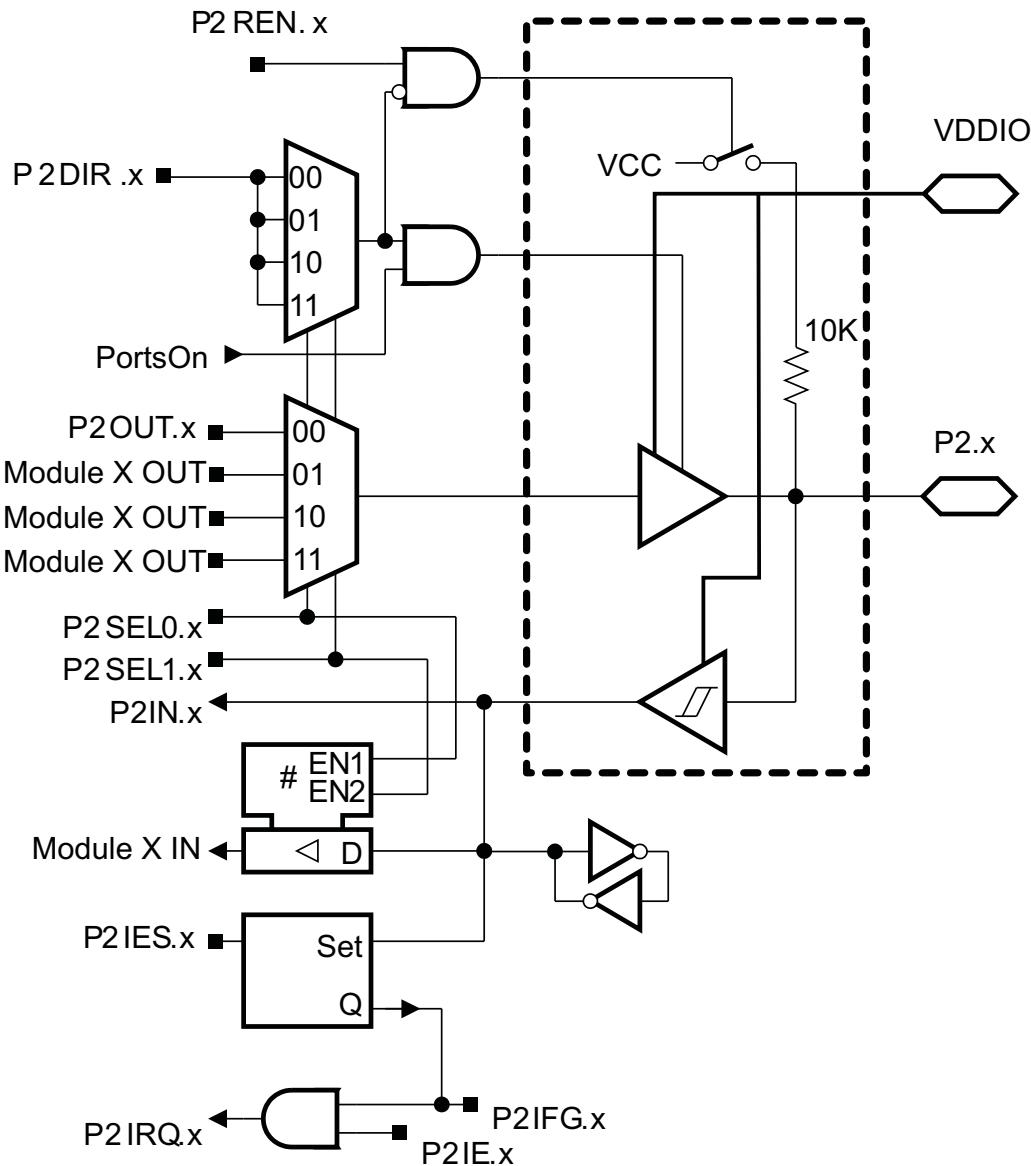
Figure 16. Port P2, P2.0, P2.1, P2.2 and P2.3, Input/Output

Table 17. Port P2 (P2.0 to P2.2) Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P2DIR.x	P2SEL1.x	P2SEL0.x	JTAG Mode
TCK/P2.0/TA1.2/TA1.1/CxOUT	0	General-purpose digital I/O	I:0; O:1	0	0	0
		Timer1_A3 Out1	1	0	1	0
		Timer1_A3 Out2	1	1	0	0
		CxOUT from Apool	1	1	1	0
		JTAG-TCK[2][3][4]	x	x	x	1

(1) X = Don't care
(2) JTAG signals TMS,TCK and TDI read as "1" when not configured as explicit JTAG terminals.
(3) JTAG overrides digital output control when configured as explicit JTAG terminals.
(4) JTAG function with enabled pull up resistors is default after power up.

Table 17. Port P2 (P2.0 to P2.2) Functions (continued)

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P2DIR.x	P2SEL1.x	P2SEL0.x	JTAG Mode
TMS/P2.1/ EXT_CLK/TA0.1/TA0.2	1	General-purpose digital I/O	I:0; O:1	0	0	0
		EXT_CLK Out	1	0	1	0
		Timer0_A3 Out1	1	1	0	0
		Timer0_A3 Out2	1	1	1	0
		JTAG-TMS [2][3][4]	x	x	x	1
TDI/P2.2/HF_CLK/CxOUT/TA1.0	2	General-purpose digital I/O	I:0; O:1	0	0	0
		HF_CLK Out	1	0	1	0
		Timer1_A3 Out0	1	1	0	0
		CxOUT from Apool	1	1	1	0
		JTAG-TDI [2][3][4]	X	X	X	1

Port P2, P2.3, Input/Output

Table 18. Port P2 (P2.3) Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
TDO/P2.3/LFCLK/TA0.2	3	General-purpose digital I/O	I:0; O:1	0	0
		LFCLK Out	1	0	1
		Timer0_A3 Out2	1	1	0
		JTAG-TDO [2][3]	1	1	1

(1)   X = Don't care
(2)   Configuring P2.3 to JTAG-TDO turns P2.0 to P2.3 also into JTAG functions
(3)   JTAG function with disabled pull up resistors is default after power up.
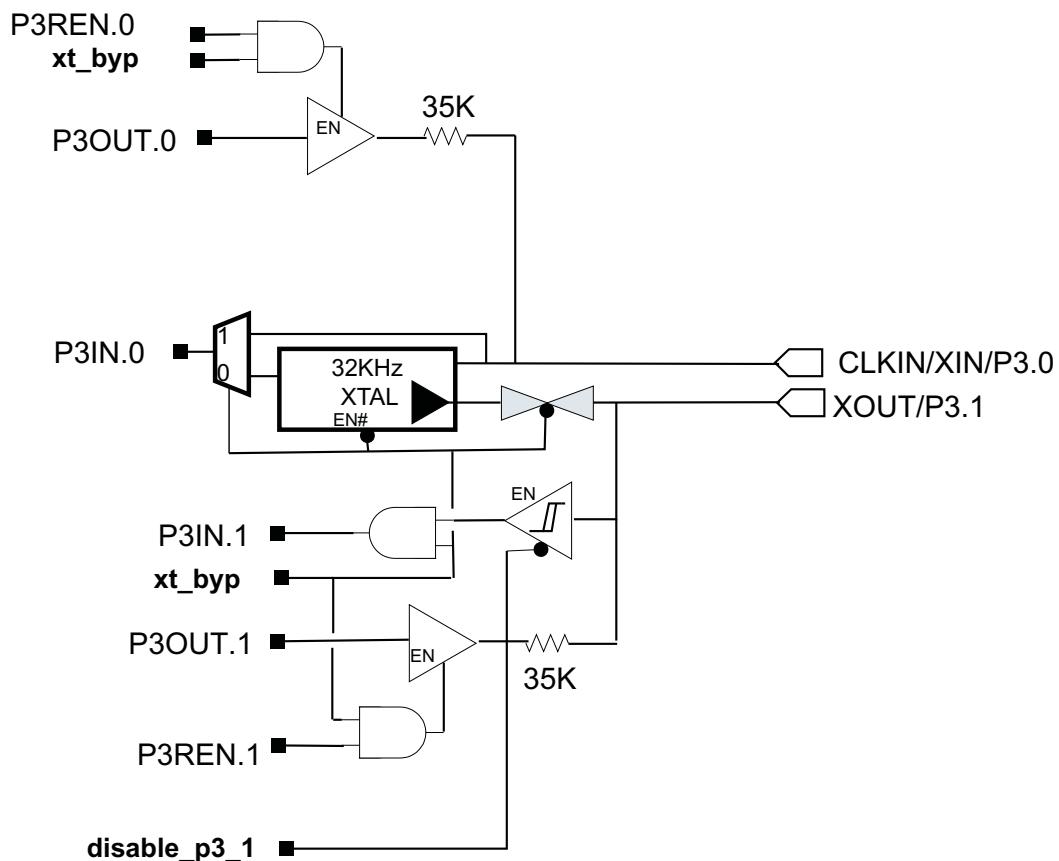
Figure 17. Port P3, P3.0, P3.1 Input/Output

Product Folder Link(s) :*AFE4110*
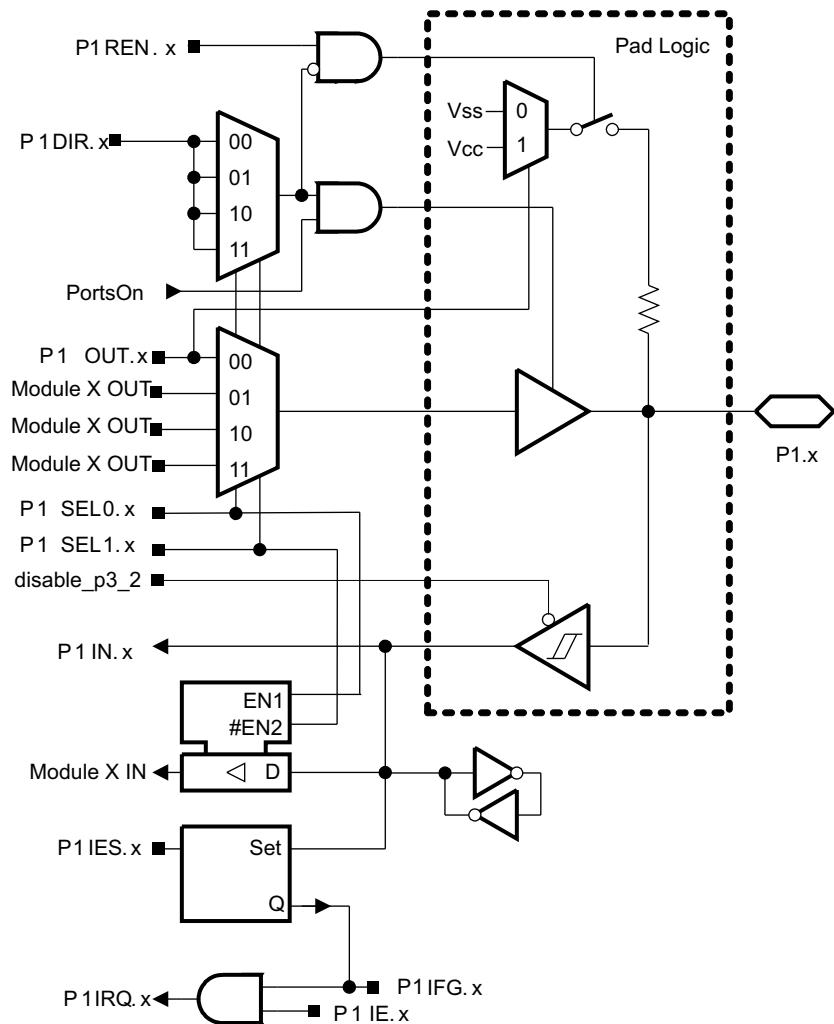
Figure 18. Port P3, P3.2, P3.4 Input/Output

Table 19. Port P3 (P3.2, P3.4, P3.5) Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P3DIR.x	P3SEL1.x	P3SEL0.x	disable_p3_x
P3.2/ TA0.1/TA1.1/TA1.0	2	General-purpose digital I/O	I:0; O:1	0	0	I:0; O:X
		Timer0_A3 Out1 output	1	0	1	X
		Timer1_A3 Out1 output	1	1	0	X
		Timer1_A3 Out0 output	1	1	1	X
P3.4/TA0.1/TA1.1/TA1.0/ TA1.CCI2A2	4	General-purpose digital I/O	I:0; O:1	0	0	In:0; Out:X
		Timer0_A3 Out1 output	1	0	1	X
		Timer1_A3 Out1 output	1	1	0	X
		Timer1_A3 Out0 output	1	1	1	X
		Timer1_A3 CCR2A2 capture: CCI2A2 input compare	X	X	X	0

(1) Don't Care

Table 19. Port P3 (P3.2, P3.4, P3.5) Functions (continued)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P3DIR.x	P3SEL1.x	P3SEL0.x	disable_p3_x
P3.5/TA0.1/TA1.1/TA1.0/ TA1.CCI2A3	5	General-purpose digital I/O	I:0; O:1	0	0	In:0; Out:X
		Timer0_A3 Out1 output	1	0	1	X
		Timer1_A3 Out1 output	1	1	0	X
		Timer1_A3 Out0 output	1	1	1	X
		Timer1_A3 CCR2A3 capture: CCI2A3 input, compare	X	X	X	0

Table 20. Port P3 (P3.6) Functions
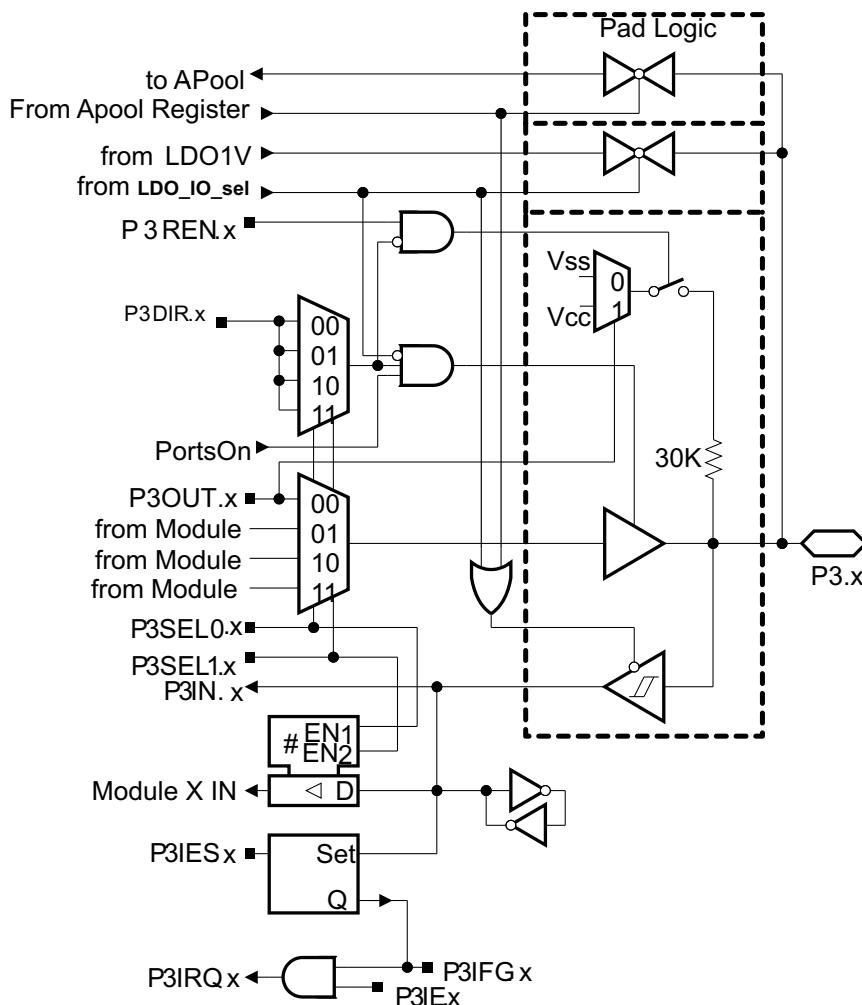
PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P3DIR.x	P3SEL1.x	P3SEL0.x	Sel_port3_6<1:0>
P3.6/TA0.0/TA0.1/TA0.2/TA0.0 N/ TA0.1N/TA0.2N/TA1.CCI1A3/ TA1.1/BOR/ACTSEN/LFOSC/C P18OK	6	10mA General-purpose digital I/O	In:0; Out:1	0	0	XX
		Timer0_A3 Out0 output	1	0	1	00
		Timer0_A3 Out1 output	1	0	1	01
		Timer0_A3 Out2 output	1	0	1	10
		Timer1_A3 Out1 output	1	0	1	11
		Timer0_A3 Out0# output	1	1	0	00
		Timer0_A3 Out1# output	1	1	0	01
		Timer0_A3 Out2# output	1	1	0	10
		Timer1_A3 Out1# output	1	1	0	11
		BOR Out	1	1	1	00
		Activation Sense Output	1	1	1	01
		LFCLK Out	1	1	1	10
		CP 1.8V OK Out	1	1	1	11
		Timer1_A3 CCR1A3 capture: CCI1A3 input, compare	X	X	X	XX

(1)   Don't Care

Table 21. Port P3 (P3.7) Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P3DIR.x	P3SEL1.x	P3SEL0.x	Sel_port3_7<1:0>
P3.7/TA0.0/TA0.1/TA0.2/TA0.0 N/TA0.1N/ TA0.2N/TA1.CCI2A1/HFOSC/L CDCPCLK/ LCDFCLK/1KCLK/LCDCMP	7	10mA General-purpose digital I/O	In:0; Out:1	0	0	XX
		Timer0_A3 Out0 output	1	0	1	00
		Timer0_A3 Out1 output	1	0	1	01
		Timer0_A3 Out2 output	1	0	1	10
		LCD Voltage Comparator Out	1	0	1	11
		Timer0_A3 Out0# output	1	1	0	00
		Timer0_A3 Out1# output	1	1	0	01
		Timer0_A3 Out2# output	1	1	0	10
		LCD Voltage Comparator Out#	1	1	0	11
		LCD Charge Pump Clock Out	1	1	1	00
		LCD Frame Clock Out	1	1	1	01
		HFCLK Out	1	1	1	10
		1Khz Activation Clock Out	1	1	1	11
		Timer1_A3 CCR2A1 capture: CCI2A1 input, compare				

(1)   Don't Care

Figure 19. Port P3, P3.3, Input/Output

Table 22. Port P3 (P3.3) Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]				
			P1DIR.x	P1SEL1.x	P1SEL0.x	NSELx/PSELx	LDO_IO_sel <3-0>
P3.3/ TA0.1/TA1.1/TA1.0/A0/LDO1	3	General-purpose digital I/O	In:0; Out:1	0	0	0	0XXX
		Timer0_A3 Out1 output	1	0	1	0	0XXX
		Timer1_A3 Out1 output	1	1	0	0	0XXX
		Timer1_A3 Out0 output	1	1	1	0	0XXX
		Analog input A0 – A-Pool	X	X	X	0	XXXX
		LDO 1V Out	1	X	X	X	1XXX

(1)   X = Don't care

Product Folder Link(s) :*AFE4110*
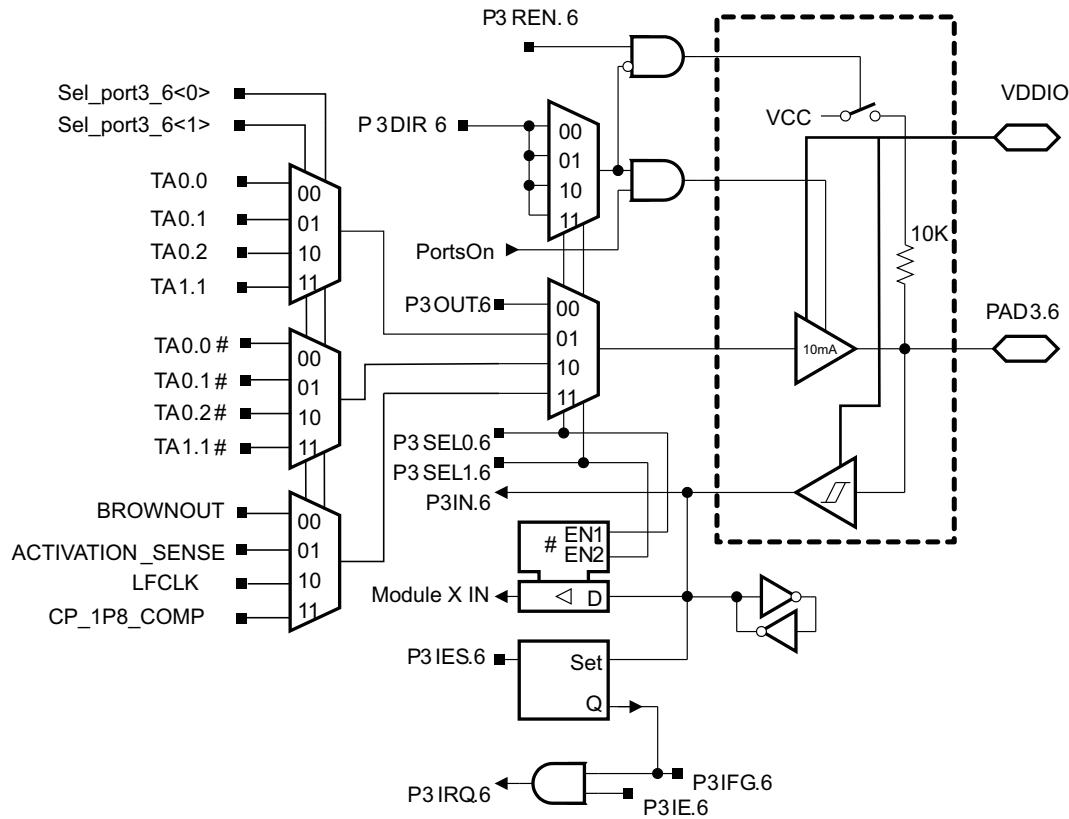
Figure 20. Port P3, P3.6, Input/Output
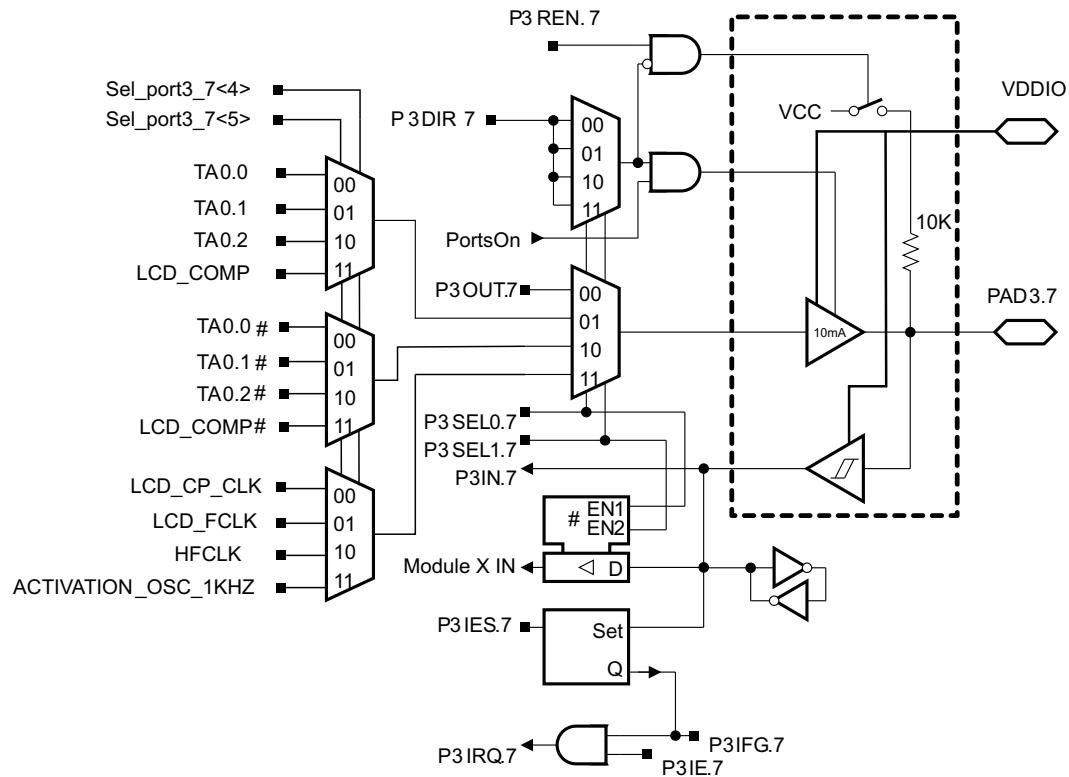
Figure 21. Port P3, P3.7, Input/Output
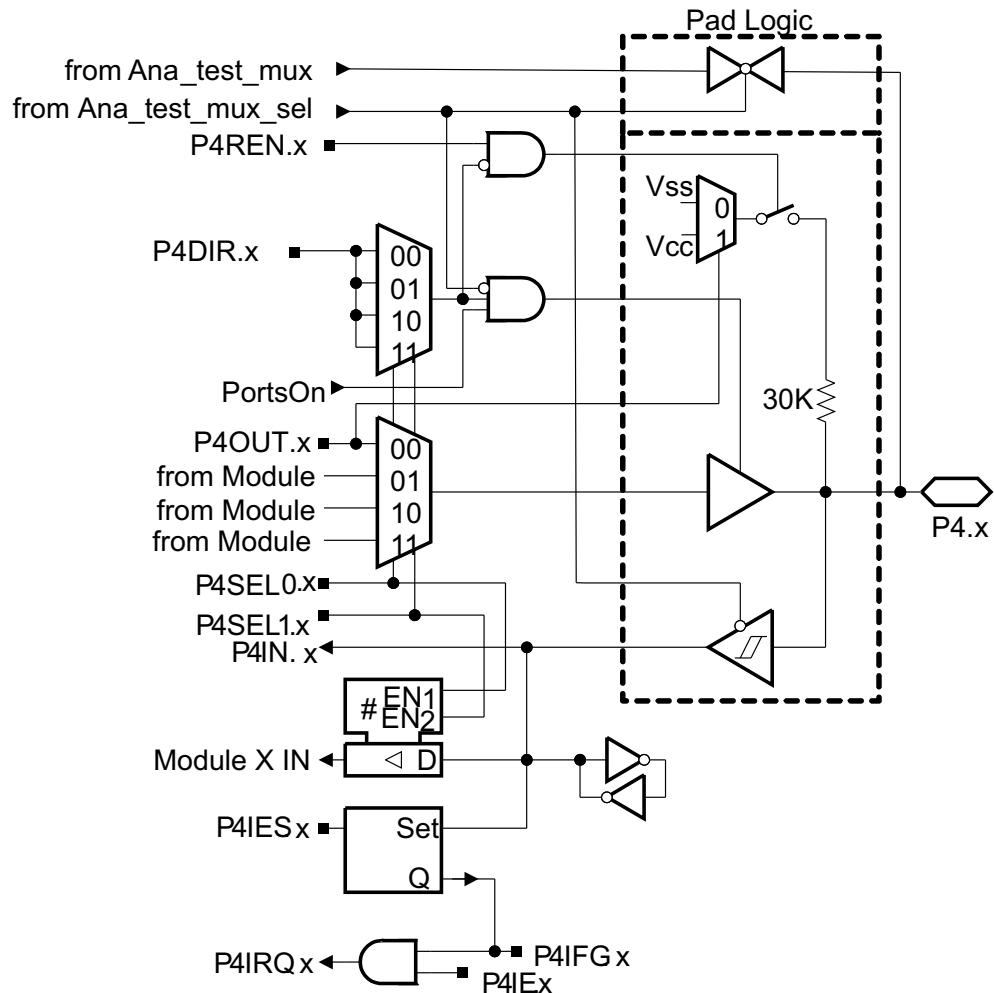
Figure 22. Port P4 (P4.0) Pin Input/Output

Table 23. Port P4 (P4.0) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P4DIR.x	P4SEL1.x	P4SEL0.x	Ana_test_mux<3:0>
P4.0/TA0.2/TA1.2/ACLK/ATEST/SPI_CS	0	General-purpose digital I/O	I:0; O:1	0	0	0
		Timer0_A3 Out2 output	1	0	1	0
		Timer1_A3 Out2 output	1	1	0	0
		ACLK Out	1	1	1	0
		Analog Test Multiplexer Out				/=0
		SPI Chip Select	1	0	0	0

(1) Don't Care
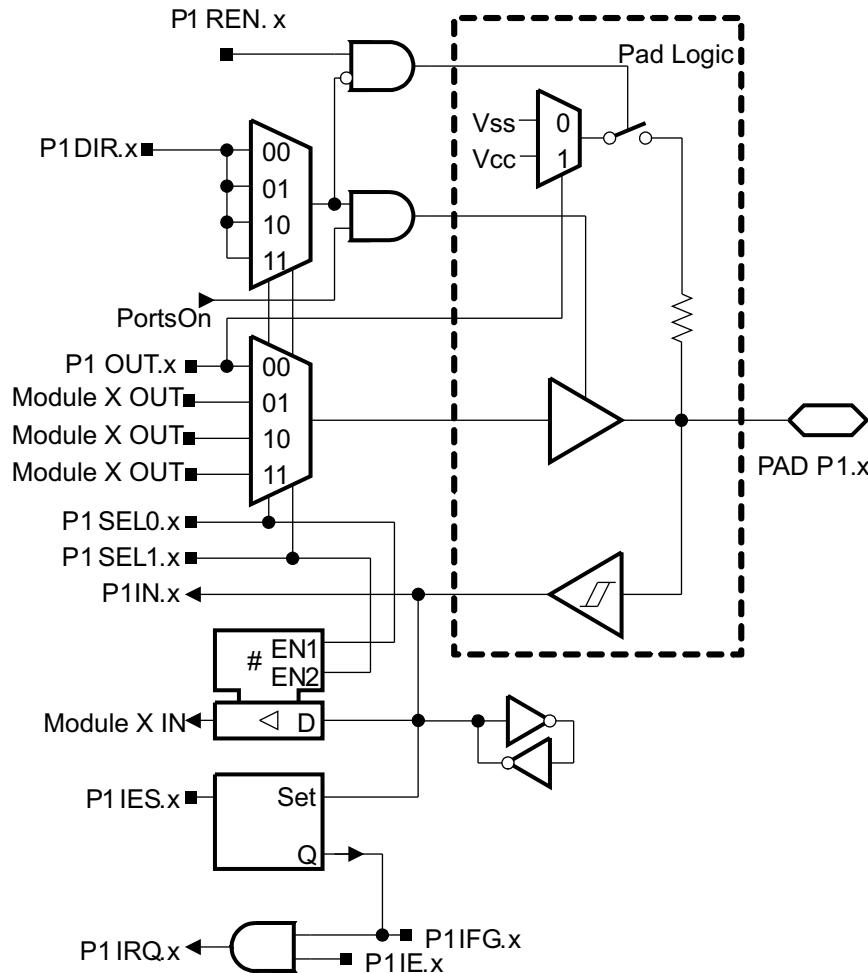
Figure 23. Port P4 (P4.1, P4.2, P4.3) Pin Input/Output

Table 24. Port P4 (P4.1, P4.2, P4.3) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.1/TA0.2/TA1.2/SMCLK/ SPI_MOSI	1	General-purpose digital I/O	I:0; O:1	0	0
		Timer0_A3 Out2 output	1	0	1
		Timer1_A3 Out2 output	1	1	0
		SMCLK Out	0	1	1
		SPI Serial In	0	0	0
P4.2/TA0.2/TA1.2/MCLK/ SPI_CLK	2	General-purpose digital I/O	I:0; O:1	0	0
		Timer0_A3 Out2 output	1	0	1
		Timer1_A3 Out2 output	1	1	0
		MCLK Out	0	1	1
		SPI Clock Out	1	0	0
P4.3/TA0.2/TA1.2/1KOSC/ SPI_MISO	3	General-purpose digital I/O	I:0; O:1	0	0
		Timer0_A3 Out2 output	1	0	1
		Timer1_A3 Out2 output	1	1	0
		1Khz Activation Oscillator Out	0	1	1
		SPI Serial Out	1	0	0

(1) Don't Care

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
AFE4110B000YS	ACTIVE	WAFERSALE	YS	0	1	TBD	Call TI	Call TI	

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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