STM32MP131C STM32MP131F

Arm® Cortex®-A7 up to 1 GHz, 1×ETH, 1×ADC, 24 timers, audio, crypto and adv. security

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

Core

- 32-bit Arm® Cortex®-A7
  - L1 32-Kbyte I / 32-Kbyte D
  - 128-Kbyte unified level 2 cache
  - Arm® NEON™ and Arm® TrustZone®

Memories

- External DDR memory up to 1 Gbyte
  - up to LPDDR2/LPDDR3-1066 16-bit
  - up to DDR3/DDR3L-1066 16-bit
- 168 Kbytes of internal SRAM: 128 Kbytes of AXI SYSRAM + 32 Kbytes of AHB SRAM and 8 Kbytes of SRAM in Backup domain
- Dual Quad-SPI memory interface
- Flexible external memory controller with up to 16-bit data bus: parallel interface to connect external ICs and SLC NAND memories with up to 8-bit ECC

Security/safety

- Secure boot, TrustZone® peripherals, 12 x tamper pins including 5 x active tampers
- Temperature, voltage, frequency and 32 kHz monitoring

Reset and power management

- 1.71 V to 3.6 V I/Os supply (5 V-tolerant I/Os)
- POR, PDR, PVD and BOR
- On-chip LDOs (USB 1.8 V, 1.1 V)
- Backup regulator (~0.9 V)
- Internal temperature sensors
- Low-power modes: Sleep, Stop, LPLV-Stop, LPLV-Stop2 and Standby

LFBGA289 (14 × 14mm)
Pitch 0.8 mm

TFBGA289 (9 × 9 mm)
TFBGA320 (11 × 11 mm)
min pitch 0.5 mm

- DDR retention in Standby mode
- Controls for PMIC companion chip

Clock management

- Internal oscillators: 64 MHz HSI oscillator, 4 MHz CSI oscillator, 32 kHz LSI oscillator
- External oscillators: 8-48 MHz HSE oscillator, 32.768 kHz LSE oscillator
- 4 × PLLs with fractional mode

General-purpose input/outputs

- Up to 135 secure I/O ports with interrupt capability
- Up to 6 wakeup

Interconnect matrix

- 2 bus matrices
  - 64-bit Arm® AMBA® AXI interconnect, up to 266 MHz
  - 32-bit Arm® AMBA® AHB interconnect, up to 209 MHz

4 DMA controllers to unload the CPU

- 56 physical channels in total
- 1 x high-speed general-purpose master direct memory access controller (MDMA)
- 3 × dual-port DMAs with FIFO and request router capabilities for optimal peripheral management

This is information on a product in full production. www.st.com

Up to 26 communication peripherals

- 5 × I^2C FM+ (1 Mbit/s, SMBus/PMBus™)
- 4 x UART + 4 x USART (12.5 Mbit/s, ISO7816 interface, LIN, IrDA, SPI)
- 5 × SPI (50 Mbit/s, including 4 with full-duplex I^2S audio class accuracy via internal audio PLL or external clock)(+2 QUADSPI + 4 with USART)
- 2 × SAI (stereo audio: I^2S, PDM, SPDIF Tx)
- SPDIF Rx with 4 inputs
- 2 × SDMMC up to 8 bits (SD/*e*•MMC™/SDIO)
- 2 × USB 2.0 high-speed Host
  - or 1 × USB 2.0 high-speed Host + 1 × USB 2.0 high-speed OTG simultaneously
- 1 x Ethernet MAC/GMAC
  - IEEE 1588v2 hardware, MII/RMII/RGMII

6 analog peripherals

- 1 × ADCs with 12-bit max. resolution up to 5 Msps
- 1 x temperature sensor
- 1 x digital filter for sigma-delta modulator (DFSDM) with 4 channels and 2 filters
- Internal or external ADC reference V_{REF+}

Up to 24 timers and 2 watchdogs

- 2 × 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- 2 × 16-bit advanced timers
- 10 × 16-bit general-purpose timers (including 2 basic timers without PWM)
- 5 × 16-bit low-power timers
- Secure RTC with sub-second accuracy and hardware calendar
- 4 Cortex®-A7 system timers (secure, non-secure, virtual, hypervisor)
- 2 × independent watchdogs

Hardware acceleration

- AES 128, 192, 256 DES/TDES
- AES 128, 256 with DPA protection
- PKA ECC/RSA with DPA protection
- AES 128 on-the-fly DRAM encryption and decryption
- HASH (SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-3), HMAC
- 1 x true random number generator (6 triple oscillators)
- 1 x CRC calculation unit

Debug mode

- Arm® CoreSight™ trace and debug: SWD and JTAG interfaces usable as GPIOs
- 4-Kbyte embedded trace buffer

3072-bit fuses including 96-bit unique ID, up to 1280 bits available for user and 256-bit HUK to protect AES 256 keys

All packages are ECOPACK2 compliant

Contents

1 Introduction 12

2 Description 13

3 Functional overview 19

3.1 Arm Cortex-A7 subsystem 19

3.1.1 Features 19

3.1.2 Overview 19

3.2 Memories 21

3.2.1 External SDRAM 21

3.2.2 Embedded SRAM 21

3.3 DDR3/DDR3L/LPDDR2/LPDDR3 controller (DDRCTRL) 21

3.4 TrustZone address space controller for DDR (TZC) 23

3.5 Boot modes 24

3.6 Power supply management 25

3.6.1 Power supply scheme 25

3.6.2 Power supply supervisor 26

3.7 Low-power strategy 27

3.8 Reset and clock controller (RCC) 27

3.8.1 Clock management 28

3.8.2 System reset sources 28

3.9 General-purpose input/outputs (GPIOs) 29

3.10 TrustZone protection controller (ETZPC) 29

3.11 Bus-interconnect matrix 30

3.12 DMA controllers 31

3.13 Extended interrupt and event controller (EXTI) 31

3.14 Cyclic redundancy check calculation unit (CRC) 31

3.15 Flexible memory controller (FMC) 32

3.16 Dual Quad-SPI memory interface (QUADSPI) 32

3.17 Analog-to-digital converters (ADC2) 32

3.18 Temperature sensor 33

3.19 Digital temperature sensor (DTS) 33

3.20 V_{BAT} operation 33
3.21 Voltage reference buffer (VREFBUF) 34
3.22 Digital filter for sigma-delta modulator (DFSDM) 34
3.23 True random number generator (RNG) 36
3.24 Cryptographic and hash processors (CRYP, SAES, PKA and HASH) . . . 36
3.25 Boot and security and OTP control (BSEC) 36
3.26 Timers and watchdogs 37
3.26.1 Advanced-control timers (TIM1, TIM8) 38
3.26.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM12, TIM13, TIM14, TIM15, TIM16, TIM17) 38
3.26.3 Basic timers (TIM6 and TIM7) 38
3.26.4 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5) 39
3.26.5 Independent watchdogs (IWDG1, IWDG2) 39
3.26.6 Generic timers (Cortex-A7 CNT) 39
3.27 System timer generation (STGEN) 39
3.28 Real-time clock (RTC) 40
3.29 Tamper and backup registers (TAMP) 41
3.30 Inter-integrated circuit interfaces (I2C1, I2C2, I2C3, I2C4, I2C5) 41
3.31 Universal synchronous asynchronous receiver transmitter (USART1, USART2, USART3, USART6 and UART4, UART5, UART7, UART8) 42
3.32 Serial peripheral interfaces (SPI1, SPI2, SPI3, SPI4, SPI5) – inter- integrated sound interfaces (I2S1, I2S2, I2S3, I2S4) 43
3.33 Serial audio interfaces (SAI1, SAI2) 43
3.34 SPDIF receiver interface (SPDIFRX) 44
3.35 Secure digital input/output MultiMediaCard interfaces (SDMMC1, SDMMC2) 44
3.36 Universal serial bus high-speed host (USBH) 46
3.37 USB on-the-go high-speed (OTG) 46
3.38 Gigabit Ethernet MAC interface (ETH1) 47
3.39 Debug infrastructure 48

4 Pinout, pin description and alternate functions 49

5 Memory mapping 95

6 Electrical characteristics 96

6.1 Parameter conditions 96

6.1.1 Minimum and maximum values 96

6.1.2 Typical values 96

6.1.3 Typical curves 96

6.1.4 Loading capacitor 96

6.1.5 Pin input voltage 96

6.1.6 Power supply scheme 97

6.1.7 Current consumption measurement 98

6.2 Absolute maximum ratings 98

6.3 Operating conditions 100

6.3.1 General operating conditions 100

6.3.2 Operating conditions at power-up / power-down 102

6.3.3 Embedded reset and power control block characteristics 104

6.3.4 Embedded reference voltage 107

6.3.5 Embedded regulators characteristics 108

6.3.6 Supply current characteristics 109

6.3.7 Wakeup time from low-power modes 117

6.3.8 External clock source characteristics 118

6.3.9 External clock source security characteristics 124

6.3.10 Internal clock source characteristics 124

6.3.11 PLL characteristics 126

6.3.12 PLL spread spectrum clock generation (SSCG) characteristics 131

6.3.13 Memory characteristics 133

6.3.14 EMC characteristics 134

6.3.15 Absolute maximum ratings (electrical sensitivity) 136

6.3.16 I/O current injection characteristics 137

6.3.17 I/O port characteristics 138

6.3.18 NRST pin characteristics 148

6.3.19 FMC characteristics 148

6.3.20 QUADSPI interface characteristics 165

6.3.21 Delay block (DLYB) characteristics 167

6.3.22 12-bit ADC characteristics 167

6.3.23 Voltage reference buffer characteristics 176

6.3.24 Temperature sensor characteristics 177

6.3.25 DTS characteristics 178

6.3.26 VBAT ADC monitoring characteristics and charging characteristics . . 179

6.3.27 Temperature and Backup domain supply thresholds monitoring 179
6.3.28 VDDCORE, VDDCPU, VDDQ_DDR monitoring characteristics 179
6.3.29 Voltage booster for analog switch 179
6.3.30 Compensation cell 180
6.3.31 Digital filter for sigma-delta modulators (DFSDM) characteristics 180
6.3.32 Timer characteristics 183
6.3.33 Communications interfaces 183
6.3.34 USART (SPI mode) interface characteristics 198
6.3.35 USB High-Speed PHY characteristics 199
6.3.36 JTAG/SWD interface characteristics 200

7 Package information 203
7.1 LFBGA289 package information (B0ED) 203
7.2 TFBGA289 package information (B0EB) 205
7.3 TFBGA320 package information (B0EC) 208
7.4 Thermal characteristics 210
7.4.1 Reference documents 210
7.5 Device marking 212

8 Ordering information 213

9 Important security notice 214

10 Revision history 215

List of tables

Table 1. STM32MP131C/F features and peripheral counts . . . 15
Table 2. Boot modes . . . 24
Table 3. System versus CPU power mode . . . 27
Table 4. Timer feature comparison . . . 37
Table 5. USART/UART features . . . 43
Table 6. Legend/abbreviations used in the pinout table . . . 52
Table 7. STM32MP131C/F ball definitions . . . 53
Table 8. Alternate function AF0 to AF7 . . . 73
Table 9. Alternate function AF8 to AF15 . . . 82
Table 10. Voltage characteristics . . . 98
Table 11. Current characteristics . . . 99
Table 12. Thermal characteristics . . . 100
Table 13. General operating conditions . . . 100
Table 14. Operating conditions at power-up / power-down . . . 102
Table 15. Embedded reset and power control block characteristics . . . 104
Table 16. Embedded reference voltage . . . 107
Table 17. Embedded reference voltage calibration value . . . 107
Table 18. REG1V1 embedded regulator (USB_PHY) characteristics . . . 108
Table 19. REG1V8 embedded regulator (USB_PHY) characteristics . . . 108
Table 20. Current consumption (IDDCORE) in Run mode . . . 110
Table 21. Current consumption (IDDCPU) in Run mode . . . 111
Table 22. Current consumption (IDD) in Run mode . . . 112
Table 23. Current consumption in Stop mode . . . 112
Table 24. Current consumption in LPLV-Stop mode . . . 113
Table 25. Current consumption in LPLV-Stop2 mode . . . 113
Table 26. Current consumption in Standby mode . . . 114
Table 27. Current consumption in VBAT mode . . . 115
Table 28. Low-power mode wakeup timings . . . 118
Table 29. Wakeup time using USART . . . 118
Table 30. High-speed external user clock characteristics (digital bypass) . . . 119
Table 31. High-speed external user clock characteristics (analog bypass) . . . 119
Table 32. Low-speed external user clock characteristics (analog bypass) . . . 120
Table 33. Low-speed external user clock characteristics (digital bypass) . . . 121
Table 34. 8-48 MHz HSE oscillator characteristics . . . 122
Table 35. Low-speed external user clock characteristics . . . 123
Table 36. High-speed external user clock security system (HSE CSS) . . . 124
Table 37. HSI oscillator characteristics . . . 124
Table 38. CSI oscillator characteristics . . . 125
Table 39. LSI oscillator characteristics . . . 126
Table 40. PLL1 characteristics . . . 126
Table 41. PLL2 characteristics . . . 128
Table 42. PLL3, PLL4 characteristics . . . 129
Table 43. USB_PLL characteristics . . . 131
Table 44. SSCG parameters constraint . . . 131
Table 45. OTP characteristics . . . 133

Table 46. DC specifications – DDR3 or DDR3L mode . . . 134
Table 47. DC specifications – LPDDR2 or LPDDR3 mode. . . . 134
Table 48. EMS characteristics . . . 135
Table 49. EMI characteristics for fHSE = 24 MHz and Fmpuss_ck = 650 MHz . . . 136
Table 50. EMI characteristics for fHSE = 24 MHz and Fmpuss_ck = 1 GHz . . . 136
Table 51. ESD absolute maximum ratings . . . 137
Table 52. Electrical sensitivities . . . 137
Table 53. I/O current injection susceptibility . . . 138
Table 54. I/O static characteristics . . . 138
Table 55. Output voltage characteristics for all I/Os except PC13, PC14, PC15, PI0 PI1, PI2, PI3 . 140
Table 56. Output voltage characteristics for PC13, PC14, PC15, PI0, PI1, PI2, PI3 . . . 141
Table 57. Output timing characteristics (HSLV OFF) . . . 142
Table 58. Output timing characteristics (HSLV ON, _h IO structure) . . . 144
Table 59. Output timing characteristics (HSLV OFF, _vh IO structure) . . . 145
Table 60. Output timing characteristics (HSLV ON, _vh IO structure) . . . 147
Table 61. NRST pin characteristics . . . 148
Table 62. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings . . . 150
Table 63. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings . . . 150
Table 64. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . 151
Table 65. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings. . . . 152
Table 66. Asynchronous multiplexed PSRAM/NOR read timings. . . . 153
Table 67. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings . . . 153
Table 68. Asynchronous multiplexed PSRAM/NOR write timings . . . 155
Table 69. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings . . . 155
Table 70. Synchronous multiplexed NOR/PSRAM read timings . . . 157
Table 71. Synchronous multiplexed PSRAM write timings. . . . 159
Table 72. Synchronous non-multiplexed NOR/PSRAM read timings . . . 161
Table 73. Synchronous non-multiplexed PSRAM write timings . . . 163
Table 74. Switching characteristics for NAND flash read cycles . . . 164
Table 75. Switching characteristics for NAND flash write cycles . . . 165
Table 76. QUADSPI characteristics in SDR mode . . . 165
Table 77. QUADSPI characteristics in DDR mode . . . 166
Table 78. Dynamics characteristics: Delay block characteristics . . . 167
Table 79. 12-bit ADC characteristics . . . 168
Table 80. Minimum sampling time vs RAIN (12-bit ADC). . . . 172
Table 81. 12-bit ADC accuracy. . . . 174
Table 82. VREFBUF characteristics . . . 176
Table 83. Temperature sensor characteristics . . . 177
Table 84. Temperature sensor calibration values. . . . 178
Table 85. DTS characteristics. . . . 178
Table 86. V_{BAT} ADC monitoring characteristics . . . 179
Table 87. V_{BAT} charging characteristics . . . 179
Table 88. V_{DDCORE}, V_{DDCPU}, V_{DDQ_DDR} monitoring characteristics . . . 179
Table 89. Voltage booster for analog switch characteristics. . . . 179
Table 90. Compensation cell characteristics . . . 180
Table 91. DFSDM measured timing . . . 180
Table 92. TIMx characteristics . . . 183
Table 93. LPTIMx characteristics . . . 183
Table 94. I2C analog filter characteristics. . . . 184
Table 95. I2C FM+ pin characteristics . . . 184
Table 96. SPI dynamic characteristics . . . 185
Table 97. I2S dynamic characteristics . . . 188

Table 98. SAI characteristics 190
Table 99. Dynamics characteristics: SD characteristics, VDD = 1.71 V to 3.6 V 192
Table 100. Dynamics characteristics: e•MMC characteristics VDD = 1.71 V to 3.6 V 193
Table 101. Dynamics characteristics: Ethernet MAC timings for MDIO/SMA. 195
Table 102. Dynamics characteristics: Ethernet MAC timings for RMII 195
Table 103. Dynamics characteristics: Ethernet MAC timings for MII 196
Table 104. Dynamics characteristics: Ethernet MAC signals for RGMII 197
Table 105. USART (SPI mode) characteristics 198
Table 106. USB High-Speed PHY characteristics 199
Table 107. Dynamics characteristics: JTAG characteristics. 201
Table 108. Dynamics characteristics: SWD characteristics 201
Table 109. LFBGA289 - Mechanical data. 204
Table 110. LFBGA289 - Recommended PCB design rules 205
Table 111. TFBGA289 - Mechanical data 206
Table 112. TFBGA289 - Recommended PCB design rules 207
Table 113. TFBGA320 - Mechanical data 208
Table 114. TFBGA320 - Recommended PCB design rules 209
Table 115. Thermal characteristics. 210
Table 116. STM32MP131C/F ordering information scheme. 213
Table 117. Document revision history 215

List of figures

Figure 1. STM32MP131C/F block diagram . . . 18
Figure 2. Power-up/down sequence . . . 26
Figure 3. STM32MP131C/F bus matrix . . . 30
Figure 4. Voltage reference buffer . . . 34
Figure 5. STM32MP131C/F LFBGA289 ballout . . . 49
Figure 6. STM32MP131C/F TFBGA289 ballout . . . 50
Figure 7. STM32MP131C/F TFBGA320 ballout . . . 51
Figure 8. Pin loading conditions . . . 96
Figure 9. Pin input voltage . . . 96
Figure 10. Power supply scheme . . . 97
Figure 11. Current consumption measurement scheme . . . 98
Figure 12. VDDCORE / VDDCPU rise time from reset . . . 103
Figure 13. VDDCORE / VDDCPU rise time from LPLV-Stop . . . 104
Figure 14. High-speed external clock source AC timing diagram (digital bypass) . . . 119
Figure 15. High-speed external clock source AC timing diagram (analog bypass) . . . 120
Figure 16. Low-speed external clock source AC timing diagram (analog bypass) . . . 121
Figure 17. AC timing diagram for low-speed external square clock source . . . 121
Figure 18. Typical application with a 24 MHz crystal . . . 123
Figure 19. Typical application with a 32.768 kHz crystal . . . 124
Figure 20. PLL output clock waveforms in center spread mode . . . 133
Figure 21. PLL output clock waveforms in down spread mode . . . 133
Figure 22. VIL/VIH for FT I/Os . . . 139
Figure 23. Recommended NRST pin protection . . . 148
Figure 24. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . 149
Figure 25. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . 151
Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms . . . 152
Figure 27. Asynchronous multiplexed PSRAM/NOR write waveforms . . . 154
Figure 28. Synchronous multiplexed NOR/PSRAM read timings . . . 156
Figure 29. Synchronous multiplexed PSRAM write timings . . . 158
Figure 30. Synchronous non-multiplexed NOR/PSRAM read timings . . . 160
Figure 31. Synchronous non-multiplexed PSRAM write timings . . . 162
Figure 32. NAND controller waveforms for read access . . . 164
Figure 33. NAND controller waveforms for write access . . . 164
Figure 34. QUADSPI timing diagram - SDR mode . . . 166
Figure 35. QUADSPI timing diagram - DDR mode . . . 166
Figure 36. ADC accuracy characteristics . . . 174
Figure 37. Typical connection diagram using the ADC with FT/TT pins featuring analog switch function . . . 175
Figure 38. Channel transceiver timing diagrams . . . 182
Figure 39. SPI timing diagram - slave mode and CPHA = 0 . . . 186
Figure 40. SPI timing diagram - slave mode and CPHA = 1(1) . . . 187
Figure 41. SPI timing diagram - master mode(1) . . . 187
Figure 42. I2S slave timing diagram (Philips protocol)(1) . . . 189
Figure 43. I2S master timing diagram (Philips protocol)(1) . . . 189
Figure 44. SAI master timing waveforms . . . 191
Figure 45. SAI slave timing waveforms . . . 192
Figure 46. SD high-speed mode . . . 194
Figure 47. SD default mode . . . 194

Figure 48. SDMMC DDR mode 194
Figure 49. Ethernet MDIO/SMA timing diagram 195
Figure 50. Ethernet RMII timing diagram 196
Figure 51. Ethernet MII timing diagram 197
Figure 52. Ethernet RGMII timing diagram 197
Figure 53. USART timing diagram in SPI master mode. 199
Figure 54. USART timing diagram in SPI slave mode 199
Figure 55. JTAG timing diagram 202
Figure 56. SWD timing 202
Figure 57. LFBGA289 - Outline 203
Figure 58. LFBGA289 - Recommended footprint 204
Figure 59. TFBGA289 - Outline 205
Figure 60. TFBGA289 - Recommended footprint 207
Figure 61. TFBGA320 - Outline 208
Figure 62. TFBGA320 - Recommended footprint 209

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32MP131C/F microprocessors.

This document should be read in conjunction with the STM32MP131 reference manual (RM0475), available from the STMicroelectronics website *www.st.com*.

For information on the Arm®[a] Cortex®-A7, refer to the Cortex®-A7 *Technical Reference Manuals*.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32MP131x/3x/5x device errata (ES0539), available on the STMicroelectronics website *www.st.com*.

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2 Description

The STM32MP131C/F devices are based on the high-performance Arm® Cortex®-A7 32-bit RISC core operating at up to 1 GHz. The Cortex®-A7 processor includes a 32-Kbyte L1 instruction cache, a 32-Kbyte L1 data cache and a 128-Kbyte level2 cache. The Cortex®-A7 processor is a very energy-efficient application processor designed to provide rich performance in high-end wearables, and other low-power embedded and consumer applications. It provides up to 20 % more single thread performance than the Cortex®-A5 and provides similar performance to the Cortex®-A9.

The Cortex®-A7 incorporates all features of the high-performance Cortex®-A15 and Cortex®-A17 processors, including virtualization support in hardware, NEON™, and 128-bit AMBA®4 AXI bus interface.

The STM32MP131C/F devices provide an external SDRAM interface supporting external memories up to 8-Gbit density (1 Gbyte), 16-bit LPDDR2/LPDDR3 or DDR3/DDR3L up to 533 MHz.

The STM32MP131C/F devices incorporate high-speed embedded memories with 168 Kbytes of internal SRAM (including 128 Kbytes of AXI SYSRAM, two banks of 8 Kbytes and one bank of 16 Kbytes securable AHB SRAM, and 8 Kbytes of SRAM in Backup domain), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, and a 64-bit multi-layer AXI interconnect supporting internal and external memories access.

All the devices offer one ADC, a low-power secured RTC, ten general-purpose 16-bit timers, two 32-bit timers, two PWM timers for motor control, five low-power timers, a secured true random number generator (RNG), and an advanced secured cryptographic acceleration cell. The devices support two digital filters for external sigma-delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals:
  - Five I^2Cs
  - Four USARTs and four UARTs
  - Five SPIs, four I^2Ss full-duplex master/slave. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
  - Two SAI serial audio interfaces (up to four audio channels each)
  - One SPDIF Rx interface
  - Two SDMMC interfaces
  - A USB OTG high-speed controller
  - A USB high-speed Host controller with two ports and two high-speed phys. The second high-speed phy can be shared between the USB high-speed Host and the USB OTG high-speed.
  - One Gigabit Ethernet interface
- Advanced peripherals including:
  - A flexible memory control (FMC) interface
  - A Quad-SPI flash memory interface

Refer to *Table 1: STM32MP131C/F features and peripheral counts* for the specificity for each package type.

A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32MP131C/F devices are proposed in three packages ranging from 289 to 320 balls, with pitch 0.5 mm to 0.8 mm.

These features make the STM32MP131C/F suitable for a wide range of consumer, industrial, point of sales, white goods and medical applications.

Figure 1 shows the general block diagram of the device family.

Table 1. STM32MP131C/F features and peripheral counts

Features			STM32MP131CAE STM32MP131FAE	STM32MP131CAG STM32MP131FAG	STM32MP131CAF STM32MP131FAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Package		Body size (mm)	14x14	9x9	11x11	-
		Pitch (mm)	0.8	0.5	0.5	
		Ball size (mm)	0.40	0.30	0.30	
		Thickness (mm)	< 1.4	< 1.2	< 1.2	
		Ball count	289	289	320	
CPU			Cortex-A7 FPU Neon TrustZone			-
		Caches size	32-Kbyte L1 data cache			
			32-Kbyte L1 instruction cache			
			128-Kbyte L2 unified coherent cache			
		Frequency	STM32MP131C: 650 MHz STM32MP131F: 1 GHz			
ROM			128 Kbytes (secure)			-
Embedded SRAM		System RAM	128 Kbytes (securable)			168 Kbytes
		Backup	8 Kbytes (securable, tamper protected)			
		AHB SRAM	32 Kbytes			
SDRAM			Securable and on-the-fly data encryption			-
	LPDDR2/3	16-bit 533 MHz	Up to 1 Gbyte, single rank			
	DDR3/3L	16-bit 533 MHz				
Backup registers			128 bytes (32x32-bit, securable, tamper protected)			-
Timers	Advanced	16 bits	2			24 timers
	General purpose	16 bits	8 (6 securable)			
		32 bits	2			
	Basic	16 bits	2			
	Low power	16 bits	5 (2 securable)			
	A7 timers	64 bits	4 (secure, non-secure, virtual, hypervisor)			
	RTC/AWU		1 (securable)			

Table 1. STM32MP131C/F features and peripheral counts (continued)

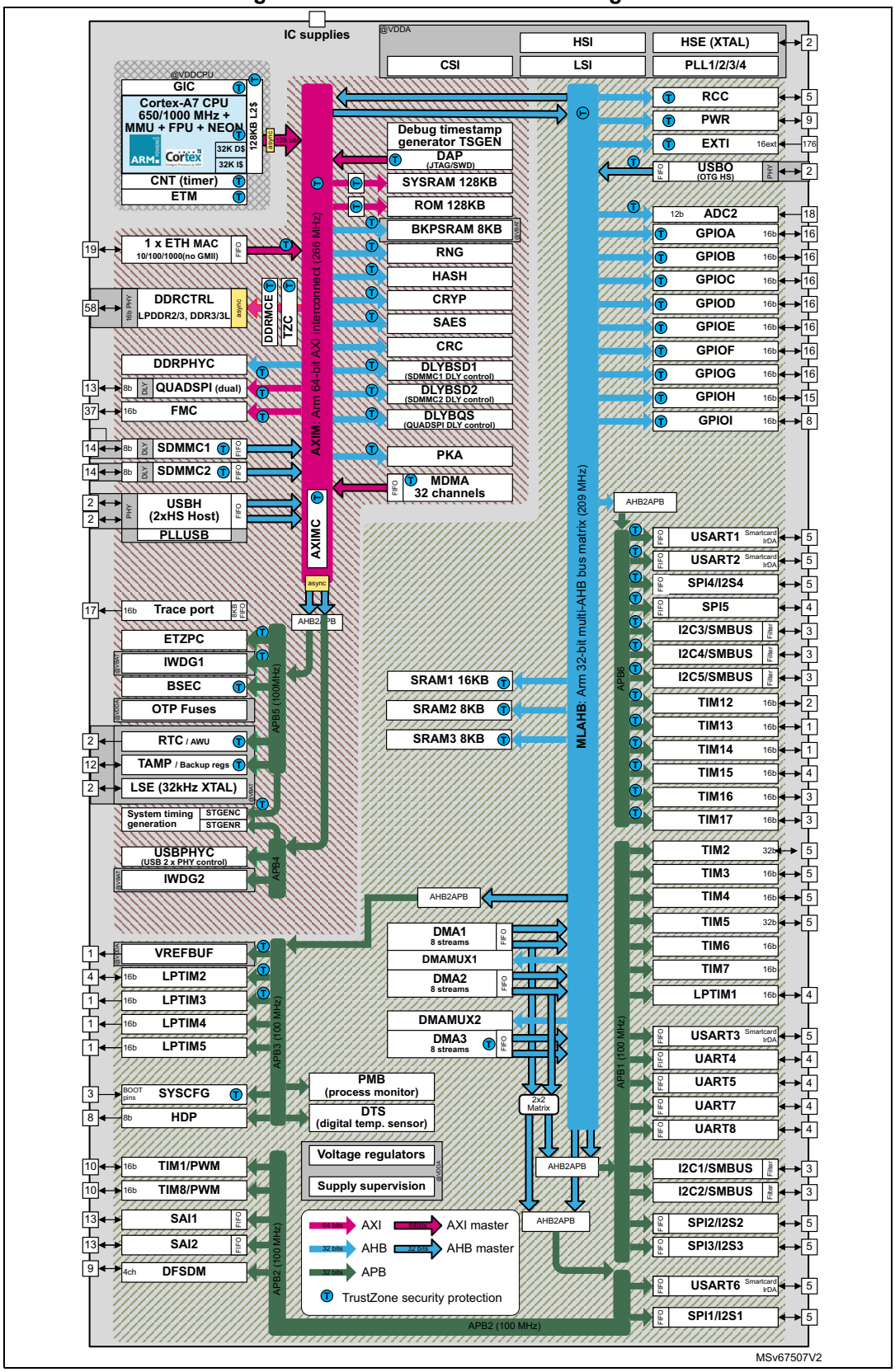
Features			STM32MP131CAE STM32MP131FAE	STM32MP131CAG STM32MP131FAG	STM32MP131CAF STM32MP131FAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Watchdogs			2 (independent, independent secure)			-
Communication peripherals	SPI		5 (2 securable)			-
		Having I2S	4			
	I2C (with SMB/PMB support)		5 (3 securable)			
	USART (smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)		4 + 4 (including 2 securable USART), some can be a boot source			Boot
	SAI		2 (up to 4 audio channels), with I2S master/slave, PCM input, SPDIF-TX			-
	USB	EHCI/OHCI Host	2 ports			-
			Embedded HSPHY with BCD			
		OTG HS	Embedded HS PHY with BCD (securable), can be a boot source			Boot
		Embedded PHYs	2 × HS shared between Host and OTG			-
	SPDIFRX		4 inputs			-
SDMMC (SD, SDIO, *e*•MMC)			2 (8 + 8 bits) (securable), *e*•MMC or SD can be a boot source 2 optional independant power supplies for SD card interfaces			Boot
QUADSPI			1 (dual-quad) (securable), can be a boot source			Boot (1)
FMC	Parallel address/data 8/16-bit		4 × CS, up to 4 × 64 Mbyte			-
	Parallel AD-mux 8/16-bit					
	NAND 8/16-bit		Yes, 2× CS, SLC, BCH4/8, can be a boot source			Boot
10/100M/Gigabit Ethernet			1 x (MII, RMI, RGMII) with PTP and EEE (securable)			-
DMA			3 instances (1 secure), 33-channel MDMA			-
Cryptography			PKA (with DPA protection), DES, TDES, AES (with DPA protection) (all securable)			-
Hash			SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-3, HMAC (securable)			-
True random number generator			True-RNG (securable)			-
Fuses (one-time programmable)			3072 effective bits (secure, 1280 bits available for the user)			-

Table 1. STM32MP131C/F features and peripheral counts (continued)

Features		STM32MP131CAE STM32MP131FAE	STM32MP131CAG STM32MP131FAG	STM32MP131CAF STM32MP131FAF	Miscellaneous
		LFBGA289	TFBGA289	TFBGA320	
GPIOs with interrupt (total count)		135[2]			-
	Securable GPIOs	All			
	Wakeup pins	6			
	Tamper pins (active tamper)	12 (5)			
DFSDM		4 input channels with 2 filters			-
Up to 12-bit synchronized ADC		1 (up to 5 Msps on 12-bit each) (securable)			-
	12-bit ADC channels in total[3]	ADC2: 18 channels including 6x internal, 12 channels available for user including 6x differential			
Internal ADC VREF		1.65 V, 1.8 V, 2.048 V, 2.5 V or VREF+ input			-
	VREF+ input pin	Yes			

1. QUADSPI may boot either from dedicated GPIOs or using some FMC Nand8 boot GPIOs (PD4, PD1, PD5, PE9, PD11, PD15 (see *Table 7: STM32MP131C/F ball definitions*).
2. This total GPIO count includes four JTAG GPIOs and three BOOT GPIOs with limited usage (may conflict with external device connection during boundary scan or boot).
3. In addition, there are also internal channels:
   - ADC2 internal channels: temperature, internal voltage reference, V_{DDCORE}, V_{DDCPU}, V_{DDQ_DDR}, V_{BAT} / 4.

Figure 1. STM32MP131C/F block diagram



3 Functional overview

3.1 Arm Cortex-A7 subsystem

3.1.1 Features

- ARMv7-A architecture
- 32-Kbyte L1 instruction cache
- 32-Kbyte L1 data cache
- 128-Kbyte level2 cache
- Arm + Thumb®-2 instruction set
- Arm TrustZone security technology
- Arm NEON advanced SIMD
- DSP and SIMD extensions
- VFPv4 floating-point
- Hardware virtualization support
- Embedded trace module (ETM)
- Integrated generic interrupt controller (GIC) with 160 shared peripheral interrupts
- Integrated generic timer (CNT)

3.1.2 Overview

The Cortex-A7 processor is a very energy-efficient applications processor designed to provide rich performance in high-end wearables, and other low-power embedded and consumer applications. It provides up to 20 % more single thread performance than the Cortex-A5 and provides similar performance than the Cortex-A9.

The Cortex-A7 incorporates all features of the high-performance Cortex-A15 and Cortex-A17 processors, including virtualization support in hardware, NEON, and 128-bit AMBA 4 AXI bus interface.

The Cortex-A7 processor builds on the energy-efficient 8-stage pipeline of the Cortex-A5 processor. It also benefits from an integrated L2 cache designed for low-power, with lower transaction latencies and improved OS support for cache maintenance. On top of this, there is improved branch prediction and improved memory system performance, with 64-bit load-store path, 128-bit AMBA 4 AXI buses and increased TLB size (256 entry, up from 128 entry for Cortex-A9 and Cortex-A5), increasing performance for large workloads such as web browsing.

Thumb-2 technology

Delivers the peak performance of traditional Arm code while also providing up to a 30 % reduction in memory requirement for instructions storage.

TrustZone technology

Ensures reliable implementation of security applications ranging from digital rights management to electronic payment. Broad support from technology and industry partners.

NEON

NEON technology can accelerate multimedia and signal processing algorithms such as video encode/decode, 2D/3D graphics, gaming, audio and speech processing, image processing, telephony, and sound synthesis. The Cortex-A7 provides an engine that offers both the performance and functionality of the Cortex-A7 floating-point unit (FPU) and an implementation of the NEON advanced SIMD instruction set for further acceleration of media and signal processing functions. The NEON extends the Cortex-A7 processor FPU to provide a quad-MAC and additional 64-bit and 128-bit register set supporting a rich set of SIMD operations over 8-, 16- and 32-bit integer and 32-bit floating-point data quantities.

Hardware virtualization

Highly efficient hardware support for data management and arbitration, whereby multiple software environments and their applications are able to simultaneously access the system capabilities. This enables the realization of devices that are robust, with virtual environments that are well isolated from each other.

Optimized L1 caches

Performance and power optimized L1 caches combine minimal access latency techniques to maximize performance and minimize power consumption.

Integrated L2 cache controller

Provides low-latency and high-bandwidth access to cached memory in high-frequency, or to reduce the power consumption associated with off-chip memory access.

Cortex-A7 floating-point unit (FPU)

The FPU provides high-performance single and double precision floating-point instructions compatible with the Arm VFPv4 architecture that is software compatible with previous generations of Arm floating-point coprocessor.

Snoop control unit (SCU)

The SCU is responsible for managing the interconnect, arbitration, communication, cache to cache and system memory transfers, cache coherence and other capabilities for the processor.

This system coherence also reduces software complexity involved in maintaining software coherence within each OS driver.

Generic interrupt controller (GIC)

Implementing the standardized and architected interrupt controller, the GIC provides a rich and flexible approach to inter-processor communication and the routing and prioritization of system interrupts.

Supporting up to 192 independent interrupts, under software control, hardware prioritized, and routed between the operating system and TrustZone software management layer.

This routing flexibility and the support for virtualization of interrupts into the operating system, provides one of the key features required to enhance the capabilities of a solution utilizing a hypervisor.

3.2 Memories

3.2.1 External SDRAM

The STM32MP131C/F devices embed a controller for external SDRAM that supports the following:

- LPDDR2 or LPDDR3, 16-bit data, up to 1 Gbyte, up to 533 MHz clock
- DDR3 or DDR3L, 16-bit data, up to 1 Gbyte, up to 533 MHz clock

3.2.2 Embedded SRAM

All devices feature:

- SYSRAM: 128 Kbytes (with programmable size secure zone)
- AHB SRAM: 32 Kbytes (securable)
- BKPSRAM (backup SRAM): 8 Kbytes

  The content of this area is protected against possible unwanted write accesses, and can be retained in Standby or V_{BAT} mode.

  BKPSRAM can be defined (in ETZPC) as accessible by secure software only.

3.3 DDR3/DDR3L/LPDDR2/LPDDR3 controller (DDRCTRL)

DDRCTRL combined with DDRPHYC provides a complete memory interface solution for DDR memory subsystem.

- One 64-bit AMBA 4 AXI ports interface (XPI)
- AXI clock asynchronous to the controller
- DDR memory cypher engine (DDRMCE) featuring AES-128 DDR on-the-fly write encryption/read decryption.
- Supported standards:
  - JEDEC DDR3 SDRAM specification, JESD79-3E for DDR3/3L with 16-bit interface
  - JEDEC LPDDR2 SDRAM specification, JESD209-2E for LPDDR2 with 16-bit interface
  - JEDEC LPDDR3 SDRAM specification, JESD209-3B for LPDDR3 with 16-bit interface
- Advanced scheduler and SDRAM command generator
- Programmable full data width (16-bit) or half data width (8-bit)
- Advanced QoS support with three traffic class on read and two traffic classes on write
- Options to avoid starvation of lower priority traffic
- Guaranteed coherency for write-after-read (WAR) and read-after-write (RAW) on AXI ports
- Programmable support for burst length options (4, 8, 16)
- Write combine to allow multiple writes to the same address to be combined into a single write
- Single rank configuration

- Support of automatic SDRAM power-down entry and exit caused by lack of transaction arrival for programmable time
- Support of automatic clock stop (LPDDR2/3) entry and exit caused by lack of transaction arrival
- Support of automatic low-power mode operation caused by lack of transaction arrival for programmable time via hardware low-power interface
- Programmable paging policy
- Support of automatic or under software control self-refresh entry and exit
- Support of deep power-down entry and exit under software control (LPDDR2 and LPDDR3)
- Support of explicit SDRAM mode register updates under software control
- Flexible address mapper logic to allow application specific mapping of row, column, bank bits
- User-selectable refresh control options
- DDRPERFM associated block to help for performance monitoring and tuning

DDRCTRL and DDRPHYC can be defined (in ETZPC) as accessible by secure software only.

The DDRMCE (DDR memory cypher engine) main features are listed below:

- AXI system bus master/slave interfaces (64-bit)
- In-line encryption (for writes) and decryption (for reads), based on embedded firewall programming
- Two encryption mode per region (maximum one region): no encryption (bypass mode), block cipher mode
- Start and end of regions defined with 64-Kbyte granularity
- Default filtering (region 0): any access granted
- Region access filtering: none
  - Supported block cipher: AES
  - Supported chaining mode
- Block mode with AES cipher is compatible with ECB mode specified in NIST FIPS publication 197 advanced encryption standard (AES), with an associated key derivation function based on Keccak-400 algorithm published on https://keccak.team website.
- One set of write-only and lockable master key registers
- AHB configuration port, privileged aware

3.4 TrustZone address space controller for DDR (TZC)

TZC is used to filter read/write accesses to DDR controller according to TrustZone rights and according to non-secure master (NSAID) on up to nine programmable regions:

- Configuration supported by trusted software only
- One filter unit
- Nine regions:
  - Region 0 is always enabled and covers the whole address range.
  - Regions 1 to 8 have programmable base-/end-address and can be assigned to any one or both filters.
- Secure and non-secure access permissions programmed per region
- Non-secure accesses filtered according to NSAID
- Regions controlled by same filter must not overlap
- Fail modes with error and/or interrupt
- Acceptance capability = 256
- Gate keeper logic to enable and disable of each filter
- Speculative accesses

3.5 Boot modes

At startup, the boot source used by the internal boot ROM is selected by the BOOT pin and OTP bytes.

Table 2. Boot modes

BOOT2	BOOT1	BOOT0	Initial boot mode	Comments
0	0	0	UART and USB(1)	Wait incoming connection on: – USART3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins(2)
0	0	1	Serial NOR flash(3)	Serial NOR flash on QUADSPI(5)
0	1	0	*e*•MMC(3)	*e*•MMC on SDMMC2 (default)(5)(6)
0	1	1	NAND flash(3)	SLC NAND flash on FMC
1	0	0	Development boot (no flash memory boot)	Used to get debug access without boot from flash memory(4)
1	0	1	SD card(3)	SD card on SDMMC1 (default)(5)(6)
1	1	0	UART and USB(1)(3)	Wait incoming connection on: – USART3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins(2)
1	1	1	Serial NAND flash(3)	Serial NAND flash on QUADSPI(5)

1. Can be disabled by OTP settings.
2. USB requires HSE clock/crystal (see AN5474 for supported frequencies with and without OTP settings).
3. Boot source can be changed by OTP settings (for example initial boot on SD card, then *e*•MMC with OTP settings).
4. Cortex®-A7 core in infinite loop toggling PA13.
5. Default pins can be altered by OTP.
6. Alternatively, another SDMMC interface than this default can be selected by OTP.

Although low level boot is done using internal clocks, ST supplied software packages as well as major external interfaces such as DDR, USB (but not limited to) require a crystal or an external oscillator to be connected on HSE pins.

See RM0475 “STM32MP13xx advanced Arm®-based 32-bit MPUs” or AN5474 "Getting started with STM32MP13xx lines hardware development" for constraints and recommendations regarding HSE pins connection and supported frequencies.

3.6 Power supply management

3.6.1 Power supply scheme

- V_{DD} is the main supply for I/Os and internal part kept powered during Standby mode. Useful voltage range is 1.71 V to 3.6 V (1.8 V, 2.5 V, 3.0 V or 3.3 V typ.)
  - V_{DD_PLL} and V_{DD_ANA} must be star-connected to V_{DD}.
- V_{DDCPU} is the Cortex-A7 CPU dedicated voltage supply, whose value depends on the desired CPU frequency. 1.22 V to 1.38 V in run mode. V_{DD} must be present before V_{DDCPU}.
- V_{DDCORE} is the main digital voltage and is usually shutdown during Standby mode. Voltage range is 1.21 V to 1.29 V in run mode. V_{DD} must be present before V_{DDCORE}.
- The VBAT pin can be connected to the external battery (1.6 V < V_{BAT} < 3.6 V). If no external battery is used, this pin must be connected to V_{DD}.
- V_{DDA} is the analog (ADC/VREF), supply voltage (1.62 V to 3.6 V). Using the internal V_{REF+} requires V_{DDA} equal to or higher than V_{REF+} + 0.3 V.
- The VDDA1V8_REG pin is the output of the internal regulator, connected internally to USB PHY and USB PLL. The internal V_{DDA1V8_REG} regulator is enabled by default and can be controlled by software. It is always shut down during Standby mode.

  The specific BYPASS_REG1V8 pin must never be left floating. It must be connected either to V_{SS} or to V_{DD} to activate or deactivate the voltage regulator. When V_{DD} = 1.8 V, BYPASS_REG1V8 should be set.
- VDDA1V1_REG pin is the output of the internal regulator, connected internally to USB PHY. The internal V_{DDA1V1_REG} regulator is enabled by default and can be controlled by software. It is always shut down during Standby mode.
- V_{DD3V3_USBHS} is the USB high-speed supply. Voltage range is 3.07 V to 3.6 V.

Caution: V_{DD3V3_USBHS} must not be present unless V_{DDA1V8_REG} is present, otherwise permanent damage may occur on the STM32MP131C/F. This must be ensured by PMIC ranking order or with external component in case of discrete component power supply implementation.

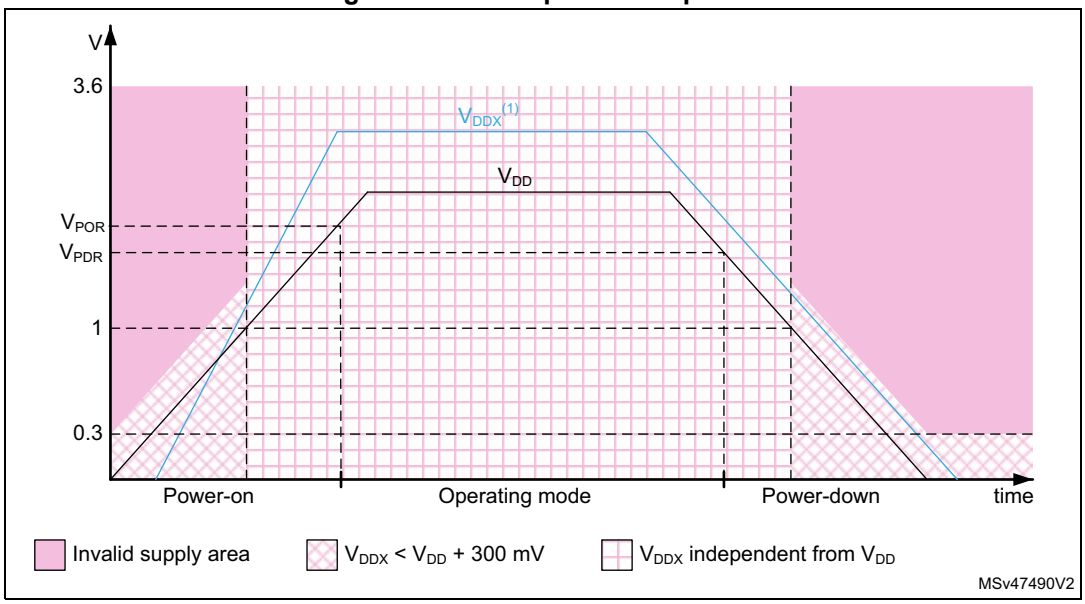
- V_{DDSD1} and V_{DDSD2} are respectively SDMMC1 and SDMMC2 SD card power supplies to support ultra-high-speed mode.
- V_{DDQ_DDR} is the DDR IO supply.
  - 1.425 V to 1.575 V for interfacing DDR3 memories (1.5 V typ.)
  - 1.283 V to 1.45 V for interfacing DDR3L memories (1.35 V typ.)
  - 1.14 V to 1.3 V for interfacing LPDDR2 or LPDDR3 memories (1.2 V typ.)

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDCORE}, V_{DDCPU}, V_{DDSD1}, V_{DDSD2}, V_{DDA}, V_{DDA1V8_REG}, V_{DDA1V1_REG}, V_{DD3V3_USBHS}, V_{DDQ_DDR}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the STM32MP131C/F remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power- down transient phase.

Figure 2. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDCORE}, V_{DDCPU}, V_{DDSD1}, V_{DDSD2}, V_{DDA}, V_{DDA1V8_REG}, V_{DDA1V1_REG}, V_{DD3V3_USBHS}, V_{DDQ_DDR}.

3.6.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in reset mode when V_{DD} is below this threshold,
- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.
- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.
- Power-on reset V_{DDCORE} (POR_VDDCORE)

  The POR_VDDCORE supervisor monitors V_{DDCORE} power supply and compares it to a fixed threshold. The V_{DDCORE} domain remains in reset mode when V_{DDCORE} is below this threshold.
- Power-down reset V_{DDCORE} (PDR_VDDCORE)

  The PDR_VDDCORE supervisor monitors V_{DDCORE} power supply. A V_{DDCORE} domain reset is generated when V_{DDCORE} drops below a fixed threshold.
- Power-on-reset V_{DDCPU} (POR_VDDCPU)

  The POR_VDDCPU supervisor monitors V_{DDCPU} power supply and compares it to a fixed threshold. The V_{DDCPU} domain remains in reset mode when V_{DDCORE} is below this threshold.

Note: The PDR_ON pin is reserved for STMicroelectronics production tests and must always be connected to V_{DD} in an application.

3.7 Low-power strategy

There are several ways to reduce power consumption on STM32MP131C/F:

- Decrease dynamic power consumption by slowing down the CPU clocks and/or the bus matrix clocks and/or controlling individual peripheral clocks.
- Save power consumption when the CPU is IDLE, by selecting among the available low-power modes according to the user application needs. This allows the best compromise between short startup time, low-power consumption, as well as available wakeup sources, to be achieved.
- Use the DVFS (dynamic voltage and frequency scaling) operating points that directly controls the CPU clock frequency as well as the V_{DDCPU} output supply.

The operating modes allow the control of the clock distribution to the different system parts and the power of the system. The system operation mode is driven by the MPU sub-system.

The MPU sub-system low-power modes are listed below:

- CSleep: The CPU clocks are stopped and the peripheral(s) clock operates as previously set in the RCC (reset and clock controller).
- CStop: The CPU peripheral(s) clocks are stopped.
- CStandby: V_{DDCPU} OFF

CSleep and CStop low-power modes are entered by the CPU when executing the WFI (wait for interrupt) or WFE (wait for event) instructions.

The system operating modes available are the followings:

- Run (system at its full performance, V_{DDCORE}, V_{DDCPU} and clocks ON)
- Stop (clocks OFF)
- LP-Stop (clocks OFF)
- LPLV-Stop (clocks OFF, V_{DDCORE} and V_{DDCPU} supply level may be lowered)
- LPLV-Stop2 (V_{DDCPU} OFF, V_{DDCORE} lowered, and clocks OFF)
- Standby (V_{DDCPU}, V_{DDCORE}, and clocks OFF)

Table 3. System versus CPU power mode

System power mode	CPU
Run mode	CRun or CSleep
Stop mode LP-Stop mode LPLV-Stop mode LPLV-Stop2 mode	CStop or CStandby
Standby mode	CStandby

3.8 Reset and clock controller (RCC)

The clock and reset controller manages the generation of all the clocks, as well as the clock gating, and the control of the system and peripheral resets.RCC provides a high flexibility in the choice of clock sources and allows application of clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with

two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baudrate.

3.8.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, three internal oscillators with fast startup time and four PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock (1 % accuracy)
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - 8-48 MHz HSE clock
  - 32.768 kHz LSE clock

The RCC provides four PLLs:

- PLL1 dedicated to the CPU clocking
- PLL2 providing:
  - clocks for the AXI-SS (including APB4, APB5, AHB5 and AHB6 bridges)
  - clocks for the DDR interface
- PLL3 providing:
  - clocks for the multi-Layer AHB and peripheral bus matrix (including the APB1, APB2, APB3, APB6, AHB1, AHB2, and AHB4)
  - kernel clocks for peripherals
- PLL4 dedicated to the generation of the kernel clocks for various peripherals

The system starts on the HSI clock. The user application can then select the clock configuration.

3.8.2 System reset sources

The power-on reset initializes all registers except for the debug, a part of the RCC, a part of the RTC and power controller status registers, as well as the Backup power domain.

An application reset is generated from one of the following sources:

- a reset from NRST pad
- a reset from POR and PDR signal (generally called power-on reset)
- a reset from BOR (generally called brownout)
- a reset from the independent watchdog 1
- a reset from the independent watchdog 2
- a software system reset from the Cortex-A7 (CPU)
- a failure on HSE, when the clock security system feature is activated

A system reset is generated from one of the following sources:

- an application reset
- a reset from POR_VDDCORE signal
- an exit from Standby mode to Run mode

A MPU processor reset is generated from one of the following sources:

- a system reset
- every time the MPU exits CStandby
- a software MPU reset from the Cortex-A7 (CPU)

3.9 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

All GPIO pins can be individually set as secure, which means that software accesses to these GPIOs and associated peripherals defined as secure are restricted to secure software running on the CPU.

3.10 TrustZone protection controller (ETZPC)

ETZPC is used to configure TrustZone security of bus masters and slaves with programmable-security attributes (securable resources). For instance:

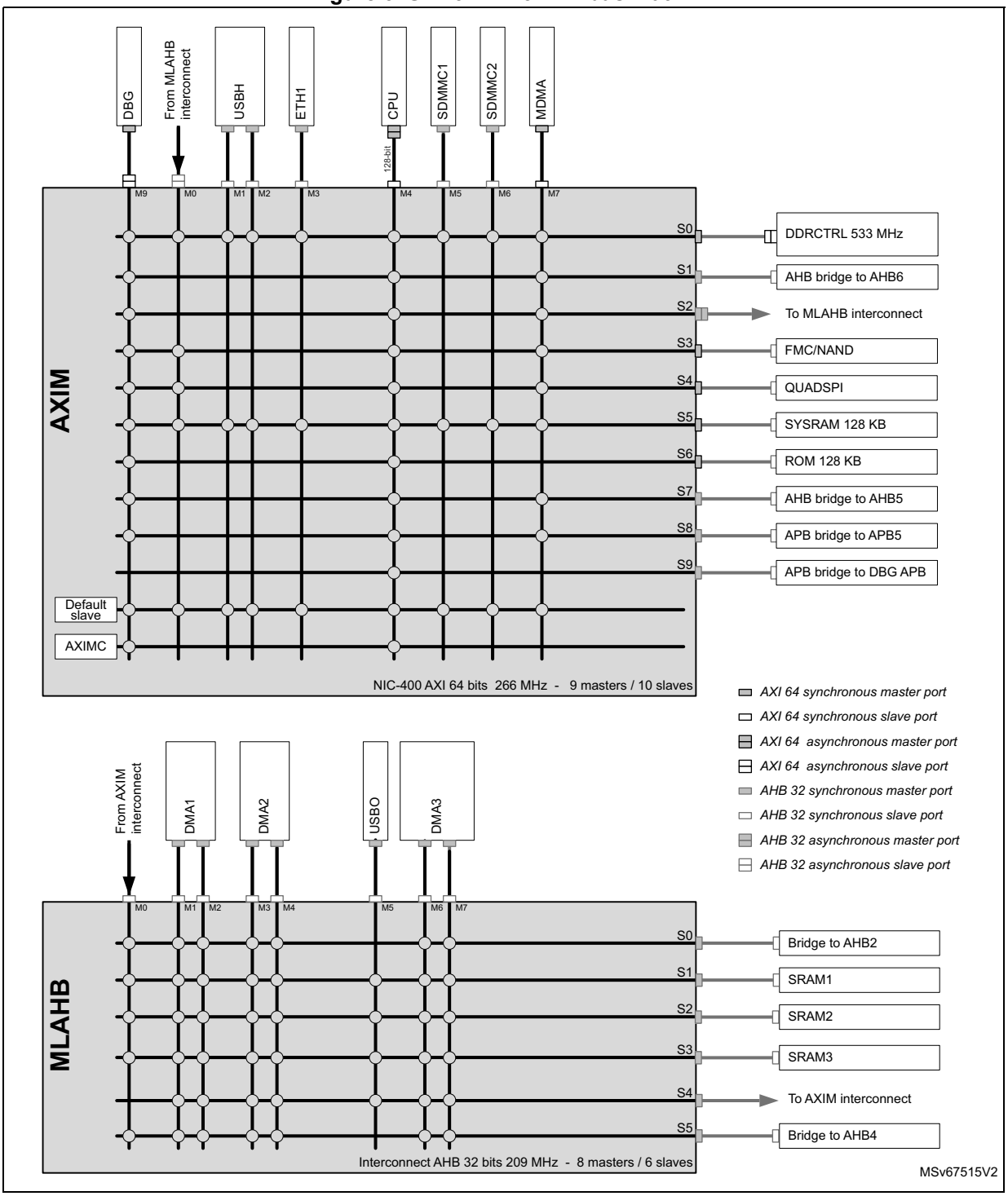
- On-chip SYSRAM secure region size can be programmed.
- AHB and APB peripherals can be made secure or non-secure.
- AHB SRAM can be made secure or non-secure.

Note: By default, SYSRAM, AHB SRAMs and securable peripherals are set to secure access only, so, not accessible by non-secure masters such as DMA1/DMA2.

3.11 Bus-interconnect matrix

The devices feature an AXI bus matrix, one main AHB bus matrix and bus bridges that allow bus masters to be interconnected with bus slaves (see the figure below, the dots represent the enabled master/slave connections).

Figure 3. STM32MP131C/F bus matrix



3.12 DMA controllers

The devices feature the following DMA modules to unload CPU activity:

- a master direct memory access (MDMA)

  The MDMA is a high-speed DMA controller, that is in charge of all types of memory transfers (peripheral-to-memory, memory-to-memory, memory-to-peripheral), without any CPU action. It features a master AXI interface.

  The MDMA is able to interface with the other DMA controllers to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

  Each of the 32 channels can perform block transfers, repeated block transfers and linked list transfers.

  The MDMA can be set to make secure transfers to secured memories.
- three DMA controllers (not secure DMA1 and DMA2, plus secure DMA3)

  Each controller has a dual-port AHB, for a total of 16 non-secure and eight secure DMA channels to perform FIFO-based block transfers.

Two DMAMUX units multiplex and route the DMA peripheral requests to the three DMA controllers, with high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output triggers or DMA events.

DMAMUX1 maps DMA requests from non-secure peripherals to DMA1 and DMA2 channels. DMAMUX2 maps DMA requests from secure peripherals to DMA3 channels.

3.13 Extended interrupt and event controller (EXTI)

The extended interrupt and event controller (EXTI) manages the CPU and system wakeup through configurable and direct event inputs. EXTI provides wakeup requests to the power control, and generates an interrupt request to the GIC, and events to the CPU event input.

The EXTI wakeup requests allow the system to be woken up from Stop mode, and the CPU to be woken up from CStop and CStandby modes.

The interrupt request and event request generation can also be used in Run mode.

The EXTI also includes the EXTI IOport selection.

Each interrupt or event can be set as secure in order to restrict access to secure software only.

3.14 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps computing a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.15 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - NOR flash memory
  - Static or pseudo-static random access memory (SRAM, PSRAM)
  - NAND flash memory with 4-bit/8-bit BCH hardware ECC
- 8-,16-bit data bus width
- Independent chip-select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

The FMC configuration registers can be made secure.

3.16 Dual Quad-SPI memory interface (QUADSPI)

The QUADSPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers.
- Status-polling mode: the external flash memory status register is periodically read and an interrupt can be generated in case of flag setting.
- Memory-mapped mode: the external flash memory is mapped to the address space and is seen by the system as if it was an internal memory.

Both throughput and capacity can be increased two-fold using dual-flash mode, where two Quad-SPI flash memories are accessed simultaneously.

QUADSPI is coupled with a delay block (DLYBQS) allowing the support of external data frequency above 100 MHz.

The QUADSPI configuration registers can be secure, as well as its delay block.

3.17 Analog-to-digital converters (ADC2)

The devices embed one analog-to-digital converter, whose resolution can be configured to 12-, 10-, 8- or 6-bit. The ADC has up to 12 external channels, performing conversions in the single-shot or scan mode. In scan mode, the automatic conversion is performed on a selected group of analog inputs.

The ADC has securable bus interface.

The ADC can be served by a DMA controller, thus allowing the automatic transfer of ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

In order to synchronize A/D conversion and timers, the ADC can be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, LPTIM1, LPTIM2 and LPTIM3 timers.

3.18 Temperature sensor

The devices embed a temperature sensor that generates a voltage (V_{TS}) that varies linearly with the temperature. This temperature sensor is internally connected to ADC2_INP12 and can measure the device ambient temperature ranging from –40 to +125 °C with a precision of ±2 %.

The temperature sensor has a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the OTP area, that is accessible in read-only mode.

3.19 Digital temperature sensor (DTS)

The devices embed a frequency output temperature sensor. DTS counts the frequency based on the LSE or PCLK to provide the temperature information.

Following functions are supported:

- interrupt generation by temperature threshold
- wakeup signal generation by temperature threshold

3.20 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers and the backup SRAM.

In order to optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} has dropped below the PDR level.

The voltage on the VBAT pin can be provided by an external battery, a supercapacitor or directly by V_{DD}. In the later case, VBAT mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

Note: None of these events (external interrupts, TAMP event, or RTC alarm/events) are able to directly restore the V_{DD} supply and force the device out of the V_{BAT} operation. Nevertheless, TAMP events and RTC alarm/events can be used to generate a signal to an external circuitry (typically a PMIC) that can restore the V_{DD} supply.

3.21 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer that can be used as voltage reference for the ADCs, and also as voltage reference for external components through the VREF+ pin.

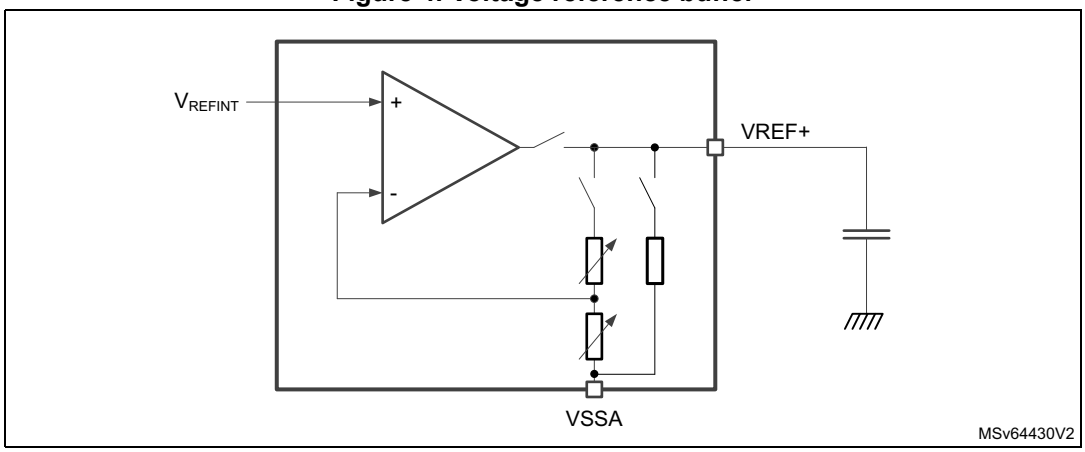
VREFBUF can be secure.

The internal VREFBUF supports four voltages:

- 1.65 V
- 1.8 V
- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal VREFBUF is off.

Figure 4. Voltage reference buffer



3.22 Digital filter for sigma-delta modulator (DFSDM)

The devices embed one DFSDM with support for two digital filters modules and four external input serial channels (transceivers) or alternately four internal parallel inputs.

The DFSDM interfaces external ΣΔ modulators to the device and performs digital filtering of the received data streams. ΣΔ modulators are used to convert analog signals into digital-serial streams that constitute the inputs of the DFSDM.

The DFSDM can also interface PDM (pulse-density modulation) microphones and perform the PDM to PCM conversion and filtering (hardware accelerated). The DFSDM features optional parallel data stream inputs from the ADCs or from the device memory (through DMA/CPU transfers into DFSDM).

The DFSDM transceivers support several serial-interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user-defined filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- Four multiplexed input digital serial channels:
  - configurable SPI interface to connect various ΣΔ modulators
  - configurable Manchester coded 1-wire interface
  - PDM (pulse-density modulation) microphone input
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for ΣΔ modulators (0 to 20 MHz)
- Alternative inputs from four internal digital parallel channels (up to 16-bit input resolution):
  - internal sources: ADC data or memory data streams (DMA)
- Two digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1 to 5), oversampling ratio (1 to 1024)
  - integrator: oversampling ratio (1 to 256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM)
- Analog watchdog featuring:
  - low-value and high-value data threshold registers
  - dedicated configurable $Sinc^x$ digital filter (order = 1 to 3, oversampling ratio = 1 to 32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- Short-circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1 to 256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- Break signal generation on analog watchdog event or on short-circuit detector event
- Extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- "Regular" or "injected" conversions:
  - "regular" conversions can be requested at any time or even in continuous mode without having any impact on the timing of "injected" conversions
  - "injected" conversions for precise timing and with high conversion priority

3.23 True random number generator (RNG)

The devices embed one RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

The RNG can be defined (in ETZPC) as accessible by secure software only.

The true RNG connects to the secured AES and PKA peripherals via a dedicated bus (not readable by the CPU).

3.24 Cryptographic and hash processors (CRYP, SAES, PKA and HASH)

The devices embed one cryptographic processor that supports the advanced cryptographic algorithms usually required to ensure confidentiality, authentication, data integrity and non-repudiation when exchanging messages with a peer.

The devices also embed a dedicated DPA resistant secure AES 128- and 256-bit key (SAES) and PKA hardware encryption/decryption accelerator, with dedicated hardware bus not accessible by the CPU.

CRYP main features:

- DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
- AES (advanced encryption standard): ECB, CBC, GCM, CCM, and CTR (counter mode) chaining algorithms, 128-, 192- or 256-bit key

Universal HASH main features:

- SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-3 (secure HASH algorithms)
- HMAC

The cryptographic accelerator supports DMA request generation.

CRYP, SAES, PKA and HASH can be defined (in ETZPC) as accessible by secure software only.

3.25 Boot and security and OTP control (BSEC)

The BSEC (boot and security and OTP control) is intended to control an OTP (one-time programmable) fuse box, used for embedded non-volatile storage for device configuration and security parameters. Some part of BSEC must be configured as accessible by secure software only.

The BSEC can use OTP words for storage of HWKEY 256-bit for SAES (secure AES).

3.26 Timers and watchdogs

The devices include two advanced-control timers, ten general-purpose timers (out of which seven are secured), two basic timers, five low-power timers, two watchdogs, and four system timers in each Cortex-A7.

All timer counters can be frozen in debug mode.

The table below compares the features of the advanced-control, general-purpose, basic and low-power timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolu-tion	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Advanced -control	TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	6	4	104.5	209
General purpose	TIM2 TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No	104.5	209
	TIM3 TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No	104.5	209
	TIM12(2)	16-bit	Up	Any integer between 1 and 65536	No	2	No	104.5	209
	TIM13(2) TIM14(2)	16-bit	Up	Any integer between 1 and 65536	No	1	No	104.5	209
	TIM15(2)	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	104.5	209
	TIM16(2) TIM17(2)	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	104.5	209
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	104.5	209
Low-power	LPTIM1, LPTIM2(2), LPTIM3(2), LPTIM4, LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	1(3)	No	104.5	104.5

1. The maximum timer clock is up to 209 MHz depending on TIMGxPRE bit in the RCC.
2. Securable timer.
3. No capture channel on LPTIM.

3.26.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge- or center-aligned modes)
- one-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100 %).

The advanced-control timer can work together with the general-purpose timers via the timer link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.26.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM12, TIM13, TIM14, TIM15, TIM16, TIM17)

There are ten synchronizable general-purpose timers embedded in the STM32MP131C/F devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  TIM 2 and TIM5 are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler, while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  These general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8, via the timer link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from one to four hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

  Each of these timers can be defined (in ETZPC) as accessible by secure software only.

3.26.3 Basic timers (TIM6 and TIM7)

These timers are mainly used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.26.4 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

Each low-power timer has an independent clock and runs also in Stop mode if it is clocked by LSE, LSI or an external clock. An LPTIMx is able to wake up the device from Stop mode.

These low-power timers support the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Selectable clock source:
  - internal clock source: LSE, LSI, HSI or APB clock
  - external clock source over LPTIM input (working even with no internal clock source running, used by the pulse counter application)
- Programmable digital glitch filter
- Encoder mode

LPTIM2 and LPTIM3 can be defined (in ETZPC) as accessible by secure software only.

3.26.5 Independent watchdogs (IWDG1, IWDG2)

An independent watchdog is based on a 12-bit downcounter and a 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and, as it operates independently from the main clock, it can operate in Stop and Standby modes. IWDG can be used as a watchdog to reset the device when a problem occurs. It is hardware- or software-configurable through the option bytes.

IWDG1 can be defined (in ETZPC) as accessible by secure software only.

3.26.6 Generic timers (Cortex-A7 CNT)

Cortex-A7 generic timers embedded inside Cortex-A7 are fed by value from system timing generation (STGEN).

The Cortex-A7 processor provides the following timers:

- physical timer for use in secure and non-secure modes

  The registers for the physical timer are banked to provide secure and non-secure copies.
- virtual timer for use in non-secure modes
- physical timer for use in hypervisor mode

Generic timers are not memory mapped peripherals and are then accessible only by specific Cortex-A7 coprocessor instructions (cp15).

3.27 System timer generation (STGEN)

The system timing generation (STGEN) generates a time-count value that provides a consistent view of time for all Cortex-A7 generic timers.

The system timing generation has the following key features:

- 64-bit wide to avoid roll-over issues
- Start from zero or a programmable value
- Control APB interface (STGENC) that enables the timer to be saved and restored across powerdown events
- Read-only APB interface (STGENR) that enables the timer value to be read by non-secure software and debug tools
- Timer value incrementing that can be stopped during system debug

STGENC can be defined (in ETZPC) as accessible by secure software only.

3.28 Real-time clock (RTC)

The RTC provides an automatic wakeup to manage all low-power modes.RTC is an independent BCD timer/counter and provides a time-of-day clock/calendar with programmable alarm interrupts.

The RTC includes also a periodic programmable wakeup flag with interrupt capability.

Two 32-bit registers contain the seconds, minutes, hours (12- or 24-hour format), day (day of week), date (day of month), month, and year, expressed in binary coded decimal format (BCD). The sub-seconds value is also available in binary format.

Binary mode is supported to ease software driver management.

Compensations for 28-, 29- (leap year), 30-, and 31-day months are performed automatically. Daylight saving time compensation can also be performed.

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

A digital calibration feature is available to compensate for any deviation in crystal oscillator accuracy.

After Backup domain reset, all RTC registers are protected against possible parasitic write accesses and protected by secured access.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode or under reset).

The RTC main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), day (day of week), date (day of month), month, and year
- Daylight saving compensation programmable by software
- Programmable alarm with interrupt function. The alarm can be triggered by any combination of the calendar fields.
- Automatic wakeup unit generating a periodic flag that triggers an automatic wakeup interrupt
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Accurate synchronization with an external clock using the sub-second shift feature
- Digital calibration circuit (periodic counter correction): 0.95 ppm accuracy, obtained in a calibration window of several seconds

- Timestamp function for event saving
- Storage of SWKEY in RTC backup registers with direct bus access to SAE (not readable by the CPU)
- Maskable interrupts/events:
  - Alarm A
  - Alarm B
  - Wakeup interrupt
  - Timestamp
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wakeup timer and timestamp individual secure or non-secure configuration
  - RTC calibration done in secure on non-secure configuration

3.29 Tamper and backup registers (TAMP)

32 x 32-bit backup registers are retained in all low-power modes and also in VBAT mode. They can be used to store sensitive data as their content is protected by a tamper detection circuit.

Seven tamper input pins and five tamper output pins are available for anti-tamper detection. The external tamper pins can be configured for edge detection, edge and level, level detection with filtering, or active tamper that increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features

- 32 backup registers (TAMP_BKPxR) implemented in the RTC domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off
- 12 tamper pins available (seven inputs and five outputs)
- Any tamper detection can generate a RTC timestamp event.
- Any tamper detection erases the backup registers.
- TrustZone support:
  - Tamper secure or non-secure configuration
  - Backup registers configuration in three configurable-size areas:
    . one read/write secure area
    . one write secure/read non-secure area
    . one read/write non-secure area
- Monotonic counter

3.30 Inter-integrated circuit interfaces (I2C1, I2C2, I2C3, I2C4, I2C5)

The devices embed five I^2C interfaces.

The I^2C bus interface handles communications between the STM32MP131C/F and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I^2C communication speed to be independent from the PCLK reprogramming
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

I2C3, I2C4 and I2C5 can be defined (in ETZPC) as accessible by secure software only.

3.31 Universal synchronous asynchronous receiver transmitter (USART1, USART2, USART3, USART6 and UART4, UART5, UART7, UART8)

The devices have four embedded universal synchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8). Refer to the table below for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 13 Mbit/s.

USART1, USART2, USART3 and USART6 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the STM32MP131C/F from Stop mode using baudrates up to 200 Kbaud.The wakeup events from Stop mode are programmable and can be:

- start bit detection
- any received data frame
- a specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 5. USART/UART features

USART modes/features[1]	USART1/2/3/6	UART4/5/7/8
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous SPI mode (master/slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wakeup from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X
USART data length	7, 8 and 9 bits	

1. X = supported.

USART1 and USART2 can be defined (in ETZPC) as accessible by secure software only.

3.32 Serial peripheral interfaces (SPI1, SPI2, SPI3, SPI4, SPI5) – inter- integrated sound interfaces (I2S1, I2S2, I2S3, I2S4)

The devices feature up to five SPIs (SPI2S1, SPI2S2, SPI2S3, SPI2S4, and SPI5) that allow communication at up to 50 Mbit/s in master and slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives eight master mode frequencies and the frame is configurable from 4 to 16 bits. All SPI interfaces support NSS pulse mode, TI mode, hardware CRC calculation and multiply of 8-bit embedded Rx and Tx FIFOs with DMA capability.

I2S1, I2S2, I2S3, and I2S4 are multiplexed with SPI1, SPI2, SPI3 and SPI4. They can be operated in master or slave mode, in full-duplex and half-duplex communication modes, and can be configured to operate with a 16- or 32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. All I^2S interfaces support multiply of 8-bit embedded Rx and Tx FIFOs with DMA capability.

SPI4 and SPI5 can be defined (in ETZPC) as accessible by secure software only.

3.33 Serial audio interfaces (SAI1, SAI2)

The devices embed two SAIs that allow the design of many stereo or mono audio protocols

such as I^2S, LSB or MSB-justified, PCM/DSP, TDM or AC'97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, each SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.
Audio sampling frequencies up to 192 kHz are supported.
In addition, up to eight microphones can be supported thanks to an embedded PDM interface.
The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.34 SPDIF receiver interface (SPDIFRX)

The SPDIFRX is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The SPDIFRX main features are the following:

- Up to four inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Support of audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal is available, the SPDIFRX re-samples the incoming signal, decodes the Manchester stream, and recognizes frames, sub-frames and blocks elements. The SPDIFRX delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, that toggles at the S/PDIF sub-frame rate that is used to compute the exact sample rate for clock drift algorithms.

3.35 Secure digital input/output MultiMediaCard interfaces (SDMMC1, SDMMC2)

Two secure digital input/output MultiMediaCard interfaces (SDMMC) provide an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices.

The SDMMC features include the following:

- Compliance with *Embedded MultiMediaCard System Specification Version 5.1*
  Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit

(HS200 SDMMC_CK speed limited to maximum allowed I/O speed)(HS400 is not supported)

- Full compatibility with previous versions of MultiMediaCards (backward compatibility)
- Full compliance with *SD memory card specifications version 4.1*
  (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported)
- Full compliance with SDIO card specification version 4.0
  Card support for two different databus modes: 1-bit (default) and 4-bit
  (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported)
- Data transfer up to 208 Mbyte/s for the 8-bit mode
  (depending maximum allowed I/O speed)
- Data and command output enable signals to control external bidirectional drivers
- Dedicated DMA controller embedded in the SDMMC host interface, allowing high-speed transfers between the interface and the SRAM
- IDMA linked list support
- Dedicated power supplies, V_{DDSD1} and V_{DDSD2} for SDMMC1 and SDMMC2 respectively, removing the need for level-shifter insertion on the SD card interface in UHS-I mode

Only some GPIOs for SDMMC1 and SDMMC2 are available on a dedicated VDDSD1 or VDDSD2 supply pin. Those are part of the default boot GPIOs for SDMMC1 and SDMMC2 (SDMMC1: PC[12:8], PD[2], SDMMC2: PB[15,14,4,3], PE3, PG6). They can be identified in the alternate function table by signals with a "_VSD1" or "_VSD2" suffix.

Each SDMMC is coupled with a delay block (DLYBSD) allowing support of an external data frequency above 100 MHz.

Both SDMMC interfaces have securable configuration ports.

3.36 Universal serial bus high-speed host (USBH)

The devices embed one USB high-speed host (up to 480 Mbit/s) with two physical ports. USBH supports both low, full-speed (OHCI) as well as high-speed (EHCI) operations independently on each port. It integrates two transceivers that can be used for either low-speed (1.2 Mbit/s), full-speed (12 Mbit/s) or high-speed operation (480 Mbit/s). The second high-speed transceiver is shared with OTG high-speed.

The USBH is compliant with the USB 2.0 specification. The USBH controllers require dedicated clocks that are generated by a PLL inside the USB high-speed PHY.

3.37 USB on-the-go high-speed (OTG)

The devices embed one USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG supports both full-speed and high-speed operations. The transceiver for high-speed operation (480 Mbit/s) is shared with the USB Host second port.

The USB OTG HS is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controllers require a dedicated 48 MHz clock that is generated by a PLL inside RCC or inside the USB high-speed PHY.

The USB OTG HS main features are listed below:

- Combined Rx and Tx FIFO size of 4 Kbyte with dynamic FIFO sizing
- SRP (session request protocol) and HNP (host negotiation protocol) support
- Eight bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (link power management) support
- Battery charging specification revision 1.2 support
- HS OTG PHY support
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected.

The USB OTG configuration port can be secure.

3.38 Gigabit Ethernet MAC interface (ETH1)

The devices provide one IEEE-802.3-2002-compliant gigabit media access controllers (GMAC) for Ethernet LAN communications through an industry-standard medium-independent interface (MII), a reduced medium-independent interface (RMII), or a reduced gigabit medium-independent interface (RGMII).

The devices require an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device port using 17 signals for MII, 7 signals for RMII, or 13 signals for RGMII, and can be clocked using the 25 MHz (MII, RMII, RGMII) or 125 MHz (RGMII) from the STM32MP131C/F or from the PHY.

The devices include the following features:

- Operation modes and PHY interfaces
  - 10-, 100-, and 1000-Mbit/s data transfer rates
  - Support of both full-duplex and half-duplex operations
  - MII, RMII and RGMII PHY interfaces
- Processing control
  - Multi-layer Packet filtering: MAC filtering on source (SA) and destination (DA) address with perfect and hash filter, VLAN tag-based filtering with perfect and hash filter, Layer 3 filtering on IP source (SA) or destination (DA) address, Layer 4 filtering on source (SP) or destination (DP) port
  - Double VLAN processing: insertion of up to two VLAN tags in transmit path, tag filtering in receive path
  - IEEE 1588-2008/PTPv2 support
  - Supports network statistics with RMON/MIB counters (RFC2819/RFC2665)
- Hardware offload processing
  - Preamble and start-of-frame data (SFD) insertion or deletion
  - Integrity checksum offload engine for IP header and TCP/UDP/ICMP payload: transmit checksum calculation and insertion, receive checksum calculation and comparison
  - Automatic ARP request response with the device MAC address
  - TCP segmentation: automatic split of large transmit TCP packet into multiple small packets
- Low-power mode
  - Energy efficient Ethernet (standard IEEE 802.3az-2010)
  - Remote wakeup packet and AMD Magic Packet™ detection

The ETH1 can be programmed as secure. When secure, transactions over the AXI interface are secure, and the configuration registers can only be modified by secure accesses.

3.39 Debug infrastructure

The devices offer the following debug and trace features to support software development and system integration:

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Trace port
- Arm CoreSight debug and trace components

The debug can be controlled via a JTAG/serial-wire debug access port, using industry standard debugging tools.

A trace port allows data to be captured for logging and analysis.

A debug access to secure areas is enabled by the authentication signals in the BSEC.

4 Pinout, pin description and alternate functions

Figure 5. STM32MP131C/F LFBGA289 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	PA9	PD10	PB7	PE7	PD5	PE8	PG4	PH9	PH13	PC7	PB9	PB14	PG6	PD2	PC9	VSS
B	PD3	PF5	PD14	PE12	PE1	PE9	PH14	PE10	PF1	PF3	PC6	PB15	PB4	PC10	PC12	DDR_DQ4	DDR_DQ0
C	PB6	PH12	PE14	PE13	PD8	PD12	PD15	VSS	PG7	PB5	PB3	VDDSD1	PF0	PC11	DDR_DQ1	DDR_DQS0N	DDR_DQS0P
D	PB8	PD6	VSS	PE11	PD1	PE0	PG0	PE15	PB12	PB10	VDDSD2	VSS	PE3	PC8	DDR_DQM0	DDR_DQ5	DDR_DQ3
E	PG9	PD11	PA12	PD0	VSS	PA15	PD4	PD9	PF2	PB13	PH10	VDDQ_DDR	DDR_DQ2	DDR_DQ6	DDR_DQ7	DDR_A5	DDR_RESETN
F	PG10	PG5	PG8	PH2	PH8	VDDCPU	VDD	VDDCPU	VDDCPU	VDD	VDD	VDDQ_DDR	VSS	DDR_A13	VSS	DDR_A9	DDR_A2
G	PF9	PF6	PF10	PG15	PF8	VDD	VSS	VSS	VSS	VSS	VSS	VDDQ_DDR	DDR_BA2	DDR_A7	DDR_A3	DDR_A0	DDR_BA0
H	PH11	PI3	PH7	PB2	PE4	VDDCPU	VSS	VDDCORE	VDDCORE	VDDCORE	VSS	VDDQ_DDR	DDR_WEN	VSS	DDR_ODT	DDR_CSN	DDR_RASN
J	PD13	VBAT	PI2	VSS_PLL	VDD_PLL	VDDCPU	VSS	VDDCORE	VSS	VDDCORE	VSS	VDDQ_DDR	VDDCORE	DDR_A10	DDR_CASN	DDR_CLKP	DDR_CLKN
K	PC14-OSC32_IN	PC15-OSC32_OUT	VSS	PC13	PI1	VDD	VSS	VDDCORE	VDDCORE	VDDCORE	VSS	VDDQ_DDR	DDR_A11	DDR_CKE	DDR_A1	DDR_A15	DDR_A12
L	PE2	PF4	PH6	PI0	PG3	VDD	VSS	VSS	VSS	VSS	VSS	VDDQ_DDR	DDR_ATO	DDR_DTO0	DDR_A8	DDR_BA1	DDR_A14
M	PF7	PA8	PG11	VDD_ANA	VSS_ANA	VDD	VDD	VDD	VDD	VDD	VDD	VDDQ_DDR	DDR_VREF	DDR_A4	VSS	DDR_DTO1	DDR_A6
N	PE6	PG1	PD7	VSS	PB11	PF13	VSSA	PA3	NJTRST	VSS_USB HS	VDDA1V1_REG	VDDQ_DDR	PWR_LP	DDR_DQM1	DDR_DQ10	DDR_DQ8	DDR_ZQ
P	PH0-OSC_IN	PH1-OSC_OUT	PA13	PF14	PA2	VREF-	VDDA	PG13	PG14	VDD3V3_USBHS	VSS	PI5-BOOT1	VSS_PLL2	PWR_ON	DDR_DQ11	DDR_DQ13	DDR_DQ9
R	PG2	PH3	PWR_CPU_ON	PA1	VSS	VREF+	PC5	VSS	VDD	PF15	VDDA1V8_REG	PI6-BOOT2	VDD_PLL2	PH5	DDR_DQ12	DDR_DQS1N	DDR_DQS1P
T	PG12	PA11	PC0	PF12	PC3	PF11	PB1	PA6	PE5	PDR_ON	USB_DP2	PA14	USB_DP1	BYPASS_REG1V8	PH4	DDR_DQ15	DDR_DQ14
U	VSS	PA7	PA0	PA5	PA4	PC4	PB0	PC1	PC2	NRST	USB_DM2	USB_RREF	USB_DM1	PI4-BOOT0	PA10	PI7	VSS

MSv65067V5

The above figure shows the package top view.

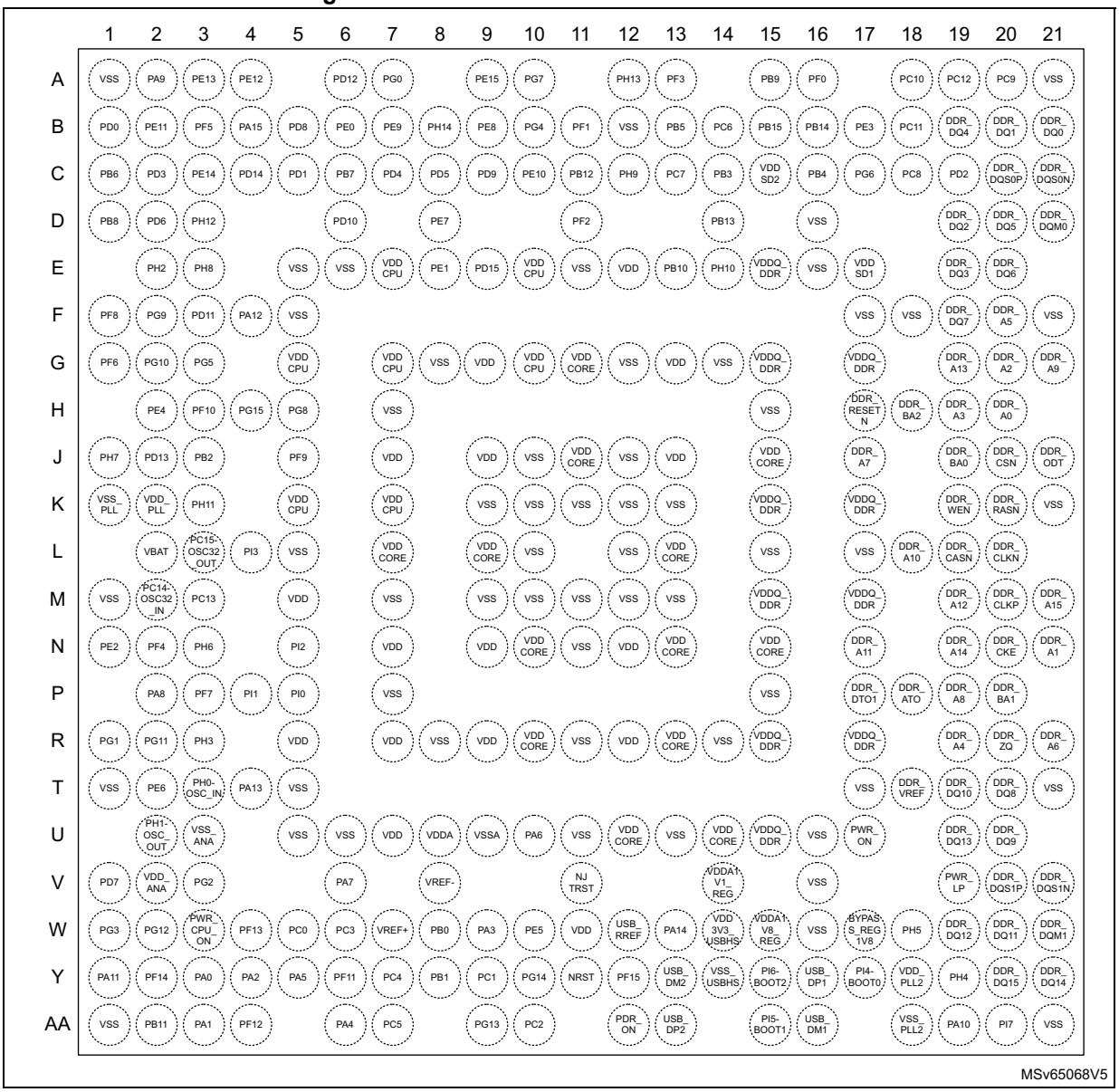
Figure 6. STM32MP131C/F TFBGA289 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	PD4	PE9	PG0	PD15	PE15	PB12	PF1	PC7	PC6	PF0	PB14	VDDSD2	VDDSD1	DDR_DQ4	DDR_DQ0	VSS
B	PE12	PD8	PE0	PD5	PD9	PH14	PF2	VSS	PF3	PB13	PB3	PE3	PC12	VSS	DDR_DQ1	DDR_DQS0N	DDR_DQS0P
C	PE13	PD1	PE1	PE7	VSS	VDD	PE10	PG7	PG4	PB9	PH10	PC11	PC8	DDR_DQ2	DDR_DQM0	DDR_DQ3	DDR_DQ5
D	PF5	PA9	PD10	VDDCPU	PB7	VDDCPU	PD12	VDDCPU	PH9	VDD	PB15	VDD	VSS	VDDQ_DDR	DDR_RESETN	DDR_DQ7	DDR_DQ6
E	PD0	PE14	VSS	PE11	VDDCPU	VSS	PA15	VSS	PH13	VSS	PB4	VSS	VDDQ_DDR	VSS	VDDQ_DDR	VSS	DDR_A13
F	PH8	PA12	VDD	VDDCPU	VSS	VDDCORE	PD14	PE8	PB5	VDDCORE	PC10	VDDCORE	VSS	VDDQ_DDR	DDR_A7	DDR_A5	DDR_A9
G	PD11	PH2	PB6	PB8	PG9	PD3	PH12	PG15	PD6	PB10	PD2	PC9	DDR_A2	DDR_BA2	DDR_A3	DDR_A0	DDR_ODT
H	PG5	PG10	PF8	VDDCPU	VSS	VDDCORE	PH11	PI3	PF9	PG6	BYPASS_REG1V8	VDDCORE	VSS	VDDQ_DDR	DDR_BA0	DDR_CSN	DDR_WEN
J	VDD_PLL	VSS_PLL	PG8	PI2	VBAT	PH6	PF7	PA8	PF12	VDD	VDDA1V8_REG	PA10	DDR_VREF	DDR_RASN	DDR_A10	VSS	DDR_CASN
K	PE4	PF10	PB2	VDD	VSS	VDDCORE	PA13	PA1	PC4	NRST	VSS_PLL2	VDDCORE	VSS	VDDQ_DDR	DDR_A15	DDR_CLKP	DDR_CLKN
L	PF6	VSS	PH7	VDD_ANA	VSS_ANA	PG12	PA0	PF11	PE5	PF15	VDD_PLL2	PH5	DDR_CKE	DDR_A12	DDR_A1	DDR_A11	DDR_A14
M	PC14-OSC32_IN	PC15-OSC32_OUT	PC13	VDD	VSS	PB11	PA5	PB0	VDDCORE	USB_RREF	PI6-BOOT2	VDDCORE	VSS	VDDQ_DDR	DDR_A6	DDR_A8	DDR_BA1
N	PD13	VSS	PI0	PI1	PA11	VSS	PA4	PB1	VSS	VSS	PI5-BOOT1	VSS	VDDQ_DDR	VSS	VDDQ_DDR	VSS	DDR_ATO
P	PH0-OSC_IN	PH1-OSC_OUT	PF4	PG1	VSS	VDD	PC3	PC5	VDD	VDD	PI4-BOOT0	VDD	VSS	VDDQ_DDR	DDR_A4	DDR_ZQ	DDR_DQ8
R	PG11	PE6	PD7	PWR_CPU_ON	PA2	PA7	PC1	PA6	PG13	NJTRST	PA14	VSS	PWR_ON	DDR_DQM1	DDR_DQ12	DDR_DQ11	DDR_DQ9
T	PE2	PH3	PF13	PC0	VSSA	VREF-	PA3	PG14	USB_DP2	VSS	VSS_USBHS	USB_DP1	PH4	DDR_DQ13	DDR_DQ14	DDR_DQS1P	DDR_DQS1N
U	VSS	PG3	PG2	PF14	VDDA	VREF+	PDR_ON	PC2	USB_DM2	VDDA1V1_REG	VDD3V3_USBHS	USB_DM1	PI7	PWR_LP	DDR_DQ15	DDR_DQ10	VSS

MSv67512V3

The above figure shows the package top view.

Figure 7. STM32MP131C/F TFBGA320 ballout



The above figure shows the package top view.

Table 6. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	O	Output only pin
	I/O	Input/output pin
	A	Analog or special level pin
I/O structure	FT(U/D/PD)	5 V tolerant I/O (with fixed pull-up / pull-down / programmable pull-down)
	DDR	1.5 V, 1.35 V or 1.2 V I/O for DDR3, DDR3L, LPDDR2/LPDDR3 interface
	A	Analog signal
	RST	Reset pin with weak pull-up resistor
	Option for FT I/Os	
	_f(1)	I2C FM+ option
	_a(2)	Analog option (supplied by VDDA for the analog part of the I/O)
	_u(3)	USB option (supplied by VDD3V3_USBxx for the USB part of the I/O)
	_h(4)	High-speed output for 1.8V typ. VDD (for SPI, SDMMC, QUADSPI, TRACE)
	_vh(5)	Very-high-speed option for 1.8V typ. VDD (for ETH, SPI, SDMMC, QUADSPI, TRACE)
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 7* are: FT_f, FT_fh, FT_fvh
2. The related I/O structures in *Table 7* are: FT_a, FT_ha, FT_vha
3. The related I/O structures in *Table 7* are: FT_u
4. The related I/O structures in *Table 7* are: FT_h, FT_fh, FT_fvh, FT_vh, FT_ha, FT_vha
5. The related I/O structures in *Table 7* are: FT_vh, FT_vha, FT_fvh

Table 7. STM32MP131C/F ball definitions

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
K10	F6	U14	VDDCORE	S	-	-	-	-
A2	D2	A2	PA9	I/O	FT_h	-	TIM1_CH2, I2C3_SMBA, DFSDM1_DATIN0, USART1_TX, UART4_TX, FMC_NWAIT(boot)	-
A1	A1	T5	VSS	S	-	-	-	-
M6	F3	U7	VDD	S	-	-	-	-
D4	E4	B2	PE11	I/O	FT_vh	-	TIM1_CH2, USART2_CTS/USART2_NSS, SAI1_D2, SPI4_MOSI/I2S4_SDO, SAI1_FS_A, USART6_CK, ETH1_MII_TX_ER, FMC_D8(boot)/FMC_AD8	-
B2	D1	B3	PF5	I/O	FT_h	-	TRACED12, DFSDM1_CKIN0, I2C1_SMBA, FMC_A5	-
B1	G6	C2	PD3	I/O	FT_f	-	TIM2_CH1, USART2_CTS/USART2_NSS, DFSDM1_CKOUT, I2C1_SDA, SAI1_D3, FMC_CLK	-
C3	E2	C3	PE14	I/O	FT_h	-	TIM1_BKIN, SAI1_D4, UART8_RTS/UART8_DE, QUADSPI_BK1_NCS, QUADSPI_BK2_IO2, FMC_D11(boot)/FMC_AD11	TAMP_IN6
F6	D4	E7	VDDCPU	S	-	-	-	-
E4	E1	B1	PD0	I/O	FT	-	SAI1_MCLK_A, SAI1_CK1, FMC_D2(boot)/FMC_AD2	-
C2	G7	D3	PH12	I/O	FT_fh	-	USART2_TX, TIM5_CH3, DFSDM1_CKIN1, I2C3_SCL, SPI5_MOSI, SAI1_SCK_A, QUADSPI_BK2_IO2, SAI1_CK2, ETH1_MII_CRS, FMC_A6	-
C1	G3	C1	PB6	I/O	FT_h	-	TRACED6, TIM16_CH1N, TIM4_CH1, TIM8_CH1, USART1_TX, SAI1_CK2, QUADSPI_BK1_NCS, FMC_NE3, HDP6	-
A17	A17	T17	VSS	S	-	-	-	-
M7	-	J13	VDD	S	-	-	-	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
D2	G9	D2	PD6	I/O	FT	-	TIM16_CH1N, SAI1_D1, SAI1_SD_A, UART4_TX(boot)	-
F5	F1	E3	PH8	I/O	FT_fh	-	TRACED9, TIM5_ETR, USART2_RX, I2C3_SDA, FMC_A8, HDP2	-
D1	G4	D1	PB8	I/O	FT_f	-	TIM16_CH1, TIM4_CH3, I2C1_SCL, I2C3_SCL, DFSDM1_DATIN1, UART4_RX, SAI1_D1, FMC_D13(boot)/FMC_AD13	-
E3	F2	F4	PA12	I/O	FT_h	-	TIM1_ETR, SAI2_MCLK_A, USART1_RTS/USART1_DE, FMC_A7	-
F8	D6	E10	VDDCPU	S	-	-	-	-
F4	G2	E2	PH2	I/O	FT_h	-	LPTIM1_IN2, UART7_TX, QUADSPI_BK2_IO0(boot), ETH1_MII_CRS, FMC_NE4	-
C8	B8	T21	VSS	S	-	-	-	-
E2	G1	F3	PD11	I/O	FT_h	-	LPTIM2_IN2, I2C4_SMBA, USART3_CTS/USART3_NSS, SPDIFRX_IN0, QUADSPI_BK1_IO2, FMC_CLE(boot)/FMC_A16, UART7_RX	-
E1	G5	F2	PG9	I/O	FT_f	-	DBTRGO, I2C2_SDA, USART6_RX, SPDIFRX_IN3, FMC_NE2, FMC_NCE(boot)	-
G5	H3	F1	PF8	I/O	FT_h	-	TIM16_CH1N, TIM4_CH3, TIM8_CH3, SAI1_SCK_B, USART6_TX, TIM13_CH1, QUADSPI_BK1_IO0(boot)	WKUP1
M8	-	M5	VDD	S	-	-	-	-
F3	J3	H5	PG8	I/O	FT_h	-	TIM2_CH1, TIM8_ETR, SPI5_MISO, SAI1_MCLK_B, USART3_RTS/USART3_DE, SPDIFRX_IN2, QUADSPI_BK2_IO2, QUADSPI_BK1_IO3, FMC_NE2	TAMP_IN4
F9	D8	G5	VDDCPU	S	-	-	-	-
F2	H1	G3	PG5	I/O	FT_h	-	TIM17_CH1, FMC_A15	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
G4	G8	H4	PG15	I/O	FT_h	-	USART6_CTS/USART6_NSS, UART7_CTS, QUADSPI_BK1_IO1	-
F1	H2	G2	PG10	I/O	FT_h	-	SPI5_SCK, SAI1_SD_B, UART8_CTS, QUADSPI_BK2_IO1(boot), FMC_NE3	-
D3	B14	U5	VSS	S	-	-	-	-
G3	K2	H3	PF10	I/O	FT_h	-	TIM16_BKIN, SAI1_D3, TIM8_BKIN, SPI5_NSS, USART6_RTS/USART6_DE, UART7_RTS/UART7_DE, QUADSPI_CLK(boot)	TAMP_IN1
H8	F10	-	VDDCORE	S	-	-	-	-
G2	L1	G1	PF6	I/O	FT_vh	-	TIM16_CH1, SPI5_NSS, UART7_RX(boot), QUADSPI_BK1_IO2	-
D12	C5	U6	VSS	S	-	-	-	-
M9	K4	N7	VDD	S	-	-	-	-
G1	H9	J5	PF9	I/O	FT_h	-	TIM17_CH1N, TIM1_CH1, DFSDM1_CKIN3, SAI1_D4, UART7_CTS, UART8_RX, TIM14_CH1, QUADSPI_BK1_IO1(boot), QUADSPI_BK2_IO3, FMC_A9	-
H5	K1	H2	PE4	I/O	FT_h	-	SPI5_MISO, SAI1_D2, DFSDM1_DATIN3, TIM15_CH1N, I2S_CKIN, SAI1_FS_A, UART7_RTS/UART7_DE, UART8_TX, QUADSPI_BK2_NCS, FMC_NCE2, FMC_A25	-
H6	E5	G7	VDDCPU	S	-	-	-	-
H4	K3	J3	PB2	I/O	FT_h	-	RTC_OUT2, SAI1_D1, I2S_CKIN, SAI1_SD_A, UART4_RX, QUADSPI_BK1_NCS(boot), FMC_A6	TAMP_IN7
E5	D13	U11	VSS	S	-	-	-	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
H3	L3	J1	PH7	I/O	FT_fh	-	SAI2_FS_B, I2C3_SDA, SPI5_SCK, QUADSPI_BK2_IO3, ETH1_MII_TX_CLK, QUADSPI_BK1_IO3	-
H1	H7	K3	PH11	I/O	FT_fh	-	SPI5_NSS, TIM5_CH2, SAI2_SD_A, SPI2_NSS/I2S2_WS, I2C4_SCL, USART6_RX, QUADSPI_BK2_IO0, FMC_A12	-
J1	N1	J2	PD13	I/O	FT_h	-	LPTIM2_ETR, TIM4_CH2, TIM8_CH2, SAI1_CK1, SAI1_MCLK_A, USART1_RX, QUADSPI_BK1_IO3, QUADSPI_BK2_IO2, FMC_A18	-
J5	J1	K2	VDD_PLL	S	-	-	-	-
J4	J2	K1	VSS_PLL	S	-	-	-	-
H2	H8	L4	PI3	I/O	FT	(1)	SPDIFRX_IN3, ETH1_MII_RX_ER	TAMP_IN4/TAMP_OUT5, WKUP2
K4	M3	M3	PC13	I/O	FT	(1)	-	RTC_OUT1/RTC_TS/RTC_LSCO, TAMP_IN1/TAMP_OUT2, WKUP3
J3	J4	N5	PI2	I/O	FT	(1)	SPDIFRX_IN2	TAMP_IN3/TAMP_OUT4, WKUP5
K5	N4	P4	PI1	I/O	FT	(1)	SPDIFRX_IN1	RTC_OUT2/RTC_LSCO, TAMP_IN2/TAMP_OUT3, WKUP4
F13	L2	U13	VSS	S	-	-	-	-
J2	J5	L2	VBAT	S	-	-	-	-
L4	N3	P5	PI0	I/O	FT	(1)	SPDIFRX_IN0	TAMP_IN8/TAMP_OUT1
K2	M2	L3	PC15-OSC32_OUT	I/O	FT	(1)	-	OSC32_OUT
F15	N2	U16	VSS	S	-	-	-	-
K1	M1	M2	PC14-OSC32_IN	I/O	FT	(1)	-	OSC32_IN

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
G7	E3	V16	VSS	S	-	-	-	-
H9	K6	N15	VDDCORE	S	-	-	-	-
M10	M4	N9	VDD	S	-	-	-	-
G8	E6	W16	VSS	S	-	-	-	-
L2	P3	N2	PF4	I/O	FT_h	-	USART2_RX, FMC_A4	-
M2	J8	P2	PA8	I/O	FT_fh	-	MCO1, SAI2_MCLK_A, TIM8_BKIN2, I2C4_SDA, SPI5_MISO, SAI2_CK1, USART1_CK, SPI2_MOSI/I2S2_SDO, OTG_HS_SOF, FMC_A21	-
L1	T1	N1	PE2	I/O	FT_fh	-	TRACECLK, TIM2_ETR, I2C4_SCL, SPI5_MOSI, SAI1_FS_B, USART6_RTS/USART6_DE, SPDIFRX_IN1, FMC_A23	-
M1	J7	P3	PF7	I/O	FT_vh	-	TIM17_CH1, UART7_TX(boot), UART4_CTS, ETH1_RGMII_CLK125, FMC_A18	-
M3	R1	R2	PG11	I/O	FT_vh	-	SAI2_D3, I2S2_MCK, USART3_TX, UART4_TX, FMC_A24	-
L3	J6	N3	PH6	I/O	FT_fh	-	TIM12_CH1, USART2_CK, I2C5_SDA, SPI2_SCK/I2S2_CK, QUADSPI_BK1_IO2, ETH1_PHY_INTN, ETH1_MII_RX_ER, QUADSPI_BK1_NCS	-
N2	P4	R1	PG1	I/O	FT_vh	-	LPTIM1_ETR, TIM4_ETR, SAI2_FS_A, I2C2_SMBA, SPI2_MISO/I2S2_SDI, SAI2_D2, FMC_NBL0	-
M11	-	N12	VDD	S	-	-	-	-
N1	R2	T2	PE6	I/O	FT_vh	-	MCO2, TIM1_BKIN2, SAI2_SCK_B, TIM15_CH2, I2C3_SMBA, SAI1_SCK_B, UART4_RTS/UART4_DE, FMC_A22	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
P1	P1	T3	PH0-OSC_IN	I/O	FT	-	-	OSC_IN
G9	U1	N11	VSS	S	-	-	-	-
P2	P2	U2	PH1-OSC_OUT	I/O	FT	-	-	OSC_OUT
R2	T2	R3	PH3	I/O	FT_fh	-	I2C3_SCL, SPI5_MOSI, QUADSPI_BK2_IO1, ETH1_MII_COL, QUADSPI_BK1_IO0	-
M5	L5	U3	VSS_ANA	S	-	-	-	-
L5	U2	W1	PG3	I/O	FT_fvh	-	TIM8_BKIN2, I2C2_SDA, SAI2_SD_B, ETH1_MDIO, FMC_A13	-
M4	L4	V2	VDD_ANA	S	-	-	-	-
R1	U3	V3	PG2	I/O	FT	-	MCO2, TIM8_BKIN, SAI2_MCLK_B, ETH1_MDC	-
T1	L6	W2	PG12	I/O	FT	-	LPTIM1_IN1, SAI2_SCK_A, SAI2_CK2, USART6_RTS/USART6_DE, USART3_CTS, ETH1_PHY_INTN	-
F7	P6	R5	VDD	S	-	-	-	-
G10	E8	T1	VSS	S	-	-	-	-
N3	R3	V1	PD7	I/O	FT_fh	-	MCO1, USART2_CK, I2C2_SCL, I2C3_SDA, SPDIFRX_IN0, ETH1_MII_RX_CLK/ETH1_RGMII_RX_CLK/ETH1_RMII_REF_CLK, QUADSPI_BK1_IO2, FMC_NE1	-
P3	K7	T4	PA13	I/O	FT	-	DBTRGO, DBTRGI, MCO1, UART4_TX	BOOTFAILN
R3	R4	W3	PWR_CPU_ON	O	FT	-	-	-
T2	N5	Y1	PA11	I/O	FT_f	-	TIM1_CH4, I2C5_SCL, SPI2_NSS/I2S2_WS, USART1_CTS/USART1_NSS, ETH1_CLK	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
N5	M6	AA2	PB11	I/O	FT_vh	-	TIM2_CH4, LPTIM1_OUT, I2C5_SMBA, USART3_RX, ETH1_MII_TX_EN/ETH1_RGMII_TX_CTL/ETH1_RMII_TX_EN	-
P4	U4	Y2	PF14(JTCK/SWCLK)	I/O	FT	(2)	JTCK/SWCLK	-
U3	L7	Y3	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, TIM15_BKIN, SAI1_SD_B, UART5_TX, ETH1_MII_CRS	ADC2_INP7, ADC2_INN3
N6	T3	W4	PF13	I/O	FT_a	-	TIM2_ETR, SAI1_MCLK_B, DFSDM1_DATIN3, USART2_TX, UART5_RX	ADC2_INP11, ADC2_INN10
G11	E10	P7	VSS	S	-	-	-	-
F10	-	-	VDD	S	-	-	-	-
R4	K8	AA3	PA1	I/O	FT_a	-	TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, DFSDM1_CKIN0, USART2_RTS/USART2_DE, ETH1_MII_RX_CLK/ETH1_RGMII_RX_CLK/ETH1_RMII_REF_CLK	ADC2_INP3
P5	R5	Y4	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, USART2_TX, ETH1_MDIO	ADC2_INP1
U4	M7	Y5	PA5	I/O	FT_a	-	TIM2_CH1/TIM2_ETR, USART2_CK, TIM8_CH1N, SAI1_D1, SPI1_NSS/I2S1_WS, SAI1_SD_A, ETH1_PPS_OUT	-
T3	T4	W5	PC0	I/O	FT_ha	-	SAI1_SCK_A, SAI1_CK2, I2S1_MCK, SPI1_MOSI/I2S1_SDO, USART1_TX	ADC2_INP0, ADC2_INN1, TAMP_IN3
T4	J9	AA4	PF12	I/O	FT_vha	-	SPI1_NSS/I2S1_WS, SAI1_SD_A, UART4_TX, ETH1_MII_TX_ER, ETH1_RGMII_CLK125	-
R6	U6	W7	VREF+	S	-	-	-	-
P7	U5	U8	VDDA	S	-	-	-	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
P6	T6	V8	VREF-	S	-	-	-	-
N7	T5	U9	VSSA	S	-	-	-	-
U2	R6	V6	PA7	I/O	FT_ha	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SAI2_D1, SPI1_SCK/I2S1_CK, USART1_CTS/USART1_NSS, TIM14_CH1, ETH1_MII_RX_DV/ETH1_RGMII_RX_CTL/ETH1_RMII_CRS_DV, SAI2_SD_A	-
T6	L8	Y6	PF11	I/O	FT_a	-	USART2_TX, SAI1_D2, DFSDM1_CKIN3, SAI1_FS_A	ADC2_INP8, ADC2_INN4
U5	N7	AA6	PA4	I/O	FT_a	-	TIM5_ETR, USART2_CK, SAI1_SCK_B, SPI1_NSS/I2S1_WS, DFSDM1_CKIN1, ETH1_PPS_OUT, SAI1_SCK_A	-
U6	K9	Y7	PC4	I/O	FT_a	-	TIM3_ETR, DFSDM1_CKIN2, SAI1_D3, I2S1_MCK, UART5_RTS/UART5_DE, SPDIFRX_IN2, ETH1_MII_RXD0/ETH1_RGMII_RXD0/ETH1_RMII_RXD0, SAI2_D3	ADC2_INP4
F11	P9	-	VDD	S	-	-	-	-
H7	E12	P15	VSS	S	-	-	-	-
T5	P7	W6	PC3	I/O	FT_ha	-	SAI1_CK1, DFSDM1_CKOUT, SPI1_MISO/I2S1_SDI, SPI1_SCK/I2S1_CK, UART5_CTS, SAI1_MCLK_A, ETH1_MII_TX_CLK	TAMP_IN5
J8	M9	-	VDDCORE	S	-	-	-	-
R7	P8	AA7	PC5	I/O	FT_a	-	DFSDM1_DATIN2, SAI2_D4, I2S_CKIN, SAI1_D4, USART2_CTS/USART2_NSS, SPDIFRX_IN3, ETH1_MII_RXD1/ETH1_RGMII_RXD1/ETH1_RMII_RXD1	ADC2_INP10

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
U7	M8	W8	PB0	I/O	FT_a	-	DBTRGI, TIM1_CH2N, TIM3_CH3, TIM8_CH2N, USART1_RX, I2S1_MCK, SAI2_FS_A, USART1_CK, UART4_CTS, SAI2_D2, ETH1_MII_RXD2/ETH1_RGMII_RXD2	ADC2_INP9, ADC2_INN5
N8	T7	W9	PA3	I/O	FT_ha	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, SPI1_MOSI/I2S1_SDO, SAI1_FS_B, USART2_RX, ETH1_MII_COL	PVD_IN, WKUP6
T7	N8	Y8	PB1	I/O	FT_ha	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI1_SCK/I2S1_CK, DFSDM1_DATIN1, UART4_RX, ETH1_MII_RXD3/ETH1_RGMII_RXD3	ADC2_INP5
U8	R7	Y9	PC1	I/O	FT_vha	-	DFSDM1_DATIN0, SAI1_D3, ETH1_MII_RX_DV/ETH1_RMII_CRS_DV, ETH1_RGMII_GTX_CLK	ADC2_INP2
H10	-	R10	VDDCORE	S	-	-	-	-
T8	R8	U10	PA6	I/O	FT_ha	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SAI2_CK2, SPI1_MISO/I2S1_SDI, USART1_CK, UART4_RTS/UART4_DE, TIM13_CH1, SAI2_SCK_A	TAMP_IN2
H11	E14	R8	VSS	S	-	-	-	-
G6	P10	-	VDD	S	-	-	-	-
J10	-	R13	VDDCORE	S	-	-	-	-
P8	R9	AA9	PG13	I/O	FT_vha	-	LPTIM1_OUT, USART6_CTS/USART6_NSS, ETH1_MII_TXD0/ETH1_RGMII_TXD0/ETH1_RMII_TXD0	ADC2_INP6, ADC2_INN2
T9	L9	W10	PE5	I/O	FT_vh	-	SAI2_SCK_B, TIM8_CH3, TIM15_CH1, UART4_RX, ETH1_MII_TXD3/ETH1_RGMII_TXD3, FMC_NE1	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
P9	T8	Y10	PG14	I/O	FT_vh	-	LPTIM1_ETR, SAI2_D1, USART6_TX, SAI2_SD_A, ETH1_MII_TXD1/ETH1_RGMII_TXD1/ETH1_RMII_TXD1	-
J13	-	U12	VDDCORE	S	-	-	-	-
U9	U8	AA10	PC2	I/O	FT_vha	-	SPI5_NSS, SPI1_NSS/I2S1_WS, SAI2_MCLK_A, USART1_RTS/USART1_DE, SAI2_CK1, ETH1_MII_TXD2/ETH1_RGMII_TXD2	-
H14	E16	R11	VSS	S	-	-	-	-
R9	J10	W11	VDD	S	-	-	-	-
K8	-	G11	VDDCORE	S	-	-	-	-
N9	R10	V11	NJTRST	I	FTU	-	-	-
U10	K10	Y11	NRST	I/O	RST	-	-	-
T10	U7	AA12	PDR_ON	I	FT	-	-	-
U12	M10	W12	USB_RREF	A	A	-	-	-
P10	U11	W14	VDD3V3_USBHS	S	-	-	-	-
T11	T9	AA13	USB_DP2	A	FT_u	-	-	USBH_HS_DP2 (boot), OTG_HS_DP
U11	U9	Y13	USB_DM2	A	FT_u	-	-	USBH_HS_DM2 (boot), OTG_HS_DM
N10	T11	Y14	VSS_USBHS	S	-	-	-	-
R10	L10	Y12	PF15 (JTMS/SWDIO)	I/O	FT	(3)	JTMS/SWDIO	-
T12	R11	W13	PA14	I/O	FT	-	DBTRGO, DBTRGI, MCO2, OTG_HS_SOF	-
R12	M11	Y15	PI6-BOOT2 (BOOT2)	I/O	FT	(4)	BOOT2	-
K6	-	-	VDD	S	-	-	-	-
L6	-	-	VDD	S	-	-	-	-
-	-	R7	VDD	S	-	-	-	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
R11	J11	W15	VDDA1V8_ REG	S	-	-	-	-
J7	R12	R14	VSS	S	-	-	-	-
N11	U10	V14	VDDA1V1_ REG	S	-	-	-	-
J9	T10	-	VSS	S	-	-	-	-
-	-	R9	VDD	S	-	-	-	-
-	-	R12	VDD	S	-	-	-	-
P12	N11	AA15	PI5-BOOT1 (BOOT1)	I/O	FT	(4)	BOOT1	-
U14	P11	Y17	PI4-BOOT0 (BOOT0)	I/O	FT	(4)	BOOT0	-
U13	U12	AA16	USB_DM1	A	FT_u	-	-	USBH_HS_DM1
T13	T12	Y16	USB_DP1	A	FT_u	-	-	USBH_HS_DP1
U15	J12	AA19	PA10	I/O	FT_u	-	TIM1_CH3	OTG_HS_ID
U16	U13	AA20	PI7	I/O	FT_u	-	-	OTG_HS_VBUS
R13	L11	Y18	VDD_PLL2	S	-	-	-	-
P13	K11	AA18	VSS_PLL2	S	-	-	-	-
K9	F12	J11	VDDCORE	S	-	-	-	-
T14	H11	W17	BYPASS_REG 1V8	I	FT	-	-	-
-	F5	B12	VSS	S	-	-	-	-
T15	T13	Y19	PH4(JTDI)	I/O	FT	(3)	JTDI	-
R14	L12	W18	PH5(JTDO)	I/O	FT	(3)	JTDO	-
N13	U14	V19	PWR_LP	O	FT	-	-	-
P14	R13	U17	PWR_ON	O	FT	-	-	PWR_ONLP
-	F13	F17	VSS	S	-	-	-	-
-	P12	E12	VDD	S	-	-	-	-
E12	K14	E15	VDDQ_DDR	S	-	-	-	-
R15	R15	W19	DDR_DQ12	I/O	DDR	-	-	-
F12	M14	G15	VDDQ_DDR	S	-	-	-	-
T16	U15	Y20	DDR_DQ15	I/O	DDR	-	-	-
-	H5	A1	VSS	S	-	-	-	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
T17	T15	Y21	DDR_DQ14	I/O	DDR	-	-	-
-	H13	A21	VSS	S	-	-	-	-
P15	R16	W20	DDR_DQ11	I/O	DDR	-	-	-
G12	N13	G17	VDDQ_DDR	S	-	-	-	-
N14	R14	W21	DDR_DQM1	O	DDR	-	-	-
H12	N15	K15	VDDQ_DDR	S	-	-	-	-
R17	T16	V20	DDR_DQS1P	I/O	DDR	-	-	-
-	J16	AA1	VSS	S	-	-	-	-
R16	T17	V21	DDR_DQS1N	I/O	DDR	-	-	-
-	K5	AA21	VSS	S	-	-	-	-
-	K13	G14	VSS	S	-	-	-	-
M13	J13	T18	DDR_VREF	A	A	-	-	-
-	H6	J15	VDDCORE	S	-	-	-	-
J12	P14	K17	VDDQ_DDR	S	-	-	-	-
P16	T14	U19	DDR_DQ13	I/O	DDR	-	-	-
K12	-	M15	VDDQ_DDR	S	-	-	-	-
P17	R17	U20	DDR_DQ9	I/O	DDR	-	-	-
-	M5	D16	VSS	S	-	-	-	-
N15	U16	T19	DDR_DQ10	I/O	DDR	-	-	-
-	M13	E5	VSS	S	-	-	-	-
N16	P17	T20	DDR_DQ8	I/O	DDR	-	-	-
L12	-	M17	VDDQ_DDR	S	-	-	-	-
N17	P16	R20	DDR_ZQ	A	A	-	-	-
M16	-	P17	DDR_DTO1	O	DDR	-	-	-
M12	-	R15	VDDQ_DDR	S	-	-	-	-
M14	P15	R19	DDR_A4	O	DDR	-	-	-
L15	M16	P19	DDR_A8	O	DDR	-	-	-
M17	M15	R21	DDR_A6	O	DDR	-	-	-
-	N6	E6	VSS	S	-	-	-	-
L13	N17	P18	DDR_ATO	A	A	-	-	-
-	N9	E11	VSS	S	-	-	-	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
L14	-	-	DDR_DTO0	O	DDR	-	-	-
N12	-	R17	VDDQ_DDR	S	-	-	-	-
L16	M17	P20	DDR_BA1	O	DDR	-	-	-
-	-	U15	VDDQ_DDR	S	-	-	-	-
L17	L17	N19	DDR_A14	O	DDR	-	-	-
-	N10	E16	VSS	S	-	-	-	-
K13	L16	N17	DDR_A11	O	DDR	-	-	-
-	N12	F5	VSS	S	-	-	-	-
L8	N14	K11	VSS	S	-	-	-	-
K14	L13	N20	DDR_CKE	O	DDR	-	-	-
-	H12	L7	VDDCORE	S	-	-	-	-
K15	L15	N21	DDR_A1	O	DDR	-	-	-
K17	L14	M19	DDR_A12	O	DDR	-	-	-
K16	K15	M21	DDR_A15	O	DDR	-	-	-
-	N16	F18	VSS	S	-	-	-	-
J16	K16	M20	DDR_CLKP	O	DDR	-	-	-
-	P5	F21	VSS	S	-	-	-	-
J17	K17	L20	DDR_CLKN	O	DDR	-	-	-
-	H14	-	VDDQ_DDR	S	-	-	-	-
J14	J15	L18	DDR_A10	O	DDR	-	-	-
-	P13	G8	VSS	S	-	-	-	-
H17	J14	K20	DDR_RASN	O	DDR	-	-	-
J15	J17	L19	DDR_CASN	O	DDR	-	-	-
H13	H17	K19	DDR_WEN	O	DDR	-	-	-
-	U17	G12	VSS	S	-	-	-	-
P11	-	L12	VSS	S	-	-	-	-
-	-	H7	VSS	S	-	-	-	-
-	K12	L9	VDDCORE	S	-	-	-	-
H16	H16	J20	DDR_CSN	O	DDR	-	-	-
G17	H15	J19	DDR_BA0	O	DDR	-	-	-
J11	-	H15	VSS	S	-	-	-	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
H15	G17	J21	DDR_ODT	O	DDR	-	-	-
K3	-	J10	VSS	S	-	-	-	-
G16	G16	H20	DDR_A0	O	DDR	-	-	-
G15	G15	H19	DDR_A3	O	DDR	-	-	-
G14	F15	J17	DDR_A7	O	DDR	-	-	-
-	D14	-	VDDQ_DDR	S	-	-	-	-
F17	G13	G20	DDR_A2	O	DDR	-	-	-
-	E13	-	VDDQ_DDR	S	-	-	-	-
E16	F16	F20	DDR_A5	O	DDR	-	-	-
G13	G14	H18	DDR_BA2	O	DDR	-	-	-
F16	F17	G21	DDR_A9	O	DDR	-	-	-
K7	-	J12	VSS	S	-	-	-	-
F14	E17	G19	DDR_A13	O	DDR	-	-	-
K11	-	K9	VSS	S	-	-	-	-
E17	D15	H17	DDR_RESETN	O	DDR	-	-	-
-	E15	-	VDDQ_DDR	S	-	-	-	-
E15	D16	F19	DDR_DQ7	I/O	DDR	-	-	-
-	F14	-	VDDQ_DDR	S	-	-	-	-
E14	D17	E20	DDR_DQ6	I/O	DDR	-	-	-
L7	-	K10	VSS	S	-	-	-	-
R5	-	L15	VSS	S	-	-	-	-
L9	-	K12	VSS	S	-	-	-	-
-	M12	L13	VDDCORE	S	-	-	-	-
D17	C16	E19	DDR_DQ3	I/O	DDR	-	-	-
D16	C17	D20	DDR_DQ5	I/O	DDR	-	-	-
C17	B17	C20	DDR_DQS0P	I/O	DDR	-	-	-
L10	-	K13	VSS	S	-	-	-	-
C16	B16	C21	DDR_DQS0N	I/O	DDR	-	-	-
L11	-	K21	VSS	S	-	-	-	-
D15	C15	D21	DDR_DQM0	O	DDR	-	-	-
E13	C14	D19	DDR_DQ2	I/O	DDR	-	-	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
C15	B15	B20	DDR_DQ1	I/O	DDR	-	-	-
M15	-	L5	VSS	S	-	-	-	-
B17	A16	B21	DDR_DQ0	I/O	DDR	-	-	-
N4	-	L10	VSS	S	-	-	-	-
B16	A15	B19	DDR_DQ4	I/O	DDR	-	-	-
A16	G12	A20	PC9	I/O	FT_h	(5)	TRACED1, TIM3_CH4, TIM8_CH4, USART3_RTS, UART5_CTS, SDMMC1_D1	-
C12	A14	E17	VDDSD1	S	-	-	-	-
R8	-	L17	VSS	S	-	-	-	-
D14	C13	C18	PC8	I/O	FT_h	(5)	TRACED0, TIM3_CH3, TIM8_CH3, SPI3_MISO/I2S3_SDI, USART6_CK, USART3_CTS, SAI2_FS_B, UART5_RTS/UART5_DE, SDMMC1_D0(boot)	-
A15	G11	C19	PD2	I/O	FT_h	(5)	TRACED4, TIM3_ETR, I2C1_SMBA, SPI3_NSS/I2S3_WS, SAI2_D1, USART3_RX, SDMMC1_CMD(boot)	-
B15	B13	A19	PC12	I/O	FT_h	(5)	TRACECLK, UART7_TX, SAI2_SD_B, SDMMC1_CK(boot)	-
B14	F11	A18	PC10	I/O	FT_fh	(5)	TRACED2, I2C1_SCL, SPI3_SCK/I2S3_CK, USART3_TX, SAI2_MCLK_B, SDMMC1_D2	-
C14	C12	B18	PC11	I/O	FT_fh	(5)	TRACED3, I2C1_SDA, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_RX, SAI2_SCK_B, SDMMC1_D3	-
-	-	N10	VDDCORE	S	-	-	-	-
A14	H10	C17	PG6	I/O	FT_h	(6)	TRACED3, TIM17_BKIN, TIM5_CH4, SAI2_D1, USART1_RX, SAI2_SD_A, SDMMC2_CMD(boot), HDP3	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
D13	B12	B17	PE3	I/O	FT_h	(6)	TRACED11, SAI2_D4, TIM15_BKIN, SPI4_MISO/I2S4_SDI, USART3_RTS/USART3_DE, SDMMC2_CK(boot)	-
B13	E11	C16	PB4	I/O	FT_h	(6)	TRACED14, TIM16_BKIN, TIM3_CH1, SAI2_CK2, SPI4_SCK/I2S4_CK, USART3_CK, SDMMC2_D3, SAI2_SCK_A	-
A13	A12	B16	PB14	I/O	FT_h	(6)	TRACED0, TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SDMMC2_D0(boot), SDMMC1_D4	-
-	-	N13	VDDCORE	S	-	-	-	-
D11	A13	C15	VDDSD2	S	-	-	-	-
U1	-	M1	VSS	S	-	-	-	-
C11	B11	C14	PB3	I/O	FT_h	(6)	TRACED2, TIM2_CH2, SAI2_CK1, SPI4_NSS/I2S4_WS, SDMMC1_D123DIR, SDMMC2_D2, SAI2_MCLK_A, UART7_RX	-
B12	D11	B15	PB15	I/O	FT_h	(6)	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, SAI2_D2, SPI4_MOSI/I2S4_SDO, DFSDM1_CKIN2, UART7_CTS, SDMMC1_CKIN, SDMMC2_D1, SAI2_FS_A	-
U17	-	M7	VSS	S	-	-	-	-
C13	A11	A16	PF0	I/O	FT_h	-	TRACED13, DFSDM1_CKOUT, USART3_CK, SDMMC2_D4, FMC_A0	-
E11	C11	E14	PH10	I/O	FT_h	-	TRACED0, TIM5_CH1, SAI2_D3, DFSDM1_DATIN2, I2S3_MCK, SPI2_MOSI/I2S2_SDO, USART3_CTS/USART3_NSS, SDMMC1_D4, HDP0	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
A12	C10	A15	PB9	I/O	FT_fh	-	TRACED3, TIM4_CH4, I2C4_SDA, SDMMC2_D5, UART5_TX, SDMMC1_CDIR(boot)	-
-	D10	G9	VDD	S	-	-	-	-
-	-	M9	VSS	S	-	-	-	-
E10	B10	D14	PB13	I/O	FT_fh	-	TRACECLK, TIM1_CH1N, LPTIM2_OUT, SPI2_NSS/I2S2_WS, I2C4_SCL, SDMMC1_D123DIR, UART5_TX(boot)	-
D10	G10	E13	PB10	I/O	FT_h	-	TIM2_CH3, LPTIM2_IN1, I2C5_SMBA, SPI4_NSS/I2S4_WS, SPI2_SCK/I2S2_CK, USART3_TX(boot)	-
B11	A10	B14	PC6	I/O	FT_h	-	TRACED2, TIM3_CH1, TIM8_CH1, DFSDM1_DATIN0, I2S3_MCK, USART6_TX(boot), SDMMC1_D6, SDMMC2_D0DIR, SDMMC2_D6, FMC_A19, HDP2	-
C10	F9	B13	PB5	I/O	FT_h	-	TRACED4, TIM17_BKIN, TIM3_CH2, SPI2_MISO/I2S2_SDI, I2C4_SMBA, SDMMC1_CKIN, UART5_RX(boot)	-
A11	A9	C13	PC7	I/O	FT_h	-	TRACED4, TIM3_CH2, TIM8_CH2, I2S2_MCK, USART6_RX(boot), USART3_CTS, SDMMC2_CDIR, SDMMC2_D7, SDMMC1_D7, HDP4	-
B10	B9	A13	PF3	I/O	FT_fh	-	LPTIM2_IN2, I2C5_SDA, SPI4_MISO/I2S4_SDI, SPI3_NSS/I2S3_WS, FMC_A3	-
A9	D9	C12	PH9	I/O	FT_h	-	TIM1_CH4, TIM12_CH2, SPI4_SCK/I2S4_CK, FMC_A20	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
-	C6	G13	VDD	S	-	-	-	-
-	-	M10	VSS	S	-	-	-	-
B9	A8	B11	PF1	I/O	FT_fh	-	TRACED7, I2C2_SDA, SPI3_MOSI/I2S3_SDO, FMC_A1, HDP7	-
A10	E9	A12	PH13	I/O	FT_fh	-	TRACED15, USART2_CK, TIM8_CH1N, I2C5_SCL, SPI3_SCK/I2S3_CK, UART4_TX	-
C9	C8	A10	PG7	I/O	FT_h	-	TRACED8, TIM1_ETR, SPI3_MISO/I2S3_SDI, UART7_CTS, SDMMC2_CKIN	-
A8	C9	B10	PG4	I/O	FT_h	-	TRACED1, TIM1_BKIN2, DFSDM1_CKIN3, USART3_RX, SDMMC2_D123DIR, FMC_A14, HDP1	-
D9	A7	C11	PB12	I/O	FT_h	-	TRACED10, I2C2_SMBA, DFSDM1_DATIN1, UART7_RTS/UART7_DE, USART3_RX(boot), UART5_RX, SDMMC1_D5	-
E9	B7	D11	PF2	I/O	FT_fh	-	TRACED1, I2C2_SCL, DFSDM1_CKIN1, USART6_CK, SDMMC2_D0DIR, SDMMC1_D0DIR, FMC_A2	-
-	-	M11	VSS	S	-	-	-	-
-	-	J7	VDD	S	-	-	-	-
J6	F4	G10	VDDCPU	S	-	-	-	-
B8	C7	C10	PE10	I/O	FT	-	TIM1_CH2N, UART7_RX, FMC_D7(boot)/FMC_AD7	-
-	-	M12	VSS	S	-	-	-	-
D8	A6	A9	PE15	I/O	FT_fh	-	TIM2_ETR, TIM1_BKIN, USART2_CTS/USART2_NSS, I2C4_SCL, FMC_D12(boot)/FMC_AD12, HDP7	-
-	H4	-	VDDCPU	S	-	-	-	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
B7	B6	B8	PH14	I/O	FT_fh	-	DFSDM1_DATIN2, I2C3_SDA, UART4_RX	-
A7	F8	B9	PE8	I/O	FT_f	-	TIM1_CH1N, DFSDM1_CKIN2, I2C1_SDA, UART7_TX, FMC_D5(boot)/FMC_AD5	-
C7	A5	E9	PD15	I/O	FT_h	-	USART2_RX, TIM4_CH4, DFSDM1_DATIN2, QUADSPI_BK1_IO3, FMC_D1(boot)/FMC_AD1	-
E8	B5	C9	PD9	I/O	FT_h	-	TRACECLK, DFSDM1_DATIN3, SDMMC2_CDIR, FMC_D14(boot)/FMC_AD14	-
-	-	M13	VSS	S	-	-	-	-
D7	A4	A7	PG0	I/O	FT_h	-	FMC_A10	-
A6	B4	C8	PD5	I/O	FT_h	-	QUADSPI_BK1_IO0, FMC_NWE(boot)	-
-	-	J9	VDD	S	-	-	-	-
B6	A3	B7	PE9	I/O	FT_h	-	TIM1_CH1, QUADSPI_BK1_IO1, FMC_D6(boot)/FMC_AD6, HDP3	-
A5	C4	D8	PE7	I/O	FT_h	-	TIM1_ETR, LPTIM2_IN1, UART5_TX, FMC_D4(boot)/FMC_AD4	-
D6	B3	B6	PE0	I/O	FT_h	-	UART8_RX(boot), FMC_A11	-
C6	D7	A6	PD12	I/O	FT_f	-	LPTIM1_IN1, TIM4_CH1, I2C1_SCL, USART3_RTS/USART3_DE, FMC_ALE(boot)/FMC_A17	-
E7	A2	C7	PD4	I/O	FT_h	-	USART2_RTS/USART2_DE, SPI3_MISO/I2S3_SDI, DFSDM1_CKIN0, QUADSPI_CLK, FMC_NOE(boot)	-
C5	B2	B5	PD8	I/O	FT	-	USART2_TX, I2S4_WS, USART3_TX, UART4_RX(boot)	-
B5	C3	E8	PE1	I/O	FT_h	-	LPTIM1_IN2, UART8_TX(boot), FMC_NBL1	-

Table 7. STM32MP131C/F ball definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Ball functions	
LFBGA289	TFBGA289	TFBGA320					Alternate functions	Additional functions
A4	D5	C6	PB7	I/O	FT_f	-	TIM17_CH1N, TIM4_CH2, I2S4_CK, I2C4_SDA, FMC_NCE2, FMC_NL	-
B4	B1	A4	PE12	I/O	FT_h	-	TIM1_CH3N, SPI4_SCK/I2S4_CK, UART8_RTS/UART8_DE, FMC_D9(boot)/FMC_AD9, HDP4	-
-	-	K7	VDDCPU	S	-	-	-	-
D5	C2	C5	PD1	I/O	FT_fh	-	I2C5_SCL, SPI4_MOSI/I2S4_SDO, UART4_TX, QUADSPI_BK1_NCS, FMC_D3(boot)/FMC_AD3	-
-	-	K5	VDDCPU	S	-	-	-	-
A3	D3	D6	PD10	I/O	FT_h	-	RTC_REFIN, I2C5_SMBA, SPI4_NSS/I2S4_WS, USART3_CK, FMC_D15(boot)/FMC_AD15	-
E6	E7	B4	PA15	I/O	FT_h	-	TRACED5, TIM2_CH1, I2S4_MCK, UART4_RTS/UART4_DE, UART4_RX, FMC_A9, HDP5	-
C4	C1	A3	PE13	I/O	FT_fh	-	TIM1_CH3, I2C5_SDA, SPI4_MISO/I2S4_SDI, FMC_D10(boot)/FMC_AD10	-
B3	F7	C4	PD14	I/O	FT_fh	-	TIM4_CH3, I2C3_SDA, USART1_RX, UART8_CTS, FMC_D0(boot)/FMC_AD0	-
-	D12	-	VDD	S	-	-	-	-

1. Power supply is V_{BAT}.
2. During reset and when configured as alternate function for JTAG/SWD an internal pull-down is present.
3. During reset and when configured as alternate function for JTAG/SWD an internal pull-up is present.
4. During reset an internal pull-down is present.
5. Power supply is V_{DDSD1}.
6. Power supply is V_{DDSD2}.

Table 8. Alternate function AF0 to AF7

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		RTC/SYS	LPTIM1/RTC/ SPI5/SYS/ TIM1/2/16/17/ USART2	SAI1/2/SYS/ TIM1/3/4/5/12/ USART2	DFSDM1/ LPTIM2/3/4/5/ SAI2/TIM8/ USART2	DFSDM1/ I2C1/2/3/4/5/ LPTIM2/SAI1/2/ TIM15/USART1	I2C1/3/SPI1/ I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/ I2S4/SPI5	DFSDM1/I2C4/ SAI1/2/SPI1/I2 S1/SPI2/I2S2/S PI3/I2S3/SPI5	UART4/7/ USART1/2/3/6
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	TIM15_BKIN	-	SAI1_SD_B	-
	PA1	-	TIM2_CH2	TIM5_CH2	LPTIM3_OUT	TIM15_CH1N	-	DFSDM1_ CKIN0	USART2_RTS/ USART2_DE
	PA2	-	TIM2_CH3	TIM5_CH3	LPTIM4_OUT	TIM15_CH1	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	LPTIM5_OUT	TIM15_CH2	SPI1_MOSI/ I2S1_SDO	SAI1_FS_B	USART2_RX
	PA4	-	-	TIM5_ETR	USART2_CK	SAI1_SCK_B	SPI1_NSS/ I2S1_WS	DFSDM1_ CKIN1	-
	PA5	-	TIM2_CH1/ TIM2_ETR	USART2_CK	TIM8_CH1N	SAI1_D1	SPI1_NSS/ I2S1_WS	SAI1_SD_A	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	SAI2_CK2	SPI1_MISO/ I2S1_SDI	-	USART1_CK
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	SAI2_D1	SPI1_SCK/ I2S1_CK	-	USART1_CTS/ USART1_NSS
	PA8	MCO1	-	SAI2_MCLK_A	TIM8_BKIN2	I2C4_SDA	SPI5_MISO	SAI2_CK1	USART1_CK
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	DFSDM1_ DATIN0	USART1_TX
	PA10	-	TIM1_CH3	-	-	-	-	-	-
	PA11	-	TIM1_CH4	-	-	I2C5_SCL	SPI2_NSS/ I2S2_WS	-	USART1_CTS/ USART1_NSS
	PA12	-	TIM1_ETR	SAI2_MCLK_A	-	-	-	-	USART1_RTS/ USART1_DE
	PA13	DBTRGO	DBTRGI	MCO1	-	-	-	-	-

Table 8. Alternate function AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		RTC/SYS	LPTIM1/RTC/ SPI5/SYS/ TIM1/2/16/17/ USART2	SAI1/2/SYS/ TIM1/3/4/5/12/ USART2	DFSDM1/ LPTIM2/3/4/5/ SAI2/TIM8/ USART2	DFSDM1/ I2C1/2/3/4/5/ LPTIM2/SAI1/2/ TIM15/USART1	I2C1/3/SPI1/ I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/ I2S4/SPI5	DFSDM1/I2C4/ SAI1/2/SPI1/I2 S1/SPI2/I2S2/S PI3/I2S3/SPI5	UART4/7/ USART1/2/3/6
Port A	PA14	DBTRGO	DBTRGI	MCO2	-	-	-	-	-
	PA15	TRACED5	TIM2_CH1	-	-	-	I2S4_MCK	-	UART4_RTS/ UART4_DE
Port B	PB0	DBTRGI	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	USART1_RX	I2S1_MCK	SAI2_FS_A	USART1_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	SPI1_SCK/ I2S1_CK	DFSDM1_ DATIN1	UART4_RX
	PB2	-	RTC_OUT2	SAI1_D1	-	-	I2S_CKIN	SAI1_SD_A	-
	PB3	TRACED2	TIM2_CH2	-	-	SAI2_CK1	SPI4_NSS/ I2S4_WS	-	-
	PB4	TRACED14	TIM16_BKIN	TIM3_CH1	-	SAI2_CK2	SPI4_SCK/ I2S4_CK	-	USART3_CK
	PB5	TRACED4	TIM17_BKIN	TIM3_CH2	-	-	SPI2_MISO/ I2S2_SDI	I2C4_SMBA	-
	PB6	TRACED6	TIM16_CH1N	TIM4_CH1	TIM8_CH1	USART1_TX	-	SAI1_CK2	-
	PB7	-	TIM17_CH1N	TIM4_CH2	-	-	I2S4_CK	I2C4_SDA	-
	PB8	-	TIM16_CH1	TIM4_CH3	-	I2C1_SCL	I2C3_SCL	DFSDM1_ DATIN1	-
	PB9	TRACED3	-	TIM4_CH4	-	-	-	I2C4_SDA	-
	PB10	-	TIM2_CH3	-	LPTIM2_IN1	I2C5_SMBA	SPI4_NSS/ I2S4_WS	SPI2_SCK/ I2S2_CK	USART3_TX
	PB11	-	TIM2_CH4	-	LPTIM1_OUT	I2C5_SMBA	-	-	USART3_RX
	PB12	TRACED10	-	-	-	I2C2_SMBA	-	DFSDM1_ DATIN1	UART7_RTS/ UART7_DE

Table 8. Alternate function AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		RTC/SYS	LPTIM1/RTC/ SPI5/SYS/ TIM1/2/16/17/ USART2	SAI1/2/SYS/ TIM1/3/4/5/12/ USART2	DFSDM1/ LPTIM2/3/4/5/ SAI2/TIM8/ USART2	DFSDM1/ I2C1/2/3/4/5/ LPTIM2/SAI1/2/ TIM15/USART1	I2C1/3/SPI1/ I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/ I2S4/SPI5	DFSDM1/I2C4/ SAI1/2/SPI1/I2 S1/SPI2/I2S2/S PI3/I2S3/SPI5	UART4/7/ USART1/2/3/6
Port B	PB13	TRACECLK	TIM1_CH1N	-	-	LPTIM2_OUT	SPI2_NSS/ I2S2_WS	I2C4_SCL	-
	PB14	TRACED0	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	-	-	-
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	SAI2_D2	SPI4_MOSI/ I2S4_SDO	DFSDM1_ CKIN2	UART7_CTS
Port C	PC0	-	-	SAI1_SCK_A	-	SAI1_CK2	I2S1_MCK	SPI1_MOSI/ I2S1_SDO	USART1_TX
	PC1	-	-	-	DFSDM1_ DATIN0	-	-	SAI1_D3	-
	PC2	-	SPI5_NSS	-	-	-	SPI1_NSS/ I2S1_WS	SAI2_MCLK_A	USART1_RTS/ USART1_DE
	PC3	-	-	SAI1_CK1	DFSDM1_ CKOUT	-	SPI1_MISO/ I2S1_SDI	SPI1_SCK/ I2S1_CK	-
	PC4	-	-	TIM3_ETR	DFSDM1_ CKIN2	SAI1_D3	I2S1_MCK	-	-
	PC5	-	-	-	DFSDM1_ DATIN2	SAI2_D4	I2S_CKIN	SAI1_D4	USART2_CTS/ USART2_NSS
	PC6	TRACED2	-	TIM3_CH1	TIM8_CH1	DFSDM1_ DATIN0	I2S3_MCK	-	USART6_TX
	PC7	TRACED4	-	TIM3_CH2	TIM8_CH2	-	-	I2S2_MCK	USART6_RX
	PC8	TRACED0	-	TIM3_CH3	TIM8_CH3	-	SPI3_MISO/ I2S3_SDI	-	USART6_CK
	PC9	TRACED1	-	TIM3_CH4	TIM8_CH4	-	-	-	USART3_RTS

Table 8. Alternate function AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		RTC/SYS	LPTIM1/RTC/ SPI5/SYS/ TIM1/2/16/17/ USART2	SAI1/2/SYS/ TIM1/3/4/5/12/ USART2	DFSDM1/ LPTIM2/3/4/5/ SAI2/TIM8/ USART2	DFSDM1/ I2C1/2/3/4/5/ LPTIM2/SAI1/2/ TIM15/USART1	I2C1/3/SPI1/ I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/ I2S4/SPI5	DFSDM1/I2C4/ SAI1/2/SPI1/I2 S1/SPI2/I2S2/S PI3/I2S3/SPI5	UART4/7/ USART1/2/3/6
Port C	PC10	TRACED2	-	-	-	-	I2C1_SCL	SPI3_SCK/ I2S3_CK	USART3_TX
	PC11	TRACED3	-	-	-	I2C1_SDA	-	SPI3_MOSI/ I2S3_SDO	USART3_CK
	PC12	TRACECLK	-	-	-	-	-	-	-
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-
Port D	PD0	-	-	SAI1_MCLK_A	-	-	-	SAI1_CK1	-
	PD1	-	-	-	-	I2C5_SCL	SPI4_MOSI/ I2S4_SDO	-	-
	PD2	TRACED4	-	TIM3_ETR	-	I2C1_SMBA	SPI3_NSS/ I2S3_WS	SAI2_D1	USART3_RX
	PD3	-	-	TIM2_CH1	USART2_CTS/ USART2_NSS	DFSDM1_ CKOUT	I2C1_SDA	SAI1_D3	-
	PD4	-	-	-	USART2_RTS/ USART2_DE	-	SPI3_MISO/ I2S3_SDI	DFSDM1_ CKIN0	-
	PD5	-	-	-	-	-	-	-	-
	PD6	-	TIM16_CH1N	SAI1_D1	-	-	-	SAI1_SD_A	-
	PD7	MCO1	-	-	USART2_CK	I2C2_SCL	I2C3_SDA	-	-
	PD8	-	-	-	USART2_TX	-	I2S4_WS	-	USART3_TX
	PD9	TRACECLK	-	-	DFSDM1_ DATIN3	-	-	-	-

Table 8. Alternate function AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		RTC/SYS	LPTIM1/RTC/ SPI5/SYS/ TIM1/2/16/17/ USART2	SAI1/2/SYS/ TIM1/3/4/5/12/ USART2	DFSDM1/ LPTIM2/3/4/5/ SAI2/TIM8/ USART2	DFSDM1/ I2C1/2/3/4/5/ LPTIM2/SAI1/2/ TIM15/USART1	I2C1/3/SPI1/ I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/ I2S4/SPI5	DFSDM1/I2C4/ SAI1/2/SPI1/I2 S1/SPI2/I2S2/S PI3/I2S3/SPI5	UART4/7/ USART1/2/3/6
Port D	PD10	RTC_REFIN	-	-	-	I2C5_SMBA	SPI4_NSS/ I2S4_WS	-	USART3_CK
	PD11	-	-	-	LPTIM2_IN2	I2C4_SMBA	-	-	USART3_CTS/ USART3_NSS
	PD12	-	LPTIM1_IN1	TIM4_CH1	-	-	I2C1_SCL	-	USART3_RTS/ USART3_DE
	PD13	-	LPTIM2_ETR	TIM4_CH2	TIM8_CH2	SAI1_CK1	-	SAI1_MCLK_A	USART1_RX
	PD14	-	-	TIM4_CH3	-	I2C3_SDA	-	-	USART1_RX
	PD15	-	USART2_RX	TIM4_CH4	DFSDM1_ DATIN2	-	-	-	-
Port E	PE0	-	-	-	-	-	-	-	-
	PE1	-	LPTIM1_IN2	-	-	-	-	-	-
	PE2	TRACECLK	TIM2_ETR	-	-	I2C4_SCL	SPI5_MOSI	SAI1_FS_B	USART6_RTS/ USART6_DE
	PE3	TRACED11	-	SAI2_D4	-	TIM15_BKIN	SPI4_MISO/ I2S4_SDI	-	-
	PE4	-	SPI5_MISO	SAI1_D2	DFSDM1_ DATIN3	TIM15_CH1N	I2S_CKIN	SAI1_FS_A	UART7_RTS/U ART7_DE
	PE5	-	-	SAI2_SCK_B	TIM8_CH3	TIM15_CH1	-	-	-
	PE6	MCO2	TIM1_BKIN2	SAI2_SCK_B	-	TIM15_CH2	I2C3_SMBA	SAI1_SCK_B	-
	PE7	-	TIM1_ETR	-	-	LPTIM2_IN1	-	-	-
	PE8	-	TIM1_CH1N	-	DFSDM1_ CKIN2	-	I2C1_SDA	-	UART7_TX

Table 8. Alternate function AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		RTC/SYS	LPTIM1/RTC/ SPI5/SYS/ TIM1/2/16/17/ USART2	SAI1/2/SYS/ TIM1/3/4/5/12/ USART2	DFSDM1/ LPTIM2/3/4/5/ SAI2/TIM8/ USART2	DFSDM1/ I2C1/2/3/4/5/ LPTIM2/SAI1/2/ TIM15/USART1	I2C1/3/SPI1/ I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/ I2S4/SPI5	DFSDM1/I2C4/ SAI1/2/SPI1/I2 S1/SPI2/I2S2/S PI3/I2S3/SPI5	UART4/7/ USART1/2/3/6
Port E	PE9	-	TIM1_CH1	-	-	-	-	-	-
	PE10	-	TIM1_CH2N	-	-	-	-	-	UART7_RX
	PE11	-	TIM1_CH2	USART2_CTS/ USART2_NSS	-	SAI1_D2	SPI4_MOSI/ I2S4_SDO	SAI1_FS_A	USART6_CK
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK/ I2S4_CK	-	-
	PE13	-	TIM1_CH3	-	-	I2C5_SDA	SPI4_MISO/ I2S4_SDI	-	-
	PE14	-	TIM1_BKIN	-	-	SAI1_D4	-	-	-
	PE15	-	TIM2_ETR	TIM1_BKIN	USART2_CTS/ USART2_NSS	-	-	I2C4_SCL	-
Port F	PF0	TRACED13	-	-	DFSDM1_ CKOUT	-	-	-	USART3_CK
	PF1	TRACED7	-	-	-	I2C2_SDA	SPI3_MOSI/ I2S3_SDO	-	-
	PF2	TRACED1	-	-	-	I2C2_SCL	-	DFSDM1_ CKIN1	USART6_CK
	PF3	-	-	-	LPTIM2_IN2	I2C5_SDA	SPI4_MISO/ I2S4_SDI	SPI3_NSS/ I2S3_WS	-
	PF4	-	-	-	USART2_RX	-	-	-	-
	PF5	TRACED12	-	-	-	DFSDM1_ CKIN0	I2C1_SMBA	-	-
	PF6	-	TIM16_CH1	-	-	-	SPI5_NSS	-	UART7_RX

Table 8. Alternate function AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		RTC/SYS	LPTIM1/RTC/ SPI5/SYS/ TIM1/2/16/17/ USART2	SAI1/2/SYS/ TIM1/3/4/5/12/ USART2	DFSDM1/ LPTIM2/3/4/5/ SAI2/TIM8/ USART2	DFSDM1/ I2C1/2/3/4/5/ LPTIM2/SAI1/2/ TIM15/USART1	I2C1/3/SPI1/ I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/ I2S4/SPI5	DFSDM1/I2C4/ SAI1/2/SPI1/I2 S1/SPI2/I2S2/S PI3/I2S3/SPI5	UART4/7/ USART1/2/3/6
Port F	PF7	-	TIM17_CH1	-	-	-	-	-	UART7_TX
	PF8	-	TIM16_CH1N	TIM4_CH3	TIM8_CH3	-	-	SAI1_SCK_B	USART6_TX
	PF9	-	TIM17_CH1N	TIM1_CH1	DFSDM1_CKIN 3	-	-	SAI1_D4	UART7_CTS
	PF10	-	TIM16_BKIN	SAI1_D3	TIM8_BKIN	-	SPI5_NSS	-	USART6_RTS/ USART6_DE
	PF11	-	USART2_TX	SAI1_D2	DFSDM1_ CKIN3	-	-	SAI1_FS_A	-
	PF12	-	-	-	-	-	SPI1_NSS/ I2S1_WS	SAI1_SD_A	-
	PF13	-	TIM2_ETR	SAI1_MCLK_B	-	-	-	DFSDM1_ DATIN3	USART2_TX
	PF14	JTCK/SWCLK	-	-	-	-	-	-	-
	PF15	JTMS/SWDIO	-	-	-	-	-	-	-
Port G	PG0	-	-	-	-	-	-	-	-
	PG1	-	LPTIM1_ETR	TIM4_ETR	SAI2_FS_A	I2C2_SMBA	SPI2_MISO/ I2S2_SDI	SAI2_D2	-
	PG2	-	MCO2	-	TIM8_BKIN	-	-	-	-
	PG3	-	-	-	TIM8_BKIN2	I2C2_SDA	-	SAI2_SD_B	-
	PG4	TRACED1	TIM1_BKIN2	-	-	DFSDM1_ CKIN3	-	-	-
	PG5	-	TIM17_CH1	-	-	-	-	-	-
	PG6	TRACED3	TIM17_BKIN	TIM5_CH4	SAI2_D1	USART1_RX	-	SAI2_SD_A	-

Table 8. Alternate function AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		RTC/SYS	LPTIM1/RTC/ SPI5/SYS/ TIM1/2/16/17/ USART2	SAI1/2/SYS/ TIM1/3/4/5/12/ USART2	DFSDM1/ LPTIM2/3/4/5/ SAI2/TIM8/ USART2	DFSDM1/ I2C1/2/3/4/5/ LPTIM2/SAI1/2/ TIM15/USART1	I2C1/3/SPI1/ I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/ I2S4/SPI5	DFSDM1/I2C4/ SAI1/2/SPI1/I2 S1/SPI2/I2S2/S PI3/I2S3/SPI5	UART4/7/ USART1/2/3/6
Port G	PG7	TRACED8	TIM1_ETR	-	-	-	SPI3_MISO/ I2S3_SDI	-	-
	PG8	-	TIM2_CH1	-	TIM8_ETR	-	SPI5_MISO	SAI1_MCLK_B	-
	PG9	DBTRGO	-	-	-	I2C2_SDA	-	-	USART6_RX
	PG10	-	-	-	-	-	SPI5_SCK	SAI1_SD_B	-
	PG11	-	-	-	-	SAI2_D3	I2S2_MCK	-	USART3_TX
	PG12	-	LPTIM1_IN1	-	-	SAI2_SCK_A	-	SAI2_CK2	USART6_RTS/ USART6_DE
	PG13	-	LPTIM1_OUT	-	-	-	-	-	USART6_CTS/ USART6_NSS
	PG14	-	LPTIM1_ETR	-	-	-	-	SAI2_D1	USART6_TX
	PG15	-	-	-	-	-	-	-	USART6_CTS/ USART6_NSS
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH2	-	LPTIM1_IN2	-	-	-	-	-	-
	PH3	-	-	-	-	I2C3_SCL	SPI5_MOSI	-	-
	PH4	JTDI	-	-	-	-	-	-	-
	PH5	JTDO	-	-	-	-	-	-	-
	PH6	-	-	TIM12_CH1	USART2_CK	I2C5_SDA	SPI2_SCK/ I2S2_CK	-	-
	PH7	-	-	SAI2_FS_B	-	-	I2C3_SDA	SPI5_SCK	-

Table 8. Alternate function AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		RTC/SYS	LPTIM1/RTC/ SPI5/SYS/ TIM1/2/16/17/ USART2	SAI1/2/SYS/ TIM1/3/4/5/12/ USART2	DFSDM1/ LPTIM2/3/4/5/ SAI2/TIM8/ USART2	DFSDM1/ I2C1/2/3/4/5/ LPTIM2/SAI1/2/ TIM15/USART1	I2C1/3/SPI1/ I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/ I2S4/SPI5	DFSDM1/I2C4/ SAI1/2/SPI1/I2 S1/SPI2/I2S2/S PI3/I2S3/SPI5	UART4/7/ USART1/2/3/6
Port H	PH8	TRACED9	-	TIM5_ETR	USART2_RX	I2C3_SDA	-	-	-
	PH9	-	TIM1_CH4	TIM12_CH2	-	-	SPI4_SCK/ I2S4_CK	-	-
	PH10	TRACED0	-	TIM5_CH1	SAI2_D3	DFSDM1_ DATIN2	I2S3_MCK	SPI2_MOSI/ I2S2_SDO	USART3_CTS/ USART3_NSS
	PH11	-	SPI5_NSS	TIM5_CH2	SAI2_SD_A	-	SPI2_NSS/ I2S2_WS	I2C4_SCL	USART6_RX
	PH12	-	USART2_TX	TIM5_CH3	DFSDM1_ CKIN1	I2C3_SCL	SPI5_MOSI	SAI1_SCK_A	-
	PH13	TRACED15	-	USART2_CK	TIM8_CH1N	I2C5_SCL	-	SPI3_SCK/ I2S3_CK	-
	PH14	-	-	-	DFSDM1_ DATIN2	I2C3_SDA	-	-	-
Port I	PI0	-	-	-	-	-	-	-	-
	PI1	-	-	-	-	-	-	-	-
	PI2	-	-	-	-	-	-	-	-
	PI3	-	-	-	-	-	-	-	-
	PI4	BOOT0	-	-	-	-	-	-	-
	PI5	BOOT1	-	-	-	-	-	-	-
	PI6	BOOT2	-	-	-	-	-	-	-
	PI7	-	-	-	-	-	-	-	-

Table 9. Alternate function AF8 to AF15

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port A	PA0	UART5_TX	-	-	ETH1_MII_CRS	-	-	-	-
	PA1	-	-	-	ETH1_MII_RX_CLK/ ETH1_RGMII_RX_CLK/ ETH1_RMII_REF_CLK	-	-	-	-
	PA2	-	-	-	ETH1_MDIO	-	-	-	-
	PA3	-	-	-	ETH1_MII_COL	-	-	-	-
	PA4	-	-	ETH1_PPS_OUT	-	SAI1_SCK_A	-	-	-
	PA5	-	-	ETH1_PPS_OUT	-	-	-	-	-
	PA6	UART4_RTS/ UART4_DE	TIM13_CH1	-	-	SAI2_SCK_A	-	-	-
	PA7	-	TIM14_CH1	-	ETH1_MII_RX_DV/ ETH1_RGMII_RX_CTL/ ETH1_RMII_CRS_DV	SAI2_SD_A	-	-	-
	PA8	SPI2_MOSI/ I2S2_SDO	-	OTG_HS_SOF	-	FMC_A21	-	-	-
	PA9	UART4_TX	-	FMC_NWAIT	-	-	-	-	-
	PA10	-	-	-	-	-	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port A	PA11	-	-	-	ETH1_CLK	-	-	-	-
	PA12	-	-	-	-	FMC_A7	-	-	-
	PA13	UART4_TX	-	-	-	-	-	-	-
	PA14	-	-	OTG_HS_SOF	-	-	-	-	-
	PA15	UART4_RX	-	-	-	FMC_A9	-	-	HDP5
Port B	PB0	UART4_CTS	-	SAI2_D2	ETH1_MII_ RXD2/ ETH1_RGMII_ RXD2	-	-	-	-
	PB1	-	-	-	ETH1_MII_ RXD3/ ETH1_RGMII_ RXD3	-	-	-	-
	PB2	UART4_RX	QUADSPI_ BK1_NCS	-	-	FMC_A6	-	-	-
	PB3	SDMMC1_ D123DIR	-	SDMMC2_D2	-	SAI2_MCLK_A	UART7_RX	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port B	PB4	-	-	SDMMC2_D3	-	SAI2_SCK_A	-	-	-
	PB5	SDMMC1_ CKIN	-	-	UART5_RX	-	-	-	-
	PB6	-	QUADSPI_ BK1_NCS	-	-	FMC_NE3	-	-	HDP6
	PB7	-	-	FMC_NCE2	-	FMC_NL	-	-	-
	PB8	UART4_RX	-	SAI1_D1	-	FMC_D13/FMC _AD13	-	-	-
	PB9	-	-	SDMMC2_D5	UART5_TX	SDMMC1_ CDIR	-	-	-
	PB10	-	-	-	-	-	-	-	-
	PB11	-	-	-	ETH1_MII_TX_ EN/ ETH1_RGMII_ TX_CTL/ ETH1_RMII_TX _EN	-	-	-	-
	PB12	USART3_RX	-	-	UART5_RX	SDMMC1_D5	-	-	-
	PB13	SDMMC1_ D123DIR	-	-	UART5_TX	-	-	-	-
	PB14	-	-	SDMMC2_D0	SDMMC1_D4	-	-	-	-
Port B	PB15	SDMMC1_ CKIN	-	SDMMC2_D1	-	SAI2_FS_A	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port C	PC0	-	-	-	-	-	-	-	-
	PC1	-	-	ETH1_MII_RX_DV/ ETH1_RMII_CRS_DV	ETH1_RGMII_GTX_CLK	-	-	-	-
	PC2	-	-	SAI2_CK1	ETH1_MII_TXD2/ ETH1_RGMII_TXD2	-	-	-	-
	PC3	UART5_CTS	-	SAI1_MCLK_A	ETH1_MII_TX_CLK	-	-	-	-
	PC4	UART5_RTS/ UART5_DE	SPDIFRX_IN2	-	ETH1_MII_RXD0/ ETH1_RGMII_RXD0/ ETH1_RMII_RXD0	SAI2_D3	-	-	-
	PC5	-	SPDIFRX_IN3	-	ETH1_MII_RXD1/ ETH1_RGMII_RXD1/ ETH1_RMII_RXD1	-	-	-	-
	PC6	SDMMC1_D6	SDMMC2_D0DIR	SDMMC2_D6	-	FMC_A19	-	-	HDP2

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port C	PC7	USART3_CTS	SDMMC2_ CDIR	SDMMC2_D7	-	SDMMC1_D7	-	-	HDP4
	PC8	USART3_CTS	-	SAI2_FS_B	UART5_RTS/ UART5_DE	SDMMC1_D0	-	-	-
	PC9	UART5_CTS	-	-	-	SDMMC1_D1	-	-	-
	PC10	-	-	SAI2_MCLK_B	-	SDMMC1_D2	-	-	-
	PC11	UART5_RX	-	SAI2_SCK_B	-	SDMMC1_D3	-	-	-
	PC12	UART7_TX	-	SAI2_SD_B	-	SDMMC1_CK	-	-	-
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-
Port D	PD0	-	-	-	-	FMC_D2/ FMC_AD2	-	-	-
	PD1	UART4_TX	QUADSPI_BK1 _NCS	-	-	FMC_D3/ FMC_AD3	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port D	PD2	-	-	-	-	SDMMC1_CMD	-	-	-
	PD3	-	-	-	-	FMC_CLK	-	-	-
	PD4	-	QUADSPI_CLK	-	-	FMC_NOE	-	-	-
	PD5	-	QUADSPI_BK1 _IO0	-	-	FMC_NWE	-	-	-
	PD6	UART4_TX	-	-	-	-	-	-	-
	PD7	-	SPDIFRX_IN0	ETH1_MII_RX_ CLK/ ETH1_RGMII_ RX_CLK/ ETH1_RMII_ REF_CLK	QUADSPI_BK1 _IO2	FMC_NE1	-	-	-
	PD8	UART4_RX	-	-	-	-	-	-	-
	PD9	-	-	SDMMC2_ CDIR	-	FMC_D14/ FMC_AD14	-	-	-
	PD10	-	-	-	-	FMC_D15/ FMC_AD15	-	-	-
	PD11	SPDIFRX_IN0	QUADSPI_BK1 _IO2	-	-	FMC_CLE/FMC _A16	UART7_RX	-	-
	PD12	-	-	-	-	FMC_ALE/FMC _A17	-	-	-
	PD13	-	QUADSPI_BK1 _IO3	-	QUADSPI_BK2 _IO2	FMC_A18	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port D	PD14	UART8_CTS	-	-	-	FMC_D0/FMC_ AD0	-	-	-
	PD15	-	QUADSPI_BK1 _IO3	-	-	FMC_D1/FMC_ AD1	-	-	-
Port E	PE0	UART8_RX	-	-	-	FMC_A11	-	-	-
	PE1	UART8_TX	-	-	-	FMC_NBL1	-	-	-
	PE2	-	SPDIFRX_IN1	-	-	FMC_A23	-	-	-
	PE3	USART3_RTS/ USART3_DE	-	SDMMC2_CK	-	-	-	-	-
	PE4	UART8_TX	QUADSPI_BK2 _NCS	FMC_NCE2	-	FMC_A25	-	-	-
	PE5	UART4_RX	-	ETH1_MII_ TXD3/ ETH1_RGMII_ TXD3	-	FMC_NE1	-	-	-
	PE6	UART4_RTS/ UART4_DE	-	-	-	FMC_A22	-	-	-
	PE7	UART5_TX	-	-	-	FMC_D4/ FMC_AD4	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port E	PE8	-	-	-	-	FMC_D5/ FMC_AD5	-	-	-
	PE9	-	QUADSPI_BK1 _IO1	-	-	FMC_D6/ FMC_AD6	-	-	HDP3
	PE10	-	-	-	-	FMC_D7/ FMC_AD7	-	-	-
	PE11	-	-	-	ETH1_MII_TX_ ER	FMC_D8/ FMC_AD8	-	-	-
	PE12	UART8_RTS/ UART8_DE	-	-	-	FMC_D9/ FMC_AD9	-	-	HDP4
	PE13	-	-	-	-	FMC_D10/ FMC_AD10	-	-	-
	PE14	UART8_RTS/ UART8_DE	QUADSPI_BK1 _NCS	QUADSPI_BK2 _IO2	-	FMC_D11/ FMC_AD11	-	-	-
	PE15	-	-	-	-	FMC_D12/ FMC_AD12	-	-	HDP7
Port F	PF0	-	-	SDMMC2_D4	-	FMC_A0	-	-	-
	PF1	-	-	-	-	FMC_A1	-	-	HDP7
	PF2	-	SDMMC2_ D0DIR	-	SDMMC1_ D0DIR	FMC_A2	-	-	-
	PF3	-	-	-	-	FMC_A3	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port F	PF4	-	-	-	-	FMC_A4	-	-	-
	PF5	-	-	-	-	FMC_A5	-	-	-
	PF6	-	QUADSPI_BK1 _IO2	-	-	-	-	-	-
	PF7	UART4_CTS	-	ETH1_RGMII_ CLK125	-	FMC_A18	-	-	-
	PF8	-	TIM13_CH1	QUADSPI_BK1 _IO0	-	-	-	-	-
	PF9	UART8_RX	TIM14_CH1	QUADSPI_BK1 _IO1	QUADSPI_BK2 _IO3	FMC_A9	-	-	-
	PF10	UART7_RTS/ UART7_DE	QUADSPI_CLK	-	-	-	-	-	-
	PF11	-	-	-	-	-	-	-	-
Port F	PF12	UART4_TX	-	ETH1_MII_TX_ ER	ETH1_RGMII_ CLK125	-	-	-	-
	PF13	UART5_RX	-	-	-	-	-	-	-
	PF14	-	-	-	-	-	-	-	-
	PF15	-	-	-	-	-	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port G	PG0	-	-	-	-	FMC_A10	-	-	-
	PG1	-	-	-	-	FMC_NBL0	-	-	-
	PG2	-	-	SAI2_MCLK_B	ETH1_MDC	-	-	-	-
	PG3	-	-	-	ETH1_MDIO	FMC_A13	-	-	-
	PG4	USART3_RX	-	SDMMC2_ D123DIR	-	FMC_A14	-	-	HDP1
	PG5	-	-	-	-	FMC_A15	-	-	-
	PG6	-	-	SDMMC2_CMD	-	-	-	-	HDP3
	PG7	UART7_CTS	-	SDMMC2_ CKIN	-	-	-	-	-
	PG8	USART3_RTS/ USART3_DE	SPDIFRX_IN2	QUADSPI_BK2 _IO2	QUADSPI_BK1 _IO3	FMC_NE2	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port G	PG9	SPDIFRX_IN3	-	FMC_NE2	-	FMC_NCE	-	-	-
	PG10	UART8_CTS	-	QUADSPI_BK2 _IO1	-	FMC_NE3	-	-	-
	PG11	UART4_TX	-	-	-	FMC_A24	-	-	-
	PG12	USART3_CTS	-	-	ETH1_PHY_ INTN	-	-	-	-
	PG13	-	-	-	ETH1_MII_ TXD0/ ETH1_RGMII_ TXD0/ ETH1_RMII_ TXD0	-	-	-	-
	PG14	-	-	SAI2_SD_A	ETH1_MII_ TXD1/ ETH1_RGMII_ TXD1/ ETH1_RMII_ TXD1	-	-	-	-
Port G	PG15	UART7_CTS	QUADSPI_BK1 _IO1	-	-	-	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH2	UART7_TX	QUADSPI_BK2 _IO0	-	ETH1_MII_CRS	FMC_NE4	-	-	-
	PH3	-	QUADSPI_BK2 _IO1	ETH1_MII_COL	-	-	QUADSPI_BK1 _IO0	-	-
	PH4	-	-	-	-	-	-	-	-
	PH5	-	-	-	-	-	-	-	-
	PH6	-	QUADSPI_BK1 _IO2	ETH1_PHY_IN TN	ETH1_MII_RX_ ER	-	QUADSPI_BK1 _NCS	-	-
	PH7	-	QUADSPI_BK2 _IO3	-	ETH1_MII_TX_ CLK	-	QUADSPI_BK1 _IO3	-	-
	PH8	-	-	-	-	FMC_A8	-	-	HDP2
	PH9	-	-	-	-	FMC_A20	-	-	-
	PH10	SDMMC1_D4	-	-	-	-	-	-	HDP0
Port H	PH11	-	QUADSPI_BK2 _IO0	-	-	FMC_A12	-	-	-
	PH12	-	QUADSPI_BK2 _IO2	SAI1_CK2	ETH1_MII_CRS	FMC_A6	-	-	-
	PH13	UART4_TX	-	-	-	-	-	-	-
	PH14	UART4_RX	-	-	-	-	-	-	-

Table 9. Alternate function AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SDMMC1/ SPDIFRX/SPI2/ I2S2/ UART4/5/7/8/ USART3	QUADSPI/ SDMMC2/ SPDIFRX/ TIM13/14	ETH1/FMC/ OTG_HS/ QUADSPI/ SAI1/2/ SDMMC2	ETH1/ QUADSPI/ SDMMC1/ UART5	FMC/ SAI1/2/ SDMMC1	QUADSPI/ UART7		HDP/SYS
Port I	PI0	SPDIFRX_IN0	-	-	-	-	-	-	-
	PI1	SPDIFRX_IN1	-	-	-	-	-	-	-
	PI2	SPDIFRX_IN2	-	-	-	-	-	-	-
	PI3	SPDIFRX_IN3	-	-	ETH1_MII_RX_ ER	-	-	-	-
	PI4	-	-	-	-	-	-	-	-
	PI5	-	-	-	-	-	-	-	-
	PI6	-	-	-	-	-	-	-	-
	PI7	-	-	-	-	-	-	-	-

5 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 °C and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V, V_{DDCORE} = 1.25 V, V_{DDCPU} = 1.25 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

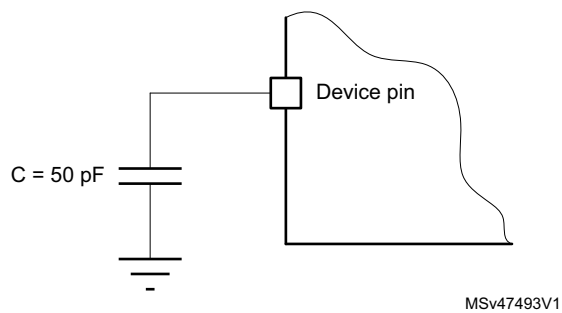
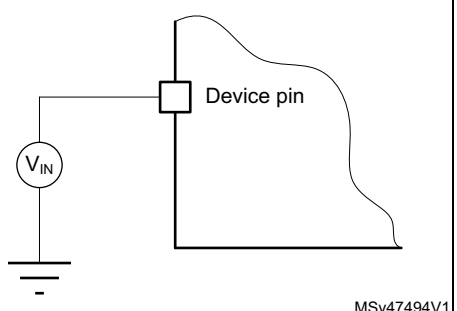
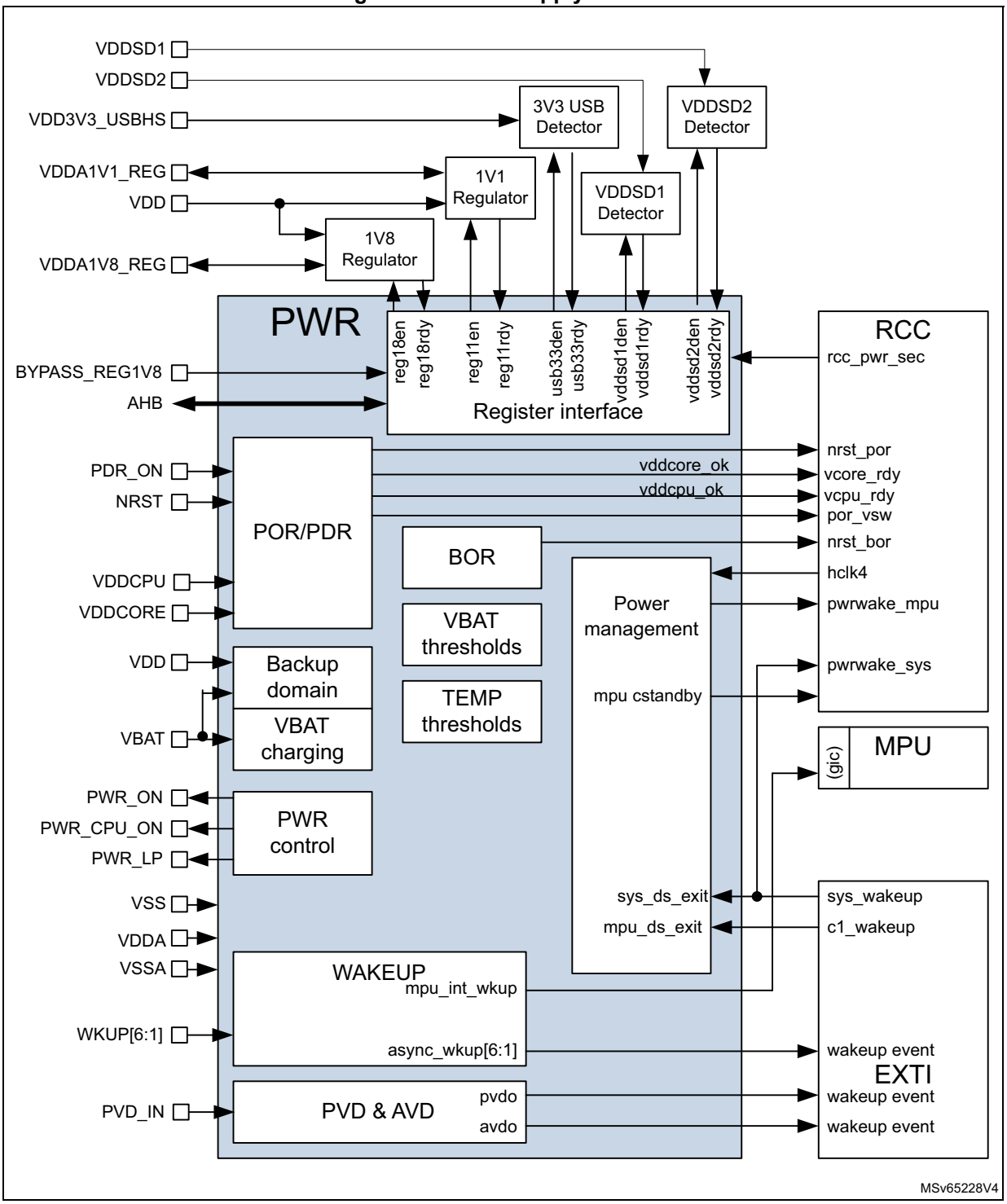


Figure 9. Pin input voltage



6.1.6 Power supply scheme

Figure 10. Power supply scheme

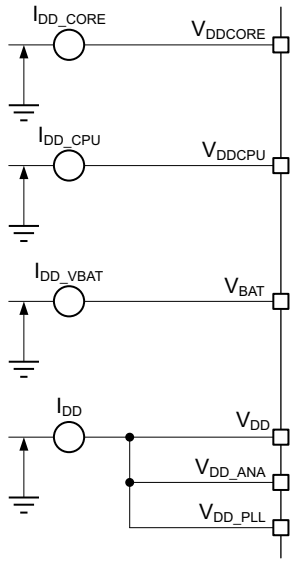


Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDSDx}/V_{SS}, V_{DDCORE}/V_{SS}, V_{DDCPU}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure

good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 10: Voltage characteristics*, *Table 11: Current characteristics*, and *Table 12: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 10. Voltage characteristics (1)

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SSX}	External main supply voltage (including V_{DD}, V_{DDSD1}, V_{DDSD2}, V_{DD_ANA}, V_{DD_PLL}, V_{DDA}, V_{DD3V3_USBHS}, V_{BAT}, V_{REF+})	-0.3	3.9	V
V_{DDCORE} - V_{SS}	External core supply voltage	-0.3	1.5	V
V_{DDCPU} - V_{SS}	External Cortex®-A7 CPU supply voltage	-0.3	1.5	V
V_{DDA_DDR} - V_{SS}	DDR IO supply voltage	-0.3	1.98	V

Table 10. Voltage characteristics (continued)(1)

Symbols	Ratings	Min	Max	Unit
V_{DDA1V8} - V_{SS}	1.8 V supply (V_{DDA1V8_REG})	-0.3	3.9	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS} - 0.3	(3)	V
	Input voltage on TT_xx pins		3.9	V
	Input voltage on USB/OTG_HS_DP/DM pins		(4)	V
	Input voltage on any other pins		3.9	V
$\|\Delta V_{DDX}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins	-	50	mV
V_{REF+} - V_{DDA}	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V

1. All power (V_{DD}, V_{DDSD1}, V_{DDSD2}, V_{DDA}, V_{DD3V3_USBHS}, V_{DDCORE}, V_{DDCPU}, V_{BAT}) and ground (V_{SS}, V_{SSA}, V_{SSX}) pins must always be connected to the external/internal power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 53* for the maximum allowed injected current values.
3. Min(6.0, V_{DD}+3.9, V_{DDA}+3.9, V_{DD3V3_USBHS}+3.9, V_{BAT}+3.9).
   This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
   To sustain a voltage higher than 3.9 V the internal pull-up/pull-down resistors must be disabled.
4. Min(5.25, V_{DD}+3.9, V_{DD3V3_USBHS}+3.9).

Table 11. Current characteristics(1)

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)	440	mA
IV_{DD}	Maximum current into each V_{DD} power pin (source)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, NRST pins	-5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All power (V_{DD}, V_{DDSD1}, V_{DDSD2}, V_{DDA}, V_{DD3V3_USBHS}) and ground (V_{SS}, V_{SSA}, V_{SSX}) pins must always be connected to the external/internal power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 10: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 12. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (suffix 7)	105	
	Maximum junction temperature (suffix 3)	125	

6.3 Operating conditions

6.3.1 General operating conditions

Table 13. General operating conditions

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
F_{mpuss_ck}	Cortex-A7 subsystem	STM32MP131F	0	-	1000	MHz
		STM32MP131C	0	-	650	
F_{axiss_ck}, F_{hclk5}, F_{hclk6}	Internal AXI, AHB5, AHB6 clock frequency	-	0	-	266.5	
F_{ahb_ck}	Internal AHB clock frequency	-	0	-	209	
F_{pclk1}	Internal APB1 clock frequency	-	0	-	104.5	
F_{pclk2}	Internal APB2 clock frequency	-	0	-	104.5	
F_{pclk3}	Internal APB3 clock frequency	-	0	-	104.5	
F_{pclk4}	Internal APB4 clock frequency	-	0	-	133	
F_{pclk5}	Internal APB5 clock frequency	-	0	-	133	
F_{pclk6}	Internal APB6 clock frequency	-	0	-	133	
V_{DD}	I/Os and embedded regulators (REG1V1, REG1V8) supply voltage	SYSCFG_HSLVENxR = 0	1.71(1)(2)	-	3.6	V
		SYSCFG_HSLVENxR ≠ 0	1.71	-	2.7	
V_{DDSD1}, V_{DDSD2}	VDDSD1, VDDSD2, power section I/O's	SYSCFG_HSLVENxR = 0	0(3)	-	3.6	V
		SYSCFG_HSLVENxR ≠ 0	0	-	2.7	
V_{DD_ANA}(4)	System analog supply voltage	-	1.71	-	3.6	V
V_{DD_PLL}, V_{DD_PLL2}(5)	PLL supply voltage	-	1.71	-	3.6	V

Table 13. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
V_{DDCPU}	Cortex®-A7 CPU	Run Overdrive mode(6) (F_{mpuss_ck} above 650 MHz)	1.32	1.35	1.38	V
		Run mode(6) (F_{mpuss_ck} up to 650 MHz)	1.21	1.25	1.38(7)	
		Run OppMin mode (F_{mpuss_ck} = 64 MHz)	1.15	-	1.38(7)	
		Stop, LP-Stop mode	1.15	1.25	1.38(7)(8)	
		LPLV-Stop mode on V_{DDCPU}	0.85	0.9	1.38(7)(8)	
		LPLV-Stop2 mode	0	0	0	
V_{DDCORE}	Digital core domain supply voltage	Run mode(6)	1.21	1.25	1.29	V
		Stop, LP-Stop mode	1.15	1.25	1.29	
		LPLV-Stop mode	0.85	0.90	1.29(9)	
		LPLV-Stop2 mode	0.85	0.90	1.29(9)	
		Standby mode	0	0	0.75	
V_{DDA}	Analog operating voltage	ADC used with V_{REF} < 2 V(10)	1.62	-	2.15	V
		ADC used with V_{REF} > 2 V(10)	2	-	3.6	
		VREFBUF with V_{REF} = 1.65 V	1.95	-	3.6	
		VREFBUF with V_{REF} = 1.8 V	2.1	-	3.6	
		VREFBUF with V_{REF} = 2.048 V	2.35	-	3.6	
		VREFBUF with V_{REF} = 2.5 V	2.8	-	3.6	
		ADC, V_{REF} not used	0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.6	-	3.6	V
V_{DD3V3_USBHS}(11)	USB HS I/O supply voltage	USBH or USB OTG HS used	3.07	3.3	3.6	V
		USBH and USB OTG HS not used	0	-	3.6	
V_{DDQ_DDR}(12)	DDR PHY supply voltage	DDR3 memory	1.425	1.5	1.575	V
		DDR3L memory	1.283	1.35	1.45	
		LPDDR2 or LPDDR3	1.14	1.2	1.3	
V_{DDA1V8_REG}	USB HS PHY voltage supply with 1.8 V regulator in bypass mode	BYPASS_REG1V8 = V_{DD}	1.65	1.8	1.95	V
VIN	I/O Input voltage	TTxa I/O	-0.3	-	V_{DD}+0.3	V
		DDR I/O	-0.3	-	V_{DDQ_DDR}	
		USB HS I/O	-1	-	5.25	
		All I/O except TTxa	-0.3	-	See(13)	

Table 13. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
T_J	Junction temperature range	Suffix 7 version	-40	-	105	°C
		Suffix 3 version	-40	-	125	

1. Once nRST is released functionality is guaranteed down to V_{BOR} falling edge max.
2. Min V_{DD} is 2.25 V when REG1V8 is used BYPASS_REG1V8 = 0.
3. V_{DDSD1}, V_{DDSD2} voltages should be above Max_Vpad - 3.6V. Where Max_Vpad is the maximum input voltage present on device I/O's.
4. Should be connected to same power supply voltage as V_{DD}.
5. It is required to connect V_{DD_PLL} and V_{DD_PLL2} to same power supply as V_{DD}.
6. The min/typ/max values do not take into account any ripple. The values must be considered at the device power balls. It is not possible to start the device in overdrive mode since at reset the bit MPU_RAM_LOWSPEED = 1.
7. The device is functional up to 1.38 V but using V_{DDCPU} > 1.29 V does not guarantee life time according mission profile "Cortex®-A7 @650 MHz, -40 °C < T_J < 125 °C"
Refer also to the application note AN5438 "STM32MP1 Series lifetime estimates" available from the ST website *www.st.com*.
8. 1.38 V is the max allowed voltage, however LPLV-Stop mode is only relevant for V_{DDCPU} up to 0.95 V.
9. 1.29 V is the max allowed voltage, however LPLV-Stop mode is only relevant for VDDCORE up to 0.95 V. In LPLV-Stop mode, if VDDQ_DDR is not shutdown, to avoid overconsumption on VDDQ_DDR, the DDR memory must be put in SelfRefresh and DDR PHY must be set in retention mode (setting bit DDRRETEN: DDR retention enable of PWR control register 3 (PWR_CR3)).
10. V_{DDA} should always be ≥ V_{REF}.
11. For operation with voltage higher than Min (V_{DD}, V_{DDA}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
12. Independent from any other supply.
13. Min(5.5, V_{DD}+3.6, V_{DDA}+3.6). This formula has to be applied on power supplies related to the IO structure described by the pin definition table.

6.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions.

Table 14. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	20	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDD3V3_USBHS}(2)	V_{DD3V3_USBHS} rise time rate	0	∞	
	V_{DD3V3_USBHS} fall time rate	10	∞	

Table 14. Operating conditions at power-up / power-down (continued)

Symbol	Parameter	Min	Max	Unit
t_{VDDCPU}	V_{DDCPU} rise time rate (from reset or LPLV-Stop2 mode to RUN mode)	-	2000	µs/V
	V_{DDCPU} rise time rate (from LPLV-Stop to RUN mode)	-	1000(3)	
	V_{DDCPU} fall time rate	7.33	∞	
$t_{VDDCORE}$	V_{DDCORE} rise time rate (from reset to RUN mode)	-	2000	
	V_{DDCORE} rise time rate (from LPLV-Stop or LPLV-Stop2 mode to RUN mode)	-	1000(3)	
	V_{DDCORE} fall time rate	7.33	∞	

1. V_{DD} must be present before V_{DDCORE} and V_{DDCPU}.
2. V_{DDA1V8_REG} must be present before V_{DD3V3_USBHS}.
3. In case V_{DDCORE} or V_{DDCPU} rise time at exit of LPLV-Stop is larger than 1 ms/V, there is a risk of unwanted reset due to V_{DDCORE} or V_{DDCPU} potentially not yet established after $t_{SEL_VDDCORETEMPO}$ (cf. *Table 14* and *Figure 13*). In such a case, the V_{DDCORE} or V_{DDCPU} supply should not be decreased during LPLV-Stop mode.

Figure 12. V_{DDCORE} / V_{DDCPU} rise time from reset

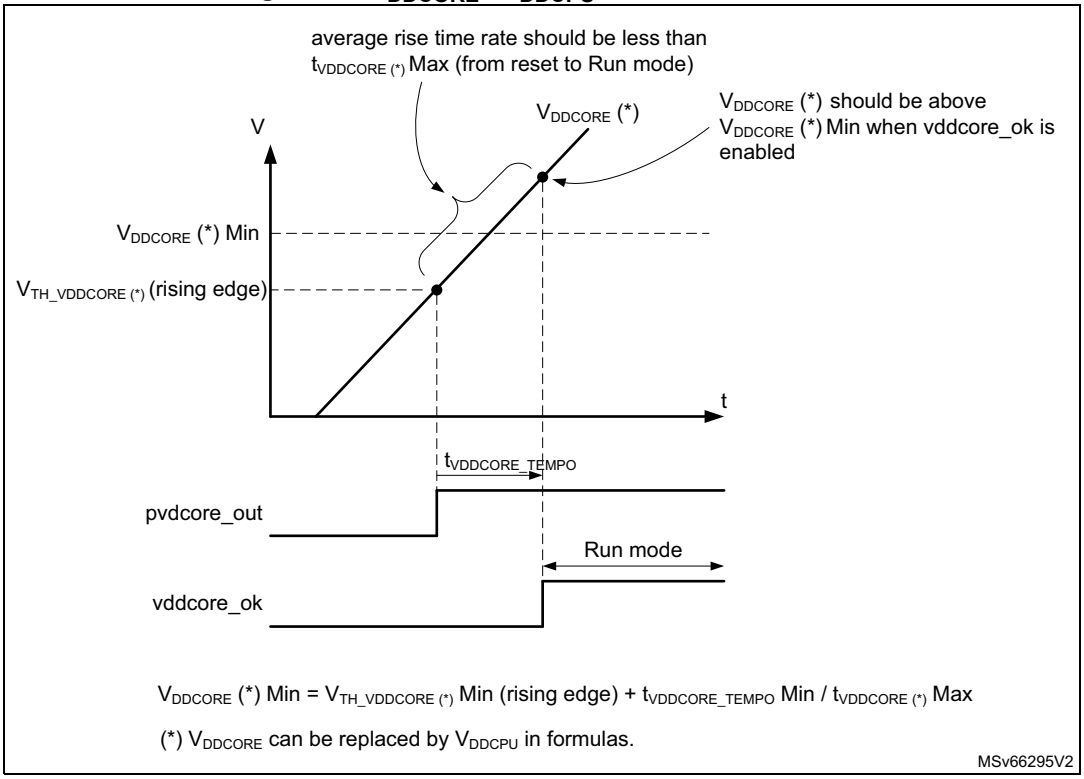
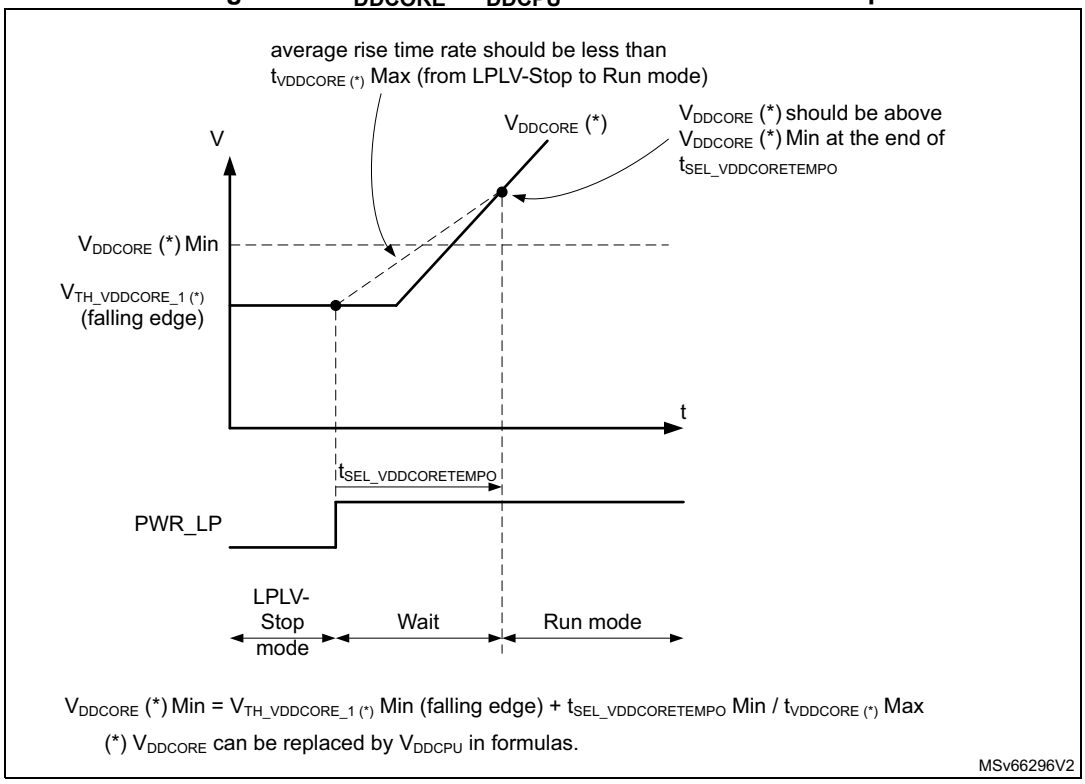


Figure 13. V_{DDCORE} / V_{DDCPU} rise time from LPLV-Stop



6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 15* are derived from tests performed under ambient.

temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 15. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset delay after BOR0 released	-	-	377	550	µs
V_{BOR0}(1)(2)	Brown-out reset threshold 0	Rising edge	1.62	1.67	1.71	V
		Falling edge	1.58	1.63	1.67	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.055	2.1	2.145	V
		Falling edge	1.955	2	2.045	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.355	2.4	2.445	V
		Falling edge	2.255	2.3	2.345	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.655	2.7	2.745	V
		Falling edge	2.555	2.6	2.645	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.905	1.95	1.995	V
		Falling edge	1.805	1.85	1.895	

Table 15. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.055	2.1	2.145	V
		Falling edge	1.955	2	2.045	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.205	2.25	2.295	V
		Falling edge	2.105	2.15	2.195	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.355	2.4	2.445	V
		Falling edge	2.255	2.3	2.345	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.505	2.55	2.595	V
		Falling edge	2.405	2.45	2.495	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.655	2.7	2.745	V
		Falling edge	2.555	2.6	2.645	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.805	2.85	2.895	V
		Falling edge in RUN mode	2.705	2.75	2.795	
V_{hyst_BOR0}	Hysteresis voltage of BOR0	Hysteresis in RUN mode	-	40	-	mV
V_{hyst_BOR}	Hysteresis voltage of BOR	Unless BOR0	-	100	-	mV
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BOR (unless BOR0) and PVD(3)	Hysteresis in RUN mode	-	100	-	mV
$I_{DD_BOR_PVD}$(1)(4)	BOR (unless BOR0) and PVD consumption from V_{DD}	-	0.246	-	0.626	µA
V_{AVM_0}	Analog voltage (V_{DDA}) detector threshold 0	Rising edge	1.655	1.7	1.745	V
		Falling edge	1.555	1.6	1.645	
V_{AVM_1}	Analog voltage (V_{DDA}) detector threshold 1	Rising edge	2.055	2.1	2.145	V
		Falling edge	1.955	2	2.045	
V_{AVM_2}	Analog voltage (V_{DDA}) detector threshold 2	Rising edge	2.455	2.5	2.545	V
		Falling edge	2.355	2.4	2.445	
V_{AVM_3}	Analog voltage (V_{DDA}) detector threshold 3	Rising edge	2.755	2.8	2.845	V
		Falling edge	2.655	2.7	2.745	
V_{hyst_VDDA}	Hysteresis of analog voltage (V_{DDA}) detector	-	-	100	-	mV
I_{VDD_AVM}(1)	Analog Voltage Monitoring (V_{DDA}) consumption on V_{DD}	-	-	-	0.248	µA
I_{VDDA_AVM}(1)	Analog Voltage Monitoring (V_{DDA}) consumption on V_{DDA}	Resistor bridge	-	2.12	-	µA
$V_{TH_VDDCORE}$(5)	Digital core domain supply voltage (V_{DDCORE}) detector threshold 0 (Run)	Rising edge	0.95	0.995	1.04	V
		Falling edge	0.91	0.955	1	

Table 15. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TH_VDDCORE_1}$ (6)	Digital core domain supply voltage (V_{DDCORE}) detector threshold 1 (LPLV_Stop)	Falling edge	0.71	0.755	0.8	V
$V_{hyst_VDDCORE}$	Hysteresis of Digital core domain supply voltage (V_{DDCORE}) detector	-	-	40	-	mV
$t_{VDDCORE_TEMPO}$	Delay on $V_{TH_VDDCORE}$ at rising edge of V_{DDCORE} to ensure that V_{DDCORE} is fully established	-	200	340	550	µs
$t_{SEL_VDDCORETEMPO}$	Delay on $V_{TH_VDDCORE_1}$ at rising edge of V_{DDCORE} to ensure that V_{DDCORE} is fully established on exit of LPLV-Stop mode	-	234	380	700	µs
$I_{VDD_VDDCOREVM}$ (1)	V_{DDCORE} Voltage Monitoring consumption on V_{DD}	-	1.7	2.6	4.2	µA
V_{TH_VDDCPU}(7)	Digital MPU domain supply voltage (V_{DDCPU}) detector threshold 0 (Run)	Rising edge	0.95	0.995	1.04	V
		Falling edge	0.91	0.955	1	
$V_{TH_VDDCPU_1}$(8)	Digital MPU domain supply voltage (V_{DDCPU}) detector threshold 1 (LPLV_Stop)	Falling edge	0.71	0.755	0.8	V
V_{hyst_VDDCPU}	Hysteresis of Digital MPU domain supply voltage (V_{DDCPU}) detector	-	-	40	-	mV
t_{VDDCPU_TEMPO}	Delay on V_{TH_VDDCPU} at rising edge of V_{DDCPU} to ensure that V_{DDCPU} is fully established	-	200	340	550	µs
$t_{SEL_VDDCPUTEMPO}$(9)	Delay on $V_{TH_VDDCPU_1}$ at rising edge of V_{DDCPU} to ensure that V_{DDCPU} is fully established on exit of LPLV-Stop mode	-	234	380	700	µs
$I_{VDD_VDDCPUVM}$(1)	V_{DDCPU} Voltage Monitoring consumption on V_{DD}	-	2.2	3.5	5.2	µA
V_{TH_VDDUSB}	V_{DD3V3_USBHS} Threshold voltage	-	-	1.21	-	V
V_{TH_VDDSD1}	V_{DDSD1} Threshold voltage	-	-	1.21	-	V
V_{TH_VDDSD2}	V_{DDSD2} Threshold voltage	-	-	1.21	-	V

1. Specified by design, not tested in production.
2. VPOR (power-on reset Voltage threshold) = BOR0 rising edge value
   VPDR (power-down reset Voltage threshold) = BOR0 falling edge value
3. No hysteresis when using PVD_IN pin.
4. BOR0 is enabled in all modes and its consumption is therefore included in the supply current characteristics tables.

5. During the first rising edge of V_{DDCORE}, the slope should be less than 2 ms/V to ensure V_{DDCORE} is fully established before the end of the $t_{VDDCORE_TEMPO}$.
6. When exiting from LPLV-Stop mode to RUN mode the rising slope for V_{DDCORE} should be less than 1 ms/V to ensure V_{DDCORE} is fully established before the end of the $t_{VDDCORE_TEMPO}$.
7. During the first rising edge of V_{DDCORE}, the slope should be less than 2 ms/V to ensure V_{DDCORE} is fully established before the end of the $t_{VDDCORE_TEMPO}$.
8. When exiting from LPLV-Stop mode to RUN mode the rising slope for V_{DDCPU} should be less than 1 ms/V to ensure V_{DDCPU} is fully established before the end of the t_{VDDCPU_TEMPO}.
9. $t_{SEL_VDDCPUTEMPO}$ is identical to $t_{SEL_VDDCORETEMPO}$ since both V_{DDCORE} and V_{DDCPU} are following same supply voltage increase on exit from LPLV-Stop mode.

6.3.4 Embedded reference voltage

The parameters given in *Table 16*, *Table 17* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 16. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltages	-40 °C < T_J < 125 °C	1.175	1.210	1.241	V
$t_{S_vrefint}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}(1)	V_{BAT} sampling time when reading the internal V_{BAT} reference voltage	-	9.8	-	-	
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	0.8	-	4.6	
I_{refbuf}(2)	Reference Buffer consumption for ADC	V_{DDA} = 3.3 V	9.1	13.6	27.7	µA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	-40 °C < T_J < 125 °C	-	4.3	15	mV
$T_{coeff_VREFINT}$	Average temperature coefficient	Average temperature coefficient	-	19	67	ppm/°C
$V_{DDcoeff}$	Average Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	10	1370	ppm/V

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Specified by design, not tested in production.

Table 17. Embedded reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = V_{REF+} = 3.3 V	0x5C00 5250[31:16](1)(2)

1. Mandatory to read in 32-bits word and do relevant mask and shift to isolate required bits.
2. These address is inside BSEC which should be enabled in RCC to allow access.

6.3.5 Embedded regulators characteristics

The parameters given in *Table 18*, *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

REG1V1 embedded regulator (USB_PHY)

Table 18. REG1V1 embedded regulator (USB_PHY) characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA1V1_REG}	Regulated output voltage	-	1.045	1.1	1.155	V
C_L	Load Capacitor	-	1.1	2.2(2)	3.3	µF
esr	Equivalent Serial Resistor of Cload	-	0.1	25	600	mΩ
I_{load}	Static load current(3)	-	0	-	30	mA
t_{START}	Start-up time. from PWR_CR3.REG11EN = 1 to PWR_CR3.REG11RDY = 1	C_L=2.2uF	-	93	-	µs
		C_L=3.3uF	-	-	180	
I_{INRUSH}	V_{DD} Inrush Current to load external capacitor at start	-	-	50	60	mA
I_{VDD}	Regulator Current consumption on V_{DD}	Regulator Enabled and I_{load} = 0 mA	-	150	205	µA
		Regulator Enabled and I_{load} = 30 mA	-	176	242	

1. Specified by design, not tested in production.
2. For better dynamic performances a 2.2 µF typical value external capacitor is recommended.
3. Load is for internal STM32MP131C/F analog blocks, no additional external load is accepted unless mentioned.

Table 19. REG1V8 embedded regulator (USB_PHY) characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Regulator input voltage	-	2.25	3.3	3.6	V
V_{DDA1V8_REG}	Regulated output voltage	after trimming	1.7	1.8	1.9	V
C_L	Load Capacitor	-	0.5	2.2(2)	3.3	µF
esr	Equivalent Serial Resistor of Cload	-	0.1	25	600	mΩ
I_{load}	Static load current(3)	-	-	-	70	mA
t_{START}	Start-up time. from PWR_CR3.REG11EN = 1 to PWR_CR3.REG11RDY = 1	C_L=2.2uF	-	81	-	µs
		C_L=3.3uF	-	-	150	
I_{INRUSH}	V_{DD} Inrush Current to load external capacitor at start	-	-	80	100	mA

Table 19. REG1V8 embedded regulator (USB_PHY) characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{VDD}	Regulator Current consumption on V_{DD}	Regulator Enabled and I_{load} = 0 mA	-	130	181	µA
		Regulator Enabled and I_{load} = 70 mA	-	170	231	

1. Specified by design, not tested in production.
2. For better dynamic performances a 2.2 µF typical value external capacitor is recommended.
3. Load is for internal STM32MP131C/F analog blocks, no additional external load is accepted unless mentioned.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.

All the Run mode current consumption measurements given in this section are performed with a CoreMark code unless otherwise specified.

Typical and maximum current consumption

The device is placed under the following conditions:

- All I/O pins are in analog input mode except when explicitly mentioned.
- All peripherals are disabled except when explicitly mentioned.
- The maximum values are obtained for V_{DD}/V_{BAT} = 3.6 V, V_{DDCORE} = 1.29 V, and V_{DDCPU} = 1.29 V, and the typical values for V_{DD}/V_{BAT} = 3.3 V, V_{DDCORE} = 1.25 V and V_{DDCPU} = 1.25 V unless otherwise specified.

The parameters given in *Table 22* to *Table 27* are derived from tests performed under supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 20. Current consumption (I_{DDCORE}) in Run mode

Symbol	Parameter	Conditions				Typ	Max				Unit
		-	MPU SS mode	Oscillator	AXI clk (MHz)	Tj = 25 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDCORE}	Supply current in Run mode	All peripherals enabled(1)	CRun	AHB clock = 64 MHz(2)	266	115	143	213	267	340	mA
I_{DDCORE}	Supply current in Run mode	All peripherals disabled	CRun	AHB clock = 200 MHz(3)	266	82	99	172	224	301	mA
				AHB clock = 64 MHz(4)	266	62	83.4	156	208	284	
					150	41	59.7	133	183	256	
					64	30	47.6	121	171	244	
					24	24	41.1	115	168	237	

1. Activity on peripherals and bus masters other than processors, could lead to additional power consumption above these values, largely dependent on the amount of initialized peripherals and their activity.
2. Peripheral clocks set at default values (see table “Peripheral clock distribution overview” in reference manual) with pll4_r_ck = pll4_q_ck = 50 MHz, pll4_p_ck = 125 Mhz, pclk1/2/3 = 32 MHz, pclk4 = 132 MHz, pclk5 = 66 MHz, pclk6 = 64 MHz.
3. pclk1/2/3 = 100 MHz, pclk4 = 132 MHz, pclk5 = 66 MHz, pclk6 = 104.5 MHz.
4. pclk1/2/3 = 32 MHz, pclk4 = AXI clock/2, pclk5 = AXI clock/4, pclk6 = 64 MHz.

Table 21. Current consumption (I_{DDCPU}) in Run mode

Symbol	Parameter	Conditions		Typ	Max				Unit
		MPU SS mode	MPU clk (MHz)	Tj = 25 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDCPU}	Supply current in Run mode	CRun	1000(1)	150	167	225	268	-	mA
			900(1)	135	153	211	254	-	
			780(1)	115	135	194	235	-	
			650	88.5	104	153	188	239	
			600	82	98	147	181	232	
			400	56	69	119	153	203	
			300	43	54.7	105	139	188	
			150	30	40.9	91.5	125	174	
			64	12	22.5	73.2	107	156	
			24	6.65	16.5	67.1	100.6	149	
I_{DDCPU}	Supply current in Run mode OppMin	CRun	64(2)	10.5	19.7	64.1	93.5	136	mA
I_{DDCPU}	Supply current in Run mode	CSleep (MPU in CSleep with WFI (CLK OFF))	900(1)	20	32.9	93.8	133	-	mA
			780(1)	18	30.8	91.6	131	-	
			650	13.5	23.9	74.3	108	156	
			600	13	23.1	73.5	107	156	
			300	8.2	18.2	68.6	102.2	151	
			150	6.65	16.5	66.9	100.5	149	
			64	4.5	14.3	64.7	98.2	147	
			24	3.85	13.6	64.0	97.5	146	

1. Typical value given with V_{DDCPU} = 1.35 V, maximum values given with V_{DDCPU} = 1.37 V.
2. Typical and maximum values given with V_{DDCPU} = 1.15 V, V_{DDCORE} = 1.25 V, V_{DD} = 3.3 V.

Table 22. Current consumption (I_{DD}) in Run mode[1]

Symbol	Parameter	Conditions		Typ	Max				Unit
		MPU SS mode	Oscillator	Tj = 25 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DD}	Supply current in Run mode	CRun	HSE+HSI+LSI+CSI+ PLL1,2,3,4	2.75	2.98	2.95	2.96	2.61[2]	mA
I_{DD}	Supply current in Run mode	CSleep	HSI+PLL1,2	1.95	2.1	2.1	2.1	2.1	mA
			HSE+HSI	0.56	0.64	0.65	0.67	0.70	
			HSI	0.29	0.33	0.33	0.34	0.36	

1. HSE = 24 MHz.
2. Value provided with PLL1 @648 MHz while other values on the same row are provided with PLL1 @1 GHz (not allowed at 125°C).

Table 23. Current consumption in Stop mode

Symbol	Parameter	Conditions		Typ				Max				Unit
		-	MPU SS mode	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DD}	Supply current in Stop mode	All peripherals disabled	CStop	10.0	13.0	17.5	28	15.1	22.4	37.4	74.0	µA
I_{DDCORE}				5.35	29	52.5	89.5	20.2	92.0	142	211	mA
I_{DDCPU}				3.45	19	34	58.5	12.6	60.2	92.4	137	

Table 24. Current consumption in LPLV-Stop mode

Symbol	Parameter	Conditions		Typ(1)				Max(2)				Unit
		-	MPU SS mode	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DD}	Supply current in LPLV-Stop mode	All Peripheral disabled	CStop	10.0	13.0	17.5	28	15.1	22.4	37.4	74.0	µA
I_{DDCORE}				1.85	12.0	21.5	40.0	6.55	38.2	62.8	98.9	mA
I_{DDCPU}				1.30	8.00	14.0	26.5	4.17	25.4	41.3	64.9	

1. V_{DDCORE} = 0.9 V, V_{DDCPU} = 0.9 V.
2. V_{DDCORE} = 0.95 VV_{DDCPU} = 0.95 V.

Table 25. Current consumption in LPLV-Stop2 mode

Symbol	Parameter	Conditions		Typ(1)				Max(2)				Unit
		-	MPU SS mode	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DD}	Supply current in LPLV-Stop2 mode	All Peripheral disabled	CStandby	7.50	10.5	13.5	21.5	11.5	17.1	28.3	54.9	µA
I_{DDCORE}				1.80	13.0	22.0	37.5	6.6	38.3	62.8	98.9	mA
I_{DDCPU}				0	0	0	0	0	0	0	0	

1. V_{DDCORE} = 0.9 V, V_{DDCPU} = 0 V.
2. V_{DDCORE} = 0.95 V, V_{DDCPU} = 0 V.

Table 26. Current consumption in Standby mode(1)

Symbol	Parameter	Conditions		Typ				Max				Unit
		-	MPU SS mode	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj= 125 °C	
I_{DD}	Supply current in Standby mode	Backup SRAM OFF, RTC OFF, LSE OFF	CStandby	3.65	5.95	9	16	3.91	7.63	13.1	26.6	µA
		Backup SRAM ON, RTC ON, LSE ON, medium_high drive		8.2	21	33.5	56.5	17	33	57	116	

1. IWDG OFF, LSI OFF, $V_{DDCORE} = V_{DDCPU} = 0$ V.

Table 27. Current consumption in V_{BAT} mode

Symbol	Parameter	Conditions		Typ				Max				Unit
		-	V_{BAT} (V)	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDVBAT}	Supply current in V_{BAT} mode	Backup SRAM OFF, RTC OFF, LSE OFF, LSE CSS OFF, temperature monitoring OFF	1.6	< 0.1	0.120	0.330	0.905	< 0.1	0.726	2.52	7.24	µA
			2.4	< 0.1	0.135	0.365	0.975	< 0.1	0.937	2.84	7.82	
			3	< 0.1	0.195	0.505	1.20	< 0.1	1.13	3.12	8.30	
			3.3	< 0.1	0.515	1.30	3.30	< 0.1	1.27	3.34	8.66	
			3.6	< 0.1	0.610	1.45	3.50	0.207	1.55	3.71	9.21	
		Backup SRAM OFF, RTC ON, LSE ON, medium_high drive, LSE CSS OFF, temperature monitoring OFF	1.6	0.915	1.10	1.35	1.95	0.378	1.35	3.17	7.90	
			2.4	1.25	1.45	1.70	2.35	0.985	2.03	3.95	8.96	
			3	1.55	1.80	2.15	2.95	1.79	2.79	4.78	9.95	
			3.3	1.70	2.30	3.15	5.20	2.32	3.28	5.32	10.60	
			3.6	1.95	2.60	3.50	5.65	2.92	3.93	6.04	11.6	
		Backup SRAM ON, RTC ON,. LSE ON, medium_high drive, LSE CSS OFF, temperature monitoring OFF	1.6	3.20	12.5	21.0	35.5	5.22	23.6	42.3	74.9	
			2.4	3.65	13.0	22.0	36.5	6.93	27.2	46.8	81.8	
			3	4.05	13.5	22.5	38.5	8.07	29.4	49.2	84.8	
			3.3	4.40	14.5	24.5	41.5	8.78	30.9	50.9	86.4	
			3.6	4.70	15.5	26.0	43.5	9.59	32.3	52.9	88.5	
		Backup SRAM ON, RTC ON,. LSE ON, high drive, LSE CSS OFF, temperature monitoring OFF	1.6	3.55	12.5	21.5	35.5	5.19	23.6	42.3	74.9	
			2.4	3.95	13.5	22.0	37.0	5.83	25.6	45.2	79.7	
			3	4.40	14.0	23.0	39.0	8.08	29.5	49.2	84.7	
			3.3	4.70	15.0	25.0	41.5	8.79	30.9	51.1	86.5	
			3.6	5.05	16.0	26.0	43.0	9.60	33.3	52.9	88.6	

Table 27. Current consumption in V_{BAT} mode (continued)

Symbol	Parameter	Conditions		Typ				Max				Unit
		-	V_{BAT} (V)	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDVBAT}	Supply current in V_{BAT} mode	Backup SRAM ON, RTC ON, LSE ON, high drive, LSE CSS ON, temperature monitoring ON	1.6	3.55	12.5	21.0	36.0	7.95	28.0	47.9	82.3	µA
			2.4	3.95	13.5	22.0	37.0	8.99	29.6	49.4	84.3	
			3	4.45	14.0	23.0	38.5	10.02	32.1	51.8	87.2	
			3.3	4.65	15.0	24.5	41.5	10.7	33.2	53.6	89.0	
			3.6	5.00	16.0	26.0	43.5	11.2	35.9	55.5	90.8	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 54: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

The I/Os used by an application contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

The theoretical formula is provided below:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: C = CINT+ CEXT

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 28* are measured starting from the wakeup event trigger up to the first instruction executed by the MPU:

- For CSleep modes:
  - the MPU goes in low-power mode after WFE (Wait For Event) instruction.
- For CStop modes:
  - the MPU goes in low-power mode after WFI (Wait For Interrupt) instruction.
- WKUPx pin is used to wakeup from low-power modes.

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.3 V.

Table 28. Low-power mode wakeup timings

Symbol	Parameter	System mode	Conditions (after wakeup)	Typ(1)	Max(1)	Unit
MPU wakeup						
$t_{WUCSLEEP_MPU}$	MPU wakeup from CSleep	Run	HSE 24 MHz, SYSRAM	31	32	mpuss_ck clock cycles
$t_{WUCSTOP_MPU}$	MPU wakeup from CStop	Stop	HSI 64 MHz, SYSRAM	16	17	µs
			HSE + PLL 1000 MHz, SYSRAM	64	73	
			HSE + PLL 650 MHz, SYSRAM	64	73	
$t_{WULPLV_Stop_MPU}$	MPU wakeup from CStop with system in LPLV-Stop (LVDS=1)	LPLV-Stop	HSI 64 MHz, SYSRAM	410	470	
$t_{WULPLV_Stop2_MPU}$	MPU wakeup from CStandby with system in LPLV-Stop2	LPLV-Stop2	HSI 64 MHz, SYSRAM	9000(2)	-	

1. Evaluated by characterization, not tested in production unless otherwise specified.
2. On exit from LPLV-Stop2 the boot ROM is activated and a branch is done to the address stored in the BSEC_SCRATCH register. A system initialization is done which duration depends on the user application. Here are application dependent parameters used for characterization:
   - MMU description table size: 32 Bytes (could be up to 20 Kbytes for a Linux application)
   - HSI frequency: 64 kHz (waking up with a fast PLL would significantly reduce $t_{WULPLV_Stop2_MPU}$)
   Note: branching directly to a function that toggles a GPIO would result in $t_{WULPLV_Stop2_MPU} \approx 1500$ µs.
   The wakeup time will depend on the V_{DDCPU} ramp-up time.

Table 29. Wakeup time using USART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
tWUUSART	Wakeup time needed to calculate the maximum USART baud rate allowing the wakeup from stop mode when USART clock source is HSI.	Stop	-	6.7	µs
		LPLV-Stop	-	318(2)	µs

1. Specified by design, not tested in production.
2. Including the $t_{SEL_VDDCORETEMPO}$ = 234 µs.

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

Digital and analog bypass modes are available.

The external clock signal has to respect the *Table 54: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 14* for digital bypass mode and in *Figure 15* for analog bypass mode. In analog bypass mode the clock can be a sinusoidal waveform.

Table 30. High-speed external user clock characteristics (digital bypass)(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	8	24	48	MHz
V_{HSEH}	OSC_IN input pin high level voltage	$0.7 \times V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	$0.3 \times V_{DD}$	
$t_{W(HSE)}$	OSC_IN high or low time	7	-	-	ns

1. Specified by design, not tested in production.

Figure 14. High-speed external clock source AC timing diagram (digital bypass)

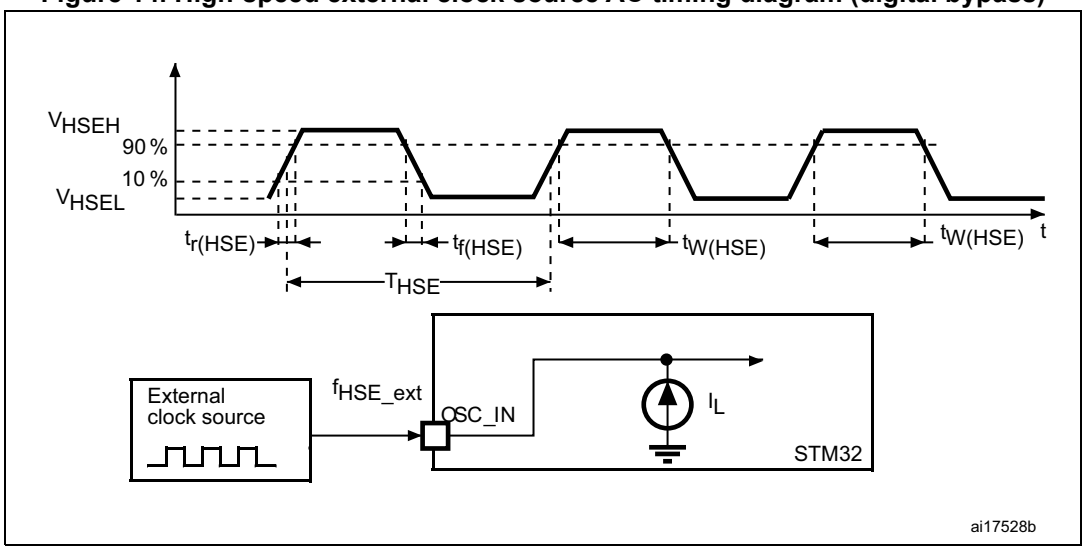


Table 31. High-speed external user clock characteristics (analog bypass)(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	8	24	48	MHz
	duty cycle (Square wave)	45	50	55	%
	duty cycle deterioration	0	±10(2)	±20(3)	%
V_{HSE}	Absolute input range	0	-	V_{DD}	-
V_{PP}	OSC_IN peak-to-peak amplitude	0.2(4)	-	$0.67 \times V_{DD}$	V
t_{SU}(5)	Time to start	-	1	10(6)	µs
$tr/tf_{(HSE)}$	Rise and Fall time (10% to 90% threshold levels of the input peak-to-peak amplitude)	$0.05 \times T_{HSE}$	-	$0.3 \times T_{HSE}$	ns
$I_{(HSE)}$	Power consumption	-	150(7)	500(8)	µA

1. Specified by design, not tested in production.
2. Specified by design, not tested in production: with a square wave signal (@25 °C, V_{DD}=3.3 V /V_{PP} = 400 mV / V_{DC}=1 V) where V_{DC} is the DC component of the input signal.

3. Specified by design, not tested in production: with a square wave signal (@25 °C, V_{DD}=1.71 V /V_{PP} = 200 mV / V_{DC}=0.8 V) where V_{DC} is the DC component of the input signal.
4. minimum peak-to-peak amplitude (@25 °C, 0.1<V_{DC}<V_{DD}-0.1 V) where V_{DC} is the DC component of the input signal.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized analog bypass clock interface is reached. This value is measured with 200 mV peak-to-peak amplitude.
6. Maximum start-up time is obtained with 200 mV peak-to-peak amplitude.
7. with a sine wave signal (V_{PP} = 400 mV / V_{DC}=0.4 V) where V_{DC} is the DC component of the input signal.
8. with a sine wave signal (V_{DD} = 3.6 V / V_{PP} = 800 mV / V_{DC} = 1.8 V) where V_{DC} is the DC component of the input signal.

Figure 15. High-speed external clock source AC timing diagram (analog bypass)

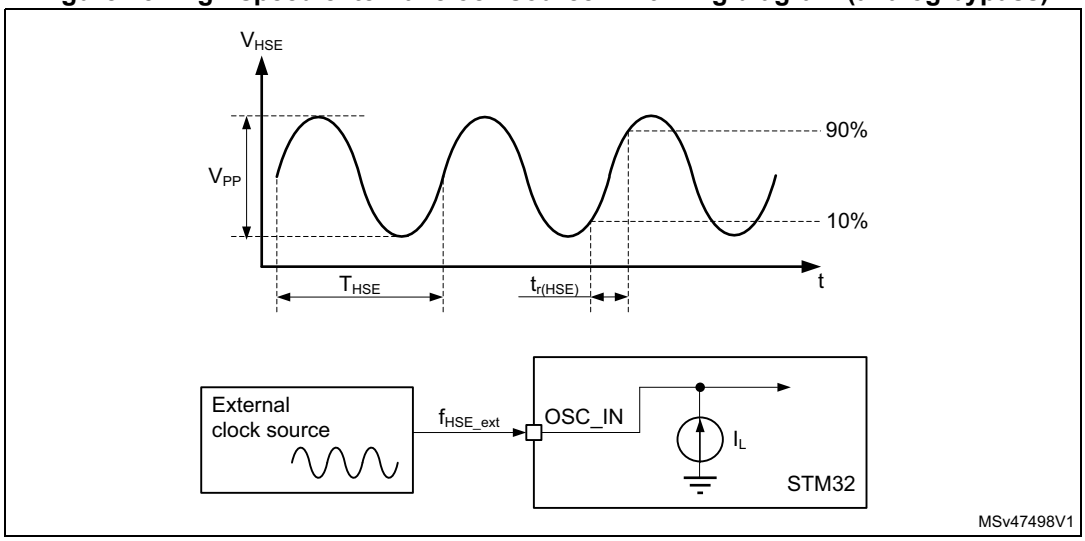
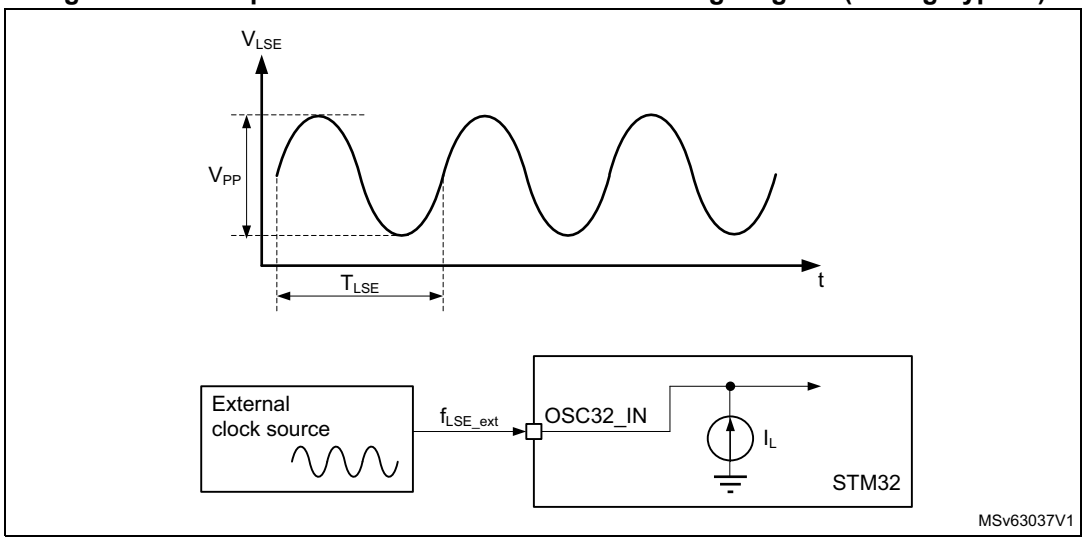


Table 32. Low-speed external user clock characteristics (analog bypass)(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	-	kHz
V_{LSE}	Absolute input range	0	-	V_{SW}(2)	-
V_{PP}	OSC32_IN peak-to-peak amplitude	0.2(3)	1	-	V
$I_{(LSE)}$	Power consumption	-	120	-	nA

1. Specified by design, not tested in production.
2. V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise
3. Minimum peak-to-peak amplitude (@25 °C, 0.1 < V_{DC} < V_{SW} - 0.1 V) where V_{DC} is the DC component of the input signal.

Figure 16. Low-speed external clock source AC timing diagram (analog bypass)



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 54: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 17* for digital bypass and *Figure 16* for analog bypass.

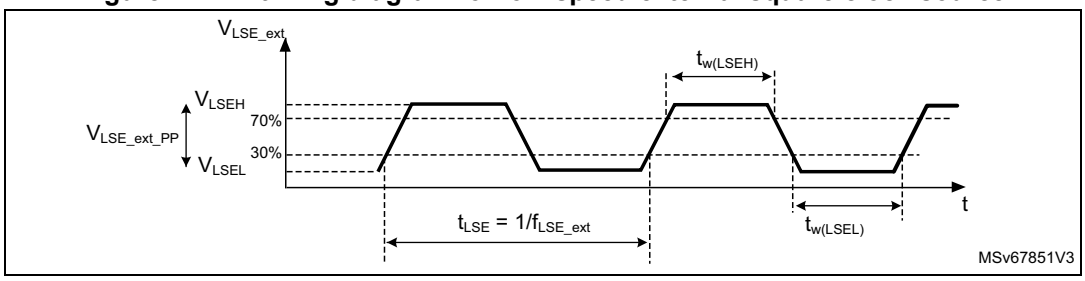
Table 33. Low-speed external user clock characteristics (digital bypass)(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	5	32.768	40	kHz
$V_{LSE_ext_PP}$	OSC32_IN peak-to-peak amplitude	0.3	-	V_{SW}(2)	V
V_{LSE_ext}	OSC32_IN input range	0	-	V_{SW}(2)	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time for square signal input	10	-	-	ns

1. Specified by design. Not tested in production.
2. $V_{SW} = V_{DD}$ when V_{DD} is above V_{BOR0}, and $V_{SW}=V_{BAT}$ when V_{DD} is below V_{BOR0}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 17. AC timing diagram for low-speed external square clock source



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 8 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 34*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 34. 8-48 MHz HSE oscillator characteristics(1)

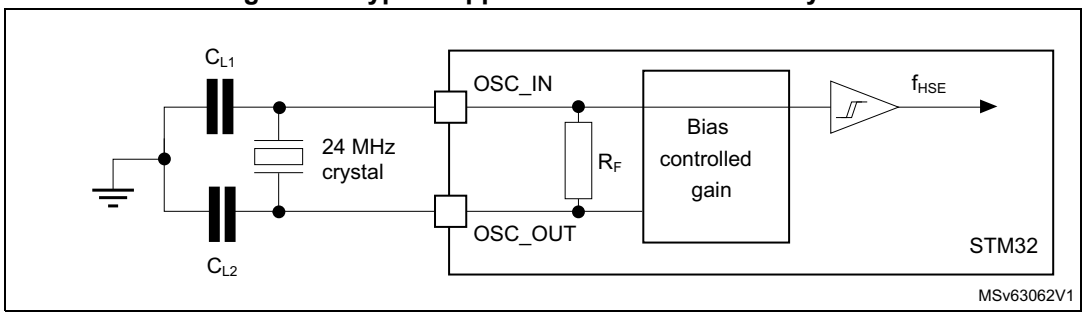
Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	8	24	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	8	mA
		V_{DD} = 3.3 V, Rm = 150 Ω C_L = 12 pF at 4 MHz	-	0.53	-	
		V_{DD} = 3.3 V, Rm = 120 Ω C_L = 10 pF at 16 MHz	-	0.61	-	
		V_{DD} = 3.3 V, Rm = 100 Ω C_L = 10 pF at 24 MHz	-	0.63	-	
		V_{DD} = 3.3 V, Rm = 80 Ω C_L = 8 pF at 32 MHz	-	0.63	-	
		V_{DD} = 3.3 V, Rm = 80 Ω C_L = 8 pF at 48 MHz	-	0.81	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.15	mA/V
t_{SU}(4)	Start-up time	V_{DD} is stabilized	-	2	-	ms

1. Specified by design, not tested in production.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 18*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitance must be included (4 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with a 24 MHz crystal



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 35*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

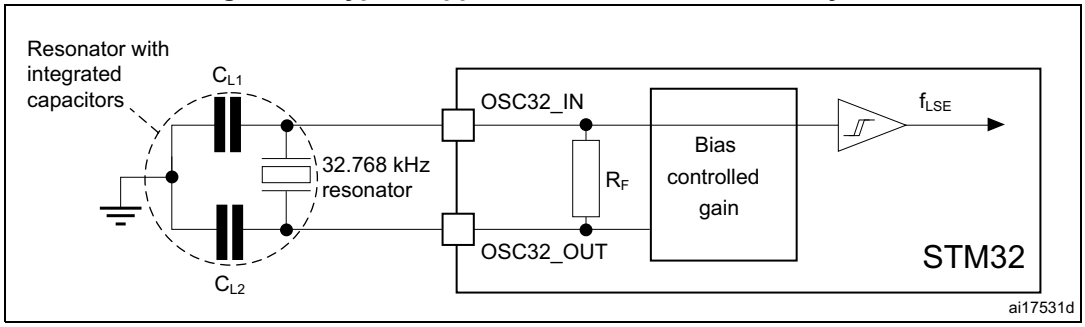
Table 35. Low-speed external user clock characteristics(1)

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	303	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	466	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	636	-	
		LSEDRV[1:0] = 11, High drive capability	-	1028	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Specified by design, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers.
3. t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 19. Typical application with a 32.768 kHz crystal



1. Adding an external resistor between OSC32_IN and OSC32_OUT is forbidden.

6.3.9 External clock source security characteristics

Table 36. High-speed external user clock security system (HSE CSS)(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{DCM(HSE_CSS)}$	Time to detect clock missing	-	2	-	µs
$t_{DCP(HSE_CSS)}$	Time to detect clock presence	-	-	250	ns
$I_{VDD(HSE_CSS)}$	Power consumption (f_{HSE} = 48 MHz)	-	-	50	µA

1. Specified by design, not tested in production.

6.3.10 Internal clock source characteristics

The parameters given in *Table 37*, *Table 38* and *Table 39* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

64 MHz high-speed internal RC oscillator (HSI)

Table 37. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}(2)	HSI frequency	V_{DD} = 3.3 V, T_J = 30 °C	63.7	64	64.3	MHz
TRIM	HSI user trimming step	Trimming is not a multiple of 32	-	0.24	0.33	%
		Trimming is 128, 256 and 384	-	-2.43	-	
		Trimming is 64, 192, 320 and 448	-	-0.70	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)	-	-0.30	-	
DuCy(HSI)	Duty Cycle	-	45	-	55	%

Table 37. HSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta_{VDD\ (HSI)}$	HSI oscillator frequency drift over V_{DD} (reference is 3.3 V)	V_{DD} = 1.71 to 3.6 V	-0.12	-	0.03	%
$\Delta_{TEMP\ (HSI)}$(3)	HSI oscillator frequency drift over temperature after factory calibration	T_J = -20 to 110 °C	-1.25	-	0.75	%
		T_J = -40 to 125 °C	-1.75	-	0.95	
t_{su}(HSI)	HSI oscillator start-up time (Time between Enable rising and First output clock edge.)	-	-	1.47	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1% of target frequency	-	3	-	µs
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. Specified by design, not tested in production unless otherwise specified.
2. Guaranteed by testing.
3. Evaluated by characterization, not tested in production.

4 MHz low-power internal RC oscillator (CSI)

Table 38. CSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}(2)	CSI frequency	V_{DD} = 3.3 V, T_J = 30 °C	3.98	4	4.02	MHz
TRIM	Trimming step	Trimming code is not a multiple of 16	-	0.85	1	%
		Trimming code is a multiple of 16	-	-1.65	-	-
DuCy(CSI)	Duty Cycle	-	45	-	55	%
Δ_{VDD} (CSI) + Δ_{TEMP} (CSI)(3)	CSI oscillator frequency drift over V_{DD} & drift over temperature	V_{DD} = 1.71 to 3.6 V T_J = 0 to 85 °C	-	±1.43	-	%
$t_{su(CSI)}$	CSI oscillator startup time	-	-	1.5	2.4	µs
$t_{stab(CSI)}$	CSI oscillator stabilization time (to reach ±5% of f_{CSI})	T_J = 0 to 85 °C	-	5	-	cycle
$I_{DD(CSI)}$	CSI oscillator power consumption	-	-	30	-	µA

1. Specified by design, not tested in production.
2. Guaranteed by testing.
3. Evaluated by characterization, not tested in production.

32 kHz low-speed internal (LSI) RC oscillator

Table 39. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	T_J = 30 °C,(2) V_{DD} = 3.3 V	31.4	32	32.6	kHz
		T_J = -40 to 125 °C, V_{DD} = 1.71 to 3.6 V	29	32	33.6	
$t_{su(LSI)}$	LSI oscillator startup time (Time between Enable rising and First output clock edge.)	-	-	64	125	µs
$t_{stab(LSI)}$	LSI oscillator stabilization time (5% of final value)	-	-	110	170	
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	120	230	nA

1. Specified by design, not tested in production.
2. Guaranteed by testing.

6.3.11 PLL characteristics

The parameters given in *Table 41*, *Table 42*, *Table 43* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

PLL1 characteristics

Table 40. PLL1 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Normal mode and Sigma delta mode	8	-	16	MHz
	PLL input clock duty cycle	-	10	-	90	%
$f_{PLL_P_Q_R_OUT}$	PLL P,Q,R multiplier output clock	-	3.875	-	1000 (2)	MHz
	PLL P,Q,R clock duty cycle	Division by 1	47.5	50	52.5	%
		Even divisions (N multiple of 2)	47.5	50	52.5	
		Odd divisions (N not multiple of 2)	[100×(N+1)/2N] - 5	[100×(N+1)/2N]	[100×(N+1)/2N] + 5	
f_{VCO_OUT}	PLL VCO output	Direct VCO clock after internal divider/2	496	-	1000	MHz
	PLL VCO Duty Cycle		47.5	50	52.5	%

Table 40. PLL1 characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{LOCK}	PLL lock time	Normal mode		-	50	150	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)		-	65	170	
A_{LOCK}	Lock Accuracy (Ratio VCO frequency versus target frequency at lock)	-		-	-	±2	%
Jitter	RMS cycle-to-cycle jitter	$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 Without Fractional mode	VCO = 992 MHz	-	24(3)	-	±ps
			VCO = 1066 MHz	-	24(3)	-	
			VCO = 2000 MHz	-	23(3)	-	
		$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 With Fractional mode	VCO = 992 MHz	-	23(3)	-	
			VCO = 2000 MHz	-	24(3)	-	
	RMS period jitter	$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 Without Fractional mode	VCO = 992 MHz	-	16(3)	-	±ps
			VCO = 1066 MHz	-	16(3)	-	
			VCO = 2000 MHz	-	14(3)	-	
		$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 With Fractional mode	VCO = 992 MHz	-	22(3)	-	
			VCO = 2000 MHz	-	15(3)	-	
	Long term jitter	$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 f_{PLL_IN} = 8 MHz Without Fractional mode	VCO = 992 MHz	-	185(4)	-	ps
			VCO = 1066 MHz	-	180(4)	-	
			VCO = 2000 MHz	-	103(4)	-	
		$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 f_{PLL_IN} = 8 MHz With Fractional mode	VCO = 992 MHz	-	270(4)	-	
			VCO = 1066 MHz	-	260(4)	-	
			VCO = 2000 MHz	-	104(4)	-	
	Peak to Peak Period Jitter	f_{VCO_OUT}	1000 MHz	-30	-	30	ps
I_{VDD_PLL}(2)	PLL power consumption on $V_{DD_PLL\ (Analog)}$	VCO freq = 2000 MHz		-	1000	1050	µA
		VCO freq = 992 MHz		-	560	600	
$I_{VDDCORE}$(2)	PLL power consumption on $V_{DDCORE\ (Digital)}$	VCO freq = 2000 MHz (V_{DDCORE} = 1.26 V)		-	4300	10000	µA
		VCO freq = 992 MHz (V_{DDCORE} = 1.26 V)		-	2300	7000	

1. Specified by design, not tested in production unless otherwise specified.
2. Evaluated by characterization, not tested in production.
3. Measured on DDR high speed IO.
4. Measured on DDR high speed IO for 10000 output clock cycles.

PLL2 characteristics

Table 41. PLL2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Normal mode and Sigma delta mode	8	-	16	MHz
	PLL input clock duty cycle	-	10	-	90	%
$f_{PLL_P_Q_R_OUT}$	PLL P,Q,R multiplier output clock	-	3.125	-	800(2)	MHz
	PLL P,Q,R clock duty cycle	Division by 1	45	50	55	%
		Even divisions (N multiple of 2)	45	50	55	
		Odd divisions (N not multiple of 2)	[100×(N+1)/2N] - 5	[100×(N+1)/2N]	[100×(N+1)/2N] + 5	
f_{VCO_OUT}	PLL VCO output	Direct VCO clock after internal divider/2	400	-	800	MHz
	PLL VCO Duty Cycle		45	50	55	%
t_{LOCK}	PLL lock time	Normal mode	-	50	150	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)	-	65	170	
A_{LOCK}	Lock Accuracy (Ratio VCO frequency versus target frequency at lock)	-	-	-	±2	%

Table 41. PLL2 characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter	RMS cycle-to-cycle jitter	$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 Without Fractional mode	VCO = 800 MHz	-	18(3)	-	±ps
			VCO = 1066 MHz	-	14(3)	-	
			VCO = 1600 MHz	-	12(3)	-	
		$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 With Fractional mode	VCO = 1066 MHz	-	20(3)	-	
			VCO = 1600 MHz	-	18(3)	-	
	RMS period jitter	$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 Without Fractional mode	VCO = 800 MHz	-	16(3)	-	±ps
			VCO = 1066 MHz	-	12(3)	-	
			VCO = 1600 MHz	-	10(3)	-	
		$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 With Fractional mode	VCO = 1066 MHz	-	16(3)	-	
			VCO = 1600 MHz	-	15(3)	-	
	Long term jitter	$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 f_{PLL_IN} = 8 MHz Without Fractional mode	VCO = 800 MHz	-	225(4)	-	ps
			VCO = 1066 MHz	-	200(4)	-	
			VCO = 1600 MHz	-	100(4)	-	
		$f_{PLL_P_Q_R_OUT}$ division = 1 to 16 f_{PLL_IN} = 8 MHz With Fractional mode	VCO = 800 MHz	-	350(4)	-	
			VCO = 1066 MHz	-	250(4)	-	
			VCO = 1600 MHz	-	150(4)	-	
I_{VDD_PLL}(2)	PLL power consumption on $V_{DD_PLL\ (Analog)}$	VCO freq = 1600 MHz		-	930	-	µA
		VCO freq = 800 MHz		-	560	-	
$I_{VDDCORE}$(2)	PLL power consumption on $V_{DDCORE\ (Digital)}$	VCO freq = 1600 MHz (V_{DDCORE} = 1.26 V)		-	4200	-	µA
		VCO freq = 800 MHz (V_{DDCORE} = 1.26 V)		-	2100	-	

1. Specified by design, not tested in production unless otherwise specified.
2. Evaluated by characterization, not tested in production.
3. Measured on DDR high speed IO.
4. Measured on DDR high speed IO for 10000 output clock cycles.

PLL3, PLL4 characteristics

Table 42. PLL3, PLL4 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Normal mode	4	-	16	MHz
	-	Sigma delta mode	8	-	16	
	PLL input clock duty cycle	-	10	-	90	%

Table 42. PLL3, PLL4 characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{PLL_P_Q_R_OUT}$	PLL P,Q,R multiplier output clock	-		3.125	-	800(2)	MHz
	PLL P,Q,R clock duty cycle	Even divisions (N multiple of 2)		45	50	55	%
		Odd divisions (N not multiple of 2)		[100×(N+1)/2N] - 5	[100×(N+1)/2N]	[100×(N+1)/2N] + 5	
f_{VCO_OUT}	PLL VCO output	Direct VCO clock (no internal divider/2)		400	-	800	MHz
	PLL VCO Duty Cycle			40	-	60	%
t_{LOCK}	PLL lock time	Normal mode		15	50	150	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)		25	65	170	
A_{LOCK}	Lock accuracy (Ratio VCO frequency versus target frequency at lock)	-		-	-	±2	%
Jitter	RMS cycle-to-cycle jitter	$f_{PLL_P_Q_R_OUT}$ division = 25 to 100 Without Fractional mode	VCO = 400 MHz	-	80(3)	-	±ps
			VCO = 600 MHz	-	50(3)	-	
			VCO = 800 MHz	-	45(3)	-	
		$f_{PLL_P_Q_R_OUT}$ division = 25 to 100 With Fractional mode	VCO = 600 MHz	-	65(3)	-	
			VCO = 800 MHz	-	60(3)	-	
	RMS period jitter	$f_{PLL_P_Q_R_OUT}$ division = 25 to 100 Without Fractional mode	VCO = 400 MHz	-	75(3)	-	±ps
			VCO = 600 MHz	-	38(3)	-	
			VCO = 800 MHz	-	30(3)	-	
		$f_{PLL_P_Q_R_OUT}$ division = 25 to 100 With Fractional mode	VCO = 600 MHz	-	55(3)	-	
			VCO = 800 MHz	-	50(3)	-	
	Long term jitter	$f_{PLL_P_Q_R_OUT}$ division = 25 to 100 f_{PLL_IN} = 8 MHz Without Fractional mode	VCO = 400 MHz	-	225(4)	-	ps
			VCO = 600 MHz	-	150(4)	-	
			VCO = 800 MHz	-	125(4)	-	
		$f_{PLL_P_Q_R_OUT}$ division = 25 to 100 f_{PLL_IN} = 8 MHz With Fractional mode	VCO = 400 MHz	-	300(4)	-	
			VCO = 600 MHz	-	200(4)	-	
			VCO = 800 MHz	-	150(4)	-	
I_{VDD_PLL}	PLL power consumption on $V_{DD_PLL\ (Analog)}$	VCO freq = 800 MHz		-	600	610	µA
		VCO freq = 400 MHz		-	320	350	

Table 42. PLL3, PLL4 characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDDCORE}$	PLL power consumption on $V_{DDCORE\ (Digital)}$	VCO freq = 800 MHz (V_{DDCORE} = 1.26 V)	-	2200	5250	µA
		VCO freq = 400 MHz (V_{DDCORE} = 1.26 V)	-	1130	4550	

1. Specified by design, not tested in production unless otherwise specified.
2. Evaluated by characterization, not tested in production.
3. Measured on GPIO.
4. Measured on GPIO for 10000 output clock cycles.

PLL_USB (2880 MHz) characteristics

Table 43. USB_PLL characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock		19.2	24	38.4	MHz
f_{PLL_INFIN}	PFD input clock		19.2	24	38.4	MHz
f_{PLL_OUT}	PLL multiplier output clock		-	480	-	MHz
f_{VCO_OUT}	PLL VCO output		-	2880	-	MHz
t_{LOCK}	PLL lock time		-	-	100	µs
t_{PDN}	PLL power down time		10	-	-	µs
$I_{DDA1V1_REG(PLL)}$	PLL power consumption on V_{DDA1V1_REG} (internal connection)	PLL in power down	-	5	425	µA
		f_{VCO_OUT} = 2880 MHz	-	4.4	5.6	mA
$I_{DDA1V8_REG(PLL)}$	PLL power consumption on V_{DDA1V8_REG} (internal connection)	PLL in power down	-	-	2	µA
		f_{VCO_OUT} = 2880 MHz	-	2	2.5	mA

1. Specified by design, not tested in production unless otherwise specified.

6.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows the reduction of electromagnetic interferences (see *Table 49: EMI characteristics for fHSE = 24 MHz and Fmpuss_ck = 650 MHz*).

Table 44. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	20	-	60	kHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	2^{15}-1	-

1. Specified by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and fMod must be expressed in Hz.

As an example:

If f_{PLL_IN} = 8 MHz, and f_{MOD} = 40 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[8 \times 10^6 / 4 \times 40 \times 10^3] = 50$$

Equation 2

Equation 2 allows the increment step (INCSTEP) calculation:

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2% (4% peak-to-peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 50)] = 629 md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (50 \times 629 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2\%(peak)$$

Figure 20 and *Figure 21* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 20. PLL output clock waveforms in center spread mode

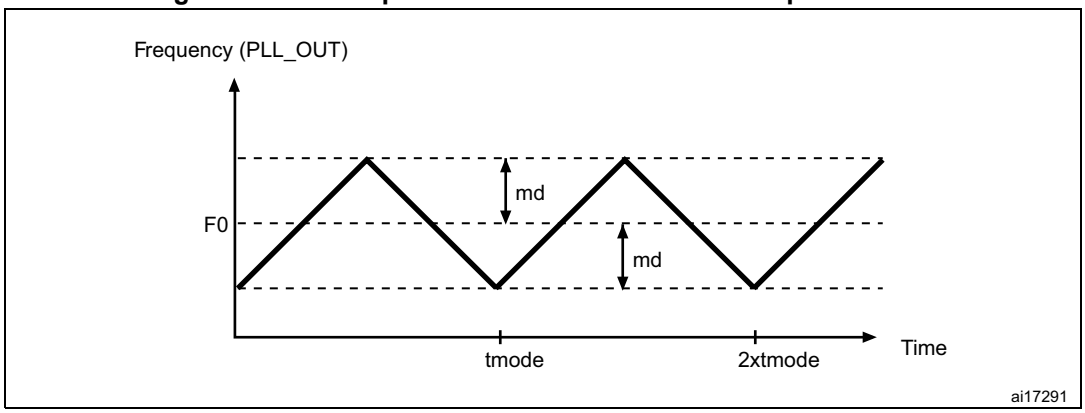
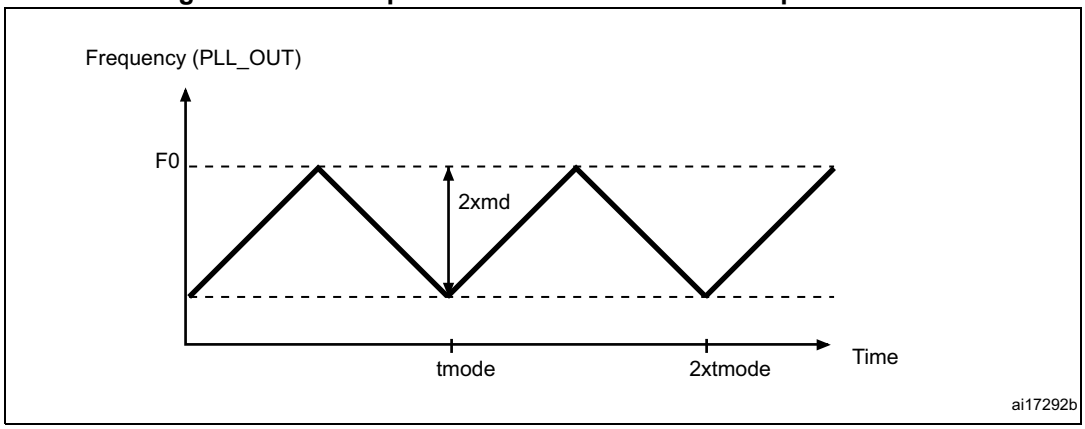


Figure 21. PLL output clock waveforms in down spread mode



6.3.13 Memory characteristics

OTP characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 45. OTP characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{VDDCORE}$	OTP consumption on V_{DDCORE}	Programming	-	450	µA
		Reading	-	490	µA
		PowerDown	-	4.2	µA
I_{VDD}	OTP consumption on V_{DD}	Programming	-	10000	µA
		Reading	-	2200	µA
		PowerDown	-	1	µA
F_{OTP} (1)	OTP operating Frequency	-	-	67	MHz
NB_CYCLE (2)	Maximum number of reading cycles	-	-	500	Million

1. Specified by design, not tested in production.
2. Evaluated by characterization, not tested in production.

DDR characteristics

DDR3, DDR3L I/O DC specifications

The following table provides input and output DC threshold values and on-die-termination (ODT) recommended values. The conditions for the output threshold values are un-terminated outputs loaded with 1 pF capacitor load. The ODT values are measured after impedance calibration.

Table 46. DC specifications – DDR3 or DDR3L mode(1)

Symbol	Parameter	Min	Typ	Max	Unit
$V_{IH(DC)}$	DC input voltage high	V_{REF} + 0.09	-	V_{DDQ}	V
$V_{IL(DC)}$	DC input voltage low	V_{SSQ} - 0.3	-	V_{REF} - 0.09	V
V_{OH}	DC output logic high	0.8 × V_{DDQ}	-	-	V
V_{OL}	DC output logic low	-	-	0.2 × V_{DDQ}	V
R_{TT}	Input termination resistance (ODT) to V_{DDQ}/2	100 54 36	120 60 40	140 66 44	Ω
I_{LS}	Input leakage current, SSTL mode, unterminated	-	0.01	4.8	µA

1. Specified by design, not tested in production.

LPDDR2, LPDDR3 I/O DC specifications

The following table provides input and output DC threshold values. The conditions for the output threshold values are un-terminated outputs loaded with 1 pF capacitor load.

Table 47. DC specifications – LPDDR2 or LPDDR3 mode(1)

Symbol	Parameter	Min	Typ	Max	Unit
$V_{IH(DC)}$	DC input voltage high	V_{REF} + 0.13	-	V_{DDQ}	V
$V_{IL(DC)}$	DC input voltage low	V_{SSQ}	-	V_{REF} - 0.13	V
V_{OH}	DC output logic high	0.9 × V_{DDQ}	-	-	V
V_{OL}	DC output logic low	-	-	0.1 × V_{DDQ}	V
ILEAK	Input leakage current	-	0.01	4.51	µA

1. Specified by design, not tested in production.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: a burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709 available from the ST website *www.st.com*.

Table 48. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, TFBGA320, F_{mpuss_ck} = 650 or 1000 MHz, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ), located as close as possible to the STM32MP131 device, to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened

to prevent unrecoverable errors occurring (see application note AN1015 available from the ST website *www.st.com*.).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 49. EMI characteristics for f_{HSE} = 24 MHz and F_{mpuss_ck} = 650 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak(1)	V_{DD} = 3.6 V, T_A = 25 °C, TFBFGA320 package, conforming to IEC61967-2	0.1 to 30 MHz	4	dBµV
			30 to 130 MHz	8	
			130 MHz to 1 GHz	21	
			1 GHz to 2 GHz	16	
	Level(2)	-	0.1 MHz to 2 GHz	3.5	-

1. Refer to AN1709 "EMI radiated test" section.
2. Refer to AN1709 "EMI level classification" section.

Table 50. EMI characteristics for f_{HSE} = 24 MHz and F_{mpuss_ck} = 1 GHz

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak(1)	V_{DD} = 3.6 V, T_A = 25 °C, TFBFGA320 package, conforming to IEC61967-2	0.1 to 30 MHz	4	dBµV
			30 to 130 MHz	16	
			130 MHz to 1 GHz	19	
			1 GHz to 2 GHz	20	
	Level(2)	-	0.1 MHz to 2 GHz	4	-

1. Refer to AN1709 "EMI radiated test" section.
2. Refer to AN1709 "EMI level classification" section.

6.3.15 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 51. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All	C2a	500	

1. Evaluated by characterization, not tested in production.

Static latchup

Two complementary static tests are required on three parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 52. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	130 °C conforming to JESD78	II level A

6.3.16 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the device in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 53. I/O current injection susceptibility(1)

Symbol	Description	Negative injection	Positive injection	Unit
I_{INJ}	PB5, PE13	0	NA	mA
	All other FTxx I/Os	5	NA	

1. Evaluated by characterization, not tested in production.

6.3.17 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 54: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 13: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 54. I/O static characteristics

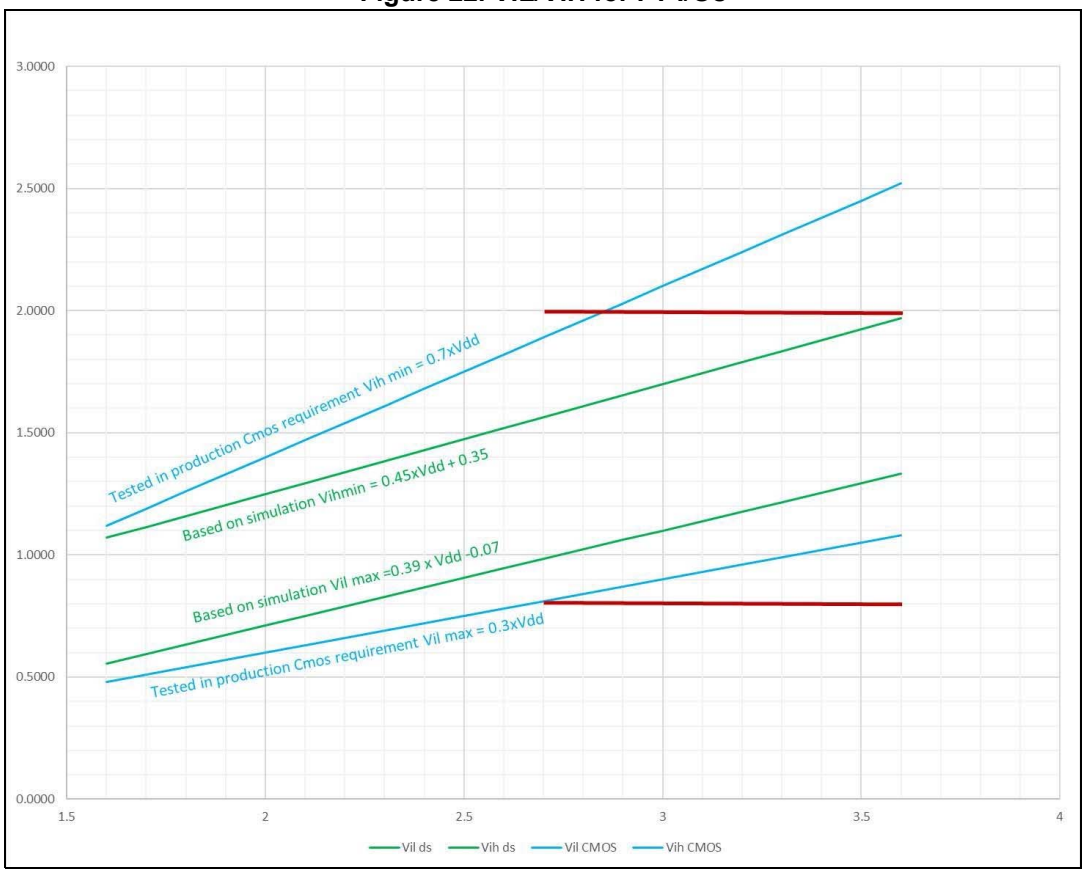
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage	1.71 V < V_{DD} < 3.6 V	-	-	0.3 × V_{DD}(1)	V
			-	-	0.39 x V_{DD} - 0.07(2)	
V_{IH}	I/O input high level voltage	1.71 V < V_{DD} < 3.6 V	0.7 × V_{DD}(1)	-	-	V
			0.45 × V_{DD} + 0.35(2)	-	-	
V_{HYS}	TT_xx, FT_xxx and NRST I/O input hysteresis	1.71 V < V_{DD} < 3.6 V	-	0.1 × V_{DD}	-	mV
I_{leak}	FT_xx input leakage current	0 < V_{IN} ≤ Max(V_{DD})(5)	-	-	250	nA
		Max(V_{DD}) < V_{IN} ≤ 5.5 V (3)(4)(5)	-	-	3500	
	FT_u, IO	0 < V_{IN} ≤ Max(V_{DD})(5)	-	-	500	
		Max(V_{DD}) < V_{IN} ≤ 5.5 V (3)(4)(5)	-	-	5000(6)	
	TT_xx input leakage current	0 < V_{IN} ≤ Max(V_{DD}) (5)	-	-	100	
R_{PU}	Weak pull-up equivalent resistor(7)	V_{IN}=V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	V_{IN}=V_{DD}(5)	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Compliant with CMOS requirements.
2. Specified by Design, not tested in production.
3. All FT_xx IO except FT_uf, FT_u.
4. V_{IN} must be less than Max(V_{DD}) + 3.6 V.
5. Max(V_{DD}) is the maximum value of all the I/O supplies.
6. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DD3V3_USBHS}) +0.3 V, the internal pull-up and pull-down resistors must be disabled.

7. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 22*.

Figure 22. VIL/VIH for FT I/Os



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run mode consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating $\sum I_{VDD}$ (see *Table 11*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run mode consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $\sum I_{VSS}$ (see *Table 11*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 55. Output voltage characteristics for all I/Os except PC13, PC14, PC15, PI0 PI1, PI2, PI3[1]

Symbol	Parameter	Conditions[3]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port[2] I_{IO} = 8 mA 2.0 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[2] I_{IO} = -8 mA 2.0 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}[3]	Output low level voltage	TTL port[2] I_{IO} = 8 mA 2.0 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[3]	Output high level voltage	TTL port[2] I_{IO} = -8 mA 2.0 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}[3]	Output low level voltage	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}[3]	Output high level voltage	I_{IO} = -20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}[3]	Output low level voltage	I_{IO} = 1 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.2	
		I_{IO} = 4 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.45	
V_{OH} [3]	Output high level voltage	I_{IO} = -1 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.2	-	
		I_{IO} = -4 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.45	-	
V_{OLFM+}[3]	Output low level voltage for an FT_f IO pin in FM+ mode	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 10 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 10: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ∑IIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design, not tested in production.

Table 56. Output voltage characteristics for PC13, PC14, PC15, PI0, PI1, PI2, PI3[1]

Symbol	Parameter	Conditions[3]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port[2] I_{IO} = 3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[2] I_{IO} = -3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4	-	
V_{OL}[3]	Output low level voltage	TTL port[2] I_{IO} = 3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[2]	Output high level voltage	TTL port[2] I_{IO} = -3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}[2]	Output low level voltage	I_{IO} = 1.5 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[2]	Output high level voltage	I_{IO} = -1.5 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 10: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design, not tested in production.

Output buffer timing characteristics (HSLV option disabled)

Table 57. Output timing characteristics (HSLV OFF)(1)(2)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	21	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	23	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	9	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	8	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	22	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	19	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	17	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	15	
01	F_{max}(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	33	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	44	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	66	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	15	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	15	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	15	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	15	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	6.2	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.2	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.5	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.6	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	11.0	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	9.0	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	8.0	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	7.0	

Table 57. Output timing characteristics (HSLV OFF)(1)(2) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	83	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	100	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	133	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	166	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	32	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	37	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	42	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	50	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	3.5	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	2.7	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	2.2	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	1.6	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	6.6	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	5.0	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	4.2	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	3.3	
11	F_{max}(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	133	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	166	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	200	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	233	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	45	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	50	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	55	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	60	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	2.9	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	2.0	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	1.7	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	1.3	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	5.4	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	4.0	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	3.3	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	2.5	

1. Specified by design, not tested in production.
2. GPIO under VSW domain (PC13, PC14, PC15, PI0, PI1, PI2, PI3) are frequency limited. The maximum frequency is 2 MHz with a maximum load of 30 pF. Only one I/O at a time can be used as GPIO output and these I/Os must not be used as a current source (e.g to drive a LED). For theses IOs, the speed value must be kept to (default) 00.

3. The maximum frequency is defined with the following conditions: $(t_r+t_f) \leq 2/3$, skew ≤ 1/20 T and 45% < duty cycle < 55%.
4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
5. Compensation system enabled.

Output buffer timing characteristics (IO structure with _h, HSLV option enabled)

The HSLVEN bits of SYSCFG_HSLVENxR register (together with OTP bit PRODUCT_BELOW_2V5) can be used to optimize the I/O speed when the product voltage is below 2.5 V typ. (2.7 V max.).

Table 58. Output timing characteristics (HSLV ON, _h IO structure)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	21	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	23	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	25	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	27	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	12.5	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	10.5	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	9	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	7.5	
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	33	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	44	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	55	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	66	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	7.3	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5.7	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	4.8	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	3.8	
10	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	66	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	90	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	110	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	133	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	5.0	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	3.5	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.7	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.0	

Table 58. Output timing characteristics (HSLV ON, _h IO structure)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
11	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	100	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	133	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	166	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	200	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	4.6	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	3.1	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.4	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	1.7	

1. Specified by design, not tested in production.
2. The maximum frequency is defined with the following conditions: (t_r+t_f) ≤ 2/3, skew ≤ 1/20 T and 45% < duty cycle < 55%.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Output buffer timing characteristics (IO structure with _vh, HSLV option disabled)

Table 59. Output timing characteristics (HSLV OFF, _vh IO structure)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 10, 20, 30, 50 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	17	MHz
			C = 10, 20, 30, 50 pF, 1.71 V ≤ V_{DDIOX} ≤ 2.7 V	-	5	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 10, 20, 30, 50 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	12	ns
			C = 10, 20, 30, 50 pF, 1.71 V ≤ V_{DDIOX} ≤ 2.7 V	-	22	
01	F_{max}(2)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	33	MHz
			C = 30 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	44	
			C = 20 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	55	
			C = 10 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	66	
			C = 10, 20, 30, 50 pF, 1.71 V ≤ V_{DDIOX} ≤ 2.7 V	-	15	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	6.2	ns
			C = 30 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	5.2	
			C = 20 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	4.5	
			C = 10 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	3.6	
			C = 10, 20, 30, 50 pF, 1.71 V ≤ V_{DDIOX} ≤ 2.7 V	-	11.0	

Table 59. Output timing characteristics (HSLV OFF, _vh IO structure)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}(2)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	83	MHz
			C = 30 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	100	
			C = 20 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	133	
			C = 10 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	166	
			C = 10, 20, 30, 50 pF, 1.71 V ≤ V_{DDIOX} ≤ 2.0 V(4)	-	30	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	3.5	ns
			C = 30 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	2.7	
			C = 20 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	2.2	
			C = 10 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	1.6	
			C = 10, 20, 30, 50 pF, 1.71 V ≤ V_{DDIOX} ≤ 2.0 V(4)	-	6.6	
11	F_{max}(2)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	133	MHz
			C = 30 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	166	
			C = 20 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	200	
			C = 10 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	233	
			C = 10, 20, 30, 50 pF, 1.71 V ≤ V_{DDIOX} ≤ 2.0 V(4)	-	45	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	2.9	ns
			C = 30 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	2.0	
			C = 20 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	1.7	
			C = 10 pF, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V(4)	-	1.3	
			C = 10, 20, 30, 50 pF, 1.71 V ≤ V_{DDIOX} ≤ 2.0 V(4)	-	5.4	

1. Specified by design, not tested in production.
2. The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3, skew ≤ 1/20 T and 45% < Duty cycle < 55%.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Output buffer timing characteristics (IO structure with _vh, HSLV option enabled)

The HSLVEN bits of SYSCFG_HSLVENxR register (together with OTP bit PRODUCT_BELOW_2V5) can be used to optimize the I/O speed when the product voltage is below 2.5 V typ. (2.7 V max.).

Table 60. Output timing characteristics (HSLV ON, _vh IO structure)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	25	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	30	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	35	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	40	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	9.5	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	7.7	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	6.6	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5.4	
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	44	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	55	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	66	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	77	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	6.5	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	4.9	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	4.1	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	3.1	
10	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	66	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	90	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	110	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	133	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	5.1	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	3.6	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.8	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.1	
11	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	110	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	150	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	190	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	233	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	4.5	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	3.0	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.2	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	1.5	

1. Specified by design, not tested in production.
2. The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3, skew ≤ 1/20 T and 45% < Duty cycle < 55%.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

4. Compensation system enabled.

6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 54: I/O static characteristics*).

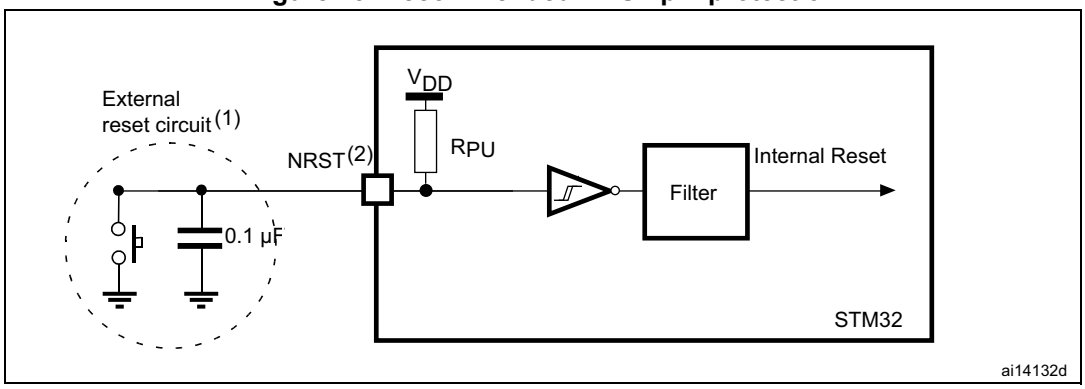
Unless otherwise specified, the parameters given in *Table 61* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 61. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST input not filtered pulse	1.71 V < V_{DD} < 3.6 V	350	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Specified by design, not tested in production.

Figure 23. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 54*. Otherwise the reset is not taken into account by the device.

6.3.19 FMC characteristics

Unless otherwise specified, the parameters given in *Table 62* to *Table 75* for the FMC interface are derived from tests performed under the ambient temperature, F_{mc_hclk} (F_{hclk6}) frequency and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5×V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

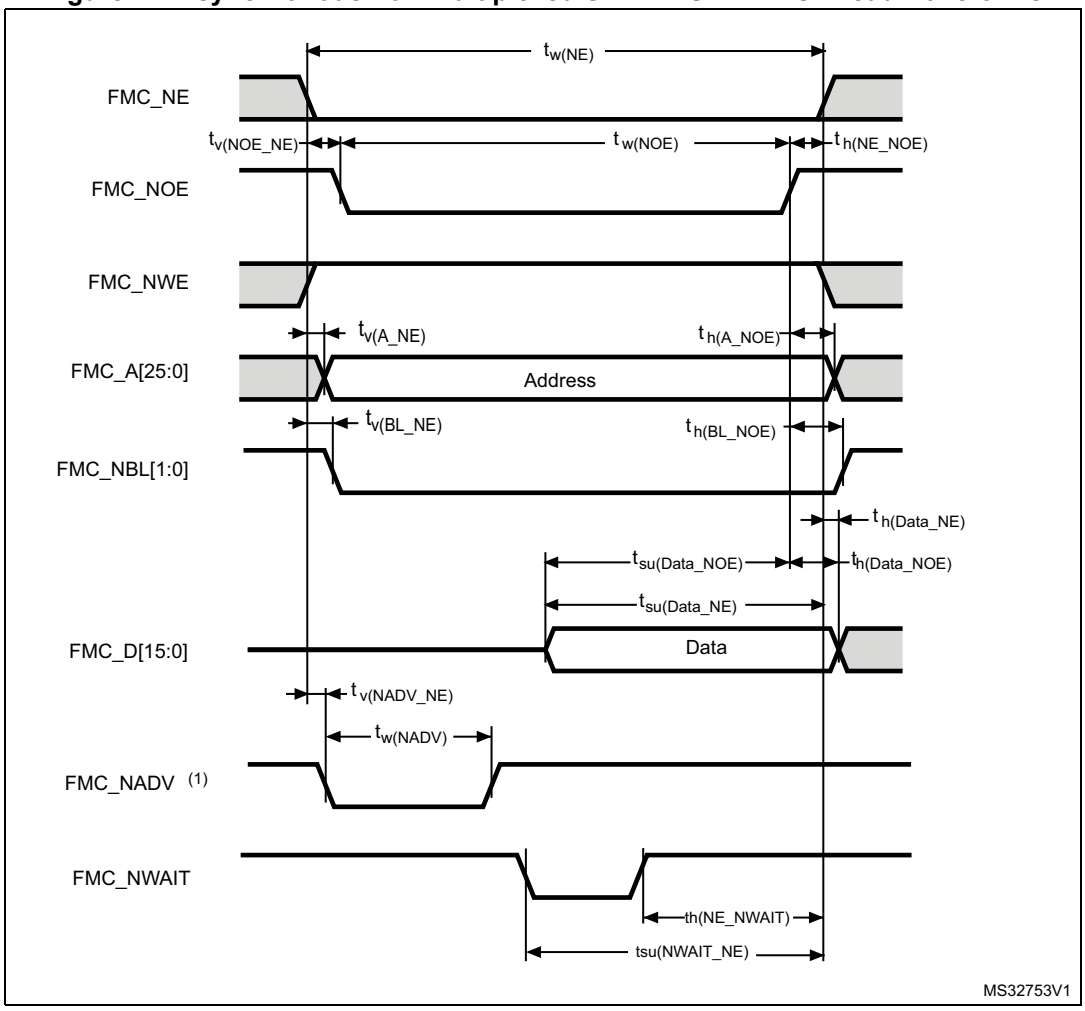
Asynchronous waveforms and timings

Figure 24 through *Figure 27* represent asynchronous waveforms and *Table 62* through *Table 69* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- DataHoldTime = 0x1 ($1 \times T_{fmc_ker_ck}$ for read operations and $2 \times T_{fmc_ker_ck}$ for write operations)
- ByteLaneSetup = 0x1
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all the timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Figure 24. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 62. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck}$-1	$3T_{fmc_ker_ck}$+0.5	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc_ker_ck}$-1	$2T_{fmc_ker_ck}$+0.5	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$-1	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$2T_{fmc_ker_ck}$-1	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck}$+15.5	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	16	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck}$+1	

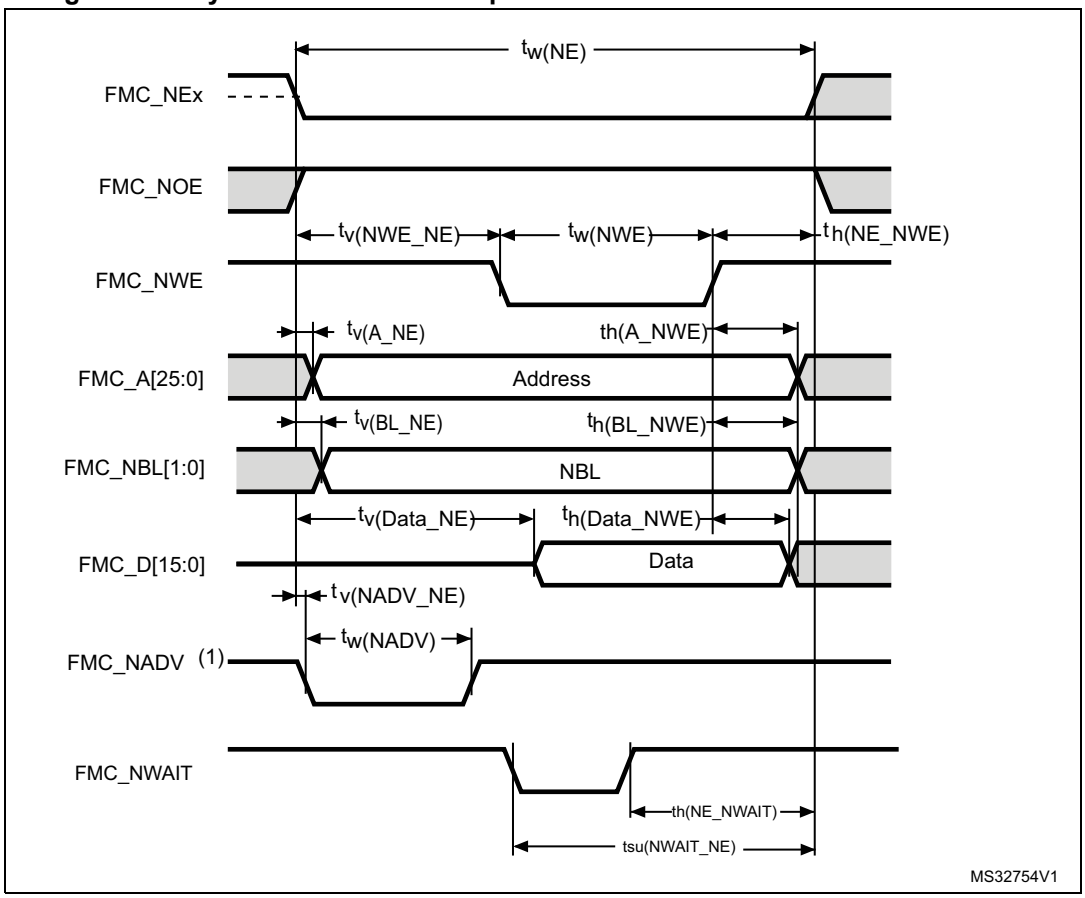
1. Evaluated by characterization, not tested in production.

Table 63. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{fmc_ker_ck}$-0.5	$7T_{fmc_ker_ck}$+1	ns
$t_{w(NOE)}$	FMC_NWE low time	$6T_{fmc_ker_ck}$-0.5	$6T_{fmc_ker_ck}$+1	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck}$	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$7T_{fmc_ker_ck}$+2	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$5T_{fmc_ker_ck}$	-	

1. Evaluated by characterization, not tested in production.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 25. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 64. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck}$-0.5	$4T_{fmc_ker_ck}$+0.5	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck}$-0.5	$T_{fmc_ker_ck}$+1	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck}$-0.5	$T_{fmc_ker_ck}$+0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{fmc_ker_ck}$-0.5	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$3T_{fmc_ker_ck}$-1	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$3T_{fmc_ker_ck}$-0.5	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	3.5	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$2T_{fmc_ker_ck}$-1	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck}$+1	

1. Evaluated by characterization, not tested in production.

Table 65. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck}$-0.5	$8T_{fmc_ker_ck}$+0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$5T_{fmc_ker_ck}$-0.5	$5T_{fmc_ker_ck}$+1	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$8T_{fmc_ker_ck}$+4	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$6T_{fmc_ker_ck}$	-	

1. Evaluated by characterization, not tested in production.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms

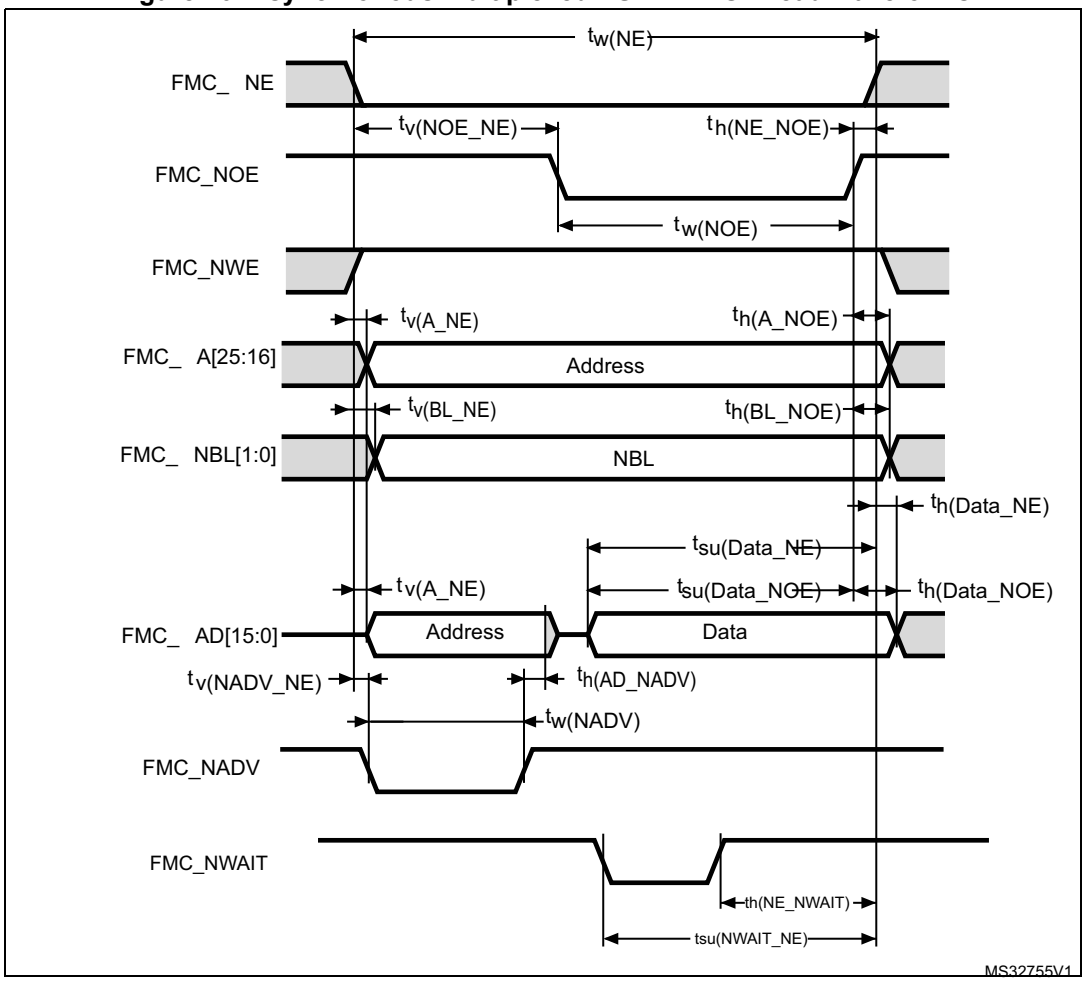


Table 66. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck}$-0.5	$4T_{fmc_ker_ck}$+1	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc_ker_ck}$-0.5	$2T_{fmc_ker_ck}$+1	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck}$-0.5	$T_{fmc_ker_ck}$+0.5	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$-1	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	4	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck}$	$T_{fmc_ker_ck}$+1	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck}$-3	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	Address held until next read operation	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck}$+15	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	16	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Evaluated by characterization, not tested in production.

Table 67. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck}$-0.5	$8T_{fmc_ker_ck}$+1	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc_ker_ck}$-0.5	$5T_{fmc_ker_ck}$+1	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$7T_{fmc_ker_ck}$+2	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$5T_{fmc_ker_ck}$	-	

1. Evaluated by characterization, not tested in production.

Figure 27. Asynchronous multiplexed PSRAM/NOR write waveforms

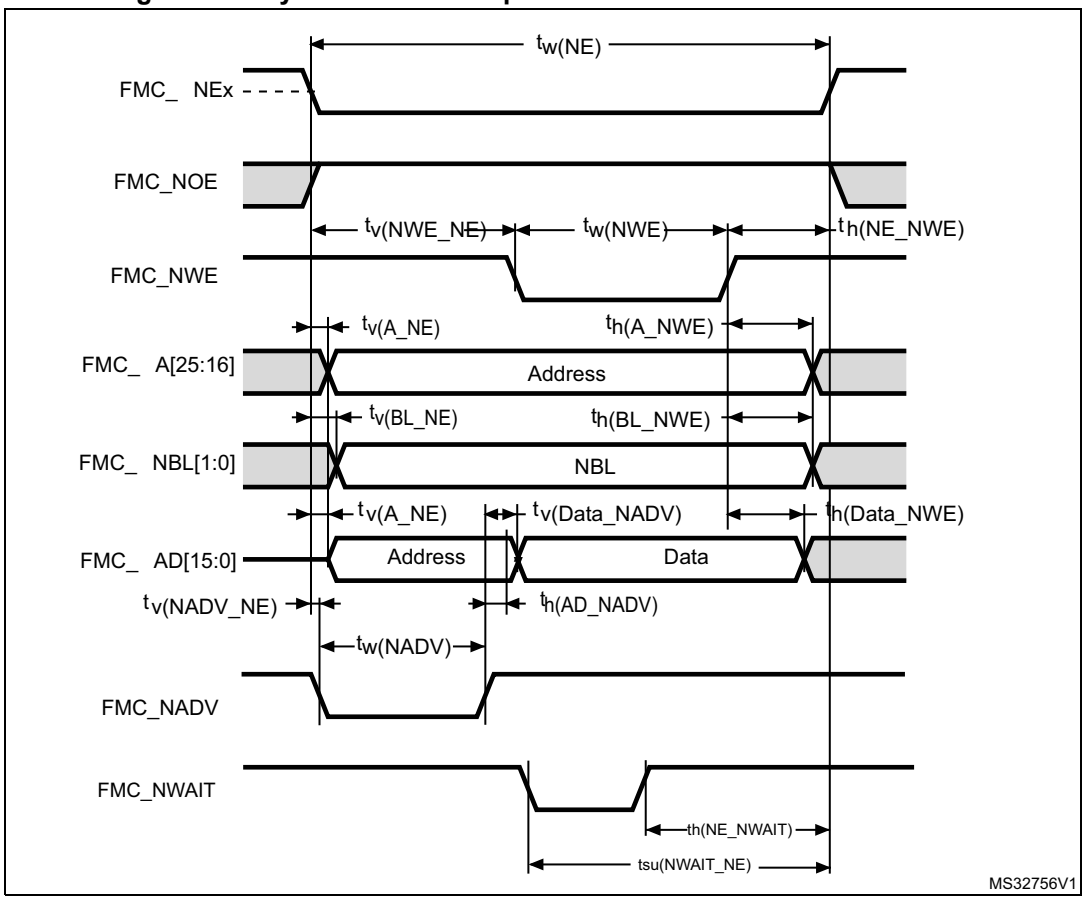


Table 68. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$5T_{fmc_ker_ck}$-0.5	$5T_{fmc_ker_ck}$+1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck}$-0.5	$T_{fmc_ker_ck}$+1	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc_ker_ck}$-1	$2T_{fmc_ker_ck}$+0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{fmc_ker_ck}$-0.5	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck}$+0.5	$T_{fmc_ker_ck}$+1.5	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck}$+0.5	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	Address held until next write operation	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$3T_{fmc_ker_ck}$-1	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc_ker_ck}$+5	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$2T_{fmc_ker_ck}$+0.5	-	

1. Evaluated by characterization, not tested in production.

Table 69. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck}$-0.5	$9T_{fmc_ker_ck}$+0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc_ker_ck}$-0.5	$6T_{fmc_ker_ck}$+1	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$8T_{fmc_ker_ck}$+4	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$6T_{fmc_ker_ck}$	-	

1. Evaluated by characterization, not tested in production.

Synchronous waveforms and timings

Figure 28 through *Figure 31* represent synchronous waveforms and *Table 70* through *Table 73* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period, with the following FMC_CLK maximum values:

Conditions: synchronous **read or write, NWAIT enabled**

- 2.7 V < V_{DD} < 3.6 V, FMC_CLK = 48 MHz at 20 pF
- 1.71 V < V_{DD} < 2.7 V, FMC_CLK = 30 MHz at 20 pF

Conditions: synchronous **read, NWAIT disabled**

- 2.7 V < V_{DD} < 3.6 V, FMC_CLK = 54 MHz at 20 pF
- 1.71 V < V_{DD} < 2.7 V, FMC_CLK = 34 MHz at 20 pF

Conditions: synchronous **write, NWAIT disabled**

- 2.7 V < V_{DD} < 3.6 V, FMC_CLK = 130 MHz at 20 pF
- 1.71 V < V_{DD} < 2.7 V, FMC_CLK = 78 MHz at 20 pF

Figure 28. Synchronous multiplexed NOR/PSRAM read timings

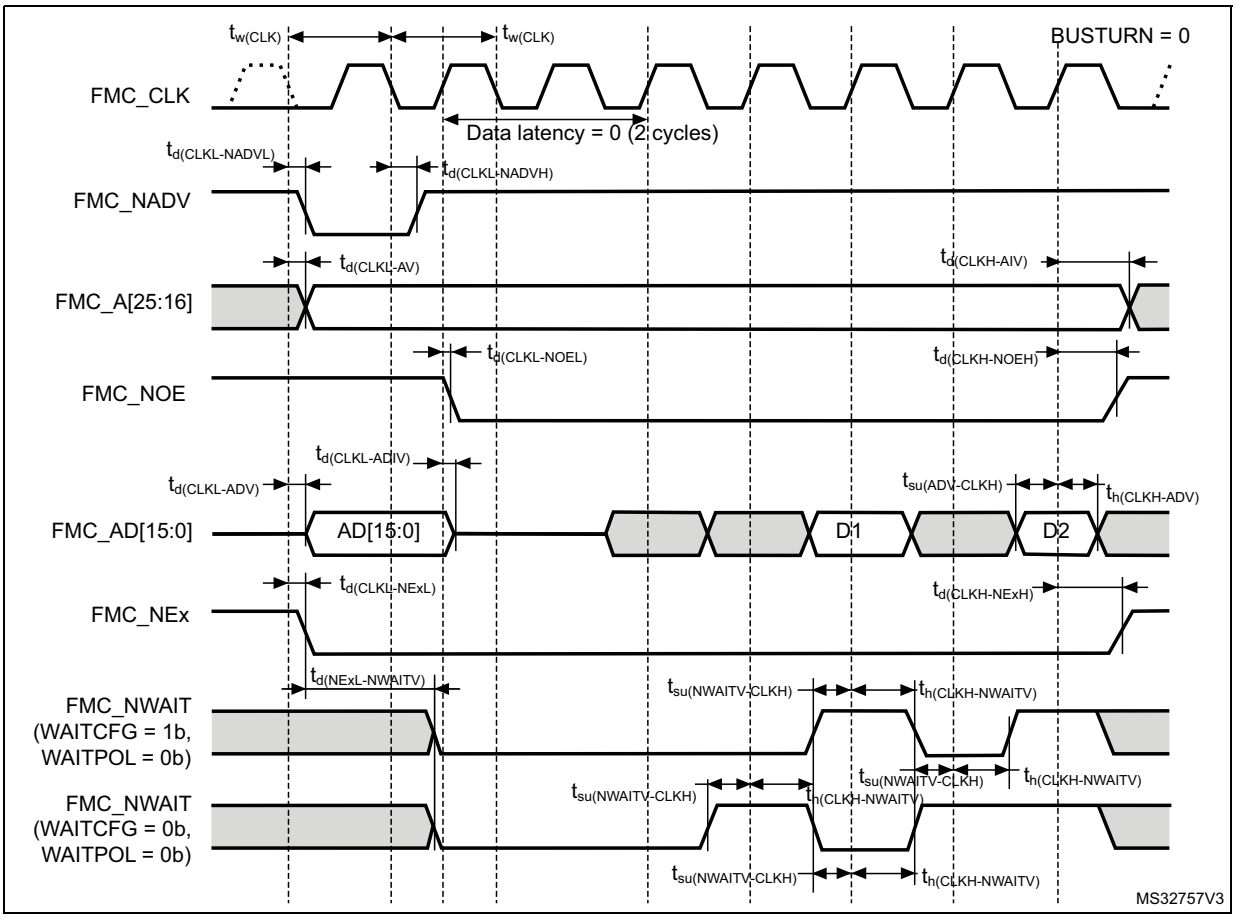


Table 70. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck}$-1(2)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0..2)	$R \times T_{fmc_ker_ck}/2+0.5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16..25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16..25)	$R \times T_{fmc_ker_ck}/2+1.5$(2)	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc_ker_ck}/2$(2)	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	1	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	3	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT active (x=0..2)	-	((DATLAT+2.5) × $t_{w(CLK)}$) - 4	

1. Evaluated by characterization, not tested in production.
2. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

Figure 29. Synchronous multiplexed PSRAM write timings

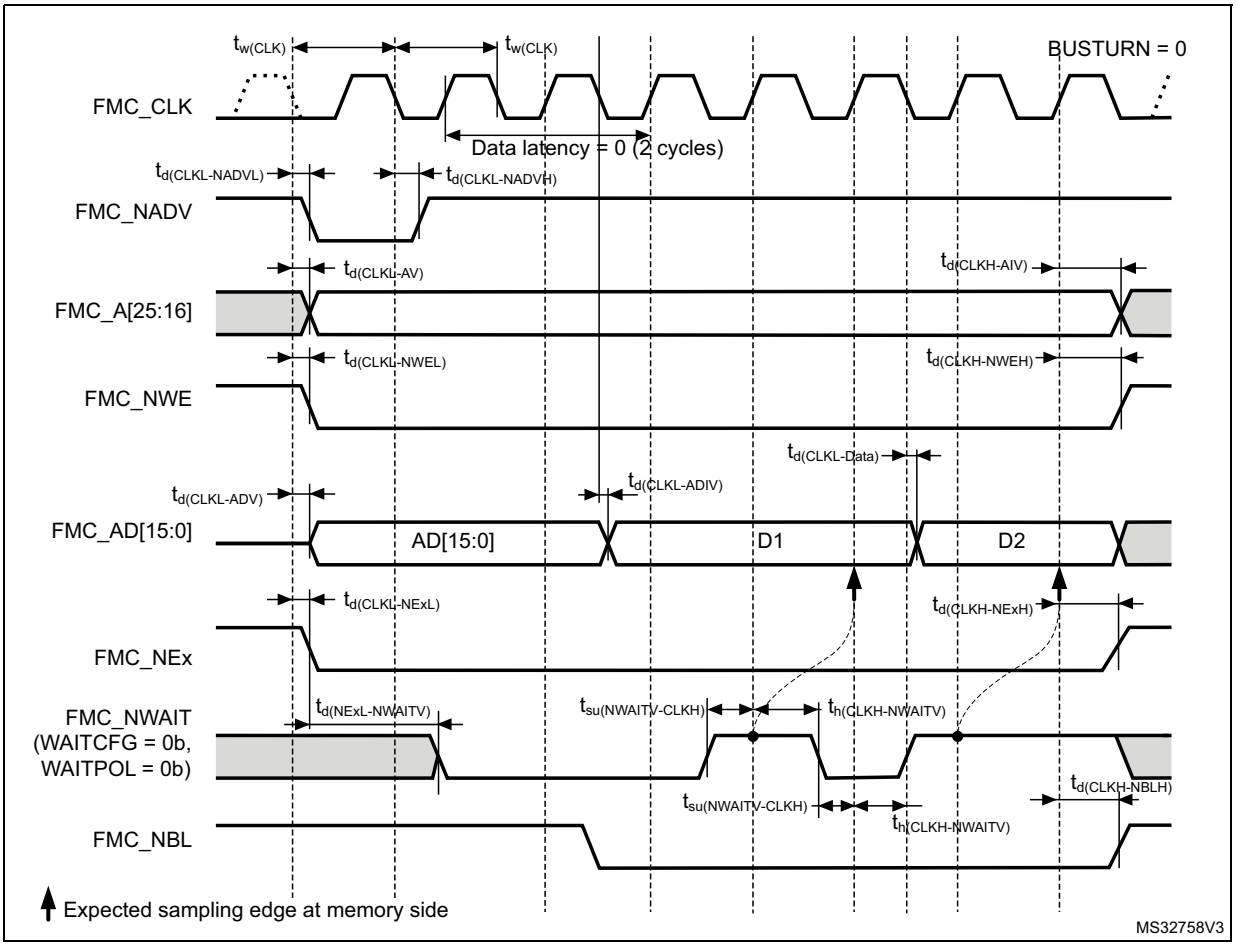


Table 71. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, V_{DD} range = 2.7 to 3.6 V	$R \times T_{fmc_ker_ck}-1$(2)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0..2)	$R \times T_{fmc_ker_ck}/2+0.5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16..25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16..25)	$R \times T_{fmc_ker_ck}/2+1.5$(2)	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R \times T_{fmc_ker_ck}/2+0.5$(2)	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	1.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	1	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc_ker_ck}/2+0.5$(2)	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT active (x=0..2)	-	$((DATLAT+2.5) \times t_{w(CLK)}) - 4$	

1. Evaluated by characterization, not tested in production.
2. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

Figure 30. Synchronous non-multiplexed NOR/PSRAM read timings

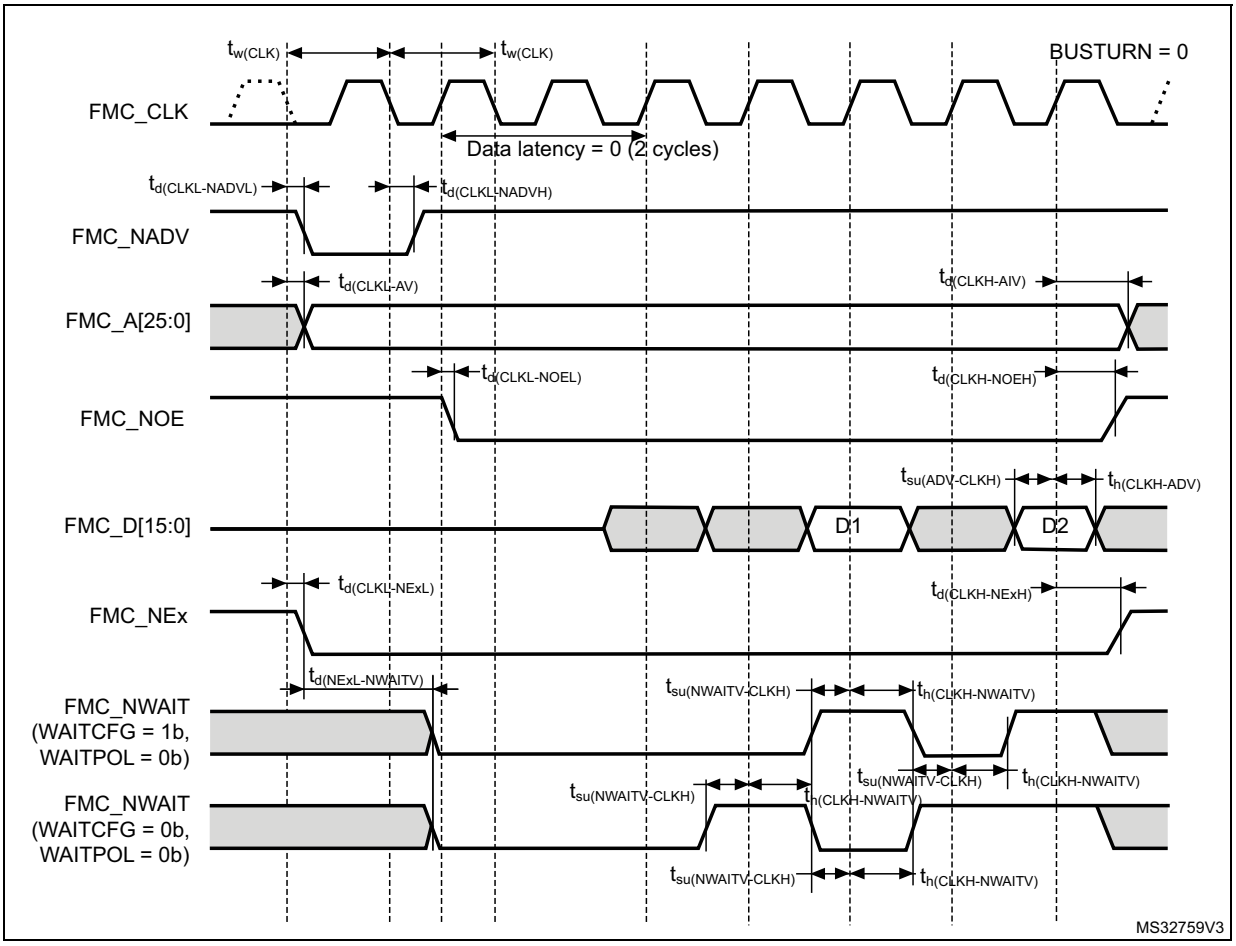


Table 72. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck}-1$(2)	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0..2)	$R \times T_{fmc_ker_ck}/2+0.5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=0..25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=0..25)	$R \times T_{fmc_ker_ck}/2+1.5$(2)	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc_ker_ck}/2+1.5$(2)	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	1	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT active (x=0..2)	-	$((DATLAT+2.5) \times t_{w(CLK)}) - 4$	

1. Evaluated by characterization, not tested in production.
2. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

Figure 31. Synchronous non-multiplexed PSRAM write timings

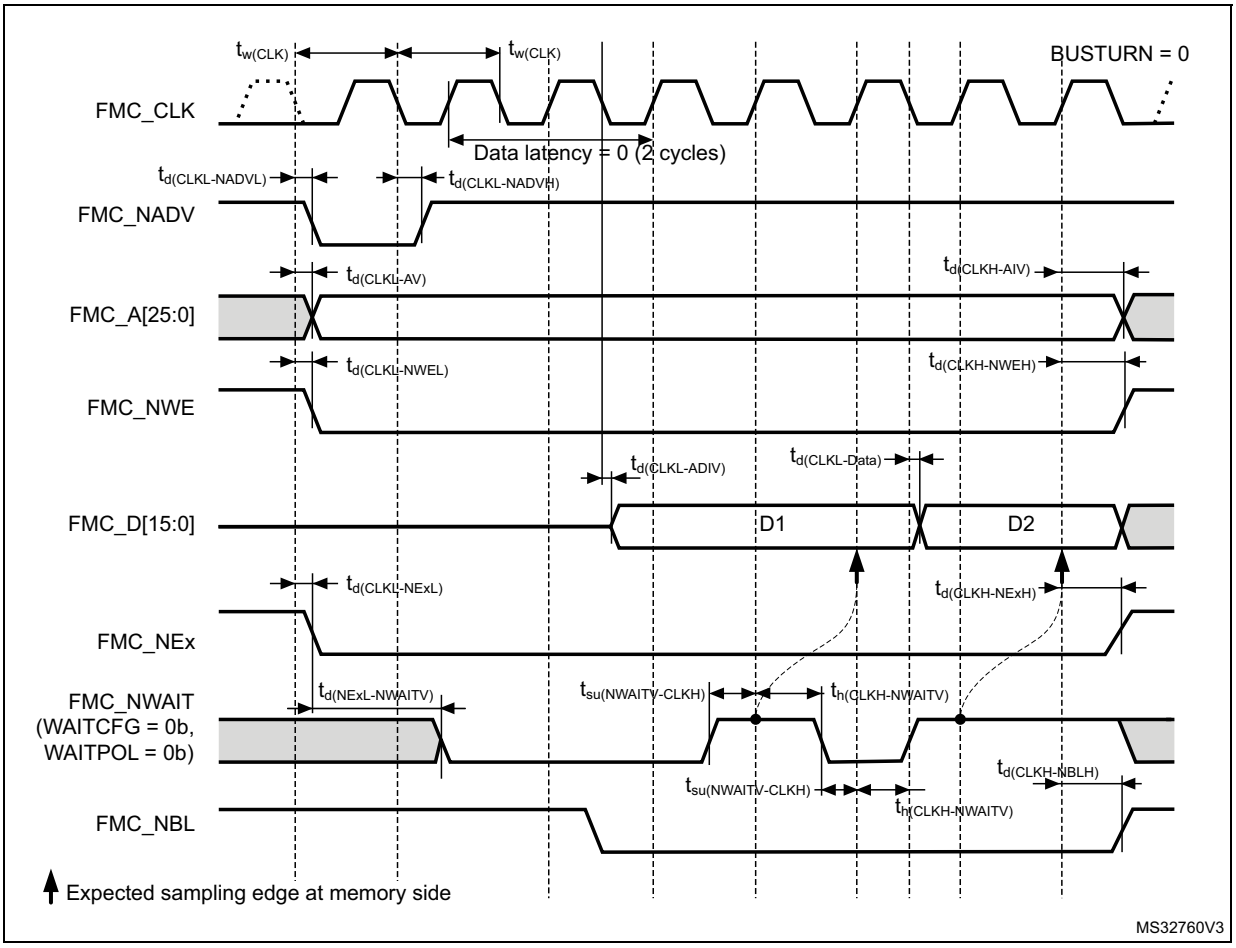


Table 73. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck}$ -1(2)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0..2)	$R \times T_{fmc_ker_ck}/2+0.5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=0..25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=0..25)	$R \times T_{fmc_ker_ck}/2+1.5$(2)	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R \times T_{fmc_ker_ck}/2+0.5$(2)	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc_ker_ck}/2+0.5$(2)	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT active (x=0..2)	-	((DATLAT+2.5) × $t_{w(CLK)}$) - 4	

1. Evaluated by characterization, not tested in production.
2. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

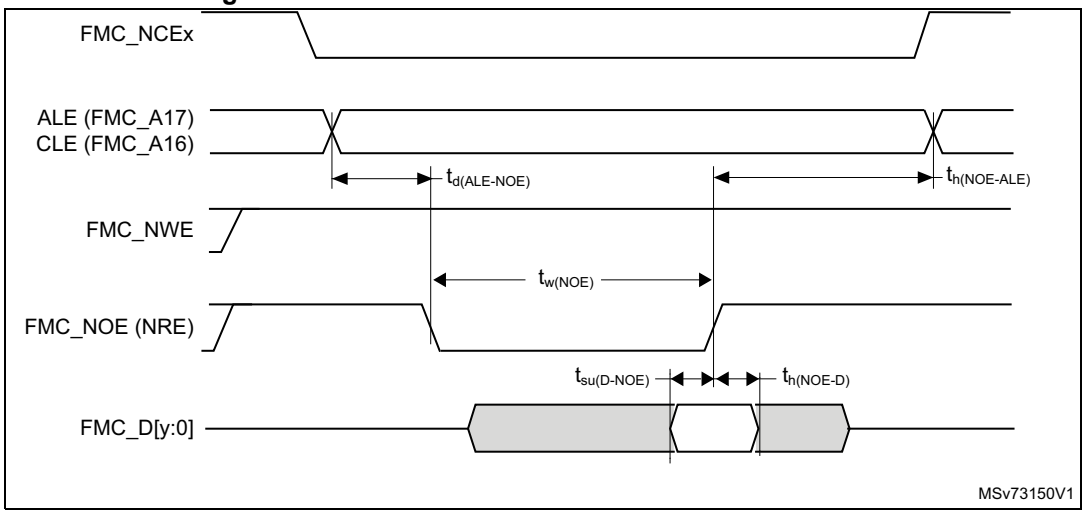
NAND controller waveforms and timings

Figure 32 and *Figure 33* represent synchronous waveforms, and *Table 74* and *Table 75* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- FMC_SetupTime = 0x01
- FMC_WaitSetupTime = 0x03
- FMC_HoldSetupTime = 0x02
- FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- C_L = 30 pF

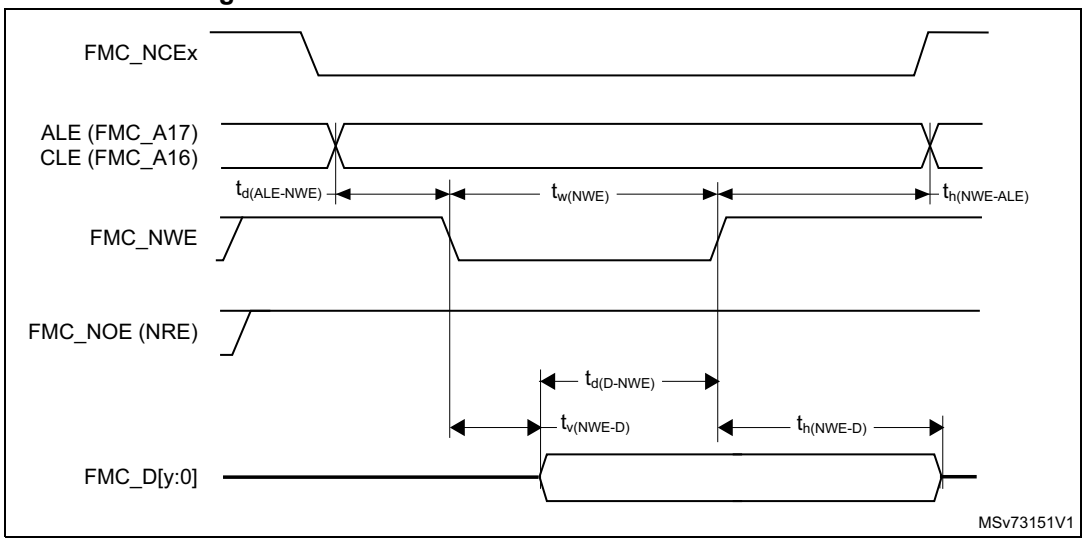
In all timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Figure 32. NAND controller waveforms for read access



1. y = 7 or 15 depending on the NAND flash memory interface.

Figure 33. NAND controller waveforms for write access



1. y = 7 or 15 depending on the NAND flash memory interface.

Table 74. Switching characteristics for NAND flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc_ker_ck}$-1	$4T_{fmc_ker_ck}$+1	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	11	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$2T_{fmc_ker_ck}$+1	
$t_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$3T_{fmc_ker_ck}$+0.5	-	

1. Evaluated by characterization, not tested in production.

Table 75. Switching characteristics for NAND flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc_ker_ck}$-1	$4T_{fmc_ker_ck}$+1	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$3T_{fmc_ker_ck}$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$4T_{fmc_ker_ck}$-3.5	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$2T_{fmc_ker_ck}$+1	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{fmc_ker_ck}$+0.5	-	

1. Evaluated by characterization, not tested in production.

6.3.20 QUADSPI interface characteristics

Unless otherwise specified, the parameters given in *Table 76* and *Table 77* for QUADSPI are derived from tests performed under the ambient temperature, F_{axiss_ck} frequency and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 76. QUADSPI characteristics in SDR mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1/t(CLK)}$	QUADSPI clock frequency	2.7 V ≤ V_{DD} < 3.6 V C_L = 20 pF	-	-	166	MHz
		1.71 V < V_{DD} <3.6 V C_L = 15 pF	-	-	90	
$t_{w(CLKH)}$	QUADSPI clock high and low time	Even clock division ratio	$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	
$t_{s(IN)}$	Data input setup time	-	2.5	-	-	
$t_{h(IN)}$	Data input hold time	-	1.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1	1.5	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

Table 77. QUADSPI characteristics in DDR mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1/t(CLK)}$	QUADSPI clock frequency	2.7 V < V_{DD} < 3.6 V CL=20 pF	-	-	90	MHz
		1.71 V < V_{DD} < 3.6 V CL=15 pF	-	-	90	
$t_{w(CLKH)}$	QUADSPI clock high and low time	Even clock division ratio	$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	-	2	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	-	1.5	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	DHHC = 0	-	1	1.5	
		DHHC = 1 Pres = 1, 2...	-	$t_{(CLK)}/4$+1	$t_{(CLK)}/4$+1.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	DHHC = 0	0	-	-	
		DHHC = 1 Pres = 1, 2...	$t_{(CLK)}/4$	-	-	

Figure 34. QUADSPI timing diagram - SDR mode

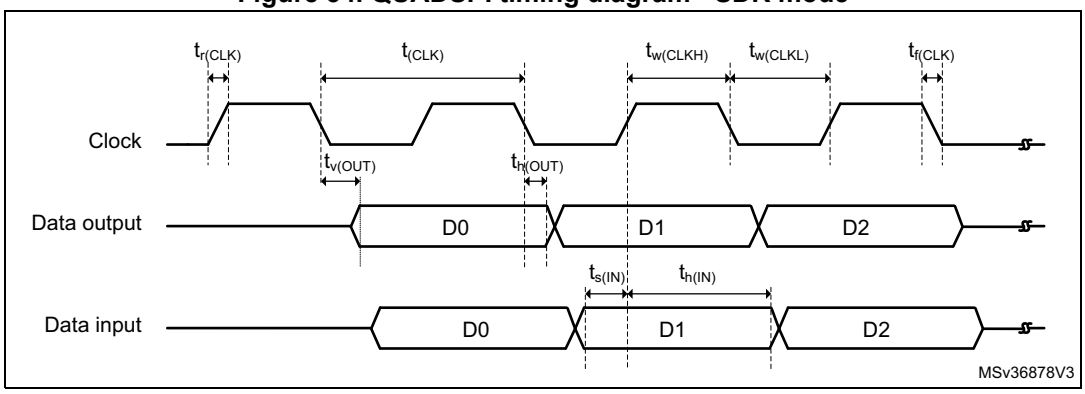
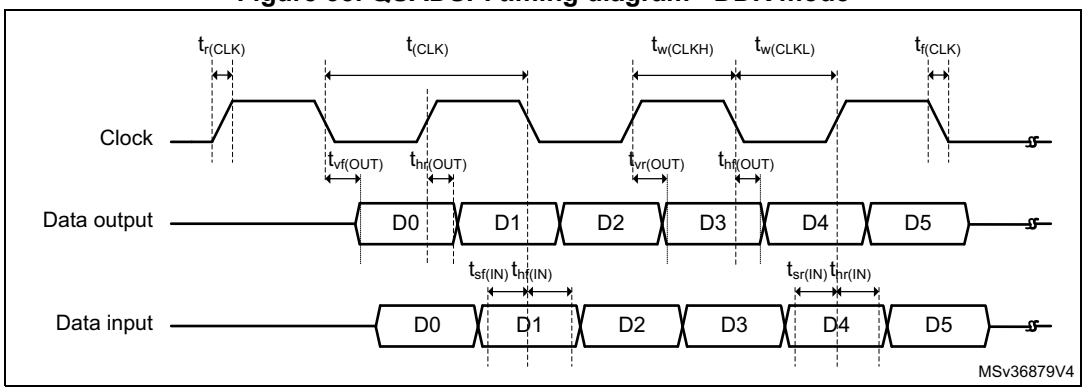


Figure 35. QUADSPI timing diagram - DDR mode



6.3.21 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 78* for the delay block are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in *Table 13: General operating conditions*.

Table 78. Dynamics characteristics: Delay block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	350	500	800	ps
t_{Δ}	Unit Delay	-	37	40	43	

6.3.22 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 79*, *Table 80* and *Table 81* are derived from tests performed under the ambient temperature and V_{DDA} supply voltage conditions summarized in *Table 13: General operating conditions*. In *Table 79*, *Table 80* and *Table 81*, f_{ADC} refers to $f_{adc_ker_ck}$.

Note: When both ADCs are used, the kernel clock should be the same for both ADCs and the embedded ADC prescalers cannot be used.

Table 79. 12-bit ADC characteristics(1)(2)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{DDA}	Analog power supply for ADC ON	-			1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq V_{REF+}$			1.62	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-			V_{SSA}	-	-	
f_{ADC}	ADC clock frequency	1,62 V ≤ V_{DDA} ≤ 3.6 V			1.5	-	75	MHz
f_S	Sampling rate for fast channels (VIN[0:5])	Resolution = 12 bits –40 °C ≤ T_J ≤ 125 °C SMP = 2.5	Continuous mode(3)	1.8 V ≤ V_{DDA} ≤ 3.6 V f_{ADC} = 75 MHz	-	-	5.00	MSPS
				1.62 V ≤ V_{DDA} ≤ 3.6 V f_{ADC} = 70 MHz	-	-	4.66	
			Single or Discontinuous mode	2.4 V ≤ V_{DDA} ≤ 3.6 V f_{ADC} = 60 MHz(4)	-	-	4.00	
				1.62 V ≤ V_{DDA} ≤ 3.6V f_{ADC} = 50 MHz(4)	-	-	3.33	
		Resolution = 10 bits –40 °C ≤ T_J ≤ 125 °C SMP = 2.5	Continuous mode(3)	1.62 V ≤ V_{DDA} ≤ 3.6V f_{ADC} = 75 MHz	-	-	5.77	
			Single or Discontinuous mode	2.4 V ≤ V_{DDA} ≤ 3.6 V f_{ADC} = 75 MHz(4)	-	-	5.77	
				1.62 V ≤ V_{DDA} ≤ 3.6V f_{ADC} = 65 MHz(4)	-	-	5.00	
		Resolution = 8 bits –40 °C ≤ T_J ≤ 125 °C SMP = 2.5	All modes(3)	1.62 V ≤ V_{DDA} ≤ 3.6V f_{ADC} = 75 MHz	-	-	6.82	
		Resolution = 6 bits –40 °C ≤ T_J ≤ 125 °C SMP = 2.5	All modes(3)	1.62 V ≤ V_{DDA} ≤ 3.6V f_{ADC} = 75 MHz	-	-	8.33	

Table 79. 12-bit ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
f_S	Sampling rate for slow channels	Resolution = 12 bits –40 °C ≤ T_J ≤ 125 °C SMP = 2.5	-	f_{ADC} = 35 MHz(4)	-	-	2.3	MSPS
		Resolution = 10 bits –40 °C ≤ T_J ≤ 125 °C SMP = 2.5			-	-	2.7	
		Resolution = 8 bits –40 °C ≤ T_J ≤ 125 °C SMP = 2.5		f_{ADC} = 50 MHz(4)	-	-	4.5	
		Resolution = 6 bits –40 °C ≤ T_J ≤ 125 °C SMP = 2.5			-	-	5.5	
t_{TRIG}	External trigger period	Resolution = 12 bits			-	-	15	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-			0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	Differential mode			V_{REF}/2− 10%	V_{REF}/2	V_{REF}/2+ 10%	
R_{AIN}(5)	External input impedance	Resolution = 12 bits, T_J = 125 °C			-	-	220	Ω
		Resolution = 10 bits, T_J = 125 °C			-	-	2100	
		Resolution = 8 bits, T_J = 125 °C			-	-	12000	
		Resolution = 6 bits, T_J = 125 °C			-	-	80000	
C_{ADC}	Internal sample and hold capacitor	-			-	3	-	pF
$t_{ADC_VREG_STUP}$	ADC LDO startup time	-			-	5	10	µs
t_{STAB}	ADC power-up time	LDO already started			1	-	-	con-version cycle

Table 79. 12-bit ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{OFF_CAL}	Offset calibration time	-		135		$1/f_{ADC}$
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	
		CKMODE = 01	-	-	2.5	
		CKMODE = 10	-	-	2.5	
		CKMODE = 11	-	-	2.25	
$t_{LATR\ INJ}$	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	2.5	3	3.5	
		CKMODE = 01	-	-	3.5	
		CKMODE = 10	-	-	3.5	
		CKMODE = 11	-	-	3.25	
t_S	Sampling time(6)	-	2.5	-	640.5	
t_{CONV}	Total conversion time (including sampling time)	N-bits resolution	t_S + 0.5 + N	-	-	
I_{DDA_D} (ADC)	ADC consumption on V_{DDA} and V_{REF}, Differential mode	f_S= 5 MSPS	-	540	-	µA
		f_S= 1 MSPS	-	190	-	
		f_S=0.1 MSPS	-	49	-	
I_{DDA_SE} (ADC)	ADC consumption on V_{DDA} and V_{REF}, Single-ended mode	f_S= 5 MSPS	-	416	-	
		f_S= 1 MSPS	-	153	-	
		f_S= 0.1 MSPS	-	46	-	
I_{DD} (ADC)	ADC consumption on V_{DD}	f_{ADC} = 75 MHz	-	180	-	µA
		f_{ADC} = 50 MHz	-	135	-	
		f_{ADC} = 25 MHz	-	90	-	
		f_{ADC} = 12.5 MHz	-	45	-	
		f_{ADC} = 6.25 MHz	-	22	-	
		f_{ADC} = 3.125 MHz	-	11	-	

1. Specified by design, not tested in production.

2. The voltage booster on ADC switches must be used for V_{DDA} < 2.4 V (embedded I/O switches).
3. The conversion of the first element in the group is excluded.
4. f_{ADC} value corresponds to the maximum frequency that can be reached considering a 2.5 sampling period. For other SMPy sampling periods, the maximum frequency is f_{ADC} value * SMPy / 2.5 with a limitation to 75 MHz.
5. The tolerance is 2 LSBs for 12-bit, 10-bit and 8-bit resolutions. It is otherwise specified.
6. The sampling time can vary depending on the condition with ±0.5 clock cycles. Resulting in minimum of 2.0 cycles and maximum of 641 cycles. Refer to the detailed description in the reference manual.

Table 80. Minimum sampling time vs R_{AIN} (12-bit ADC)(1)(2)

Resolution	RAIN (Ω)	Minimum sampling time (s)	
		Fast channels(3)	Slow channels(4)
12 bits	47	3.75E-08	6.12E-08
	68	3.94E-08	6.25E-08
	100	4.36E-08	6.51E-08
	150	5.11E-08	7.00E-08
	220	6.54E-08	7.86E-08
	330	8.80E-08	9.57E-08
	470	1.17E-07	1.23E-07
	680	1.60E-07	1.65E-07
10 bits	47	3.19E-08	5.17E-08
	68	3.35E-08	5.28E-08
	100	3.66E-08	5.45E-08
	150	4.35E-08	5.83E-08
	220	5.43E-08	6.50E-08
	330	7.18E-08	7.89E-08
	470	9.46E-08	1.00E-07
	680	1.28E-07	1.33E-07
	1000	1.81E-07	1.83E-07
	1500	2.63E-07	2.63E-07
	2200	3.79E-07	3.76E-07
	3300	5.57E-07	5.52E-07
8 bits	47	2.64E-08	4.17E-08
	68	2.76E-08	4.24E-08
	100	3.02E-08	4.39E-08
	150	3.51E-08	4.66E-08
	220	4.27E-08	5.13E-08
	330	5.52E-08	6.19E-08
	470	7.17E-08	7.72E-08
	680	9.68E-08	1.00E-07
	1000	1.34E-07	1.37E-07
	1500	1.93E-07	1.94E-07
	2200	2.76E-07	2.74E-07
	3300	4.06E-07	4.01E-07
	4700	5.73E-07	5.62E-07

Table 80. Minimum sampling time vs R_{AIN} (12-bit ADC)(1)(2) (continued)

Resolution	RAIN (Ω)	Minimum sampling time (s)	
		Fast channels(3)	Slow channels(4)
8 bits (continued)	6800	8.21E-07	7.99E-07
	10000	1.20E-06	1.17E-06
	15000	1.79E-06	1.74E-06
6 bits	47	2.14E-08	3.16E-08
	68	2.23E-08	3.21E-08
	100	2.40E-08	3.31E-08
	150	2.68E-08	3.52E-08
	220	3.13E-08	3.87E-08
	330	3.89E-08	4.51E-08
	470	4.88E-08	5.39E-08
	680	6.38E-08	6.79E-08
	1000	8.70E-08	8.97E-08
	1500	1.23E-07	1.24E-07
	2200	1.73E-07	1.73E-07
	3300	2.53E-07	2.49E-07
	4700	3.53E-07	3.45E-07
	6800	5.04E-07	4.90E-07
	10000	7.34E-07	7.11E-07
	15000	1.09E-06	1.05E-06

1. Specified by design, not tested in production.
2. Data valid up to 130 °C, with a 22 pF PCB capacitor and V_{DDA} = 1.62 V.
3. Fast channels correspond to ADCx_INx[0:5].
4. Slow channels correspond to all ADC inputs except for the Fast channels.

Table 81. 12-bit ADC accuracy(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Fast and slow channel	Single ended	-	±3.5	±12	±LSB
			Differential	-	±2.5	±5	
EO	Offset error	Single ended		-	±3	±5.5	
		Differential		-	±2	±3.5	
EG	Gain error	Single ended		-	±3.5	±11	
		Differential		-	±2.5	±5	
ED	Differential linearity error	Single ended		-	±0.75	+1.5/-1	
		Differential		-	±0.75	+2.5/-1	
EL	Integral linearity error	Fast and slow channel	Single ended	-	±2	±4.5	
			Differential	-	±1	±2	
ENOB	Effective number of bits	Single ended		-	10.8	-	bits
		Differential		-	11.5	-	
SINAD	Signal-to-noise and distortion ratio	Single ended		-	68	-	dB
		Differential		-	71	-	
SNR	Signal-to-noise ratio	Single ended		-	70	-	
		Differential		-	72	-	
THD	Total harmonic distortion	Single ended		-	-70	-	
		Differential		-	-80	-	

1. Evaluated by characterization, not tested in production.
2. ADC DC accuracy values are measured after internal calibration in Continuous mode.

Figure 36. ADC accuracy characteristics

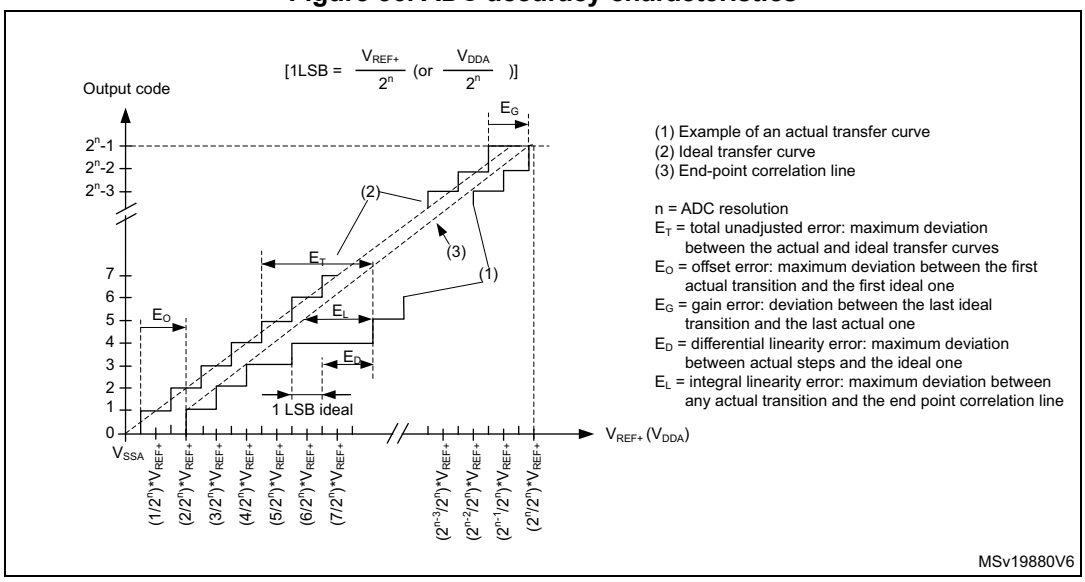
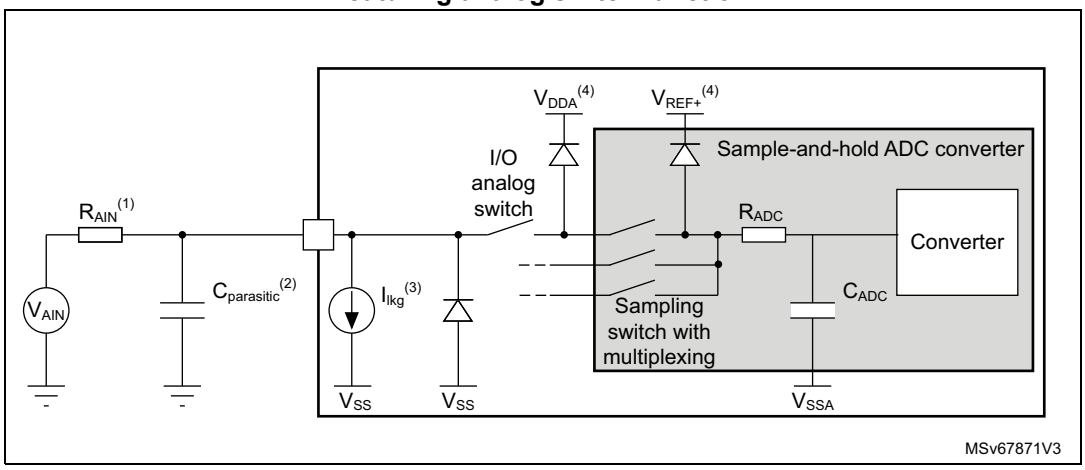


Figure 37. Typical connection diagram using the ADC with FT/TT pins featuring analog switch function



1. Refer to *Table 79* and *Table 80* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 54: I/O static characteristics*). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 54: I/O static characteristics* for value of I_{leak}.
4. Refer to *Figure 10: Power supply scheme*.

6.3.23 Voltage reference buffer characteristics

Table 82. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VSCALE = 000	2.8	3.3	3.6	V
			VSCALE = 001	2.4	-	3.6	
			VSCALE = 010	2.1	-	3.6	
			VSCALE = 011	1.95	-	3.6	
		Degraded mode(2)	VSCALE = 000	1.62	-	2.80	
			VSCALE = 001	1.62	-	2.40	
			VSCALE = 010	1.62	-	2.10	
			VSCALE = 011	1.62	-	1.95	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode @30 °C @I_{load} = 10 uA V_{DDA} = 3.3 V	VSCALE = 000	2.497	2.5	2.503	
			VSCALE = 001	2.045	2.048	2.051	
			VSCALE = 010	1.798	1.8	1.802	
			VSCALE = 011	1.648	1.65	1.652	
		Degraded mode(2)	VSCALE = 000	Min (V_{DDA}- 0.22, 2.498)	-	2.502	
			VSCALE = 001	Min (V_{DDA}- 0.22, 2.047)	-	2.051	
			VSCALE = 010	Min (V_{DDA}- 0.22, 1.800)	-	1.807	
			VSCALE = 011	Min (V_{DDA}- 0.22, 1.65)	-	1.657	
TRIM	Trim step resolution	-	-	-	±0.05	-	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal Mode	-	50	-	ppm/ mA

Table 82. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{coeff}	Temperature coefficient	-40 °C < T_J < +125 °C	-	-	$T_{coeff_VREF_INT}$ +75	-	ppm/°C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100 kHz	-	-	40	-	
t_{START}	Start-up time(3)	C_L = 0.5 µF	-	-	300	350	µs
		C_L = 1 µF	-	-	500	650	
		C_L = 1.5 µF	-	-	650	800	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(4)	-		-	8	13.5	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	16	µA
		I_{LOAD} = 500 µA	-	-	16	21	
		I_{LOAD} = 4 mA	-	-	32	41	
$R_{VREFBUF_PullDown}$	Pull-down resistor when ENVR = HIZ = 0	-		-	100	-	Ω

1. Specified by design, not tested in production.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}-drop voltage).
3. if VREF+ pin has residual voltage when VREFBUF is enabled (VREFBUF_CSR.ENVR=1), this might create an overshoot on VREFBUF output longer than t_{START}.
   To avoid this, it is necessary that VREF+ pin is correctly discharged before being enabled (below VREFBUF_OUT minus 1 V, for example below 1.5 V for VSCALE = 000)
   This could be achieved by ensuring VREFBUF is in OFF mode (VREFBUF_CSR.ENVR=0 and VREFBUF_CSR.HIZ=0) for sufficient time to discharge C_L through VREFBUF pull-down.
4. To properly control VREFBUF I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 1.95 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VSCALE = 011, 010, 001 and 000, respectively.

6.3.24 Temperature sensor characteristics

Table 83. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	VSENSE linearity with temperature (from Vsensor voltage)	-	-	±3	°C
	VSENSE linearity with temperature (from ADC counter)	-	-	±3	
Avg_Slope(2)	Average slope (from Vsensor voltage)	-	2	-	mV/°C
	Average slope (from ADC counter)	-	2	-	
V_{30}(3)	Voltage at 30 °C ± 5 °C	-	0.62	-	V
t_{start_run}(1)	Startup time in Run mode (buffer startup)	5.3	-	40.5	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9.8	-	-	

Table 83. Temperature sensor characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
I_{sens}(1)	Sensor consumption	0.11	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	2.3	3.8	6.1	

1. Specified by design, not tested in production.
2. Evaluated by characterization, not tested in production.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

Table 84. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ±5 °C V_{DDA} = V_{REF+} = 3.3 V ±10 mV	0x5C00 525C[15:0](1)(2)
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C ±2 °C V_{DDA} = V_{REF+} = 3.3 V ±10 mV	0x5C00 525C[31:16](1)(2)

1. It is mandatory to read a 32-bit word and to do relevant masking and shifting to isolate the required bits.
2. This address is located inside the BSEC and the access is allowed after being enabled in the RCC.

6.3.25 DTS characteristics

Table 85. DTS characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}	Output Clock frequency (PTAT clock)	-	-	500	-	kHz
T_{SLOPE}	Average slope	-	-	1600	-	Hz/°C
T_L	Linearity with temperature (from Output clock frequency).	V_{DDCORE} = 1.25 V	-	-	±3.8	°C
T_{TOTAL_ERROR}	Temperature measurement error	Temperature: -40 to 125 °C	-5	-	+5	°C
$T_{VDD\ CORE}$	Additional error due to V_{DDCORE} variation	-	-	10	-	°C/V
t_{TRIM}	Calibration time	-	2	-	-	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready signal = 1	-	-	50	-	µs
I_{DDCORE_DTS}	DTS consumption on V_{DDCORE}	-	-	20	-	µA

1. Specified by design, not tested in production.

6.3.26 V_{BAT} ADC monitoring characteristics and charging characteristics

Table 86. V_{BAT} ADC monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	4×26	-	kΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(2)	Error on Q	–10	-	+10	%
t_{S_vbat}(2)	ADC sampling time when reading V_{BAT} input	9.8	-	-	µs

1. 1.20 V ≤ V_{BAT} ≤ 3.6 V
2. Specified by design, not tested in production.

Table 87. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	kΩ
		VBRS in PWR_CR3= 1	-	1.5	-	

6.3.27 Temperature and Backup domain supply thresholds monitoring

The temperature and Backup domain supply monitoring characteristics are provided in the technical note STM32MP13xC/F MPUs for PCI products (TN1358). A NDA is required.

6.3.28 V_{DDCORE}, V_{DDCPU}, V_{DDQ_DDR} monitoring characteristics

Table 88. V_{DDCORE}, V_{DDCPU}, V_{DDQ_DDR} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$t_{S_vddcore}$(1)	ADC sampling time when reading V_{DDCORE} input	1	-	-	µs
t_{S_vddcpu}(1)	ADC sampling time when reading V_{DDCPU} input	1	-	-	µs
$t_{S_vddq_ddr}$(1)	ADC sampling time when reading V_{DDQ_DDR} input	1	-	-	µs

1. Specified by design, not tested in production.

6.3.29 Voltage booster for analog switch

Table 89. Voltage booster for analog switch characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.71	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.71 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

6.3.30 Compensation cell

Table 90. Compensation cell characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{COMPCELL}$	V_{DD} current consumption during code calculation	1.71 V ≤ V_{DD} ≤ 2.7 V	-	-	3.5	mA
		2.7 V < V_{DD} < 3.6 V	-	-	10	
T_{READY}	Time needed for code calculation	1.71 V ≤ V_{DD} ≤ 2.7 V	-	-	300	µs
		2.7 V < V_{DD} < 3.6 V	-	-	250	

6.3.31 Digital filter for sigma-delta modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 91* for DFSDM are derived from tests performed under the ambient temperature, f_{pclkx} frequency and V_{DD} supply voltage summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5×V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDMx_CKINx, DFSDMx_DATINx, DFSDMx_CKOUT for DFSDMx).

Table 91. DFSDM measured timing

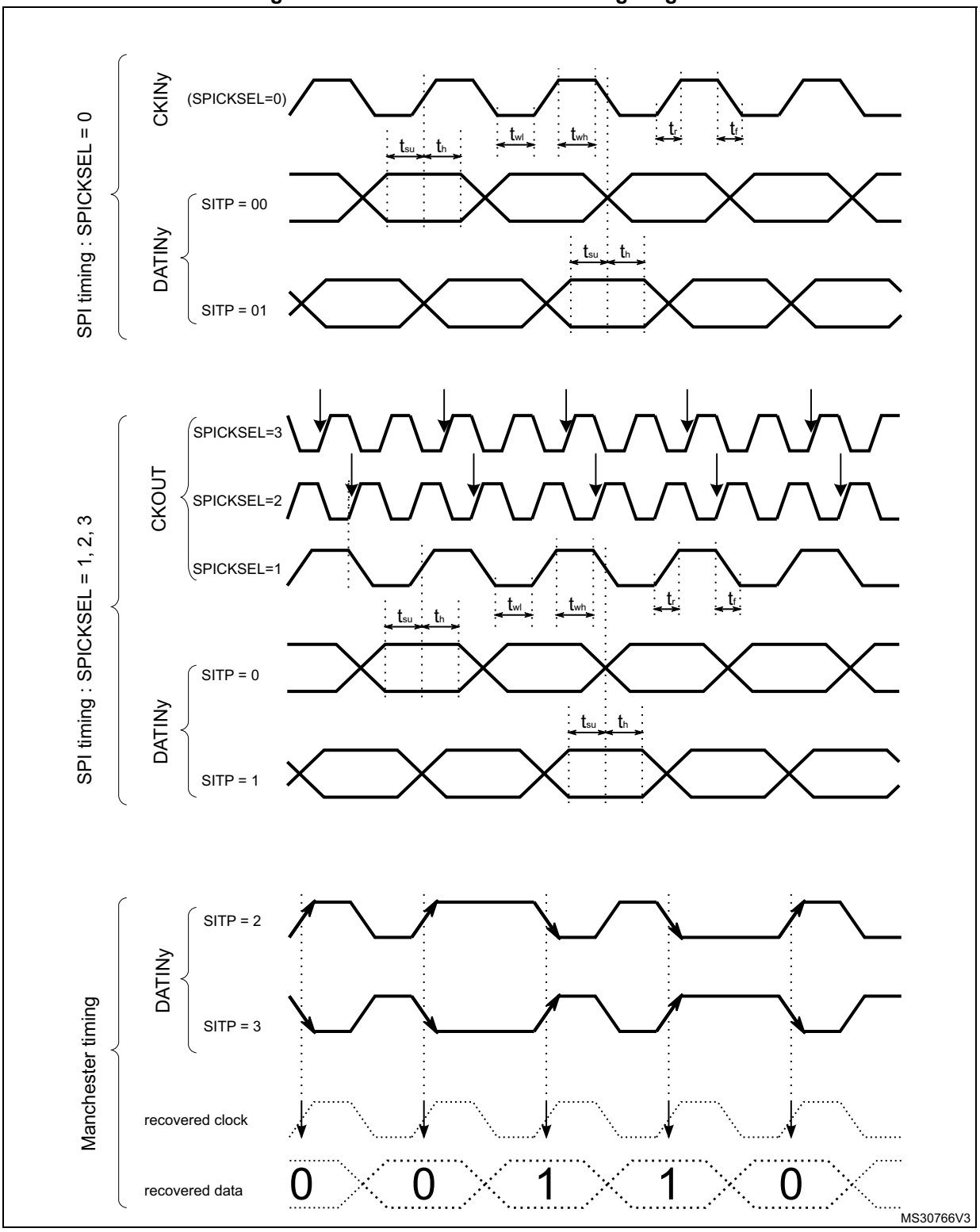
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.71 V < V_{DD} < 3.6 V	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 V < V_{DD} < 3.6 V	-	-	33	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < V_{DD} < 3.6 V	-	-	33	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V_{DD} < 3.6 V	-	-	33	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 2.7 < V_{DD} < 3.6 V	-	-	33	
f_{CKOUT}	Output clock frequency	1.71 < V_{DD} < 3.6 V	-	-	33	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.71 < V_{DD} < 3.6 V	45	50	55	%

Table 91. DFSDM measured timing (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	$T_{CKIN}/2$ - 0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	1	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	1	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V_{DD} < 3.6 V	(CKOUTDIV+1) ×$T_{DFSDMCLK}$(1)	-	(2×CKOUTDIV) × $T_{DFSDMCLK}$(1)	

1. See DFSDM section in Reference manual for definition of CKOUTDIV.

Figure 38. Channel transceiver timing diagrams



6.3.32 Timer characteristics

The parameters given in *Table 92* are specified by design, not tested in production.

Refer to *Section 6.3.17: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 92. TIMx characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{TIMxCLK}$	Timer kernel clock	0	209	MHz
f_{EXT}	Timer external clock frequency on CH1 to CH4	0	$f_{TIMxCLK}/2$	
Res_{TIM}	Timer resolution	-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 16-bit counters	-	65536	$t_{TIMxCLK}$
	Maximum possible count with 32-bit counter (TIM2, TIM5)		65536 × 65536	

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Specified by design, not tested in production.

Table 93. LPTIMx characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	104.5	MHz
f_{EXT}	Timer external clock frequency on Input1 and Input2	0	$f_{LPTIMxCLK}/2$	
Res_{TIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{TIMxCLK}$

1. LPTIMx is used as a general term to refer to the LPTIM1 to LPTIM5 timers.
2. Specified by design, not tested in production.

6.3.33 Communications interfaces

I2C interface characteristics

The I2C interface meets the timings requirements of the I^2C-bus specification for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are specified by design, not tested in production, when the I2C peripheral is properly configured and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{load} supported in Fm+, which is given by these formulas:

$t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$

$R_{p(min)} = (V_{DD}-V_{OL(max)})/I_{OL(max)}$

Where R_p is the I2C lines pull-up. Refer to *Section 6.3.17: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to *Table 94* for the analog filter characteristics:

Table 94. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	120(3)	ns

1. Specified by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
   At -40 °C it is possible to have 40 ns instead of 50 ns as minimum pulse width.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

The I2C pins can be set in FM+ mode in SYSCFG_PMCR register.

Unless otherwise specified, the parameters given in *Table 95* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 95. I2C FM+ pin characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
F_{max}(1)	Maximum frequency	C = 50 pF $1.71 \le V_{DD} \le 3.6$ V	-	1	MHz
T_f(2)	Output high to low level fall time		-	5	ns

1. The maximum frequency is defined with the following conditions:
   - (Tr + Tf) ≤ ⅔T
   - 45% < duty cycle < 55%.
2. The fall time is defined between 70% and 30% of the output waveform accordingl to I^2C specification NXP UM10204 rev- Oct 2012.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 96* for the SPI interface are derived from tests performed under the ambient temperature, f_{pclkx} frequency and V_{DD}

supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 96. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V SPI1,2,3,4	-	-	100	MHz
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V SPI5			52	
		Slave receiver mode 1.71 V ≤ V_{DD} ≤ 3.6 V SPI1,2,3,4			100	
		Slave receiver mode 1.71 V ≤ V_{DD} ≤ 3.6 V SPI5			52	
		Slave mode transmitter/full duplex 2.7 V ≤ V_{DD} ≤ 3.6 V			38(2)	
		Slave mode transmitter/full duplex 1.71 V ≤ V_{DD} ≤ 3.6 V			35(2)	
$t_{su(NSS)}$	NSS setup time	Slave mode	2	-	-	ns
$t_{h(NSS)}$	NSS hold time		2	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{pclk} - 1	T_{pclk}	T_{pclk} + 1	

Table 96. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MI)}$	Data input setup time	Master mode	4	-	-	ns
$t_{su(SI)}$		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	1.5	-	-	
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	8.5	10	16	
$t_{dis(SO)}$	Data output disable time	Slave mode	4.5	5	7.5	
$t_{v(SO)}$	Data output valid time	Slave mode $2.7\ V \le V_{DD} \le 3.6\ V$	-	10	13	
		Slave mode $1.71\ V \le V_{DD} \le 3.6\ V$	-	11	14	
$t_{v(MO)}$		Master mode	-	1.5	2	
$t_{h(SO)}$	Data output hold time	Slave mode $1.71\ V \le V_{DD} \le 3.6\ V$	8	-	-	
$t_{h(MO)}$		Master mode	1	-	-	

1. Evaluated by characterization, not tested in production.
2. Maximum frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a manager having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%.

Figure 39. SPI timing diagram - slave mode and CPHA = 0

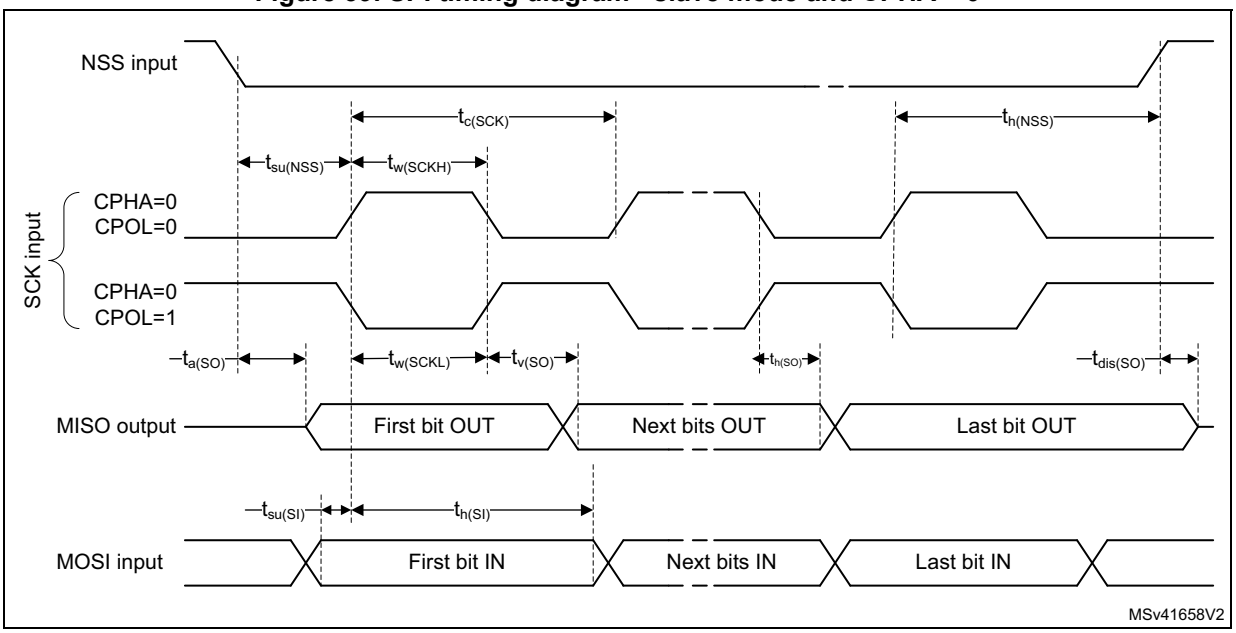
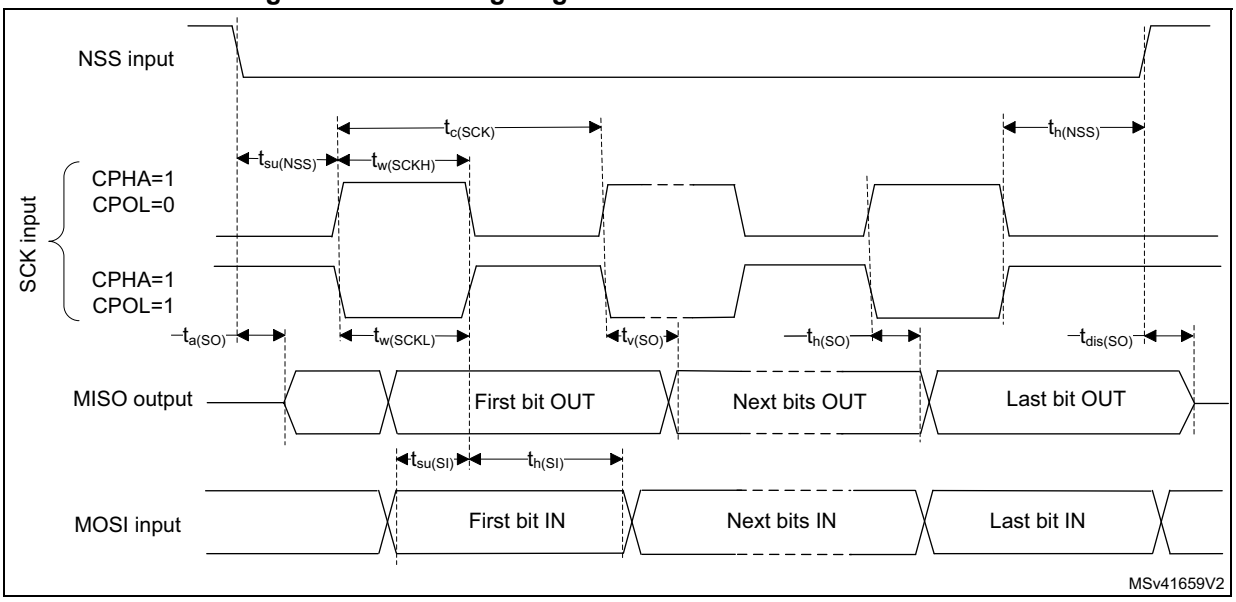
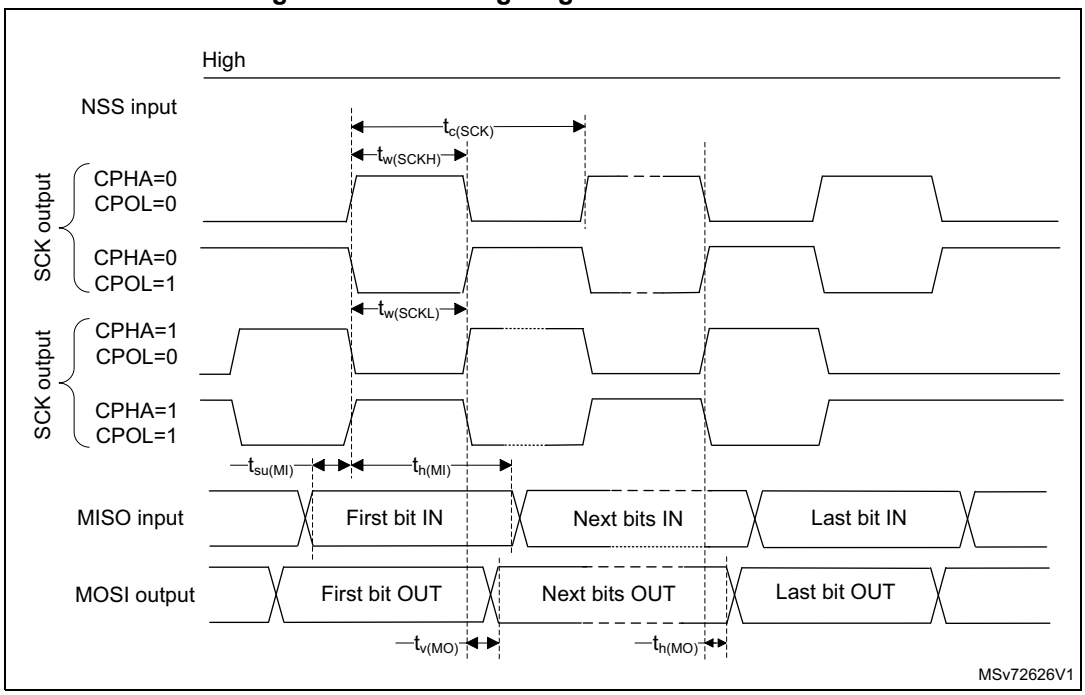


Figure 40. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at 0.5×V_{DD} and with external C_L = 30 pF.

Figure 41. SPI timing diagram - master mode(1)



1. Measurement points are done at 0.5×V_{DD} and with external C_L = 30 pF.

I2S interface characteristics

Unless otherwise specified, the parameters given in *Table 97* for the I2S interface are derived from tests performed under the ambient temperature, f_{pclkx} frequency and V_{DD}

supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled
- HSLV activated when $V_{DD} \leq 2.7$ V

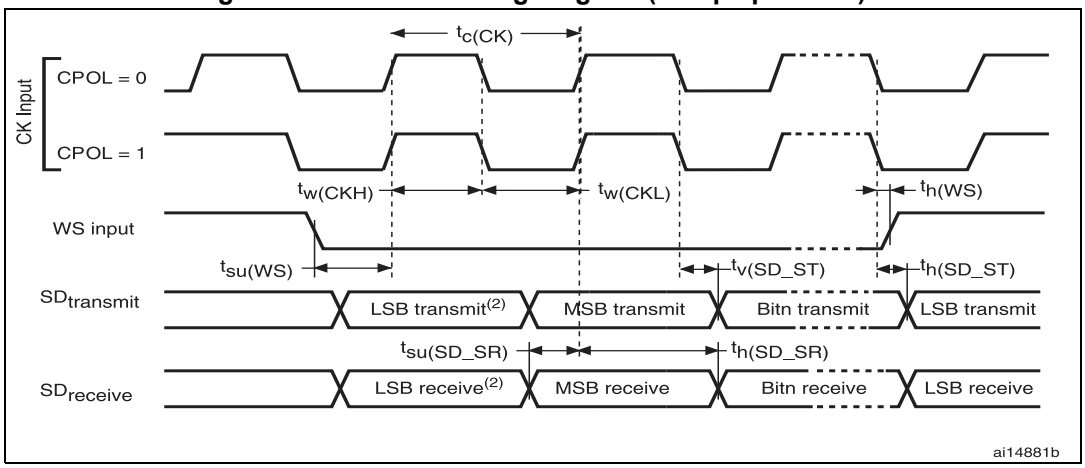
Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 97. I2S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	-	256×8K	256×Fs	MHz
f_{CK}	I2S clock frequency	Master data	-	64×Fs	MHz
		Slave data	-	64×Fs	
$t_{v(WS)}$	WS valid time	Master mode	-	2	ns
$t_{h(WS)}$	WS hold time	Master mode	1	-	
$t_{su(WS)}$	WS setup time	Slave mode	3.5	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	3.5	-	
$t_{su(SD_SR)}$		Slave receiver	2	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	1	-	
$t_{h(SD_SR)}$		Slave receiver	1	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	10	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	1	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	1	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0.5	-	

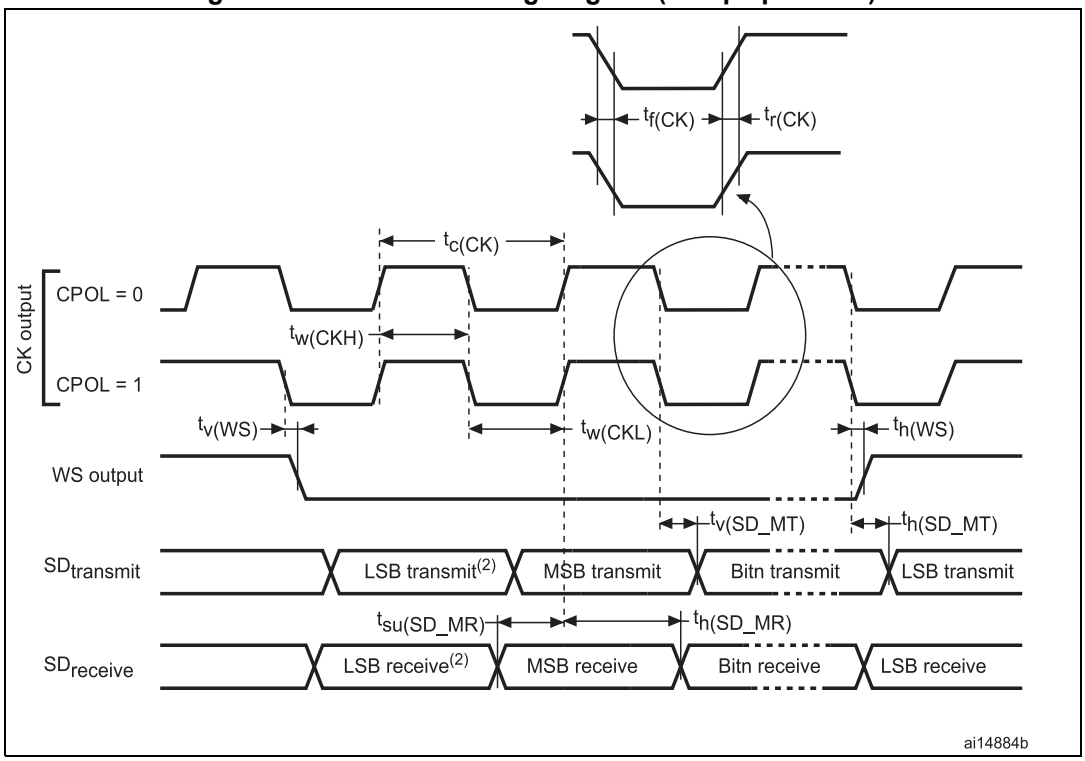
1. Evaluated by characterization, not tested in production.

Figure 42. I2S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 43. I2S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 98* for SAI are derived from tests performed under the ambient temperature, F_{pclk2} frequency and V_{DD} supply voltage

conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are performed at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 98. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	-	50	MHz
F_{CK}	SAI bit clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V	-	45	MHz
		Master transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V	-	27	
		Master receiver 1.71 V ≤ V_{DD} ≤ 3.6 V	-	27	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V	-	43	
		Slave transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V	-	30	
		Slave receiver 1.71 ≤ V_{DD} ≤ 3.6 V	-	50	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	11	ns
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V	-	18	
$t_{su(FS)}$	FS setup time	Slave mode	6.5	-	
$t_{h(FS)}$	FS hold time	Master mode	2	-	
		Slave mode	2	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	3.5	-	
$t_{su(SD_B_SR)}$		Slave receiver	2	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	1	-	
$t_{h(SD_B_SR)}$		Slave receiver	0.5	-	

Table 98. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	11.5	ns
		Slave transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	16.5	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
		Master transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	18	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	6.5	-	

1. Evaluated by characterization, not tested in production.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 44. SAI master timing waveforms

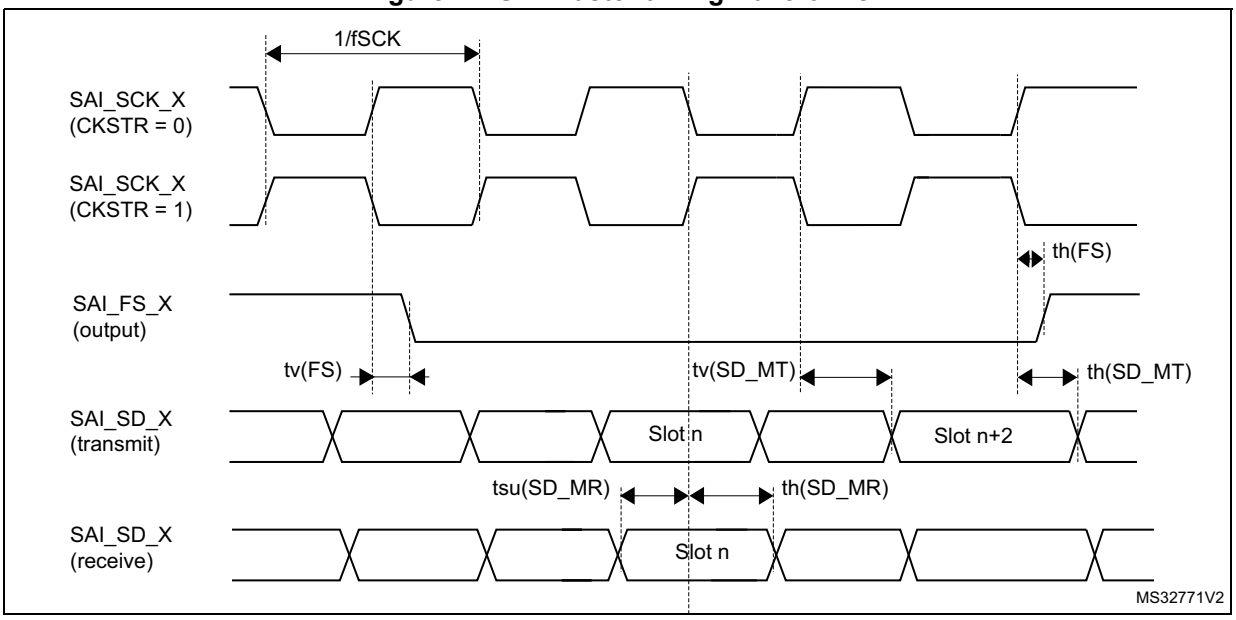
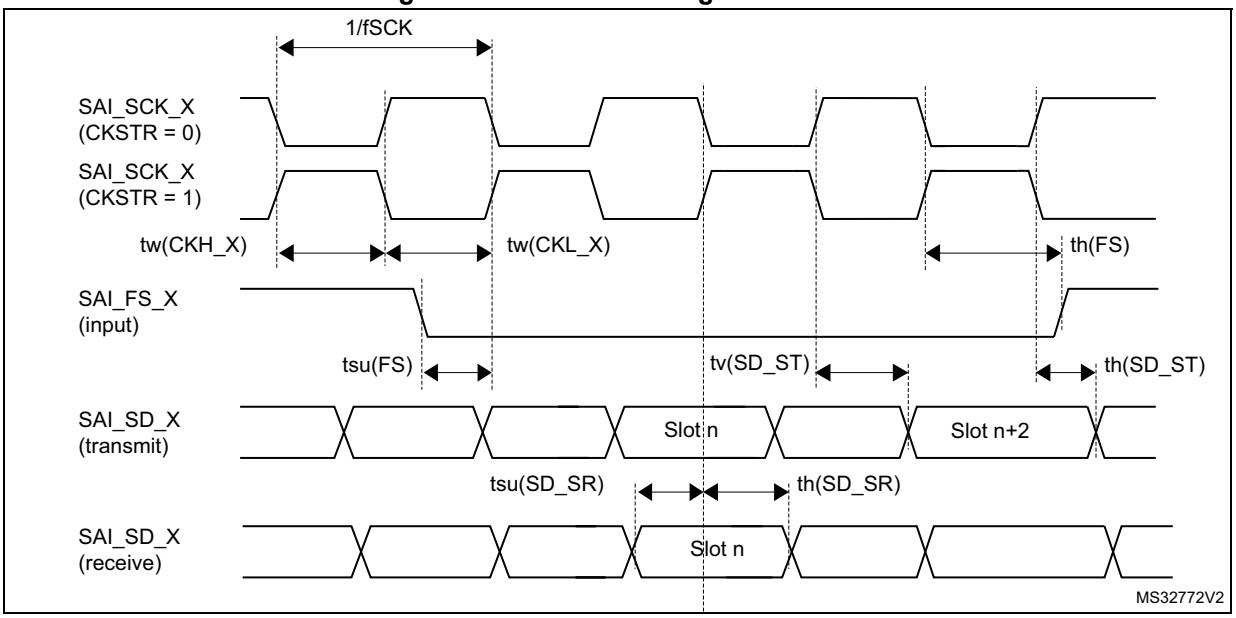


Figure 45. SAI slave timing waveforms



SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 99* for the SDIO/MMC interface are derived from tests performed under the ambient temperature, F_{hclk6} frequency and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled
- HSLV activated when $V_{DD} \leq 2.7$ V
- Delay block disabled

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 99. Dynamics characteristics: SD characteristics, V_{DD} = 1.71 V to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$2.7 < V_{DD} < 3.6$ V	-	-	130	MHz
		$1.71 < V_{DD} < 1.9$ V	-	-	105	
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} =52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} =52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in SD HS/SDR/DDR mode						

Table 99. Dynamics characteristics: SD characteristics, V_{DD} = 1.71 V to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IHD}	Input hold time HS	-	0.5	-	-	
T_{idw}(3)	Input valid window (variable window)	-	2.5	-	-	
CMD, D outputs (referenced to CK) in SD HS/SDR/DDR mode						
t_{OV}	Output valid time HS	-	-	5	6	ns
t_{OH}	Output hold time HS	-	4.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	2.5	-	-	ns
t_{IHD}	Input hold time SD	-	0.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	0.5	1	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. Data based on characterization results, not tested in production.
2. Above 100 MHz, CL applied is 20 pF.
3. The minimum window of time where the data need to be stable for proper sampling in tuning mode.

Table 100. Dynamics characteristics: *e*•MMC characteristics V_{DD} = 1.71 V to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	2.7 < V_{DD} < 3.6 V	-	-	130	MHz
		1.71 < V_{DD} < 1.9 V	-	-	105	
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} =52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} =52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in *e*•MMC mode						
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IH}	Input hold time HS	-	0.5	-	-	
T_{idw}(3)	Input valid window (variable window)	-	2.5	-	-	
CMD, D outputs (referenced to CK) in *e*•MMC mode						
t_{OV}	Output valid time HS	-	-	5	6	ns
t_{OH}	Output hold time HS	-	4	-	-	

1. ata based on characterization results, not tested in production.
2. C_{LOAD} = 20 pF.
3. The minimum window of time where the data need to be stable for proper sampling in tuning mode.

Figure 46. SD high-speed mode

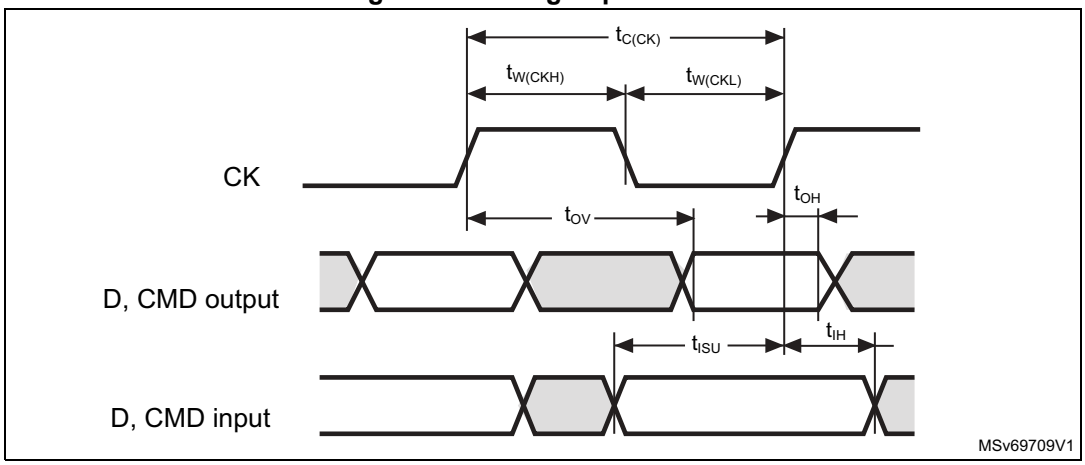


Figure 47. SD default mode

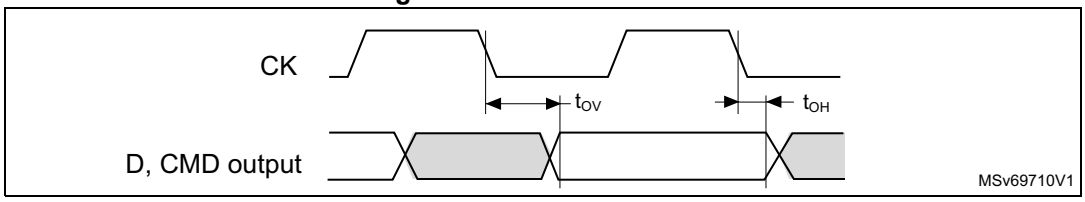
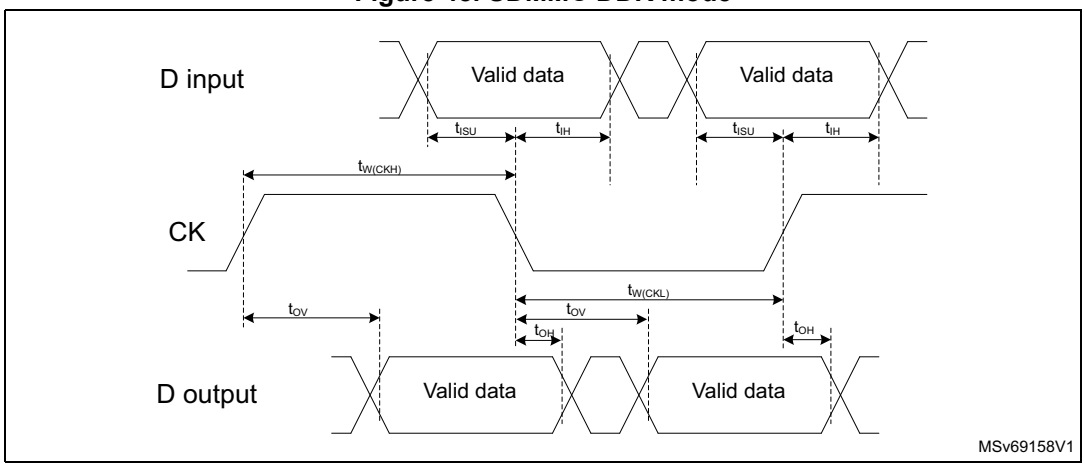


Figure 48. SDMMC DDR mode



Ethernet (ETH) characteristics

Unless otherwise specified, the parameters given in *Table 101*, *Table 102*, *Table 103* and *Table 104* for MDIO/SMA, RMII, RGMII and MII are derived from tests performed under the ambient temperature, F_{axiss_ck} frequency summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$.
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 101 gives the list of Ethernet MAC timings for the MDIO/SMA and *Figure 49* shows the corresponding timing diagram.

Table 101. Dynamics characteristics: Ethernet MAC timings for MDIO/SMA(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	399	400	401	ns
$T_{d(MDIO)}$	Write data valid time	0.5	1	3.5	
$t_{su(MDIO)}$	Read data setup time	17.5	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Evaluated by characterization, not tested in production.

Figure 49. Ethernet MDIO/SMA timing diagram

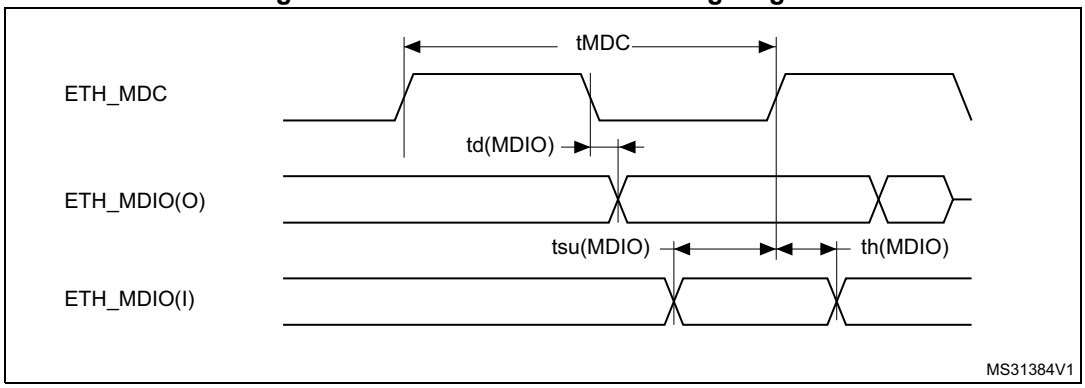


Table 102 gives the list of Ethernet MAC timings for the RMII and *Figure 50* shows the corresponding timing diagram.

Table 102. Dynamics characteristics: Ethernet MAC timings for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1.5	-	-	
$t_{su(CRS)}$	Carrier sense setup time	1.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	1.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	5.5	8.5	10.5	
$t_{d(TXD)}$	Transmit data valid delay time	6	8.5	11	

1. Evaluated by characterization, not tested in production.

Figure 50. Ethernet RMII timing diagram

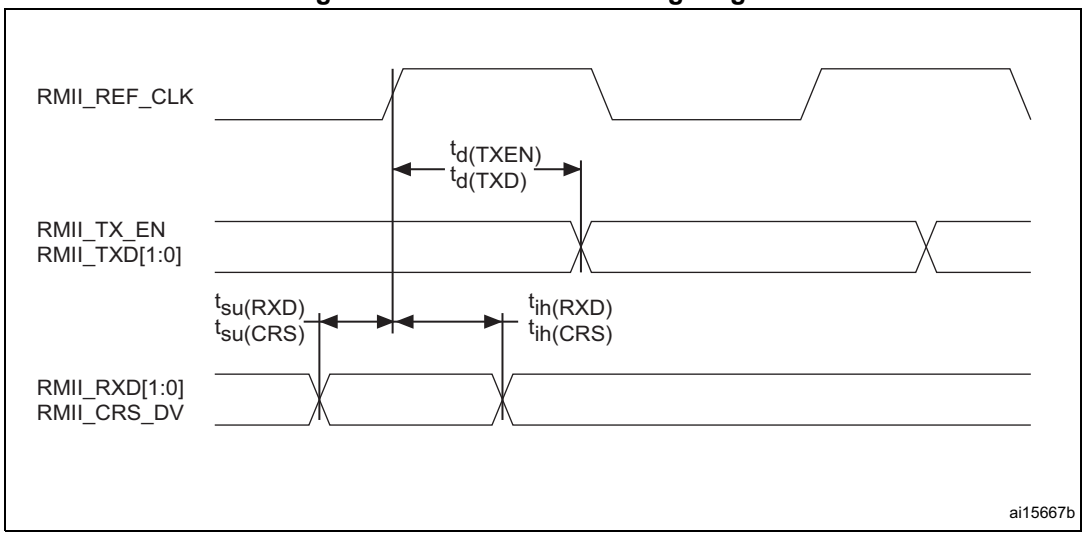


Table 103 gives the list of Ethernet MAC timings for MII and *Figure 51* shows the corresponding timing diagram.

Table 103. Dynamics characteristics: Ethernet MAC timings for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1.5	-	-	
$t_{su(DV)}$	Data valid setup time	1	-	-	
$t_{ih(DV)}$	Data valid hold time	1.5	-	-	
$t_{su(ER)}$	Error setup time	1.5	-	-	
$t_{ih(ER)}$	Error hold time	1	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	7	9	12	
$t_{d(TXD)}$	Transmit data valid delay time	7	9	12	

1. Evaluated by characterization, not tested in production.

Figure 51. Ethernet MII timing diagram

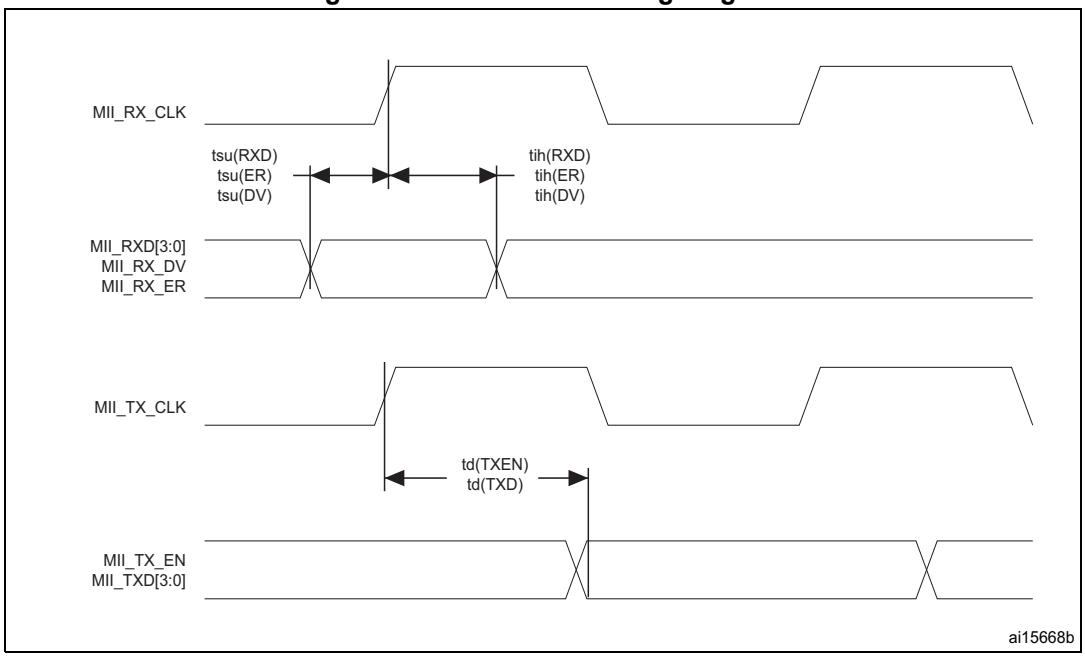
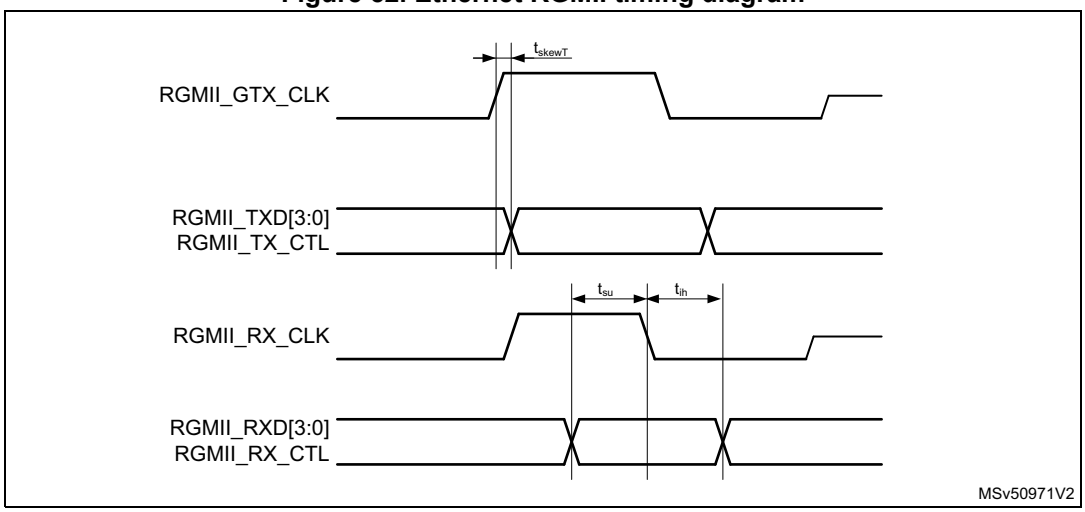


Table 104. Dynamics characteristics: Ethernet MAC signals for RGMII (1)

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1.5	-	-	
$t_{su(RX_CTL)}$	Receive control valid setup time	1	-	-	
$t_{ih(RX_CTL)}$	Receive control valid hold time	1.5	-	-	
$T_{skewT(TX_CTL)}$	Transmit control valid delay time	-0.25	0.25	0.5	
$T_{skewT(TXD)}$	Transmit data valid delay time	-0.25	0.25	0.5	

1. Evaluated by characterization, not tested in production.

Figure 52. Ethernet RGMII timing diagram



6.3.34 USART (SPI mode) interface characteristics

Unless otherwise specified, the parameters given in *Table 105* for USART are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 105*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 105. USART (SPI mode) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	SPI master mode	-	-	13	MHz
		SPI slave mode	-	-	27	
$t_{su(NSS)}$	NSS setup time	SPI slave mode	t_{ker}+2	-	-	ns
$t_{h(NSS)}$	NSS hold time	SPI slave mode	2	-	-	ns
$t_{w(CKH)}$, $t_{w(CKL)}$	CK high and low time	SPI master mode	$1/f_{CK}/2 - 1$	1/fck/2	$1/f_{CK}/2 + 1$	ns
$t_{su(RX)}$	Data input setup time	SPI master mode	16	-	-	ns
		SPI slave mode	2.5	-	-	
$t_{hRX)}$	Data input hold time	SPI master mode	0.5	-	-	ns
		SPI slave mode	1	-	-	
$t_{v(TX)}$	Data output valid time	SPI slave mode	-	10	18	ns
		SPI master mode	-	1.5	2.5	
th(TX)	Data output hold time	SPI slave mode	8	-	-	ns
		SPI master mode	0	-	-	

1. 1.Evaluated by characterization, not tested in production.

Figure 53. USART timing diagram in SPI master mode

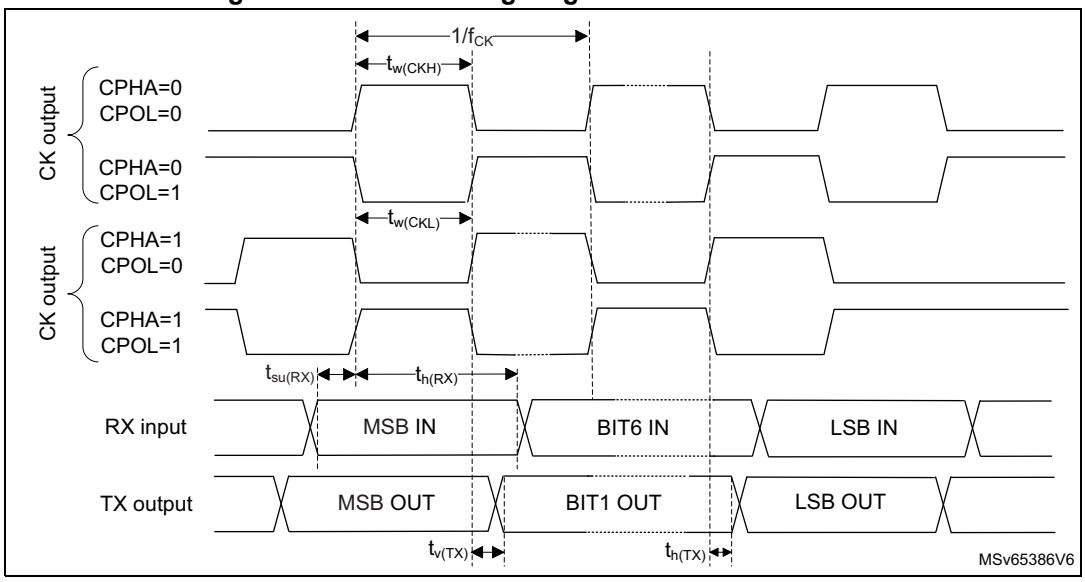
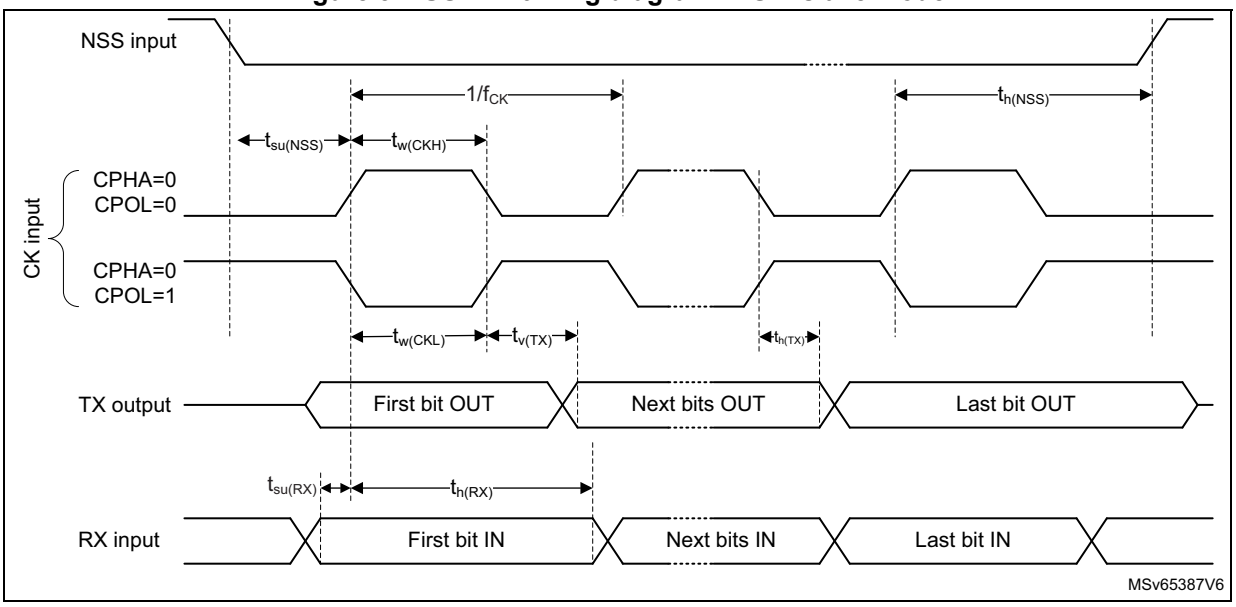


Figure 54. USART timing diagram in SPI slave mode



6.3.35 USB High-Speed PHY characteristics

Table 106. USB High-Speed PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{REF}	Reference resistor on USB_RREF pin	-	2.97	3.00	3.03	kΩ

Table 106. USB High-Speed PHY characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA1V1_REG(PHY)}$	High-Speed TX(2)	One USB port	-	1.4	-	mA
		Two USB ports	-	2.4	-	
	High-Speed RX(3) / Idle	One USB port	-	5.4	-	
		Two USB ports	-	10.4	-	
	Ful-Speed and Low-Speed mode (Suspend, TX or RX)		-	0	-	
$I_{DDA1V8_REG(PHY)}$	High-Speed TX(2)	One USB port	-	25.5	-	mA
		Two USB ports	-	50.5	-	
	High-Speed RX(3) / Idle	One USB port	-	2.5	-	
		Two USB ports	-	5.5	-	
	Ful-Speed and Low-Speed mode (Suspend, TX or RX)		-	0	-	
$I_{DDA3V3_USBHS(PHY)}$	High-Speed TX(2)	One USB port	-	5	-	mA
		Two USB ports	-	7	-	
	High-Speed RX(3) / Idle	One USB port	-	6	-	
		Two USB ports	-	10	-	
	Full-Speed Suspend (host mode)	One USB port	-	0	-	
		Two USB ports	-	0	-	
	Full-Speed Suspend (peripheral mode)	One USB port	-	0.2	-	
		Two USB ports	-	0.4	-	
	Full-Speed TX(2)	One USB port	-	6.5	-	
		Two USB ports	-	10.5	-	
	Full-Speed RX(3)	One USB port	-	6.5	-	
		Two USB ports	-	11.5	-	
	Low-Speed TX(2)	One USB port	-	7	-	
		Two USB ports	-	11.5	-	
	Low-Speed RX(3)	One USB port	-	4.3	-	
		Two USB ports	-	6.1	-	
t_{INIT}	Initialization time(4)	-	-	-	200	µs

1. Specified by design, not tested in production unless otherwise specified.
2. USB link 100% of the time in transmission
3. USB link 100% of the time in reception
4. This time includes the PLL_USB t_{LOCK}.

6.3.36 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 107* and *Table 108* for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$

frequency and V_{DD} supply voltage summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 107. Dynamics characteristics: JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	T_{CK} clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	35	MHz
$1/t_{c(TCK)}$		1.71 V < V_{DD} < 3.6 V	-	-	27	
$ti_{su(TMS)}$	TMS input setup time	-	2.5	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	2	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	1	-	-	
$t_{ov\ (TDO)}$	TDO output valid time	2.7 V < V_{DD} < 3.6 V	-	9.5	14	
		1.71 V < V_{DD}< 3.6 V	-	9.5	18	
$t_{oh(TDO)}$	TDO output hold time	-	8	-	-	

Table 108. Dynamics characteristics: SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	71	MHz
$1/t_{c(SWCLK)}$		1.71 V < V_{DD} < 3.6 V	-	-	55	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time	-	1	-	-	
$t_{ov\ (SWDIO)}$	SWDIO output valid time	2.7 V < V_{DD} < 3.6 V	-	10.5	14	
		1.71 V < V_{DD} < 3.6 V	-	10.5	18	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	9	-	-	

Figure 55. JTAG timing diagram

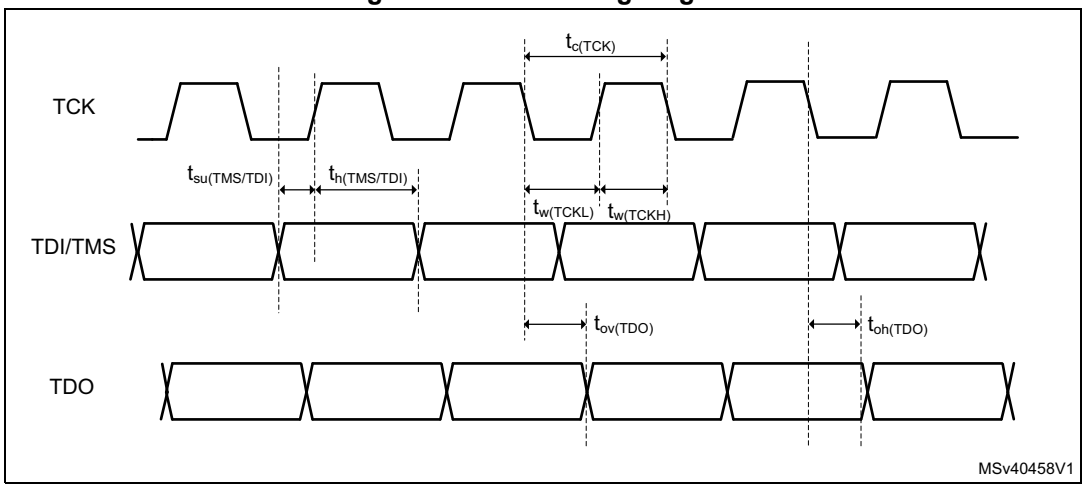
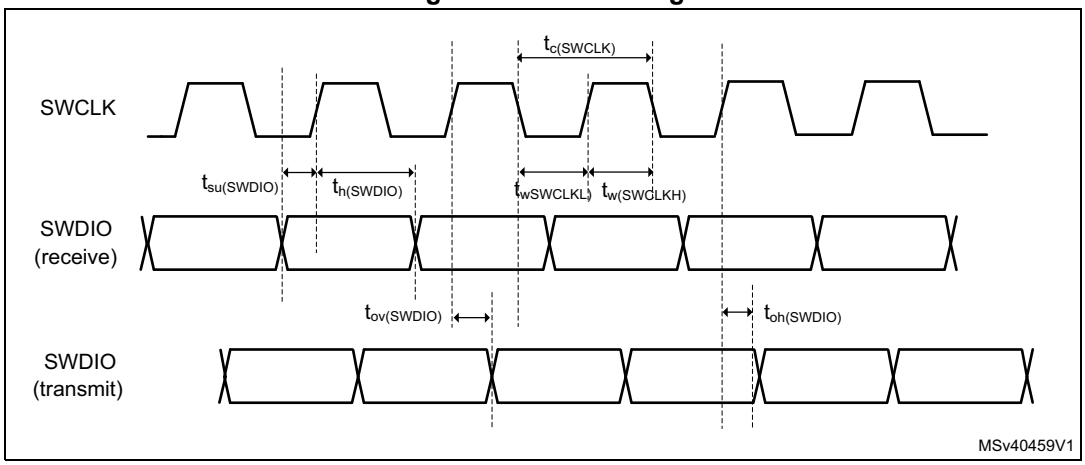


Figure 56. SWD timing



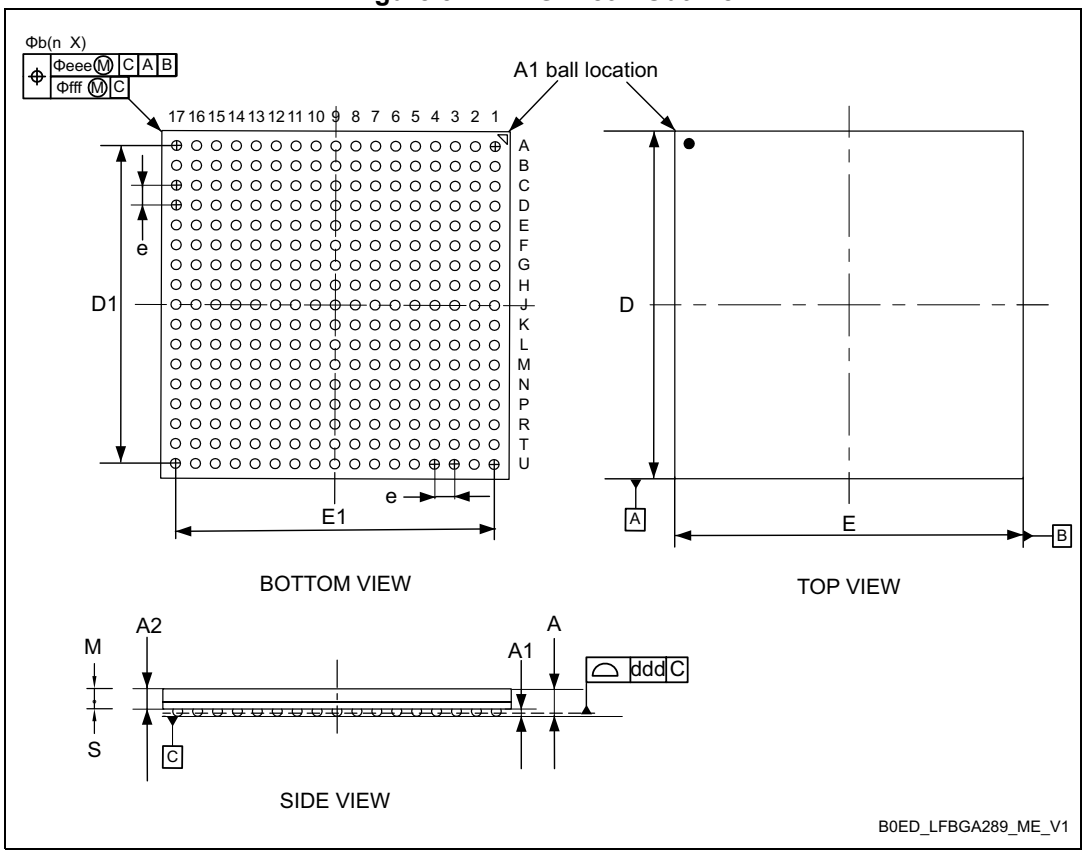
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 LFBGA289 package information (B0ED)

This LFBGA is a 289 ball, 14x14 mm, 0.8 mm pitch, low profile fine pitch ball grid array package.

Figure 57. LFBGA289 - Outline



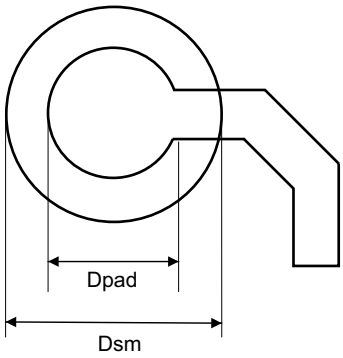
1. Drawing is not to scale.
2. The tolerance of position controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Table 109. LFBGA289 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.700	-	-	0.0669
A1	0.210	0.290	-	0.0083	0.0114	-
A2	-	0.816	-	-	32.1260	-
b[3]	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	13.850	14.000	14.150	0.5453	0.5512	0.5571
D1	-	12.800	-	-	0.5039	-
E	13.850	14.000	14.150	0.5453	0.5512	0.5571
E1	-	12.800	-	-	0.5039	-
e	-	0.800	-	-	0.0315	-
M	-	0.530	-	-	0.0209	-
S	-	0.286	-	-	0.0113	-
ddd[4]	-	0.120	-	-	0.0047	-
eee[5]	-	0.150	-	-	0.0059	-
fff	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. LFBGA stands for low profile fine pitch ball grid array. The total profile height (Dim A) is measured from the seating plane to the top of the component.
3. Initial ball equal 0.400 mm
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones

Figure 58. LFBGA289 - Recommended footprint



B02D_FP_V1

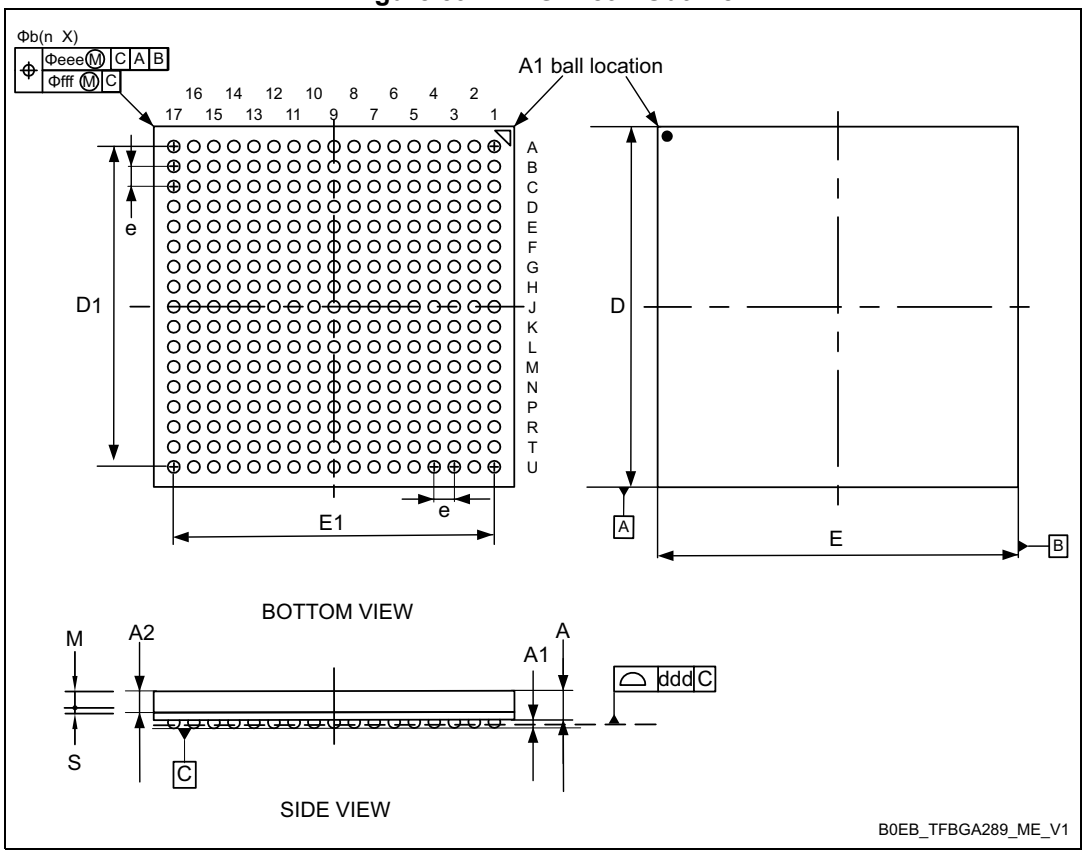
Table 110. LFBGA289 - Recommended PCB design rules

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.320 mm
Dsm	0.420 mm typ.
Stencil opening	0.320 mm
Stencil thickness	0.125 mm to 0.100 mm

7.2 TFBGA289 package information (B0EB)

This TFBGA is a 289 ball, 9x9 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package.

Figure 59. TFBGA289 - Outline



1. Drawing is not to scale.
2. The tolerance of position controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

Table 111. TFBGA289 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.200	-	-	0.0472
A1	0.140	0.210	-	0.0055	0.0083	-
A2	-	0.716	-	-	28.1890	-
b[3]	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	8.850	9.000	9.150	0.3484	0.3543	0.3602
D1	-	8.000	-	-	0.3150	-
E	8.850	9.000	9.150	0.3484	0.3543	0.3602
E1	-	8.000	-	-	0.3150	-
e	-	0.500	-	-	0.0197	-
M	-	0.530	-	-	0.0209	-
S	-	0.186	-	-	0.0073	-
ddd[4]	-	0.080	-	-	0.0031	-
eee[5]	-	0.150	-	-	0.0059	-
fff	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. TFBGA stands for thin profile fine pitch ball grid array. The total profile height (dim A) is measured from the seating plane to the top of the component.
3. Initial ball equal 0.300 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones

Figure 60. TFBGA289 - Recommended footprint

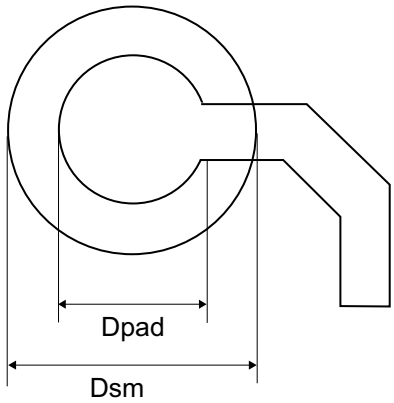


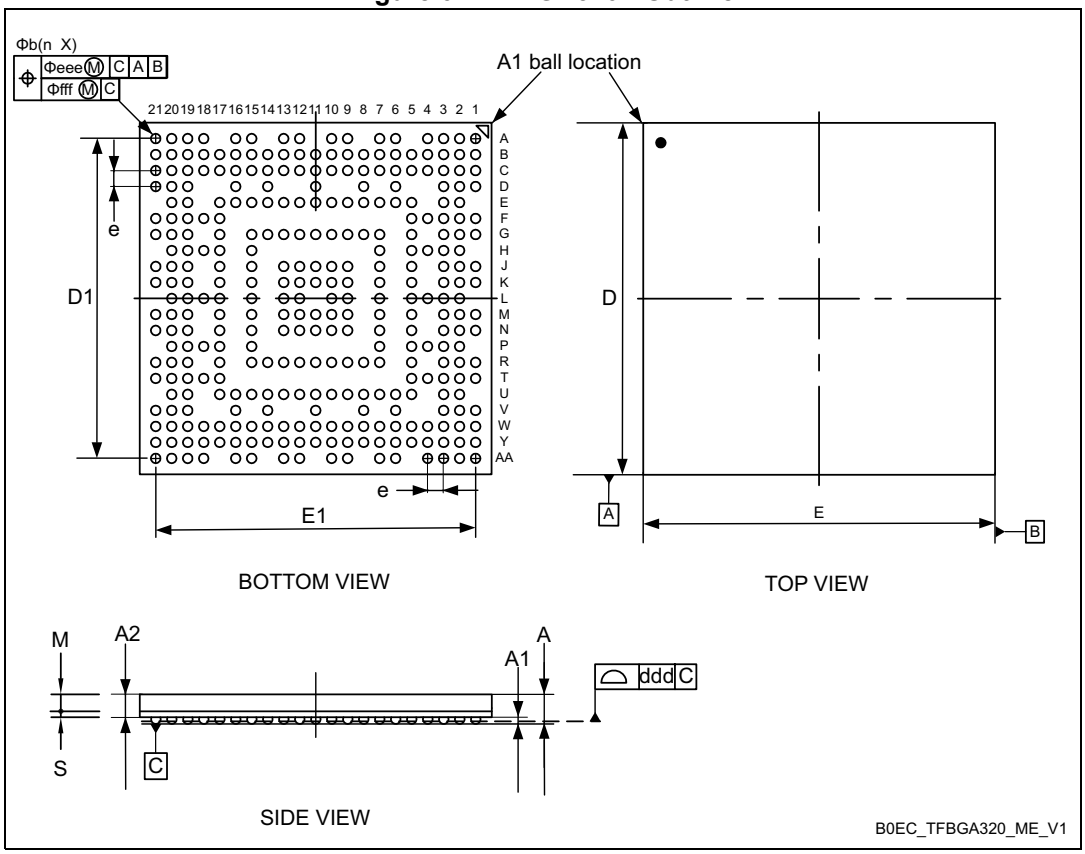
Table 112. TFBGA289 - Recommended PCB design rules

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.230 mm
Dsm	0.330 mm typ.
Stencil opening	0.230 mm
Stencil thickness	0.125 mm to 0.100 mm

7.3 TFBGA320 package information (B0EC)

This TFBGA is a 320 ball, 11x11 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package.

Figure 61. TFBGA320 - Outline



1. Drawing is not to scale.
2. The tolerance of position controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

Table 113. TFBGA320 - Mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	-	-	1.200	-	-	0.0472
A1	0.140	0.210	-	0.0055	0.0083	-
A2	-	0.716	-	-	0.0282	-
b(3)	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	10.850	11.000	11.150	0.4272	0.4331	0.4390
D1	-	10.000	-	-	0.3937	-
E	10.850	11.000	11.150	0.4272	0.4331	0.4390
E1	-	10.000	-	-	0.3937	-

Table 113. TFBGA320 - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
M	-	0.530	-	-	0.0209	-
S	-	0.186	-	-	0.0073	-
ddd[4]	-	0.080	-	-	0.0031	-
eee[5]	-	0.150	-	-	0.0059	-
fff	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. TFBGA stands for thin profile fine pitch ball grid array. The total profile height (dim A) is measured from the seating plane to the top of the component.
3. Initial ball equal 0.300 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones

Figure 62. TFBGA320 - Recommended footprint

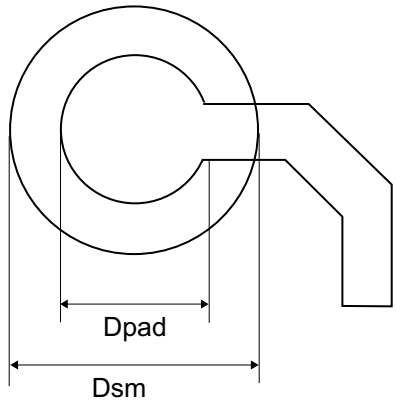


Table 114. TFBGA320 - Recommended PCB design rules

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.230 mm
Dsm	0.330 mm typ.
Stencil opening	0.230 mm
Stencil thickness	0.125 mm to 0.100 mm

7.4 Thermal characteristics

Package thermal characteristics in *Table 115* are specified with conditions as per JEDEC JESD51-6, JESD51-8, JESD51-9, and JESD51-12. These typical values will vary in function of board thermal characteristics and other components on the board.

Θ_{JA} : Thermal resistance junction-ambient.
Θ_{JB}: Thermal resistance junction-board.
Θ_{JC}: Thermal resistance junction-top-case.
Θjb: Thermal parameter junction-board.
Ψjt: Thermal parameter junction-top-case.
Motherboard type: four layers, JEDEC 2S2P

Table 115. Thermal characteristics

Symbol	Parameter	Value		Unit
		Natural convection	1m/s (200 ft/mn)	
Θ_{JA}(1)	LFBGA289 - 289-ball 14x14 mm 0.80 mm pitch	31.7	29.2	°C/W
	TFBGA289 - 289-ball 9x9 mm 0.50 mm pitch	29.3	27	
	TFBGA320 - 320-ball 11x11 mm 0.50 mm pitch	29	26.6	
Θ_{JB}(2)	LFBGA289 - 289-ball 14x14 mm 0.80 mm pitch	21.2		°C/W
	TFBGA289 - 289-ball 9x9 mm 0.50 mm pitch	15.9		
	TFBGA320 - 320-ball 11x11 mm 0.50 mm pitch	16.9		
Θ_{JC}(3)	LFBGA289 - 289-ball 14x14 mm 0.80 mm pitch	8.9		°C/W
	TFBGA289 - 289-ball 9x9 mm 0.50 mm pitch	8.6		
	TFBGA320 - 320-ball 11x11 mm 0.50 mm pitch	8.5		
Ψjb (4)	LFBGA289 - 289-ball 14x14 mm 0.80 mm pitch	21.1	20.9	°C/W
	TFBGA289 - 289-ball 9x9 mm 0.50 mm pitch	15.9	15.8	
	TFBGA320 - 320-ball 11x11 mm 0.50 mm pitch	16.9	16.8	
Ψjt (5)	LFBGA289 - 289-ball 14x14 mm 0.80 mm pitch	0.21	0.29	°C/W
	TFBGA289 - 289-ball 9x9 mm 0.50 mm pitch	0.18	0.26	
	TFBGA320 - 320-ball 11x11 mm 0.50 mm pitch	0.18	0.26	

1. Per JEDEC JESD51-9
2. Per JEDEC JESD51-8
3. Per JEDEC JESD51-12 best practice guidelines
4. Per JEDEC JESD51-12.
5. Per JEDEC JESD51-12.

7.4.1 Reference documents

JESD51-6 Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air). Available from www.jedec.org.

JESD51-8 Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board. Available from www.jedec.org.

JESD51-9 Test Boards for Area Array Surface. Mount Package Thermal. Measurements.

Available from www.jedec.org.

JESD51-12 Guidelines for Reporting and Using Electronic Package Thermal Information. Available from www.jedec.org.

7.5 Device marking

Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on *www.st.com*, for the location of ball A1 as well as the location and orientation of the marking areas versus ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8 Ordering information

Table 116. STM32MP131C/F ordering information scheme

Example: STM32 MP 131 C AE 3 T

Device family

STM32 = Arm-based 32-bit processor

Product type

MP = MPU product

Device subfamily

131 = STM32MP131 line

Security option

C = Secure boot, security features, cryptography hardware, 650 MHz
F = Secure boot, security features, cryptography hardware, 1000 MHz

Package and pin count

AE = LFBGA289 14x14, 289 balls pitch 0.8 mm

AF = TFBGA320 11x11, 320 balls pitch 0.5 mm

AG = TFBGA289 9x9, 289 balls pitch 0.5 mm

Junction temperature range

3 = -40 °C < T_J < +125 °C up to 650 MHz Cortex®-A7[1]

7 = -40 °C < T_J < +105 °C up to 1000 MHz Cortex®-A7[1]

Options

Blank = no options

Packing

T = tape and reel

No character = tray or tube

1. Refer also to the application note AN5438 “STM32MP1 Series lifetime estimates” available from the ST website *www.st.com*.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

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10 Revision history

Table 117. Document revision history

Date	Revision	Changes
16-Feb-2023	1	Initial release.
12-Jun-2023	2	Updated $t_{WULPLV_Stop2_MPU}$ and associated footnote in *Table 28: Low-power mode wakeup timings*. Added t_{INIT} in *Table 106: USB High-Speed PHY characteristics*.
07-Sep-2023	3	Removed bullet '16-byte access granularity' in *Section 3.3: DDR3/DDR3L/LPDDR2/LPDDR3 controller (DDRCTRL)*. Removed row 'Input voltage on OTG_VBUS pin' in *Table 10: Voltage characteristics*. Removed row 'OTG_VBUS I/O' in *Table 13: General operating conditions*. Updated *Figure 32: NAND controller waveforms for read access* and *Figure 32: NAND controller waveforms for read access*. Suppressed the following 2 figures. Updated *Figure 39: SPI timing diagram - slave mode and CPHA = 0*, *Figure 40: SPI timing diagram - slave mode and CPHA = 1*(1) and *Figure 41: SPI timing diagram - master mode*(1).
27-Mar-2024	4	Updated SPI on cover page. Updated V_{DDCORE} in *Section 3.6.1: Power supply scheme*. Updated *Section 3.6.2: Power supply supervisor*. Updated *Section 3.20: V_{BAT} operation*. Updated *Section 3.26.5: Independent watchdogs (IWDG1, IWDG2)*. Updated *Figure 19: Typical application with a 32.768 kHz crystal*. Updated *Figure 33: NAND controller waveforms for write access*. Updated *Figure 74: Switching characteristics for NAND flash read cycles*.
25-Sep-2024	5	Updated *Up to 26 communication peripherals*. Updated *Section 3.31: Universal synchronous asynchronous receiver transmitter (USART1, USART2, USART3, USART6 and UART4, UART5, UART7, UART8)*. Updated *Table 5: USART/UART features*. Updated *Section 3.35: Secure digital input/output MultiMediaCard interfaces (SDMMC1, SDMMC2)*. Updated *Table 7: STM32MP131C/F ball definitions*. Updated *Table 8: Alternate function AF0 to AF7*. Updated *Section 6.3.19: FMC characteristics*.

Table 117. Document revision history

Date	Revision	Changes
25-Sep-2024	5 (continued)	Updated *Figure 28: Synchronous multiplexed NOR/PSRAM read timings*. Updated *Table 70: Synchronous multiplexed NOR/PSRAM read timings*. Updated *Figure 29: Synchronous multiplexed PSRAM write timings*. Updated *Table 71: Synchronous multiplexed PSRAM write timings*. Updated *Figure 30: Synchronous non-multiplexed NOR/PSRAM read timings*. Updated *Table 72: Synchronous non-multiplexed NOR/PSRAM read timings*. Updated *Figure 31: Synchronous non-multiplexed PSRAM write timings*. Updated *Table 73: Synchronous non-multiplexed PSRAM write timings*. Added Updated *Figure 28: Synchronous multiplexed NOR/PSRAM read timings*. Added *Figure 36: ADC accuracy characteristics*. Added *Figure 37: Typical connection diagram using the ADC with FT/TT pins featuring analog switch function*. Updated *Section 6.3.34: USART (SPI mode) interface characteristics*. Updated *Table 105: USART (SPI mode) characteristics*. Added *Figure 53: USART timing diagram in SPI master mode*. Added *Figure 54: USART timing diagram in SPI slave mode*. Added package code in the following section tites: *Section 7.1: LFBGA289 package information (B0ED)*, *Section 7.2: TFBGA289 package information (B0EB)*, *Section 7.3: TFBGA320 package information (B0EC)*.
01-Mar-2025	6	Updated *Section : High-speed external clock generated from a crystal/ceramic resonator*. Updated *Section 6.3.12: PLL spread spectrum clock generation (SSCG) characteristics*. Updated *Figure 2: Power-up/down sequence*. Updated *Figure 4: Voltage reference buffer*. Updated *Figure 10: Power supply scheme*. Updated *Figure 34: QUADSPI timing diagram - SDR mode*. Updated *Figure 35: QUADSPI timing diagram - DDR mode*. Updated *Figure 38: Channel transceiver timing diagrams*. Updated *Figure 44: SAI master timing waveforms*. Updated *Figure 45: SAI slave timing waveforms*. Removed Section USB OTG_FS characteristics.

Table 117. Document revision history

Date	Revision	Changes
04-Apr-2025	7	Updated *Table 76: QUADSPI characteristics in SDR mode*. Updated *Table 77: QUADSPI characteristics in DDR mode*.

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