ILPS28QSW

Datasheet

Dual full-scale, 1260 hPa and 4060 hPa, absolute digital output barometer with Qvar detection in a water-resistant package

CCLGA-7L
2.8 x 2.8 x 1.95 mm

Product status link
ILPS28QSW

Product summary	
Order code	ILPS28QSWTR
Temperature range	-40 to +105 °C
Package	CCLGA-7L 2.8 x 2.8 x 1.95 mm
Packing	Tape and reel

Product resources
TN0018 (design and soldering)

Product labels
SUSTAINABLE TECHNOLOGY; LONGEVITY 10 YEARS COMMITMENT

Features

- Dual full-scale absolute pressure sensor in a water-resistant package
  - Mode 1: 260 ~ 1260 hPa
  - Mode 2: 260 ~ 4060 hPa
- Embedded analog hub for processing analog input data
- Embedded Qvar for detecting electric charge variation
- Current consumption down to 1.7 µA
- Absolute pressure accuracy: 0.5 hPa
- Low pressure sensor noise: 0.32 Pa
- Embedded temperature compensation
- Extended temperature range from -40 to +105 °C
- 24-bit pressure data output
- ODR from 1 Hz to 200 Hz
- I²C or MIPI I3C^{SM} interface
- Embedded FIFO
- Supply voltage: 1.7 to 3.6 V
- Easily sealed package with O-ring
- ECOPACK lead-free compliant

Applications

- Industrial applications
- Gas and water metering
- Weather station equipment
- Altimeters and barometers for outdoor devices
- Smart filters
- Ventilators and CPAP equipment
- Man-down detection

Description

The ILPS28QSW is an ultracompact, piezoresistive, absolute pressure sensor that functions as a digital output barometer, supporting dual full-scale up to user-selectable 4060 hPa.

The device comprises a sensing element and an IC interface that communicates over the I²C or MIPI I3C^{SM} interface from the sensing element to the application. The ILPS28QSW provides lower power consumption, achieving lower pressure noise than its predecessor.

The ILPS28QSW embeds an analog hub sensing functionality that is able to connect an analog input and convert it to a digital signal for embedded processing. In addition, an embedded Qvar (electric charge variation detection) channel can be enabled for sensing in applications such as water-leak detection, tap, double tap, long press, and L/R - R/L swipe.

The ILPS28QSW is available in a ceramic LGA package with metal lid. It is guaranteed to operate over a temperature range extending from -40 °C to +105 °C. The package is holed to allow external pressure to reach the sensing element. Gel inside the IC protects the electrical components from water and the metal cap is, optionally, connected to ground or left floating electrically in the application PCB layout. The connection of the metal cap is determined according to the customer's target application.

1 Block diagrams

Figure 1. **Device architecture block diagram**

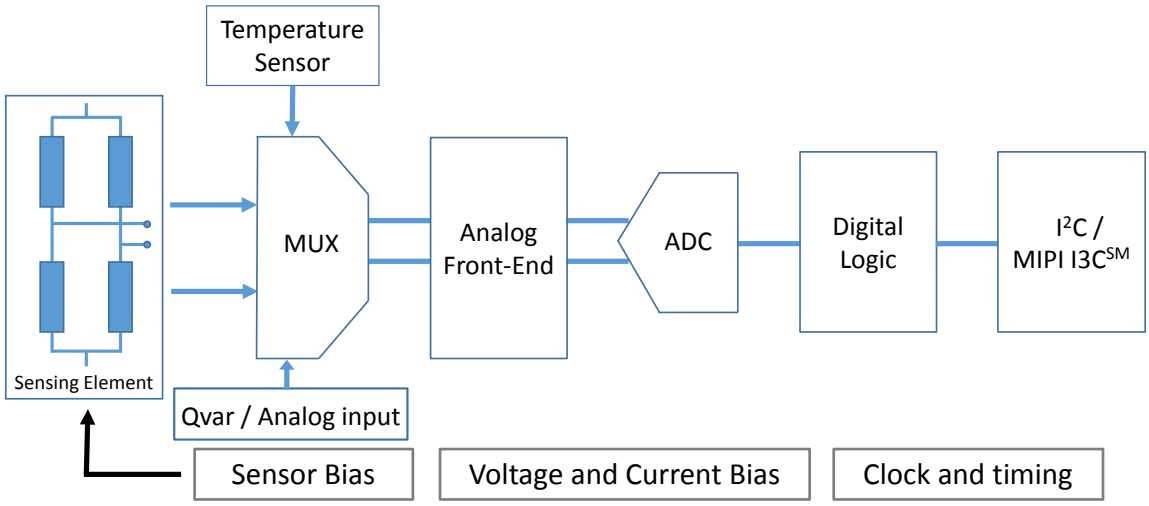
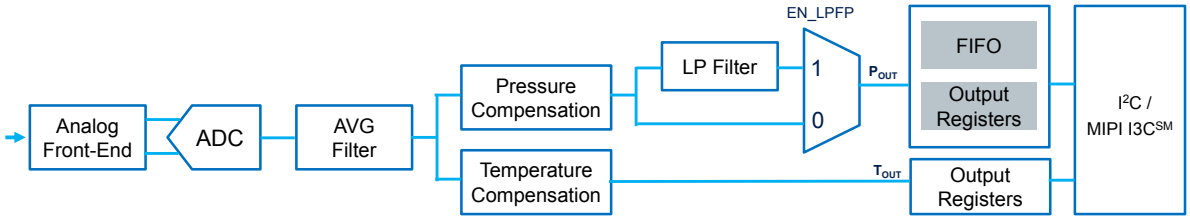


Figure 2. **Digital logic**



2 Pin description

Figure 3. **Pin connections (bottom view)**

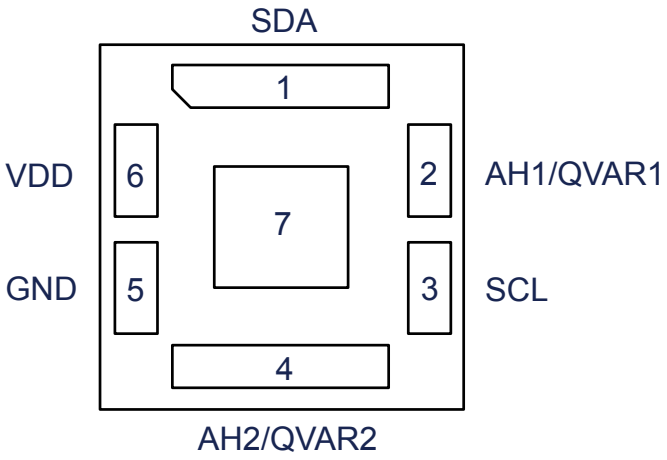


Table 1. **Pin description**

Pin number	Name	Function
1	SDA	I²C / MIPI I3C^{SM} serial data (SDA)
2	AH1/QVAR1	Connect to GND if analog input / Qvar sensing is not needed.
3	SCL	I²C / MIPI I3C^{SM} serial clock (SCL)
4	AH2/QVAR2	Connect to GND if analog input / Qvar sensing is not needed.
5	GND	0 V supply
6	VDD	Power supply
7	PAD2LID	Pad connection to metal lid

3 Mechanical and electrical specifications

3.1 Mechanical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 2. Pressure and temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Pressure sensor characteristics						
P_{Top}	Operating temperature range		-40		+105	°C
P_{op}	Operating pressure range Mode 1 Mode 2		 260 260		 1260 4060	hPa
P_{bits}	Pressure output data			24		bits
P_{sens}	Pressure sensitivity Mode 1 Mode 2			 4096 2048		LSB/hPa
P_{AccRel}	Relative pressure accuracy(2) Mode 1 Mode 2	T =25 °C P= 800 ~ 1100 hPa P = 2060 ~ 4060 hPa		 ±0.015 ±1		hPa
P_{AccT}	Absolute pressure accuracy Mode 1 Mode 2 Refer to Table 3	P = 660 ~ 1260 T = 0 ~ 65 °C T = -40 ~ 105 °C P = 1260 ~ 4060 hPa T = 0 ~ 65 °C T = -20 ~ 105 °C		 ±1 ±2.5 ±0.43% ±0.6%		hPa
P_{noise}	RMS pressure sensing noise(3) Mode1 Mode 2 Refer to Table 25	T = 25 °C		 0.32 0.57		Pa RMS
ODR_{Pres}	Pressure output data rate			1 4 10 25 50 75 100 200		Hz
P_longterm	Pressure accuracy, long-term stability(4)			±1		hPa/year
P_drift	Soldering drift			±0.5		hPa
Temperature sensor characteristics						
T_{op}	Operating temperature range		-40		+105	°C
T_{sens}	Temperature sensitivity			100		LSB/°C

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
T_{acc}	Temperature absolute accuracy	T= 25 to 65 °C		±1.5		°C
ODR_T	Output temperature data rate			1 4 10 25 50 75 100 200		Hz

1. *Typical specifications are not guaranteed.*
2. *The typ. value is defined based on characterization data with 10 hPa pressure interval in mode 1 and 100 hPa pressure interval in mode 2.*
3. *Pressure noise RMS evaluated in a controlled environment, based on the average standard deviation of 50 measurements with AVG = 512, BW = ODR/9.*
4. *Typ. value is defined considering a 5-year life cycle of the final application.*

Table 3. Absolute pressure accuracy at different full-scale modes

Full-scale mode	Condition	Typ. absolute pressure accuracy [hPa]
Mode 1 (full scale up to 1260 hPa)	P = 660 ~ 1260 & T = 0 ~ 65 °C	±1 hPa
	P = 660 ~ 1260 & T = -40 ~ 105 °C	±2.5 hPa
Mode 2 (full scale up to 4060 hPa)	P = 1260 ~ 2060 & T = 0 ~ 65 °C	±0.15% of input pressure
	P = 1260 ~ 2060 & T = -40 ~ 105 °C	±0.23% of input pressure
	P = 2060 ~ 3060 & T = 0 ~ 65 °C	±0.25% of input pressure
	P = 2060 ~ 3060 & T = -40 ~ 105 °C	±0.34% of input pressure
	P = 3060 ~ 4060 & T = 0 ~ 65 °C	±0.43% of input pressure
	P = 3060 ~ 4060 & T = -40 ~ 105 °C	±0.6% of input pressure

3.2 Electrical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
VDD	Supply voltage		1.7		3.6	V
Idd	Supply current for pressure acquisition	@ 1 Hz one-shot AVG = 4 when AH and Qvar are disabled(2) AVG = 4 when AH and Qvar are enabled		1.7 4.2		µA
		@ 1 Hz one-shot AVG = 128 when AH and Qvar are disabled(2) AVG = 128 when AH and Qvar are enabled		9.4 11.9		
IddPdn	Power-down current when AH and Qvar are disabled(2) Power-down current when AH and Qvar are enabled			1 3.6		µA

1. *Typical specifications are not guaranteed.*
2. *To use only the pressure sensor without Qvar, 00h must be written in register 5Fh when the device is powered on. AH1/QVAR1(pin 2) and AH2/QVAR2 (pin 4) must be connected to GND.*

Table 5. Electrical parameters of Qvar (@Vdd = 1.8 V, T = 25 °C)

Parameter	Typ.	Unit
Offset (shorted inputs)	±0.021	mV
Noise (shorted inputs)	9	µV
Qvar gain	426k	LSB/mV
CMRR	64	dB
Input impedance	18(1)	MΩ
Input range	±18	mV

1. *Depending on ODR and AVG, refer to Table 6*

Table 6. Input impedance of Qvar

Input impedance [MΩ]	R_{IN} (ODR, AVG) [MΩ] ODR [Hz]							
AVG	1	4	10	25	50	75	100	200
4	21.6	21.5	21.4	21.1	20.5	20.0	19.6	17.9
8	21.6	21.4	21.2	20.5	19.6	18.7	17.9	15.3
16	21.5	21.2	20.7	19.6	17.9	16.5	15.3	11.8
32	21.4	20.9	19.9	17.9	15.3	13.3	11.8	8.1
64	21.2	20.3	18.5	15.3	11.8	9.6	8.1	5.0
128	20.9	19.1	16.2	11.8	8.1	6.2	5.0	2.8
512	19.1	14.1	9.3	5.0	2.8	2.0	1.5	0.8

Table 7. **DC characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DC input characteristics						
Vil	Low-level input voltage (Schmitt buffer)	-	-	-	0.3 * VDD	V
Vih	High-level input voltage (Schmitt buffer)	-	0.7 * VDD	-	-	V
DC output characteristics						
Vol	Low-level output voltage		-	-	0.2	V
Voh	High-level output voltage		VDD - 0.2	-	-	V

4 Communication interface characteristics

4.1 I²C - inter-IC control interface

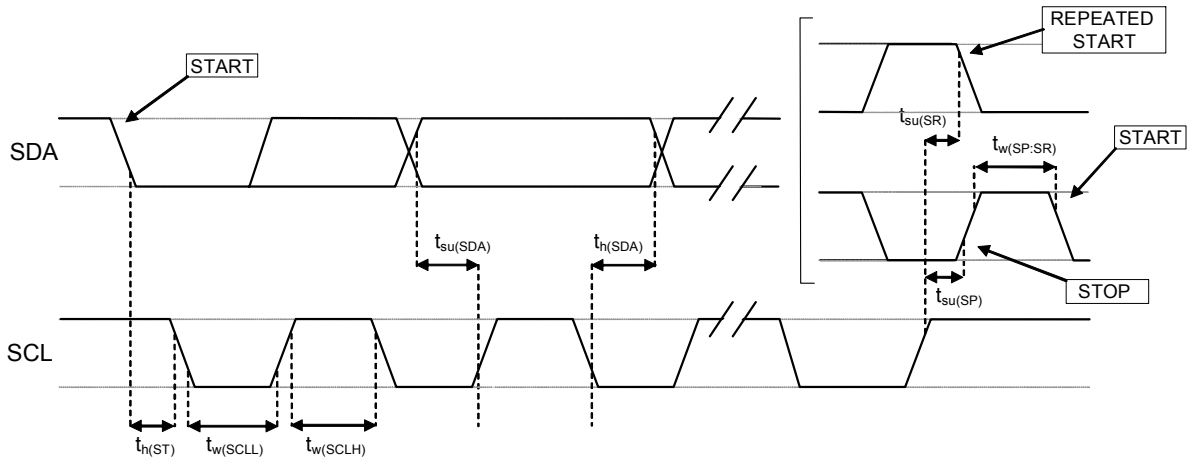
Subject to general operating conditions for Vdd and T_{OP}.

Table 8. I²C slave timing values

Symbol	Parameter	I²C fast mode(1)(2)		I²C fast mode plus(1)(2)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	400	0	1000	kHz
$t_{w(SCLL)}$	SCL clock low time	1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	0.6		0.26		
$t_{su(SDA)}$	SDA setup time	100		50		ns
$t_{h(SDA)}$	SDA data hold time	0	0.9	0		µs
$t_{h(ST)}$	START/REPEATED START condition hold time	0.6		0.26		
$t_{su(SR)}$	REPEATED START condition setup time	0.6		0.26		
$t_{su(SP)}$	STOP condition setup time	0.6		0.26		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	1.3		0.5		
	Data valid time		0.9		0.45	
	Data valid acknowledge time		0.9		0.45	
C_B	Capacitive load for each bus line		400		550	pF

1. *Data based on standard I²C protocol requirement, not tested in production.*
2. *Data for I²C fast mode and I²C fast mode plus have been validated by characterization, not tested in production.*

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.3·VDD and 0.7·VDD for both ports.

4.2 Absolute maximum ratings

Stress above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Ratings	Maximumvalue	Unit
VDD	Supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to VDD+0.3	V
P_{water}	Overpressure	1	MPa
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

5 Functionality

The ILPS28QSW is a high-resolution, digital output pressure sensor packaged in a CCLGA package with metal lid. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach and an IC interface which communicates a digital signal from the sensing element to the application.

5.1 Sensing element

An ST proprietary process is used to obtain a silicon membrane for MEMS pressure sensors. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances whose output signal is converted by the IC interface.

5.2 IC interface

The complete measurement chain is composed of a low-noise amplifier which converts the resistance unbalance of the MEMS sensors (pressure and temperature) into an analog voltage using an analog-to-digital converter.

The pressure and temperature data may be accessed through an I²C/MIPI I3C^{SM} interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The ILPS28QSW features a data-ready signal which indicates when a new set of measured pressure and temperature data are available, thus simplifying data synchronization in the digital system that uses the device.

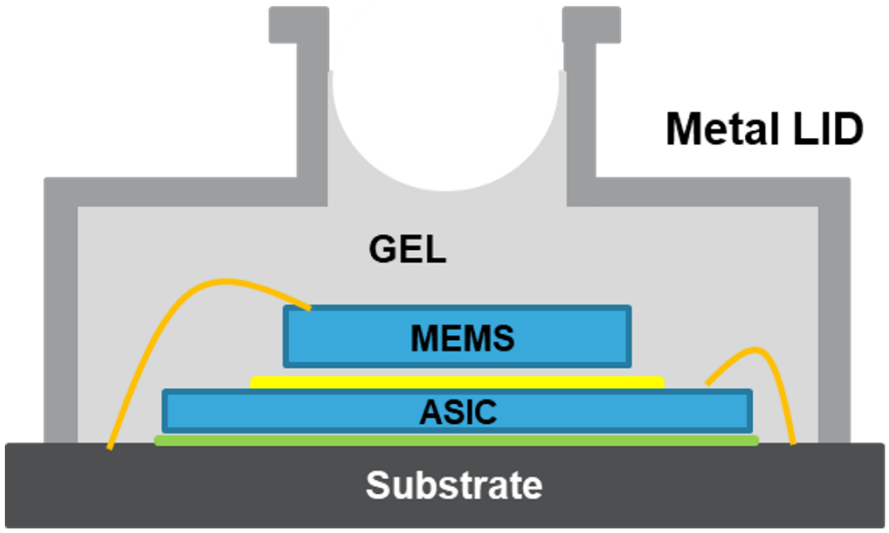
5.3 Factory calibration

The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation which allows the device to be used without requiring any further calibration.

5.4 Device structure

The ILPS28QSW has a unique cylindrical package solution with a full metal lid assembled on ceramic substrate and this cylindrical package provides an easy assembly with O-rings in the end user's application.

Figure 5. ILPS28QSW internal structure



This structure (Figure 5) is designed and verified to resist water pressure up to 10 ATM and the potting gel in the ILPS28QSW has been proven to protect electronic components from long-term exposure to harsh environments such as water mixed with chlorine, bromine, commercial washing detergent and fuels, solvents and chemicals. It also provides excellent low-stress encapsulation performance for sensitive electronic components from severe environmental conditions such as high temperature and humidity, refer to the properties of the gel that are given in the following table.

Table 10. Potting gel properties

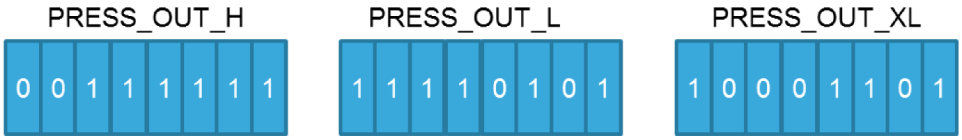
Properties	Potting gel
Permeability g/m^2·24 hr	7
Hardness (penetration) based on ASTM D1403	70
Ultralow Young's modulus	Less than 0.01 GPa
TCE (thermal coefficient of expansion)	300 ppm/°C

5.5 Interpreting pressure readings

The pressure data are stored in three registers: PRESS_OUT_H (2Ah), PRESS_OUT_L (29h), and PRESS_OUT_XL (28h). The value is expressed as a 24-bit signed number (in two's complement).

To obtain the pressure in hPa, take the complete 24-bit word and then divide by the sensitivity 4096 LSB/hPa when the FS_MODE bit is 0 (in mode 1, full scale is up to 1260 hPa) or divide by the sensitivity 2096 LSB/hPa when the FS_MODE bit is 1 (in mode 2, full scale is up to 4060 hPa). This same interpretation is applied to pressure readings when FIFO is enabled and the pressure data are stored in three registers: FIFO_DATA_OUT_PRESS_XL (78h), FIFO_DATA_OUT_PRESS_L (79h), and FIFO_DATA_OUT_PRESS_H (7Ah).

Figure 6. Pressure readings



$$Pressure\,Value = PRESS\_OUT\_H(2Ah)\,\&\,PRESS\_OUT\_L(29h)\,\&\,PRESS\_OUT\_XL \quad (1)$$

$$(28h) = 3FF58Dh = 4191629\,LSB\ \ (signed\ decimal) \quad (2)$$

When the FS_MODE bit = 0, (CTRL_REG2 (11h)) for full scale up to 1260 hPa:

$$Pressure\ (hPA) = \frac{Pressure\ value\ (LSB)}{Sensitivity} = \frac{4191629\ LSB}{4096\ LSB/hPA} = 1023.3\ hPA$$

When the FS_MODE bit = 1, (CTRL_REG2 (11h)) for full scale up to 4060 hPa:

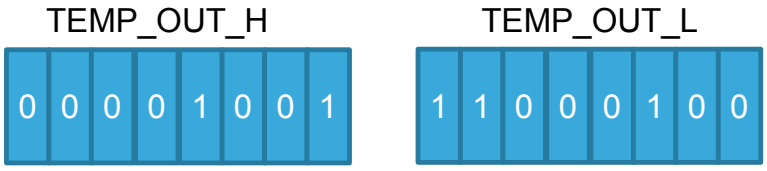
$$Pressure\ (hPA) = \frac{Pressure\ value\ (LSB)}{Sensitivity} = \frac{4191629\ LSB}{2048\ LSB/hPA} = 2046.7\ hPA$$

5.6 Interpreting temperature readings

The temperature data are stored in two registers: TEMP_OUT_H (2Ch) and TEMP_OUT_L (2Bh).

The value is expressed as two's complement. To obtain the temperature in °C, take the two's complement of the complete 16-bit word and then divide by the sensitivity 100 LSB/°C.

Figure 7. Temperature readings



Temperature Value (LSB) = TEMP_OUT_H (2Ch) & TEMP_OUT_L (2Bh)
= 09C4 = 2500 LSB (decimal signed)

$$\text{Temperature (°C)} = \frac{\text{Temperature Value (LSB)}}{\text{Sensitivity}} = \frac{2500\ \text{LSB}}{100\ \text{LSB/°C}} = 25.00\text{°C}$$

6 FIFO

The ILPS28QSW embeds 128 slots of 24-bit data FIFO to store the pressure output values. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to six different modes:

- Bypass mode
- FIFO mode
- Continuous (dynamic-stream) mode
- Continuous (dynamic-stream)-to-FIFO mode
- Bypass-to-continuous (dynamic-stream)
- Bypass-to-FIFO mode

The FIFO buffer is enabled when a configuration different from all bits 0 are written in FIFO_CTRL (14h) and each mode is selected by the TRIG_MODES bit and F_MODE[1:0] bits in FIFO_CTRL (14h). Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the FIFO_STATUS1 (25h) and FIFO_STATUS2 (26h) registers.

FIFO_STATUS2 (26h)(FIFO_WTM_IA) goes to 1 when the number of unread samples (FIFO_STATUS1 (25h) (FSS[7:0]) is greater than or equal to WTM[6:0] in FIFO_WTM (15h). If FIFO_WTM (15h)(WTM[6:0]) is equal to 0, FIFO_STATUS2 (26h)(FIFO_WTM_IA) stays at 0.

FIFO_STATUS2 (26h)(FIFO_OVR_IA) is equal to 1 if a FIFO slot is overwritten.

FIFO_STATUS1 (25h)(FSS[7:0]) contains stored data levels of unread samples; when FSS[7:0] is equal to 00000000, FIFO is empty; when FSS[7:0] is equal to 10000000, FIFO is full and the unread samples are 128.

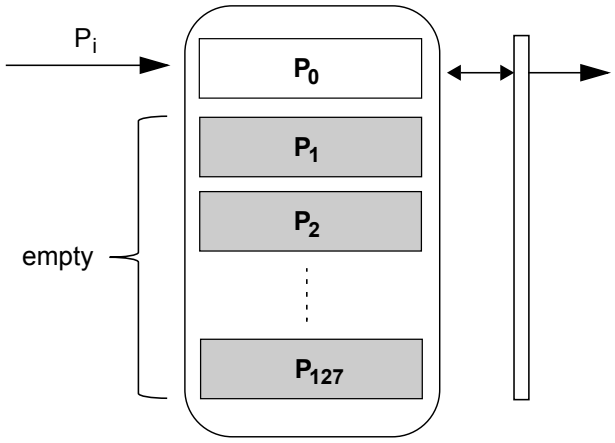
6.1 Bypass mode

In bypass mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 000 or 100), the FIFO is not operational and it remains empty.

Switching to bypass mode is also used to reset the FIFO. Passing through bypass mode is mandatory when switching between different FIFO buffer operating modes.

As described in the next figure, for each channel only the first address is used. When new data is available, the older data is overwritten.

Figure 8. Bypass mode



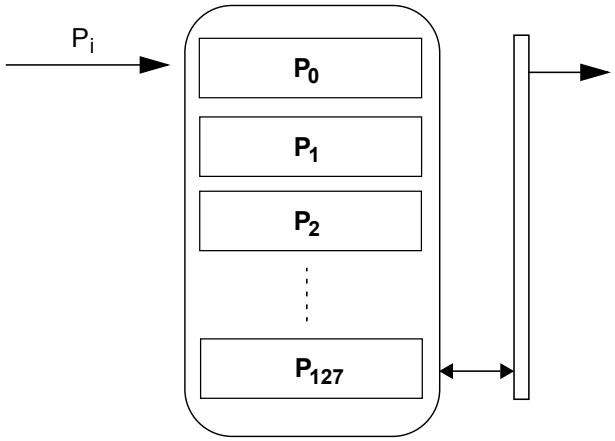
6.2 FIFO mode

In FIFO mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 001) data from the output PRESS_OUT_XL (28h), PRESS_OUT_L (29h), and PRESS_OUT_H (2Ah) are stored in the FIFO until it is full.

To reset FIFO content, in order to select bypass mode the value 000 must be written in FIFO_CTRL (14h) (TRIG_MODE & F_MODE[1:0]). After this reset command it is possible to restart FIFO mode by writing the value 001 in FIFO_CTRL (14h)(TRIG_MODE & F_MODE[1:0]).

The FIFO buffer memorizes 128 levels of data, but the depth of the FIFO can be resized/reduced by setting the FIFO_CTRL (14h)(STOP_ON_WTM) bit. If the STOP_ON_WTM bit is set to 1, FIFO depth is limited to FIFO_WTM (15h)(WTM[6:0]) data.

Figure 9. FIFO mode



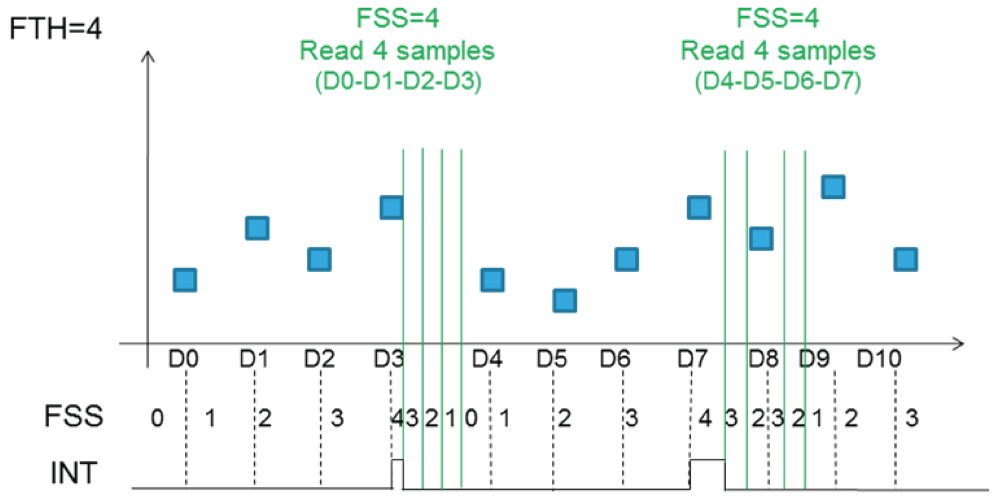
6.3 Continuous (dynamic-stream) mode

In continuous (dynamic-stream) mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 011) after emptying the FIFO, the first new sample that arrives becomes the first to be read in a subsequent read burst. In this way, the number of new data available in FIFO does not depend on the previous read.

In continuous (dynamic-stream) mode FIFO_STATUS1 (25h)(FSS[7:0]) is the number of new pressure and temperature samples available in the FIFO buffer.

Continuous (dynamic-stream) is intended to be used to read FIFO_STATUS1 (25h)(FSS[7:0]) samples when it is not possible to guarantee reading data within 1/ODR time period.

Figure 10. Continuous (dynamic-stream) mode

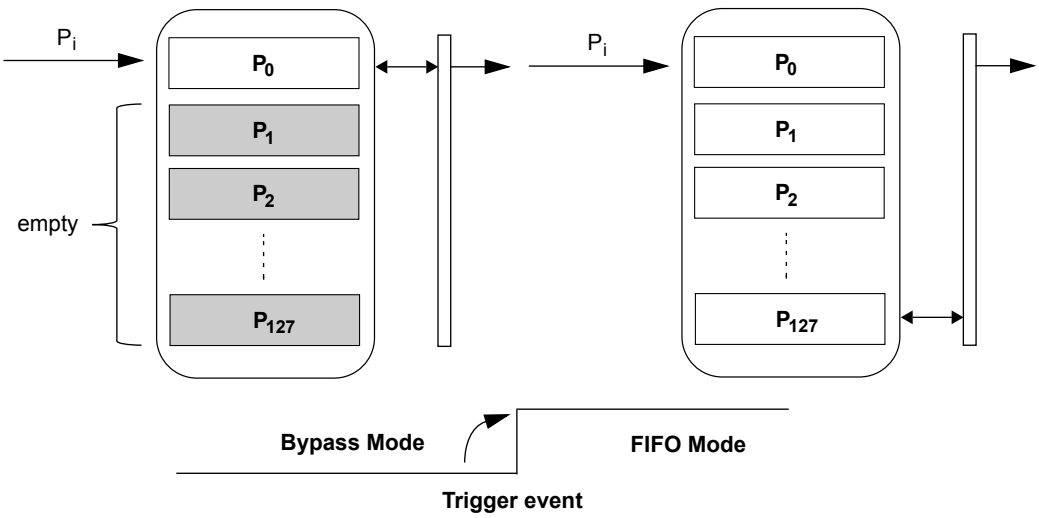


6.4 Bypass-to-FIFO mode

In bypass-to-FIFO mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 101), FIFO behavior switches when the INT_SOURCE (24h)(IA) bit rises for the first time. When the INT_SOURCE (24h)(IA) bit is equal to 0, FIFO behaves like in bypass mode. Once the INT_SOURCE (24h)(IA) bit rises to 1, FIFO behavior switches and keeps behaving like in FIFO mode.

An interrupt generator has to be set to the desired configuration through INTERRUPT_CFG (0Bh).

Figure 11. Bypass-to-FIFO mode

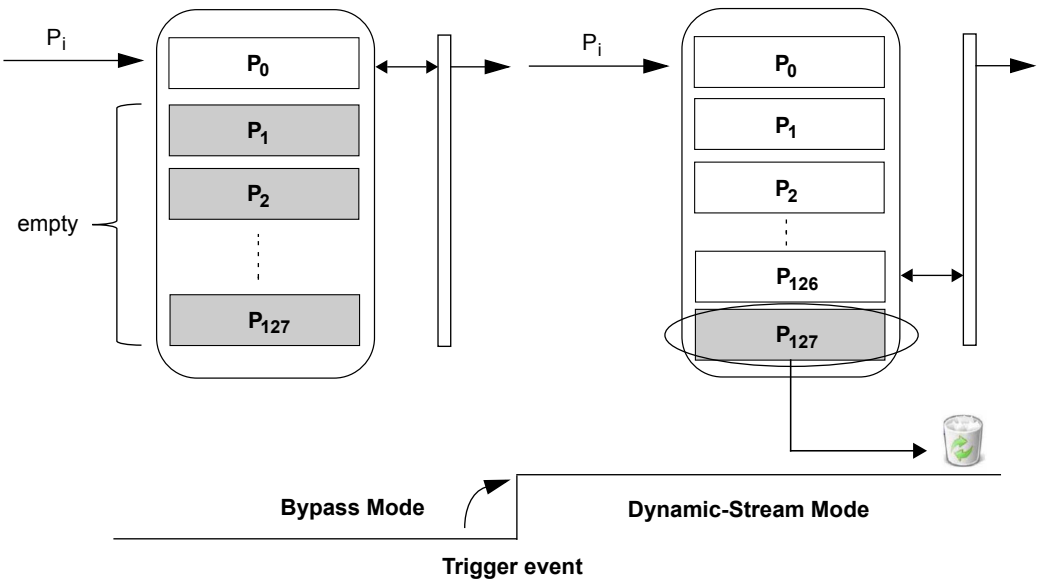


6.5 Bypass-to-continuous (dynamic-stream) mode

In bypass-to-continuous (dynamic-stream) mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 110), FIFO operates in bypass mode until it switches to continuous (dynamic-stream) mode behavior when INT_SOURCE (24h)(IA) rises to 1, then FIFO behavior keeps behaving like in continuous (dynamic-stream) mode.

An interrupt generator has to be set to the desired configuration through INTERRUPT_CFG (0Bh).

Figure 12. Bypass-to-continuous (dynamic-stream) mode

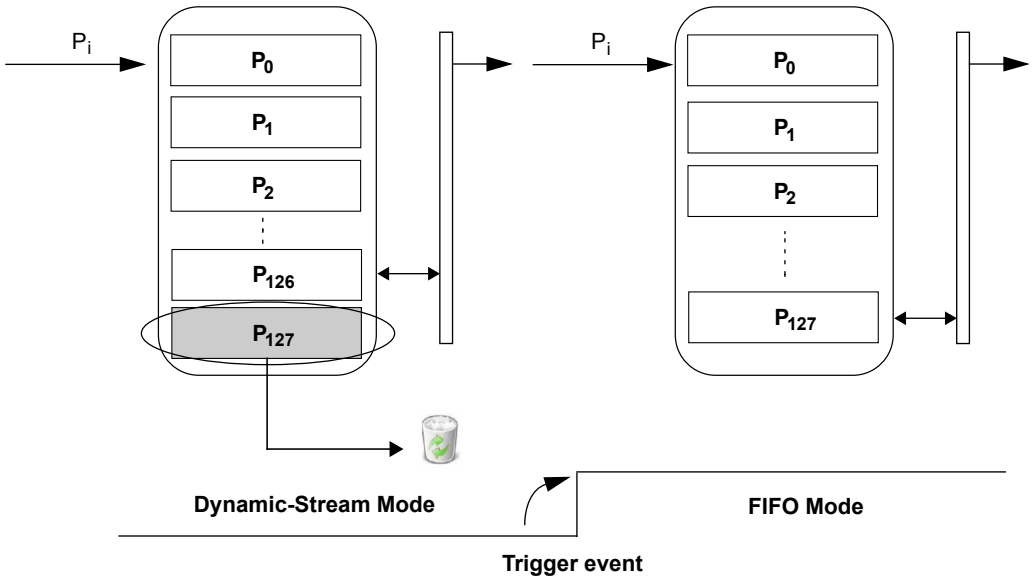


6.6 Continuous (dynamic-stream)-to-FIFO mode

In continuous (dynamic-stream)-to-FIFO mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 111), data are stored in FIFO and FIFO operates in continuous (dynamic-stream) mode behavior until it switches to FIFO mode behavior when INT_SOURCE (24h)(IA) rises to 1.

An interrupt generator has to be set to the desired configuration through INTERRUPT_CFG (0Bh).

Figure 13. Continuous (dynamic-stream)-to-FIFO mode



6.7 Retrieving data from FIFO

FIFO data is read through FIFO_DATA_OUT_PRESS (78h, 79h, and 7Ah).

The read address is automatically updated by the device and it rolls back to 78h when register 7Ch is reached. In order to read all FIFO levels in a multiple byte read, 384 bytes (3 output registers with 128 levels) must be read.

7 Application hints

Figure 14. **ILPS28QSW electrical connections**

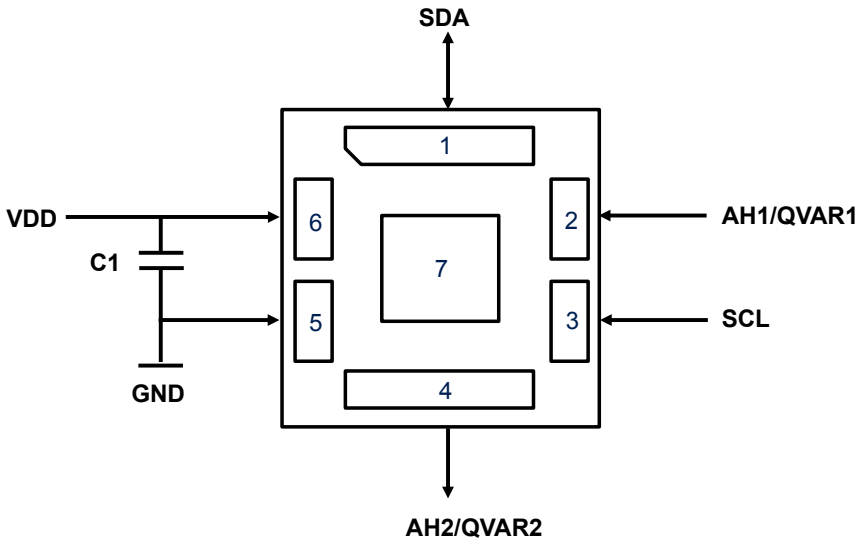
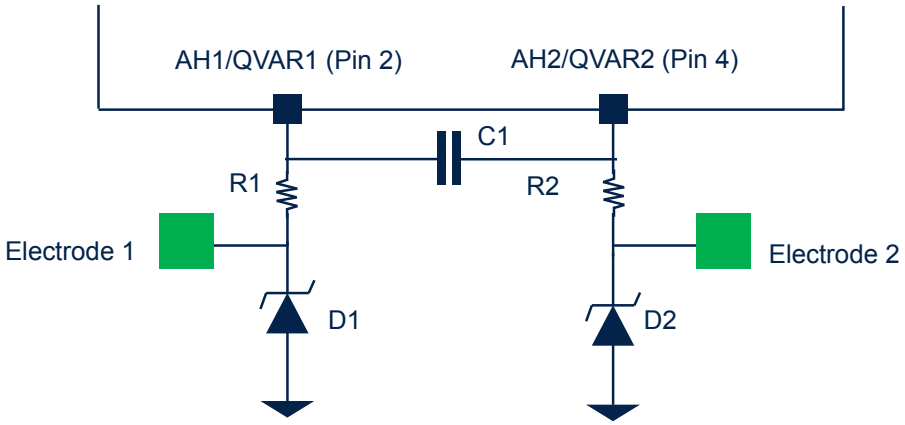


Figure 15. **AH (analog hub) / Qvar external connections to pin 2, pin 4**



Name	Value
C1	10nF
R1,R2	500 Ohm
D1,D2	ESD Diode*

*ST ESDALCL5-1BM2 is reference as ST catalog product but other similar features of ESD diode also can be used.

The device power supply must be provided through the VDD line; a power supply decoupling capacitor C1 (100 nF) must be placed as near as possible to the supply pins of the device. Depending on the application, an additional capacitor of 4.7 µF could be placed on the VDD line.

In case the AH (analog hub) / Qvar is not used, both AH1/QVAR1 (pin 2) and AH2/QVAR2 (pin 4) need to be connected to GND. Otherwise, when the AH (analog hub) / Qvar function is enabled in the application, the external network (see Figure 15) needs to be connected to both pin 2 and pin 4.

The functionality of the device and the measured data outputs are selectable and accessible through the I²C, MIPI I3C^{SM} interface.

The metal lid is physically connected to pin 7 at component level and pin 7 can be used to connect the metal lid either to GND or left unconnected (floating) on the PCB of the application. The following table indicates the two cases of the metal LID connection. It is highly recommended that pin 7 be soldered to the PCB (left unconnected electrically) or soldered to GND to enhance the solderability of the device.

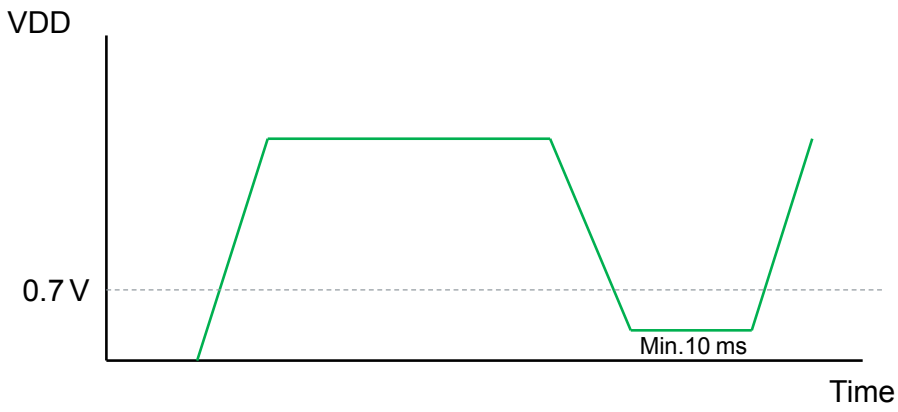
Table 11. Metal lid and pin 7 connections

Metal lid	Pin 7 connection to PCB(1)
Leave unconnected (floating)	Electrically leave unconnected (floating)
Connect to GND	Electrically connect to GND

1. *Pin 7 should be soldered to the PCB to improve the solderability of the device.*

Note: To guarantee proper power-off of the device, it is recommended to maintain the duration of the VDD line to GND for at least 10 ms.

Figure 16. ILPS28QSW power-off sequence



- VDD rise / fall time : 10 µs ~ 100 ms
- VDD must be lower than 0.7 V for at least 10 ms during power-off sequence for correct POR

7.1 Analog hub (AH) / Qvar functions

The ILPS28QSW embeds an analog hub sensing functionality that is able to connect an analog input and convert it to a digital signal as output. In addition, Qvar sensing with external electrodes can be used for user interfaces like water-leak detection, tap, double tap, long press, and L/R - R/L swipe. Refer to application note AN5755 for additional details.

The input impedance between AH/QVAR1 (pin 2) and AH/QVAR2 (pin 4) of ILPS28QSW depends on the AVG and ODR configuration in Table 6. Input impedance of Qvar.

7.2 Power-saving tip for the pressure sensor, disabling the analog hub (AH) / Qvar feature

The analog hub (AH) / Qvar feature is enabled by default and this feature causes slightly higher power consumption during operating and power-down modes to support the AH/Qvar functions. Thus, it is recommended to use the following procedure to save power consumption in case the application doesn't need the AH/Qvar feature.

How to save power consumption? First of all, AH1/QVAR1 (pin 2) and AH2/QVAR2 (pin 4) must be connected to GND on the PCB (hardware design). Second, the application must write 00h in the 5Fh register whenever the application is powered on. Following this procedure, the device operates only in pressure sensor mode, disabling AH/Qvar to achieve lower power consumption as described in Table 4. Electrical characteristics.

7.3 Soldering information

The CCLGA package is compliant with the ECOPACK standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

8 Digital interfaces

8.1 Serial interfaces

The registers embedded in the ILPS28QSW may be accessed through the I²C, MIPI I3C^{SM} serial interfaces.

Table 12. Serial interface pin description

Pin name	Pin description
SCL	I²C / MIPI I3C^{SM} serial clock (SCL)
SDA	I²C / MIPI I3C^{SM} serial data (SDA)

8.2 I²C serial interface

The ILPS28QSW I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in the following table.

Table 13. I²C terminology

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines have to be connected to VDD through pull-up resistors.

The I²C interface is compliant with fast mode plus (1 MHz) I²C standards as well as with the normal mode.

8.2.1 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After the master has transmitted this, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The 7-bit slave address (SAD) associated to the ILPS28QSW is 1011100b = 5Ch.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the ASIC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge has been returned (SAK), an 8-bit subaddress is transmitted (SUB). The IF_ADD_INC bit in CTRL_REG2 (11h) enables subaddress auto increment (IF_ADD_INC is 1 by default), so if IF_ADD_INC = 1 the SUB (subaddress) is automatically increased to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the master transmits to the slave with direction unchanged. Table 14 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 14. **SAD+read/write patterns**

Command	SAD[6:0]	R/W	SAD + R/W
Read	1011100	1	10111001 (B9h)
Write	1011100	0	10111000 (B8h)

Table 15. **Transfer when master is writing one byte to slave**

Master	ST	SAD+ W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 16. **Transfer when master is writing multiple bytes to slave**

Master	ST	SAD+ W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 17. **Transfer when master is receiving (reading) one byte of data from slave**

Master	ST	SAD+ W		SUB		SR	SAD+ R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 18. **Transfer when master is receiving (reading) multiple bytes of data from slave**

Master	ST	SAD+ W		SUB		SR	SAD+ R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a slave receiver does not acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function), the data line must be kept high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

8.3 MIPI I3C^{SM} slave interface

The ILPS28QSW interface includes an MIPI I3C^{SM} SDR only slave interface (compliant with release 1.1 of the specification) with MIPI I3C^{SM} SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- In-band interrupt request
- Slave reset pattern
- Group address
- Asynchronous modes 0 and 1
- Synchronous mode
- Error detection and recovery methods (S0-S6)

8.3.1 MIPI I3C^{SM} CCC supported commands

The list of MIPI I3C^{SM} CCC commands supported by the device is detailed in the following table.

Table 19. MIPI I3C^{SM} CCC commands

Command	Command code	Default	Description
ENTDAA	0x07		DAA procedure
SETDASA	0x87		Assign dynamic address using static address 0x5C
ENEC	0x80 / 0x00		Slave activity control (direct and broadcast)
DISEC	0x81/ 0x01		Slave activity control (direct and broadcast)
ENTAS0	0x82 / 0x02		Enter activity state (direct and broadcast)
SETXTIME	0x98 / 0x28		Timing information exchange
GETXTIME	0x99	0x07 0x00 0x0C 0x92	Timing information exchange
RSTDAA	0x06		Reset the assigned dynamic address (broadcast only)
SETMWL	0x89 / 0x08		Define maximum write length during private write (direct and broadcast)
SETMRL	0x8A / 0x09		Define maximum read length during private read (direct and broadcast)
SETNEWDA	0x88		Change dynamic address
GETMWL	0x8B	0x00 0x08 (2 byte)	Get maximum write length during private write
GETMRL	0x8C	0x00 0x10 0x05 (3 byte)	Get maximum read length during private read
GETPID	0x8D	0x02 0x08 0x00	

Command	Command code	Default	Description
		0xB4 0x10 0x0B	
GETBCR	0x8E	0x07 (1 byte)	Bus characteristics register
GETDCR	0x8F	0x62 default	MIPI I3C^{SM} device characteristics register
GETSTATUS	0x90	0x00 0x00 (2 byte)	Status register
GETMXDS	0x94	0x08 0x60	Return maximum write and read speed
GETCAPS	0x95	0x00 0x11 0x18 0x00	Provide information about device capabilities and supported extended features
SETGRPA	0x9B		Group address assignment command
RSTGRPA	0x2C/0x9C		Reset the group address
RSTACT	0x9A/0x2A		Configure slave reset action

8.3.2 Overview of anti-spike filter management

The device acts as a standard I²C target as long as it has an I²C static address. The device is capable of detecting and disabling the I²C anti-spike filter after detecting the broadcast address (7'h7E/W). In order to guarantee proper behavior of the device, the I3C master must emit the first START, 7'h7E/W at open-drain speed using I²C fast mode plus reference timing.

After detecting the broadcast address, the device can receive the I3C dynamic address following the I3C push-pull timing. If the device is not assigned a dynamic address, then the device continues to operate as an I²C device with no anti-spike filter. For the case in which the host decides to keep the device as I²C with anti-spike filter, there is a configuration required to keep the anti-spike filter active. This configuration is done by writing the ASF_ON bit to 1 in the I3C_IF_CTRL (19h) register. This configuration forces the anti-spike filter to always be turned on instead of being managed by the communication on the bus.

9 Register mapping

The following table provides a quick overview of the 8-bit registers embedded in the device.

Table 20. Registers address map

Name	Type	Register address	Default	Function and comment
		Hex	Hex	
Reserved	-	00 – 0A	-	Reserved
INTERRUPT_CFG	R/W	0B	00h	Interrupt register
THS_P_L	R/W	0C	00h	Pressure threshold registers
THS_P_H	R/W	0D	00h	
IF_CTRL	R/W	0E	00h	Interface control register
WHO_AM_I	R	0F	B4h	Who am I
CTRL_REG1	R/W	10	00h	Control registers
CTRL_REG2	R/W	11	00h	
CTRL_REG3	R/W	12	01h	
Reserved	-	13	-	Reserved
FIFO_CTRL	R/W	14	00h	FIFO configuration registers
FIFO_WTM	R/W	15	00h	
REF_P_L	R	16	00h	Reference pressure registers
REF_P_H	R	17	00h	
Reserved	-	18	-	Reserved
I3C_IF_CTRL	R/W	19	80h	Interface configuration register
RPDS_L	R/W	1A	00h	Pressure offset registers
RPDS_H	R/W	1B	00h	
Reserved	-	1C-23	-	Reserved
INT_SOURCE	R	24	Output	Interrupt register
FIFO_STATUS1	R	25	Output	FIFO status registers
FIFO_STATUS2	R	26	Output	
STATUS	R	27	Output	Status register
PRESSURE_OUT_XL	R	28	Output	Pressure output registers Qvar output registers
PRESSURE_OUT_L	R	29	Output	
PRESSURE_OUT_H	R	2A	Output	
TEMP_OUT_L	R	2B	Output	Temperature output registers
TEMP_OUT_H	R	2C	Output	
Reserved	-	2D - 77	-	Reserved
FIFO_DATA_OUT_PRESS_XL	R	78	Output	FIFO pressure output registers FIFO Qvar output registers
FIFO_DATA_OUT_PRESS_L	R	79	Output	
FIFO_DATA_OUT_PRESS_H	R	7A	Output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee the proper behavior of the device, all register addresses not listed in the above table must not be accessed and the content stored in those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

10 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

10.1 INTERRUPT_CFG (0Bh)

Interrupt mode for pressure acquisition configuration (R/W)

7	6	5	4	3	2	1	0
AUTOREFP	RESET_ARP	AUTOZERO	RESET_AZ	-	LIR	PLE	PHE

AUTOREFP	Enable AUTOREFP function. Default value: 0 (0: normal mode; 1: AUTOREFP enabled)
RESET_ARP	Reset AUTOREFP function. Default value: 0 (0: normal mode; 1: reset AUTOREFP function)
AUTOZERO	Enable AUTOZERO function. Default value: 0 (0: normal mode; 1: AUTOZERO enabled)
RESET_AZ	Reset AUTOZERO function. Default value: 0 (0: normal mode; 1: reset AUTOZERO function)
LIR	Latch interrupt request to the INT_SOURCE (24h) register. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
PLE	Enable interrupt generation on pressure low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on pressure value lower than preset threshold)
PHE	Enable interrupt generation on pressure high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on pressure value higher than preset threshold)

Referring to Figure 17. “Threshold-based” interrupt event, the ILPS28QSW can be set by the user to support the interrupt function when P_DIFF_IN (defined below) is higher or lower than the threshold value stored in THS_P_L (0Ch) and THS_P_H (0Dh).

It is enabled when either the PHE bit or PLE bit (or both bits) is set to 1. Then, the differential pressure can be compared to a user-defined threshold stored in the 15-bit THS_P (0Ch and 0Dh) registers.

The threshold pressure value defined by the user is a 15-bit unsigned value in a 16-bit register composed of THS_P_L (0Ch) and THS_P_H (0Dh). The value is:

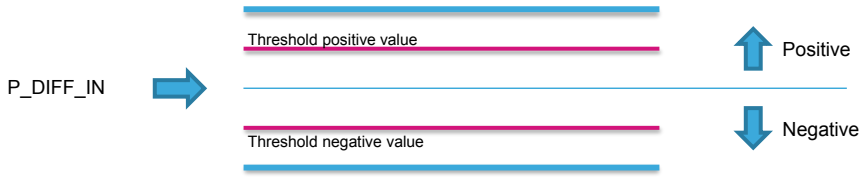
THS_P (15-bit unsigned) = desired interrupt threshold (hPa) x 16 for full-scale mode 1 (up to 1260 hPa)

THS_P (15-bit unsigned) = desired interrupt threshold (hPa) x 8 for full-scale mode 2 (up to 4060 hPa)

The PHE and PLE bits in INTERRUPT_CFG (0Bh) enable the differential pressure interrupt generation on the positive or negative event respectively.

The differential interrupt must be used with AUTOREFP or AUTOZERO mode.

Figure 17. **"Threshold-based" interrupt event**



To enable the **AUTOZERO** mode, the AUTOZERO bit must be set to 1 and then the measured pressure value is used as the reference and stored in the register REF_P (REF_P_L (16h), REF_P_H (17h)). From this point on, the output pressure value (PRESS_OUT_XL (28h), PRESS_OUT_L (29h), PRESS_OUT_H (2Ah)) is updated with the difference between the measured pressure and REF_P.

- P_DIFF_IN = measured pressure - REF_P
- PRESS_OUT = measured pressure - REF_P

After the first conversion, the AUTOZERO bit is automatically set back to 0. In order to return back to normal mode, the RESET_AZ bit in the INTERRUPT_CFG (0Bh) register has to be set to 1. This also resets the content of the REF_P registers to 0.

AUTOREFP mode allows using the pressure differential for the generation of the interrupt keeping the output pressure registers PRESS_OUT (PRESS_OUT_XL (28h), PRESS_OUT_L (29h), PRESS_OUT_H (2Ah)) without comparing REF_P. If the AUTOREFP bit is set to 1, the measured output pressure is used as the reference in the register REF_P (REF_P_L (16h), REF_P_H (17h)) for interrupt generation with the following:

- P_DIFF_IN = measured pressure - REF_P

The output registers PRESS_OUT (28h, 29h, and 2Ah) are not changed by REF_P and shows as follows.

- PRESS_OUT = measured pressure

After the first conversion, the AUTOREFP bit is automatically set to 0. In order to return back to normal mode, the RESET_ARP bit has to be set to 1.

10.2 THS_P_L (0Ch)

User-defined threshold value for pressure interrupt event (least significant bits) (R/W)

7	6	5	4	3	2	1	0
THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

THS[7:0]	This register contains the low part of threshold value for pressure interrupt generation. Default value: 00h

The threshold value for pressure interrupt generation is a 15-bit unsigned right-justified value composed of THS_P_H (0Dh) and THS_P_L (0Ch). The value is expressed as:

THS_P (15-bit unsigned) = desired interrupt threshold (hPa) x 16 for full-scale mode 1 (up to 1260 hPa)

THS_P (15-bit unsigned) = desired interrupt threshold (hPa) x 8 for full-scale mode 2 (up to 4060 hPa)

To enable the interrupt event based on this user-defined threshold, the PHE bit or PLE bit (or both bits) in INTERRUPT_CFG (0Bh) has to be enabled.

10.3 THS_P_H (0Dh)

User-defined threshold value for pressure interrupt event (Most significant bits) (R/W)

7	6	5	4	3	2	1	0
-	THS14	THS13	THS12	THS11	THS10	THS9	THS8

THS[14:8]	This register contains the high part of threshold value for pressure interrupt generation. Default value: 00h Refer to THS_P_L (0Ch).

10.4 IF_CTRL (0Eh)

Interface control register (R/W)

7	6	5	4	3	2	1	0
0	0	0	SDA_PU_EN	0	0	-	-

SDA_PU_EN	Enable pull-up on the SDA pin. Default value: 0 (0: SDA pin pull-up disconnected; 1: SDA pin with pull-up)

10.5 WHO_AM_I (0Fh)

Device Who am I

7	6	5	4	3	2	1	0
1	0	1	1	0	1	0	0

10.6 CTRL_REG1 (10h)

Control register 1 (R/W)

7	6	5	4	3	2	1	0
0	ODR3	ODR2	ODR1	ODR0	AVG2	AVG1	AVG0

ODR[3:0]	Output data rate selection. Default value: 0000 Refer to Table 21.
AVG[2:0]	Average selection. Default value: 000 Refer to Table 22.

Table 21. Output data rate bit configurations

ODR[3:0]	ODR of pressure, temperature, and Qvar
0000	Power-down / one-shot
0001	1 Hz
0010	4 Hz
0011	10 Hz
0100	25 Hz
0101	50 Hz
0110	75 Hz
0111	100 Hz
1000	200 Hz

Table 22. Averaging selection

AVG[2:0]	Averaging of pressure, temperature, and Qvar
000	4
001	8
010	16
011	32
100	64
101	128
111	512

The power consumption of the ILPS28QSW mainly depends on the selected ODR (output data rate) and on the selected resolution. The user can select the desired ODR and the oversampling frequency for pressure measurements in the CTRL_REG1 (10h) register. The ODR[3:0] bits are dedicated to the ODR selection, while the AVG[2:0] bits are used to configure the resolution.

The following table summarizes the current consumption of all the ASIC resolution modes.

Table 23. Power consumption for pressure acquistion (when AH and Qvar are disabled)

AVG	One-shot mode		Continuous mode – current consumption (µA) vs. ODR							
	Current consumption (µA) @ 1 Hz	ODR Max	1 Hz	4 Hz	10 Hz	25 Hz	50 Hz	75 Hz	100 Hz	200 Hz
512	32.2	25	32.8	126.8	314.4	783.8	-	-	-	-
128	9.4	75	10	35.6	86.7	214.3	427	639.8	-	-
64	5.6	100	6.3	20.4	48.7	119.4	237.2	355	472.8	-
32	3.7	200	4.4	12.8	29.8	71.9	142.2	212.6	282.9	564.4
16	2.7	300	3.5	9	20.2	48.2	94.8	141.4	188	374
8	2	400	2.7	6	12.6	29.1	56.5	84.2	111.5	221.7
4	1.7	500	2.5	5	10.2	23.2	44.7	66.2	87.8	174

Table 24. Power consumption for Qvar acquisition

AVG	One-shot mode		Continuous mode – current consumption (µA) vs. ODR							
	Current consumption (µA) @ 1 Hz	ODR max	1 Hz	4 Hz	10 Hz	25 Hz	50 Hz	75 Hz	100 Hz	200 Hz
512	21.9	25	22.6	76.4	184.5	458.6	-	-	-	-
128	8.6	75	9.3	24.1	53.9	128.4	253.4	379	-	-
64	6.5	100	7.2	15.4	32.1	73.6	143.2	213.1	283.1	-
32	5.4	200	6.1	11.1	21.3	46.5	88.6	131	173.4	343.4
16	4.8	300	5.5	8.9	15.7	32.8	61.4	90	118.7	233.4
8	4.3	400	5	6.9	10.7	20	35.8	51.4	67.1	130.2
4	4.2	500	4.9	6.4	9.3	16.6	28.9	41.2	53.5	102.7

The noise performance of ILPS28QSW is also defined as depending on the ODR and selected resolution and its performance is a trade-off between the power consumption and resolution. The noise performance is indicated in the following table.

Table 25. Noise performance

AVG	FS = 1260 hPa			FS = 4060 hPa		
	Pressure noise (Pa_{rms})			Pressure noise (Pa_{rms})		
	ODR/2	ODR/4	ODR/9	ODR/2	ODR/4	ODR/9
512	0.56	0.42	0.32	1.15	0.76	0.57
128	0.86	0.63	0.46	2.03	1.43	1.02
64	1.14	0.83	0.58	2.77	1.95	1.44
32	1.50	1.10	0.80	3.78	2.77	1.98
16	2.10	1.54	1.03	5.35	3.84	2.81
8	2.88	2.05	1.45	7.44	5.27	3.84
4	3.80	2.76	1.95	10.23	7.33	5.28

When the ODR bits are set to 0000, the device is in **power-down mode**. When the device is in power-down mode, almost all internal blocks of the device are switched off to minimize power consumption. The digital interface is still active to allow communication with the device. The content of the configuration registers is preserved and output data registers are not updated, therefore keeping the last data sampled in memory before going into power-down mode.

If the ONESHOT bit in CTRL_REG2 (11h) is set to 1, **one-shot mode** is triggered and a new acquisition starts when it is required. Enabling this mode is possible only if the device was previously in power-down mode (ODR bits set to 0000). Once the acquisition is completed and the output registers updated, the device automatically enters in power-down mode. The ONESHOT bit self-clears itself.

When the ODR bits are set to a value different than 0000, the device is in **continuous mode** and automatically acquires a set of data (pressure and temperature) at the frequency selected through the ODR[3:0] bits.

10.7 CTRL_REG2 (11h)

Control register 2 (R/W)

7	6	5	4	3	2	1	0
BOOT	FS_MODE	LFPF_CFG	EN_LPFP	BDU	SWRESET	-	ONESHOT

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FS_MODE	Full-scale selection. Default value: 0 (0: mode 1, full scale up to 1260 hPa; 1: mode 2, full scale up to 4060 hPa)
LFPF_CFG	Low-pass filter configuration. Default value: 0 (0: ODR/4; 1: ODR/9)
EN_LPFP	Enable low-pass filter on pressure data. Default value: 0 (0: disable, 1: enable)
BDU(1)	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
SWRESET	Software reset. Default value: 0 (0: normal mode; 1: software reset). The bit is self-cleared when the reset is completed.
ONESHOT	Enable one-shot mode. Default value: 0 (0: idle mode; 1: a new dataset is acquired)

1. *To guarantee the correct behavior of the BDU feature, PRESS_OUT_H (2Ah) must be the last address read.*

The BOOT bit is used to refresh the content of the internal registers stored in the non-volatile memory block. At device power-up, the content of the non-volatile memory block is transferred to the internal registers related to the trimming functions to allow correct behavior of the device itself. If for any reason the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to 1, the content of the internal non-volatile memory block is copied into the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and they are different for every device. They allow the correct behavior of the device and normally they should not be changed. At the end of the boot process, the BOOT bit is set again to 0 by hardware. The BOOT bit takes effect immediately after it is set to 1.

The SWRESET bit resets the volatile registers to the default value. It returns to 0 by hardware.

The ONESHOT bit is used to start a new conversion when the ODR[3:0] bits in CTRL_REG1 (10h) are set to 0000. Writing a 1 to ONESHOT triggers a single measurement of pressure and temperature. Once the measurement is done, the ONESHOT bit self-clears, the new data are available in the output registers, and the STATUS (27h) bits are updated.

10.8 CTRL_REG3 (12h)

Control register 3 (R/W)

7	6	5	4	3	2	1	0
AH_QVAR_EN	0	AH_QVAR_P_AUTO_EN	0	0	0	0	IF_ADD_INC

AH_QVAR_EN	Enables AH (analog hub) / Qvar functions. Default : 0 (0: disable; 1: enable)
AH_QVAR_P_AUTO_EN	Enables interleaved hardware mode for AH/Qvar and pressure data. Default : 0 (0: disable; 1: enable)
IF_ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I²C or I3C). Default value: 1 (0: disable, 1: enable)

The IF_ADD_INC bit enables the address to be automatically incremented during a multiple byte access with a serial interface (I²C or I3C).

The AH_QVAR_EN bit enables the AH (analog hub) and Qvar functions. The network of external connections and electrodes must be designed in the final application if these functions need to be enabled. Refer to Figure 15. AH (analog hub) / Qvar external connections to pin 2, pin 4.

The AH_QVAR_P_AUTO_EN bit enables the interleaved hardware mode: the device alternately generates pressure data and AH / Qvar data. Before enabling this mode, the device must be configured in power-down mode and the AH_QVAR_EN bit must be set to 0. This mode applies to both continuous and one-shot mode. The least significant bit of the output data registers is set to 0 for pressure data and to 1 for AH/Qvar data.

For further information, refer to application note AN5778.

10.9 FIFO_CTRL (14h)

FIFO control register (R/W)

7	6	5	4	3	2	1	0
0	0	0	AH_QVAR_P_FIFO_EN	STOP_ON_WTM	TRIG_MODES	F_MODE1	F_MODE0

AH_QVAR_P_FIFO_EN	Enables hardware interleaved mode for AH/Qvar and pressure data in FIFO buffer. Default : 0 (0: disable; 1: enable)
STOP_ON_WTM	Stop-on-FIFO watermark. Enables use of FIFO watermark level. Default value: 0 (0: disable; 1: enable)
TRIG_MODES	Enables triggered FIFO modes. Default value: 0
F_MODE[1:0]	Selects triggered FIFO modes. Default value: 00 Refer to Table 26.

The AH_QVAR_P_FIFO_EN bit enables the hardware interleaved mode in FIFO: the pressure data and the AH/Qvar data are alternately stored in FIFO. Before enabling this mode, the device must be configured in power-down mode and the AH_QVAR_EN bit must be set to 0. When the hardware interleaved mode in FIFO is intended to be used, both the AH_QVAR_P_AUTO_EN in CTRL_REG3 (12h) register and the AH_QVAR_P_FIFO_EN bit have to be set to 1. The least significant bit of the output data registers is set to 0 for pressure data and to 1 for AH/Qvar data.

Table 26. FIFO mode selection

TRIG_MODES	F_MODE[1:0]	Mode
x	00	Bypass
0	01	FIFO mode
0	1x	Continuous (dynamic-stream)
1	01	Bypass-to-FIFO
1	10	Bypass-to-continuous (dynamic-stream)
1	11	Continuous (dynamic-stream)-to-FIFO

The STOP_ON_WTM bit enables the use of the FIFO watermark level: when the number of samples in FIFO is equal to the watermark level (set using the WTM[6:0] bits in FIFO_WTM (15h)) then FIFO is full.

The TRIG_MODES bit enables the triggered FIFO modes.

The F_MODE[1:0] bits select one of the FIFO modes, as described in Table 26.

Output pressure data are read through FIFO_DATA_OUT_PRESS_XL (78h), FIFO_DATA_OUT_PRESS_L (79h) and FIFO_DATA_OUT_PRESS_H (7Ah); both single read and multiple read operations can be used.

10.10 FIFO_WTM (15h)

FIFO threshold setting register (R/W)

7	6	5	4	3	2	1	0
0	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

WTM[6:0]	FIFO threshold. Watermark level setting. Default value: 0000000

10.11 REF_P_L (16h)

Reference pressure LSB data (R)

7	6	5	4	3	2	1	0
REFP7	REFP6	REFP5	REFP4	REFP3	REFP2	REFP1	REFP0

REFP[7:0]	This register contains the low part of the reference pressure value. Default value: 00000000

The reference pressure value is 16-bit data and it is composed of REF_P_H (17h) and REF_P_L (16h). The value is expressed as two's complement.

The reference pressure value is stored and used when the AUTOZERO or AUTOREFP function is enabled, refer to the INTERRUPT_CFG (0Bh) register description.

10.12 REF_P_H (17h)

Reference pressure MSB data (R)

7	6	5	4	3	2	1	0
REFP15	REFP14	REFP13	REFP12	REFP11	REFP10	REFP9	REFP8

REFP[15:8]	This register contains the high part of the reference pressure value. Default value: 00000000

10.13 I3C_IF_CTRL (19h)

Control register (R/W)

7	6	5	4	3	2	1	0
1	0	ASF_ON	0	0	0	I3C_Bus_Avb_Sel1	I3C_Bus_Avb_Sel0

ASF_ON	Enables anti-spike filters. Default value: 0 (0: anti-spike filters are managed by protocol and turned off after the broadcast address; 1: anti-spike filters on SCL and SDA lines are always enabled)
I3C_Bus_Avb_Sel[1:0]	These bits are used to select the bus available time when I3C IBI is used. Default value: 00 (00: bus available time equal to 50 µsec; 01: bus available time equal to 2 µsec; 10: bus available time equal to 1 msec; 11: bus available time equal to 25 msec)

10.14 RPDS_L (1Ah)

Pressure offset (LSB data)

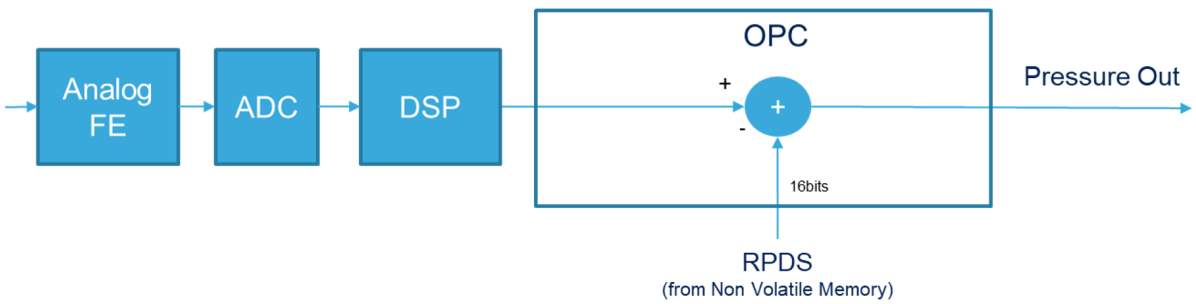
7	6	5	4	3	2	1	0
RPDS7	RPDS6	RPDS5	RPDS4	RPDS3	RPDS2	RPDS1	RPDS0

RPDS[7:0]	This register contains the low part of the pressure offset value. Default value: 00000000

The pressure offset value is 16-bit data that can be used to implement one-point calibration (OPC) after soldering. This value is composed of RPDS_H (1Bh) and RPDS_L (1Ah). The value is expressed as two's complement.

The customer can perform a one-point calibration after soldering (recommended) and the offset coefficient can be stored for OPC in register RPDS (1Ah, 1Bh). These stored offset values are directly added to the compensated pressure data in the block diagram below. To give better flexibility to the user, the OPC value can be written twice in the same register map. For further details, refer to the application note.

Figure 18. One-point calibration



10.15 RPDS_H (1Bh)

Pressure offset (MSB data)

7	6	5	4	3	2	1	0
RPDS15	RPDS14	RPDS13	RPDS12	RPDS11	RPDS10	RPDS9	RPDS8

RPDS[15:8]	This register contains the high part of the pressure offset value. Default value: 00000000

10.16 INT_SOURCE (24h)

Interrupt source (read only) register for differential pressure. A read at this address clears the INT_SOURCE register itself.

7	6	5	4	3	2	1	0
BOOT_ON	0	0	0	0	IA	PL	PH

BOOT_ON	Indication that Boot (reboot) phase is running. (0: boot phase not running; 1: boot phase is running)
IA	Interrupt active. (0: no interrupt has been generated; 1: one or more interrupt events have been generated).
PL	Differential pressure Low. (0: no interrupt has been generated; 1: low differential pressure event has occurred).
PH	Differential pressure High. (0: no interrupt has been generated; 1: high differential pressure event has occurred).

10.17 FIFO_STATUS1 (25h)

FIFO status register (read only)

7	6	5	4	3	2	1	0
FSS7	FSS6	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

FSS[7:0]	FIFO stored data level, number of unread samples stored in FIFO. (00000000: FIFO empty; 10000000: FIFO full, 128 unread samples)

10.18 FIFO_STATUS2 (26h)

FIFO status register (read only)

7	6	5	4	3	2	1	0
FIFO_WTM_IA	FIFO_OVR_IA	FIFO_FULL_IA	-	-	-	-	-

FIFO_WTM_IA	FIFO threshold (watermark) status. Default value: 0 (0: FIFO filling is lower than treshold level; 1: FIFO filling is equal or higher than the threshold level).
FIFO_OVR_IA	FIFO overrun status. Default value: 0 (0: FIFO is not completely full; 1: FIFO is full and at least one sample in the FIFO has been overwritten).
FIFO_FULL_IA	FIFO full status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled, no samples overwritten)

10.19 STATUS (27h)

Status register (read only)

7	6	5	4	3	2	1	0
-	-	T_OR	P_OR	-	-	T_DA	P_DA

T_OR	Temperature data overrun. (0: no overrun has occurred; 1: new data for temperature has overwritten the previous data)
P_OR	Pressure data overrun. (0: no overrun has occurred; 1: new data for pressure has overwritten the previous data)
T_DA	Temperature data available. (0: new data for temperature is not yet available; 1: new temperature data is generated)
P_DA	Pressure data available. (0: new data for pressure is not yet available; 1: new pressure data is generated)

This register is updated every ODR cycle.

10.20 PRESS_OUT_XL (28h)

Either pressure output or AH/Qvar output value LSB data (read only)

7	6	5	4	3	2	1	0
POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0

POUT[7:0]	This register contains the low part of the pressure or AH/Qvar output value.

The pressure output value is a 24-bit data that contains the measured pressure. It is composed of PRESS_OUT_H (2Ah), PRESS_OUT_L (29h), and PRESS_OUT_XL (28h). The value is expressed as two's complement.

The output pressure register **PRESS_OUT** is provided as the difference between the measured pressure and the content of the register RPDS (18h, 19h).

This register contains the pressure value and the resolution is: 1 LSB = 1/4096 hPa (when FS_MODE = 0), otherwise 1 LSB = 1/2048 hPa (when FS_MODE = 1), refer to Section 5.5 Interpreting pressure readings for additional information.

10.21 PRESS_OUT_L (29h)

Either pressure output or AH/Qvar output value middle data (read only)

7	6	5	4	3	2	1	0
POUT15	POUT14	POUT13	POUT12	POUT11	POUT10	POUT9	POUT8

POUT[15:8]	This register contains the mid part of the pressure or AH/Qvar output value. Refer to PRESS_OUT_XL (28h)

10.22 PRESS_OUT_H (2Ah)

Either pressure output or AH/Qvar output value MSB data (read only)

7	6	5	4	3	2	1	0
POUT23	POUT22	POUT21	POUT20	POUT19	POUT18	POUT17	POUT16

POUT[23:16]	This register contains the high part of the pressure or AH/Qvar output value. Refer to PRESS_OUT_XL (28h)

10.23 TEMP_OUT_L (2Bh)

Temperature output value LSB data (read only)

7	6	5	4	3	2	1	0
TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

TOUT[7:0]	This register contains the low part of the temperature output value.

The temperature output value is 16-bit data that contains the measured temperature. It is composed of TEMP_OUT_H (2Ch), and TEMP_OUT_L (2Bh). The value is expressed as two's complement.

This register contains the temperature value and the resolution is: 1LSB = 0.01 °C.

10.24 TEMP_OUT_H (2Ch)

Temperature output value MSB data (read only)

7	6	5	4	3	2	1	0
TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

TOUT[15:8]	This register contains the high part of the temperature output value.

10.25 FIFO_DATA_OUT_PRESS_XL (78h)

Either FIFO pressure or AH/Qvar output LSB data (read only)

7	6	5	4	3	2	1	0
FIFO_P7	FIFO_P6	FIFO_P5	FIFO_P4	FIFO_P3	FIFO_P2	FIFO_P1	FIFO_P0

FIFO_P[7:0]	Pressure or AH/Qvar LSB data in FIFO buffer

10.26 FIFO_DATA_OUT_PRESS_L (79h)

Either FIFO pressure or AH/Qvar output middle data (read only)

7	6	5	4	3	2	1	0
FIFO_P15	FIFO_P14	FIFO_P13	FIFO_P12	FIFO_P11	FIFO_P10	FIFO_P9	FIFO_P8

FIFO_P[15:8]	Pressure or AH/Qvar middle data in FIFO buffer

10.27 FIFO_DATA_OUT_PRESS_H (7Ah)

Either FIFO pressure or AH/Qvar output MSB data (read only)

7	6	5	4	3	2	1	0
FIFO_P23	FIFO_P22	FIFO_P21	FIFO_P20	FIFO_P19	FIFO_P18	FIFO_P17	FIFO_P16

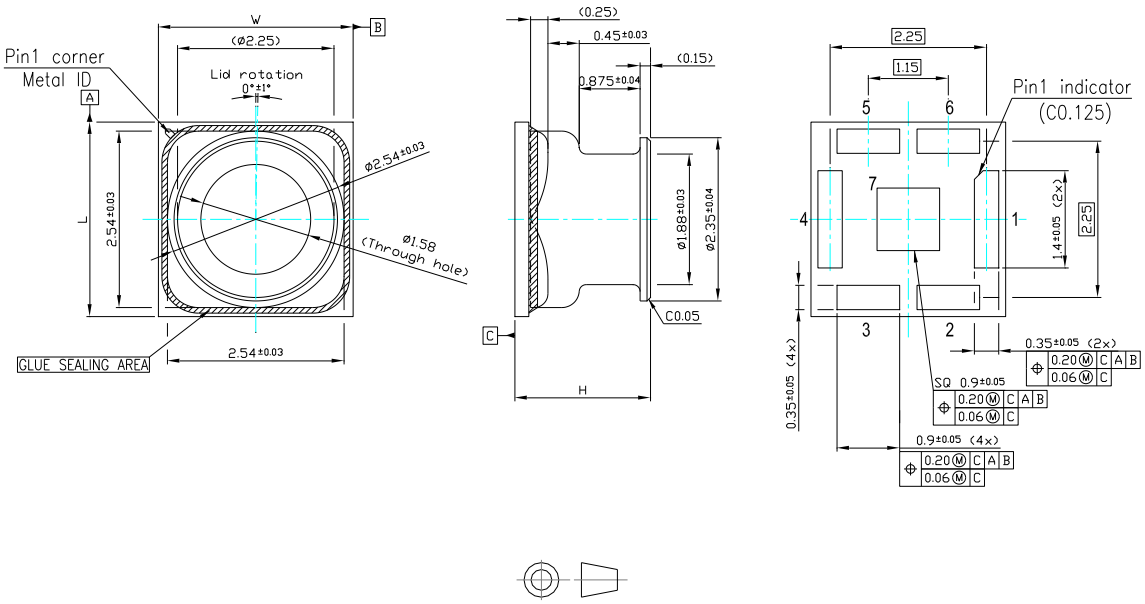
FIFO_P[23:16]	Pressure or AH/Qvar MSB data in FIFO buffer

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 CCLGA-7L package information

Figure 19. CCLGA-7L (2.8 x 2.8 x 1.95 mm typ.) package outline and mechanical dimensions



Dimensions arein millimeter unless otherwise specified
General Tolerance is +/ -0.10mm unless otherwise specified

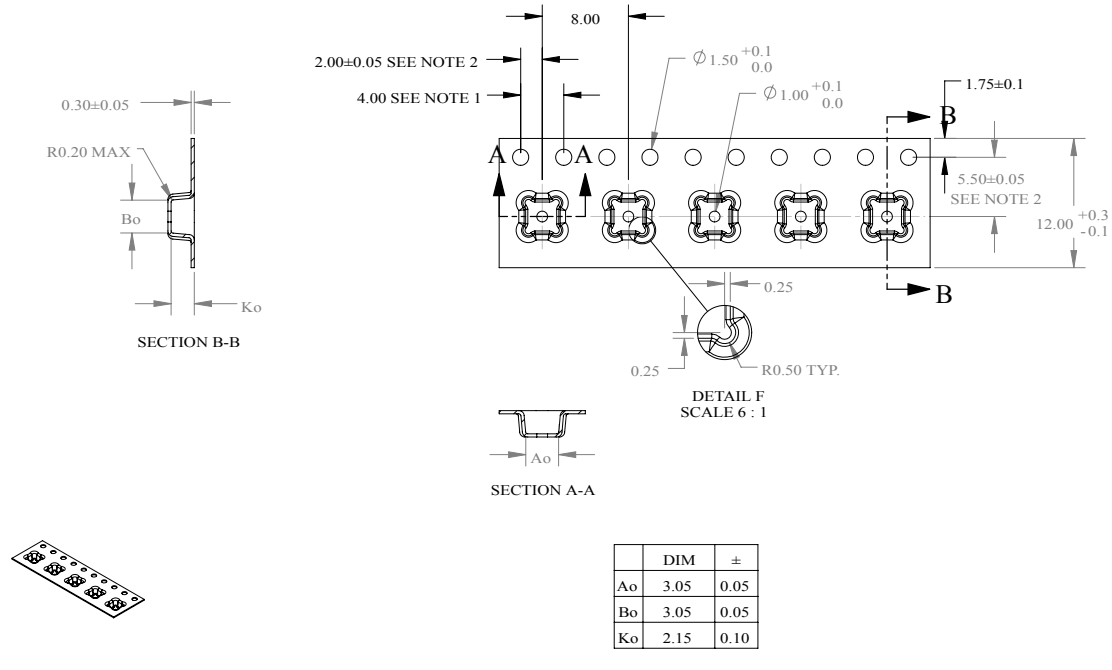
OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.8	±0.15
Width [W]	2.8	±0.15
Height [H]	2.1 MAX	/

DM00688938_2

11.2 CCLGA-7L packing information

Figure 20. **Carrier tape information for CCLGA-7L package**



	DIM	±
Ao	3.05	0.05
Bo	3.05	0.05
Ko	2.15	0.10

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 21. **CCLGA-7L package orientation in carrier tape**

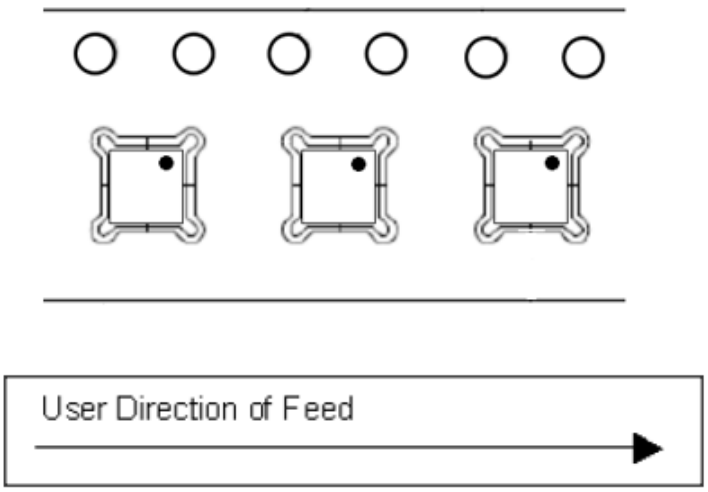


Figure 22. **Reel information for carrier tape of CCLGA-7L package**

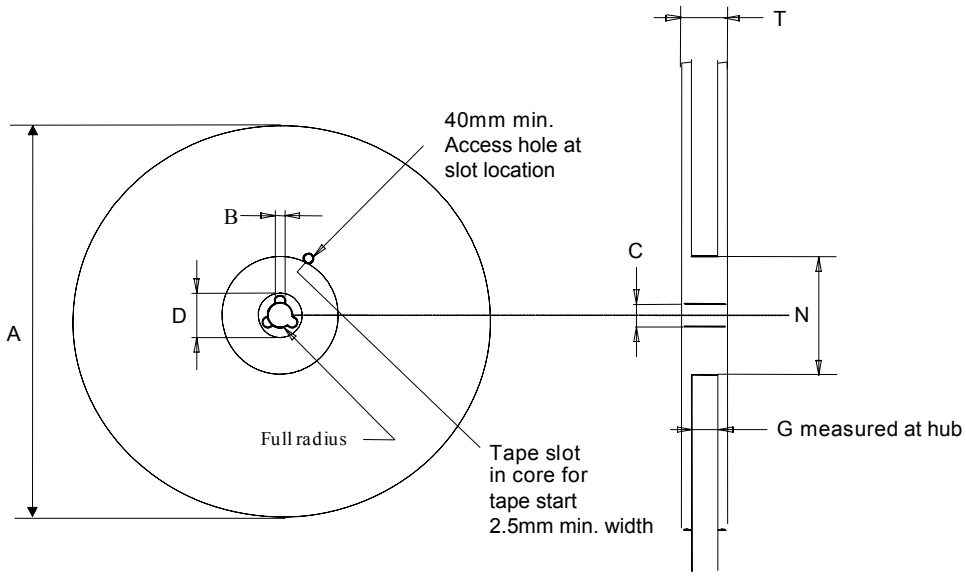


Table 27. **Reel dimensions for carrier tape of CCLGA-7L package**

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

Revision history

Table 28. **Document revision history**

Date	Version	Changes
17-Jan-2023	1	Initial release

Contents

List of tables

List of figures