# Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

## Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

# HD404374/HD404384/ HD404389/HD404082/HD404084 Series

Low-Voltage AS Microcomputers with On-Chip A/D Converter

ADE-202-086C (O)
Rev. 4.0
Feb. 2000

## Description

The HD404374, HD404384, and HD404389 Series comprise low-voltage, 4-bit single-chip microcomputers equipped with four 10-bit A/D converter channels, a serial interface, and large-current I/O pins. These devices are suitable for use in applications requiring high resolution A/D converter control, such as battery chargers.

The HD404082 and HD404084 series offer less advanced features than the HD404384 series. They are 4-bit microcomputers that support low-voltage operation for backward software compatibility.

HD404374 Series microcomputers have a 32.768 kHz sub-resonator for realtime clock use, providing a time counting facility, and a variety of low-power modes to reduce current drain.

The HD407A4374, HD407A4384, HD407A4389, HD407C4374, HD407C4384, and HD407C4389 are ZTAT™ microcomputers with on-chip PROM that drastically shortens development time and ensures a smooth transition from debugging to mass production. (The PROM programming specifications are the same as for the 27256 type.)

ZTAT™: Zero Turn-Around Time. ZTAT™ is a trademark of Hitachi, Ltd.

## Features

- 20 I/O pins
  Large-current I/O pins (source: 10 mA max.):4
  Large-current I/O pins (sink: 15 mA max.):4
  Analog input multiplexed pins: 4 (HD404374, HD404384, and HD404389 Series)
- 8-bit timer: 1 channel
  16-bit timer: 1 channel (Can also be used as two 8-bit timer channels)
- Two timer outputs (including PWM output)
- Event counter inputs (edge-programmable)
- Clock-synchronous 8-bit serial interface
- A/D converter
  4 channels × 10-bits (HD404374 and HD404384 Series)

6 channels × 10-bits (HD404389 Series)

None (HD404082 and HD404084 Series)

- On-chip oscillators
  - — HD404374 Series
    - Main clock (ceramic resonator, crystal resonator, CR oscillation* or external clock operation possible)
    - Sub-clock (32.768 kHz crystal resonator)
  - — HD404384, HD404389, HD404082, and HD404084 Series
    - Main clock (ceramic resonator, crystal resonator, CR oscillation* or external clock operation possible)

Note: CR oscillation in an optional function.

- Interrupts

  External: 2 (including one edge-programmable)

  Internal : 5 (HD404374/HD404384/HD404389 Series)

  : 4 (HD404082/HD404084 Series)
- Subroutine stack up to 16 levels, including interrupts
- Low-power dissipation modes
  - — HD404374 Series: 4
  - — HD404384, HD404389, HD404082, and HD404084 Series: 2
- Module standby (timers, serial interface, A/D converter)
- System clock division software switching (1/4 or 1/32)
- Inputs for return from stop mode (wakeup): 1
- Instruction execution time

  Min. 0.89 µs ($f_{OSC}$ = 4.5 MHz, division by 1/4)

  Min. 0.47 µs ($f_{OSC}$ = 8.5 MHz, division by 1/4)
- Operation voltage

  1.8 V to 5.5 V

  2.0 V to 5.5 V (ZTAT™)

## Cautions about operation!

- Electrical properties presented on the data sheet for the mask ROM and ZTAT™ versions will surely and sufficiently satisfy the standard values. However, real capabilities, operation margin, noise margin, and other properties may vary depending on differences of manufacturing processes, internal wiring patterns, etc. Therefore, it is requested for users to carry out an evaluation test for each product on an actual system under the same conditions to see its operation.
- After power supply has been connected, the values for the memory register, data and stack areas will be undefined. Initialize prior to use.

## Ordering Information

### HD404374 Series

| Type | Product Name | Model Name | ROM (Words) | RAM (Digits) | Package |
|---|---|---|---|---|---|
| Mask ROM | HD404372 | HD404372FT | 2,048 | 512 | 30-pin plastic SSOP(FP-30D) |
| | | HD404372H | | | 48-pin plastic LQFP(FP-48B) *1 |
| | HD40A4372 | HD40A4372FT | | | 30-pin plastic SSOP(FP-30D) |
| | | HD40A4372H | | | 48-pin plastic LQFP(FP-48B) *1 |
| | HD40C4372 | HD40C4372FT | | | 30-pin plastic SSOP(FP-30D) |
| | | HD40C4372H | | | 48-pin plastic LQFP(FP-48B) *1 |
| | HD404374 | HD404374FT | 4,096 | | 30-pin plastic SSOP(FP-30D) |
| | | HD404374H | | | 48-pin plastic LQFP(FP-48B) *1 |
| | HD40A4374 | HD40A4374FT | | | 30-pin plastic SSOP(FP-30D) |
| | | HD40A4374H | | | 48-pin plastic LQFP(FP-48B) *1 |
| | HD40C4374 | HD40C4374FT | | | 30-pin plastic SSOP(FP-30D) |
| | | HD40C4374H | | | 48-pin plastic LQFP(FP-48B) *1 |
| ZTAT™ | HD407A4374 | HD407A4374FT | 4,096 | | 30-pin plastic SSOP (FP-30D) |
| | HD407C4374 | HD407C4374FT | | | 30-pin plastic SSOP(FP-30D) |

**HD404384 Series**

| Type | Product Name | Model Name | ROM (Words) | RAM (Digits) | Package |
|---|---|---|---|---|---|
| Mask ROM | HD404382 | HD404382FT | 2,048 | 512 | 30-pin plastic SSOP (FP-30D) |
| | | HD404382S | | | 28-pin plastic DILP (DP-28S) |
| | | HD404382H | | | 48-pin plastic LQFP (FP-48B)[*1] |
| | HD40A4382 | HD40A4382FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40A4382S | | | 28-pin plastic DILP (DP-28S) |
| | | HD40A4382H | | | 48-pin plastic LQFP (FP-48B)[*1] |
| | HD40C4382 | HD40C4382FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40C4382S | | | 28-pin plastic DILP (DP-28S) |
| | | HD40C4382H | | | 48-pin plastic LQFP (FP-48B)[*1] |
| | HD404384 | HD404384FT | 4,096 | | 30-pin plastic SSOP (FP-30D) |
| | | HD404384S | | | 28-pin plastic DILP (DP-28S) |
| | | HD404384H | | | 48-pin plastic LQFP (FP-48B)[*1] |
| | HD40A4384 | HD40A4384FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40A4384S | | | 28-pin plastic DILP (DP-28S) |
| | | HD40A4384H | | | 48-pin plastic LQFP (FP-48B)[*1] |
| | HD40C4384 | HD40C4384FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40C4384S | | | 28-pin plastic DILP (DP-28S) |
| | | HD40C4384H | | | 48-pin plastic LQFP (FP-48B)[*1] |
| ZTAT™ | HD407A4384 | HD407A4384FT | 4,096 | | 30-pin plastic SSOP (FP-30D) |
| | | HD407A4384S | | | 28-pin plastic DILP (DP-28S) |
| | HD407C4384 | HD407C4384FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD407C4384S | | | 28-pin plastic DILP (DP-28S) |

**HD404389 Series**

| Type | Product Name | Model Name | ROM (Words) | RAM (Digits) | Package |
|---|---|---|---|---|---|
| Mask ROM | HD404388 | HD404388FT | 8,192 | 512 | 30-pin plastic SSOP (FP-30D) |
| | HD40A4388 | HD40A4388FT | | | |
| | HD40C4388 | HD40C4388FT | | | |
| | HD404389 | HD404389FT | 16,384 | | |
| | HD40A4389 | HD40A4389FT | | | |
| | HD40C4389 | HD40C4389FT | | | |
| ZTAT™ | HD407A4389 | HD407A4389FT | 16,384 | | |
| | HD407C4389 | HD407C4389FT | | | |

**HD404082 Series**

| Type | Product Name | Model Name | ROM (Words) | RAM (Digits) | Package |
|---|---|---|---|---|---|
| Mask ROM | HD404081 | HD404081FT | 1,024 | 128 | 30-pin plastic SSOP (FP-30D) |
| | | HD404081S | | | 28-pin plastic DILP (DP-28S) |
| | | HD404081H | | | 48-pin plastic LQFP (FP-48B)[*2] |
| | HD40A4081 | HD40A4081FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40A4081S | | | 28-pin plastic DILP (DP-28S) |
| | | HD40A4081H | | | 48-pin plastic LQFP (FP-48B)[*2] |
| | HD40C4081 | HD40C4081FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40C4081S | | | 28-pin plastic DILP (DP-28S) |
| | | HD40C4081H | | | 48-pin plastic LQFP (FP-48B)[*2] |
| | HD404082 | HD404082FT | 2,048 | | 30-pin plastic SSOP (FP-30D) |
| | | HD404082S | | | 28-pin plastic DILP (DP-28S) |
| | | HD404082H | | | 48-pin plastic LQFP (FP-48B)[*2] |
| | HCD404082 | HCD404082 | | | chip |
| | HD40A4082 | HD40A4082FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40A4082S | | | 28-pin plastic DILP (DP-28S) |
| | | HD40A4082H | | | 48-pin plastic LQFP (FP-48B)[*2] |
| | HD40C4082 | HD40C4082FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40C4082S | | | 28-pin plastic DILP (DP-28S) |
| | | HD40C4082H | | | 48-pin plastic LQFP (FP-48B)[*2] |
| | HCD40C4082 | HCD40C4082 | | | chip |
| ZTAT™ | Uses HD404384 series ZTAT™. | | | | |

Notes: 1. The FP-48B is subject to the following limitations:
(1) It is available in a mask ROM version only. For debugging, etc., the ZTAT™ version of a different package will need to be used.
(2) The WS version will become available at the beginning of mass production.
2. Currently in planning stage.

**HD404084 Series**

| Type | Product Name | Model Name | ROM (Words) | RAM (Digits) | Package |
|---|---|---|---|---|---|
| Mask ROM | HD404084 | HD404084FT | 4,096 | 256 | 30-pin plastic SSOP (FP-30D) |
| | | HD404084S | | | 28-pin plastic DILP (DP-28S) |
| | HCD404084 | HCD404084 | | | chip |
| | HD40A4084 | HD40A4084FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40A4084S | | | 28-pin plastic DILP (DP-28S) |
| | HD40C4084 | HD40C4084FT | | | 30-pin plastic SSOP (FP-30D) |
| | | HD40C4084S | | | 28-pin plastic DILP (DP-28S) |
| | HCD40C4084 | HCD40C4084 | | | chip |
| ZTAT™ | Uses HD404384 series ZTAT™ | | | | |

## List of Functions

| Product Name | | HD404372, HD40A4372, HD40C4372 | HD404374, HD40A4374, HD40C4374, HD407A4374, HD407C4374 | HD404382, HD40A4382, HD40C4382 | HD404384, HD40A4384, HD40C4384, HD407A4384, HD407C4384 | HD404388, HD40A4388, HD40C4388 |
|---|---|---|---|---|---|---|
| ROM(words) | | 2,048 | 4,096 ZTAT PROM | 2,048 | 4,096 ZTAT PROM | 8,192 |
| RAM (digit) | | 512 | | | | |
| I/O | | 20 (max) | | | | |
| | Large-current I/O pins | 4 (source, 10 mA max), 4 (sink, 15 mA max) | | | | |
| | Analog input multiplexed pins | 4 | | | | |
| Timer/ | | 3 | | | | |
| counter | Timer output | 2 (PWM output possible) | | | | |
| | Event input | 1 (edge selection possible) | | | | |
| Serial interface | | 1 (8-bit synchronous) | | | | |
| A/D converter | | 10 bits × 4 channels | | | | 10 bits × 6 channels |
| Interrupt | External | 2 | | | | |
| sources | Internal | 5 | | | | |
| Low-power | | 4 | | 2 | | |
| modes | Stop mode | Available | | | | |
| | Watch mode | Available | | — | | |
| | Standby mode | Available | | | | |
| | Subactive mode | Available | | — | | |
| Module standby | | Available | | | | |
| System clock division software switching | | Available | | | | |
| Main oscillator | Ceramic oscillation | Available | | | | |
| | Crystal oscillation | Available | | | | |
| | CR oscillation | Available (HD40C4372, HD40C4374, HD407C4374, HD40C4382, HD40C4384, HD407C4384, HD40C4388, HD40C4389, HD407C4389, HD40C4081, HD40C4082, HCD40C4082, HD40C4084, HCD40C4084) | | | | |
| Sub-oscillator | Crystal oscillation | Available (32.768kHz) | | — | | |

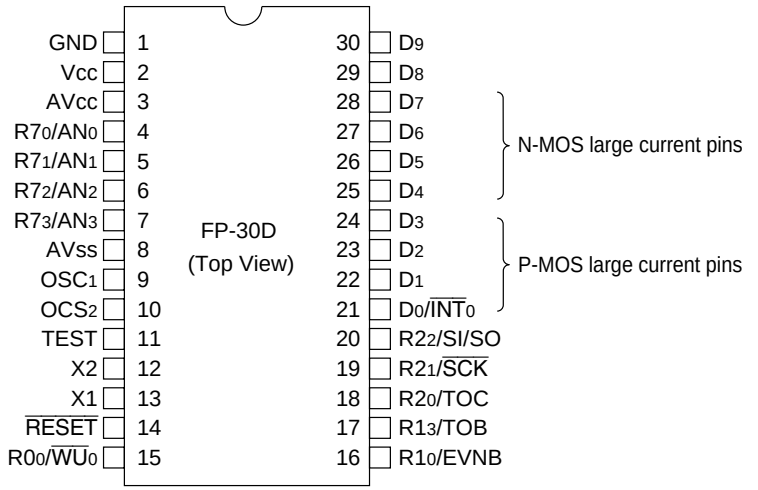
| Product Name | | HD404372, HD40A4372, HD40C4372 | HD404374, HD40A4374, HD40C4374, HD407A4374, HD407C4374 | HD404382, HD40A4382, HD40C4382 | HD404384, HD40A4384, HD40C4384, HD407A4384, HD407C4384 | HD404388, HD40A4388, HD40C4388 |
|---|---|---|---|---|---|---|
| Minimum instruction execution time | | 0.47 ms ($f_{OSC}$ = 8.5 MHz) : HD40A4372, HD40A4374, HD407A4374, HD40A4382, HD40A4384, HD407A4384, HD40A4388, HD40A4389, HD407A4389, HD40A4081, HD40A4082, HD40A4084<br>0.89 ms ($f_{OSC}$ = 4.5 MHz) : HD404372, HD404374, HD404382, HD404384, HD404388, HD404389, HD404081, HD404082, HCD404082, HD404084, HCD404084<br>1.14 ms ($f_{OSC}$ = 3.5 MHz) : HD40C4372, HD40C4374, HD407C4374, HD40C4382, HD40C4384, HD407C4384, HD40C4388, HD40C4389, HD407C4389, HD40C4081, HD40C4082, HCD40C4082, HD40C4084, HCD40C4084 | | | | |
| Operating voltage (V) | | 1.8 to 5.5 V : Mask ROM, 2.0 to 5.5 V : ZTATTM | | | | |
| Package | FP-30D | Available | | | | |
| | DP-28S | — | | Available | | — |
| | FP-48B | Available | | | | — |
| Chip | | — | | | | |
| Guaranteed operation temperature(°C) | | –20 to +75: Mask ROM<br>–40 to +85: ZTAT™ | | | | |

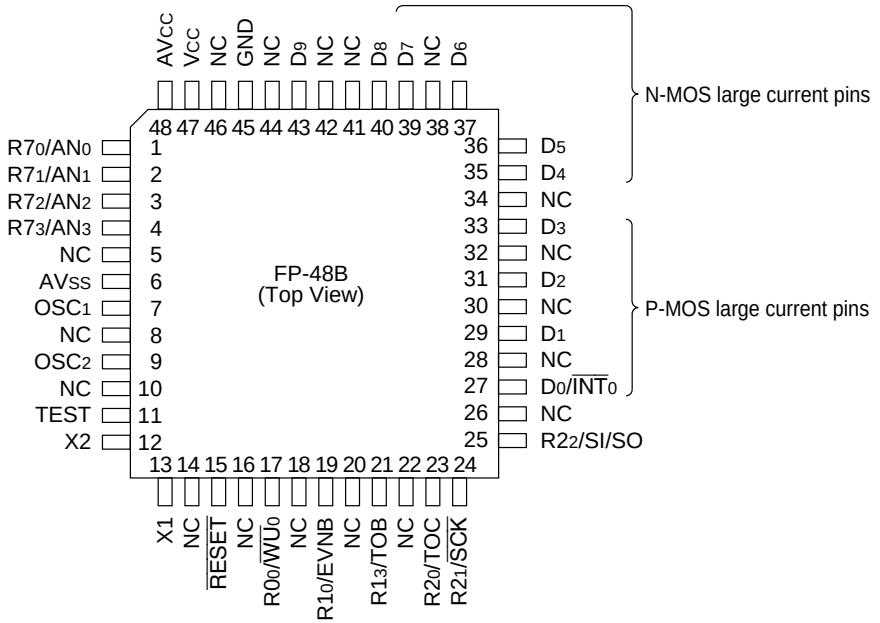
| Product Nme | | HD404389, HD40A4389, HD40C4389, HD407A4389, HD407C4389 | HD404081, HD40A4081, HD40C4081 | HD404082, HD40A4082, HD40C4082 | HCD404082, HCD40C4082 | HD404084, HD40A4084, HD40C4084 | HCD404084, HCD40C4084 |
|---|---|---|---|---|---|---|---|
| ROM(words) | | 16,384 ZTAT PROM | 1,024 | 2,048 | | 4,096 | |
| RAM (digit) | | 512 | 128 | | | | |
| I/O | | 20 (max) | | | | | |
| | Large-current I/O pins | 4 (source, 10 mA max), 4 (sink, 15 mA max) | | | | | |
| | Analog input multiplexed pins | 4 | — | | | | |
| Timer/ | | 3 | | | | | |
| counter | Timer output | 2 (PWM output possible) | | | | | |
| | Event input | 1 (edge selection possible) | | | | | |
| Serial interface | | 1 (8-bit synchronous) | | | | | |
| A/D converter | | 10 bits × 6 channels | — | | | | |
| Interrupt | External | 2 | | | | | |
| sources | Internal | 5 | 4 | | | | |
| Low-power | | 4 | | | | | |
| modes | Stop mode | Available | | | | | |
| | Watch mode | Available | | | | | |
| | Standby mode | Available | | | | | |
| | Subactive mode | Available | | | | | |
| Module standby | | Available | | | | | |
| System clock division software switching | | Available | | | | | |
| Main oscillator | Ceramic oscillation | Available | | | | | |
| | Crystal oscillation | Available | | | | | |
| | CR oscillation | Available (HD40C4372, HD40C4374, HD407C4374, HD40C4382, HD40C4384, HD407C4384, HD40C4388, HD40C4389, HD407C4389, HD40C4081, HD40C4082, HCD40C4082, HD40C4084, HCD40C4084) | | | | | |
| Sub-oscillator | Crystal oscillation | — | | | | | |

| Product Nme | | HD404389, HD40A4389, HD40C4389, HD407A4389, HD407C4389 | HD404081, HD40A4081, HD40C4081 | HD404082, HD40A4082, HD40C4082 | HCD40482, HCD40C4082 | HD404084, HD40A4084, HD40C4084 | HCD404084, HCD40C4084 |
|---|---|---|---|---|---|---|---|
| Minimum instruction execution time | | 0.47 µs ($f_{OSC}$ = 8.5 MHz) : HD40A4372, HD40A4374, HD407A4374, HD40A4382, HD40A4384, HD407A4384, HD40A4388, HD40A4389, HD407A4389, HD40A4081, HD40A4082, HD40A4084<br>0.89 µs ($f_{OSC}$ = 4.5 MHz) : HD404372, HD404374, HD404382, HD404384, HD404388, HD404389, HD404081, HD404082, HCD404082, HD404084, HCD404084<br>1.14 µs ($f_{OSC}$ = 3.5 MHz) : HD40C4372, HD40C4374, HD407C4374, HD40C4382, HD40C4384, HD407C4384, HD40C4388, HD40C4389, HD407C4389, HD40C4081, HD40C4082, HCD40C4082, HD40C4084, HCD40C4084 | | | | | |
| Operating voltage (V) | | 1.8 to 5.5 V : Mask ROM, 2.0 to 5.5 V : ZTAT™ | | | | | |
| Package | FP-30D | Available | | | | | |
| | DP-28S | — | Available | | — | Available | — |
| | FP-48B | — | In planning stage | | — | | |
| Chip | | — | | | Available | — | Available |
| Guaranteed operation temperature(°C) | | –20 to +75: Mask ROM<br>–40 to +85: ZTAT™ | | | +75 | –20 to +75: Mask ROM<br>–40 to +85: ZTAT™ | +75 |

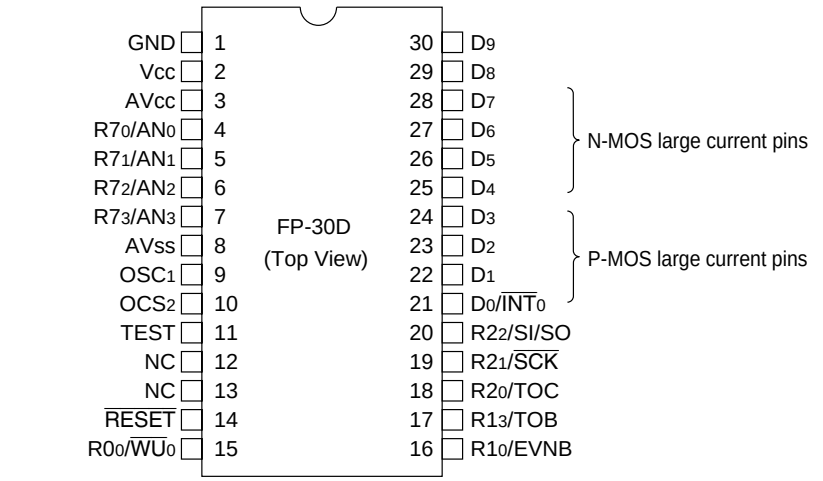
## Pin Arrangement

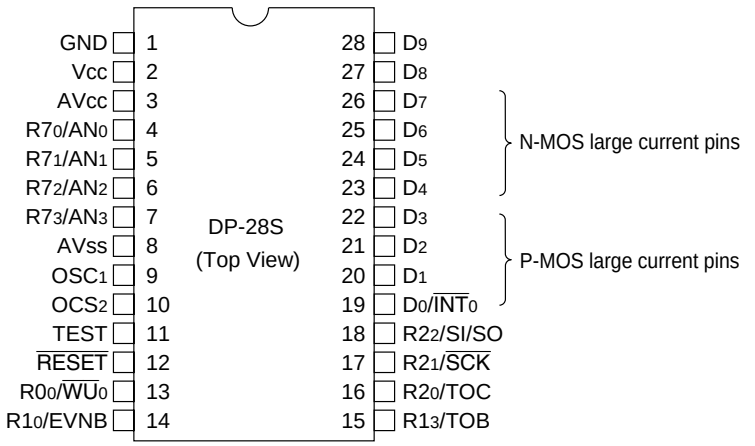
HD404374 Series

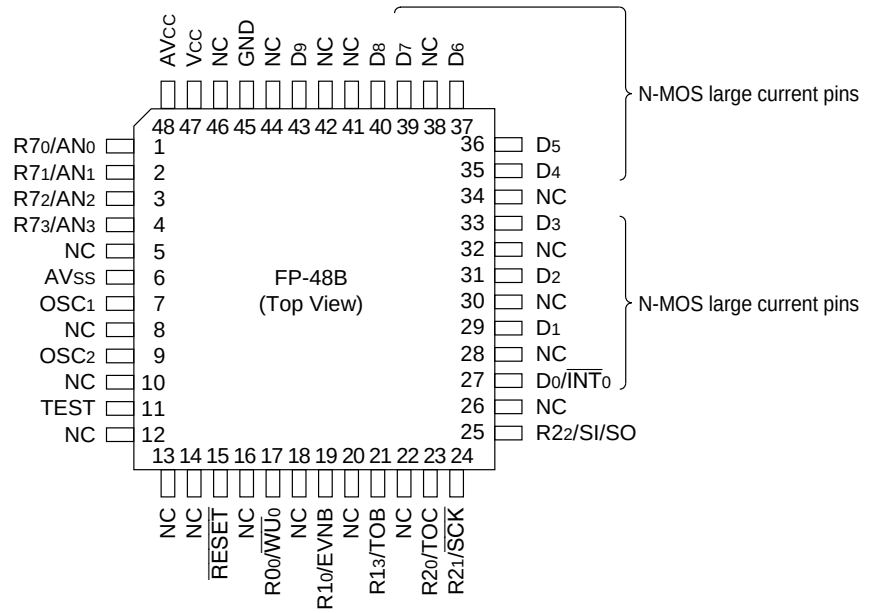


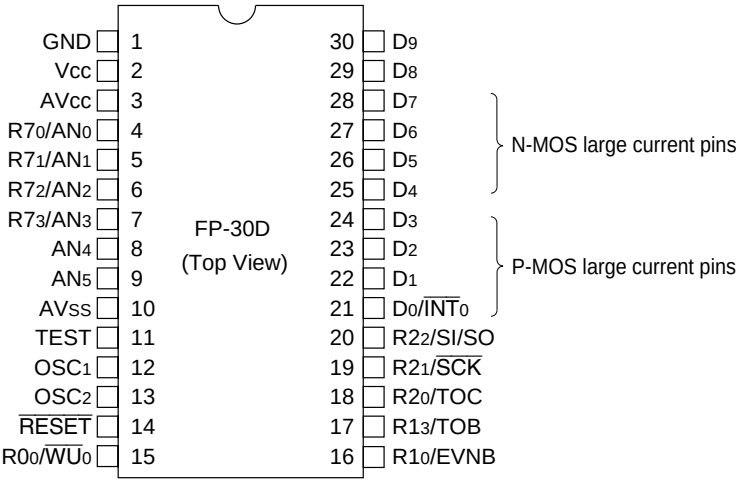
HD404384 Series



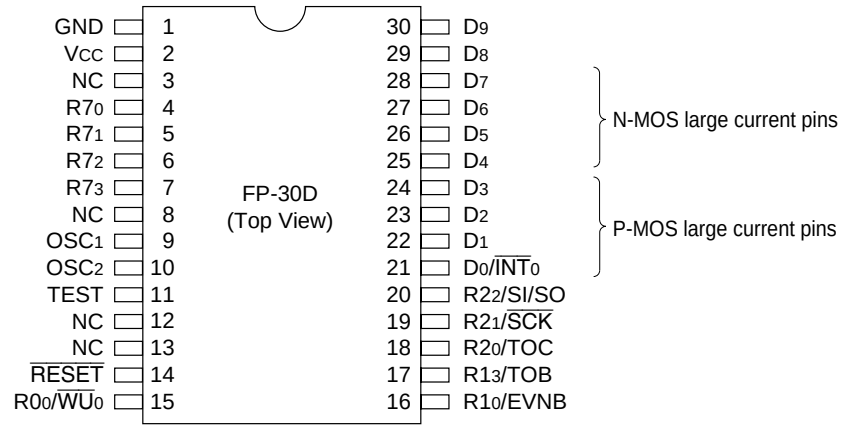



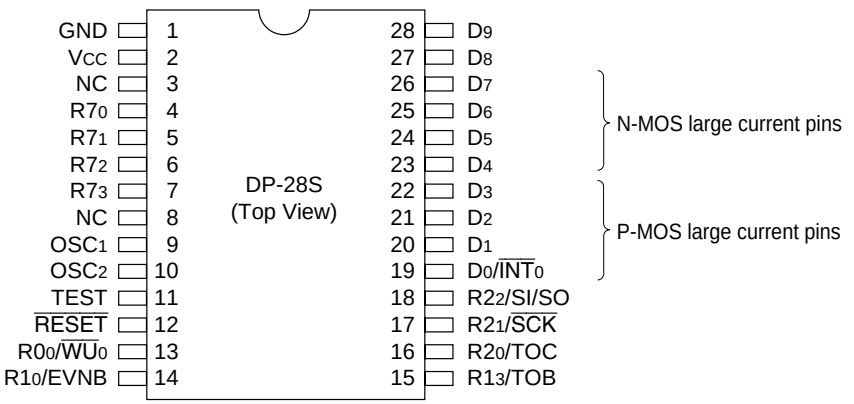



HD404389 Series



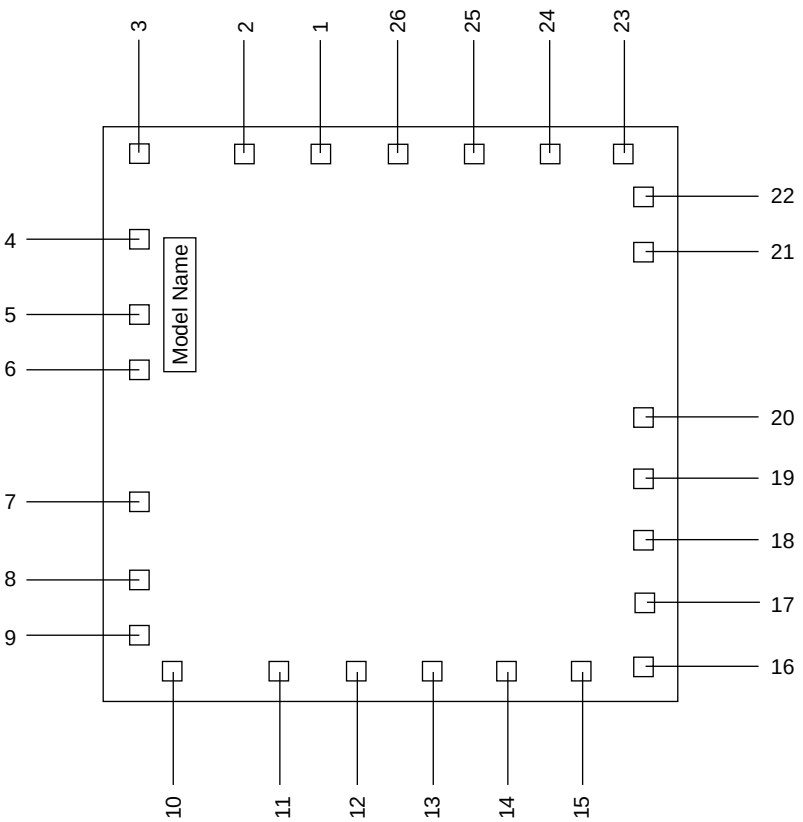

HD404082 and HD404084 Series



## Pad Arrangement

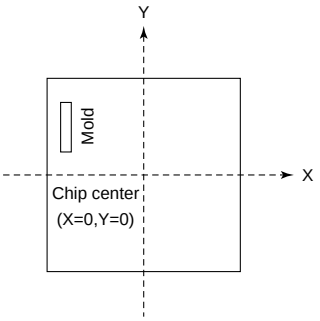
### HCD404082 and HCD404084




Model Name: HD404082 (HCD404082)
HD404084 (HCD404084)

## Pad Coordinates

### HCD404082 and HCD404084




Chip size (X × Y): 4.63 × 4.77 (mm)
Coordinates: Pad center
Home point position: Chip center
Pad size (X × Y): 90 × 90 (µm)
Chip thickness: 280 (µm)

| Pad | | Coodinates | | Pad | | Coodinates | |
|---|---|---|---|---|---|---|---|
| No. | Pad name | X (µm) | Y (µm) | No. | Pad name | X (µm) | Y (µm) |
| 1 | GND | -458 | 1403 | 14 | $R2_0$ | 572 | -1403 |
| 2 | $V_{CC}$ | -826 | 1403 | 15 | $R2_1$ | 982 | -1403 |
| 3 | $R7_0$ | -1338 | 1403 | 16 | $R2_2$ | 1338 | -1403 |
| 4 | $R7_1$ | -1338 | 1006 | 17 | $D_0$ | 1338 | -1020 |
| 5 | $R7_2$ | -1338 | 525 | 18 | $D_1$ | 1338 | -637 |
| 6 | $R7_3$ | -1338 | 285 | 19 | $D_2$ | 1338 | -254 |
| 7 | OSC1 | -1338 | -550 | 20 | $D_3$ | 1338 | 129 |
| 8 | OSC2 | -1338 | -954 | 21 | $D_4$ | 1338 | 768 |
| 9 | TEST | -1338 | -1251 | 22 | $D_5$ | 1338 | 1170 |
| 10 | RESETN | -1197 | -1403 | 23 | $D_6$ | 1153 | 1403 |
| 11 | $R0_0$ | -577 | -1403 | 24 | $D_7$ | 751 | 1403 |
| 12 | $R1_0$ | -194 | -1403 | 25 | $D_8$ | 349 | 1403 |
| 13 | $R1_3$ | 189 | -1403 | 26 | $D_9$ | -53 | 1403 |

# Pin Description

## HD404374 and HD404384 Series

| Item | Symbol | Pin Number FP-30D | DP-28S*2 | DP-48B | I/O | Function |
|---|---|---|---|---|---|---|
| Power supply | $V_{CC}$ | 2 | 2 | 47 | — | Apply the power supply voltage to this pin. |
| | GND | 1 | 1 | 45 | — | Connect to ground. |
| Test | TEST | 11 | 11 | 11 | Input | Not for use by the user application. Connect to GND potential. |
| Reset | $\overline{RESET}$ | 14 | 12 | 15 | Input | Used to reset the MCU. |
| Oscillation | $OSC_1$ | 9 | 9 | 7 | Input | Internal oscillator input/output pins. Connect a ceramic resonator, crystal resonator, or external oscillator circuit. |
| | $OSC_2$ | 10 | 10 | 9 | Output | When using CR oscillation, connect a resistor. |
| | X1 | 13*1 | — | 13*1 | Input | Realtime clock oscillator input/output pins. Connect a 32.768 kHz crystal. If 32.768 kHz crystal oscillation is not used, fix the |
| | X2 | 12*1 | — | 12*1 | Output | X1 pin to $V_{CC}$ and leave the X2 pin open. |
| Port | $D_0$–$D_9$ | 21–30 | 19–28 | 27, 29, 31, 33, 35–37, 39, 40, 43 | I/O | I/O pins addressed bit by bit. $D_0$ to $D_3$ are large-current source pins (max. 10 mA), and $D_4$ to $D_9$ are large-current sink pins (max. 15 mA). |
| | $R0_0$, $R1_0$, $R1_3$, $R2_0$, $R2_1$, $R2_2$, $R7_0$–$R7_3$ | 15–20, 4–7 | 13–18, 4–7 | 17, 19, 21, 23–25, 1–4 | I/O | I/O pins, addressed in 4-bit units. |
| Interrupt | $\overline{INT_0}$ | 21 | 19 | 27 | Input | External interrupt input pin |
| Wakeup | $\overline{WU_0}$ | 15 | 13 | 17 | Input | Input pin used for transition from stop mode to active mode. |
| Serial interface | $\overline{SCK}$ | 19 | 17 | 24 | I/O | Serial interface clock I/O pin |
| | SI | 20 | 18 | 25 | Input | Serial interface receive data input pin |
| | SO | 20 | 18 | 25 | Output | Serial interface transmit data output pin |
| Timer | TOB,TOC | 17, 18 | 15, 16 | 21, 23 | Output | Timer output pins |
| | EVNB | 16 | 14 | 19 | Input | Event count input pin |
| A/D converter | $AV_{CC}$ | 3 | 3 | 48 | — | A/D converter power supply pin. Connect as close as possible to the $V_{CC}$ pin so as to be at the same potential as $V_{CC}$. |
| | $AV_{SS}$ | 8 | 8 | 6 | — | Ground pin for $AV_{CC}$. Connect as close as possible to the GND pin so as to be at the same potential as GND. |
| | $AN_0$–$AN_3$ | 4–7 | 4–7 | 1–4 | Input | A/D converter analog input pins |
| Other | NC | 12*2, 13*2 | — | 5, 8, 10, 12*2, 13*2, 14, 16, 18, 20, 22, 26, 28, 30, 32, 34, 38, 41, 42, 44, 46 | — | Connect to GND potential. |

Notes: *1 Applies to HD404374 Series.
*2 Applies to HD404384 Series.

### HD404389 Series

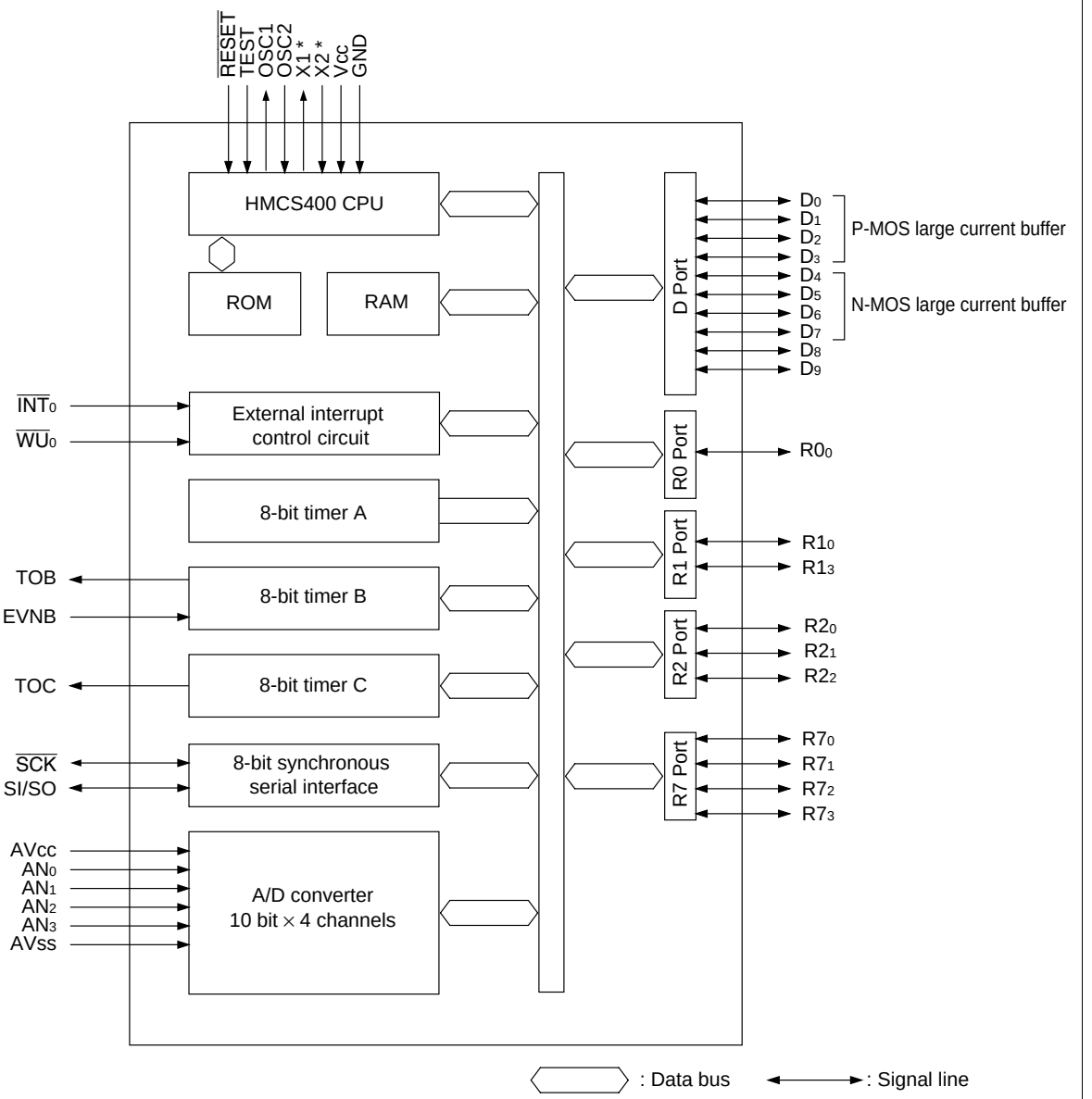
| Item | Symbol | Pin Number FP-30D | I/O | Function |
|---|---|---|---|---|
| Power supply | $V_{CC}$ | 2 | — | Apply the power supply voltage to this pin. |
| | GND | 1 | — | Connect to ground. |
| Test | TEST | 11 | Input | Not for use by the user application. Connect to GND potential. |
| Reset | $\overline{RESET}$ | 14 | Input | Used to reset the MCU. |
| Oscillation | $OSC_1$ | 12 | Input | Internal oscillator input/output pins. Connect a ceramic resonator, crystal resonator, or external oscillator circuit. |
| | $OSC_2$ | 13 | Output | When using CR oscillation, connect a resistor. |
| Port | $D_0$–$D_9$ | 21–30 | I/O | I/O pins addressed bit by bit. $D_0$ to $D_3$ are large-current source pins (max. 10 mA), and $D_4$ to $D_9$ are large-current sink pins (max. 15 mA). |
| | $R0_0$, $R1_0$, $R1_3$, $R2_0$, $R2_1$, $R2_2$, $R7_0$–$R7_3$ | 15–20, 4–7 | I/O | I/O pins, addressed in 4-bit units. |
| Interrupt | $\overline{INT}_0$ | 21 | Input | External interrupt input pin |
| Wakeup | $\overline{WU}_0$ | 15 | Input | Input pin used for transition from stop mode to active mode. |
| Serial interface | $\overline{SCK}$ | 19 | I/O | Serial interface clock I/O pin |
| | SI | 20 | Input | Serial interface receive data input pin |
| | SO | 20 | Output | Serial interface transmit data output pin |
| Timer | TOB,TOC | 17, 18 | Output | Timer output pins |
| | EVNB | 16 | Input | Event count input pin |
| A/D converter | $AV_{CC}$ | 3 | — | A/D converter power supply pin. Connect as close as possible to the $V_{CC}$ pin so as to be at the same potential as $V_{CC}$. |
| | $AV_{SS}$ | 10 | — | Ground pin for $AV_{CC}$. Connect as close as possible to the GND pin so as to be at the same potential as GND. |
| | $AN_0$–$AN_5$ | 4–9 | Input | A/D converter analog input pins |

## HD404082 and HD404084 Series

| Item | Symbol | Pin Number | | | I/O | Function |
|---|---|---|---|---|---|---|
| | | FP-30D | DP-28S | Chip | | |
| Power supply | $V_{CC}$ | 2 | 2 | 2 | — | Apply the power supply voltage to this pin. |
| | GND | 1 | 1 | 1 | — | Connect to ground. |
| Test | TEST | 11 | 11 | 9 | Input | Not for use by the user application. Connect to GND potential. |
| Reset | $\overline{RESET}$ | 14 | 12 | 10 | Input | Used to reset the MCU. |
| Oscillation | $OSC_1$ | 9 | 9 | 7 | Input | Internal oscillator input/output pins. Connect a ceramic resonator, crystal resonator, or external oscillator circuit. |
| | $OSC_2$ | 10 | 10 | 8 | Output | When using CR oscillation, connect a resistor. |
| Port | $D_0$–$D_9$ | 21–30 | 19–28 | 17–26 | I/O | I/O pins addressed bit by bit. $D_0$ to $D_3$ are large-current source pins (max. 10 mA), and $D_4$ to $D_9$ are large-current sink pins (max. 15 mA). |
| | $R0_0$, $R1_0$, $R1_3$, $R2_0$, $R2_1$, $R2_2$, $R7_0$–$R7_3$ | 15–20, 4–7 | 13–18, 4–7 | 11–16, 3–6 | I/O | I/O pins, addressed in 4-bit units. |
| Interrupt | $\overline{INT}_0$ | 21 | 19 | 17 | Input | External interrupt input pin |
| Wakeup | $\overline{WU}_0$ | 15 | 13 | 11 | Input | Input pin used for transition from stop mode to active mode. |
| Serial interface | $\overline{SCK}$ | 19 | 17 | 15 | I/O | Serial interface clock I/O pin |
| | SI | 20 | 18 | 16 | Input | Serial interface receive data input pin |
| | SO | 20 | 18 | 16 | Output | Serial interface transmit data output pin |
| Timer | TOB,TOC | 17, 18 | 15, 16 | 13, 14 | Output | Timer output pins |
| | EVNB | 16 | 14 | 12 | Input | Event count input pin |
| Other | NC | 3, 8, 12, 13 | 3, 8 | — | — | Connect to GND potential. |

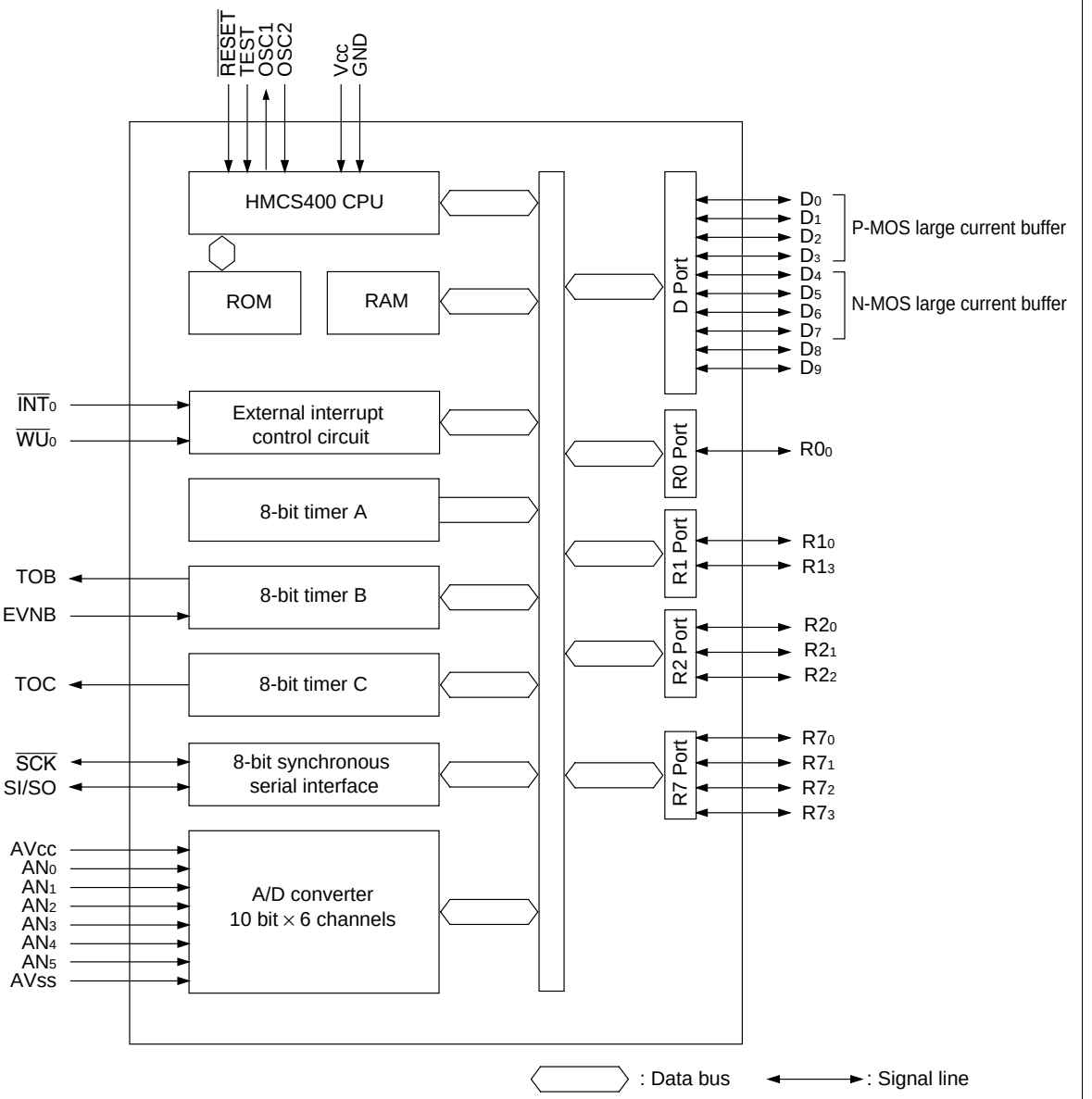
## Block Diagram

HD404374 and HD404384 Series

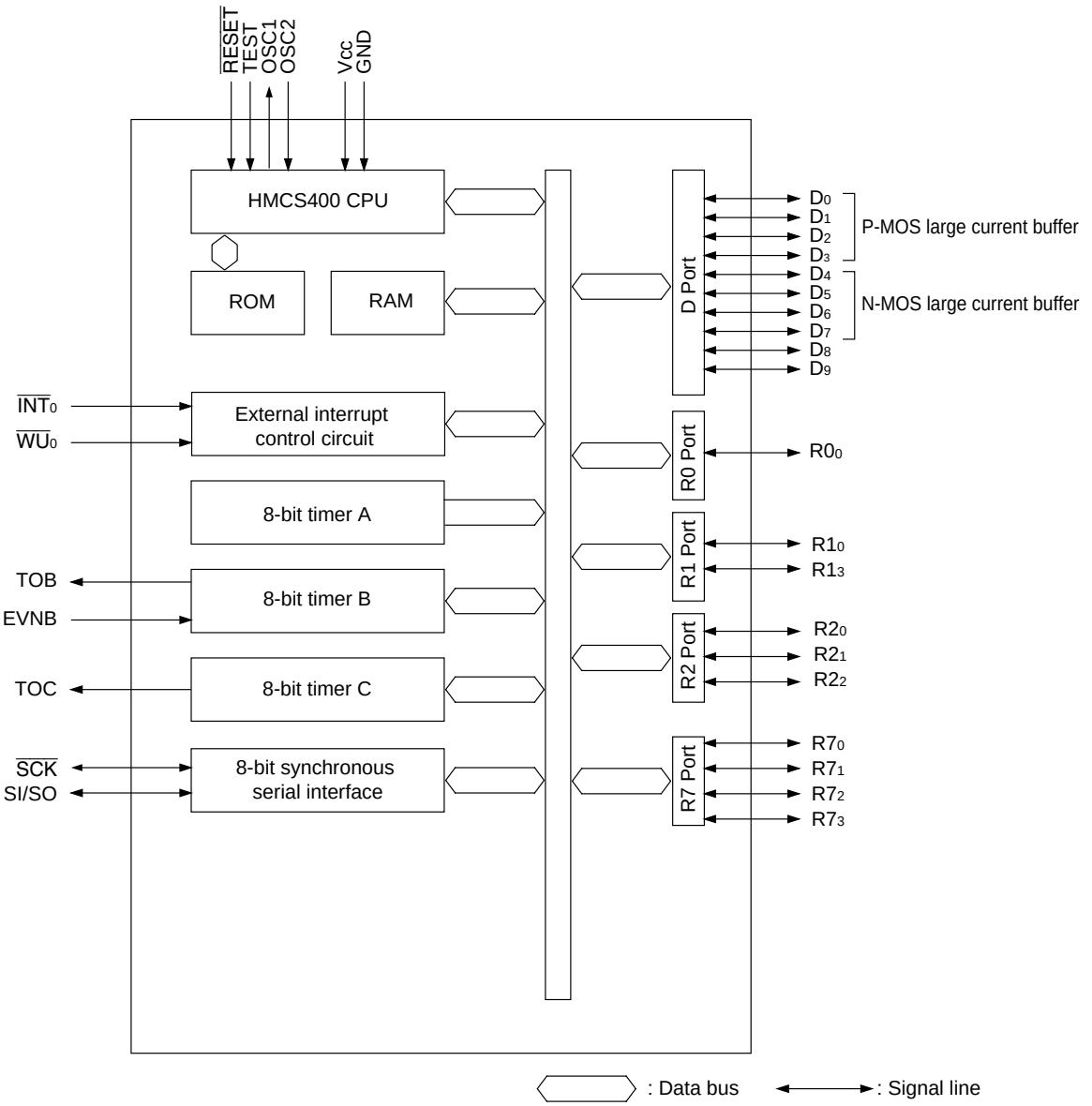



Note : * Applies to HD404374 Series.

HD404389 Series



HD404082 and HD404084 Series



## Memory Map

### ROM Memory Map

The ROM memory map is shown in figure 1 and is described below.

**Vector address area** ($0000 to $000F): When an MCU reset or interrupt handling is performed, the program is executed from the vector address. A JMPL instruction should be used to branch to the start address of the reset routine or the interrupt routine.

**Zero page subroutine area** ($0000 to $003F):A branch can be made to a subroutine in the area $0000 to $003F with the CAL instruction.

**Pattern area** ($0000 to $0FFF): ROM data in the area $0000 to $0FFF can be referenced as pattern data with the P instruction.

**Program area** ($0000 to $03FF (HD404081, HD40A4081, HD40C4081)), ($0000 to $07FF (HD404372, HD40A4372, HD40C4372, HD404382, HD40A4382, HD40C4382, HD404082, HCD404082, HD40A4082, HD40C4082, HCD40C4082)), ($0000 to $0FFF (HD404374, HD40A4374, HD40C4374, HD404384, HD40A4384, HD40C4384, HD407A4374, HD407C4374, HD407A4384, HD407C4384, HD404084, HCD404084, HD40A4084, HD40C4084, HCD40C4084)), ($0000 to $1FFF (HD404388, HD40A4388, HD40C4388)), ($0000 to $3FFF (HD404389, HD40A4389, HD40C4389, HD407A4389, HD407C4389)).

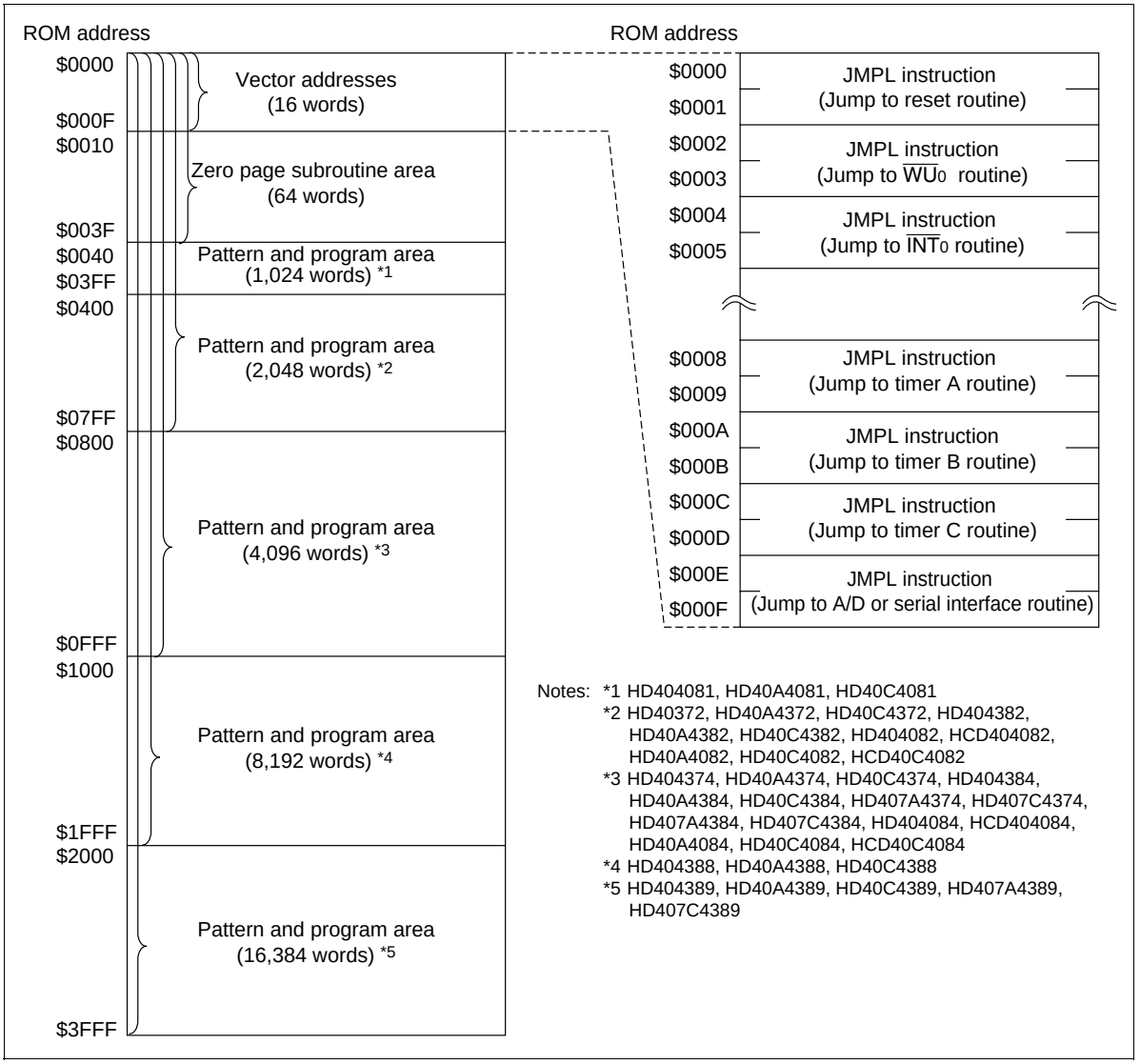
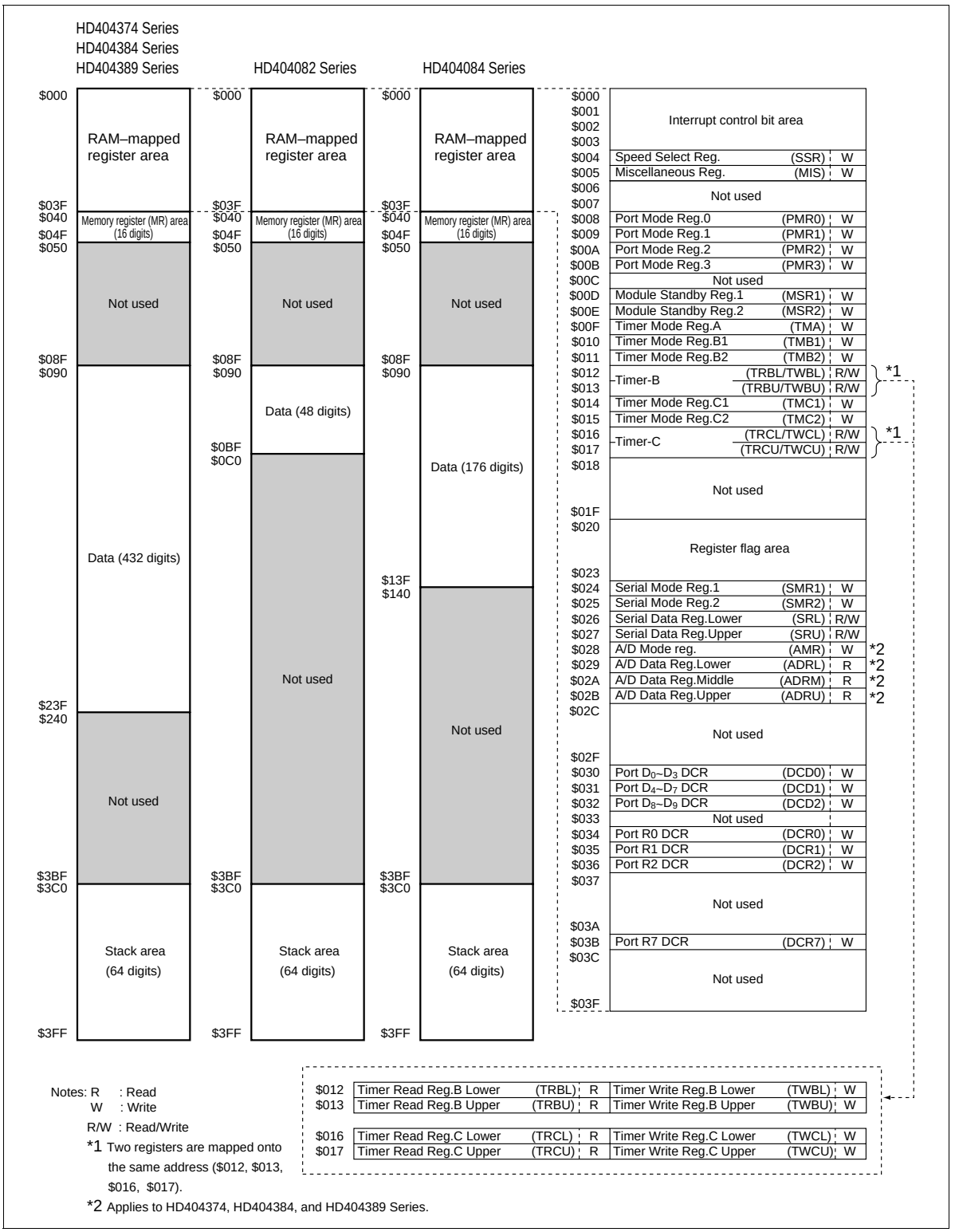



**Figure 1 ROM Memory Map**

**RAM Memory Map**

The MCU has on-chip RAM comprising a memory register area, data area, and stack area. In addition to these areas, an interrupt control bit area, special register area, and register flag area are mapped onto RAM memory space as a RAM-mapped register area.The RAM memory map is shown in figure 2 and described below.

**After power supply has been connected, regardless of a reset, the values for the memory register, data and stack areas will be undefined. Make sure to initialize prior to use.**




Notes: R : Read
W : Write
R/W : Read/Write
*1 Two registers are mapped onto the same address ($012, $013, $016, $017).
*2 Applies to HD404374, HD404384, and HD404389 Series.

**Figure 2 RAM Memory Map**

**RAM-mapped register area ($000 to $03F):**

- Interrupt control bit area ($000 to $003)

  This area consists of bits used for interrupt control. Its configuration is shown in figure 3. Individual bits can only be accessed by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, TM/TMD). There are restrictions on access to certain bits. The individual bits and instruction restrictions are shown in figure 4.
- Special register area ($004 to $01F, $024 to $03F)

  This area comprises mode registers and data registers for external interrupts, the serial interface, timers, A/D converter, etc., and I/O pin data control registers. Its configuration is shown in figures 2 and 5. These registers are of three kinds: write-only (W), read-only (R), and read/write (R/W). RAM bit manipulation instructions cannot be used on the other registers.
- Register flag area ($020 to $023)

  This area consists of the DTON and WDON flags and interrupt control bits. Its configuration is shown in figure 3. Individual bits can only be accessed by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, TM/TMD). There are restrictions on access to certain bits. The individual bits and instruction restrictions are shown in figure 4.

**Memory register (MR) area ($040 to $04F):**

In this data area, the 16 memory register digits (MR(0) to MR(15)) can also be accessed by the register-register instructions LAMR and XMRA. The configuration of this area is shown in figure 6.

**Data area** ($090 to $23F (HD404374, HD404384, HD404389 Series))
($090 to $0BF (HD404082 Series))
($090 to $13F (HD404084 Series))

**Stack area ($3C0 to $3FF):**

This is the stack area used to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when a subroutine call (CAL or CALL instruction) or interrupt handling is performed. As four digits are used for one level, the area can be used as a subroutine stack with a maximum of 16 levels. The saved data and saved status information are shown in figure 6. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored by the RTNI instruction, but are not affected by the RTN instruction. Any part of the area not used for saving can be used as a data area.

| RAM address | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|
| $000 | IMWU ($\overline{WU}_0$ interrupt mask) | IFWU ($\overline{WU}_0$ interrupt request flag) | RSP (Stack pointer reset) | IE (Interrupt enable flag) |
| $001 | Not used | Not used | IM0 ($\overline{INT}_0$ interrupt mask) | IF0 ($\overline{INT}_0$ interrupt request flag) |
| $002 | IMTB (Timer B interrupt mask) | IFTB (Timer B interrupt request flag) | IMTA (Timer A interrupt mask) | IFTA (Timer A interrupt request flag) |
| $003 | IMAD *2 (A/D converter interrupt mask) | IFAD *2 (A/D converter interrupt request flag) | IMTC (Timer C interrupt mask) | IFTC (Timer C interrupt request flag) |
| $020 | DTON *1 (DTON flag) | ADSF *2 (A/D start flag) | WDON (Watchdog on flag) | LSON *1 (Low speed on flag) |
| $021 | GEF (Gear enable flag) | Not used | Not used | Not used |
| $022 | Not used | Not used | Not used | Not used |
| $023 | IMS (Serial interrupt mask) | IFS (Serial interrupt request flag) | Not used | Not used |

IF : Interrupt Request Flag
IM : Interrupt Mask
IE : Interrupt Enable Flag
SP : Stack Pointer

Notes: *1 Applies to HD404374 Series.
*2 Applies to HD404374, HD404384, and HD404389 Series.

**Figure 3 Interrupt Control Bit and Register Flag Area Configuration**

Bits in the interrupt control bit area and register flag area can be set and reset by the SEM or SEMD instruction and the REM or REMD instruction, and tested by the TM or TMD instruction. They are not affected by any other instructions.
The following restrictions apply to individual bits.

| | SEM/SEMD | REM/REMD | TM/TMD |
|---|---|---|---|
| IE | Allowed | Allowed | Allowed |
| IM | | | |
| LSON *1 | | | |
| IF | Not executed | Allowed | Allowed |
| ICSF | | | |
| ICEF | | | |
| GEF | Allowed | Allowed | Inhibited |
| RSP | Not executed | Allowed | Inhibited |
| WDON | Allowed | Not executed | Inhibited |
| ADSF *2 | Allowed | Inhibited | Allowed |
| DTON *1 | Not executed in active mode | Allowed | Allowed |
| | Used in subactive mode | | |
| Not Used | Not executed | Not executed | Inhibited |

Notes : The WDON bit is reset only by stop mode clearance by means of an MCU reset.
Do not use the REM or REMD instruction on the ADSF bit during A/D conversion.
The DTON bit is always in the reset state in active mode.
If the TM or TMD instruction is used on a bit for which its use is prohibited, or on a nonexistent bit, the status flag value will be undetermined

* 1 Applies to HD404374 Series.
* 2 Applies to HD404374, HD404384, and HD404389 Series.

**Figure 4 Instruction Restrictions**

| RAM address | | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|
| | $000 | Interrupt control bit area | | | |
| | $003 | | | | |
| SSR | $004 | 32 kHz oscillation stop setting *1 | 32 kHz frequency division ratio selection *1 | System clock selection *1 | System clock frequency division ratio switching |
| MIS | $005 | Pull-up MOS control | Not used | Interrupt frame period selection *1 | |
| | $006 | Not used | | | |
| | $007 | | | | |
| PMR0 | $008 | Not used | | | $D_0/\overline{INT}_0$ |
| PMR1 | $009 | Not used | | | $R0_0/\overline{WU}_0$ |
| PMR2 | $00A | $R1_3$/TOB | Not used | | $R1_0$/EVNB |
| PMR3 | $00B | $R2_2$/SI/SO | | $R2_1/\overline{SCK}$ | $R2_0$/TOC |
| | $00C | Not used | | | |
| MSR1 | $00D | Not used | | Timer C clock on/off | Timer B lock on/off |
| MSR2 | $00E | Not used | | A/D clock on/off *2 | Serial clock on/off |
| TMA | $00F | Timer A / time base | Timer A clock source selection | | |
| TMB1 | $010 | Reload on/off | Timer B clock source selection | | |
| TMB2 | $011 | Not used | Timer B output mode setting | EVNB edge detection selection | |
| TRBL/TWBL | $012 | Timer B register (lower) | | | |
| TRBU/TWBU | $013 | Timer B register (upper) | | | |
| TMC1 | $014 | Reload on/off | Timer C clock source selection | | |
| TMC2 | $015 | Not used | Time C output mode selection | Not used | |
| TRCL/TWCL | $016 | Timer C register (lower) | | | |
| TRCU/TWCU | $017 | Timer C register (upper) | | | |
| | $018 | Not used | | | |
| | $01F | | | | |
| | $020 | Register flag area | | | |
| | $023 | | | | |
| SMR1 | $024 | Serial transfer clock speed selection | | | |
| SMR2 | $025 | Not used | $R2_2$/SI/SO PMOS control | SO idle H/L setting | Not used |
| SRL | $026 | Serial data register (lower) | | | |
| SRU | $027 | Serial data register (upper) | | | |
| AMR | $028 | Analog channel selection *2 | | | A/D conversion time *2 |
| ADRL | $029 | A/D data register (bit 1, 0) *2 | | Not used | |
| ADRM | $02A | A/D data register (bit 5 to 2) *2 | | | |
| ADRU | $02B | A/D data register (bit 9 to 6) *2 | | | |
| | $02C | Not used | | | |
| | $02F | | | | |
| DCD0 | $030 | $PortD_3$DCR | $PortD_2$DCR | $PortD_1$DCR | $PortD_0$DCR |
| DCD1 | $031 | $PortD_7$DCR | $PortD_6$DCR | $PorD_5$DCR | $PortD_4$DCR |
| DCD2 | $032 | Not used | | $PortD_9$DCR | $PortD_8$DCR |
| | $033 | Not used | | | |
| DCR0 | $034 | Not used | | | $PortR0_0$DCR |
| DCR1 | $035 | $PortR1_3$DCR | Not used | | $PortR1_0$DCR |
| DCR2 | $036 | Not used | $PortR2_2$DCR | $PortR2_1$DCR | $PortR2_0$DCR |
| | $037 | Not used | | | |
| | $03A | | | | |
| DCR7 | $03B | $PortR7_3$DCR | $PortR7_2$DCR | $PortR7_1$DCR | $PortR7_0$DCR |
| | $03C | Not used | | | |
| | $03F | | | | |

Notes: *1 Applies to HD404374 Series.
*2 Applies to HD404374, HD404384, and HD404389 Series.

**Figure 5 Special Function Register Area**

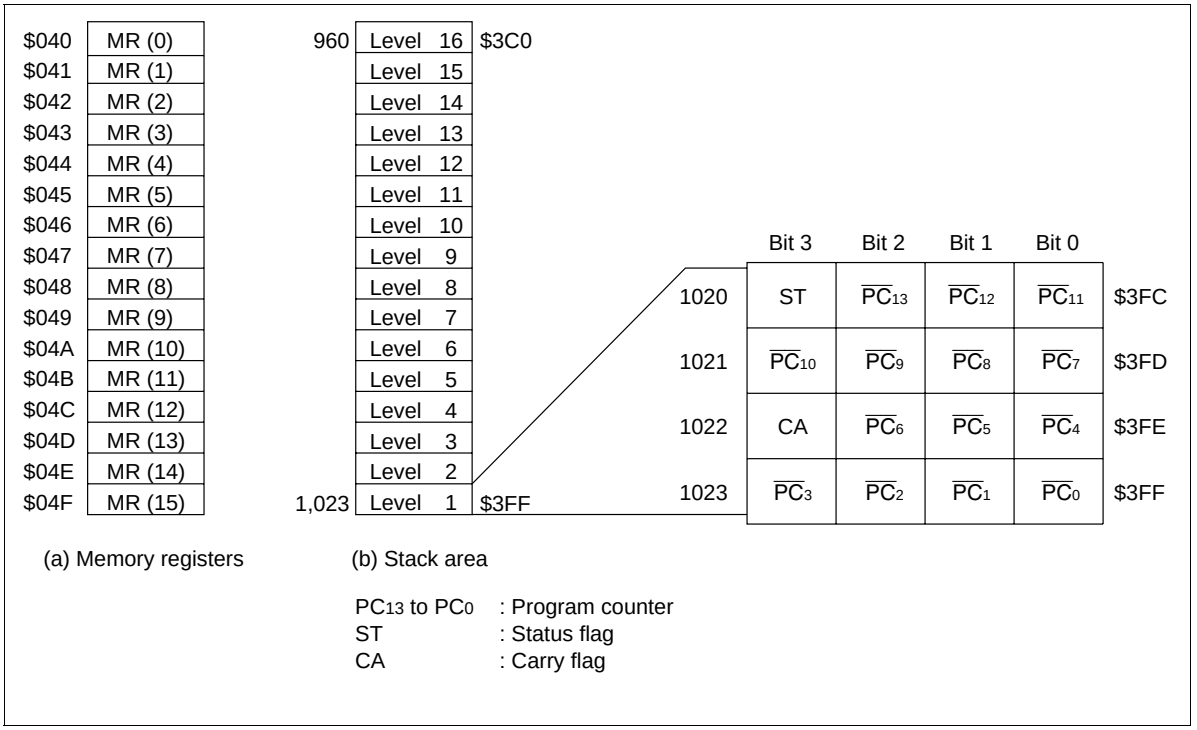



**Figure 6 Configuration of Memory Registers and Stack Area, and Stack Position**

## Functional Description

### Registers and Flags

The MCU has nine registers and two flags for CPU operations. they are shown in figure 7 and described below.

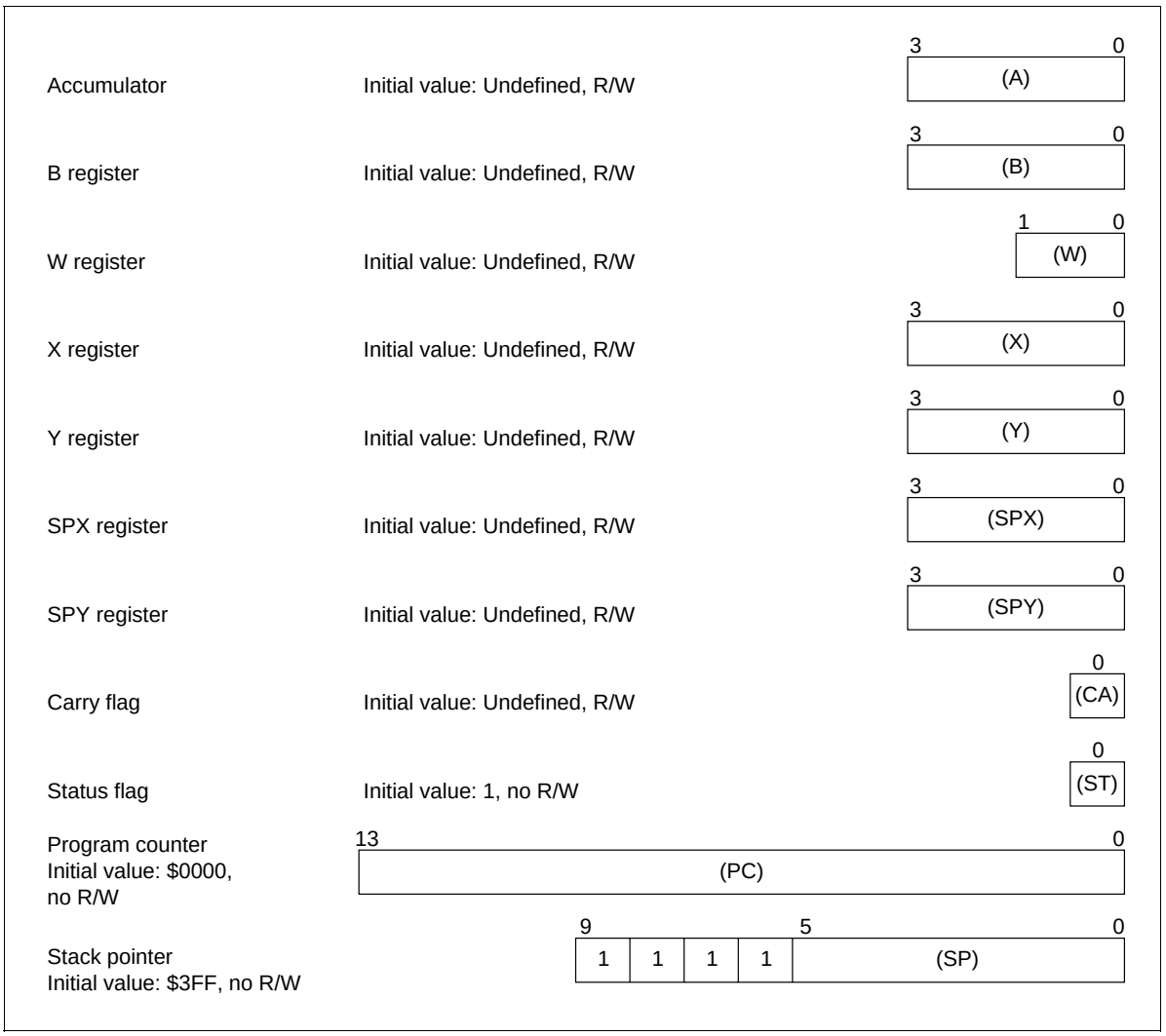



**Figure 7 Registers and Flags**

**Accumulator (A) and B register (B):**
The accumulator and B register are 4-bit registers used to hold the result of an ALU operation, and for data transfer to or from memory, an I/O area, or another register.

**W register (W), X register (X) and Y register (Y):**
The W register is a 2-bit register, and the X and Y registers are 4-bit registers, used for RAM register indirect addressing. The Y register is also used for D port addressing.

**SPX register (SPX) and SPY register (SPY):**
The SPX and SPY registers are 4-bit registers used as X register and Y register auxiliary registers, respectively.

**Carry flag (CA):**
This flag holds ALU overflow when an arithmetic/logic instruction is executed. It is also affected by the SEC, REC, ROTL, and ROTR instructions. The contents of the carry flag are saved to the stack when interrupt handling is performed, and are restored from the stack by the RTNI instruction (but are not affected by the RTN instruction).

**Status flag (ST):**
This flag holds ALU overflow when an arithmetic/logic or compare instruction is executed, and the result of an ALU non-zero or bit test instruction. It is used as the branch condition for the BR, BRL, CAL, and CALL instructions. The status flag is a latch-type flag, and does not change until the next arithmetic/logic, compare, or bit test instruction is executed. After a BR, BRL, CAL, or CALL instruction, the status flag is set to 1 regardless of whether the instruction is executed or skipped. The contents of the status flag are saved to the stack when interrupt handling is performed, and are restored from the stack by the RTNI instruction (but are not affected by the RTN instruction).

**Program counter (PC):**
This is a 14-bit binary counter that holds ROM address information.

**Stack pointer (SP):**
The stack pointer is a 10-bit register that holds the address of the next save space in the stack area. The stack pointer is initialized to $3FF by an MCU reset. The stack pointer is decremented by 4 each time data is saved, and incremented by 4 each time data is restored. The upper 4 bits of the stack pointer are fixed at 1111, so that a maximum of 16 stack levels can be used.

There are two ways in which the stack pointer is initialized to $3FF: by an MCU reset as mentioned above, or by resetting the RSP bit with the REM or REMD instruction.

**Reset**

An MCU reset is performed by driving the $\overline{\text{RESET}}$ pin low. At power-on, and when subactive mode, watch mode, or stop mode is cleared, $\overline{\text{RESET}}$ should be input for at least tRC to provide the oscillation settling time for the oscillator.In other cases, the MCU is reset by inputting $\overline{\text{RESET}}$ for at least two instruction cycles.

Table 1 shows the areas initialized by an MCU reset, and their initial values.

**Table 1 (1) Initial Values after MCU Reset**

| Item | | Abbr. | Initial value | Contents |
|---|---|---|---|---|
| Program counter | | (PC) | $0000 | Program executed from ROM start address |
| Status flag | | (ST) | 1 | Branching by conditional branch instruction enabled |
| Stack pointer | | (SP) | $3FF | Stack level is 0 |
| Interrupt | Interrupt enable flag | (IE) | 0 | All interrupts disabled |
| flags/ mask | Interrupt request flag | (IF) | 0 | No interrupt requests |
| | Interrupt mask | (IM) | 1 | Interrupt requests masked |
| I/O | Port data register | (PDR) | All bits 1 | "1" level output possible |
| | Data control registers | (DCD0 ~ 2) | All bits 0 | Output buffer off (high impedance) |
| | Data control registers | ($DCR0_0$ , $DCR1_0$, $DCR1_3$, $DCR2_0$ – $DCR2_2$, $DCR7_0$ – $DCR7_3$) | All bits 0 | |
| | Port mode register 0 | (PMR0) | ---0 | See port mode register 0 section |
| | Port mode register 1 | (PMR1) | ---0 | See port mode register 1 section |
| | Port mode register 2 | (PMR2) | 0--0 | See port mode register 2 section |
| | Port mode register 3 | (PMR3) | 0000 | See port mode register 3 section |
| Timers | Timer mode register A | (TMA) | 0000 | See timer mode register A section |
| | Timer mode register B1 | (TMB1) | 0000 | See timer mode register B1 section |
| | Timer mode register B2 | (TMB2) | -000 | See timer mode register B2 section |
| | Timer mode register C1 | (TMC1) | 0000 | See timer mode register C1 section |
| | Timer mode register C2 | (TMC2) | -0-- | See timer mode register C2 section |
| | Prescaler S | (PSS) | $000 | |
| | Prescaler W | (PSW) | $00 | |
| | Timer/counter A | (TCA) | $00 | |
| | Timer/counter B | (TCB) | $00 | |
| | Timer/counter C | (TCC) | $00 | |
| | Timer write register B | (TWBU,L) | $X0 | |
| | Timer write register C | (TWCU,L) | $X0 | |

**Table 1 (2) Initial Values after MCU Reset**

| Item | | Abbr. | Initial value | Contents |
|---|---|---|---|---|
| Serial interface | Serial mode register 1 | (SMR1) | 0000 | See serial mode register 1 section |
| | Serial mode register 2 | (SMR2) | -0X- | See serial mode register 2 section |
| | Serial data register | (SRU,L) | $XX | |
| | Octal counter | | 000 | |
| A/D converter | A/D mode register | (AMR) | 0000 | See A/D mode register section |
| | A/D data register U | (ADRU) | 0111 | See A/D data register section |
| | A/D data register M | (ADRM) | 1111 | |
| | A/D data register L | (ADRL) | 11- - | |
| Bit registers | Low speed on flag | (LSON) | 0 | See low-power mode section |
| | Watchdog timer on flag | (WDON) | 0 | See timer C section |
| | A/D start flag | (ADSF) | 0 | See A/D converter section |
| | Direct transfer on flag | (DTON) | 0 | See low-power mode section |
| | Gear enable flag | (GEF) | 0 | See system clock gear function |
| Others | Miscellaneous register | (MIS) | 0-00 | See low-power mode and input/output sections |
| | System clock select register | (SSR) | 0000 | See low-power mode and oscillator circuit sections |
| | Module standby register 1 | (MSR1) | --00 | See timer section |
| | Module standby register 2 | (MSR2) | --00 | See serial interface and A/D converter sections |

Notes: 1. The state of registers and flags other than those listed above after an MCU reset is shown in table 1 (3).
2. X: Indicates invalid value, - indicates that the bit does not exist.

**Table 1 (3) Initial Values after MCU Reset**

| Item | Abbr. | After Stop Mode Clearance by $\overline{WU_0}$ | After Other MCU Reset |
|---|---|---|---|
| Carry flag | (CA) | Retain value immediately prior to entering stop mode | Value immediately prior to MCU reset is not guaranteed. Must be initialized by program. |
| Accumulator | (A) | | |
| B register | (B) | | |
| W register | (W) | | |
| X/SPX register | (X/SPX) | | |
| Y/SPY register | (Y/SPY) | | |
| RAM | | | |

**Interrupts**

There are a total of seven interrupt sources, comprising wakeup input ($\overline{WU}_0$), external interrupts ($\overline{INT}_0$), timer/counter (timer A, timer B, timer C) interrupts, a serial interface interrupt, and an A/D converter interrupt.

Each interrupt source is provided with an interrupt request flag, interrupt mask, and vector address, used for storing and controlling interrupt requests. In addition, an interrupt enable flag is provided to control interrupts as a whole.

Of the interrupt sources, the A/D converter and serial interface share the same vector address. Software must therefore determine which of the interrupt sources is requesting an interrupt at the start of interrupt handling.

**Interrupt control bits and interrupt handling:**
The interrupt control bits are mapped onto RAM addresses $000 to $003 and $023, and can be accessed by RAM bit manipulation instructions. However, the interrupt request flags (IF) cannot be set by software. When the MCU is reset, the interrupt enable flag (IE) and interrupt request flags (IF) are initialized to 0, and the interrupt masks (IM) are initialized to 1.

Figure 8 shows a block diagram of the interrupt control circuit, table 2 shows interrupt priorities and vector addresses, and table 3 lists the conditions for executing interrupt handling for each of the nine kinds of interrupt source. When the interrupt request flag is set to 1 and the interrupt mask is cleared to 0, an interrupt is requested. If the interrupt enable flag is set to 1 at this time, interrupt handling is started. The vector address corresponding to the interrupt source is generated by the priority control circuit.

The interrupt handling sequence is shown in figure 9, and the interrupt handling flowchart in figure 10. When an interrupt is accepted, execution of the previous instruction is completed in the first cycle. In the second cycle, the interrupt enable flag (IE) is reset. In the second and third cycles, the contents of the carry flag, status flag, and program counter are saved on the stack. In the third cycle, a jump is made to the vector address and instruction execution is resumed from that address.

In each vector address area, a JMPL instruction should be written that branches to the start address of the interrupt routine. In the interrupt routine, the interrupt request flag that caused interrupt handling must be reset by software.

**Table 2 Vector Addresses and Interrupt Priorities**

| Interrupt Source | Priority | Vector Address |
|---|---|---|
| RESET | — | $0000 |
| $\overline{WU}_0$ | 1 | $0002 |
| $\overline{INT}_0$ | 2 | $0004 |
| Timer A | 3 | $0008 |
| Timer B | 4 | $000A |
| Timer C | 5 | $000C |
| Serial interface, A/D converter | 6 | $000E |

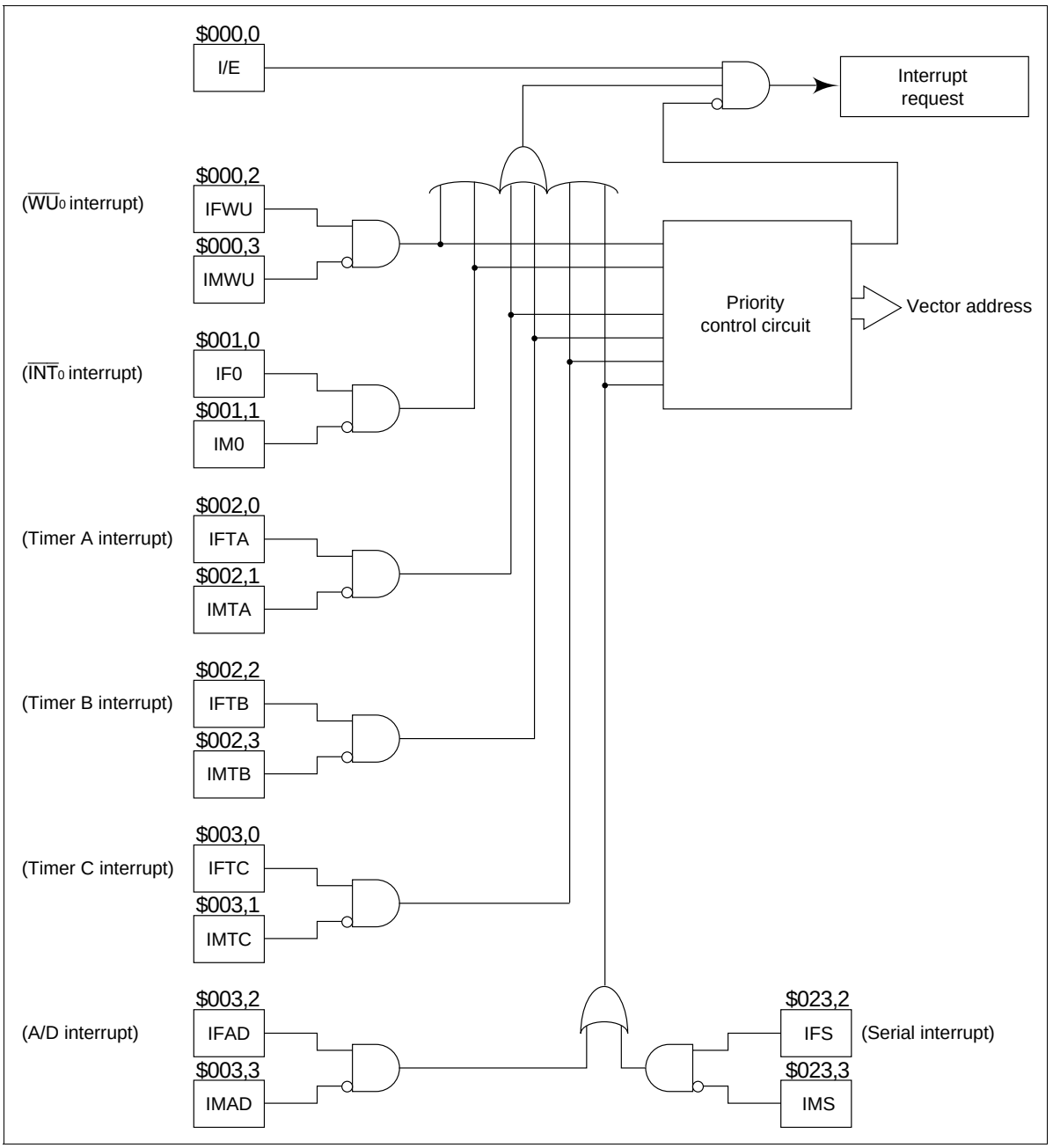



**Figure 8 Block Diagram of Interrupt Control Circuit**

**Table 3 Interrupt Processing and Activation Conditions**

| | Interrupt Source | | | | | |
|---|---|---|---|---|---|---|
| **Interrupt Control Bit** | **$\overline{WU_0}$** | **$\overline{INT_0}$** | **Timer A** | **Timer B** | **Timer C** | **A/D or Serial** |
| IE | 1 | 1 | 1 | 1 | 1 | 1 |
| IFWU•$\overline{IMWU}$ | 1 | 0 | 0 | 0 | 0 | 0 |
| IF0•$\overline{IM0}$ | * | 1 | 0 | 0 | 0 | 0 |
| IFTA•$\overline{IMTA}$ | * | * | 1 | 0 | 0 | 0 |
| IFTB•$\overline{IMTB}$ | * | * | * | 1 | 0 | 0 |
| IFTC•$\overline{IMTC}$ | * | * | * | * | 1 | 0 |
| IFAD•$\overline{IMAD}$+IFS•$\overline{IMS}$ | * | * | * | * | * | 1 |

Note: Operation is not affected whether the value is 0 or 1.

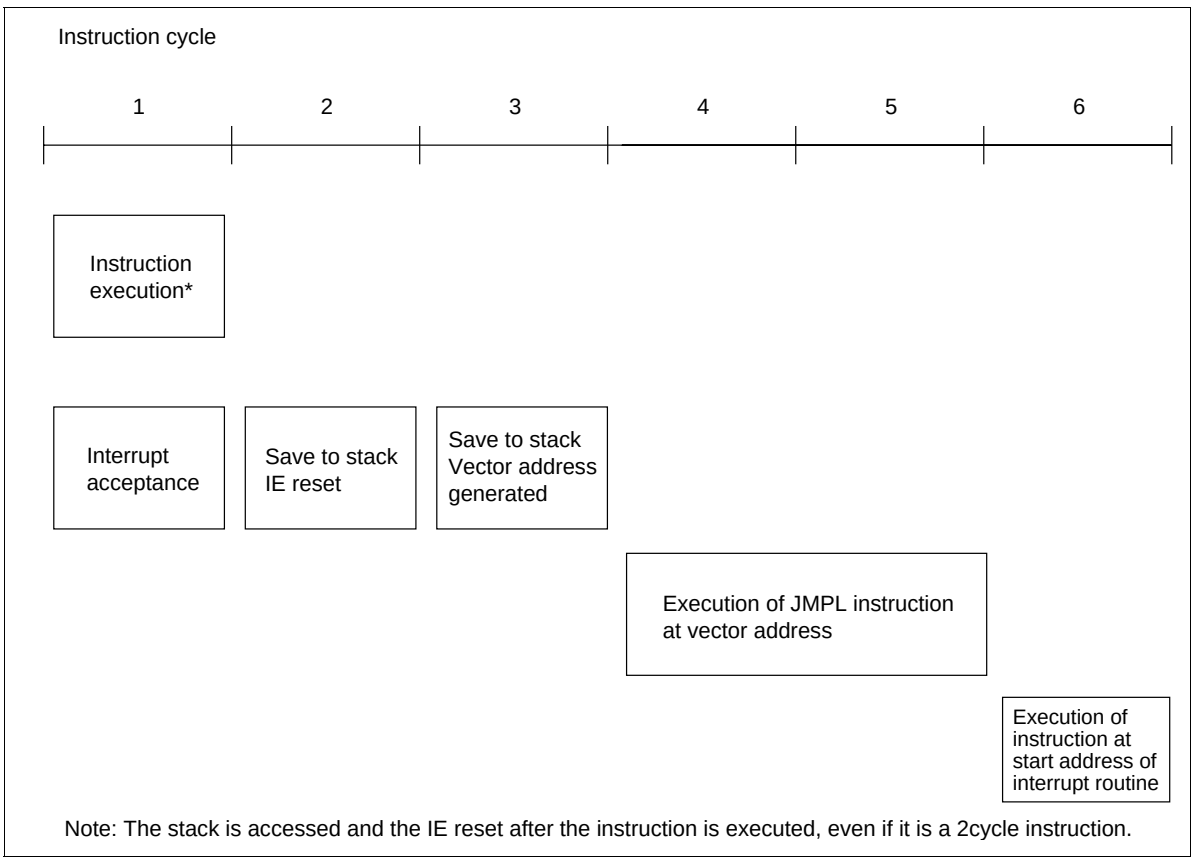



**Figure 9 Interrupt Sequence**

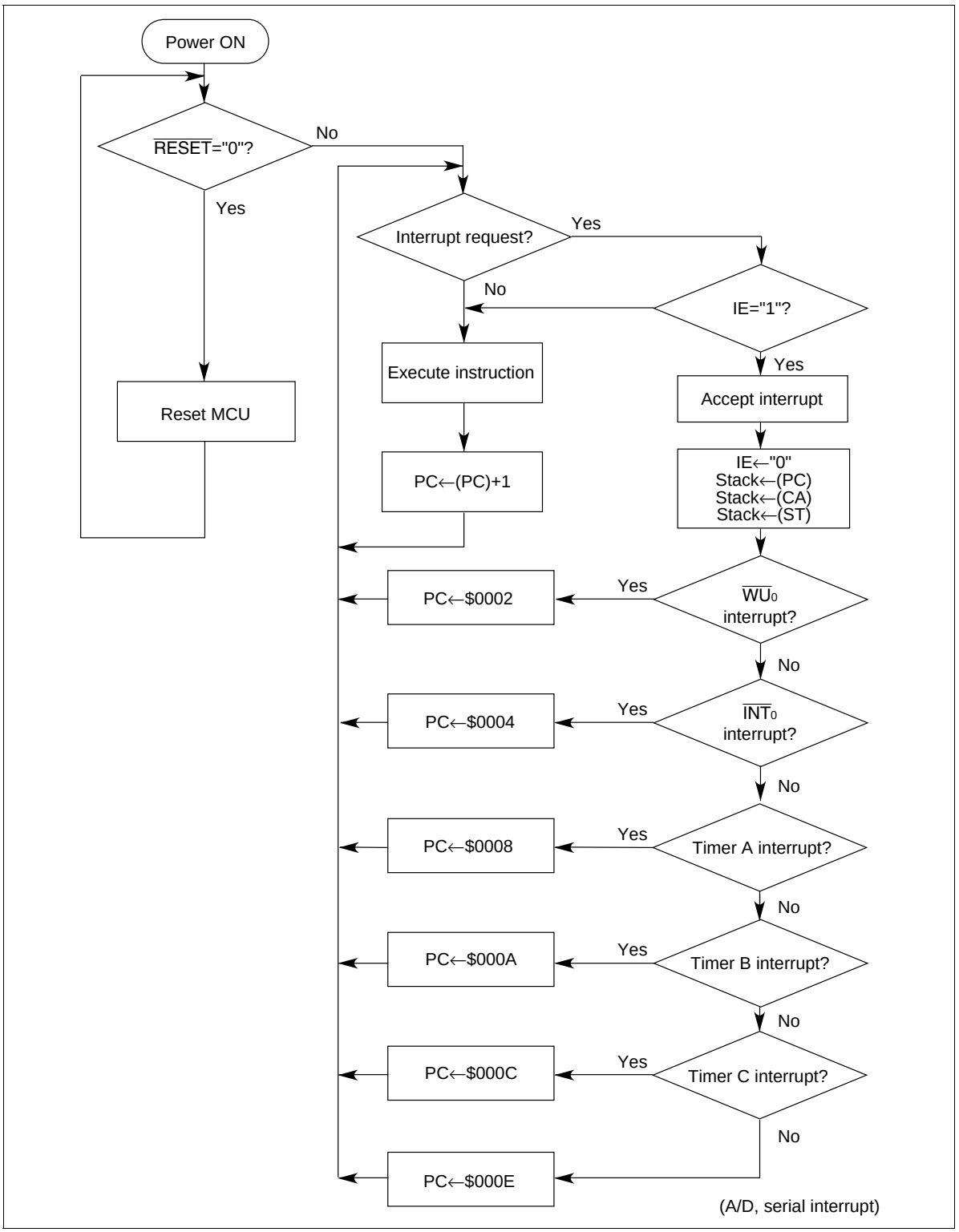



**Figure 10 Interrupt Handling Flowchart**

**Interrupt enable flag (IE: $000,0):**
The interrupt enable flag controls interrupt enabling/disabling of all interrupt requests as shown in table 4. The interrupt enable flag is reset by interrupt handling and set by the RTNI instruction.

**Table 4 Interrupt Enable Flag (IE: $000,0)**

| Interrupt Enable Flag (IE) | Interrupt Enabling/Disabling |
|---|---|
| 0 | Interrupts disabled |
| 1 | Interrupts enabled |

**Wakeup interrupt request flag (IFWU: $000,2):**
The wakeup interrupt request flag (IFWU) is set by the detection of a falling edge in $\overline{WU}_0$ input in active mode, subactive mode,watch mode, or standby mode. In stop mode, when a falling edge is detected at the wakeup pin, the MCU waits for the oscillation settling time, then switches to active mode. When a transition is made from stop mode to active mode with IE set to 1 and IMWU cleared to 0, wakeup interrupt handling is executed after the switch to active mode. The wakeup interrupt request flag (IFWU) is not set in this case (table 5).

**Table 5 Wakeup Interrupt Request Flag (IFWU: $000,2)**

| Wakeup Interrupt Request Flag (IFWU) | Interrupt Request |
|---|---|
| 0 | No wakeup interrupt request |
| 1 | Wakeup interrupt request generated |

**Wakeup Interrupt Mask (IMWU: $000,3):**
This bit masks an interrupt request by the wakeup interrupt request flag (table 6).

**Table 6 Wakeup Interrupt Request Mask (IMWU: $000,3)**

| Wakeup Interrupt Mask (IMWU) | Interrupt Request |
|---|---|
| 0 | Wakeup interrupt request enabled |
| 1 | Wakeup interrupt request masked (held pending) |

**External interrupt request flag (IF0: $001, 0):**
The external interrupt request flag is set by an $\overline{INT_0}$ input falling edge (table 7).

**Table 7 External Interrupt Request Flag (IF0: $001, 0)**

| External Interrupt Request Flag (IF0) | Interrupt Request |
|---|---|
| 0 | No external interrupt request |
| 1 | External interrupt request generated |

**External interrupt mask (IM0: $001, 1):**
This bit masks an interrupt request by the external interrupt request flag (table 8).

**Table 8 External Interrupt Mask (IM0: $001, 1)**

| External Interrupt Mask (IM0) | Interrupt Request |
|---|---|
| 0 | External interrupt request enabled |
| 1 | External interrupt request masked (held pending) |

**Timer A interrupt request flag (IFTA: $002,0):**
The timer A interrupt request flag is set by timer A overflow output (table 9).

**Table 9 Timer A Interrupt Request Flag (IFTA: $002,0)**

| Timer A Interrupt Request Flag (IFTA) | Interrupt Request |
|---|---|
| 0 | No timer A interrupt request |
| 1 | Timer A interrupt request generated |

**Timer A interrupt mask (IMTA: $002,1):**
This bit masks an interrupt request by the timer A interrupt request flag (table 10).

**Table 10 Timer A Interrupt Mask (IMTA: $002,1)**

| Timer A Interrupt Mask (IMTA) | Interrupt Request |
|---|---|
| 0 | Timer A interrupt request enabled |
| 1 | Timer A interrupt request masked (held pending) |

**Timer B interrupt request flag (IFTB: $002,2):**
The timer B interrupt request flag is set by timer B overflow output (table 11).

**Table 11 Timer B Interrupt Request Flag (IFTB: $002,2)**

| Timer B Interrupt Request Flag (IFTB) | Interrupt Request |
|---|---|
| 0 | No timer B interrupt request |
| 1 | Timer B interrupt request generated |

**Timer B interrupt mask (IMTB: $002,3):**
This bit masks an interrupt request by the timer B interrupt request flag (table 12).

**Table 12 Timer B Interrupt Mask (IMTB: $002,3)**

| Timer B Interrupt Mask (IMTB) | Interrupt Request |
|---|---|
| 0 | Timer B interrupt request enabled |
| 1 | Timer B interrupt request masked (held pending) |

**Timer C interrupt request flag (IFTC: $003,0):**
The timer C interrupt request flag is set by timer C overflow output (table 13).

**Table 13 Timer C Interrupt Request Flag (IFTC: $003,0)**

| Timer C Interrupt Request Flag (IFTC) | Interrupt Request |
|---|---|
| 0 | No timer C interrupt request |
| 1 | Timer C interrupt request generated (held pending) |

**Timer C interrupt mask (IMTC: $003,1):**
This bit masks an interrupt request by the timer C interrupt request flag (table 14).

**Table 14 Timer C Interrupt Mask (IMTC: $003,1)**

| Timer C Interrupt Mask (IMTC) | Interrupt Request |
|---|---|
| 0 | Timer C interrupt request enabled |
| 1 | Timer C interrupt request masked (held pending) |

**Serial interrupt request flag (IFS: $023,2):**
The serial interrupt request flag is set on completion of serial data transfer, or if data transfer is halted midway (table 15).

**Table 15 Serial Interrupt Request Flag (IFS: $023,2)**

| Serial Interrupt Request Flag (IFS) | Interrupt Request |
|---|---|
| 0 | No serial interrupt request |
| 1 | Serial interrupt request generated |

**Serial interrupt mask (IMS: $023,3):**
This bit masks an interrupt request by the serial interrupt request flag (table 16).

**Table 16 Serial Interrupt Mask (IMS: $023,3)**

| Serial Interrupt Mask (IMS) | Interrupt Request |
|---|---|
| 0 | Serial interrupt request enabled |
| 1 | Serial interrupt request masked (held pending) |

**A/D interrupt request flag (IFAD: $003,2) (Applies to HD404374, HD404384, and HD404389 Series):**
The A/D interrupt request flag is set on completion of A/D conversion (table 17).

**Table 17 A/D Interrupt Request Flag (IFAD: $003,2)**

| A/D Interrupt Request Flag (IFAD) | Interrupt Request |
|---|---|
| 0 | No A/D interrupt request |
| 1 | A/D interrupt request generated |

**A/D interrupt mask (IMAD: $003,3) (Applies to HD404374, HD404384, and HD404389 Series):**
This bit masks an interrupt request by the A/D interrupt request flag (table 18).

**Table 18 A/D Interrupt Mask (IMAD: $003,3)**

| Serial Interrupt Mask (IMAD) | Interrupt Request |
|---|---|
| 0 | A/D interrupt request enabled |
| 1 | A/D interrupt request masked (held pending) |

### Operating Modes

The five operating modes shown in table 19 can be used for the MCU.

The function of each mode is shown in table 20, and the state transition diagram among each mode in figure 11.

**Table 19 Operating Modes and Clock Status**

| | | Mode Name | | | | |
|---|---|---|---|---|---|---|
| | | **Active** | **Standby** | **Stop** | **Watch*[1]** | **Subactive*[1, 3]** |
| Activation method | | $\overline{\text{RESET}}$ cancellation, interrupt request, $\overline{\text{WU}}_0$ input in stop mode STOP/SBY instruction in subactive mode (when direct transfer is selected) | SBY instruction | STOP instruction when TMA3 = 0 | STOP instruction when TMA3 = 1 | $\overline{\text{INT}}_0$/timer A or $\overline{\text{WU}}_0$ interrupt request in watch mode |
| Status | System oscillator | OP | OP | Stopped | Stopped | Stopped |
| | Subsystem oscillator*[1] | OP | OP | OP*[2] | OP | OP |
| Cancellation method | | $\overline{\text{RESET}}$ input, STOP/SBY instruction | $\overline{\text{RESET}}$ input, interrupt request | $\overline{\text{RESET}}$ input, $\overline{\text{WU}}_0$ input | $\overline{\text{RESET}}$ input, $\overline{\text{INT}}_0$/timer A or $\overline{\text{WU}}_0$ interrupt request | $\overline{\text{RESET}}$ input, STOP/SBY instruction |

Notes: OP: implies in operation.

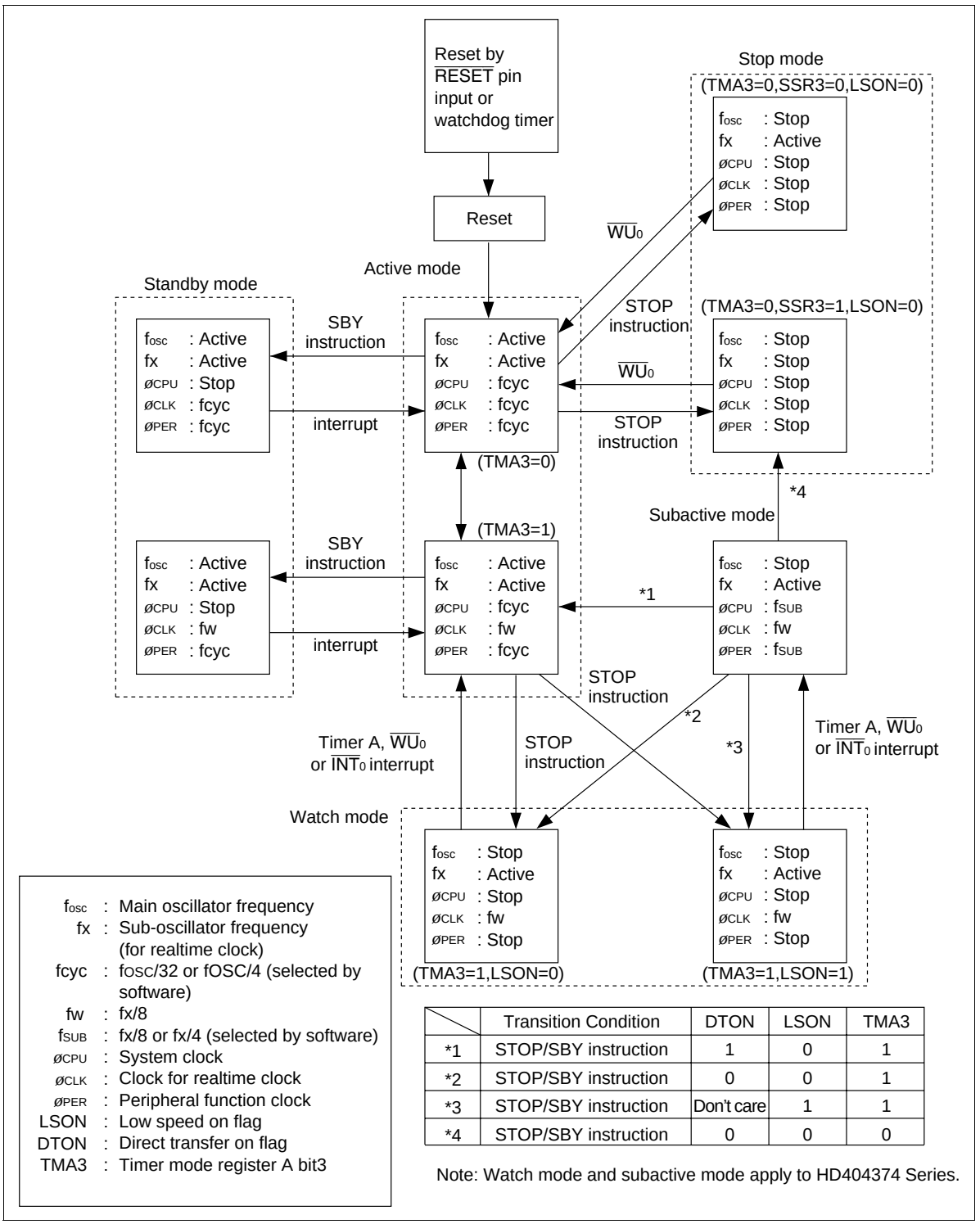
1. Applies to HD404374 Series.
2. Operating or stopping the oscillator can be selected by setting bit 3 of the system clock select register (SSR: $004)
3. Subactive mode is an optional function; specify it on the fnction option list.

**Table 20 Operation in Low-Power Dissipation Modes**

| Function | Stop Mode | Watch mode*[1] | Standby Mode | Subactive Mode*[1, 3] |
|---|---|---|---|---|
| CPU | Retained | Retained | Retained | OP |
| RAM | Retained | Retained | Retained | OP |
| Timer A | Stopped | OP | OP | OP |
| Timer B | Stopped | Stopped | OP | OP |
| Timer C | Stopped | Stopped | OP | OP |
| Serial interface | Stopped *[2] | Stopped *[2] | OP | OP |
| A/D *[4] | Stopped | Stopped | OP | Stopped |
| I/O | Retained | Retained | Retained | OP |

Notes: OP: implies in operation.

1. Applies to HD404374 Series.
2. Transmission/Reception is activated if a clock is input in external clock mode. However, interrupts stop.
3. Subactive mode is an optional function specified on the function option list.
4. Applies to HD404374, HD404384, and HD404389 Series.




| | |
|---|---|
| fosc | : Main oscillator frequency |
| fx | : Sub-oscillator frequency (for realtime clock) |
| fcyc | : fOSC/32 or fOSC/4 (selected by software) |
| fw | : fx/8 |
| fSUB | : fx/8 or fx/4 (selected by software) |
| øCPU | : System clock |
| øCLK | : Clock for realtime clock |
| øPER | : Peripheral function clock |
| LSON | : Low speed on flag |
| DTON | : Direct transfer on flag |
| TMA3 | : Timer mode register A bit3 |

| | Transition Condition | DTON | LSON | TMA3 |
|---|---|---|---|---|
| *1 | STOP/SBY instruction | 1 | 0 | 1 |
| *2 | STOP/SBY instruction | 0 | 0 | 1 |
| *3 | STOP/SBY instruction | Don't care | 1 | 1 |
| *4 | STOP/SBY instruction | 0 | 0 | 0 |

Note: Watch mode and subactive mode apply to HD404374 Series.

**Figure 11 MCU Status Transitions**

**Active mode:**
In active mode all functions operate. In this mode, the MCU operates on clocks generated by the $OSC_1$ and $OSC_2$ oscillator circuits.

**Standby mode:**
In standby mode the oscillators continue to operate but clocks relating to instruction execution halt. As a result, CPU operation stops, and registers, RAM, and the D port/R port set for output retain their state immediately prior to entering standby mode. Interrupts, timers, the serial interface, and other peripheral functions continue to operate.

Power consumption is lower than in active mode due to the halting of the CPU.

The MCU is switched to standby mode by executing the SBY instruction in active mode. Standby mode is cleared by $\overline{\text{RESET}}$ input or an interrupt request. When standby mode is cleared by $\overline{\text{RESET}}$ input, an MCU reset is performed. When standby mode is cleared by an interrupt request, the MCU enters active mode and executes a instruction following the SBY instruction. After executing the instruction, if the interrupt enable flag is set to 1, interrupt handling is executed; if the interrupt enable flag is cleared to 0, the interrupt request is held pending and normal instruction execution is continued.

MCU operation flowchart is shown in figure 12.

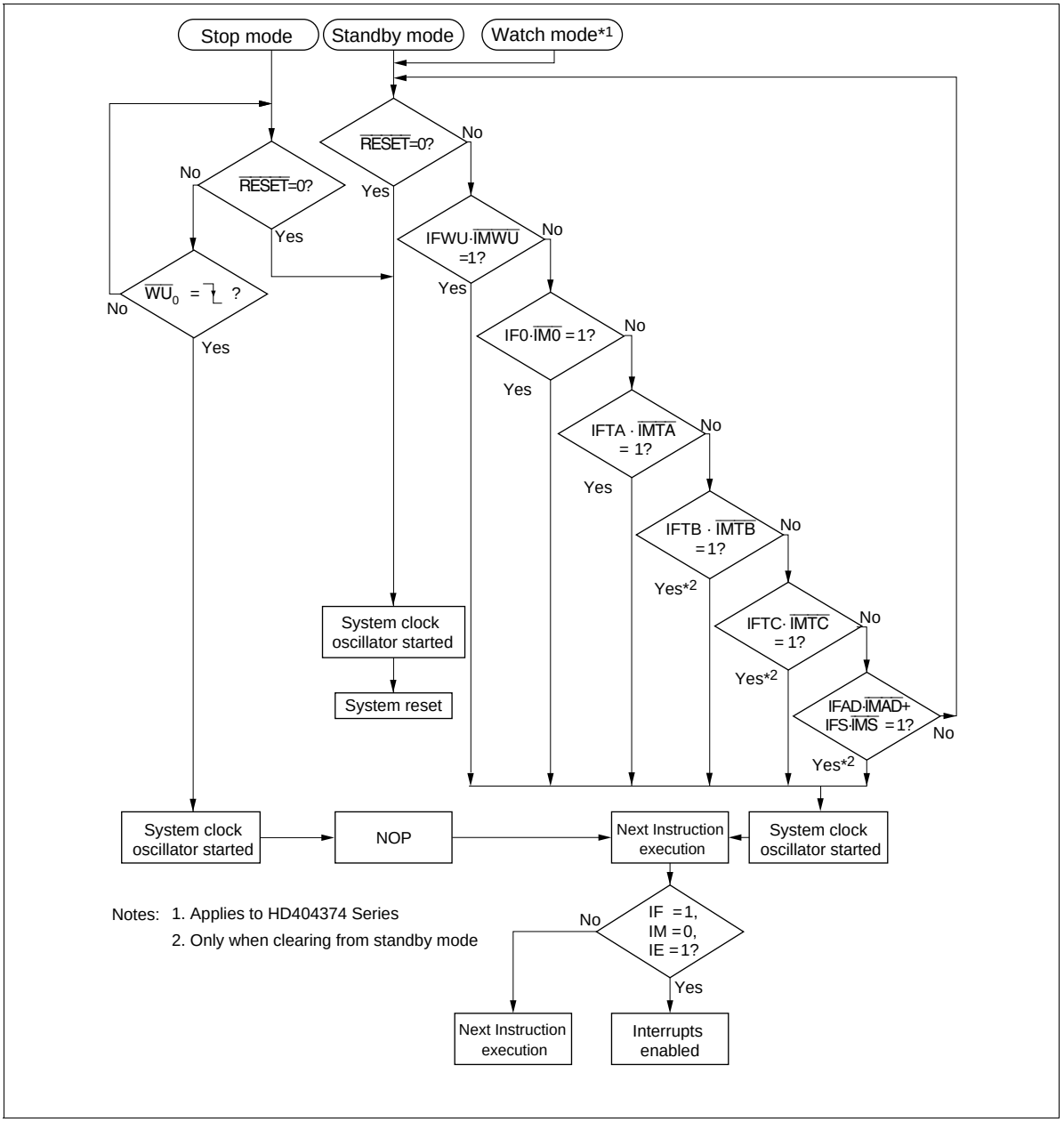



**Figure 12 MCU Operation Flowchart**

**Stop mode:**
In stop mode, all MCU function stop except that states prior to entry into stop mode are retained. This mode thus has the lowest power consumption of all operating mode.

In stop mode, the $OSC_1$ and $OSC_2$ oscillators stop. Bit 3 (SSR3) of the system clock select register (SSR: $004) (figure 22) can be used to select the active (= 0) or stopped (= 1) state for the X1 and X2 oscillators.

The MCU is switched to stop mode by executing a STOP instruction while bit 3 (TMA3) of timer mode register A (TMA: $00F) (figure 33) is cleared to 0 in active mode. Stop mode is cleared by $\overline{RESET}$ or $\overline{WU_0}$ input. When stop mode is cleared by $\overline{RESET}$, the RESET signal should be input for at least the oscillation settling time (tRC) (see "AC Characteristics") shown in figure 13. Then, the MCU is initialized and starts instruction execution from the start (address 0) of the program (IE = 0, IMWU = 0). If IE is set before entering stop mode (IE = 1, IMWU = 0), wakeup interrupt handling is executed after the transition to active mode.

When the MCU detects a falling edge at $\overline{WU_0}$ in stop mode, it automatically waits for the oscillation settling time, then switches to active mode. After the transition to active mode, the MCU resumes program execution from the instruction following the STOP instruction.

If stop mode is cleared by wakeup input, RAM data and registers retain their values prior to entering stop mode.

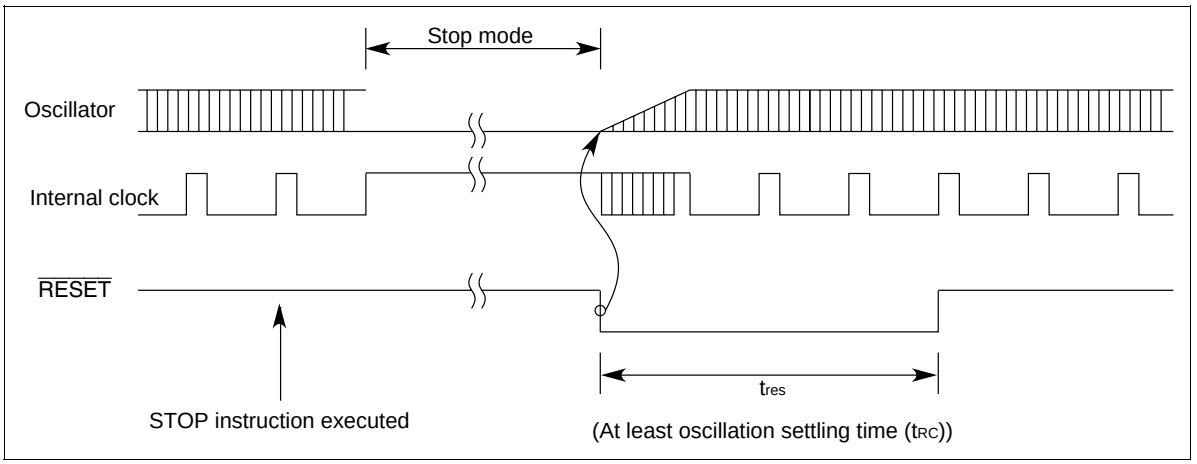



**Figure 13 Timing Chart for Clearing Stop Mode by RESET Input**

Note: If stop mode is cleared by wakeup input when an external clock is used as the system clock (OSC1), the subclock should not be stopped in stop mode.

**Watch mode ( Applies to HD404374 Series) :**
In watch mode, the realtime clock function (timer A) and LCD function using the X1 and X2 oscillators operate, but other functions stop. This mode thus has the second lowest power consumption after stop mode, and is useful for performing realtime clock display only.

In watch mode, the $OSC_1$ and $OSC_2$ oscillators stop but the X1 and X2 oscillators continue to operate.

The MCU is switched to watch mode by executing a STOP instruction while TMA3 = 1 in active mode, or by executing a STOP/SBY instruction in subactive mode.

Watch mode is cleared by $\overline{\text{RESET}}$ input or an $\overline{\text{INT}}_0$,timer A or $\overline{\text{WU}}_0$ interrupt request. For $\overline{\text{RESET}}$ input, refer to the section on stop mode. When watch mode is cleared by an $\overline{\text{INT}}_0$, timer A or $\overline{\text{WU}}_0$ interrupt request, the mode transition depends on the value of the LSON bit: the MCU enters active mode if LSON = 0, and enters subactive mode if LSON = 1. In the case of a transition to active mode, interrupt request generation is delayed to secure the oscillation settling time: the delay is the tRC set time for the timer A interrupt, and, for the $\overline{\text{INT}}_0$ interrupt or $\overline{\text{WU}}_0$ interrupt, Tx ($T + t_{RC} < Tx < 2T + t_{RC}$) if bit 1 and 0 (MIS1, MIS0) of the miscellaneous register are set to 00, or Tx ($t_{RC} < Tx < T + t_{RC}$) if MIS1 and MIS0 are set to 01 or 10 (figures 14 and 15). Other operations when the transition is made are the same as when watch mode is cleared (figure 12).

**Subactive mode ( Applies to HD404374 Series):**
In subactive mode, the $OSC_1$ and $OSC_2$ oscillator circuits stop and the MCU operates on clocks generated by the X1 and X2 oscillator circuits. In this mode, functions other than the A/D converter operate, but since the operating clocks are slow, power consumption is the lowest after watch mode.

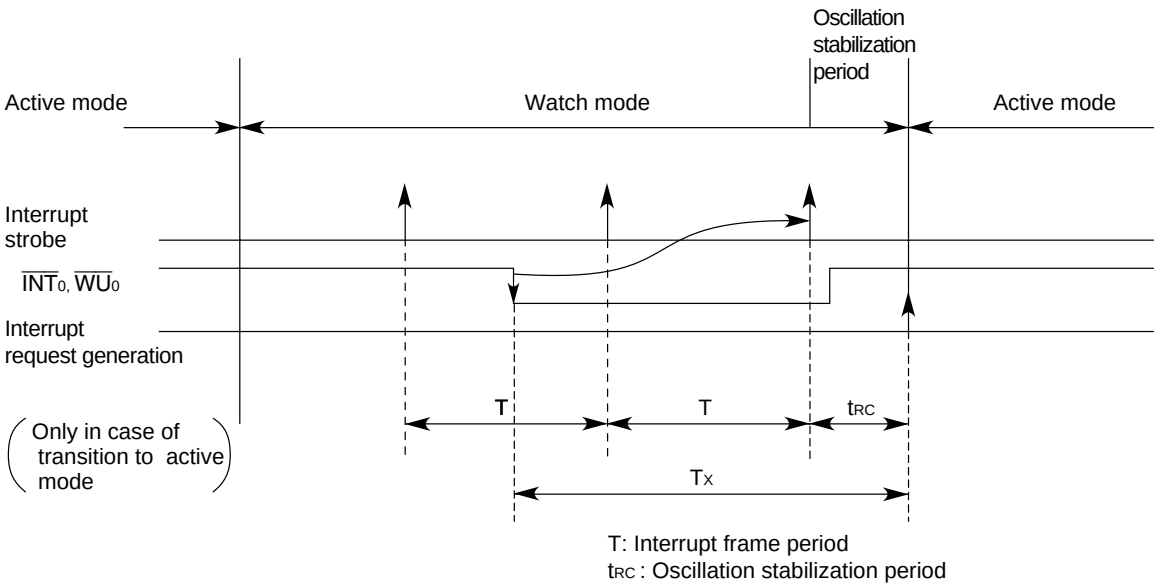
A CPU instruction processing speed of 244 µs or 122 µs can be selected according to whether bit 2 (SSR2) of the system clock select register (SSR: $004) is set to 1 or cleared to 0. The value of the SSR2 bit should be changed (0→1 or 1→0) only in active mode. If the value is changed in subactive mode, the MCU may operate incorrectly.

Subactive mode is cleared by executing a STOP/SBY instruction. A transition is then made to either watch mode or active mode according to the value of the low speed on flag (LSON: $020,0) and the direct transfer on flag (DTON: $020,3).

Subactive mode is a function option, and should be specified in the function option list.

**Interrupt frame ( Applies to HD404374 Series):**
In watch mode and subactive mode, $ø_{CLK}$ is supplied to the timer A, $\overline{\text{WU}}_0$, and $\overline{\text{INT}}_0$ acceptance circuits. Prescaler W and timer A operate as time bases, and generate interrupt frame timing. Either of two values can be selected for the interrupt frame period, T, by means of the miscellaneous register (MIS: $005) (figure 15).

In watch mode and subactive mode, the timing for generation of timer A, $\overline{\text{INT}}_0$ and $\overline{\text{WU}}_0$ interrupts is synchronized with the interrupt frame. Except for the case of an active mode transition, the interrupt strobe timing is used for interrupt request generation. Timer A generates overflow and interrupt requests at the interrupt strobe timing.




Note: If the time from the fall of the $\overline{INT_0}$ or $\overline{WU_0}$ signal until the interrupt is accepted and active mode is entered and is designated $T_X$, then $T_X$ will be in the following range :
$T+t_{RC} \leq T_X \leq 2T+t_{RC}$ (MIS1, MIS0=00)
$t_{RC} \leq T_X \leq T+t_{RC}$ (MIS1, MIS0=01 or 10)

**Figure 14 Interrupt Frame**

Miscellaneous Register (MIS: $005)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Reset | 0 | 0 | 0 | 0 |
| Bit name | MIS3 | Not used*4 | MIS1*1 | MIS0*1 |

See pull-up MOS control, figure 30

| MIS1 | MIS0 | Interrupt Frame period T(ms)*2 | Oscillation Settling Time tRC(ms)*2 | Oscillator Circuit Condition |
|---|---|---|---|---|
| 0 | 0 | 0.24414 | 0.12207(0.24414)*3 | External clock input, CR oscillation frequency |
| | 1 | 3.90625 | 7.8125 | Ceramic resonator |
| 1 | 0 | 3.90625 | 31.25 | Crystal resonator |
| | 1 | Not used | | ——— |

Notes: *1. Applies to HD404374 series.
*2. T and $t_{RC}$ values are for use of a 32.768 kHz crystal oscillator at the X1-X2 pins.
*3. This value applies only in case of direct transition operation.
*4. Must always be cleared to 0. Setting to 1 will cause incorrect operation.

**Figure 15 Miscellaneous Register (MIS)**

**Direct transition from subactive to active mode (Applies to HD404374 Series):**
A direct transition can be made from subactive mode to active mode by controlling the direct transfer on flag (DTON: $020,3) and low speed on flag (LSON: $020,0). The procedure is shown below.

(a) Set LSON = 0 and DTON = 1 in subactive mode.
(b) Execute a STOP or SBY instruction.
(c) After the lapse of the MCU internal processing time and the oscillation settling time, the MCU automatically switches from subactive mode to active mode (figure 16).

Notes: 1. The DTON flag ($020,3) can be set in only subactive mode. It is always in the reset state in active mode.
2. The condition for transition time $T_D$ from the subactive mode to active mode is as follows: $t_{RC} < T_D < T + t_{RC}$.

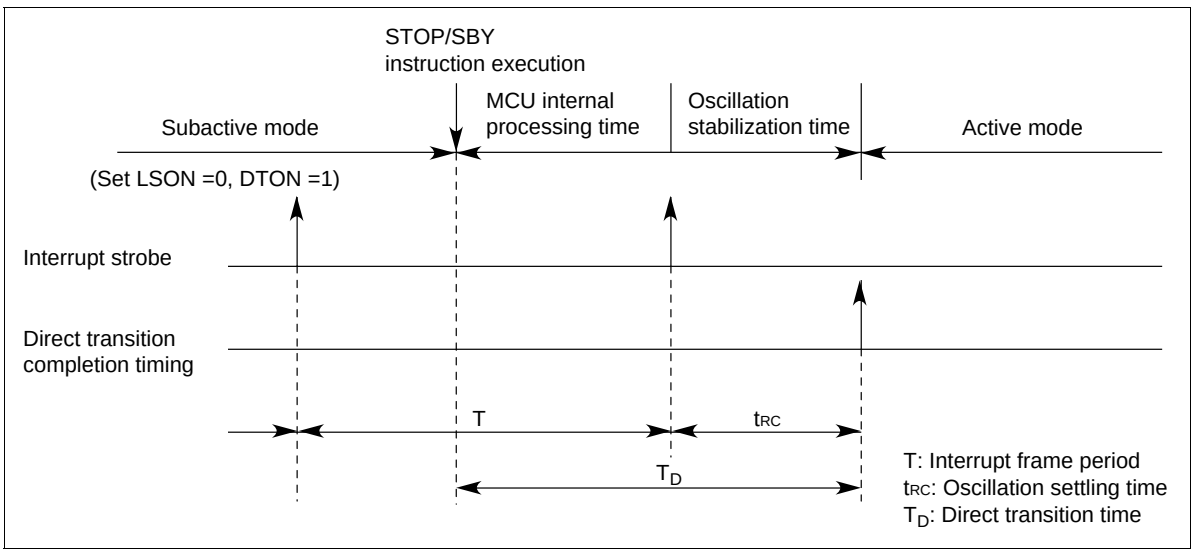
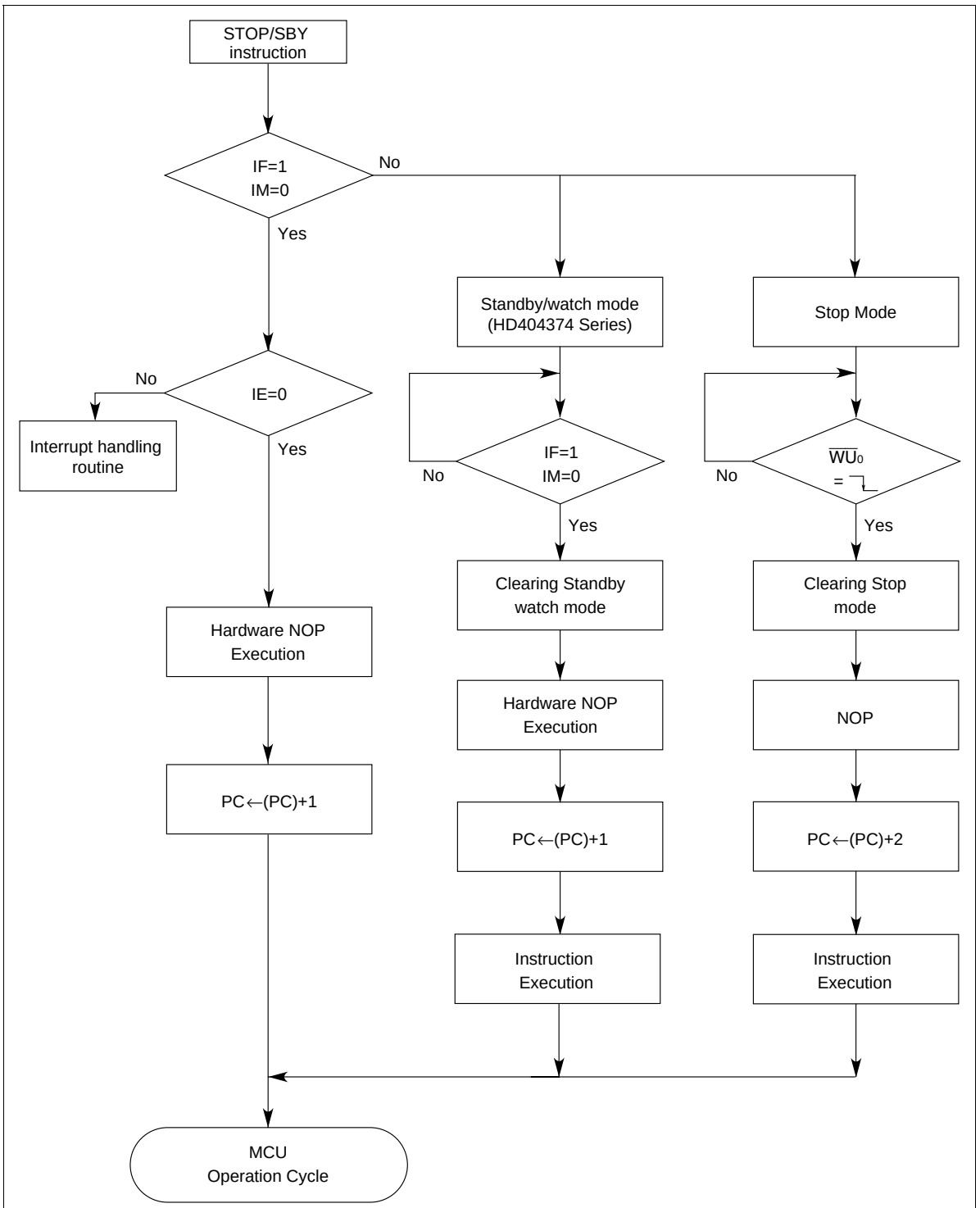



**Figure 16 Direct Transition Timing**

**MCU operation sequence:**
The MCU operates in accordance with the flowchart shown in figure 17. $\overline{\text{RESET}}$ input is asynchronous input, and the MCU immediately enters the reset state upon $\overline{\text{RESET}}$ input, regardless of its current state.

In the low-power mode operation sequence, if a STOP/SBY instruction is executed while the IE flag is cleared and the interrupt flag is set, releasing the relevant interrupt mask, the STOP/SBY instruction is canceled (regarded as NOP) and the next instruction is executed. Therefore, when executing a STOP/SBY instruction, all interrupt flags must be cleared, or interrupts masked, beforehand.




Note: See figure 12, MCU Operation Flowchart, for IF and IM operation.

**Figure 17 MCU Operating Sequence (Low-Power Mode Operation)**

**Usage notes (Applies to HD404374 Series):**
In watch mode and subactive mode, an interrupt will not be detected correctly if the $\overline{INT}_0$ or $\overline{WU}_0$ high or low-level period is shorter than the interrupt frame period.

The MCU's edge sensing method is shown in figure 18. The MCU samples the $\overline{INT}_0$ and $\overline{WU}_0$ signals at regular intervals, and if consecutive sampled values change from high to low, it determines that a falling edge has been generated.

Interrupt detection errors occur since this sampling is performed at the interrupt frame period. If the high-level period of the $\overline{INT}_0$ or $\overline{WU}_0$ signal is within an interrupt frame, as shown in figure 19 (a), the signal will be low at point A and point B, with the result that the falling edge will not be recognized. Similarly, If the low-level period of the $\overline{INT}_0$ or $\overline{WU}_0$ signal is within an interrupt frame, as shown in figure 19 (b), the signal will be high at point A and point B, with the result that the falling edge will not be recognized.

In watch mode and subactive mode, therefore, ensure that the high-level and low-level periods of the $\overline{INT}_0$ and $\overline{WU}_0$ signals is at least as long as the interrupt frame period.

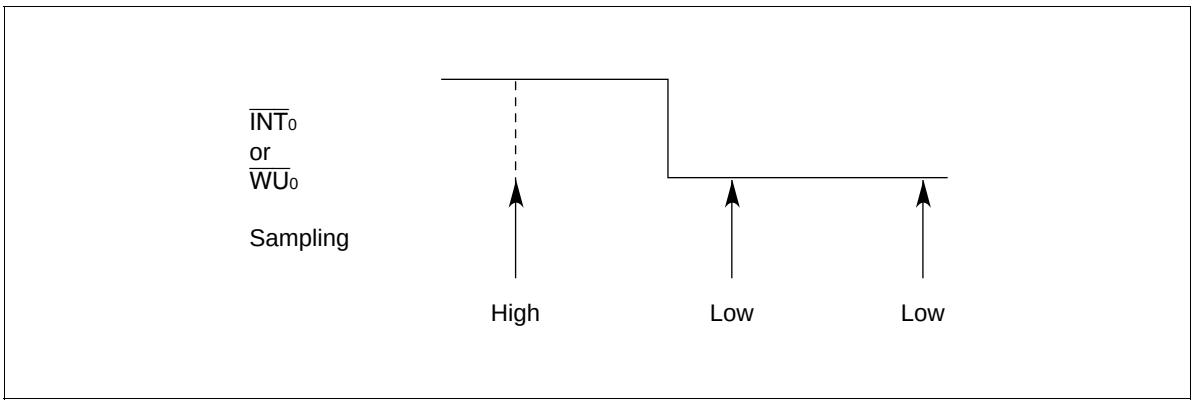



**Figure 18 Edge Sensing Method**

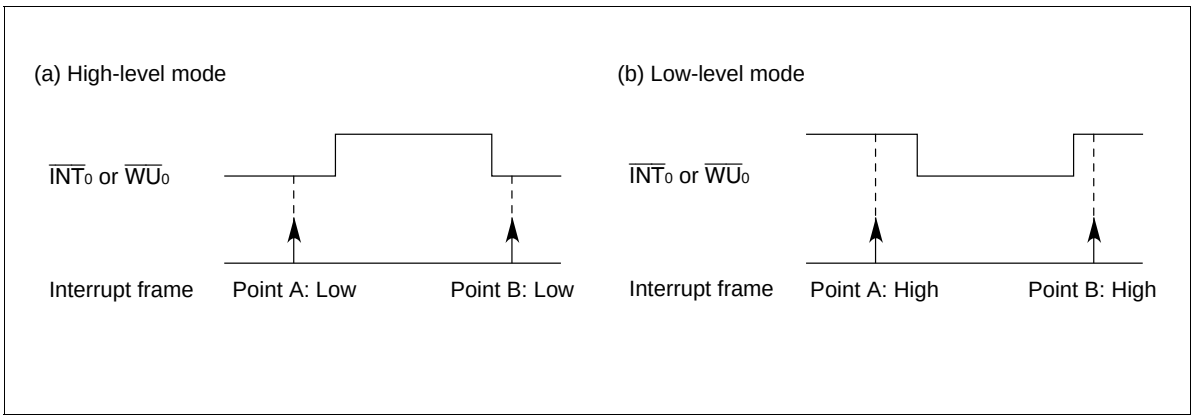


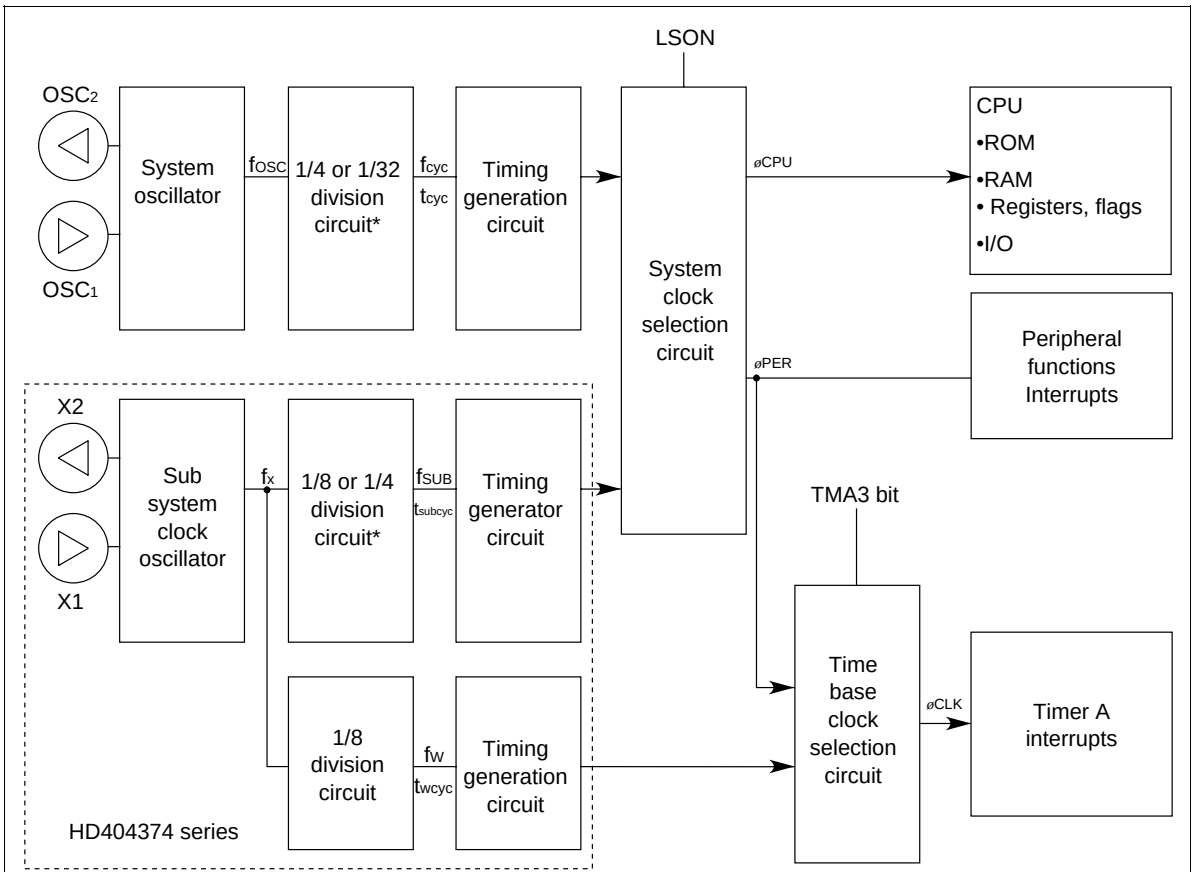

**Figure 19 Sampling Examples**

## Internal Oscillator Circuit

Figure 20 shows the clock pulse generator circuit. As shown in table 21, a ceramic oscillator or crystal oscillator can be connected to OSC1 and OSC2, and a 32.768 kHz crystal oscillator can be connected to X1 and X2. External clock operation is possible for the system oscillator. CR oscillation for system oscillator is possible. CR oscillation function is optional. Set bit 1 (SSR1) of the system clock select register (SSR: $004) according to the frequency of the oscillator connected to OSC1 and OSC2 (figure 22).

Note: If the setting of bit 1 in the system clock select register does not match the frequency of the system oscillator, the subsystem using 32.768 kHz oscillation will not operate correctly in the HD404374 Series.

Also, the CR oscillation frequency differs depending on the operating voltage and resistance value. Set bit 1 of the system clock select register to match the operating frequency. Note that if the frequency being used does not match the setting of bit 1 of the system clock select register, subsystems using the 32.768 kHz oscillation frequency will not operate correctly.




Notes: The division ratio can be selected by setting bit 0 or bit 2 in the system clock select register (SSR:$004).

**Figure 20 Clock Pulse Generator Circuit**

## System Clock Gear Function

The MCU has a built-in system clock gear function that allows the system clock divided by 4 or by 32 to be selected by software for the instruction execution time. Efficient power consumption can be achieved by operating at the divided-by-4 rate when high-speed processing is needed, and at the divided-by-32 rate at the other times. Figure 21 shows the system clock conversion method.

System clock conversion from division-by-4 to division-by-32 is performed as follows. First, make the division-by-32 setting (SSR0 write), then set the gear enable flag (GEF: $021,3). This flag is used to distinguish between gear conversion and a transition to standby mode. Next, execute an SBY instruction. When the gear enable flag is not set, standby mode is entered; when this flag is set, gear conversion mode is entered. In this case a transition is made to standby mode for the duration of the gear conversion, but after the synchronization time has elapsed, a transition is made automatically to active mode. As soon as the transition is made to active mode, the gear enable flag is reset.

The same procedure is used for conversion from division-by-32 to division-by-4.

Clear all interrupts, then disable interrupts, before carrying out gear conversion. Incorrect operation may result if an interrupt is generated during gear conversion.

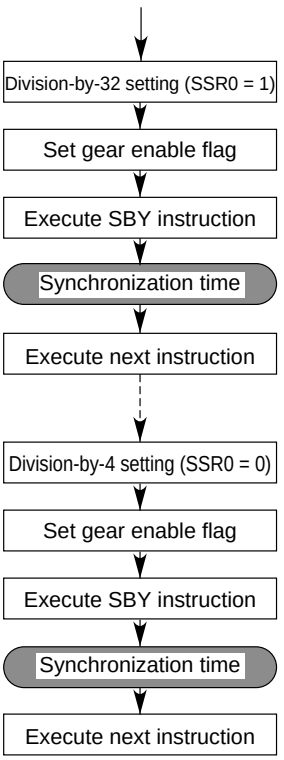



**Figure 21 System Clock Division Ratio Conversion Flowchart**

Make sure to set bit 3 of the system clock select register to 1 if the HD404374 series is being used without the subsystem clock, and on the HD404384, HD404389, HD404082, and HD404084 series. The microcomputer will malfunction if the setting is not 1.

System clock select register (SSR: $004)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | SSR3 | SSR2* | SSR1* | SSR0 |

System clock division ratio switch

| | |
|---|---|
| 0 | Division-by-4 ($f_{cyc}$ - $f_{OSC}$/4) |
| 1 | Division-by-32 ($f_{cyc}$ - $f_{OSC}$/32) |

System clock division ratio switch

| | |
|---|---|
| 0 | $f_{osc}$=0.4–1.0MHz |
| 1 | $f_{osc}$=1.6–8.5MHz |

Subsystem clock division ratio switch

| | |
|---|---|
| 0 | $f_{SUB}$=fx/8 |
| 1 | $f_{SUB}$=fx/4 |

Subsystem clock stop setting
(HD404374 Series)

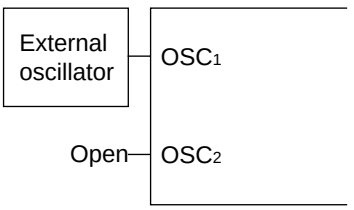
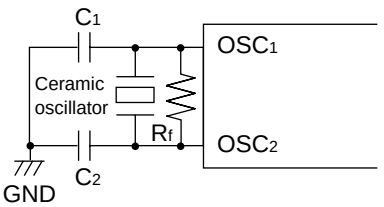
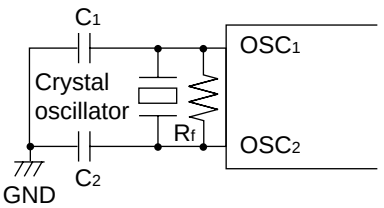
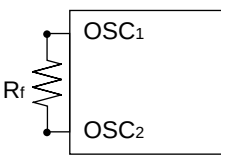
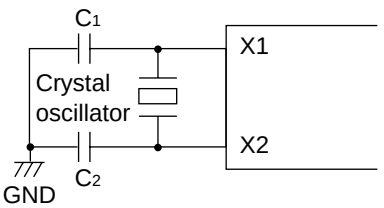
| | |
|---|---|
| 0 | Subsystem clock operates in stop mode |
| 1 | Subsystem clock stops in stop mode |

This bit must be set to 1 following power-on and reset if the HD404374 series is being used without the subsystem clock, and on the HD404384, HD404389, HD404082, and HD404084 series. If it is set to 0 (the initial value), malfunctioning may occur in the stop mode.

Note: * Applies to HD404374 Series.
The CR oscillation frequency differs depending on the operating voltage and resistance value. Set SSR1 to match the operating frequency. Note that if the frequency being used does not match the SSR1 setting, subsystems using the 32.768 kHz oscillation frequency will not operate correctly.

**Figure 22 System Clock Select Register**

**Table 21 Oscillator Circuit Examples**

| | Circuit Structure | Circuit Constants |
|---|---|---|
| External clock operation |  | |
| Ceramic oscillator ($OSC_1$, $OSC_2$) |  | Ceramic oscillator: CSA4.00MG (Murata)<br>$R_f$=1MΩ±20%<br>$C_1$=$C_2$=24pF±20% |
| Crystal oscillator ($OSC_1$, $OSC_2$) |  | $R_f$=1MΩ±20%<br>$C_1$=$C_2$=10–20pF±20% |
| CR oscillator*4 ($OSC_1$, $OSC_2$) |  | $R_f$=20kΩ±1% |
| Crystal oscillator (X1, X2) HD404374 Series |  | Crystal: 32.768 kHz: MX38T (Nihon Denpa Kogyo)<br>$C_1$=$C_2$=20pF±20% |

Notes: 1. With a crystal or ceramic oscillator, circuit constants will differ depending on the resonator, stray capacitance in the interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator manufacturer.

2. Make the connections between the $OSC_1$ and $OSC_2$ pins (X1 and X2 pins) and external components as short as possible, and ensure that no other lines cross these lines (see layout example in figure 23).

3. When 32.768 kHz crystal oscillation is not used, fix the X1 pin at $V_{CC}$ and leave the X2 pin open.

4. Applies to HD40C4372, HD40C4374, HD40C4382, HD40C4384, HD40C4388, HD40C4389, HD40C4081, HD40C4082, HCD40C4082, HD40C4084, HCD40C4084, HD407C4374 and HD407C4384.

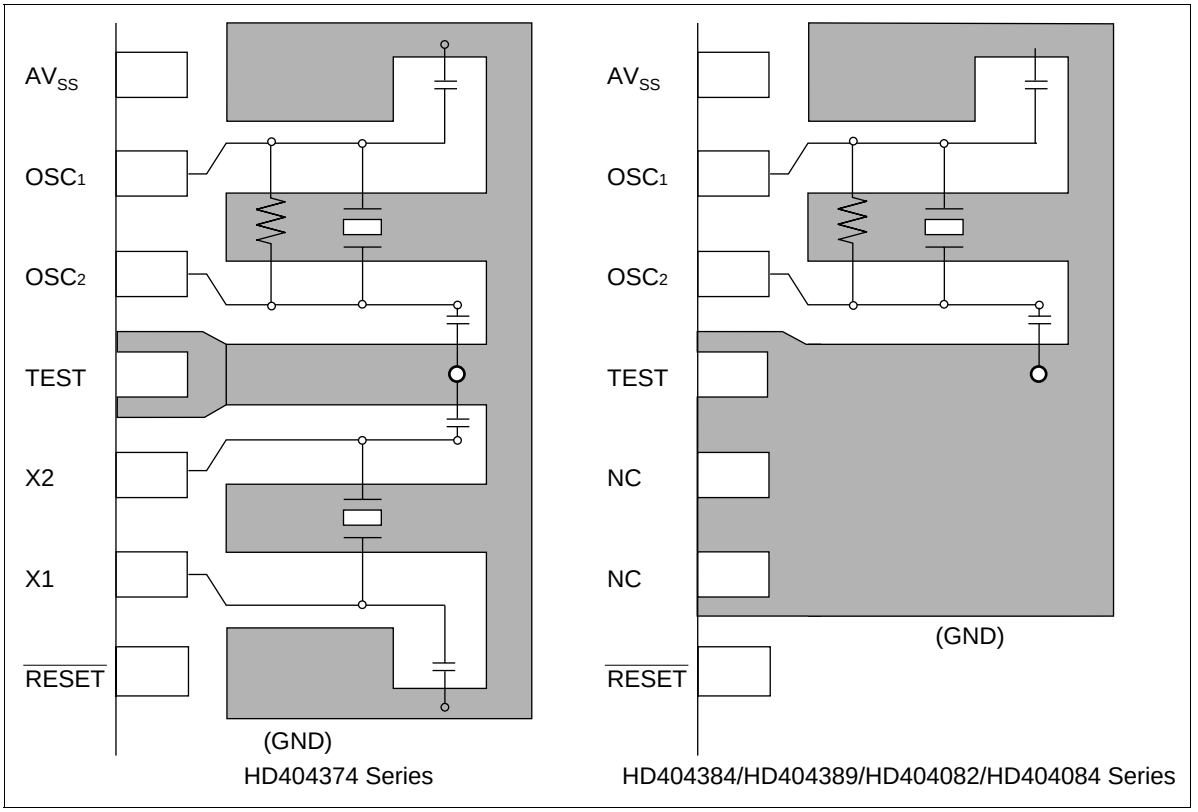



**Figure 23 Typical Layouts of Crystal and Ceramic Oscillator**

## Input/Output

The MCU has 20 input/output pins ($D_0$ to $D_9$, R0, $R1_0$, $R1_3$, $R2_0$ to $R2_2$, $R7_0$ to $R7_3$). The features of these pins are described below.

- The four pins $D_0$ to $D_3$ are source large-current (10 mA max.) I/O pins.
- The four pins $D_4$ to $D_7$ are sink large-current (15 mA max.) I/O pins.
- I/O pins comprise pins ($D_0$, $R0_0$, $R1_0$, $R1_3$, $R2_0$ to $R2_2$, $R7_0$ to $R7_3$) that also have a peripheral function (timer, serial interface, etc.). With these pins, the peripheral function setting has priority over the D port or R port pin setting. When a peripheral function setting has been made for a pin, the pin function and input/output mode will be switched automatically in accordance with that setting.
- Selection of input or output for I/O pins, or selection of the port or peripheral function for pins multiplexed as peripheral function pins, is performed by the program.
- All output of the peripheral function pins are CMOS outputs. The SO pin and $R2_2$ port pin can be designated as NMOS open-drain output by the program.
- A reset clears peripheral function selection. And since the data control registers (DCD, DCR) are also reset, input/output pins go to the high-impedance state.
- Each I/O pin has a built-in pull-up MOS that can be turned on and off individually by the program.

Figure 24 shows the I/O buffer configuration, and table 22 shows I/O pin circuit configuration control by the program.

Table 23 shows the circuit configuration of each I/O pin.

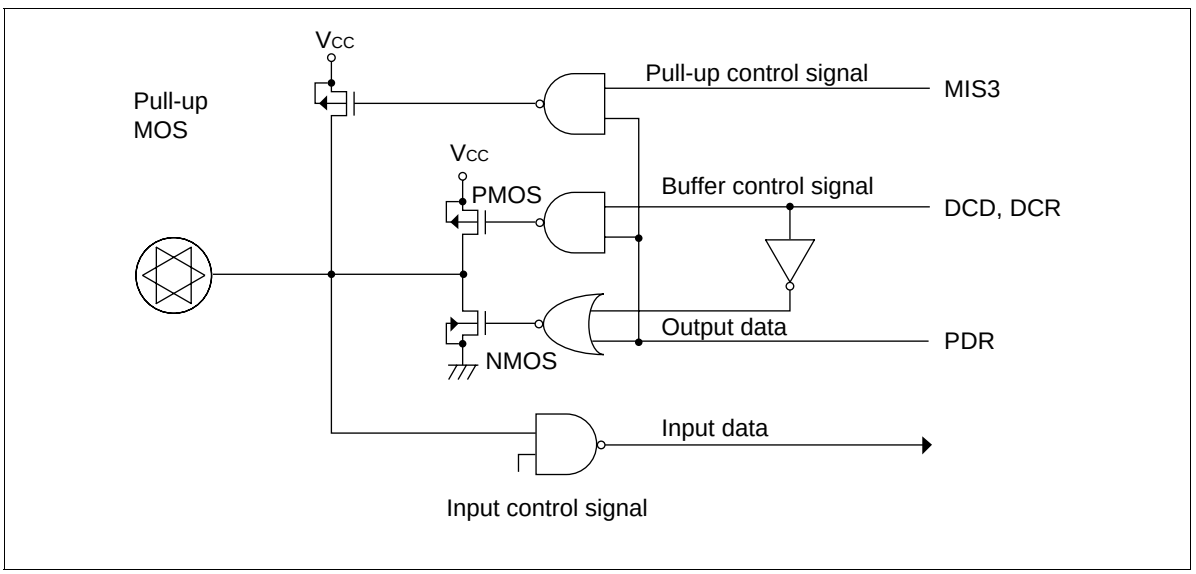


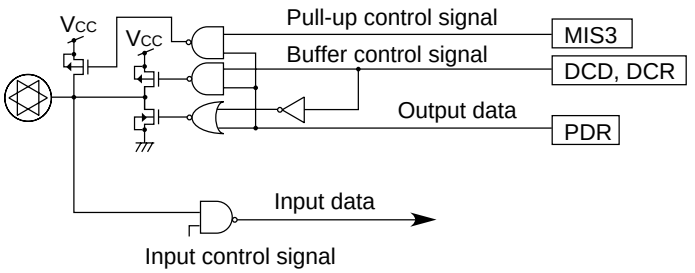
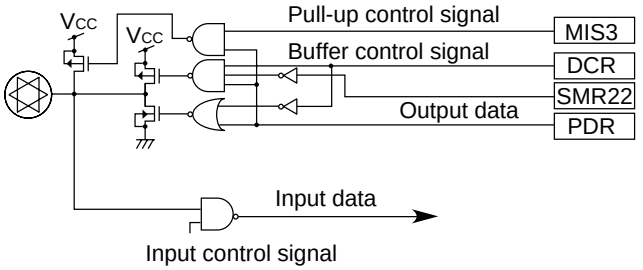
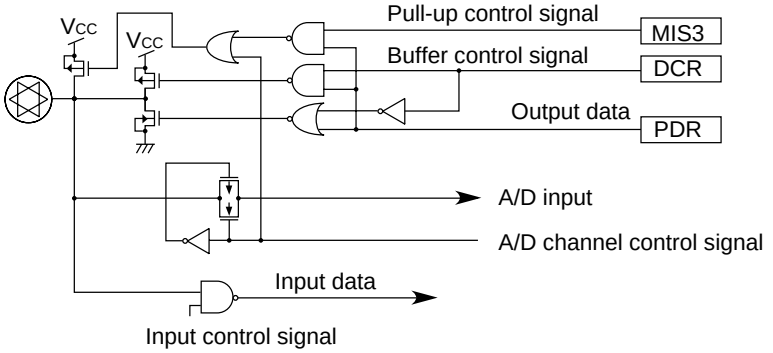

**Figure 24 I/O Pin Circuit Configuration**

**Table 22 Programmable I/O Circuits**

| MIS3 (bit 3 of MIS) | | 0 | | | | 1 | | | |
|---|---|---|---|---|---|---|---|---|---|
| DCD,DCR | | 0 | | 1 | | 0 | | 1 | |
| PDR | | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| CMOS buffer | PMOS | — | — | — | ON | — | — | — | ON |
| | NMOS | — | — | ON | — | — | — | ON | — |
| Pull-up MOS | | — | — | — | — | — | ON | — | ON |

Note: — : OFF

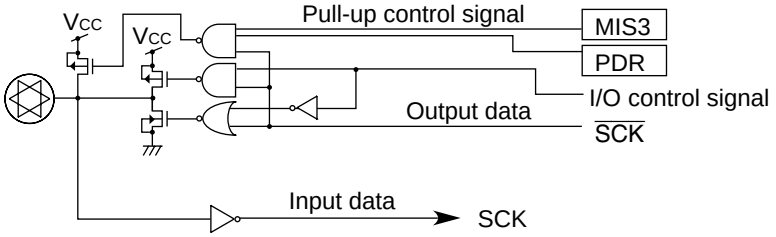
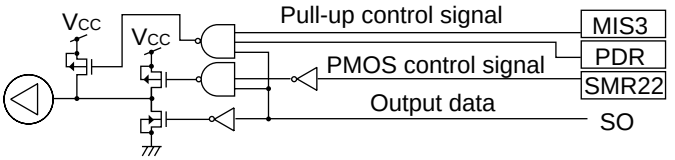
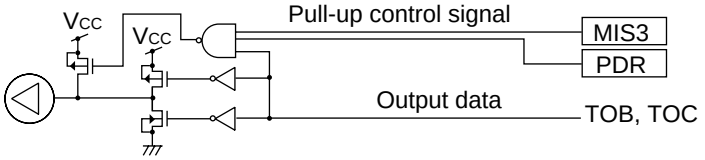
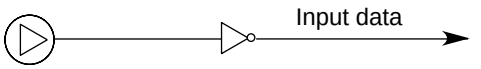
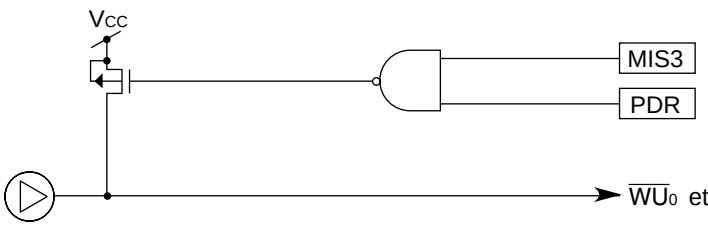
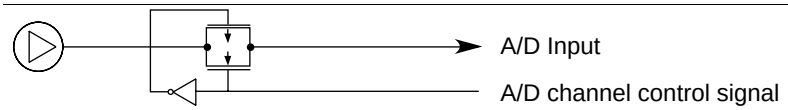
**Table 23 Circuit Configurations of I/O Pins**

| Type | Circuit Configuration | Pins |
|---|---|---|
| I/O pins |  | $D_0$-$D_9$<br>$R0_0$<br>$R1_0$, $R1_3$<br>$R2_0$, $R2_1$ |
| |  | $R2_2$<br>$R7_0$–$R7_3$ *2 |
| |  | $R7_0$-$R7_3$<br>$AN_0$-$AN_3$ *1 |

Notes: In a reset, since the I/O control registers are reset, input/output pins go to the high-impedance state and peripheral function selections are cleared.

1. Applies to HD404374, HD404384, and HD404389 Series.
2. Applies to HD404082 and HD404084 Series.

**Table 23 Circuit Configurations of I/O Pins (cont)**

| Type | | Circuit Configuration | Pins |
|---|---|---|---|
| Peripheral function pins | I/O pins |  | SCK |
| | Output pins |  | SO |
| | |  | TOB, TOC |
| | Input pins |  | RESET |
| | |  | WU0, INT0, EVNB, SI |
| | |  | AN4, AN5 *1 |

Note: In a reset, since the I/O control registers are reset, input/output pins go to the high-impedance state and peripheral function selections are cleared.

1. Applies to HD404389 Series.

**D Port**

The D port consists of 10 I/O pins that are addressed bit-by-bit.

Ports $D_0$ to $D_3$ are source large-current I/O pins, and ports $D_4$ to $D_7$ are sink large-current I/O pins.

The D port can be set and reset by the SED and RED instructions or the SEDD and REDD instructions. Output data is stored in the port data register (PDR) for each pin. The entire D port can be tested by the TD or TDD instruction.

The D port output buffer is turned on and off by the D port data control registers (DCD0 to DCD2: $030 to $032). The DCD registers are mapped onto memory addresses (figure 25).

Port $D_0$ is multiplexed as interrupt input pin $\overline{INT}_0$. Setting as interrupt pin is performed by bit 0 (PMR00) of port mode register 0 (PMR0: $008) (figure 26).

Data control registers (DCD0–2 : $030–$032)
(DCR0–2, 7 : $034–$036, $03B)

| Register Name | Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|
| DCDn (n=0 to 2) | Read/Write | W | W | W | W |
| | Reset | 0 | 0 | 0 | 0 |
| | Bit name | DCDn3 | DCDn2 | DCDn1 | DCDn0 |
| DCRm (m=0 to 2, 7) | Read/Write | W | W | W | W |
| | Reset | 0 | 0 | 0 | 0 |
| | Bit name | DCRm3 | DCRm2 | DCRm1 | DCRm0 |

| All bits | CMOS buffer control |
|---|---|
| 0 | CMOS buffer off (high impedance) |
| 1 | CMOS buffer active |

Correspondence between each bit of DCD and DCR and ports

| Register Name | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|
| DCD0 | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| DCD1 | $D_7$ | $D_6$ | $D_5$ | $D_4$ | 
| DCD2 | ——— | ——— | $D_9$ | $D_8$ |
| DCR0 | ——— | ——— | ——— | $R0_0$ |
| DCR1 | $R1_3$ | ——— | ——— | $R1_0$ |
| DCR2 | ——— | $R2_2$ | $R2_1$ | $R2_0$ |
| DCR7 | $R7_3$ | $R7_2$ | $R7_1$ | $R7_0$ |

**Figure 25 Data Control Registers (DCD, DCR)**

**R Port**

The R port consists of 10 I/O pins that are addressed in 4-bit units.

Input can be performed by means of the LAR and LBR instructions, and output by means of the LRA and LRB instructions. Output data is stored in the port data register (PDR) for each pin.

The R port output buffer is turned on and off by the R port data control registers (DCR0 to DCR2, DCR7: $034 to $036, $03B). The DCR registers are mapped onto memory addresses (figure 25).

Port $R0_0$ is multiplexed as wakeup input pin $\overline{WU}_0$. Setting of this pin as peripheral function pins is performed by port mode register 1 (PMR1: $009) (figure 27).

Port $R1_0$ is multiplexed as peripheral function pin EVNB. Setting of this pin as peripheral function pins is performed by bit 0 (PMR20) of port mode register 2 (PMR2: $00A) (figure 28).

Ports $R1_3$ and $R2_0$ are multiplexed as peripheral function pins TOB, and TOC, respectively. Setting of these pins as peripheral function pins is performed by bits 3 (PMR23) of port mode register 2 (PMR2: $00A) and bit 0 (PMR30) of port mode register 3 (PMR3: $00B)(figures 28 and 29).

Ports $R2_1$ and $R2_2$ are multiplexed as peripheral function pins $\overline{SCK}$ and SI/SO, respectively. Setting of these pins as peripheral function pins is performed by bits 1 to 3 (PMR31 to PMR33) of port mode register 3 (PMR3: $00B) (figure 29).

Ports $R7_0$ to $R7_3$ are multiplexed as peripheral function pins $AN_0$ to $AN_3$ (HD404374, HD404384, and HD404389 Series only). Setting of these pins as peripheral function pins is performed by bits 1 to 3 (AMR1 to AMR3) of the A/D mode register (AMR: $028) (see figure 64 in section 8, A/D Converter).

Port mode register 0 (PMR0: $008)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | —— | —— | —— | W |
| Initial value on reset | —— | —— | —— | 0 |
| Bit name | Not used | Not used | Not used | PMR00 |

| PMR00 | $D_0/\overline{INT}_0$ pin mode selection |
|---|---|
| 0 | $D_0$ |
| 1 | $\overline{INT}_0$ |

**Figure 26 Port Mode Register 0 (PMR0: $008)**

Port mode register 1 (PMR1: $009)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | —— | —— | —— | W |
| Initial value on reset | —— | —— | —— | 0 |
| Bit name | Not used | Not used | Not used | PMR10 |

| PMR10 | $R0_0/\overline{WU}_0$ pin mode selection |
|---|---|
| 0 | $R0_0$ |
| 1 | $\overline{WU}_0$ |

**Figure 27 Port Mode Register 1 (PMR1: $009)**

Port mode register 2 (PMR2: $00A)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | —— | —— | W |
| Initial value on reset | 0 | —— | —— | 0 |
| Bit name | PMR23 | Not used | Not used | PMR20 |

| PMR20 | $R1_0$/EVNB pin mode selection |
|---|---|
| 0 | $R1_0$ |
| 1 | EVNB |

| PMR23 | $R1_3$/TOB pin mode selection |
|---|---|
| 0 | $R1_3$ |
| 1 | TOB |

**Figure 28 Port Mode Register 2 (PMR2: $00A)**

Port mode register 3 (PMR3: $00B)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | PMR33 | PMR32 | PMR31 | PMR30 |

| PMR30 | R2₀/TOC pin mode selection |
|---|---|
| 0 | R2₀ |
| 1 | TOC |

| PMR31 | R2₁/$\overline{\text{SCK}}$ pin mode selection |
|---|---|
| 0 | R2₁ |
| 1 | $\overline{\text{SCK}}$ |

| PMR33 | PMR32 | R2₂/SI/SO pin mode selection |
|---|---|---|
| 0 | * | R2₂ |
| 1 | 0 | SI |
| | 1 | SO |

* : Don't care

**Figure 29 Port Mode Register 3 (PMR3: $00B)**

**Pull-Up MOS Control**

Program-controllable pull-ups MOS are incorporated in all I/O pins.

On/off control of all pull-ups MOS is performed by bit 3 (MIS3) of the miscellaneous register (MIS: $005) and the port data register (PDR) for each pin, enabling the pull-up MOS to be turned on or off independently for each pin (table 22, figure 30).

Except for analog input multiplexed pins, the pull-up MOS on/off setting can be made independent of the setting as an on-chip supporting module pin.

Bit 2 of the miscellaneous register must always be set to 0. The microcomputer will malfunction if it is set to 1.

Miscellaneous register (MIS: $005)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | MIS3 | Not used*1 | MIS1 | MIS0 |

$t_{RC}$ selection
(See figure 15 in the Operating Modes section)

| MIS2 | Setting bit2 |
|---|---|
| 0 | Set to 0 |
| 1 | Use prohibited |

| MIS3 | pull-up MOS control |
|---|---|
| 0 | All pull-ups MOS off |
| 1 | pull-up MOS active |

Note: 1. This bit must always be set to 0. The microcomputer will malfunction if it is set to 1.

**Figure 30 Miscellaneous Register (MIS:$005)**

**Handling of I/O Pins Not Used by User System**

If I/O pins that are not used by the user system are left floating, they may generate noise that can result in chip malfunctions. Therefore, the pin potential must be fixed.

In this case, pull the pins up to $V_{CC}$ with the built-in pull-up MOS or with an external resistor of approximately 100 kΩ.

## Prescalers

The MCU has the following prescalers, S and W (HD404374 Series).

The operating conditions for each prescaler are shown in table 24, and the output supply destinations in figure 31.

Timer A to C input clocks other than external events, and serial transfer clocks other than external clocks are selected from the prescaler outputs in accordance with the respective mode register.

### Prescaler Operation

**Prescaler S (PSS):**
Prescaler S is an 11-bit counter that has the system clock as input. When the MCU is reset, prescaler S is reset to $000, then divides the system clock. Prescaler S operation is stopped by a reset by the MCU, and in stop mode and watch mode[*1]. It does not stop in any other modes.

**Prescaler W (PSW) (HD404374 Series):**
Prescaler W is a counter that has a clock divided from the X1 input (32 kHz crystal oscillation) as input.

When the MCU is reset, prescaler W is reset to $00, then divides the input clock. Prescaler W can also be reset by software.

**Table 24 Prescaler Operating Conditions**

| Prescaler | Input Clock | Reset Conditions | Stop Conditions |
|---|---|---|---|
| Prescaler S | System clock in active and standby modes, subsystem clock in subactive mode*1 | MCU reset, stop mode clearance | MCU reset, stop mode, watch mode*1 |
| Prescaler W | Clock obtained by division-by-8 of 32.768 kHz oscillation by subsystem clock oscillator | MCU reset, software*2 | MCU reset, stop mode |

Notes: 1 Applies to HD404374 Series
2 If bits TMA3 to TMA1 in timer mode register A (TMA) are all set to 1, PSW is cleared to $00.

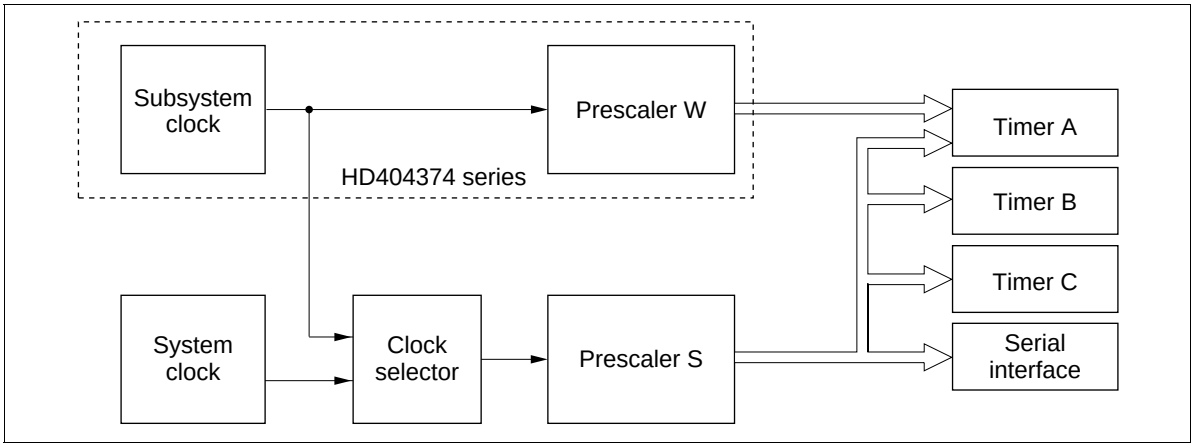



**Figure 31 Prescaler Output Destinations**

## Timers

The MCU incorporates three timers, A to C.

- Timer A: Free-running timer
- Timer B: Multifunctional timer
- Timer C: Multifunctional timer

Timer A is an 8-bit free-running timer. Timers B and C are 8-bit multifunctional timers; Each one of their have the functions shown in table 25 and their operating mode can be set by the program.

**Table 25 Timer Functions**

| Functios | | Timer A | Timer B | Timer C |
|---|---|---|---|---|
| Clock source | Prescaler S | Available | Available | Available |
| | Prescaler W* | Available | — | — |
| | External event | — | Available | — |
| Timer functions | Free-running | Available | Available | Available |
| | Time-base* | Available | — | — |
| | Event counter | — | Available | — |
| | Reload | — | Available | Available |
| | Watchdog | — | — | Available |
| Timer outputs | Toggle | — | Available | Available |
| | PWM | — | Available | Available |

Note: — implies not available
* Applies to HD404374 Series

### Timer A

#### Timer A Functions

Timer A has the following functions.

- Free-running timer
- Realtime clock time base

The block diagram of timer A is shown in figure 32.

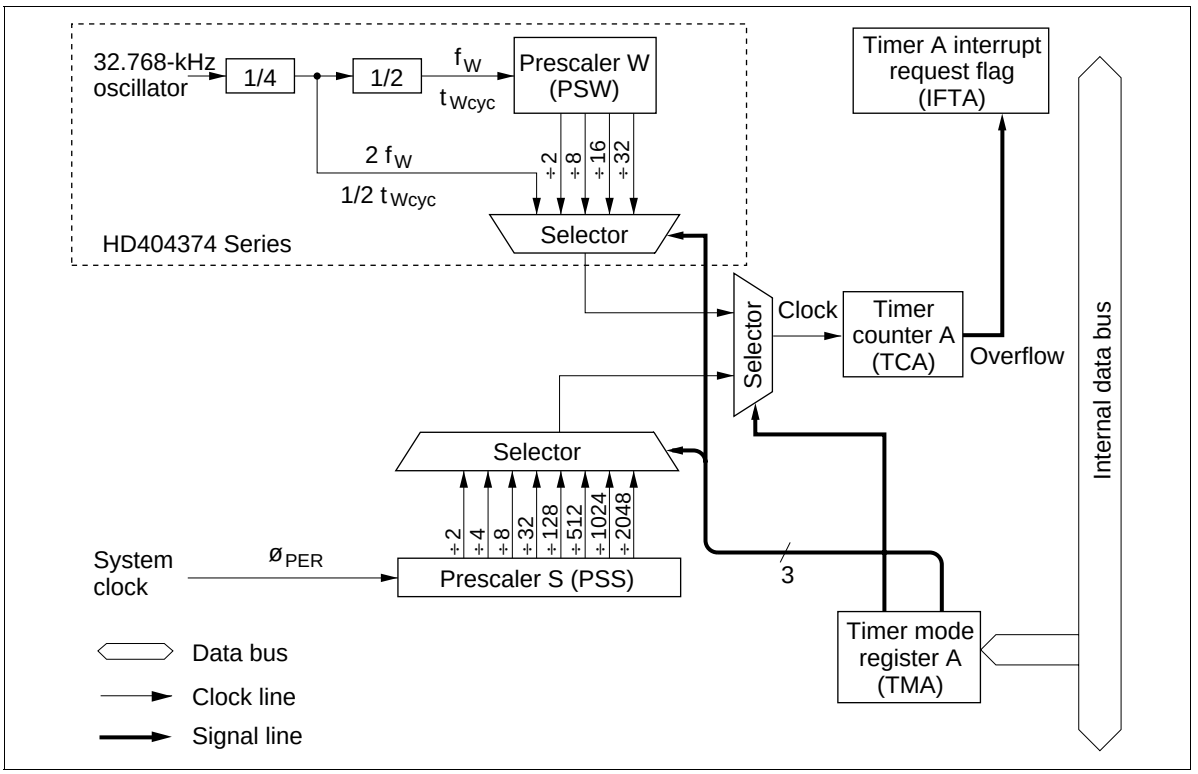



**Figure 32 Timer A Block Diagram**

**Timer A Operation**

**Free-running timer operation:**
The timer A input clock is selected by timer mode register A (TMA: $00F).

Timer A is reset to $00 by an MCU reset, and counts up each time the input clock is input. When the input clock is input after the timer A value reaches $FF, overflow output is generated, and the timer A value becomes $00. The generated overflow output sets the timer A interrupt request flag (IFTA: $002,0). Timer A continues counting up after the count value returns to $00, so that an interrupt is generated regularly every 256 input clock cycles.

**Realtime clock time base operation (HD404374 Series):**
Timer A can be used as the realtime clock time base by setting bit 3 (TMA3) of timer mode register A to 1. As the prescaler W output is input to timer/counter A, interrupts are generated with accurate timing using the 32.768 kHz crystal oscillator as the basic clock.

When timer A is used as the realtime clock time base, prescaler W and timer/counter A can be reset to $00 by the program.

**Timer A Register**

Timer A operation is set by means of the following register.

**Timer mode register A (TMA: $00F):**
Timer mode register A (TMA: $00F) is a 4-bit write-only register. Timer A operation and input clock selection are set as shown in figure 33.

Timer mode register A (TMA: $00F)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | TMA3*4 | TMA2 | TMA1 | TMA0 |

| TMA3*4 | TMA2 | TMA1 | TMA0 | Source prescaler | Input clock period | Operating mode |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | PSS | 2,048 $t_{cyc}$ | Timer A mode |
| | | | 1 | PSS | 1,024 $t_{cyc}$ | |
| | | 1 | 0 | PSS | 512 $t_{cyc}$ | |
| | | | 1 | PSS | 128 $t_{cyc}$ | |
| | 1 | 0 | 0 | PSS | 32 $t_{cyc}$ | |
| | | | 1 | PSS | 8 $t_{cyc}$ | |
| | | 1 | 0 | PSS | 4 $t_{cyc}$ | |
| | | | 1 | PSS | 2 $t_{cyc}$ | |
| 1 | 0 | 0 | 0 | PSW | 32 $t_{wcyc}$ | Time base mode |
| | | | 1 | PSW | 16 $t_{wcyc}$ | |
| | | 1 | 0 | PSW | 8 $t_{wcyc}$ | |
| | | | 1 | PSW | 2 $t_{wcyc}$ | |
| | 1 | 0 | 0 | PSW | 1/2 $t_{wcyc}$ | |
| | | | 1 | Not Used | | |
| | | 1 | x | PSW, TCA reset | | |

x : Don't care

Notes : 1. $t_{wcyc}$ = 244.14 µs (using 32.768 kHz crystal oscillator)
2. Timer/counter overflow output period (s) = input clock period (s) × 256.
3. The division ratio must not be changed while time base mode is being used, as this will result in an error in the overflow period.
4. Applies to HD404374 Series. In HD404384, HD404389, HD404082 and HD404084 Series, write as 0.

**Figure 33 Timer Mode Register A (TMA)**

**Timer B**

**Timer B Functions:** Timer B has the following functions.

- Free-running/reload timer
- External event counter
- Timer output operation (toggle output, PWM output)

The block diagram of timer B is shown in figure 34.

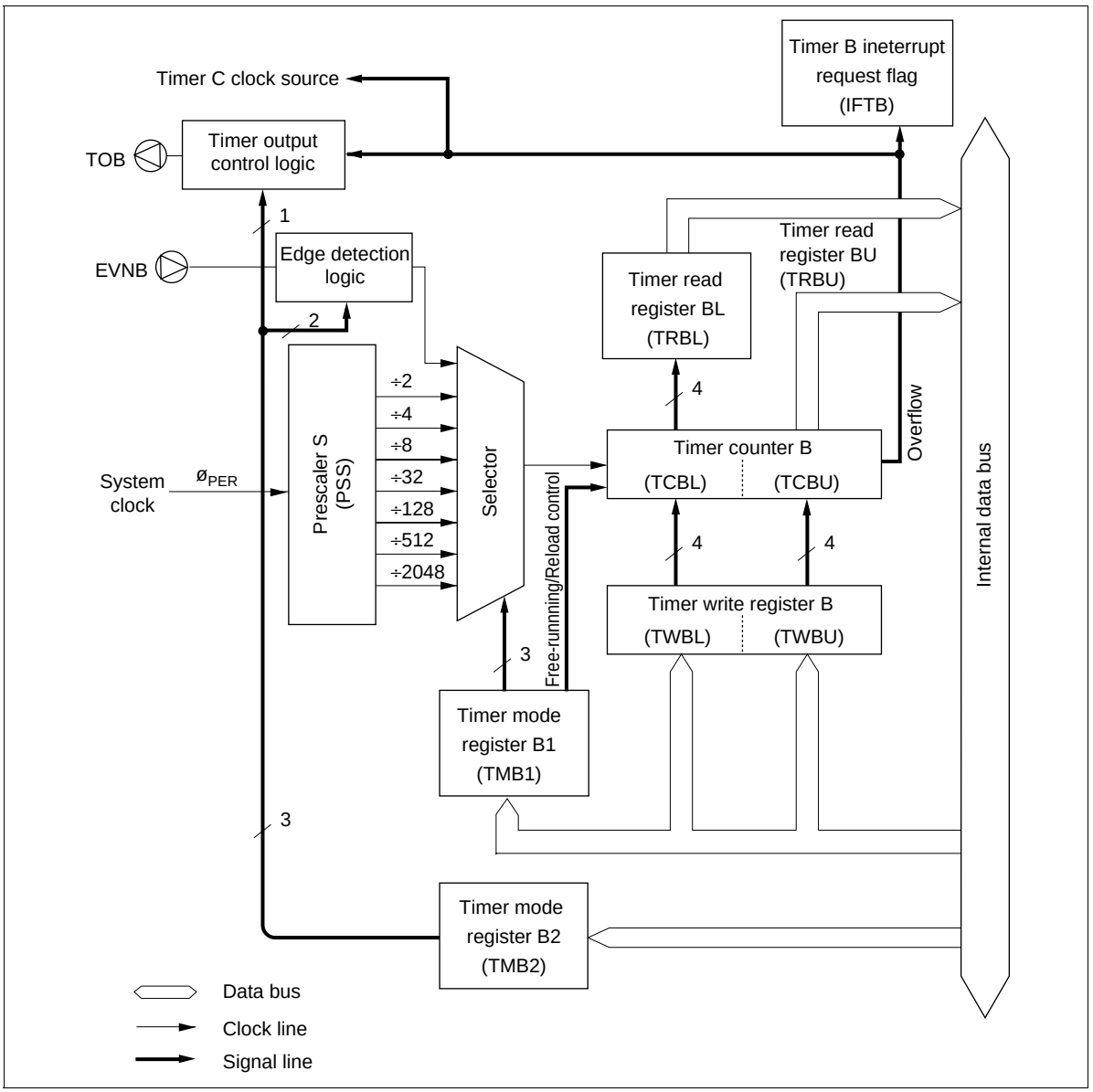



**Figure 34 Timer B Block Diagram**

**Timer B Operation**

- Free-running/reload timer:

  Free-running/reload timer operation, the input clock source, and the prescaler division ratio are selected by means of timer mode register B1 (TMB1).

  Timer B is initialized to the value written to timer write register B (TWBL, TWBU) by software, and counts up by 1 each time the input clock is input. When the input clock is input after the timer B value reaches $FF, overflow output is generated. Timer B is then set to the value in timer write register B if the reload timer function is selected, or to $00 if the free-running timer function is selected, and starts counting up again.

  Overflow output sets the timer B interrupt request flag (IFTB). This flag is reset by the program or by an MCU reset.

  For details, see figure 3, Interrupt Control Bit and Register Flag Area Configuration, and table 1, Initial Values after MCU Reset.

- External event counter operation:

  When external event input is designated for the input clock, timer B operates as an external event counter. When external event input is used, the $R1_0$/EVNB pin is designated as the EVNB pin by port mode register 2 (PMR2).

  The external event detected edge for timer B can be designated as a falling edge, rising edge, or both falling and rising edges in the input signal by means of timer mode register B2 (TMB2). If both falling and rising edges are selected, the input signal falling and rising edge interval should be at least 2tcyc.

  Timer B counts up by 1 each time a falling edge is detected in the signal input at the EVNB pin. Other operations are the same as for the free-running/reload timer function.

- Timer output operation:

  With timer B, the R13/TOB pin is designated as the TOB pin by the setting of bit 3 of port mode register 2 (PMR2), and toggle waveform output or PWM waveform output can be selected by timer mode register B2 (TMB2).

  — Toggle output:

    With toggle output, the output level is changed upon input of the next clock pulse after the timer B value reaches $FF. Use of this function in combination with the reload timer allows a clock signal with any period to be output, enabling it to be used as buzzer output. The output waveform is shown in figure 35 (1).

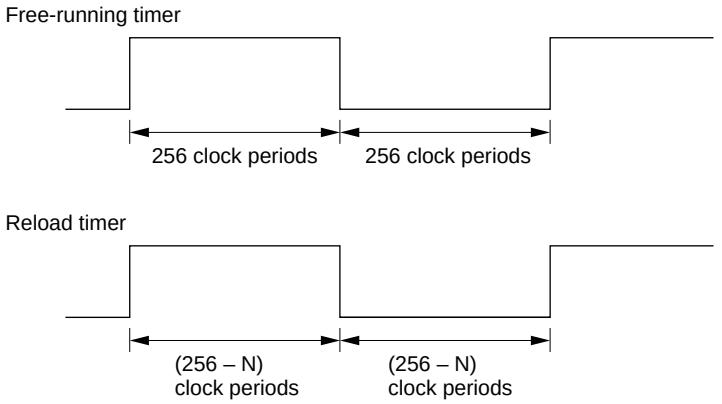
  — PWM output:

    With PWM output, variable-duty pulses are output. The output waveform is as shown in figure 35 (2), according to the contents of timer mode register B1 (TMB1) and timer write register B (TWBL, TWBU). When the waveform is output with bit 3 (TMB13) of timer mode register B1 cleared to 0, the write to timer write register B to change the duty is effective from the next frame, whereas if the waveform is output with the TMB13 bit set to 1 (reload setting), the next frame is output immediately after the timer write register write.

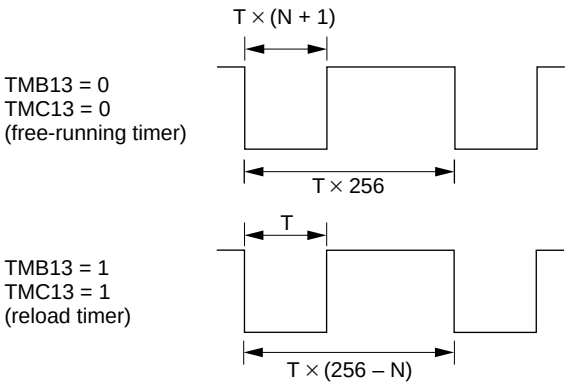
- Module standby:

  With timer B, the supply of the system clock to the timer/counter can be halted by setting bit 0 of module standby register 1 (MSR1: $00D) to 1. In the module standby state, the mode register value is retained but the counter value is not guaranteed.

(1) Toggle output waveform (timer B, timer C)




(2) PWM output waveform (timer B, timer C)




Notes: T: Counter input clock period
(The clock input source and division ratio are controlled by timer mode register B1 and timer mode register C1.)
N: Value in timer write register B or timer write register C
When N = 255 (= $FF), PWM output is always fixed at the timer low level.)

**Figure 35 Timer Output Waveforms**

**Timer B Registers**

Timer B operation setting and timer B value reading/writing is controlled by the following registers.

Timer mode register B1 (TMB1: $010)

Timer mode register B2 (TMB2: $011)

Timer write register B (TWBL: $012, TWBU: $013)

Timer read register B (TRBL: $012, TRBU: $013)

Port mode register 2 (PMR2: $00A)

Module standby register 1 (MSR1: $00D)

- Timer mode register B1 (TMB1: $010):

  Timer mode register B1 (TMB1) is a 4-bit write-only register, used to select free-running/reload timer operation and the input clock as shown in figure 36.

  Timer mode register B1 (TMB1) is reset to $0 by an MCU reset:

  A modification of timer mode register B1 (TMB1) becomes effective after execution of two instructions following the timer mode register B1 (TMB1) write instruction. The program must provide for timer B initialization by writing to timer write register B (TWBL, TWBU) to be executed after the post-modification mode has become effective.

Timer mode register B1 (TMB1: $010)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | TMB13 | TMB12 | TMB11 | TMB10 |

| TMB12 | TMB11 | TMB10 | Input clock period and input clock source |
|---|---|---|---|
| 0 | 0 | 0 | 2,048 $t_{cyc}$ |
| | | 1 | 512 $t_{cyc}$ |
| | 1 | 0 | 128 $t_{cyc}$ |
| | | 1 | 32 $t_{cyc}$ |
| 1 | 0 | 0 | 8 $t_{cyc}$ |
| | | 1 | 4 $t_{cyc}$ |
| | 1 | 0 | 2 $t_{cyc}$ |
| | | 1 | R10/EVNB (external event input) |

| TMB13 | Free-running/reload timer |
|---|---|
| 0 | Free-running timer |
| 1 | Reload timer |

**Figure 36 Timer Mode Register B1 (TMB1)**

- Timer mode register B2 (TMB2: $011):

  Timer mode register B2 (TMB2) is a 3-bit write-only register, used to select the timer B output mode and EVNB pin detected edge as shown in figure 37.

  Timer mode register B2 (TMB2) is reset to $0 by an MCU reset.

Timer mode register B2 (TMB2: $011)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | — | W | W | W |
| Initial value on reset | — | 0 | 0 | 0 |
| Bit name | — | TMB22 | TMB21 | TMB20 |

| TMB21 | TMB20 | EVNB pin detected edge |
|---|---|---|
| 0 | 0 | Not detected |
| | 1 | Falling edge detection |
| 1 | 0 | Rising edge detection |
| | 1 | Both rising and falling edge detection |

| TMB22 | Timer B output waveform |
|---|---|
| 0 | Toggle output |
| 1 | PWM output |

**Figure 37 Timer Mode Register B2 (TMB2)**

- Timer write register B (TWBL: $012, TWBU:$013):

  Timer write register B (TWBL, TWBU) is a write-only register composed of a lower digit (TWBL) and an upper digit (TWBU) (figures 38 and 39).

  The lower digit (TWBL) of timer write register B is reset to $0 by an MCU reset, while the upper digit (TWBU) is undetermined.

  Timer B can be initialized by writing to timer write register B (TWBL, TWBU). To write the data, first write the lower digit (TWBL). The lower digit write does not change the timer B value. Next, write the upper digit (TWBU). Timer B is then initialized to the timer write register B (TWBL, TWBU) value. When writing to timer write register B (TWBL, TWBU) from the second time onward, if it is not necessary to change the lower digit (TWBL) reload value, timer B initialization is completed by the upper digit write alone.

Timer write register B (lower) (TWBL: $012)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | TWBL3 | TWBL2 | TWBL1 | TWBL0 |

**Figure 38 Timer Write Register B (Lower) (TWBL)**

Timer write register B (upper) (TWBU: $013)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name | TWBU3 | TWBU2 | TWBU1 | TWBU0 |

**Figure 39 Timer Write Register B (Upper) (TWBU)**

- Timer read register B (TRBL: $012, TRBU: $013):

  Timer read register B (TRBL, TRBU) is a read-only register composed of a lower digit (TRBL) and an upper digit (TRBU) from which the value of the upper digit of timer B is read directly (figures 40 and 41).

  First, read the upper digit (TRBU) of timer read register B. The current value of the timer B upper digit is read and, at the same time, the value of the timer B lower digit is latched in the lower digit (TRBL) of timer read register B. The timer B value is obtained when the upper digit (TRBU) of timer read register B is read by reading the lower digit (TRBL) of timer read register B.

Timer read register B (lower) (TRBL: $012)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R | R | R | R |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name | TRBL3 | TRBL2 | TRBL1 | TRBL0 |

**Figure 40 Timer Read Register B (Lower) (TRBL)**

Timer read register B (upper) (TRBU: $013)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R | R | R | R |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name | TRBU3 | TRBU2 | TRBU1 | TRBU0 |

**Figure 41 Timer Read Register B (Upper) (TRBU)**

- Port mode register 2 (PMR2: $00A):

  Port mode register 2 (PMR2) is a write-only register used to set the function of the $R1_0$/EVNB and $R1_3$/TOB pins as shown in figure 42.

  Port mode register 2 (PMR2) is reset to $0 by an MCU reset.

Port mode register 2 (PMR2: $00A)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | — | — | W |
| Initial value on reset | 0 | — | — | 0 |
| Bit name | PMR23 | Not used | Not used | PMR20 |

| PMR20 | $R1_0$/EVNB pin mode selection |
|---|---|
| 0 | $R1_0$ |
| 1 | EVNB |

| PMR23 | $R1_3$/TOB pin mode selection |
|---|---|
| 0 | $R1_3$ |
| 1 | TOB |

**Figure 42 Port Mode Register 2 (PMR2: $00A)**

- Module standby register 1 (MSR1: $00D):

  Module standby register 1 (MSR1) is a write-only register used to designate supply or stopping of the clock to timer B as shown in figure 43.

  Module standby register 1 (MSR1) is reset to $0 by an MCU reset.

Module standby register 1 (MSR1: $00D)

| Bit | 3 | 2 | *1* | 0 |
|---|---|---|---|---|
| Read/Write | — | — | W | W |
| Initial value on reset | — | — | 0 | 0 |
| Bit name | Not used | Not used | MSR11 | MSR10 |

| MSR10 | Timer B clock supply control |
|---|---|
| 0 | Supplied |
| 1 | Stopped |

| MSR11 | Timer C clock supply control |
|---|---|
| 0 | Supplied |
| 1 | Stopped |

**Figure 43 Module Standby Register 1 (MSR1)**

**Timer C**

**Timer C Functions:Timer :** C has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (toggle output, PWM output)

The block diagram of timer C is shown in figure 44.

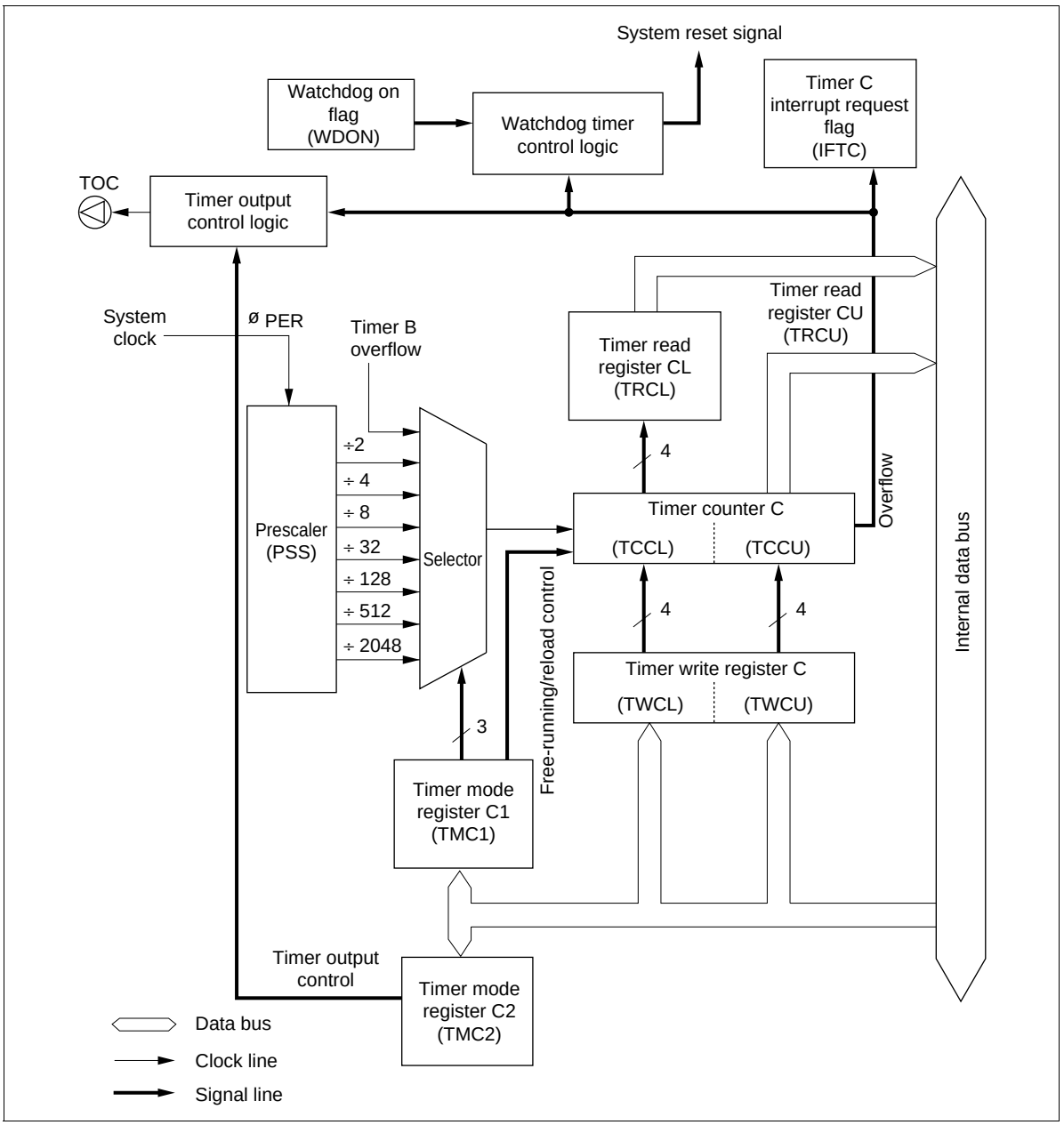



**Figure 44 Timer C Block Diagram**

**Timer C Operation**

- Free-running/reload timer:

  Free-running/reload timer operation, the input clock source, and the prescaler division ratio are selected by means of timer mode register C1 (TMC1).

  Timer C is initialized to the value written to timer write register C (TWCL, TWCU) by software, and counts up by 1 each time the input clock is input. When the input clock is input after the timer C value reaches $FF, overflow output is generated. Timer C is then set to the value in timer write register C (TWCL, TWCU) if the reload timer function is selected, or to $00 if the free-running timer function is selected, and starts counting up again.

  Overflow output sets the timer C interrupt request flag (IFTC). This flag is reset by the program or by an MCU reset.

  For details, see figure 3, Interrupt Control Bit and Register Flag Area Configuration, and table 1, Initial Values after MCU Reset.

- 16-bit timer operation:

  When timer B overflow flag is selected as the clock source, timer C can be used as a 16-bit timer that counts the timer B clock source pulses. In this case, since the timer B and timer C free-running/reload settings are independent, the settings should be made to suit the purpose.

- Watchdog timer operation:

  By using the timer C overflow output, timer C can be used as a watchdog timer for detecting program runaway. The watchdog timer is enabled when the watchdog on flag (WDON) is set to 1, and generates an MCU reset when timer C overflows. Usually, timer C initialization is performed by the program before the timer C value reaches $FF, so controlling program runaway.

- Timer output operation:

  With timer C, the $R2_0$/TOC pin is designated as the TOC pin by setting bit 0 of port mode register 3 (PMR3) to 1, and toggle waveform output or PWM waveform output can be selected by timer mode register C2 (TMC2).

  — Toggle output

    The operation is similar to that for timer B toggle output.

  — PWM output

    The operation is similar to that for timer B PWM output.

- Module standby:

  The operation is similar to that for timer B module standby.

**Timer C Registers**

Timer C operation setting and timer C value reading/writing is controlled by the following registers.

Timer mode register C1 (TMC1: $014)

Timer mode register C2 (TMC2: $015)

Timer write register C (TWCL: $016, TWCU: $017)

Timer read register C (TRCL: $016, TRCU: $017)

Port mode register 3 (PMR3: $00B)

Module standby register 1 (MSR1: $00D)

- Timer mode register C1 (TMC1: $014):

  Timer mode register C1 (TMC1) is a 4-bit write-only register, used to select free-running/reload timer operation, the input clock, and the prescaler division ratio as shown in figure 45.

  Timer mode register C1 (TMC1) is reset to $0 by an MCU reset.

  A modification of timer mode register C1 (TMC1) becomes effective after execution of two instructions following the timer mode register C1 (TMC1) write instruction. The program must provide for timer C initialization by writing to timer write register C (TWCL, TWCU) to be executed after the post-modification mode has become effective.

Timer mode register C1 (TMC1: $014)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | TMC13 | TMC12 | TMC11 | TMC10 |

| TMC12 | TMC11 | TMC10 | Input clock period |
|---|---|---|---|
| 0 | 0 | 0 | 2,048 $t_{cyc}$ |
| | | 1 | 512 $t_{cyc}$ |
| | 1 | 0 | 128 $t_{cyc}$ |
| | | 1 | 32 $t_{cyc}$ |
| 1 | 0 | 0 | 8 $t_{cyc}$ |
| | | 1 | 4 $t_{cyc}$ |
| | 1 | 0 | 2 $t_{cyc}$ |
| | | 1 | Timer B overflow |

| TMC13 | Free-running/reload timer |
|---|---|
| 0 | Free-running timer |
| 1 | Reload timer |

**Figure 45 Timer Mode Register C1 (TMC1)**

- Timer mode register C2 (TMC2: $015):

  Timer mode register C2 (TMC2) is a 1-bit write-only register, used to select the timer C output mode as shown in figure 46.

  Timer mode register C2 (TMC2) is reset to $0 by an MCU reset.

Timer mode register C2 (TMC2: $015)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | — | W | — | — |
| Initial value on reset | — | 0 | — | — |
| Bit name | — | TMC22 | — | — |

| TMC22 | Timer C output waveform |
|---|---|
| 0 | Toggle output |
| 1 | PWM output |

**Figure 46 Timer Mode Register C2 (TMC2)**

- Timer write register C (TWCL: $016, TWCU: $017):

  Timer write register C (TWCL, TWCU) is a write-only register composed of a lower digit (TWCL) and an upper digit (TWCU) (figures 47 and 48).

  Timer write register C (TWCL, TWCU) operation is similar to that for timer write register B (TWBL, TWBU).

Timer write register C (lower) (TWCL: $016)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | TWCL3 | TWCL2 | TWCL1 | TWCL0 |

**Figure 47 Timer Write Register C (Lower) (TWCL)**

Timer write register C (upper) (TWCU: $017)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name | TWCU3 | TWCU2 | TWCU1 | TWCU0 |

**Figure 48 Timer Write Register C (Upper) (TWCU)**

- Timer read register C (TRCL: $016, TRCU: $017):

  Timer read register C (TRCL, TRCU) is a read-only register composed of a lower digit (TRCL) and an upper digit (TRCU) from which the value of the upper digit of timer C is read directly (figures 49 and 50).

  Timer read register C (TRCL, TRCU) operation is similar to that for timer read register B (TRBL, TRBU).

Timer read register C (lower) (TRCL: $016)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R | R | R | R |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name | TRCL3 | TRCL2 | TRCL1 | TRCL0 |

**Figure 49 Timer Read Register C (Lower) (TRCL)**

Timer read register C (upper) (TRCU: $017)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R | R | R | R |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name | TRCU3 | TRCU2 | TRCU1 | TRCU0 |

**Figure 50 Timer Read Register C (Upper) (TRCU)**

- Port mode register 3 (PMR3: $00B):

  Port mode register 3 (PMR3) is a write-only register used to set the function of the $R2_0$/TOC pin as shown in figure 51.

  Port mode register 3 (PMR3) is reset to $0 by an MCU reset.

Port mode register 3 (PMR3: $00B)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | PMR33 | PMR32 | PMR31 | PMR30 |

| PMR30 | $R2_0$/TOC pin mode selection |
|---|---|
| 0 | $R2_0$ |
| 1 | TOC |

| PMR31 | $R2_1$/$\overline{SCK}$ pin mode selection |
|---|---|
| 0 | $R2_1$ |
| 1 | $\overline{SCK}$ |

| PMR33 | PMR32 | $R2_2$/SI/SO pin mode selection |
|---|---|---|
| 0 | * | $R2_2$ |
| 1 | 0 | SI |
| | 1 | SO |

* : Don't care

**Figure 51 Port Mode Register 3 (PMR3)**

- Module standby register 1 (MSR1: $00D):

  Module standby register 1 (MSR1) is a write-only register used to designate supply or stopping of the clock to timer C as shown in figure 43.

  Module standby register 1 (MSR1) is reset to $0 by an MCU reset.

## Serial Interface

The serial interface serially transfers and receives 8-bit data, and includes the following features.

- Multiple transmit clock sources
  - External clock
  - Internal prescaler output clock
  - System clock
- Output level control in idle states

Five registers, an octal counter, and a multiplexer are also configured for the serial interface as follows.

- Serial data register (SRL: $026, SRU: $027)
- Serial mode register 1 (SMR1: $024)
- Serial mode register 2 (SMR2: $025)
- Port mode register 3 (PMR3: $00B)
- Octal counter (OC)
- Selector

The block diagram of the serial interface is shown in figure 52.

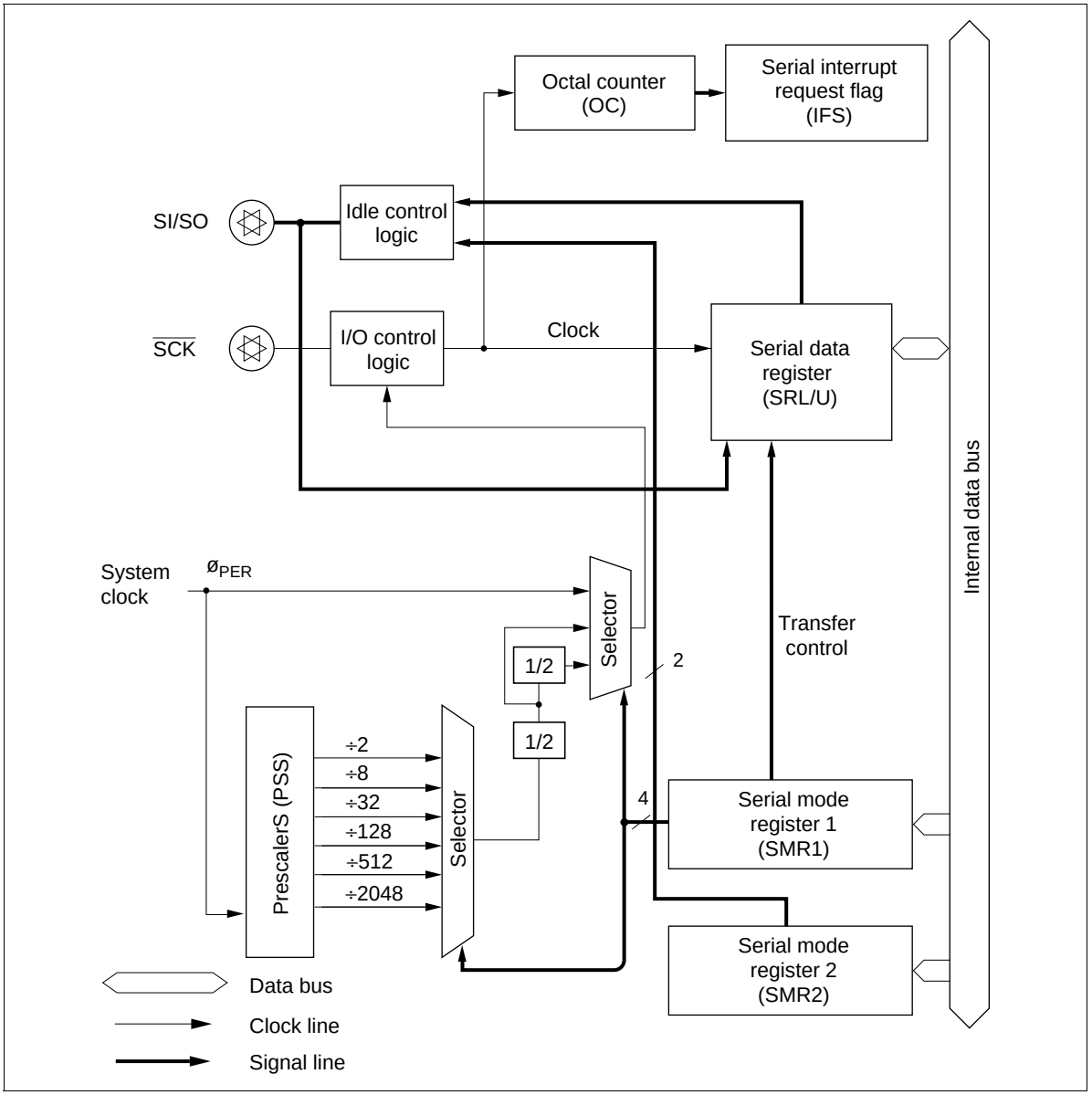



**Figure 52 Serial Interface Block Diagram**

**Serial Interface Operation**

**Selecting and changing serial interface operating mode:**
The operating modes that can be selected for the serial interface are shown in table 26. The combination of port mode register 3 (PMR3) values should be selected from this table. When the serial interface operating mode is changed, the serial interface internal state must be initialized by writing to serial mode register 1 (SMR1).

Note : The serial interface is initialized by writing to serial mode register 1 (SMR1: $024). See figure 56 Serial Mode Register 1, for details.

**Table 26 Serial Interface Operating Modes**

| PMR3 | | | |
|---|---|---|---|
| **Bit3** | **Bit2** | **Bit1** | **Serial interface operating mode** |
| 0 | * | 1 | Clock continuous output mode |
| 1 | 0 | 1 | Receive mode |
| 1 | 1 | 1 | Transmit mode |

Note : * Don't care

**Serial interface pin setting:**
The $R2_1/\overline{SCK}$ pin and $R2_2$/SI/SO pin are set by writing data to port mode register 3 (PMR3). See Serial Interface Registers, for details.

**Serial clock source setting:**
The serial clock is set by writing data to serial mode register 1 (SMR1). See Serial Interface Registers, for details.

**Serial data setting:**
Transmit serial data is set by writing data to the serial data register (SRL, SRU).

Receive serial data is obtained by reading the serial data register (SRL, SRU). Serial data is shifted by means of the serial clock to perform input/output from/to an external device.

The output level of the SO pin is undetermined until the first data is output after a reset by the MCU, or until high/low control is performed in the idle state.

**Transfer control:**
Serial interface operation is started by an STS instruction. The octal counter is reset to 000 by the STS instruction, and is incremented by 1 on each rise of the serial clock. When 8 serial clock pulses have been input, or if data transmission/reception is suspended midway, the octal counter is reset to 000, the serial interrupt request flag (IFS) is set, and transfer is terminated.

The serial clock is selected by means of serial mode register 1 (SMR1). See figure 56.

**Serial interface operating states:**

The serial interface has the operating states shown in figure 53 in external clock mode and internal clock mode.

STS instruction wait state

Serial clock wait state

Transfer state

Clock continuous output state (internal clock mode only)

- STS instruction wait state

  Upon MCU reset ((00) and (10) in figure 53), the serial interface enters the STS instruction wait state. In the STS instruction wait state, the internal state of the serial interface is initialized. Even if the serial clock is input at this time, the serial interface will not operate. When the STS instruction is executed ((01), (11)), the serial interface enters the serial clock wait state.

- Serial clock wait state

  The serial clock wait state is the interval from STS instruction execution until the first serial clock falling edge. When the serial clock is input in the serial clock wait state ((02), (12)), the octal counter begins counting, the contents of the serial data register (SRL, SRU) begin shifting, and the serial interface enters the transfer state. However, if clock continuous output mode is selected in internal clock mode, the serial interface enters the clock continuous output state ((17)) instead of the transfer state.

  If a write to serial mode register 1 (SMR1) is performed in the serial clock wait state, the serial interface enters the STS instruction wait state ((04), (14)).

- Transfer state

  The transfer state is the interval from the first serial clock falling edge until the eighth serial clock rising edge. In the transfer state, if an STS instruction is executed or if eight serial clocks have been input, the octal counter is cleared to 000, and the serial interface makes a state transition. If an STS instruction is executed ((05), (15)), the serial interface enters the serial clock wait state. After eight serial clocks have been input, the serial interface enters the serial clock wait state ((03)) when in external clock mode, and enters the STS instruction wait state ((13)) when in internal clock mode.

  In internal clock mode, the serial clock stops after output of eight clocks.

  If a write to serial mode register 1 (SMR1) is performed in the transfer state ((06), (16)), the serial interface is initialized and enters the STS instruction wait state.

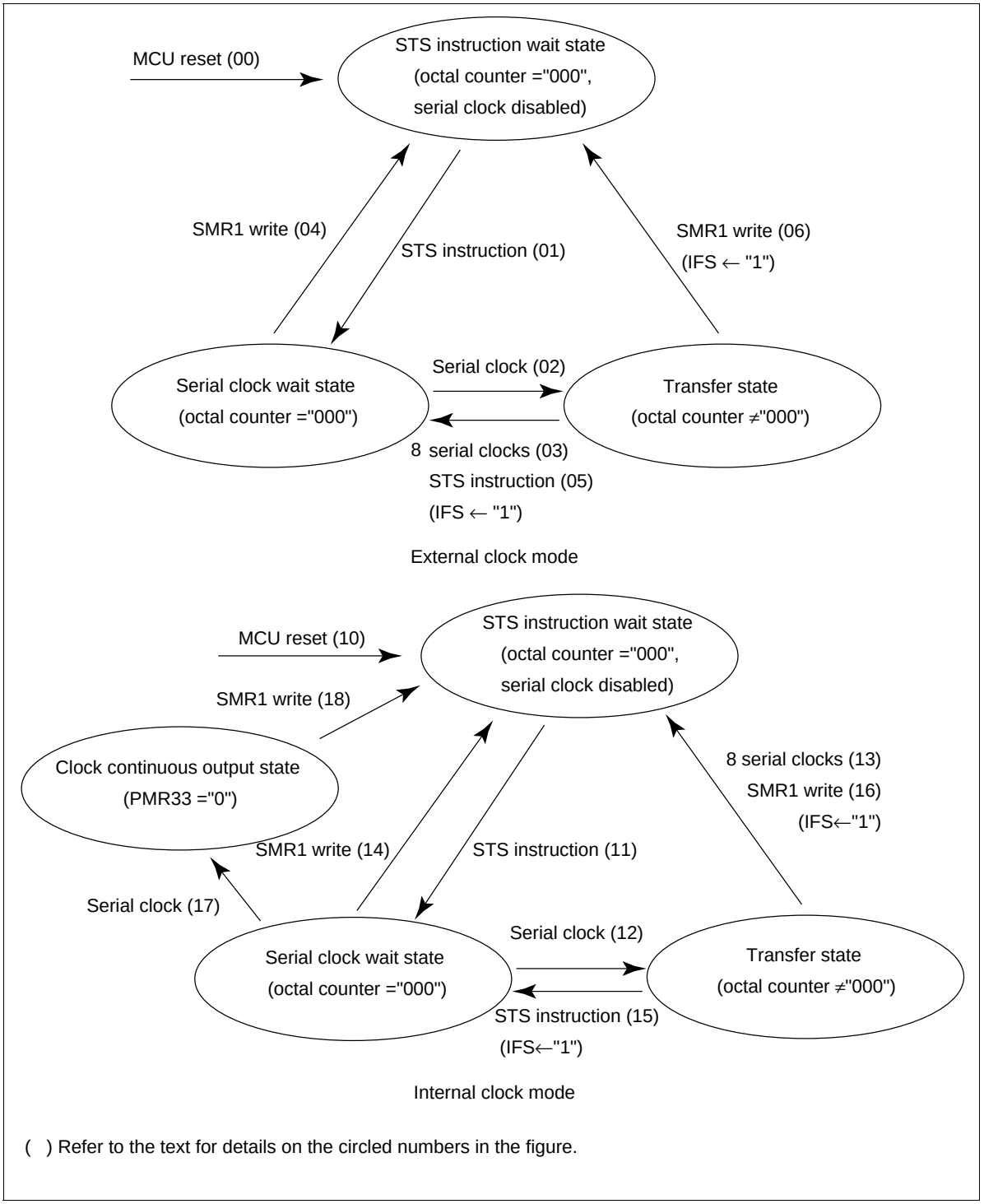
  When the serial interface switches from the transfer state to another state, the octal counter is reset to 000 and the serial interrupt request flag (IFS) is set.

- Clock continuous output state (internal clock mode only)

  In the clock continuous output state, no receive or transmit operation is performed, and the serial clock is only output from the $\overline{\text{SCK}}$ pin. It is therefore effective in internal clock mode.

  If the serial clock is input ((17)) when bit 3 (PMR33) of port mode register 3 (PMR3) is cleared to 0 and the serial interface is in the serial clock wait state, a transition is made to the clock continuous output state.

  If a write to serial mode register 1 (SMR1) is performed in the clock continuous output state ((18)), the serial interface enters the STS instruction wait state.




( ) Refer to the text for details on the circled numbers in the figure.

**Figure 53 Serial Interface Operating States**

**Idle high/low control:**
When the serial interface is in the STS instruction wait state or the serial clock wait state (i.e. when idle), the output level of the SO pin can be set arbitrarily by software. Idle high/low control is performed by writing the output level to bit 1 (SMR21) of serial mode register 2 (SMR2).

An example of idle high/low control is shown in figure 54. Idle high/low control cannot be performed in the transfer state.

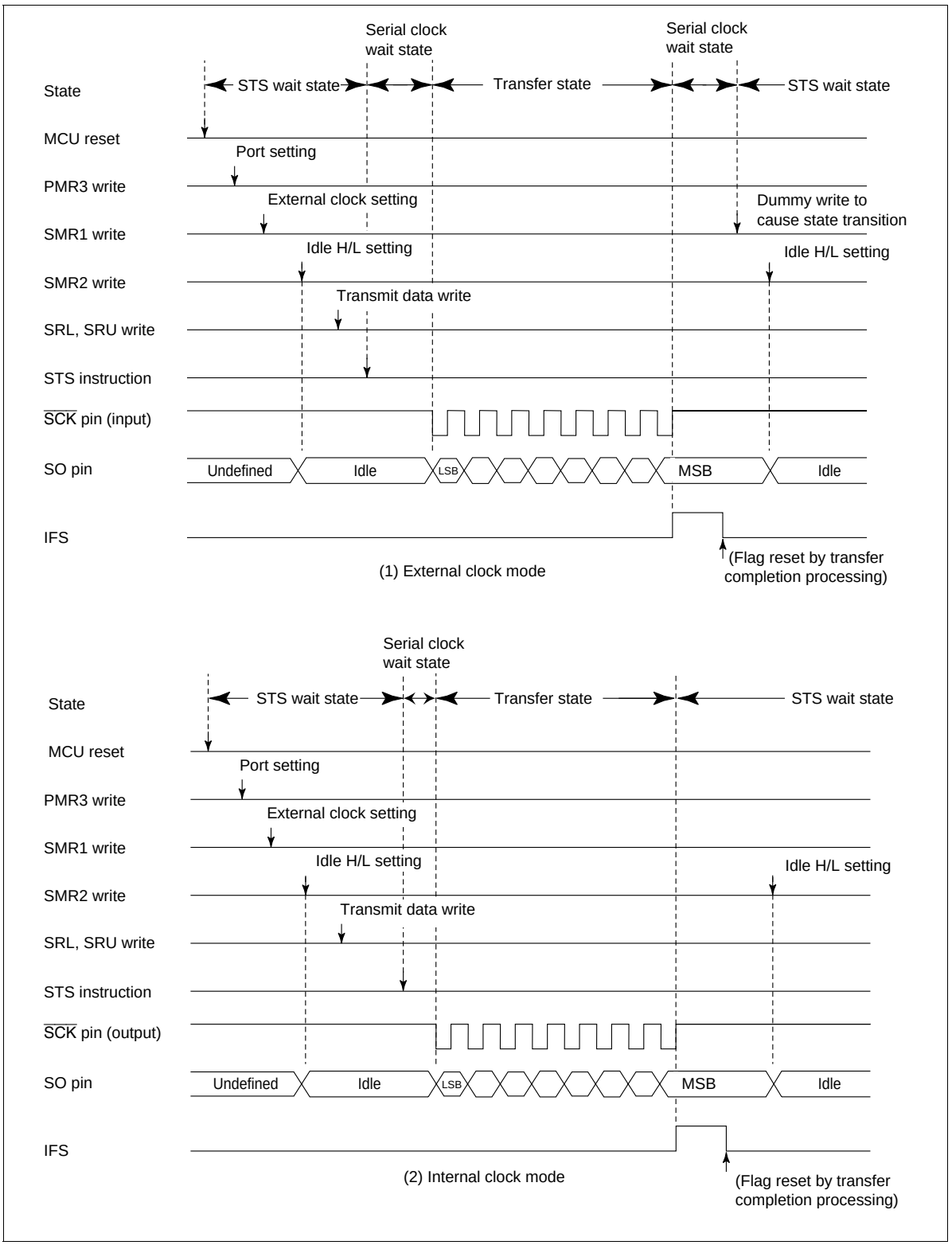



**Figure 54 Examples of Serial Interface Operation Sequence**

**Serial clock error detection (external clock mode):**

The serial interface will operate incorrectly in the transfer state if external noise results in unnecessary pulses being added to the serial clock. Serial clock error detection in such cases is carried out as shown in figure 55.

If more than eight serial clock pulses are input due to external noise while in the transfer state, at the eighth clock pulse (including any external noise pulses), the octal counter is cleared to 000 and the serial interrupt request flag (IFS) is set. At the same time, the serial interface exits the transfer state and enters the serial clock wait state, but returns to the transfer state at the next regular clock pulse falling edge.

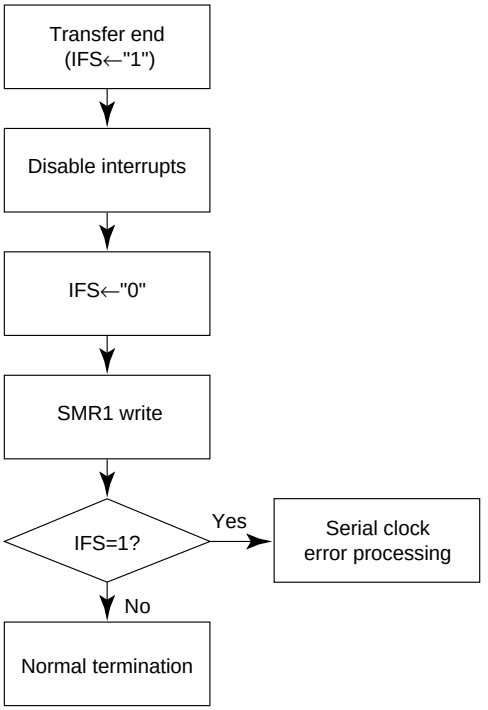
Meanwhile, in the interrupt handling routine, transfer end processing is performed, the serial interrupt request flag is reset, and a dummy write is performed into serial mode register 1 (SMR1). The serial interface then returns to the STS wait state, and the serial interrupt request flag (IFS) is set again. It is therefore possible to detect a serial clock error by testing the serial interrupt request flag after the dummy write to serial mode register 1.

**Usage notes:**

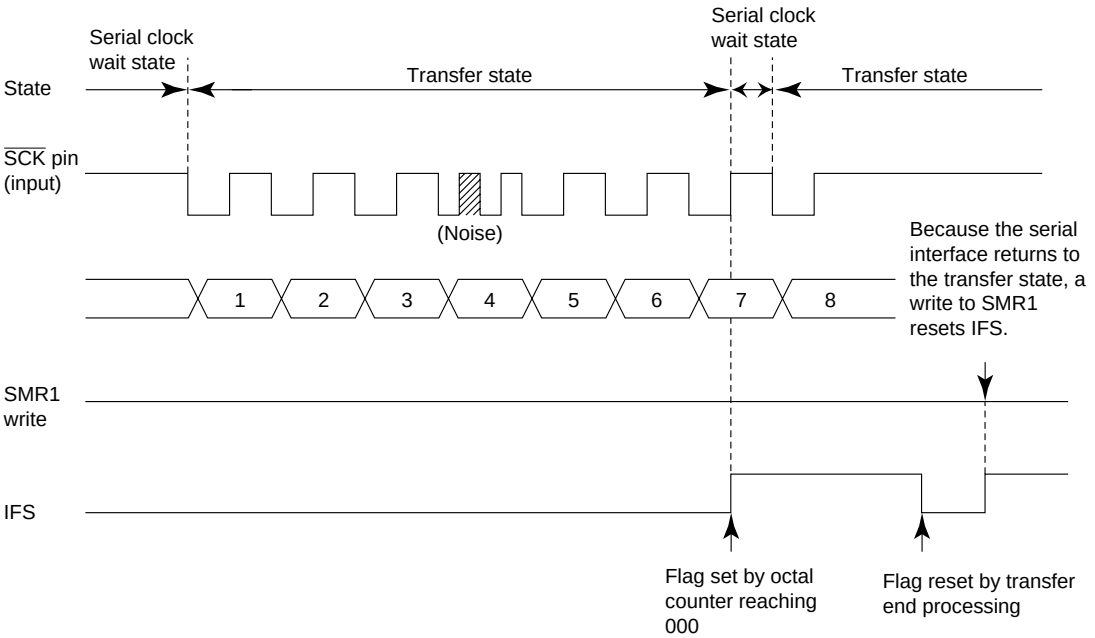
- Initialization after register modification

  If a port mode register 3 (PMR3) write is performed in the serial clock wait state or transfer state, a serial mode register 1 (SMR1) write should be performed again to initialize the serial interface.
- Serial interrupt request flag (IFS:$023, 2) setting

  If a serial mode register 1 (SMR1) write or STS instruction is executed during the first low-level interval of the serial clock in the transfer state, the serial interrupt request flag (IFS) will not be set. To ensure that the serial interrupt request flag (IFS) is properly set in this case, programming is required to make sure that the $\overline{\text{SCK}}$ pin is in the 1 state (by executing an input instruction for the R2 port) before executing a serial mode register 1 (SMR1) write or an STS instruction.




(1) Serial clock error detection flowchart




(2) Serial clock error detection sequence

**Figure 55 Example of Serial Clock Error Detection**

**Serial Interface Registers**

Serial interface operation setting and serial data reading/writing is controlled by the following registers.

Serial mode register 1 (SMR1: $024)

Serial mode register 2 (SMR2: $025)

Serial data register (SRL: $026, SRU: $027)

Port mode register 3 (PMR3: $00B)

Module standby register 2 (MSR2: $00E)

**Serial mode register 1 (SMR1: $024):**

Serial mode register 1 (SMR1) has the following functions. See figure 56.

- Serial clock selection
- Prescaler division ratio selection
- Serial interface initialization

The serial mode register 1 (SMR1) is a 4-bit write-only register, and is reset to $0 by an MCU reset.

A write to serial mode register 1 (SMR1) halts the supply of the serial clock to the serial data register (SRL, SRU) and the octal counter, and resets the octal counter to 000. Therefore, if serial mode register 1 (SMR1) is written to during serial interface operation, data transmission/reception will be suspended and the serial interrupt request flag (IFS) will be set.

A modification of serial mode register 1 (SMR1) becomes effective after execution of two instructions following the serial mode register 1 (SMR1) write instruction. The program must therefore provide for the STS instruction to be executed two cycles after the instruction that writes to serial mode register 1 (SMR1).

Serial mode register 1 (SMR1: $024)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | SMR13 | SMR12 | SMR11 | SMR10 |

| SMR13 | SMR12 | SMR11 | SMR10 | SCK pin | Serial clock source | Serial clock (PSS division ratio ÷ 2 or 4) | Serial clock cycle |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Output | PSS | (øPER/2048)÷2 | 4096 tcyc |
| | | | 1 | Output | PSS | (øPER/512)÷2 | 1024 tcyc |
| | | 1 | 0 | Output | PSS | (øPER/128)÷2 | 256 tcyc |
| | | | 1 | Output | PSS | (øPER/32)÷2 | 64 tcyc |
| | 1 | 0 | 0 | Output | PSS | (øPER/8)÷2 | 16 tcyc |
| | | | 1 | Output | PSS | (øPER/2)÷2 | 4 tcyc |
| | | 1 | 0 | Output | System clock | øPER | tcyc |
| | | | 1 | Input | External clock | ——— | ——— |
| 1 | 0 | 0 | 0 | Output | PSS | (øPER/2048)÷4 | 8192 tcyc |
| | | | 1 | Output | PSS | (øPER/512)÷4 | 2048 tcyc |
| | | 1 | 0 | Output | PSS | (øPER/128)÷4 | 512 tcyc |
| | | | 1 | Output | PSS | (øPER/32)÷4 | 128 tcyc |
| | 1 | 0 | 0 | Output | PSS | (øPER/8)÷4 | 32 tcyc |
| | | | 1 | Output | PSS | (øPER/2)÷4 | 8 tcyc |
| | | 1 | 0 | Output | System clock | øPER | tcyc |
| | | | 1 | Input | External clock | ——— | ——— |

**Figure 56 Serial Mode Register 1 (SMR1)**

**Serial mode register 2 (SMR2: $025):**

Serial mode register 2 (SMR2) has the following functions. See figure 57.

- $R2_2$/SI/SO pin PMOS control
- Idle high/low control

Serial mode register 2 (SMR2) is a 2-bit write-only register. The register value cannot be modified in the transfer state.

Bit 2 (SMR22) of serial mode register 2 (SMR2) controls the on/off status of the $R2_2$/SI/SO pin PMOS. The bit 2 (SMR22) only is reset to 0 by an MCU reset.

Bit 1 (SMR21) of serial mode register 2 (SMR2) performs SO pin high/low control in the idle state. The SO pin changes at the same time as the high/low write.

Serial mode register 2 (SMR2: $025)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | — | W | W | — |
| Initial value on reset | — | 0 | undeternined | — |
| Bit name | — | SMR22 | SMR21 | |

| SMR21 | Idle high/low control |
|---|---|
| 0 | SO pin set to low-level output in idle state |
| 1 | SO pin set to high-level output in idle state |

| SMR22 | R2$_2$/SI/SO pin output buffer control |
|---|---|
| 0 | PMOS active |
| 1 | PMOS off (NMOS open-drain output) |

**Figure 57 Serial Mode Register 2 (SMR2)**

**Serial data register (SRL: $026, SRU: $027):**

The serial data register (SRL, SRU) has the following functions. See figures 58 and 59.

- Transmit data write and shift operations
- Receive data shift and read operations

The data written to the serial data register (SRL, SRU) is output LSB-first from the SO pin in synchronization with the falling edge of the serial clock.

External data input LSB-first from the SI pin is latched in synchronization with the rising edge of the serial clock. Figure 60 shows the serial clock and data input/output timing chart.

Writing and reading of the serial data register (SRL, SRU) must be performed only after data transmission/reception is completed. The data contents are not guaranteed if a read or write is performed during data transmission or reception.

Serial data register (lower) (SRL: $026)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R/W | R/W | R/W | R/W |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name | SR3 | SR2 | SR1 | SR0 |

**Figure 58 Serial Data Register (SRL)**

Serial data register (upper) (SRU: $027)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R/W | R/W | R/W | R/W |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name | SR7 | SR6 | SR5 | SR4 |

**Figure 59 Serial Data Register (SRU)**

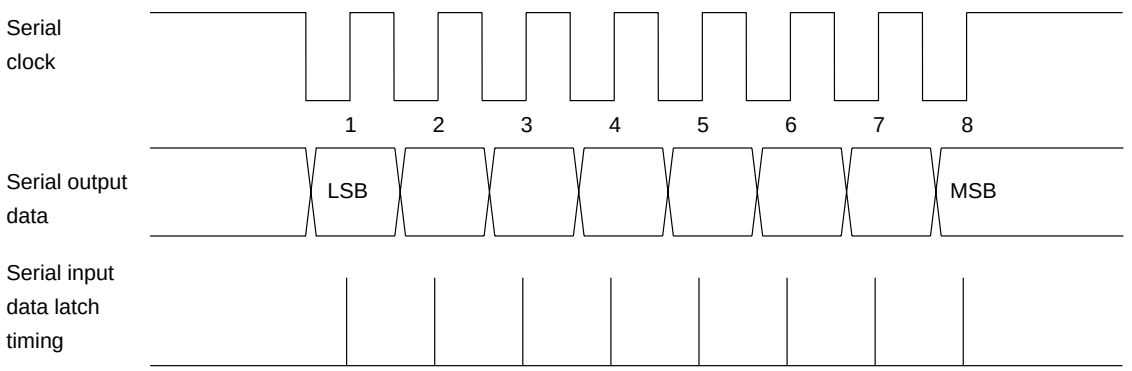



**Figure 60 Serial Interface Input/Output Timing Chart**

**Port mode register 3 (PMR3: $00B):**

Port mode register 3 (PMR3) has the following functions. See figure 61.

- $R2_1/\overline{SCK}$ pin selection
- $R2_2$/SI/SO pin selection

Port mode register 3 (PMR3) is a 4-bit write-only register used to select serial interface pin settings as shown in figure 61. It is reset to $0 by an MCU reset.

Port mode register 3 (PMR3: $00B)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | PMR33 | PMR32 | PMR31 | PMR30 |

| PMR30 | $R2_0$/TOC pin mode selection |
|---|---|
| 0 | $R2_0$ |
| 1 | TOC |

| PMR31 | $R2_1/\overline{SCK}$ pin mode selection |
|---|---|
| 0 | $R2_1$ |
| 1 | $\overline{SCK}$ |

| PMR33 | PMR32 | $R2_2$/SI/SO pin mode selection |
|---|---|---|
| 0 | * | $R2_2$ |
| 1 | 0 | SI |
| | 1 | SO |

* : Don't care

**Figure 61 Port Mode Register 3 (PMR3)**

**Module standby register 2 (MSR2: $00E):**

Module standby register 2 (MSR2) is a write-only register used to designate supply or stopping of the clock to the serial interface as shown in figure 62.

Module standby register 2 (MSR2) is reset to $0 by an MCU reset.

Module standby register 2 (MSR2: $00E)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | — | — | W | W |
| Initial value on reset | — | — | 0 | 0 |
| Bit name | — | — | MSR21 | MSR20 |

| MSR20 | Serial clock supply control |
|---|---|
| 0 | Supplied |
| 1 | Stopped |

| MSR21 | A/D clock supply control |
|---|---|
| 0 | Supplied |
| 1 | Stopped |

**Figure 62 Module Standby Register 2 (MSR2)**

## A/D Converter (HD404374/HD404384/HD404389 Series)

The MCU has a built-in successive approximation type A/D converter using a resistance ladder method, capable of digital conversion of four analog inputs with an 10-bit resolution. The A/D converter block diagram is shown in figure 63.

The A/D converter comprises the following four registers.

- A/D mode register (AMR: $028)
- A/D start flag (ADSF: $020,2)
- A/D data register (ADRL: $029, ADRM: $02A, ADRU: $02B)
- Module standby register 2 (MSR2: $00E)

Note : With the HD404374, HD404384, and HD404389 Series emulator, write 1 to bit 0 (ADRL0) of A/D data register-lower (ADRL). This bit need not be written in the mask ROM and ZTAT™ versions in these series, although writing 1 will have no effect.

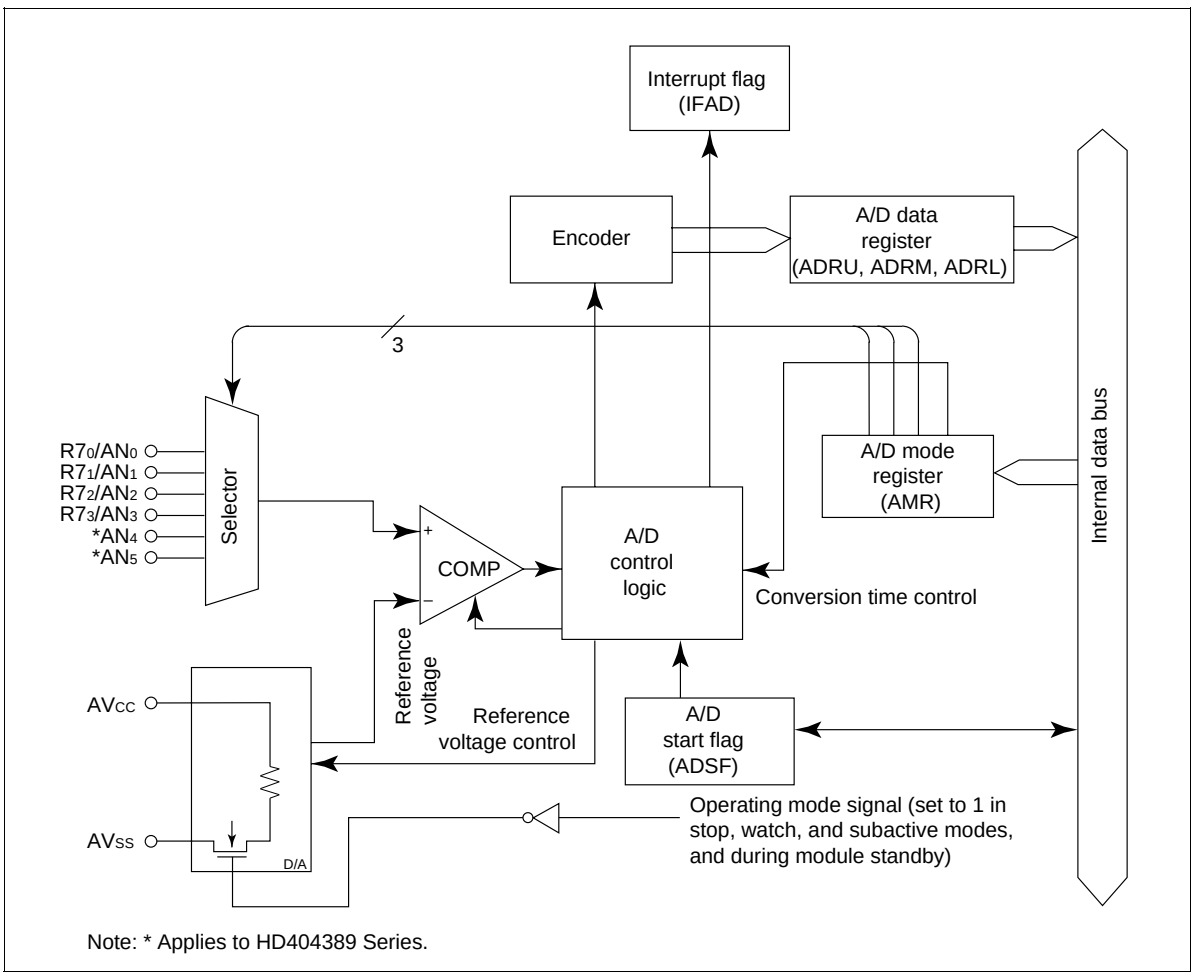



**Figure 63 A/D Converter Block Diagram**

**A/D mode register (AMR: $028):**

The A/D mode register is a 4-bit write-only register that shows the A/D converter speed setting and information on the analog input pin specification. The A/D conversion time is selected by bit 0, and the channel by bits 1, 2, and 3 (figure 64).

**A/D start flag (ADSF: $020,2):**

A/D conversion is started by writing 1 to the A/D start flag. When conversion ends, the converted data is placed in the A/D data register and the A/D start flag is cleared at the same time. (figure 65).

A/D mode register (AMR: $028)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | W | W | W | W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | AMR3 | AMR2 | AMR1 | AMR0 |

| AMR0 | A/D conversion time |
|---|---|
| 0 | 65 $t_{cyc}$ |
| 1 | 125 $t_{cyc}$ |

| AMR3 | AMR2 | AMR1 | Analog input channel selection |
|---|---|---|---|
| 0 | 0 | — | No selection |
| | 1 | 0 | AN0 |
| | | 1 | AN1 |
| 1 | 0 | 0 | AN2 |
| | | 1 | AN3 |
| | 1 | 0 | AN4* |
| | | 1 | AN5* |

Note: * Applies to the HD404389 series. This selection is not available on the HD 404374 and HD404384 series.

**Figure 64 A/D Mode Register (AMR)**

A/D start flag (ADSF: $020,2)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R/W | R/W | R/W | R/W |
| Initial value on reset | 0 | 0 | 0 | 0 |
| Bit name | DTON | ADSF | WDON | LSON |

LSON (see low-power mode section)

WDON (see timer section)

| A/D start flag (ADSF) | |
|---|---|
| 1 | A/D conversion starts |
| 0 | Indicates end of A/D conversion |

DTON (see low-power mode section)

**Figure 65 A/D Start Flag (ADSF)**

**A/D data register (ADRL: $029, ADRM: $02A, ADRU: $02B):**

The A/D data register is a read-only register consisting of a middle 4 bits and lower 2 bits. This register is not cleared by a reset. Also, data read during A/D conversion is not guaranteed. At the end of A/D conversion, the resulting 10-bit data is stored in this register, and is held until the next conversion operation starts (figures 66, 67, 68, and 69).

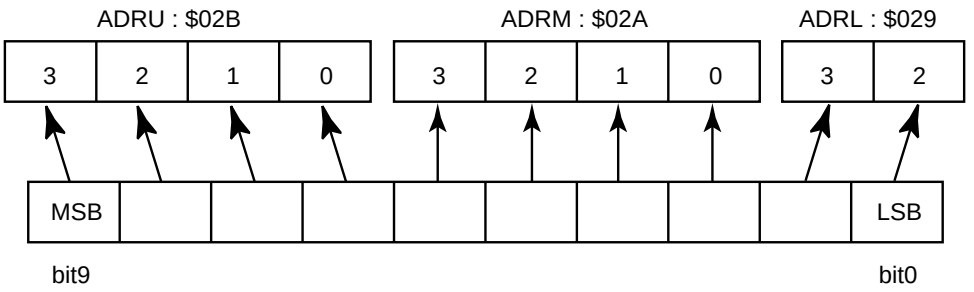



**Figure 66 A/D Data Register**

A/D data register-lower (ADRL: $029)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R | R | — | — |
| Initial value on reset | 1 | 1 | — | —* |
| Bit name | ADRL3 | ADRL2 | Not used | Not used |

Note: * Should be written with 1 with the emulator.

**Figure 67 A/D Data Register-Lower (ADRL)**

A/D data register-middle (ADRM: $02A)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R | R | R | R |
| Initial value on reset | 1 | 1 | 1 | 1 |
| Bit name | ADRM3 | ADRM2 | ADRM1 | ADRM0 |

**Figure 68 A/D Data Register-Middle (ADRM)**

A/D data register-upper (ADRU: $02B)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/Write | R | R | R | R |
| Initial value on reset | 0 | 1 | 1 | 1 |
| Bit name | ADRU3 | ADRU2 | ADRU1 | ADRU0 |

**Figure 69 A/D Data Register-Upper (ADRU)**

**Module standby register 2 (MSR2: $00E):**

Writing 1 to bit 1 of module standby register 2 stops the supply of the system clock to the A/D module and cuts the current ($I_{AD}$) flowing in the ladder resistor.

**Usage notes:**

- Use the SEM or SEMD instruction to write to the A/D start flag (ADSF).
- Do not write to the ADSF during A/D conversion.
- Data in the A/D data register is undetermined during A/D conversion.

- As the A/D converter operates on a clock from OSC, it stops in stop mode, watch mode, and subactive mode. The current flowing in the A/D converter ladder resistor is also cut in these low-power modes to reduce power consumption.
- When an analog input pin is selected by the A/D mode register, the pull-up MOS for that pin is disabled.
- Use of bit 0 of A/D data register-lower (ADRL) is prohibited, but with the emulator it should be written with 1. This bit need not be written in the mask ROM and ZTAT™ versions, although writing 1 will have no effect.

## ZTAT™ Microcomputer with Built-in Programmable ROM

### Precautions for use of ZTAT™ microcomputer with built-in programmable ROM

#### (1) Precautions for writing to programmable ROM built in ZTAT™ microcomputer

In the ZTAT™ microcomputer with built-in plastic mold one-time programmable ROM, incomplete electrical connection between the PROM writer and socket adapter causes writing errors and, makes the computer unoperatable. To enhance the writing efficiency, attention should be paid to the following points:

(a) Make sure that the socket adapter is firmly fixed to the PROM writer and connected electrically with each other (neither opened nor shorted), before starting the writing process.

(b) To secure the electrical connection between the contact pin and IC lead, make sure that there is no foreign substance on the contact pin of the socket adapter, which may cause improper electrical connection.

(c) When inserting the IC, be careful to protect the IC lead from bending in order to secure the electrical connection between the contact pin and IC lead. If the lead is bent, correct the bending and insert it again.

(d) If any trouble is noticed during a blank check to be performed to prevent erroneous writing due to improper electrical connection, carry out the writing process again according to above steps (a), (b), and (c).

(e) During the writing process, do not touch the socket adapter and IC to prevent erroneous writing.

(f) To write continuously in the IC, follow steps (a), (b), (c), (d) and (e).

(g) If a writing error recurs, or the rate of writing errors occur frequently, stop writing and check the PROM writer, socket adapter, etc. for defects.

(h) If any problem is noticed in the written program or in the program after being left at a high temperature, consult our technical staff.

#### (2) Precautions when new PROM writer, socket adapter or IC is used

When a new PROM writer, socket adapter or IC is employed, breakdown of the IC may occur or its writing may become impossible because the noise, overshoot, timing or other electrical characteristics may be inconsistent with the assured IC writing characteristics. To avoid such troubles, check the following points before starting the writing process.

(a) To ensure stable writing operation, check that the $V_{CC}$ of the power supplied to the PROM writer, power source current capacity of $V_{PP}$, and current consumption at the time of writing to IC are provided with sufficient margin.

(b) To prevent breakdown of the IC, check that the power source voltage between GND-$V_{CC}$ and GND-$V_{PP}$, and overshoot or undershoot of the power source at the connecting terminal of the socket adapter are within the ratings. Particularly, if the overshoot or undershoot exceeds the maximum rating, the p-n connection may be damaged, leading to permanent breakdown. If overshoot or undershoot occurs, recheck the power source damping resistance of capacity.

(c) To prevent breakdown of the IC and for stable writing and reading operation, insert the IC into the socket adapter and check the power noise between the GND-$V_{CC}$ and GND-$V_{PP}$ near the IC connecting

terminal. If power source noise is noticed, insert an appropriate capacitor between the GND power sources depending on the noise generated. In case of high frequency noise , insert a capacitor of low inductance.

(d) For stable writing and reading operation, insert the IC into the socket adapter and check the input waveform, timing and noise near the R/W, CS, address and data terminals. Particularly, since recent ICs have increased in speed, caution should be exercised against the noise to the power source or address due to crosstalk from the output data terminal. To avoid these problems, inserting a low inductance capacitor between the GND and power source or inserting a damping resistance to the output data terminal is effective.

(e) Particularly, when a multiple PROM writer is used, perform above items (a), (b), (c), and (d) assuming all ICs inserted into the socket adapter.

(f) In the case of a multiple PROM writer, when an unacceptable result is noticed during a blank check performed to prevent erroneous writing due to improper electrical connection of the power source, etc., rewriting is impossible unless every writing process can be stopped. Therefore, the potential increases due to erroneous writing because of improper connection. Be sure to check the electrical connection between the PROM writer and socket adapter and IC.

(g) If any abnormality is noticed while checking a written program, consult our technical staff.

**Programming of Built-in programmable ROM**

The MCU can stop its function as an MCU in PROM mode for programming the built-in PROM.

PROM mode is set up by setting the $\overline{\text{RESET}}$ and $\overline{\text{MO}}$ terminals to “Low” level and the TEST terminal to “Vpp” level.

Writing and reading specifications of the PROM are the same as those for the commercial EPROM27256. Using a socket adapter for specific use of each product, programming is possible with a general-purpose PROM writer.

Since an instruction of the HMCS400 series is 10 bits long, a conversion circuit is incorporated to adapt the general-purpose PROM writer. This circuit splits each instruction into five lower bits and five higher bits to write from or read to two addresses. This enables use of a general-purpose PROM. For instance, to write to a 16kword of built-in PROM writer with a general-purpose PROM, specify 32kbyte address ($0000-$7FFF). An example of PROM memory map is shown in figure 70.

**Notes:**

1. When programming with a PROM writer, set up each ROM size to the address given in table 29. If it is programmed erroneously to an address given in table 29 or later, check of writing of PROM may become impossible. Particularly, caution should be exercised in the case of a plastic package since reprogramming is impossible with it. Set the data in unused addresses to $FF.
2. If the indexes of the PROM writer socket, socket adapter and product are not aligned precisely, the product may break down due to overcurrent. Be sure to check that they are properly set to the writer before starting the writing process.

3. Two levels of program voltages ($V_{PP}$) are available for the PROM: 12.5V and 21V. Our product employs a $V_{PP}$ of 12.5V. If a voltage of 21V is applied, permanent breakdown of the product will result. The $V_{PP}$ of 12.5V is obtained for the PROM writer by setting it according to the Intel 27258 specifications.

**Table 27 Socket Adapters**

| Package | Model Name | Manufacturer |
|---|---|---|
| FP-30D | Please ask Hitachi service section. | |
| DP-28S | Please ask Hitachi service section. | |

## Writing/Verification

Programming of the built-in program ROM employs a high speed programming method. With this method, high speed writing is effected without voltage stress to the device or without damaging the reliability of the written data.

A basic programming flow chart is shown in figure 71 and a timing chart in figure 72.

For precautions for PROM writing procedure, refer to "Precautions for use of ZTAT™ microcomputer with build-in programmable ROM".

**Table 28 Selection of Mode**

| Mode | $\overline{CE}$ | $\overline{OE}$ | $V_{PP}$ | $O_0$ to $O_4$ |
|---|---|---|---|---|
| Writing | "Low" | "High" | $V_{PP}$ | Data input |
| Verification | "High" | "Low" | $V_{PP}$ | Data output |
| Prohibition of programming | "High" | "High" | $V_{PP}$ | High impedance |

**Table 29 PROM Writer Program Address**

| ROM size | Address |
|---|---|
| 2k | $0000~$0FFF |
| 4k | $0000~$1FFF |
| 8k | $0000~$3FFF |
| 16k | $0000~$7FFF |

## Programmable ROM

The HD407A4374/HD407C4374/HD407A4384/HD407C4384, HD407A4389/HD407C4389 are ZTAT™ microcomputers with built-in PROM that can be programmed in PROM mode.

### PROM Mode Pin Description

#### (1) HD407A4374/HD407C4374/HD407A4384/HD407C4384

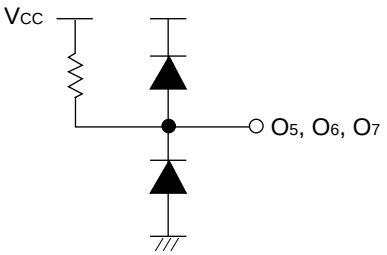
| Pin No. | | MCU Mode | | PROM Mode. | |
|---|---|---|---|---|---|
| FP-30D | DP-28S | Pin name | I/O | Pin name | I/O |
| 1 | 1 | GND | — | GND | — |
| 2 | 2 | $V_{CC}$ | — | $V_{CC}$ | — |
| 3 | 3 | $AV_{CC}$ | — | $V_{CC}$ | — |
| 4 | 4 | $R7_0/AN_0$ | I/O | $O_0$ | I/O |
| 5 | 5 | $R7_1/AN_1$ | I/O | $O_1$ | I/O |
| 6 | 6 | $R7_2/AN_2$ | I/O | $O_2$ | I/O |
| 7 | 7 | $R7_3/AN_3$ | I/O | $O_3$ | I/O |
| 8 | 8 | $AV_{SS}$ | — | GND | — |
| 9 | 9 | $OSC_1$ | I | $A_0$ | I |
| 10 | 10 | $OSC_2$ | O | — | — |
| 11 | 11 | TEST | I | $V_{PP}$ | — |
| 12 | — | $X_2$ | O | — | — |
| 13 | — | $X_1$ | I | GND | — |
| 14 | 12 | $\overline{RESET}$ | I | $\overline{RESET}$ | I |
| 15 | 13 | $R0_0/\overline{WU}_0$ | I/O | $A_1$ | I |
| 16 | 14 | $R1_0$/EVNB | I/O | $A_2$ | I |
| 17 | 15 | $R1_3$/TOB | I/O | $O_4$ | I/O |
| 18 | 16 | $R2_0$/TOC | I/O | $\overline{CE}$ | I |
| 19 | 17 | $R2_1/\overline{SCK}$ | I/O | $A_2$ | I |
| 20 | 18 | $R2_2$/SI/SO | I/O | $A_3$ | I |
| 21 | 19 | $D_0/\overline{INT}_0$ | I/O | $\overline{MO}$ | I |
| 22 | 20 | $D_1$ | I/O | $A_5$ | I |
| 23 | 21 | $D_2$ | I/O | $A_6$ | I |
| 24 | 22 | $D_3$ | I/O | $A_7$ | I |
| 25 | 23 | $D_4$ | I/O | $A_8$ | I |
| 26 | 24 | $D_5$ | I/O | $A_9$ | I |
| 27 | 25 | $D_6$ | I/O | $A_{10}$ | I |
| 28 | 26 | $D_7$ | I/O | $A_{11}$ | I |
| 29 | 27 | $D_8$ | I/O | $A_{12}$ | I |
| 30 | 28 | $D_9$ | I/O | $\overline{OE}$ | I |

**(2) HD407A4389 and HD407C4389**

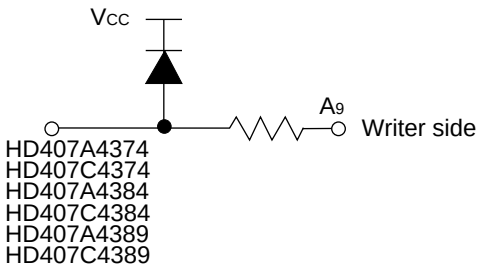
| Pin No. | MCU Mode | | PROM Mode. | |
|---|---|---|---|---|
| **FP-30D** | **Pin name** | **I/O** | **Pin name** | **I/O** |
| 1 | GND | — | GND | — |
| 2 | $V_{CC}$ | — | $V_{CC}$ | — |
| 3 | $AV_{CC}$ | — | $V_{CC}$ | — |
| 4 | $R7_0/AN_0$ | I/O | $O_0$ | I/O |
| 5 | $R7_1/AN_1$ | I/O | $O_1$ | I/O |
| 6 | $R7_2/AN_2$ | I/O | $O_2$ | I/O |
| 7 | $R7_3/AN_3$ | I/O | $O_3$ | I/O |
| 8 | $AN_4$ | I | $\overline{CE}$ | I |
| 9 | $AN_5$ | I | $\overline{OE}$ | I |
| 10 | $AV_{SS}$ | — | GND | |
| 11 | TEST | I | $V_{PP}$ | — |
| 12 | $OSC_1$ | I | $A_0$ | I |
| 13 | $OSC_2$ | O | — | — |
| 14 | $\overline{RESET}$ | I | $\overline{RESET}$ | I |
| 15 | $R0_0/\overline{WU}_0$ | I/O | $A_1$ | I |
| 16 | $R1_0$/EVNB | I/O | $A_4$ | I |
| 17 | $R1_3$/TOB | I/O | $O_4$ | I/O |
| 18 | $R2_0$/TOC | I/O | $A_{14}$ | I |
| 19 | $R2_1/\overline{SCK}$ | I/O | $A_2$ | I |
| 20 | $R2_2$/SI/SO | I/O | $A_3$ | I |
| 21 | $D_0/\overline{INT}_0$ | I/O | $\overline{MO}$ | I |
| 22 | $D_1$ | I/O | $A_5$ | I |
| 23 | $D_2$ | I/O | $A_6$ | I |
| 24 | $D_3$ | I/O | $A_7$ | I |
| 25 | $D_4$ | I/O | $A_8$ | I |
| 26 | $D_5$ | I/O | $A_9$ | I |
| 27 | $D_6$ | I/O | $A_{10}$ | I |
| 28 | $D_7$ | I/O | $A_{11}$ | I |
| 29 | $D_8$ | I/O | $A_{12}$ | I |
| 30 | $D_9$ | I/O | $A_{13}$ | I |

Note: I/O: I/O pin, I: Input-only pin, O: Output-only pin

1. Unused data pins ($O_5$ to $O_7$) on the PROM programmer side should be handled as shown below on the socket.




2. Pin $A_9$ should be handled as shown below on the socket.



**Pin Functions in PROM Mode**

**$V_{PP}$:**
Applies the on-chip PROM programming voltage (12.5 V ±0.3 V).

**$\overline{CE}$:**
Inputs a control signal to set the on-chip PROM to the write/verify enabled state.

**$\overline{OE}$:**
Inputs a data output control signal during verification.

**$A_0$ to $A_{14}$:**
On-chip PROM address input pins.

**$O_0$ to $O_4$:**
On-chip PROM data bus I/O pins.

**$\overline{MO}$, $\overline{RESET}$, TEST:**
PROM mode setting pins. PROM mode is set by driving the $\overline{RESET}$, and $\overline{MO}$ pins low, and driving the TEST pin to the $V_{PP}$ level.

**Other pins:**
$V_{CC}$ and $AV_{CC}$ should be connected to $V_{CC}$ potential.

GND, $AV_{SS}$, and X1 should be connected to GND potential.

Other pins should be left open.

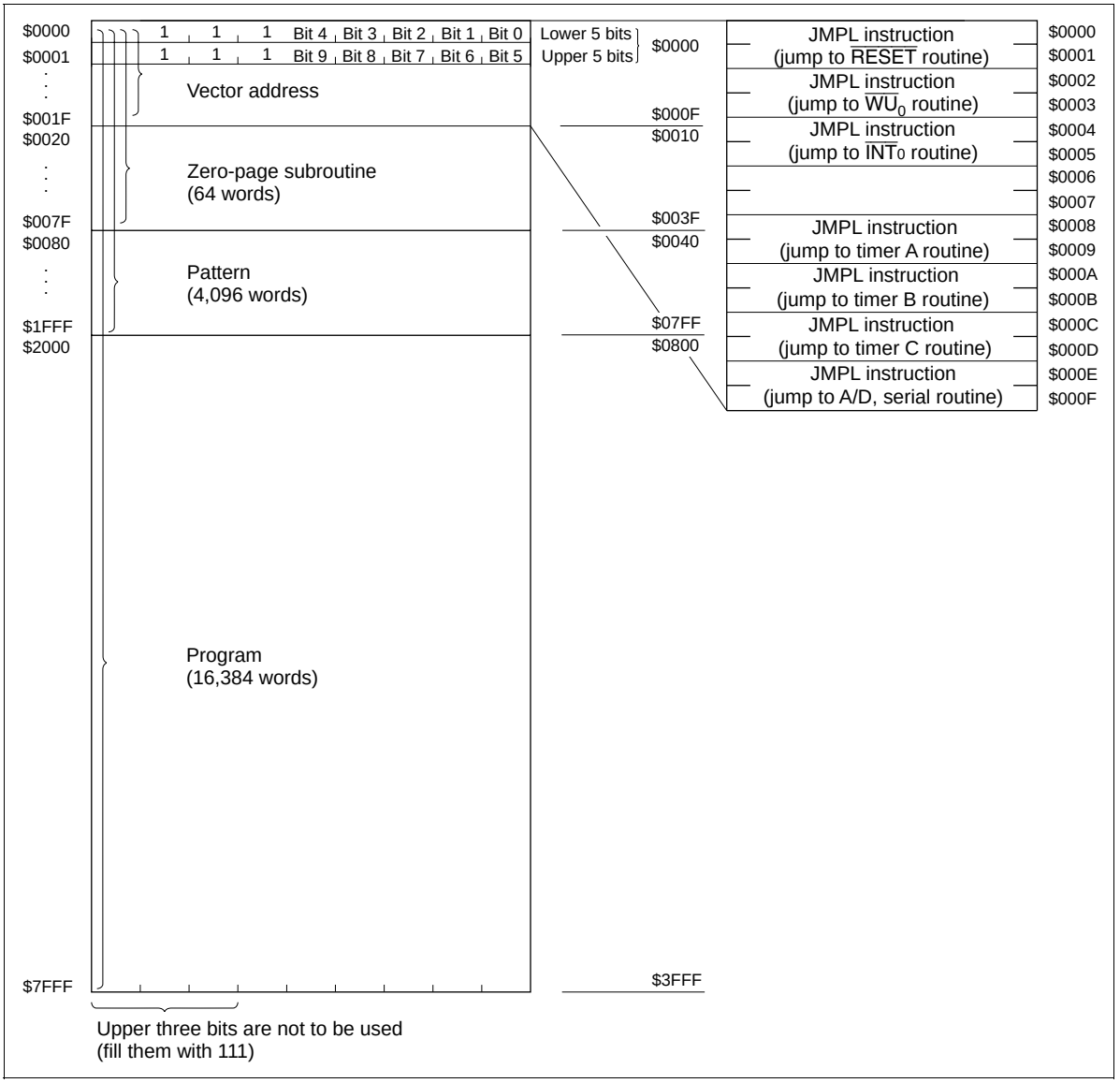



**Figure 70 Memory Map in PROM Mode**

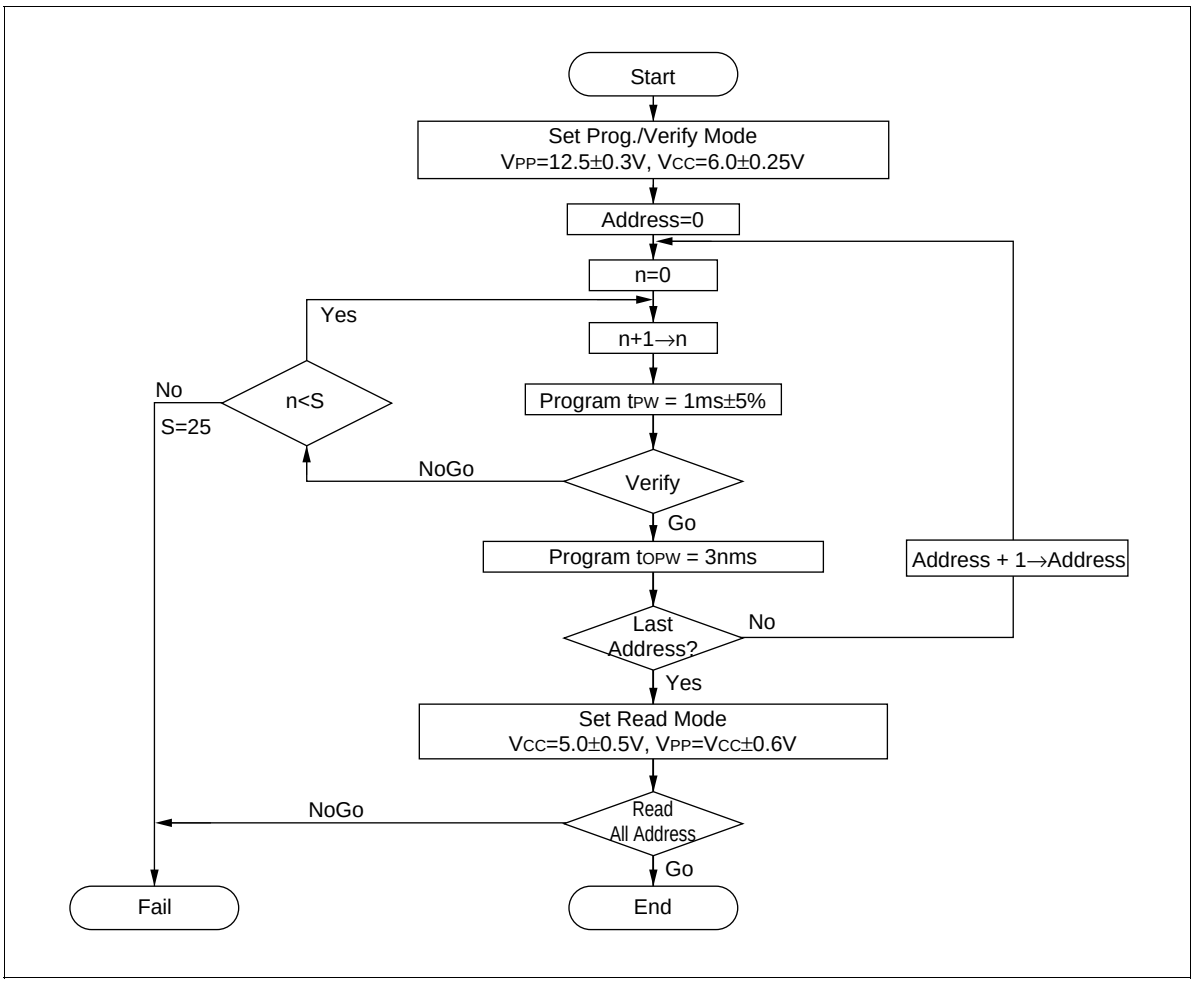



**Figure 71 Flowchart of High-Speed Programming**

**Programming Electrical Characteristics**

**DC Characteristics ($V_{CC}$ = 6V ±0.25V, $V_{PP}$ = 12.5V ±0.3V, $V_{SS}$ = 0V, $T_a$ = 25°C ±5°C, unless otherwise specified)**

| Item | | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Input high voltage | $O_0$ to $O_4$,$A_0$ to $A_{14}$, $\overline{OE}$, $\overline{CE}$ | $V_{IH}$ | | 2.2 | — | $V_{CC}$+0.3 | V |
| Input low voltage | $O_0$ to $O_4$,$A_0$ to $A_{14}$, $\overline{OE}$, $\overline{CE}$ | $V_{IL}$ | | –0.3 | — | 0.8 | V |
| Output high voltage | $O_0$ to $O_4$ | $V_{OH}$ | $I_{OH}$=–200µA | 2.4 | — | — | V |
| Output low voltage | $O_0$ to $O_4$ | $V_{OL}$ | $I_{OL}$=1.6mA | — | — | 0.4 | V |
| Input leakage current | $O_0$ to $O_4$,$A_0$ to $A_{14}$, $\overline{OE}$, $\overline{CE}$ | $\lvert I_{IL} \rvert$ | $V_{in}$=5.25V/0.5V | — | — | 2 | µA |
| $V_{CC}$ current | | $I_{CC}$ | | — | — | 30 | mA |
| $V_{PP}$ current | | $I_{PP}$ | | — | — | 40 | mA |

**AC Characteristics ($V_{CC}$ = 6V ±0.25V, $V_{PP}$ = 12.5V ±0.3V, $T_a$ = 25°C ±5°C, unless otherwise specified)**

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Address setup time | $t_{AS}$ | | 2 | — | — | µs |
| $\overline{OE}$ setup time | $t_{OES}$ | | 2 | — | — | µs |
| Data setup time | $t_{DS}$ | | 2 | — | — | µs |
| Address hold time | $t_{AH}$ | | 0 | — | — | µs |
| Data hold time | $t_{DH}$ | | 2 | — | — | µs |
| Data output disable time | $t_{DF}$ | See figure 72 | — | — | 130 | ns |
| $V_{PP}$ setup time | $t_{VPS}$ | | 2 | — | — | µs |
| Program pulse width | $t_{PW}$ | | 0.95 | 1.0 | 1.05 | ms |
| $\overline{CE}$ pulse width during overprogramming | $t_{OPW}$ | | 2.85 | — | 78.75 | ms |
| $V_{CC}$ setup time | $t_{VCS}$ | | 2 | — | — | µs |
| Data output delay time | $t_{OE}$ | | 0 | — | 500 | ns |

Notes: Input pulse level: 0.8 V to 2.2 V
Input rise/fall times: ≤ 20ns
Input timing reference levels: 1.0 V, 2.0 V
Output timing reference levels: 0.8 V, 2.0 V

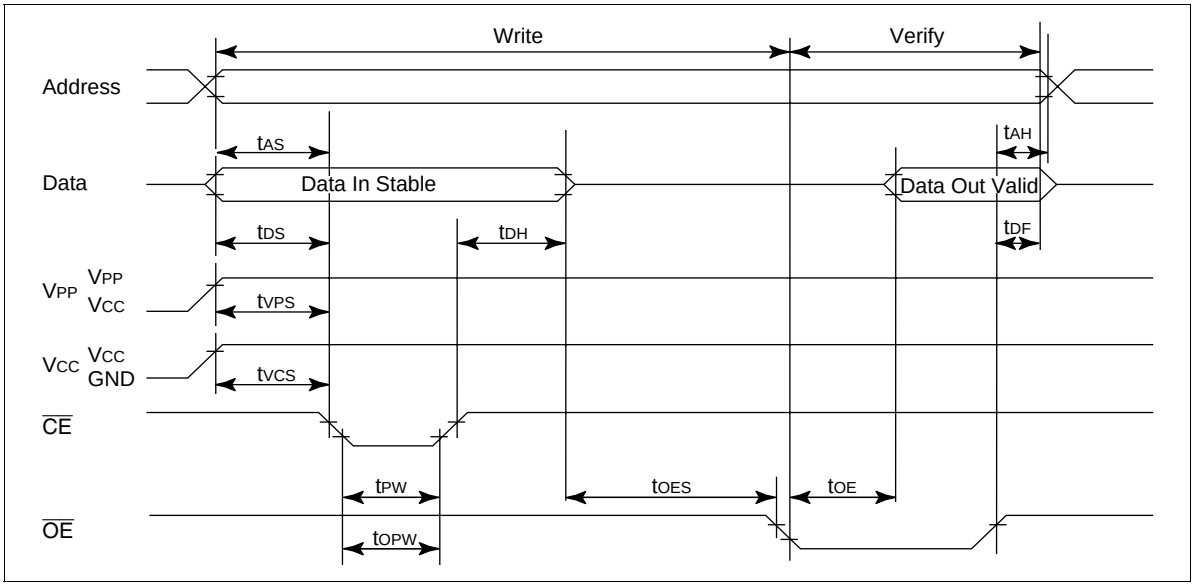



**Figure 72 PROM Write/Verify Timing**

**Notes on PROM Programming**

**Principles of Programming/Erasure:** A memory cell in a ZTAT™ microcomputer is the same as an EPROM cell; it is programmed by applying a high voltage between its control gate and drain to inject hot electrons into its floating gate. These electrons are stable, surrounded by an energy barrier formed by an $SiO_2$ film. The change in threshold voltage of a memory cell with a charged floating gate makes the corresponding bit appear as 0; a cell whose floating gate is not charged appears as a 1 bit (figure 73).

The charge in a memory cell may decrease with time. This decrease is usually due to one of the following causes:

- Ultraviolet light excites electrons, allowing them to escape. This effect is the basis of the erasure principle.
- Heat excites trapped electrons, allowing them to escape.
- High voltages between the control gate and drain may erase electrons.

If the oxide film covering a floating gate is defective, the electron erasure rate will be greater. However, electron erasure does not often occur because defective devices are detected and removed at the testing stage.

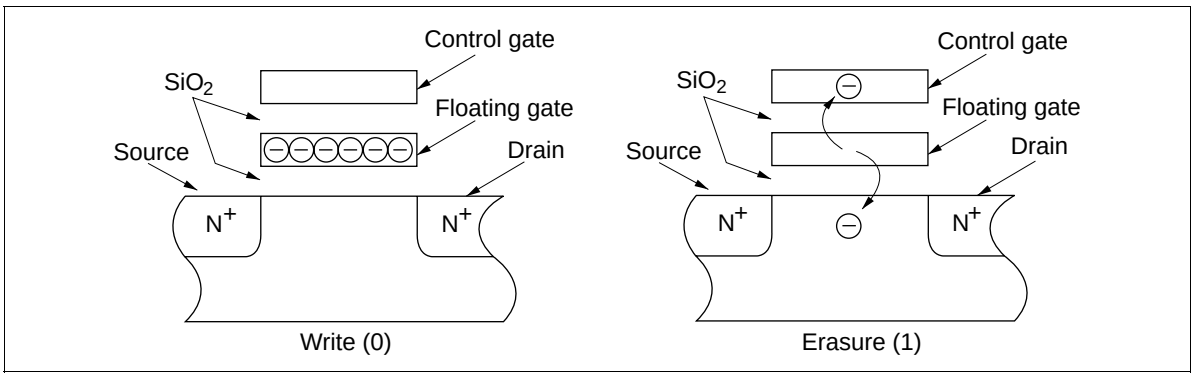



**Figure 73 Cross-Sections of a PROM Cell**

**PROM Programming:** PROM memory cells must be programmed under specific voltage and timing conditions. The higher the programming voltage $V_{PP}$ and the longer the programming pulse $t_{PW}$ is applied, the more electrons are injected into the floating gates. However, if $V_{PP}$ exceeds specifications, the pn junctions may be permanently damaged. Pay particular attention to overshooting in the PROM programmer. In addition, note that negative voltage noise will produce a parasitic transistor effect that may reduce breakdown voltages.

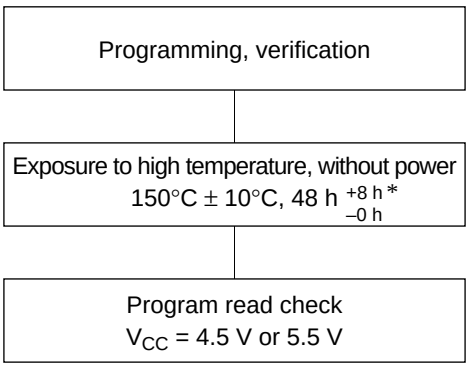
The ZTAT™ microcomputer is electrically connected to the PROM programmer by a socket adapter. Therefore, note the following points:

- Check that the socket adapter is firmly mounted on the PROM programmer.
- Do not touch the socket adapter or the LSI during the programming. Touching them may affect the quality of the contacts, which will cause programming errors.

**PROM Reliability after Programming:** In general, semiconductor devices retain their reliability, provided that some initial defects can be excluded. These initial defects can be detected and rejected by screening. Baking devices under high-temperature conditions is one method of screening that can rapidly eliminate data-hold defects in memory cells. (Refer to the previous Principles of Programming/Erasure section.)

ZTAT™ microcomputer devices are extremely reliable because they have been subjected to such a screening method during the wafer fabrication process, but Hitachi recommends that each device be exposed to 150°C at one atmosphere for at least 48 hours after it is programmed, to ensure its best performance. The recommended screening procedure is shown in figure 74.

Note: If programming errors occur continuously during PROM programming, suspend programming and check for problems in the PROM programmer or socket adapter. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi.




Note: Exposure time is measured from when the temperature in the heater reaches 150°C.

**Figure 74 Recommended Screening Procedure**

**Programming percentage:** Programming percentage is guarenteed to more than 95%.

## Addressing Modes

### RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 75 and described below.

**Register Indirect Addressing Mode:** The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

**Direct Addressing Mode:** A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

**Memory Register Addressing Mode:** The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

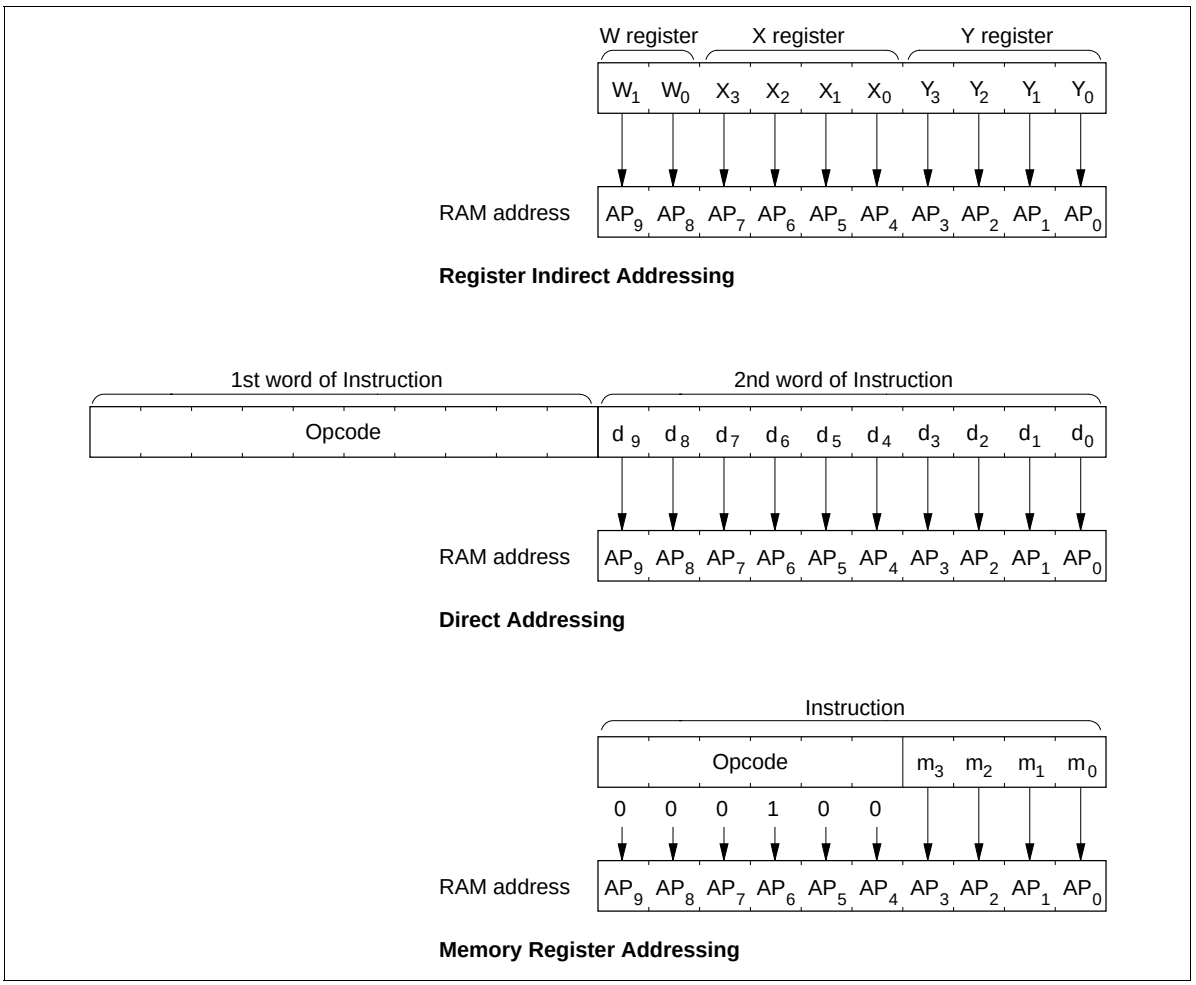



**Figure 75 RAM Addressing Modes**

**ROM Addressing Modes and the P Instruction**

The MCU has four ROM addressing modes, as shown in figure 76 and described below.

**Direct Addressing Mode:** A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits ($PC_{13}$–$PC_0$) with 14-bit immediate data.

**Current Page Addressing Mode:** The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter ($PC_7$–$PC_0$) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 78. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross assembler has an automatic paging feature for ROM pages.

**Zero-Page Addressing Mode:** A program can branch to the zero-page subroutine area located at $0000–$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter ($PC_5$–$PC_0$), and 0s are placed in the eight high-order bits ($PC_{13}$–$PC_6$).

**Table Data Addressing Mode:** A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

**P Instruction:** ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 77. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

**Branch Destination of BR Instruction on Page Boundary:** If a BR instruction is located on a page boundary (256n + 255), because of the hardware architecture the program counter contents will shift to the next page when that instruction is executed. When using a BR instruction on a page boundary, therefore, the branch destination must be set within the next page (see figure 78).

The HMCS400-series cross assembler has an automatic paging feature for ROM pages, regardless of the model.

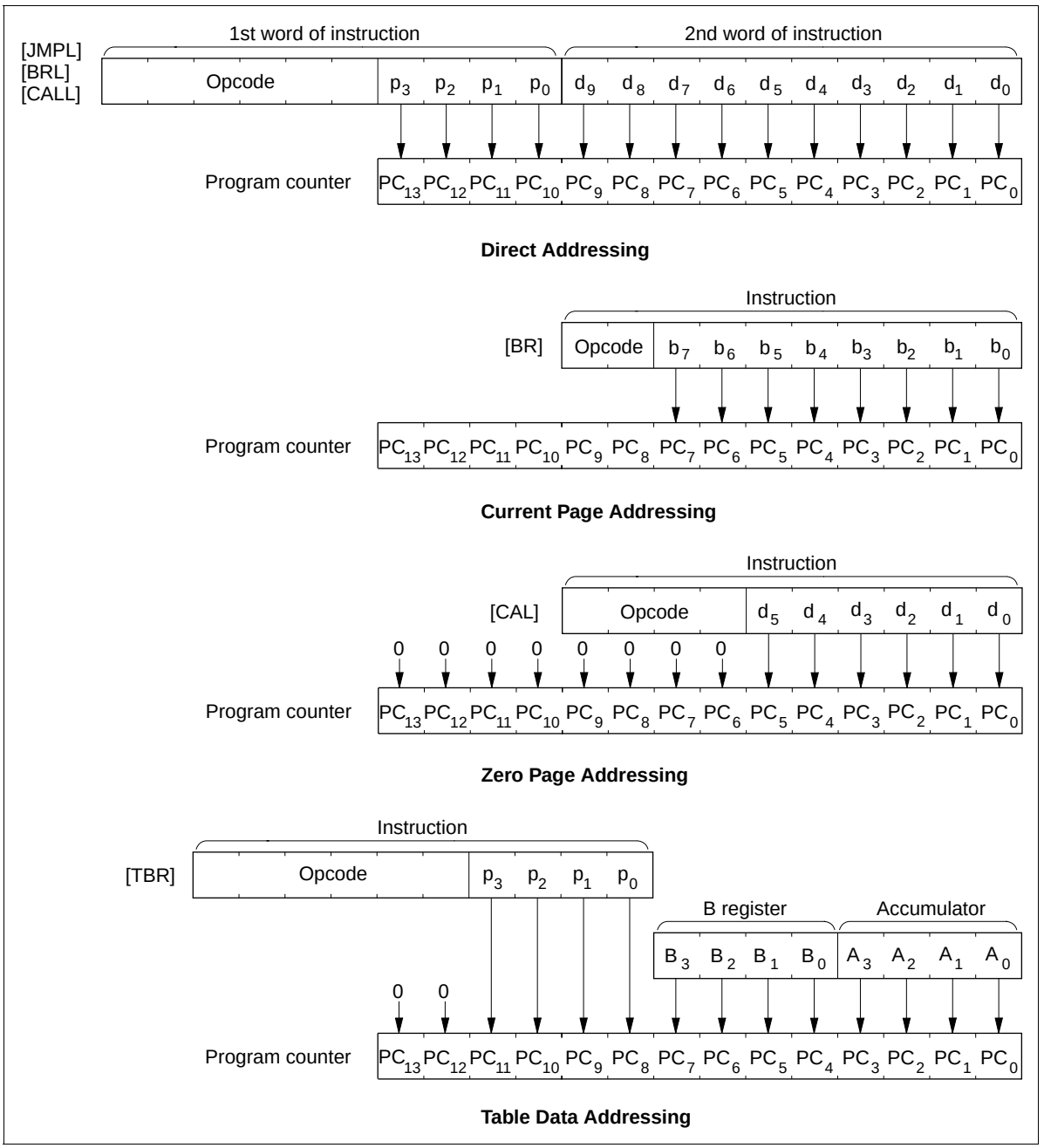



**Figure 76 ROM Addressing Modes**

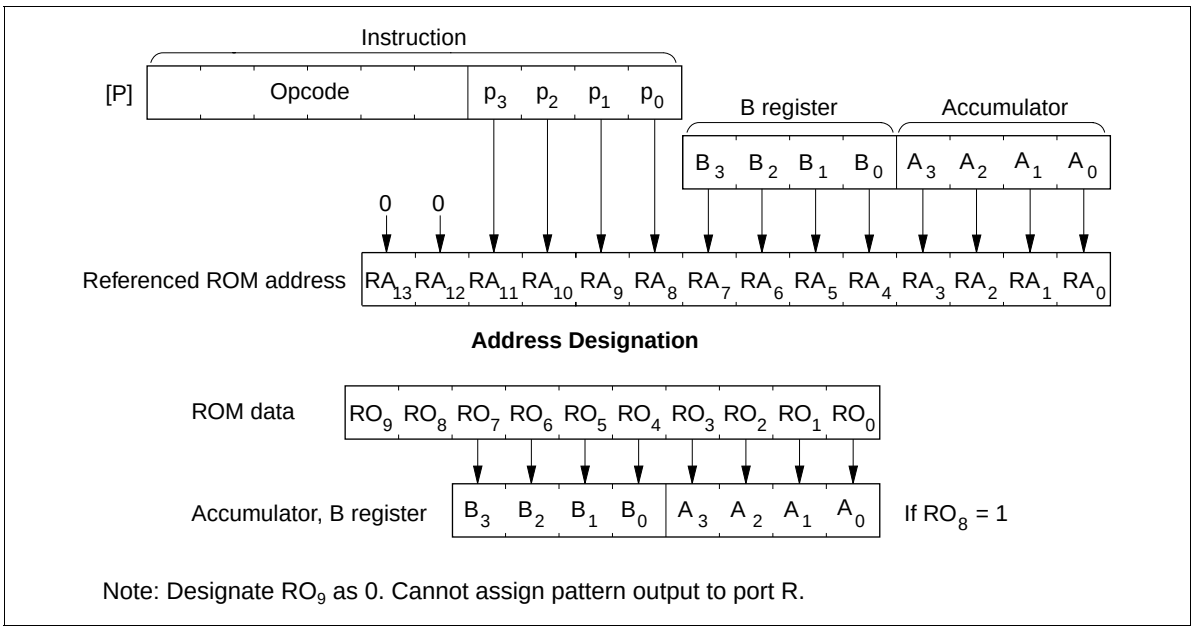



**Figure 77 P Instruction**

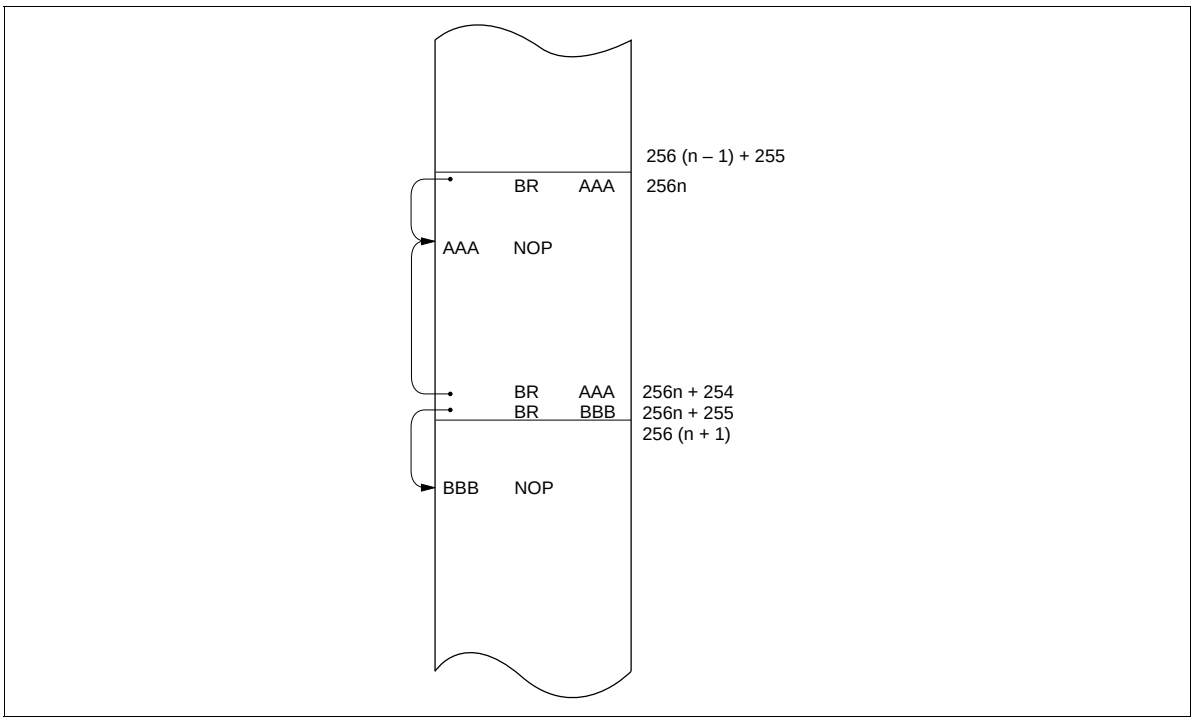



**Figure 78 Branching when the Branch Destination is on a Page Boundary**

## Instruction Set

The MCU Series has 101 instructions, classified into the following 10 groups:

- Immediate instructions
- Register-to-register instructions
- RAM addressing instructions
- RAM register instructions
- Arithmetic instructions
- Compare instructions
- RAM bit manipulation instructions
- ROM addressing instructions
- Input/output instructions
- Control instructions

The functions of these instructions are listed in tables 30 to 39, and an opcode map is shown in table 40.

**Table 30 Immediate Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| Load A from immediate | LAI i | 1 0 0 0 1 1 $i_3$ $i_2$ $i_1$ $i_0$ | i → A | | 1/1 |
| Load B from immediate | LBI i | 1 0 0 0 0 0 $i_3$ $i_2$ $i_1$ $i_0$ | i → B | | 1/1 |
| Load memory from immediate | LMID i,d | 0 1 1 0 1 0 $i_3$ $i_2$ $i_1$ $i_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | i → M | | 2/2 |
| Load memory from immediate, increment Y | LMIIY i | 1 0 1 0 0 1 $i_3$ $i_2$ $i_1$ $i_0$ | i → M, Y + 1 → Y | NZ | 1/1 |

**Table 31 Register-Register Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| Load A from B | LAB | 0 0 0 1 0 0 1 0 0 0 | B → A | | 1/1 |
| Load B from A | LBA | 0 0 1 1 0 0 1 0 0 0 | A → B | | 1/1 |
| Load A from W | LAW | 0 1 0 0 0 0 0 0 0 0<br>0 0 0 0 0 0 0 0 0 0 | W → A | | 2/2* |
| Load A from Y | LAY | 0 0 1 0 1 0 1 1 1 1 | Y → A | | 1/1 |
| Load A from SPX | LASPX | 0 0 0 1 1 0 1 0 0 0 | SPX → A | | 1/1 |
| Load A from SPY | LASPY | 0 0 0 1 0 1 1 0 0 0 | SPY → A | | 1/1 |
| Load A from MR | LAMR m | 1 0 0 1 1 1 $m_3$ $m_2$ $m_1$ $m_0$ | MR (m) → A | | 1/1 |
| Exchange MR and A | XMRA m | 1 0 1 1 1 1 $m_3$ $m_2$ $m_1$ $m_0$ | MR (m) ↔ A | | 1/1 |

Note: The assembler automatically provides an operand for the second word of the LAW instruction.

**Table 32 RAM Address Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| Load W from immediate | LWI i | 0 0 1 1 1 1 0 0 $i_1$ $i_0$ | i → W | | 1/1 |
| Load X from immediate | LXI i | 1 0 0 0 1 0 $i_3$ $i_2$ $i_1$ $i_0$ | i → X | | 1/1 |
| Load Y from immediate | LYI i | 1 0 0 0 0 1 $i_3$ $i_2$ $i_1$ $i_0$ | i → Y | | 1/1 |
| Load W from A | LWA* | 0 1 0 0 0 1 0 0 0 0<br>0 0 0 0 0 0 0 0 0 0 | A → W | | 2/2* |
| Load X from A | LXA | 0 0 1 1 1 0 1 0 0 0 | A → X | | 1/1 |
| Load Y from A | LYA | 0 0 1 1 0 1 1 0 0 0 | A → Y | | 1/1 |
| Increment Y | IY | 0 0 0 1 0 1 1 1 0 0 | Y + 1 → Y | NZ | 1/1 |
| Decrement Y | DY | 0 0 1 1 0 1 1 1 1 1 | Y – 1 → Y | NB | 1/1 |
| Add A to Y | AYY | 0 0 0 1 0 1 0 1 0 0 | Y + A → Y | OVF | 1/1 |
| Subtract A from Y | SYY | 0 0 1 1 0 1 0 1 0 0 | Y – A → Y | NB | 1/1 |
| Exchange X and SPX | XSPX | 0 0 0 0 0 0 0 0 0 1 | X ↔ SPX | | 1/1 |
| Exchange Y and SPY | XSPY | 0 0 0 0 0 0 0 0 1 0 | Y ↔ SPY | | 1/1 |
| Exchange X and SPX, Y and SPY | XSPXY | 0 0 0 0 0 0 0 0 1 1 | X ↔ SPX,Y ↔ SPY | | 1/1 |

Note: * The assembler automatically provides an operand for the second word of the LAW and LWA instruction.

**Table 33 RAM Register Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| Load A from memory | LAM | 0 0 1 0 0 1 0 0 0 0 | M → A | | 1/1 |
| | LAMX | 0 0 1 0 0 1 0 0 0 1 | M → A<br>X ↔ SPX | | |
| | LAMY | 0 0 1 0 0 1 0 0 1 0 | M → A<br>Y ↔ SPY | | |
| | LAMXY | 0 0 1 0 0 1 0 0 1 1 | M → A<br>X ↔ SPX, Y ↔ SPY | | |
| Load A from memory | LAMD d | 0 1 1 0 0 1 0 0 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | M → A | | 2/2 |
| Load B from memory | LBM | 0 0 0 1 0 0 0 0 0 0 | M → B | | 1/1 |
| | LBMX | 0 0 0 1 0 0 0 0 0 1 | M → B<br>X ↔ SPX | | |
| | LBMY | 0 0 0 1 0 0 0 0 1 0 | M → B<br>Y ↔ SPY | | |
| | LBMXY | 0 0 0 1 0 0 0 0 1 1 | M → B<br>X ↔ SPX, Y ↔ SPY | | |
| Load memory from A | LMA | 0 0 1 0 0 1 0 1 0 0 | A → M | | 1/1 |
| | LMAX | 0 0 1 0 0 1 0 1 0 1 | A → M<br>X ↔ SPX | | |
| | LMAY | 0 0 1 0 0 1 0 1 1 0 | A → M<br>Y ↔ SPY | | |
| | LMAXY | 0 0 1 0 0 1 0 1 1 1 | A → M<br>X ↔ SPX, Y ↔ SPY | | |
| Load memory from A | LMAD d | 0 1 1 0 0 1 0 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | A → M | | 2/2 |
| Load memory from A, increment Y | LMAIY | 0 0 0 1 0 1 0 0 0 0 | A → M, Y + 1 → Y | NZ | 1/1 |
| | LMAIYX | 0 0 0 1 0 1 0 0 0 1 | A → M, Y + 1 → Y<br>X ↔ SPX | | |
| Load memory from A, decrement Y | LMADY | 0 0 1 1 0 1 0 0 0 0 | A → M, Y – 1 → Y | NB | 1/1 |
| | LMADYX | 0 0 1 1 0 1 0 0 0 1 | A → M, Y – 1 → Y<br>X ↔ SPX | | |

**Table 33 RAM Register Instructions (cont)**

| Operation | Mnemonic | Operation Code | | | | | | | | | | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Exchange memory and A | XMA | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | M ↔ A | | 1/1 |
| | XMAX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | M ↔ A<br>X ↔ SPX | | |
| | XMAY | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | M ↔ A<br>Y ↔ SPY | | |
| | XMAXY | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | M ↔ A<br>X ↔ SPX, Y ↔ SPY | | |
| Exchange memory and A | XMAD d | 0<br>$d_9$ | 1<br>$d_8$ | 1<br>$d_7$ | 0<br>$d_6$ | 0<br>$d_5$ | 0<br>$d_4$ | 0<br>$d_3$ | 0<br>$d_2$ | 0<br>$d_1$ | 0<br>$d_0$ | M ↔ A | | 2/2 |
| Exchange memory and B | XMB | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | M ↔ B | | 1/1 |
| | XMBX | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | M ↔ B<br>X ↔ SPX | | |
| | XMBY | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | M ↔ B<br>Y ↔ SPY | | |
| | XMBXY | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | M ↔ B<br>X ↔ SPX, Y ↔ SPY | | |

**Table 34 Arithmetic Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| Add immediate to A | AI i | 1 0 1 0 0 0 $i_3$ $i_2$ $i_1$ $i_0$ | A + i → A | OVF | 1/1 |
| Increment B | IB | 0 0 0 1 0 0 1 1 0 0 | B + 1 → B | NZ | 1/1 |
| Decrement B | DB | 0 0 1 1 0 0 1 1 1 1 | B – 1 → B | NB | 1/1 |
| Decimal adjust for addition | DAA | 0 0 1 0 1 0 0 1 1 0 | | | 1/1 |
| Decimal adjust for subtraction | DAS | 0 0 1 0 1 0 1 0 1 0 | | | 1/1 |
| Negate A | NEGA | 0 0 0 1 1 0 0 0 0 0 | $\overline{A}$ + 1 → A | | 1/1 |
| Complement B | COMB | 0 1 0 1 0 0 0 0 0 0 | $\overline{B}$ → B | | 1/1 |
| Rotate right A with carry | ROTR | 0 0 1 0 1 0 0 0 0 0 | | | 1/1 |
| Rotate left A with carry | ROTL | 0 0 1 0 1 0 0 0 0 1 | | | 1/1 |
| Set carry | SEC | 0 0 1 1 1 0 1 1 1 1 | 1 → CA | | 1/1 |
| Reset carry | REC | 0 0 1 1 1 0 1 1 0 0 | 0 → CA | | 1/1 |
| Test carry | TC | 0 0 0 1 1 0 1 1 1 1 | | CA | 1/1 |
| Add A to memory | AM | 0 0 0 0 0 0 1 0 0 0 | M + A → A | OVF | 1/1 |
| Add A to memory | AMD d | 0 1 0 0 0 0 1 0 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | M + A → A | OVF | 2/2 |
| Add A to memory with carry | AMC | 0 0 0 0 0 1 1 0 0 0 | M + A + CA → A<br>OVF → CA | OVF | 1/1 |
| Add A to memory with carry | AMCD d | 0 1 0 0 0 1 1 0 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | M + A + CA → A<br>OVF → CA | OVF | 2/2 |
| Subtract A from memory with carry | SMC | 0 0 1 0 0 1 1 0 0 0 | M – A – $\overline{CA}$ → A<br>NB → CA | NB | 1/1 |
| Subtract A from memory with carry | SMCD d | 0 1 1 0 0 1 1 0 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | M – A – $\overline{CA}$ → A<br>NB → CA | NB | 2/2 |
| OR A and B | OR | 0 1 0 1 0 0 0 1 0 0 | A ∪ B → A | | 1/1 |
| AND memory with A | ANM | 0 0 1 0 0 1 1 1 0 0 | A ∩ M → A | NZ | 1/1 |
| AND memory with A | ANMD d | 0 1 1 0 0 1 1 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | A ∩ M → A | NZ | 2/2 |
| OR memory with A | ORM | 0 0 0 0 0 0 1 1 0 0 | A ∪ M → A | NZ | 1/1 |
| OR memory with A | ORMD d | 0 1 0 0 0 0 1 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | A ∪ M → A | NZ | 2/2 |
| EOR memory with A | EORM | 0 0 0 0 0 1 1 1 0 0 | A ⊕ M → A | NZ | 1/1 |
| EOR memory with A | EORMD d | 0 1 0 0 0 1 1 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | A ⊕ M → A | NZ | 2/2 |

**Table 35 Compare Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| Immediate not equal to memory | INEM i | 0 0 0 0 1 0 $i_3$ $i_2$ $i_1$ $i_0$ | i ≠ M | NZ | 1/1 |
| Immediate not equal to memory | INEMD i,d | 0 1 0 0 1 0 $i_3$ $i_2$ $i_1$ $i_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | i ≠ M | NZ | 2/2 |
| A not equal to memory | ANEM | 0 0 0 0 0 0 0 1 0 0 | A ≠ M | NZ | 1/1 |
| A not equal to memory | ANEMD d | 0 1 0 0 0 0 0 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | A ≠ M | NZ | 2/2 |
| B not equal to memory | BNEM | 0 0 0 1 0 0 0 1 0 0 | B ≠ M | NZ | 1/1 |
| Y not equal to immediate | YNEI i | 0 0 0 1 1 1 $i_3$ $i_2$ $i_1$ $i_0$ | Y ≠ i | NZ | 1/1 |
| Immediate less than or equal to memory | ILEM i | 0 0 0 0 1 1 $i_3$ $i_2$ $i_1$ $i_0$ | i ≤ M | NB | 1/1 |
| Immediate less than or equal to memory | ILEMD i,d | 0 1 0 0 1 1 $i_3$ $i_2$ $i_1$ $i_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | i ≤ M | NB | 2/2 |
| A less than or equal to memory | ALEM | 0 0 0 0 0 1 0 1 0 0 | A ≤ M | NB | 1/1 |
| A less than or equal to memory | ALEMD d | 0 1 0 0 0 1 0 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | A ≤ M | NB | 2/2 |
| B less than or equal to memory | BLEM | 0 0 1 1 0 0 0 1 0 0 | B ≤ M | NB | 1/1 |
| A less than or equal to immediate | ALEI i | 1 0 1 0 1 1 $i_3$ $i_2$ $i_1$ $i_0$ | A ≤ i | NB | 1/1 |

**Table 36 RAM Bit Manipulation Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| Set memory bit | SEM n | 0 0 1 0 0 0 0 1 $n_1$ $n_0$ | i → M (n) | | 1/1 |
| Set memory bit | SEMD n,d | 0 1 1 0 0 0 0 1 $n_1$ $n_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | i → M (n) | | 2/2 |
| Reset memory bit | REM n | 0 0 1 0 0 0 1 0 $n_1$ $n_0$ | 0 → M (n) | | 1/1 |
| Reset memory bit | REMD n,d | 0 1 1 0 0 0 1 0 $n_1$ $n_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | 0 → M (n) | | 2/2 |
| Test memory bit | TM n | 0 0 1 0 0 0 1 1 $n_1$ $n_0$ | | M (n) | 1/1 |
| Test memory bit | TM n,d | 0 1 1 0 0 0 1 1 $n_1$ $n_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | | M (n) | 2/2 |

**Table 37 ROM Address Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| Branch on status 1 | BR b | 1 1 $b_7$ $b_6$ $b_5$ $b_4$ $b_3$ $b_2$ $b_1$ $b_0$ | | 1 | 1/1 |
| Long branch on status 1 | BRL u | 0 1 0 1 1 1 $p_3$ $p_2$ $p_1$ $p_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | | 1 | 2/2 |
| Long jump unconditionally | JMPL u | 0 1 0 1 0 1 $p_3$ $p_2$ $p_1$ $p_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | | | 2/2 |
| Subroutine jump on status 1 | CAL a | 0 1 1 1 $a_5$ $a_4$ $a_3$ $a_2$ $a_1$ $a_0$ | | 1 | 1/2 |
| Long subroutine jump on status 1 | CALL u | 0 1 0 1 1 0 $p_3$ $p_2$ $p_1$ $p_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | | 1 | 2/2 |
| Table branch | TBR p | 0 0 1 0 1 1 $p_3$ $p_2$ $p_1$ $p_0$ | | | 1/1 |
| Return from subroutine | RTN | 0 0 0 0 0 1 0 0 0 0 | | | 1/3 |
| Return from interrupt | RTNI | 0 0 0 0 0 1 0 0 0 1 | 1 → IE,<br>carry restored | ST | 1/3 |

**Table 38 Input/Output Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| Set discrete I/O latch | SED | 0 0 1 1 1 0 0 1 0 0 | 1 → D (Y) | | 1/1 |
| Set discrete I/O latch direct | SEDD m | 1 0 1 1 1 0 $m_3$ $m_2$ $m_1$ $m_0$ | 1 → D (m) | | 1/1 |
| Reset discrete I/O latch | RED | 0 0 0 1 1 0 0 1 0 0 | 0 → D (Y) | | 1/1 |
| Reset discrete I/O latch direct | REDD m | 1 0 0 1 1 0 $m_3$ $m_2$ $m_1$ $m_0$ | 0 → D (m) | | 1/1 |
| Test discrete I/O latch | TD | 0 0 1 1 1 0 0 0 0 0 | | D (Y) | 1/1 |
| Test discrete I/O latch direct | TDD m | 1 0 1 0 1 0 $m_3$ $m_2$ $m_1$ $m_0$ | | D (m) | 1/1 |
| Load A from R-port register | LAR m | 1 0 0 1 0 1 $m_3$ $m_2$ $m_1$ $m_0$ | R (m) → A | | 1/1 |
| Load B from R-port register | LBR m | 1 0 0 1 0 0 $m_3$ $m_2$ $m_1$ $m_0$ | R (m) → B | | 1/1 |
| Load R-port register from A | LRA m | 1 0 1 1 0 1 $m_3$ $m_2$ $m_1$ $m_0$ | A → R (m) | | 1/1 |
| Load R-port register from B | LRB m | 1 0 1 1 0 0 $m_3$ $m_2$ $m_1$ $m_0$ | B → R (m) | | 1/1 |
| Pattern generation | P p | 0 1 1 0 1 1 $p_3$ $p_2$ $p_1$ $p_0$ | | | 1/2 |

**Table 39 Control Instructions**

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|---|---|---|---|---|
| No operation | NOP | 0 0 0 0 0 0 0 0 0 0 | | | 1/1 |
| Start serial | STS | 0 1 0 1 0 0 1 0 0 0 | | | 1/1 |
| Standby mode/watch mode* | SBY | 0 1 0 1 0 0 1 1 0 0 | | | 1/1 |
| Stop mode/watch mode | STOP | 0 1 0 1 0 0 1 1 0 1 | | | 1/1 |

Note: * Only after a transition from subactive mode.

**Table 40 Opcode Map**

| R9 | H \ L / R8 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | NOP | XSPX | XSPY | XSPXY | ANEM | | | | AM | | | | ORM | | | |
| | 1 | RTN | RTNI | | | ALEM | | | | AMC | | | | EORM | | | |
| | 2 | INEM i(4) | | | | | | | | | | | | | | | |
| | 3 | ILEM i(4) | | | | | | | | | | | | | | | |
| | 4 | LBM(XY) | | | | BNEM | | | | LAB | | | | IB | | | |
| | 5 | LMAIY(X) | | | | AYY | | | | LASPY | | | | IY | | | |
| | 6 | NEGA | | | | RED | | | | LASPX | | | | | | | TC |
| | 7 | YNEI i(4) | | | | | | | | | | | | | | | |
| | 8 | XMA(XY) | | | | SEM n(2) | | | | REM n(2) | | | | TM n(2) | | | |
| | 9 | LAM(XY) | | | | LMA(XY) | | | | SMC | | | | ANM | | | |
| | A | ROTR | ROTL | | | | | DAA | | | | DAS | | | | | LAY |
| | B | TBR p(4) | | | | | | | | | | | | | | | |
| | C | XMB(XY) | | | | BLEM | | | | LBA | | | | | | | DB |
| | D | LMADY(X) | | | | SYY | | | | LYA | | | | | | | DY |
| | E | TD | | | | SED | | | | LXA | | | | REC | | | SEC |
| | F | LWI i(2) | | | | | | | | | | | | | | | |
| 1 | 0 | LBI i(4) | | | | | | | | | | | | | | | |
| | 1 | LYI i(4) | | | | | | | | | | | | | | | |
| | 2 | LXI i(4) | | | | | | | | | | | | | | | |
| | 3 | LAI i(4) | | | | | | | | | | | | | | | |
| | 4 | LBR m(4) | | | | | | | | | | | | | | | |
| | 5 | LAR m(4) | | | | | | | | | | | | | | | |
| | 6 | REDD m(4) | | | | | | | | | | | | | | | |
| | 7 | LAMR m(4) | | | | | | | | | | | | | | | |
| | 8 | AI i(4) | | | | | | | | | | | | | | | |
| | 9 | LMIIY i(4) | | | | | | | | | | | | | | | |
| | A | TDD m(4) | | | | | | | | | | | | | | | |
| | B | ALEI i(4) | | | | | | | | | | | | | | | |
| | C | LRB m(4) | | | | | | | | | | | | | | | |
| | D | LRA m(4) | | | | | | | | | | | | | | | |
| | E | SEDD m(4) | | | | | | | | | | | | | | | |
| | F | XMRA m(4) | | | | | | | | | | | | | | | |

1-word/2-cycle instruction

1-word/3-cycle instruction

RAM direct address instruction (2-word/2-cycle)

2-word/2-cycle instruction

**Table 40 Opcode Map (cont)**

| R9 | H \ L | R8 = 1 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0 | 0 | LAW | | | | ANEMD | | | | AMD | | | | ORMD | | | |
| | 1 | LWA | | | | ALEMD | | | | AMCD | | | | EORMD | | | |
| | 2 | INEMD i(4) | | | | | | | | | | | | | | | |
| | 3 | ILEMD i(4) | | | | | | | | | | | | | | | |
| | 4 | COMB | | | | OR | | | | STS | | | | SBY | STOP | | |
| | 5 | JMPL p(4) | | | | | | | | | | | | | | | |
| | 6 | CALL p(4) | | | | | | | | | | | | | | | |
| | 7 | BRL p(4) | | | | | | | | | | | | | | | |
| | 8 | XMAD | | | | SEMD n(2) | | | | REMD n(2) | | | | TMD n(2) | | | |
| | 9 | LAMD | | | | LMAD | | | | SMCD | | | | ANMD | | | |
| | A | LMID i(4) | | | | | | | | | | | | | | | |
| | B | P p(4) | | | | | | | | | | | | | | | |
| | C | CAL a(6) | | | | | | | | | | | | | | | |
| | D | | | | | | | | | | | | | | | | |
| | E | | | | | | | | | | | | | | | | |
| | F | | | | | | | | | | | | | | | | |
| 1 | 0 | BR b(8) | | | | | | | | | | | | | | | |
| | 1 | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | |
| | 4 | | | | | | | | | | | | | | | | |
| | 5 | | | | | | | | | | | | | | | | |
| | 6 | | | | | | | | | | | | | | | | |
| | 7 | | | | | | | | | | | | | | | | |
| | 8 | | | | | | | | | | | | | | | | |
| | 9 | | | | | | | | | | | | | | | | |
| | A | | | | | | | | | | | | | | | | |
| | B | | | | | | | | | | | | | | | | |
| | C | | | | | | | | | | | | | | | | |
| | D | | | | | | | | | | | | | | | | |
| | E | | | | | | | | | | | | | | | | |
| | F | | | | | | | | | | | | | | | | |

1-word/2-cycle instruction

1-word/3-cycle instruction

RAM direct address instruction (2-word/2-cycle)

2-word/2-cycle instruction

## Absolute Maximum Ratings

| Item | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | –0.3 to +7.0 | V | |
| Programming voltage | $V_{PP}$ | –0.3 to +14.0 | V | 1 |
| Pin voltage | $V_T$ | –0.3 to $V_{CC}$+0.3 | V | |
| Allowable input current (total) | $\sum I_0$ | 100 | mA | 2 |
| Allowable output current (total) | $-\sum I_0$ | 50 | mA | 3 |
| Allowable input current (per pin) | $I_0$ | 4 | mA | 4,5 |
| | | 30 | mA | 4,6 |
| Allowable output current (per pin) | $-I_0$ | 4 | mA | 7,8 |
| | | 20 | mA | 7,9 |
| Operating temperature | Topr | –20 to +75 | °C | 10, 12 |
| | | –40 to +85 | °C | 11, 12 |
| Storage temperature | Tstg | –55 to +125 | °C | 13 |

Notes: Permanent damage may occur if these maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to the HD407A4374, HD407C4374, HD407A4384, HD407C4384, HD407A4389, and HD407C4389 TEST ($V_{PP}$) pin.
2. The allowable input current (total) is the sum of all currents flowing from I/O pins to ground at the same time.
3. The allowable output current (total) is the sum of all currents flowing from $V_{CC}$ to I/O pins.
4. The allowable input current (per pin) is the maximum current allowed to flow from any one I/O pin to ground.
5. Applies to pins $D_0$ to $D_3$, $D_8$, $D_9$ and port R.
6. Applies to pins $D_4$ to $D_7$.
7. The allowable output current (per pin) is the maximum current allowed to flow from $V_{CC}$ to any one I/O pin.
8. Applies to pins $D_4$ to $D_9$ and port R.
9. Applies to pins $D_0$ to $D_3$.
10. Applies to Mask ROM
11. Applies to ZTAT™.
12. The operating temperature indicates the temperature range in which power can be supplied to the LSI (voltage Vcc shown in the electrical characteristics tables can be applied).
13. In the case of chips, the storage specification differs from that of the package products. Please consult your Hitachi sales representative for details.

## Electrical Characteristics

**DC Characteristics (HD404372, HD40A4372, HD40C4372, HD404374, HD40A4374, HD40C4374, HD404382, HD40A4382, HD40C4382, HD404384, HD40A4384, HD40C4384, HD404388, HD40A4388, HD40C4388, HD404389, HD40A4389, HD40C4389, HD404081, HD40A4081, HD40C4081, HD404082, HD40A4082, HD40C4082, HD404084, HD40A4084, HD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C; HCD404082, HCD40C4082, HCD404084, HCD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = +75°C; HD407A4374, HD407C4374, HD407A4384, HD407C4384, HD407A4389, HD407C4389: $V_{CC}$ = 2.0 V to 5.5 V, GND = 0 V, $T_a$ = –40°C to +85°C, unless otherwise specified)**

| Item | Symbol | Pins | min. | typ. | max. | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $\overline{RESET}$, $\overline{SCK}$, SI, $\overline{INT_0}$, $\overline{WU_0}$, EVNB | 0.90$V_{CC}$ | — | $V_{CC}$+0.3 | V | | |
| | | $OSC_1$ | $V_{CC}$–0.3 | — | $V_{CC}$+0.3 | V | External clock operation | |
| Input low voltage | $V_{IL}$ | $\overline{RESET}$, $\overline{SCK}$, SI, $\overline{INT_0}$, $\overline{WU_0}$, EVNB | –0.3 | — | 0.10$V_{CC}$ | V | | |
| | | $OSC_1$ | –0.3 | — | 0.3 | V | External clock operation | |
| Output high voltage | $V_{OH}$ | $\overline{SCK}$, SO, TOB, TOC | $V_{CC}$–0.5 | — | — | V | $–I_{OH}$=0.3mA | |
| Output low voltage | $V_{OL}$ | $\overline{SCK}$, SO, TOB, TOC | — | — | 0.4 | V | $I_{OL}$=0.4mA | |
| I/O leakage current | $\lvert I_{IL} \rvert$ | $\overline{RESET}$, $\overline{SCK}$, SI, $\overline{INT_0}$, $\overline{WU_0}$, EVNB, $OSC_1$, TOB, TOC, SO | — | — | 1 | µA | $V_{in}$=0V to $V_{CC}$ | 1 |
| Active mode current dissipation | $I_{CC1}$ | $V_{CC}$ | — | 1.5 | 3.5 | mA | $V_{CC}$=5V, $f_{OSC}$=4MHz | 2, 7 |
| | | | — | 1.2 | 2.5 | mA | | 2, 8 |
| | $I_{CC2}$ | | — | 0.4 | 1.0 | mA | $V_{CC}$=3V, $f_{OSC}$=800kHz | 2, 7 |
| | | | — | 0.3 | 0.7 | mA | | 2, 8 |
| | $I_{CC3}$ | | — | 2.7 | 9.0 | mA | $V_{CC}$=5V, $f_{OSC}$=8MHz | 2, 9 |
| | | | — | 2.2 | 4.5 | mA | | 2, 10 |
| Standby mode current dissipation | $I_{SBY1}$ | $V_{CC}$ | — | 1.0 | 1.5 | mA | $V_{CC}$=5V, $f_{OSC}$=4MHz | 3, 7 |
| | | | — | 0.6 | 1.3 | mA | | 3, 8 |
| | $I_{SBY2}$ | | — | 0.3 | 0.6 | mA | $V_{CC}$=3V, $f_{OSC}$=800kHz | 3, 7 |
| | | | — | 0.2 | 0.5 | mA | | 3, 8 |
| | $I_{SBY3}$ | | — | 1.4 | 4.0 | mA | $V_{CC}$=5V, $f_{OSC}$=8MHz | 3, 9 |
| | | | — | 1.0 | 2.5 | mA | | 3, 10 |

| Item | Symbol | Pins | min. | typ. | max. | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Subactive mode current dissipation | $I_{SUB}$ | $V_{CC}$ | — | 18 | 35 | µA | $V_{CC}$ = 3V, 32 kHz oscillator used | 4, 5 |
| Watch mode current dissipation | $I_{WTC}$ | $V_{CC}$ | — | 6 | 10 | µA | $V_{CC}$ = 3 V, 32 kHz oscillator used | 4, 5 |
| Stop mode current dissipation | $I_{STOP}$ | $V_{CC}$ | — | — | 5 | µA | $V_{CC}$ = 3 V, no 32 kHz oscillator | 4 |
| Stop mode retention voltage | $V_{STOP}$ | $V_{CC}$ | 1.5 | — | — | V | no 32 kHz oscillator | 6 |

Notes: 1. Excludes output buffer current.

2. Power supply current when the MCU is in the reset state and there are no I/O currents.

| | | |
|---|---|---|
| Test Conditions | MCU State | • Reset state |
| | Pin States | • $\overline{\text{RESET}}$, TEST: At ground |

3. Power supply current when the on-chip timers are operating and there are no I/O currents.

| | | |
|---|---|---|
| Test Conditions | MCU State | • I/O: Same as reset state<br>• Standby mode<br>• $f_{cyc} = f_{OSC}/4$ |
| | Pin States | • $\overline{\text{RESET}}$: At $V_{CC}$<br>• TEST: At ground<br>• D port, R port: At $V_{CC}$ |

4. Power supply current when there are no I/O currents.

| | | |
|---|---|---|
| Test Conditions | Pin States | • $\overline{\text{RESET}}$: At $V_{CC}$<br>• TEST: At ground<br>• D port, R port: At $V_{CC}$ |

5. Applies to HD404374 Series.
6. Voltage needed to retain RAM data.
7. Applies to HD404374, HD404384, and HD404389 Series.
8. Applies to HD404082 and HD404084 Series.
9. Applies to HD40A4374/2, HD407A4374, HD40A4384/2, HD407A4384, HD40A4389/8 and HD407A4389.
10. Applies to HD40A4082/1 and HD40A4084.

**I/O Characteristics for Standard Pins DC Characteristics (HD404372, HD40A4372, HD40C4372, HD404374, HD40A4374, HD40C4374, HD404382, HD40A4382, HD40C4382, HD404384, HD40A4384, HD40C4384, HD404388, HD40A4388, HD40C4388, HD404389, HD40A4389, HD40C4389, HD404081, HD40A4081, HD40C4081, HD404082, HD40A4082, HD40C4082, HD404084, HD40A4084, HD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C; HCD404082, HCD40C4082, HCD404084, HCD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = +75°C; HD407A4374, HD407C4374, HD407A4384, HD407C4384, HD407A4389, HD407C4389: $V_{CC}$ = 2.0 V to 5.5 V, GND = 0 V, $T_a$ = –40°C to +85°C, unless otherwise specified)**

| Item | Symbol | Pins | min. | typ. | max. | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | R port, $D_8$, $D_9$ | $0.7V_{CC}$ | — | $V_{CC}$+0.3 | V | | |
| Input low voltage | $V_{IL}$ | R port, $D_8$, $D_9$ | –0.3 | — | $0.3V_{CC}$ | V | | |
| Output high voltage | $V_{OH}$ | R port, $D_8$, $D_9$ | $V_{CC}$–0.5 | — | — | V | $–I_{OH}$=0.3mA | |
| Output low voltage | $V_{OL}$ | R port, $D_8$, $D_9$ | — | — | 0.4 | V | $I_{OL}$=0.4mA | |
| I/O leakage current | $\lvert I_{IL} \rvert$ | R port, $D_8$, $D_9$ | — | — | 1 | µA | $V_{in}$=0V to $V_{CC}$ | 1 |
| MOS pull-up current | $–I_{PU}$ | R port, $D_8$, $D_9$ | 10 | 50 | 150 | µA | $V_{CC}$=3V, $V_{in}$=0V | |

Note: 1. Excludes output buffer current.

**I/O Characteristics for High-Current Pins DC Characteristics (HD404372, HD40A4372, HD40C4372, HD404374, HD40A4374, HD40C4374, HD404382, HD40A4382, HD40C4382, HD404384, HD40A4384, HD40C4384, HD404388, HD40A4388, HD40C4388, HD404389, HD40A4389, HD40C4389, HD404081, HD40A4081, HD40C4081, HD404082, HD40A4082, HD40C4082, HD404084, HD40A4084, HD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C; HCD404082, HCD40C4082, HCD404084, HCD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = +75°C; HD407A4374, HD407C4374, HD407A4384, HD407C4384, HD407A4389, HD407C4389: $V_{CC}$ = 2.0 V to 5.5 V, GND = 0 V, $T_a$ = –40°C to +85°C, unless otherwise specified)**

| Item | Symbol | Pins | min. | typ. | max. | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $D_0$ to $D_7$ | $0.7V_{CC}$ | — | $V_{CC}$+0.3 | V | | |
| Input low voltage | $V_{IL}$ | $D_0$ to $D_7$ | –0.3 | — | $0.3V_{CC}$ | V | | |
| Output high voltage | $V_{OH}$ | $D_4$ to $D_7$ | $V_{CC}$–0.5 | — | — | V | $–I_{OH}$=0.3mA | |
| | | $D_0$ to $D_3$ | $V_{CC}$–2.0 | — | — | V | $–I_{OH}$=10mA, $V_{CC}$=4.5 to 5.5V | |
| Output low voltage | $V_{OL}$ | $D_0$ to $D_3$ | — | — | 0.4 | V | $I_{OL}$=0.4mA | |
| | | $D_4$ to $D_7$ | — | — | 2.0 | V | $I_{OL}$=15mA $V_{CC}$=4.5V to 5.5V | |
| I/O leakage current | $\lvert I_{IL} \rvert$ | $D_0$ to $D_7$ | — | — | 1 | µA | $V_{in}$ =0V to $V_{CC}$ | 1 |
| MOS pull-up current | $–I_{PU}$ | $D_0$ to $D_7$ | 10 | 50 | 150 | µA | $V_{CC}$=3V, $V_{in}$=0V | |

Note: 1. Excludes output buffer current.

**A/D Converter Characteristics (HD404374/HD404384/HD404389 Series) (Mask ROM: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C; ZTAT™: $V_{CC}$ = 2.0 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C, unless otherwise specified)**

| Item | Symbol | Pins | min. | typ. | max. | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Analog power supply voltage | $AV_{CC}$ | $AV_{CC}$ | $V_{CC}$–0.3 | $V_{CC}$ | $V_{CC}$+0.3 | V | | 1 |
| Analog input voltage | $AV_{in}$ | $AN_0$ to $AN_5$ | $AV_{SS}$ | — | $AV_{CC}$ | V | | |
| $AV_{CC}$-$AV_{SS}$ current | $I_{AD}$ | | — | — | 500 | µA | $V_{CC}$=$AV_{CC}$=5.0V | |
| Analog input capacitance | $CA_{in}$ | $AN_0$ to $AN_5$ | — | 15 | — | pF | | |
| Resolution | | | — | 10 | — | bit | | |
| Number of inputs | | | 0 | — | 4 | channel | | |
| Absolute accuracy | | | — | — | ±4.0 | LSB | $V_{CC}$=$AV_{CC}$=1.8V to 5.5V | 2 |
| | | | | | | | $V_{CC}$=$AV_{CC}$=2.0V to 5.5V | 3 |
| Conversion time | | | 125 | — | — | $t_{cyc}$ | $V_{CC}$=$AV_{CC}$=1.8V to 2.0V or less | 2 |
| | | | 65 | — | — | $t_{cyc}$ | $V_{CC}$=$AV_{CC}$=2.0V to 5.5V | |
| Input impedance | | $AN_0$ to $AN_5$ | 1 | — | — | MΩ | | |

Notes: 1. Connect to the $V_{CC}$ pin when the A/D converter is not used. The $AV_{CC}$ setting range is 1.8 V≤$AV_{CC}$≤5.5V (Mask ROM), 2.0V ≤ $AV_{CC}$ ≤ 5.5V (ZTAT™).
2. Applies to Mask ROM.
3. Applies to ZTAT™.

**AC Characteristics DC Characteristics (HD404372, HD40A4372, HD40C4372, HD404374, HD40A4374, HD40C4374, HD404382, HD40A4382, HD40C4382, HD404384, HD40A4384, HD40C4384, HD404388, HD40A4388, HD40C4388, HD404389, HD40A4389, HD40C4389, HD404081, HD40A4081, HD40C4081, HD404082, HD40A4082, HD40C4082, HD404084, HD40A4084, HD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C; HCD404082, HCD40C4082, HCD404084, HCD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = +75°C; HD407A4374, HD407C4374, HD407A4384, HD407C4384, HD407A4389, HD407C4389: $V_{CC}$ = 2.0 V to 5.5 V, GND = 0 V, $T_a$ = –40°C to +85°C, unless otherwise specified)**

| Item | Symbol | Pins | min. | typ. | max. | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Clock oscillation frequency (ceramic oscillator, crystal oscillator) | $f_{OSC}$ | $OSC_1$, $OSC_2$ | 0.4 | — | 4.5 | MHz | Division by 4 | 1 |
| | | | 0.4 | — | 8.5 | | | 1, 3 |
| | $f_x$ | X1,X2 | — | 32.768 | — | kHz | | 4 |
| Clock oscillation frequency (Resistance oscillation) | $f_{OSC}$ | $OSC_1$, $OSC_2$ | 0.5 | 2.0 | 3.5 | MHz | Division by 4<br>Rf=20 kΩ | 2, 13 |
| | | | 0.5 | 2.2 | 3.5 | | | 2, 12 |
| Instruction cycle time (external clock, ceramic oscillator, crystal oscillator) | $t_{cyc}$ | | 0.89 | — | 10 | µs | Division by 4 | |
| | | | 0.47 | — | 10 | | | 3 |
| | $t_{subcyc}$ | | — | 244.14 | — | µs | 32 kHz oscillator used, division by 8 | 4 |
| | | | — | 122.07 | — | µs | 32 kHz oscillator used, division by 4 | 4 |
| Instruction cycle time (Resistance oscillation) | $t_{cyc}$ | | 1.14 | — | 8.0 | µs | Division by 4<br>Rf=20 kΩ | 5 |
| Oscillation settling time (external clock input) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 7.5 | ms | | 6 |
| Oscillation settling time (ceramic oscillator) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 7.5 | ms | $V_{CC}$=2.0 to 5.5V | 6 |
| Oscillation settling time(crystal oscillator) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 30 | ms | $V_{CC}$=2.0 to 5.5V | 6 |
| | | X1,X2 | — | — | 2 | s | $T_a$=–10 to +60°C,<br>$V_{CC}$=2.0 to 5.5V | 4, 6 |
| Oscillation setting time (Resistance oscillation) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 0.5 | ms | Rf=20 kΩ<br>$V_{CC}$=2.0 to 5.5V | 5, 6 |
| External clock high-level width | $t_{CPH}$ | $OSC_1$ | 105 | — | — | ns | $f_{OSC}$=4MHz | 7 |
| | | | 52.5 | | | | $f_{OSC}$=8MHz | 3, 7 |
| External clock low-level width | $t_{CPL}$ | $OSC_1$ | 105 | — | — | ns | $f_{OSC}$=4MHz | 7 |
| | | | 52.5 | | | | $f_{OSC}$=8MHz | 3, 7 |
| External clock rise time | $t_{CPr}$ | $OSC_1$ | — | — | 20 | ns | $f_{OSC}$=4MHz | 7 |
| | | | | | 10 | | $f_{OSC}$=8MHz | 3, 7 |

| Item | Symbol | Pins | min. | typ. | max. | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| External clock fall time | $t_{CPf}$ | $OSC_1$ | — | — | 20 | ns | $f_{OSC}$=4MHz | 7 |
| | | | | | 10 | | $f_{OSC}$=8MHz | 3, 7 |
| $\overline{INT_0}$, EVNB, $\overline{WU_0}$, high-level width | $t_{IH}$ | $\overline{INT_0}$, EVNB, $\overline{WU_0}$ | 2 | — | — | $t_{cyc}/t_{subcyc}$ | | 8 |
| $\overline{INT_0}$, EVNB, $\overline{WU_0}$, low-level width | $t_{IL}$ | $\overline{INT_0}$, EVNB, $\overline{WU_0}$ | 2 | — | — | $t_{cyc}/t_{subcyc}$ | | 8 |
| $\overline{RESET}$ low-level width | $t_{RSTL}$ | $\overline{RESET}$ | 2 | — | — | $t_{cyc}$ | | 9 |
| $\overline{RESET}$ rise time | $t_{RSTr}$ | $\overline{RESET}$ | — | — | 20 | ms | | 9 |
| Input capacitance | $C_{in}$ | All input pins except TEST | — | — | 15 | pF | f=1MHz,$V_{in}$=0V | |
| | | TEST | — | — | 15 | pF | | 10 |
| | | TEST | — | — | 40 | pF | | 11 |
| Capacitance between $OSC_1$ and $OSC_2$ (Resistance oscillation) | $C_{RF}$ | $OSC_1$, $OSC_2$ | — | — | 1 | pF | | 5 |

Notes:
1. When the subsystem oscillator (32.768 kHz crystal oscillation) is used, use within the range 0.4 MHz≤$f_{OSC}$≤1.0 MHz or 1.6 MHz≤$f_{OSC}$≤8.5 MHz. The SSR1 bit of the system clock select register (SSR) should be set to 0 and 1, respectively.
2. The typ. value is the value when $V_{CC}$ = 3.5 V.
3. Applies to HD40A4372/4, HD40A4382/4, HD40A4388/9, HD40A4081/2, HD40A4084, HD407A4374, HD407A4384 and HD407A4389 when $V_{CC}$ = 4.0 to 5.5 V.
4. Applies to HD404374 Series.
5. Applies to HD40C4372/4, HD407C4374, HD40C4382/4, HD407C4384, HD40C4388/9, HD407C4389, HD40C4081/2, HCD40C4082, HD40C4084, HCD40C4084.
6. The oscillation settling time is defined as follows:
   (1) The time required for the oscillation to settle after $V_{CC}$ has reached standard minimum at power-on.
   (2) The time required for the oscillation to settle after $\overline{RESET}$ input has gone low when stop mode is cleared.

   To ensure enough time for the oscillation to settle at power-on hold the $\overline{RESET}$ input low for at least time $t_{RC}$. The oscillation settling time will depend on the circuit constants and stray capacitance. The resonator should be determined in consultation with the resonator manufacturer. With regard to the system clock ($OSC_1$, $OSC_2$), bits MIS1 and MIS0 in the miscellaneous register (MIS) should be set according to the oscillation settling time of the resonator used.
7. See figure 79.
8. See figure 80.
9. See figure 81.
10. Applies to Mask ROM.
11. Applies to ZTAT™.
12. Applies to HD40C4081/2, HCD40C4082, HD40C4084, HCD40C4084.
13. Applies to HD40C4372/4, HD407C4374, HD40C4382/4, HD407C4384, HD40C4388/9, HD407C4389.

**Serial interface timing characteristics DC Characteristics (HD404372, HD40A4372, HD40C4372, HD404374, HD40A4374, HD40C4374, HD404382, HD40A4382, HD40C4382, HD404384, HD40A4384, HD40C4384, HD404388, HD40A4388, HD40C4388, HD404389, HD40A4389, HD40C4389, HD404081, HD40A4081, HD40C4081, HD404082, HD40A4082, HD40C4082, HD404084, HD40A4084, HD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C; HCD404082, HCD40C4082, HCD404084, HCD40C4084: $V_{CC}$ = 1.8 V to 5.5 V, GND = 0 V, $T_a$ = +75°C; HD407A4374, HD407C4374, HD407A4384, HD407C4384, HD407A4389, HD407C4389: $V_{CC}$ = 2.0 V to 5.5 V, GND = 0 V, $T_a$ = –40°C to +85°C, unless otherwise specified)**

| Item | Symbol | Pins | min. | typ. | max. | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Serial clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | See load in figure 83 | 1 |
| Serial clock high-level width | $t_{SCKH}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | See load in figure 83 | 1 |
| Serial clock low-level width | $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | See load in figure 83 | 1 |
| Serial clock rise time | $t_{SC\ Kr}$ | $\overline{SCK}$ | — | — | 100 | ns | See load in figure 83 | 1 |
| Serial clock fall time | $t_{SCKf}$ | $\overline{SCK}$ | — | — | 100 | ns | See load in figure 83 | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 300 | ns | See load in figure 83 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 200 | — | — | ns | | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 200 | — | — | ns | | 1 |

### During Serial Clock Input

| Item | Symbol | Pins | min. | typ. | max. | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Serial clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | | 1 |
| Serial clock high-level width | $t_{SCKH}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | | 1 |
| Serial clock low-level width | $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | | 1 |
| Serial clock rise time | $t_{SC\ Kr}$ | $\overline{SCK}$ | — | — | 100 | ns | | 1 |
| Serial clock fall time | $t_{SCKf}$ | $\overline{SCK}$ | — | — | 100 | ns | | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 300 | ns | See load in figure 83 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 200 | — | — | ns | | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 200 | — | — | ns | | 1 |

Note: 1. See figure 82.

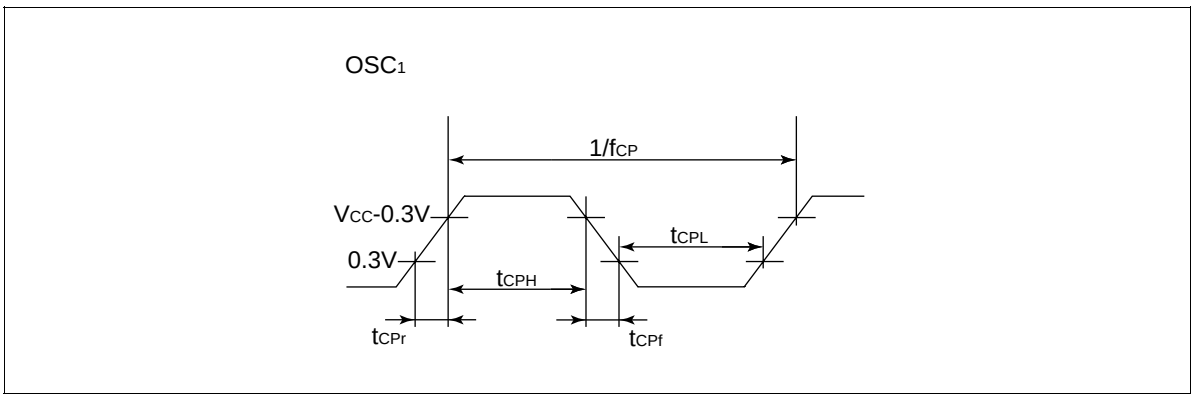



**Figure 79 External Clock Input Waveform**

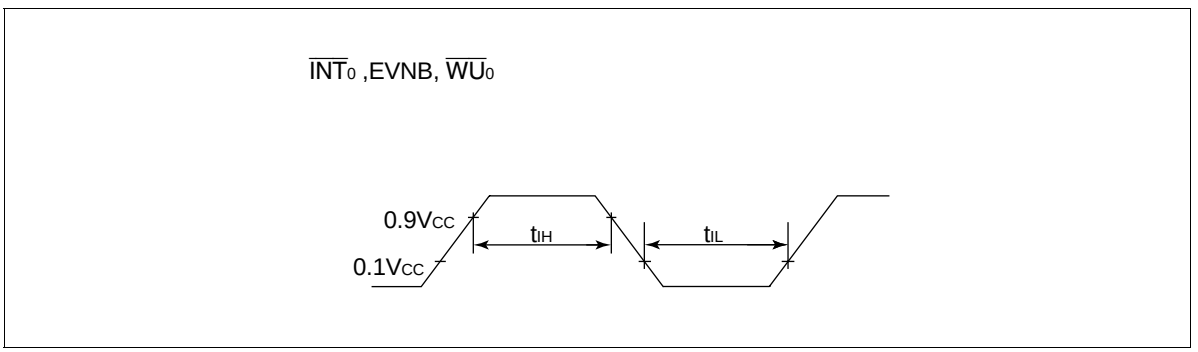



**Figure 80 Interrupt Timing**

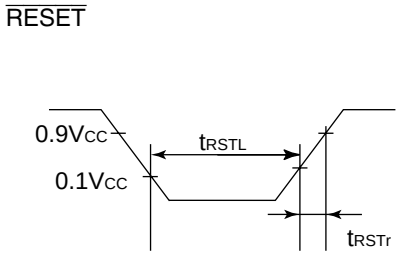
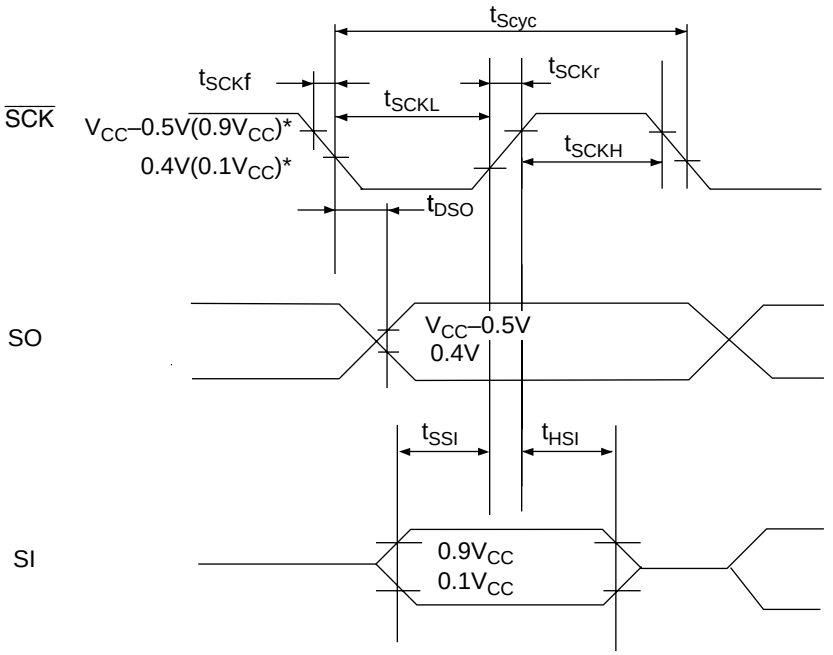



**Figure 81 Reset Timing**




Note : * $V_{CC}$–0.5V and 0.4V are the voltages during serial clock output.
0.9 $V_{CC}$ and 0.1 $V_{CC}$ are the voltages during serial clock input.

**Figure 82 Serial Interface Timing**

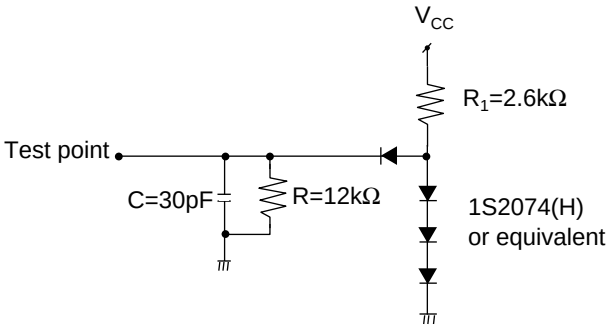
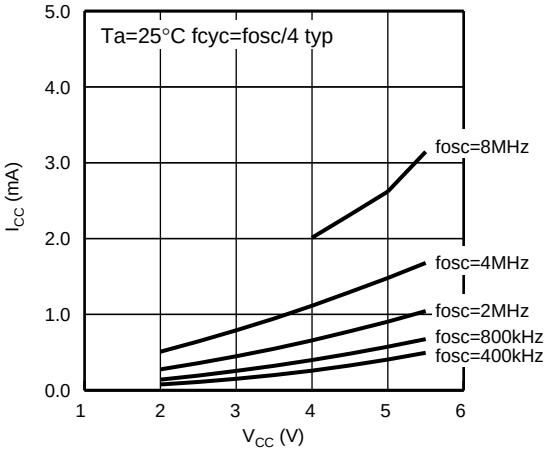
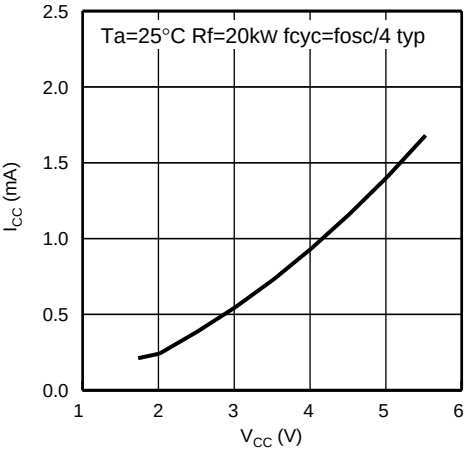


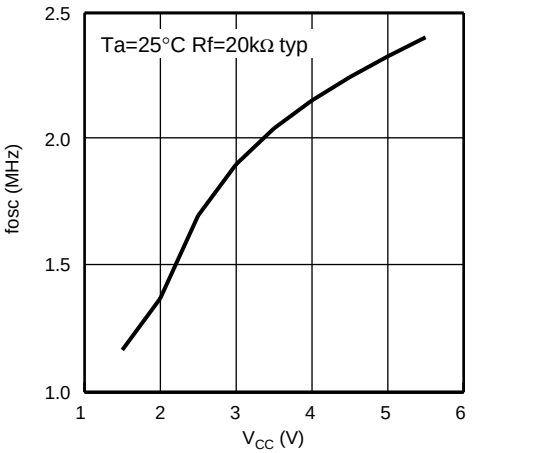

**Figure 83 Timing Load Circuit**



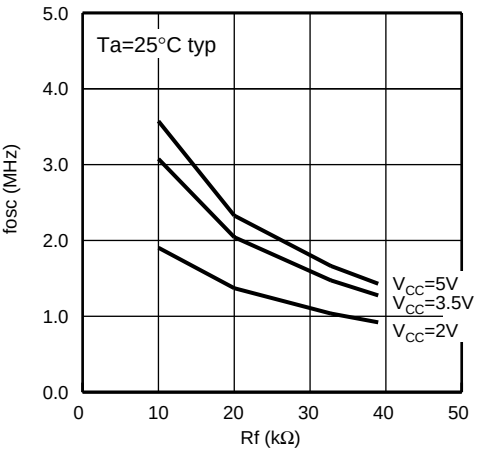

**(a) $I_{CC}$ vs. $V_{CC}$ characteristic (ceramic oscillation, crystal oscillation)**



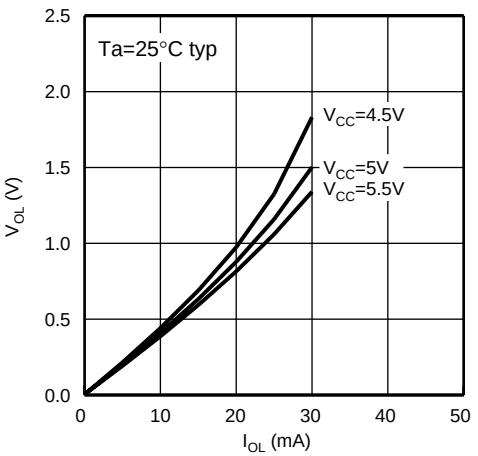

**(b) $I_{CC}$ vs. $V_{CC}$ characteristic (resistance oscillation)**



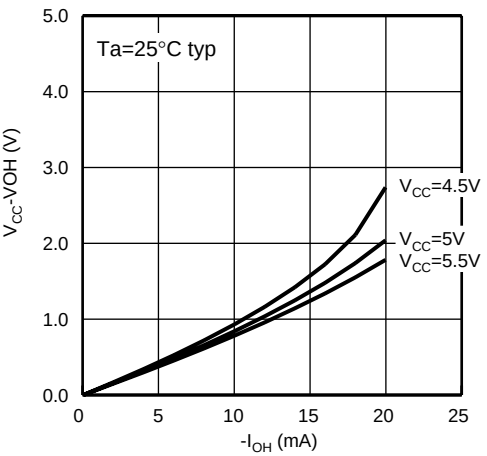

**(c) fosc vs. $V_{CC}$ characteristic (resistance oscillation)**




**(d) fosc vs. Rf characteristic (resistance oscillation)**

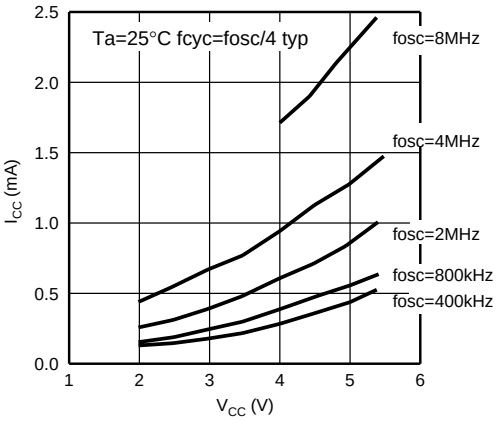



**(e) $V_{OL}$ vs. $I_{OL}$ characteristic (pins D4 to D7)**

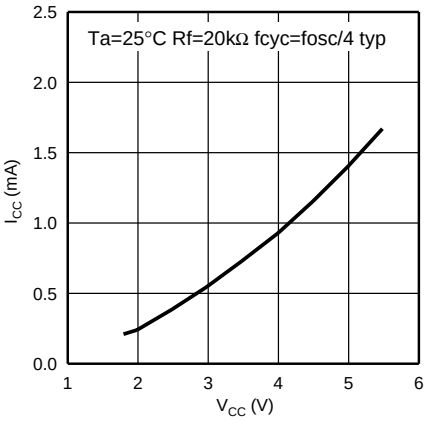



**(f) $V_{CC}$ - $V_{OH}$ vs. $I_{OH}$ characteristic (pins D0 to D3)**

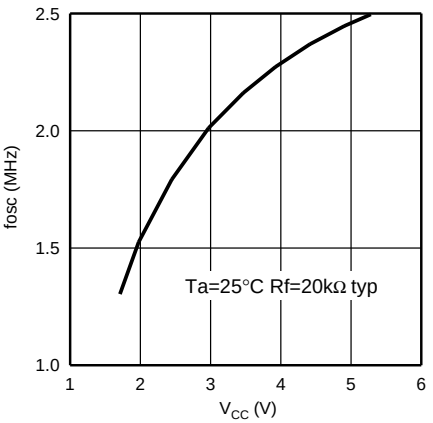
**Figure 84 HD404374, HD404384, and HD404389 Series Characteristic Curves (Reference Values)**



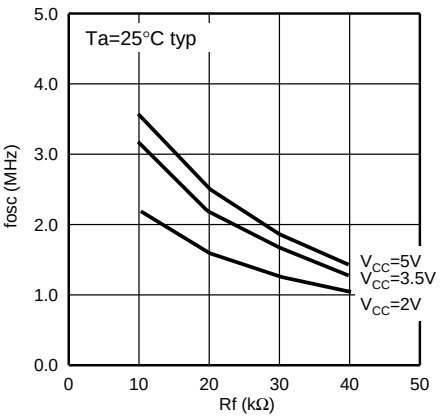

**(a) $I_{CC}$ vs. $V_{CC}$ characteristic (ceramic oscillation, crystal oscillation)**



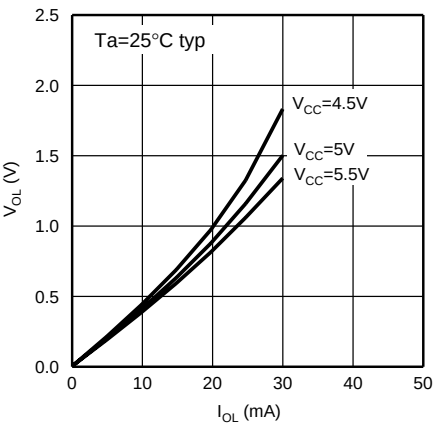

**(b) $I_{CC}$ vs. $V_{CC}$ characteristic (resistance oscillation)**



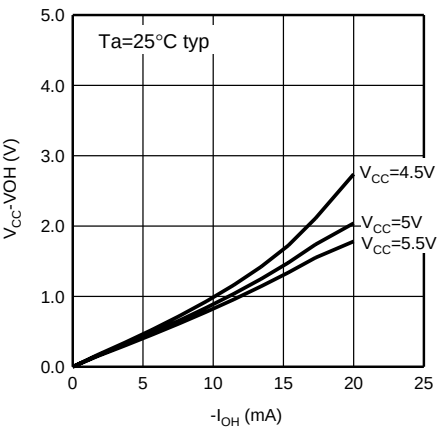

**(c) fosc vs. $V_{CC}$ characteristic (resistance oscillation)**




**(d) fosc vs. Rf characteristic (resistance oscillation)**




**(e) $V_{OL}$ vs. $I_{OL}$ characteristic (pins D4 to D7)**

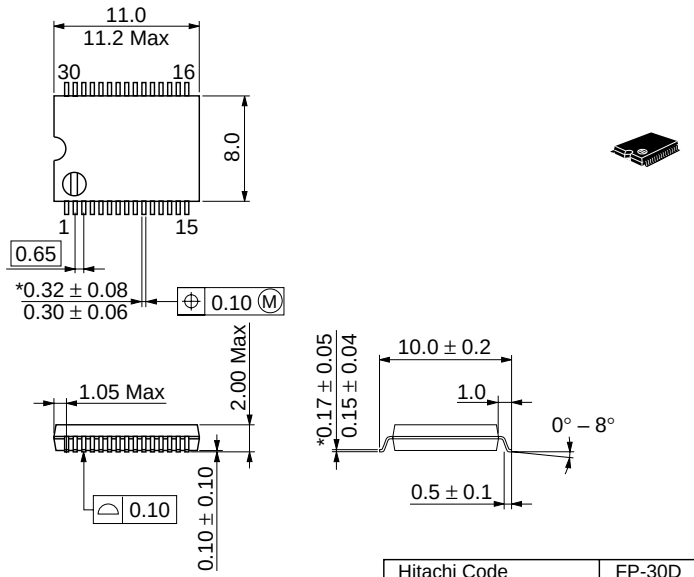



**(f) $V_{CC}$ - $V_{OH}$ vs. $I_{OH}$ characteristic (pins D0 to D3)**

**Figure 85 HD404082 and HD404084 Series Characteristic Curves (Reference Values)**

## Package Dimensions

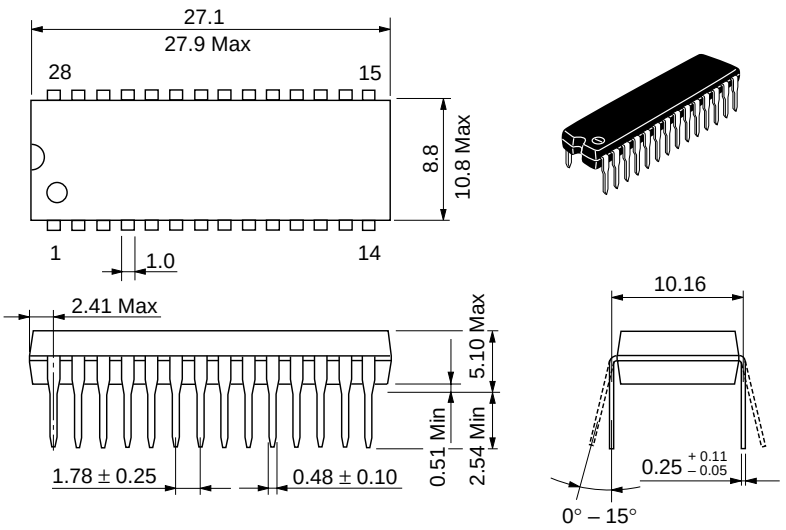
Unit: mm




| | |
|---|---|
| Hitachi Code | FP-30D |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | — |

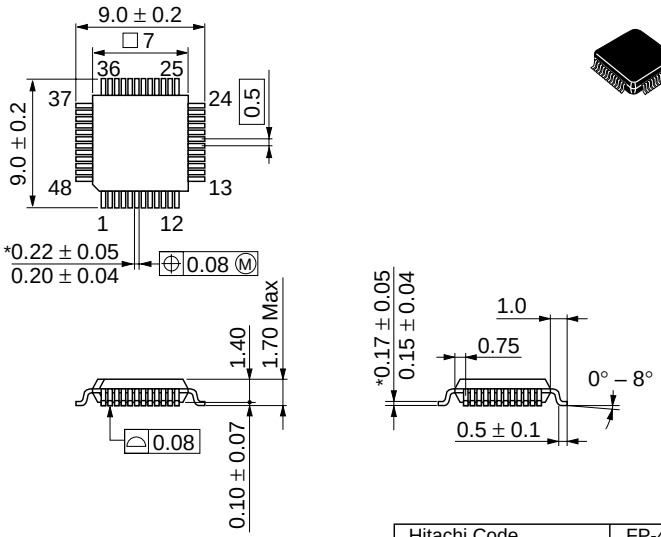
*Dimension including the plating thickness
Base material dimension

Unit: mm




| | |
|---|---|
| Hitachi Code | DP-28S |
| JEDEC | — |
| EIAJ | Conforms |
| Weight (reference value) | 1.9 g |

Unit: mm



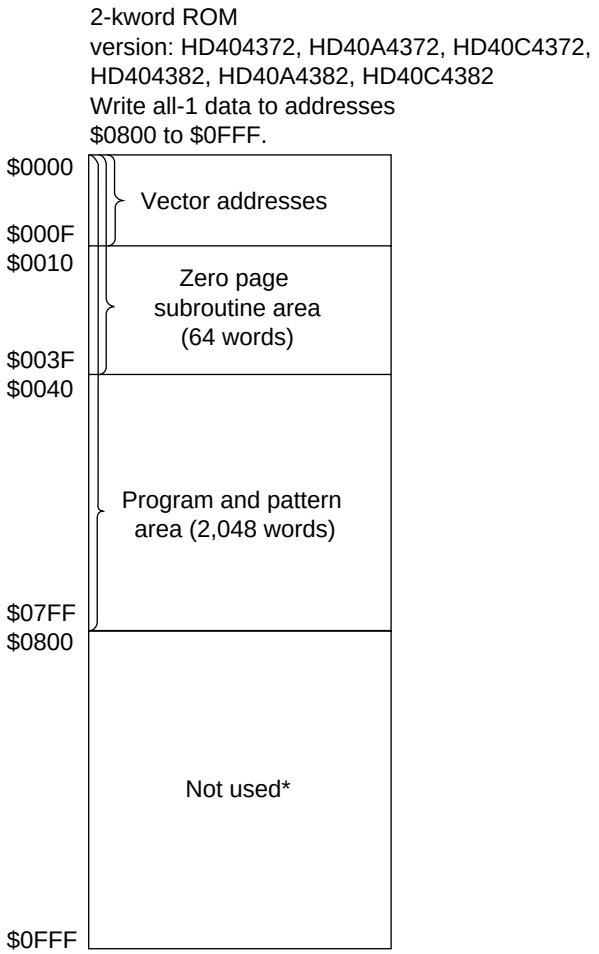

*Dimension including the plating thickness
Base material dimension

| | |
|---|---|
| Hitachi Code | FP-48B |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.2 g |

## Note on ROM Ordering

Please note the following when ordering HD404372, HD40A4372, HD40C4372, HD404382, HD40A4382 and HD40C4382 ROM.

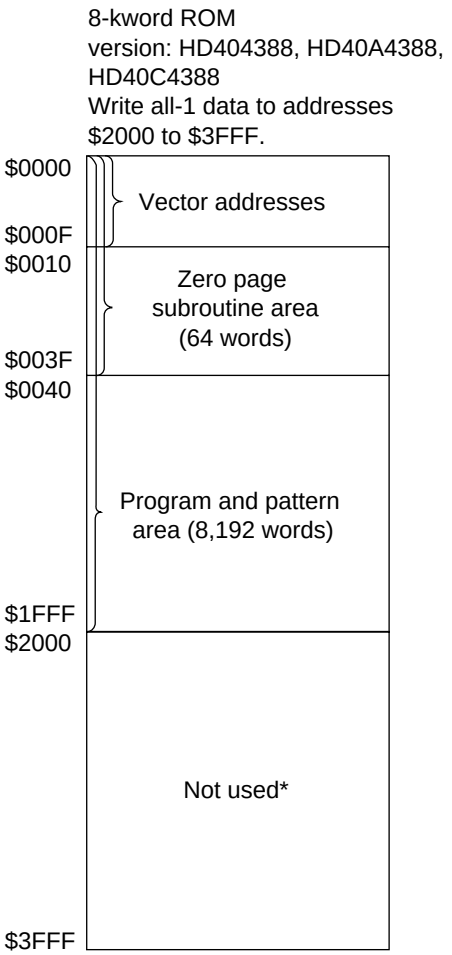
When ordering ROM, please fill the "Not used" areas below with all-1 data, to give the same amount of data as for the 4-kwords version (HD404374, HD40A4374, HD40C4372, HD404384, HD40A4384, HD40C4384). The program that converts ROM data to mask drawing data is the same as that used for the 4-kwords version, and therefore the same amount of data is necessary. This applies both to orders using EPROM and orders using data transmission.




Note : Write all-1 data in not used area.

Please note the following when ordering HD404388, HD40A4388 and HD40C4388 ROM.

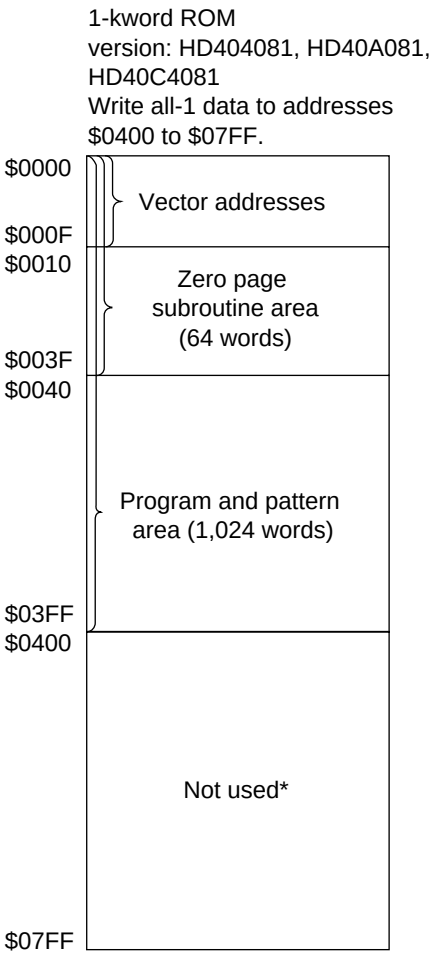
When ordering ROM, please fill the "Not used" areas below with all-1 data, to give the same amount of data as for the 16-kwords version (HD404389, HD40A4389, HD40C4389). The program that converts ROM data to mask drawing data is the same as that used for the 16-kwords version, and therefore the same amount of data is necessary. This applies both to orders using EPROM and orders using data transmission.




Note : Write all-1 data in not used area.

Please note the following when ordering HD404081, HD40A4081 and HD40C4081 ROM.

When ordering ROM, please fill the "Not used" areas below with all-1 data, to give the same amount of data as for the 2-kwords version (HD404082, HD40A4082, HD40C4082). The program that converts ROM data to mask drawing data is the same as that used for the 2-kwords version, and therefore the same amount of data is necessary. This applies both to orders using EPROM and orders using data transmission.




Note : Write all-1 data in not used area.

## Option List HD404372, HD404374, HD40A4372, HD40A4374, HD40C4372, HD40C4374

Please check off the appropriate applications and enter the necessary information.

| Date of order | Year | Month | Day |
|---|---|---|---|
| Customer | | | |
| Department | | | |
| Name | | | |
| ROM code name | | | |
| LSI number (Hitachi entry) | | | |

1. ROM Size

| | |
|---|---|
| ❑ Standard operation version: HD404372 | 2 kwords |
| ❑ High-speed operation version: HD40A4372 | |
| ❑ CR oscillation version: HD40C4372 | |
| ❑ Standard operation version: HD404374 | 4 kwords |
| ❑ High-speed operation version: HD40A4374 | |
| ❑ CR oscillation version: HD40C4374 | |

2. Function Options

| | |
|---|---|
| * ❑ | 32 kHz CPU operation, realtime clock time base |
| * ❑ | No 32 kHz CPU operation, realtime clock time base |
| ❑ | No 32 kHz CPU operation, no realtime clock time base |

Note: When an asterisked item is selected, "crystal resonator" is necessary for subsystem oscillator (X1 X2).

3. ROM Code Data Organization

For a microcomputer with EPROM mounted (including a ZTAT™ microcomputer), specify the combined upper/lower type.

❑ Combined lower/upper type

• Both the lower 5 data bits (L) and the upper 5 data bits (U) are written to a single EPROM in the order LULULU...

❑ Separate lower/upper type

• The lower 5 data bits (L) and upper 5 data bits (U) are written to separate EPROMs respectively.

4. System Oscillator (OSC1-OSC2) (Shading means selection is not available)

| | | HD404372/4, HD40A4372/4 | | HD40C4372/4 |
|---|---|---|---|---|
| ❑ | Ceramic oscillator | f = | MHz | |
| ❑ | Crystal oscillator | f = | MHz | |
| ❑ | External clock | f = | MHz | |
| ❑ | Resistance oscillator | | | |

5. Subsystem Oscillator (X1 X2)

| | | |
|---|---|---|
| ❑ | Not used | — |
| ❑ | Crystal resonator | f = 32.768 kHz |

6. Stop Mode

| | |
|---|---|
| ❑ | Yes (used) |
| ❑ | No (not used) |

7. Package

| | |
|---|---|
| ❑ | FP-30D |
| ❑ | FP-48B* |

Note: *The WS version will become available at the beginning of mass production.

## Option List HD404382, HD404384, HD40A4382, HD40A4384, HD40C4382, HD40C4384

Please check off the appropriate applications and enter the necessary information.

| | | | |
|---|---|---|---|
| Date of order | Year | Month | Day |
| Customer | | | |
| Department | | | |
| Name | | | |
| ROM code name | | | |
| LSI number (Hitachi entry) | | | |

1. ROM Size

| | |
|---|---|
| ❑ Standard operation version: HD404382 | 2 kwords |
| ❑ High-speed operation version: HD40A4382 | |
| ❑ CR oscillation version: HD40C4382 | |
| ❑ Standard operation version: HD404384 | 4 kwords |
| ❑ High-speed operation version: HD40A4384 | |
| ❑ CR oscillation version: HD40C4384 | |

2. ROM Code Data Organization

For a microcomputer with EPROM mounted (including a ZTAT™ microcomputer), specify the combined upper/lower type.

❑ Combined lower/upper type

- Both the lower 5 data bits (L) and the upper 5 data bits (U) are written to a single EPROM in the order LULULU...

❑ Separate lower/upper type

- The lower 5 data bits (L) and upper 5 data bits (U) are written to separate EPROMs respectively.

3. System Oscillator (OSC1-OSC2) (Shading means selection is not available)

| | HD404382/4, HD40A4382/4 | HD40C4382/4 |
|---|---|---|
| ❑ Crystal oscillator | f = MHz | |
| ❑ Ceramic oscillator | f = MHz | |
| ❑ External clock | f = MHz | |
| ❑ Resistance oscillator | | f = MHz |

4. Stop Mode

- ❑ Yes (used)
- ❑ No (not used)

5. Package

- ❑ FP-30D
- ❑ DP-28S
- ❑ FP-48B*

Note: *The WS version will become available at the beginning of mass production.

## Option List HD404388, HD404389, HD40A4388, HD40A4389, HD40C4388, HD40C4389

Please check off the appropriate applications and enter the necessary information.

| Date of order | Year | Month | Day |
|---|---|---|---|
| Customer | | | |
| Department | | | |
| Name | | | |
| ROM code name | | | |
| LSI number (Hitachi entry) | | | |

1. ROM Size

| | |
|---|---|
| ❑ Standard operation version: HD404388 | 8 kwords |
| ❑ High-speed operation version: HD40A4388 | |
| ❑ CR oscillation version: HD40C4388 | |
| ❑ Standard operation version: HD404389 | 16 kwords |
| ❑ High-speed operation version: HD40A4389 | |
| ❑ CR oscillation version: HD40C4389 | |

2. ROM Code Data Organization

For a microcomputer with EPROM mounted (including a ZTAT™ microcomputer), specify the combined upper/lower type.

| |
|---|
| ❑ Combined lower/upper type |
| • Both the lower 5 data bits (L) and the upper 5 data bits (U) are written to a single EPROM in the order LULULU... |
| ❑ Separate lower/upper type |
| • The lower 5 data bits (L) and upper 5 data bits (U) are written to separate EPROMs respectively. |

3. System Oscillator (OSC1-OSC2) (Shading means selection is not available)

| | HD404388/9, HD40A4388/9 | HD40C4388/9 |
|---|---|---|
| ❑ Crystal oscillator | f = MHz | |
| ❑ Ceramic oscillator | f = MHz | |
| ❑ External clock | f = MHz | |
| ❑ Resistance oscillator | | f = MHz |

4. Stop Mode

| |
|---|
| ❑ Yes (used) |
| ❑ No (not used) |

5. Package

| |
|---|
| ❑ FP-30D |

## Option List HD404081, HD404082, HCD404082, HD40A4081, HD40A4082, HD40C4081, HD40C4082, HCD40C4082

Please check off the appropriate applications and enter the necessary information.

| | | | |
|---|---|---|---|
| Date of order | Year | Month | Day |
| Customer | | | |
| Department | | | |
| Name | | | |
| ROM code name | | | |
| LSI number (Hitachi entry) | | | |

1. ROM Size

| | |
|---|---|
| ❑ Standard operation version: HD404081 | 1 kwords |
| ❑ High-speed operation version: HD40A4081 | |
| ❑ CR oscillation version: HD40C4081 | |
| ❑ Standard operation version: HD404082 | 2 kwords |
| ❑ Standard operation version: HCD404082 | |
| ❑ High-speed operation version: HD40A4082 | |
| ❑ CR oscillation version: HD40C4082 | |
| ❑ CR oscillation version: HCD40C4082 | |

2. System Oscillator (OSC1-OSC2) (Shading means selection is not available)

| | HD404081/2, HD40A4081/2, HCD404082 | HD40C4081/2, HCD40C4082 |
|---|---|---|
| ❑ Crystal oscillator | f = MHz | |
| ❑ Ceramic oscillator | f = MHz | |
| ❑ External clock | f = MHz | |
| ❑ Resistance oscillator | | f = MHz |

3. Stop Mode

| |
|---|
| ❑ Yes (used) |
| ❑ No (not used) |

4. Package

| |
|---|
| ❑ FP-30D |
| ❑ DP-28S |
| ❑ Chip |

Note: The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details.

## Option List HD404084, HCD404084, HD40A4084, HD40C4084, HCD40C4084

Please check off the appropriate applications and enter the necessary information.

| Date of order | Year | Month | Day |
|---|---|---|---|
| Customer | | | |
| Department | | | |
| Name | | | |
| ROM code name | | | |
| LSI number (Hitachi entry) | | | |

1. ROM Size

| | |
|---|---|
| ❑ Standard operation version: HD404084 | 4 kwords |
| ❑ Standard operation version: HCD404084 | |
| ❑ High-speed operation version: HD40A4084 | |
| ❑ CR oscillation version: HD40C4084 | |
| ❑ CR oscillation version: HCD40C4084 | |

2. System Oscillator (OSC1-OSC2) (Shading means selection is not available)

| | | HD404084, HD40A4084, HCD404084 | | HD40C4084, HCD40C4084 |
|---|---|---|---|---|
| ❑ | Crystal oscillator | f = | MHz | |
| ❑ | Ceramic oscillator | f = | MHz | |
| ❑ | External clock | f = | MHz | |
| ❑ | Resistance oscillator | | | |

3. Stop Mode

| | |
|---|---|
| ❑ | Yes (used) |
| ❑ | No (not used) |

4. Package

| | |
|---|---|
| ❑ | FP-30D |
| ❑ | DP-28S |
| ❑ | Chip |

Note: The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details.

## Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.