RX72T Group
Renesas MCUs

R01DS0331EJ0110
Rev.1.10
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200-MHz, 32-bit RX MCU, on-chip FPU, 1160 CoreMark, Supportive of 5V power supply, up to 1-MB flash memory, 128-KB SRAM, 32-KB data flash memory, 16-KB SRAM with ECC, Simultaneous sampling with 3 units of 12-bit A/D converter (up to 7 channels), Single-end/pseudo differential input supportive amplifier (6 channels), Analog comparator (6 channels), 200 MHz PWM (4 channels for 3-phase complementary, 2 channels for 5-phase complementary, 10 channels for single-phase complementary), 4-channel high-resolution PWM with resolution of 195 ps at the minimum, Host/function or OTG controller with full-speed USB 2.0 transfer, CAN, Encryption functions (optional)

Features

■ 32-bit RXv3 CPU core
- Maximum operating frequency: 200 MHz
  Capable of 1160 CoreMark in operation at 200 MHz
- JTAG and FINE (one-line) debugging interfaces
- A function for collectively saving the values of registers is available.

■ Low-power design and architecture
- Operation from a single 2.7- to 5.5-V supply
- Four low-power modes

■ On-chip code flash memory
- Supports versions with 1 Mbytes/512 Kbytes
- No wait cycles at up to 120 MHz or when the ROM cache is hit
- User code is programmable by on-board or off-board programming.

■ On-chip data flash memory
- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM, no wait states
- 128Kbytes of SRAM (no wait states)
- 16 Kbytes of RAM with ECC (with wait)

■ Data transfer
- DMACa: 8 channels
- DTCa: 1 channel

■ ELC
- Module operation can be initiated by event signals without using interrupts
- Linked operation between modules is possible when the CPU is in sleep mode

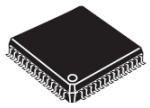
■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVDA) with voltage settings

■ Clock functions
- Frequency of resonator for main clock oscillator: 8 to 24 MHz (this can be used as the PLL reference clock)
- High-speed on-chip oscillator: 16 MHz/18 MHz/20 MHz (this can be used as the PLL reference clock)
- Low-speed on-chip oscillator: 240 kHz

■ Independent watchdog timer
- 120-kHz IWDT-dedicated on-chip oscillator clock operation

■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, functions for self-diagnosis and detection of disconnection for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test-assisting function by DOC, and CRCA, etc.
- Register write protection function can protect values in important registers against overwriting.

■ External bus
- Bus clock at 40 MHz (max)
- Four CS areas
- 8- or 16-bit bus space is selectable per area



PLQP0144KA-B 20 × 20 mm, 0.5 mm pitch
PLQP0100KB-B 14 × 14 mm, 0.5 mm pitch

■ Various communications interfaces
- Host/function or OTG controller (1 channel) with full-speed USB 2.0 (USBb) transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (1 channel)
- SCIj and SCIh with multiple functionalities (up to 6 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- SCIi with 16-byte transmission and reception FIFOs (1 channel)
- I^2C bus interface (RIICa) for transfer at up to 400 kbps (fast mode), capable of SMBus operation (1 channel)
- RSPId (1 channel) for transfer at up to 30 Mbps

■ Up to 31 extended-function timers
- 32-bit GPTW (10 channels): operation at 200 MHz, input capture, output compare, PWM waveforms: 10 output channels in single-phase complementary PWM mode/3 output channels in 3-phase complementary PWM mode/2 output channels in 5-phase complementary PWM mode, phase-counting mode, linkage with comparator (counting operation, PWM negate control)
- 16-bit MTU3d (9 channels): operation at 200 MHz, input capture, output compare, PWM waveforms: 2 output channels in 3-phase complementary PWM mode, phase-counting mode
- 8-bit TMR (8 channels)
- 16-bit CMT (4 channels)

■ High-resolution PWM waveform generation circuit (HRPWM): 4 channels
- Controlling the timing of rising or falling of the PWM output waveform for 32-bit GPTW is realized with minimum of 195 ps resolution (in operation at 160 MHz)

■ 12-bit A/D converter (S12ADH): total of 30 channels for three units
- Up to three 12-bit units of sample-and-hold circuit included
  Unit 0 (8 channels for 3 sample-and-hold circuits),
  Unit 1 (8 channels for 3 sample-and-hold circuits),
  Unit 2 (14 channels)
- Programmable gain amplifier with pseudo differential amplification (3 channels × 2)

■ Analog Comparator (CMPC): 6 channels

■ 12-bit D/A converter: 2 channels
- Usable as a reference voltage for the analog comparator

■ Temperature sensor for measuring temperature within the chip

■ Encryption functions (Trusted Secure IP Lite)
- 128- or 256-bit key length of AES for ECB, CBC, GCM, others
- True random number generator
- Unauthorized access to the encryption engine is disabled and imposture and falsification of information are prevented
- Safe management of keys

■ Up to 110 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Recommended operating temp. range (Topr)
- –40°C to +85°C
- –40°C to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package and the code flash memory capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/9)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 200 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • 113 instructions Standard provided instructions: 111 Basic instructions: 77 Single precision floating point instructions: 11 DSP instructions: 23 Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32/32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single-precision (32-bit) floating-point number • Data types and floating-point exceptions in conformance with the IEEE754 standard
	Register bank save function	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks
Memory	Code flash memory	• Capacity: 1 Mbyte, 512 Kbytes • ROM cache: Operation of an 8-Kbyte instruction fetching cache can be enabled or disabled (this is disabled by default). While ROM cache operation is enabled: - when the cache is hit, one-cycle access up to 200 MHz - when the cache is missed: one to two cycles if ICLK ≤ 120 MHz (bus wait: 0 cycles), two to three cycles if ICLK > 120 MHz (bus wait: 1 cycle). While ROM cache operation is disabled: one cycle if ICLK ≤ 120 MHz (bus wait: 0 cycles), two cycles if ICLK > 120 MHz (bus wait: 1 cycle). • On-board programming: Five types • Off-board programming (parallel programmer mode) • The trusted memory (TM) function protects against the reading of programs from blocks 8 and 9.
	Data flash memory	• Capacity: 32 Kbytes • Programming/erasing: 100,000 times
	Unique ID	• 12-byte unique ID for the device
	RAM	• Capacity: 128 Kbytes • 200 MHz No-wait access • SED (single error detection)
	RAM with ECC	• Capacity: 16 Kbytes • 00FF C000h to 00FF FFFFh (16 Kbytes) • SEC-DED (single error correction/double error detection)

Table 1.1 Outline of Specifications (2/9)

Classification	Module/Function	Description
Operating modes		• Operating modes by the mode-setting pins at the time of release from the reset state Single-chip mode Boot mode (SCI interface) Boot mode (USB interface) Boot mode (FINE interface) User boot mode • Selection of operating mode by register setting Single-chip mode, user boot mode, On-chip ROM disabled extended mode, On-chip ROM enabled extended mode • Endian selectable
Clock	Clock generation circuit	• Main clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 200 MHz Peripheral modules of MTU3 (Internal peripheral bus), GPTW (Internal peripheral bus), HRPWM (Internal peripheral bus), RSPI, and SCI11 run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz MTU3 (counter reference clocks), GPTW (counter reference clocks) are synchronized with PCLKC: Up to 200 MHz HRPWM (reference clocks) are synchronized with PCLKC: Up to 160 MHz ADCLK in the S12AD runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 40 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC rises. • Voltage-monitoring 0 reset: Generated when VCC falls. • Voltage-monitoring 1 reset: Generated when VCC falls. • Voltage-monitoring 2 reset: Generated when VCC falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC pin and generates an internal reset or internal interrupt. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from two different levels • Voltage detection circuits 1 and 2 Voltage detection level: Selectable from five different levels Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking

Table 1.1 Outline of Specifications (3/9)

Classification	Module/Function	Description
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
Interrupt	Interrupt controller (ICUC)	• Interrupt vectors: 256 • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: 2 sources • Non-maskable interrupts: 7 sources • Sixteen levels specifiable for the order of priority • Method of interrupt source selection: The interrupt vectors consist of 256 vectors (208 sources are fixed. The remaining 135 vectors are selected from among the other 48 sources.)
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 2 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8- or 16-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACAa)	• 8 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	• I/O ports for the 144-pin LFQFP I/O pins: 110 Input pin: 9 Pull-up resistors: 110 Open-drain outputs: 110 5-V tolerance: 4 Large current output: 15 • I/O ports for the 100-pin LFQFP (with PGA pseudo-differential input, and with USB) I/O pins: 69 Input pin: 9 Pull-up resistors: 69 Open-drain outputs: 69 5-V tolerance: 3 Large current output: 15 • I/O ports for the 100-pin LFQFP (with PGA pseudo-differential input, and without USB) I/O pins: 72 Input pin: 9 Pull-up resistors: 72 Open-drain outputs: 72 5-V tolerance:3 Large current output: 15 • I/O ports for the 100-pin LFQFP (without PGA pseudo-differential input, and without USB) I/O pins: 73 Input pin: 7 Pull-up resistors: 73 Open-drain outputs: 73 5-V tolerance: 3 Large current output: 15

Table 1.1 Outline of Specifications (4/9)

Classification	Module/Function	Description
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 188 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). • Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.
Timers	8-bit timers (TMR)	• (8 bits × 2 channels) × 4 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC

Table 1.1 Outline of Specifications (5/9)

Classification	Module/Function	Description
Timers	Multifunction timer pulse unit 3 (MTU3d)	• 9 channels (16 bits × 9 channels) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKC/1, PCLKC/2, PCLKC/4, PCLKC/8, PCLKC/16, PCLKC/32, PCLKC/64, PCLKC/256, PCLKC/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) 11 of the signals are available for channels 1, 3, 4, 12 are available for channel 2, and 10 are available for channel 5. • 43 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 45 interrupt sources • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion The timing of the generation of requests to start A/D conversion can be monitored by an external pin. • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • Event linking by the ELC • Internal peripheral bus clock: PCLKA • Counter reference clock: PCLKC • Frequency ratio: PCLKA to PCLKC = 1: N (N = 1 or 2)
	Port output enable 3 (POE3B)	• Control of the high-impedance state of the MTU3/GPTW's waveform output pins, and control of switching to the general I/O port pin • 9 pins for input from signal sources: POE0, POE4, POE8, POE9, POE10, POE11, POE12, POE13, POE14 • Initiation by detection of short-circuited outputs (detection of PWM outputs that have become an active level simultaneously) • Initiation by comparator detection/oscillation stop detection/software • Additional programming of output control target pins is enabled

Table 1.1 Outline of Specifications (6/9)

Classification	Module/Function	Description
Timers	General PWM timer (GPTW)	• 32 bits × 10 channels • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Capable of synchronous start, stop, or clearing of counter for any channel • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 8 ELC events • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting input level comparison • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 4 external triggers • Output pin disabling function by a dead time error or a short circuit detection among output pins • Capable of generating conversion start triggers for the A/D converters as well as monitoring external pins for a start timing of conversion. • Capable of outputting events, such as compare-match from A to F and overflow/ underflow, to ELC • Capable of using noise filter of input capture • Internal peripheral bus clock: PCLKA • Counter reference clock: PCLKC • Frequency ratio: PCLKA to PCLKC = 1: N (N = 1 or 2)
	High resolution PWM (HRPWM)	• Capable of generating the PWM waveform that is generated by GPTW0 through GPTW3 with resolution of minimum of 195 ps.
	Port output enable for GPTW (POEG)	• Controlling the output disable for GPTW waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPTW • Initiation by detection of comparator interrupt request • Initiation by detection of oscillation stop or by software
Communication function	USB 2.0 FS host/ function module (USBb)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Self-power mode and bus power are selectable • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required

Table 1.1 Outline of Specifications (7/9)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIj, SCIi, SCIh)	• 7 channels SCIj: SCI1, SCI5, SCI6, SCI8, SCI9 SCIi: SCI11 SCIh: SCI12 • SCIj, SCIi, SCIh Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 7, 8, 9-bit transfer mode Bit rate modulation Double-speed mode Data match detection (SCI12 is not supported) Event linking by the ELC (supported by SCI5 only) • SCIi Only Capable of serial sending and receiving with 16-byte FIFO-buffered structure both at transmission and reception sections • SCIh Only Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interface (RIICa)	• 1 channel Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 400 kbps • Event linking by the ELC
	CAN module (CAN)	• 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interface (RSPIc)	• 1 channel • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transmit/receive data can be swapped in byte units • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC

Table 1.1 Outline of Specifications (8/9)

Classification	Module/Function	Description
12-bit A/D converter (S12ADH)		• 12 bits (8 channels × 2 units, 14 channels × 1 unit) • 12-bit resolution • Minimum conversion time 0.9 µs per channel (when ADCLK operates at 60 MHz) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sample-and-hold function channel-dedicated sample-and-hold function (unit 0 × 3 channels, unit 1 × 3 channels) included • Sampling variable Sampling time can be set up for each channel. • Conversion function in order of arbitrarily selected channels (Serial conversion of the same channel cannot be allowed) • Double trigger mode (A/D conversion data duplicated) • Three ways to start A/D conversion Software trigger, synchronous trigger (MTU, TMR, ELC), external trigger • Prioritization in group scanning can be controlled among group A, B, and C. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function • Detection of analog input disconnection • Event linking by the ELC • Input signal amplification function by the programmable gain amplifier (unit 0 × 3 channels, unit 1 × 3 channels) Capable of supporting single end/pseudo-differential input
12-bit D/A converter (R12DAb)		• 2 channels • 12-bit resolution • Output voltage: 0 V to AVCC2 • Capable of providing as a reference voltage for comparator • Event linking by the ELC
Comparator C (CMPC)		• 6 channels • Function to compare the reference voltage and the analog input voltage • Reference voltage is selectable from 4 inputs • Analog input voltage is selectable from 4 inputs • Digital filtering
Temperature sensor		• 1 channel • Relative precision: ±1.0°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 2).
Arithmetic unit for trigonometric functions (TFU)		• Sine, cosine, arctangent, $\sqrt{x^2+y^2}$ Simultaneous calculation of sine and cosine Simultaneous calculation of arctangent and $\sqrt{x^2+y^2}$
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An access exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Protects against the reading of programs from blocks 8 and 9 of the code flash memory • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.

Table 1.1 Outline of Specifications (9/9)

Classification	Module/Function	Description
Safety	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$, $X^{32}+X^{28}+X^{27}+X^{26}+X^{25}+X^{23}+X^{22}+X^{20}+X^{19}+X^{18}+X^{14}+X^{13}+X^{11}+X^{10}+X^9+X^8+X^6+1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection function	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB.
	Data operation circuit (DOC)	• The function to compare, add, or subtract 16-bit data
Encryption functions	Trusted Secure IP (TSIP-Lite)	• Access management circuit • Encryption engine 128- or 256-bit key sizes of AES Block cipher mode of operation: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR • Hash function • True random number generator • Prevention from illicit copying of a key
Operating frequency		Up to 200 MHz
Power supply voltage		VCC = 2.7 to 5.5V AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V (VCC ≤ AVCC0 = AVCC1 = AVCC2) With USB in use: VCC_USB = 3.0 to 3.6V (VCC ≥ VCC_USB) With USB not in use: VCC_USB = VCC VSS = AVSS0 = AVSS1 = AVSS2 = VSS_USB = 0V
Operating temperature		D-version: –40 to +85°C G-version: –40 to +105°C
Package		144-pin LFQFP 0.5 mm pitch 100-pin LFQFP 0.5 mm pitch
Debugging interfaces		• JTAG and One-line FINE interfaces

Table 1.2 Comparison of Functions for Different Packages (1/2)

Module/Functions		RX72T Group			
		With PGA pseudo-differential input			Without PGA pseudo-differential input
		With USB		Without USB	
		144 Pins	100 Pins	100 Pins	100 Pins
Code flash memory capacity		Maximum 1 Mbyte			
External bus	External bus width	16 bits			
	Address Space	2 Mbytes × 4 areas			2 Mbytes × 3 areas
External interrupts	NMI	Available			
	IRQ	16 channels			
DMA	DMA controller	Available			
	Data transfer controller	Available			
Timers	Multifunction timer pulse unit 3	9 channels (Ch. 0 to 7, Ch. 9)			
	General PWM timer	10 channels			
	High resolution PWM	4 channels			
	Port output enable 3	Available			
	Port Output Enable for GPTW	Available			
	8-bit timer	2 channels × 4 units			
	Compare match timer	2 channels × 2 units			
	Independent watchdog timer	Available			
Communication functions	USB 2.0 FS host/function module	1 channel		—	
	Serial communications interfaces (SCIj)	5 channels (SCI1, 5, 6, 8, 9)			
	Serial communications interfaces (SCIi)	1 channel (SCI11)			
	Serial communications interfaces (SCIh)	1 channel (SCI12)			
	I^2C bus interfaces	1 channel			
	Serial peripheral interface	1 channel			
	CAN module	1 channel			
12-bit A/D Converter		AN000 to 007*1 (unit 0: 8 channels)	AN000 to 003, 007*1 (unit 0: 5 channels)		AN000 to 003 (unit 0: 4 channels)
		AN100 to 107*1 (unit 1: 8 channels)	AN100 to 103, 107*1 (unit 1: 5 channels)		AN100 to 103 (unit 1: 4 channels)
		AN200 to 211, 216, 217 (unit 2: 14 channels)	AN200 to 203, 206 to 211, 216, 217 (unit 2: 12 channels)		AN200 to 211, 216, 217 (unit 2: 14 channels)
	3 channels simultaneous sampling function	3 channels × 2 units (unit 0, 1)			
	Programmable gain amplifier	6 channels			
Comparator C		6 channels			
D/A converter		2 channels			
Temperature sensor		1 channel			
CRC calculator		Available			

Table 1.2 Comparison of Functions for Different Packages (2/2)

	RX72T Group			
	With PGA pseudo-differential input			Without PGA pseudo-differential input
	With USB		Without USB	
Module/Functions	**144 Pins**	**100 Pins**	**100 Pins**	**100 Pins**
Clock frequency accuracy measurement circuit	Available			
Trusted Secure IP (TSIP-Lite)	Available/Not available			
Event link controller	Available			
Packages	144-pin LFQFP	100-pin LFQFP	100-pin LFQFP	100-pin LFQFP

Note 1. AN007 and AN107 cannot be used when PGA pseudo-differential input is enabled.

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	PGA pseudo-differential input	TSIP-Lite	USB	Operating temperature
RX72T (D-version)	R5F572TKCDFB	PLQP0144KA-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Not available	Available	-40 to 85°C
	R5F572TKGDFB	PLQP0144KA-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Available	Available	-40 to 85°C
	R5F572TFCDFB	PLQP0144KA-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Not available	Available	-40 to 85°C
	R5F572TFGDFB	PLQP0144KA-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Available	Available	-40 to 85°C
	R5F572TKADFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Not available	Not available	-40 to 85°C
	R5F572TKBDFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Not available	Not available	Not available	-40 to 85°C
	R5F572TKCDFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Not available	Available	-40 to 85°C
	R5F572TKEDFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Available	Not available	-40 to 85°C
	R5F572TKFDFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Not available	Available	Not available	-40 to 85°C
	R5F572TKGDFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Available	Available	-40 to 85°C
	R5F572TFADFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Not available	Not available	-40 to 85°C
	R5F572TFBDFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Not available	Not available	Not available	-40 to 85°C
	R5F572TFCDFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Not available	Available	-40 to 85°C
	R5F572TFEDFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Available	Not available	-40 to 85°C
	R5F572TFFDFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Not available	Available	Not available	-40 to 85°C
	R5F572TFGDFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Available	Available	-40 to 85°C
RX72T (G-version)	R5F572TKCGFB	PLQP0144KA-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Not available	Available	-40 to 105°C
	R5F572TKGGFB	PLQP0144KA-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Available	Available	-40 to 105°C
	R5F572TFCGFB	PLQP0144KA-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Not available	Available	-40 to 105°C
	R5F572TFGGFB	PLQP0144KA-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Available	Available	-40 to 105°C
	R5F572TKAGFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Not available	Not available	-40 to 105°C
	R5F572TKBGFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Not available	Not available	Not available	-40 to 105°C
	R5F572TKCGFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Not available	Available	-40 to 105°C
	R5F572TKEGFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Available	Not available	-40 to 105°C
	R5F572TKFGFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Not available	Available	Not available	-40 to 105°C
	R5F572TKGGFP	PLQP0100KB-B	1 Mbyte	128 Kbytes	32 Kbytes	Available	Available	Available	-40 to 105°C
	R5F572TFAGFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Not available	Not available	-40 to 105°C
	R5F572TFBGFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Not available	Not available	Not available	-40 to 105°C
	R5F572TFCGFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Not available	Available	-40 to 105°C
	R5F572TFEGFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Available	Not available	-40 to 105°C
	R5F572TFFGFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Not available	Available	Not available	-40 to 105°C
	R5F572TFGGFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	32 Kbytes	Available	Available	Available	-40 to 105°C

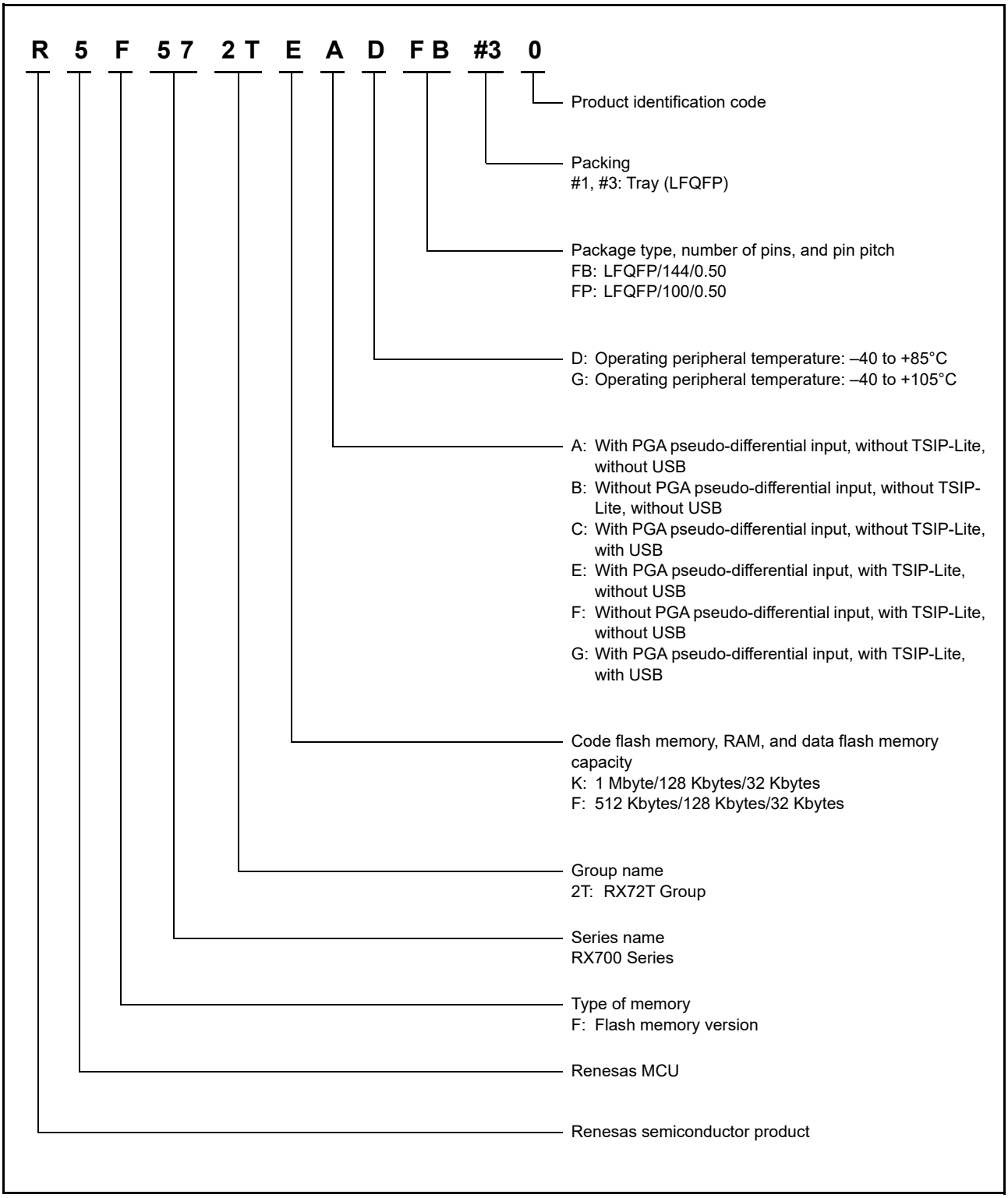


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

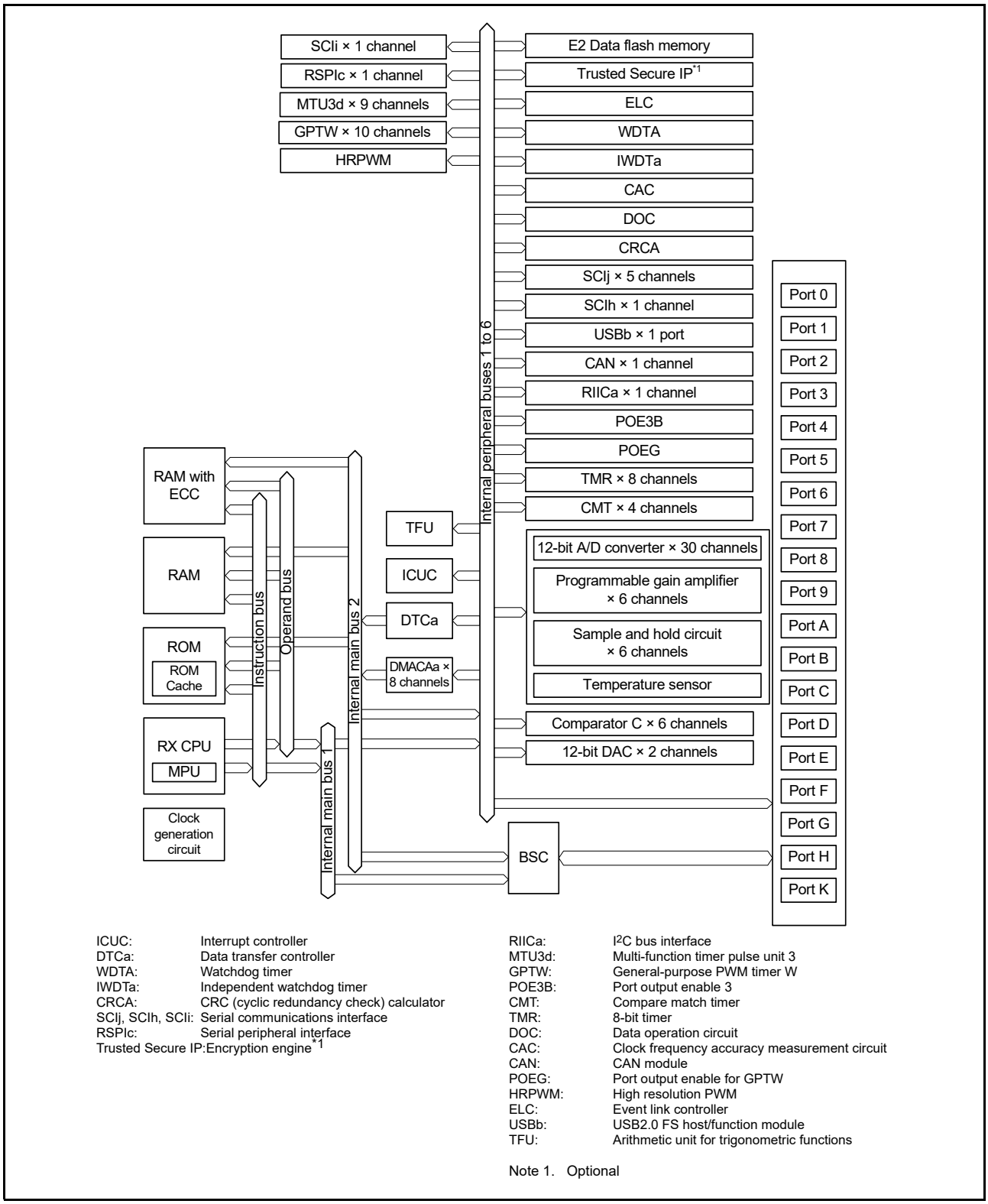


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/6)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	—	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	—	Connect this pin to VSS via a 0.47-μF smoothing capacitor used to stabilize the internal power supply. The capacitor should be placed close to the pin.
	VSS	—	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
	UB	Input	Enable pin for boot mode (USB interface) and user boot mode
	UPSEL	Input	Selects the power supply method in boot mode (USB interface). The low level selects self-power mode and the high level selects bus power mode.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	FINE interface pin.
	TRST#	Input	Pins for the on-chip emulator. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRSYNC1	Output	This pin indicates that output from the TRDATA4 to TRDATA7 pins is valid.
	TRDATA0, TRDATA1, TRDATA2, TRDATA3, TRDATA4, TRDATA5, TRDATA6, TRDATA7	Output	These pins output the trace information.
Address bus	A0 to A20	Output	Output pins for the address
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode

Table 1.4 Pin Functions (2/6)

Classifications	Pin Name	I/O	Description
Bus control	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS3#	Output	Select signals for CS areas
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
	IRQ0-DS to IRQ15-DS	Input	Maskable interrupt request pins or pins which can also be used as triggers for release from deep software standby
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC0A#, MTIOC0B#, MTIOC0C#, MTIOC0D#	I/O	The TGRA0 to TGRD0 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC1A#, MTIOC1B#	I/O	The TGRA1 and TGRB1 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC2A#, MTIOC2B#	I/O	The TGRA2 and TGRB2 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC3A#, MTIOC3B#, MTIOC3C#, MTIOC3D#	I/O	The TGRA3 to TGRD3 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIOC4A#, MTIOC4B#, MTIOC4C#, MTIOC4D#	I/O	The TGRA4 to TGRD4 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins
	MTIC5U#, MTIC5V#, MTIC5W#	Input	The TGRU5, TGRV5, and TGRW5 input capture inverted input/ external pulse inverted input pins.
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC6A#, MTIOC6B#, MTIOC6C#, MTIOC6D#	I/O	The TGRA6 to TGRD6 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC7A#, MTIOC7B#, MTIOC7C#, MTIOC7D#	I/O	The TGRA7 to TGRD7 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D	I/O	The TGRA9 to TGRD9 input capture input/output compare output/PWM output pins
	MTIOC9A#, MTIOC9B#, MTIOC9C#, MTIOC9D#	I/O	The TGRA9 to TGRD9 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
	MTCLKA#, MTCLKB#, MTCLKC#, MTCLKD#	Input	Inverted input pins for the external clock.
	ADSM0, ADSM1	Output	A/D conversion start request frame synchronization signal output pins.

Table 1.4 Pin Functions (3/6)

Classifications	Pin Name	I/O	Description
General PWM timer	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pin
	GTIOC0A to GTIOC9A, GTIOC0B to GTIOC9B	I/O	Input capture input/output compare output/PWM output pins
	GTIOC0A# to GTIOC9A#, GTIOC0B# to GTIOC9B#	I/O	Input capture inverted input/output compare inverted output/ PWM inverted output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
8-bit timer	TMO0 to TMO7	Output	Compare match output pins.
	TMCI0 to TMCI7	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI7	Input	Counter reset input pins.
Port output enable 3	POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, POE14#	Input	Input pins for request signals to switch the MTU3 and GPTW pins between the high impedance state
Serial communications interface (SCIj)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock
	RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data
	TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data
	CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock
	SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmit data.
	SS1#, SS5#, SS6#, SS8#, SS9#	Input	Chip-select input pins.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data

Table 1.4 Pin Functions (4/6)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIi)	• Asynchronous mode/clock synchronous mode		
	SCK11	I/O	Input/output pin for the clock
	RXD11	Input	Input pin for received data
	TXD11	Output	Output pin for transmitted data
	CTS11#	Input	Input pin for controlling the start of transmission and reception
	RTS11#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL11	I/O	Input/output pin for the I^2C clock
	SSDA11	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK11	I/O	Input/output pin for the clock
	SMISO11	I/O	Input/output pin for slave transmission of data
	SMOSI11	I/O	Input/output pin for master transmission of data
	SS11#	Input	Chip-select input pin
I^2C bus interface	SCL0	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.
USB 2.0 host/function module	VCC_USB	Input	Power supply pins
	VSS_USB	Input	Ground pins
	USB0_DP	I/O	Input or output USB transceiver D+ data
	USB0_DM	I/O	Input or output USB transceiver D- data.
	USB0_EXICEN	Output	Connect to the OTG power IC.
	USB0_ID	Input	Connect to the OTG power IC.
	USB0_VBUSEN	Output	USB VBUS power enable pins
	USB0_OVRCURA, USB0_OVRCURB	Input	USB overcurrent pins
	USB0_VBUS	Input	USB cable connection/disconnection detection input pins
CAN module	CRX	Input	Input pins
	CTX	Output	Output pins
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.

Table 1.4 Pin Functions (5/6)

Classifications	Pin Name	I/O	Description
12-bit A/D converter	AN000 to AN002, AN100 to AN102	Input	Input pins for the analog signals to be processed by the A/D converter. (Positive side input at PGA pseudo-differential input.)
	AN003 to AN007, AN103 to AN107, AN200 to AN211, AN216 to AN217	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADST0, ADST1, ADST2	Output	Output pins for A/D conversion status.
	ADTRG0#, ADTRG1#, ADTRG2#	Input	Input pins for the external trigger signals that start the A/D conversion.
	PGAVSS0, PGAVSS1	Input	A common reference ground pin for PGA pseudo-differential input in the unit
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator C	COMP0 to COMP5	Output	Comparator detection result output pins.
	CVREFC0, CVREFC1	Input	Analog reference voltage supply pins for comparator C.
	CMPCnm	Input	Analog input pin for CMPCnm (n = 0 to 5, m = 0 to 3)
Analog power supply	AVCC0	—	Analog voltage supply pin for 12-bit A/D converter unit 0. Connect the AVCC0 pin to AVCC1 or AVCC2 when 12-bit A/D converter unit 0 is not used.
	AVSS0	—	Analog ground pin for 12-bit A/D converter unit 0. Connect the AVSS0 pin to AVSS1 or AVSS2 when 12-bit A/D converter unit 0 is not used.
	AVCC1	—	Analog voltage supply pin for 12-bit A/D converter unit 1. Connect this pin to AVCC0 when not using the 12-bit A/D converter 1 but using the 12-bit A/D converter 0. Connect this pin to AVCC2 when not using the 12-bit A/D converter 0 and the 12-bit A/D converter 1.
	AVSS1	—	Analog ground pin for 12-bit A/D converter unit 1. Connect this pin to AVSS0 when not using the 12-bit A/D converter 1 but using the 12-bit A/D converter 0. Connect this pin to AVSS2 when not using the 12-bit A/D converter 0 and the 12-bit A/D converter 1.
	AVCC2	—	Analog voltage supply pin for the 12-bit A/D converter unit 2, reference voltage supply pin for the 12-bit D/A converter, analog voltage supply pin for the comparator C, and analog voltage supply pin for the temperature sensor. Connect this pin to either of AVCC0 or AVCC1 when not using the 12-bit A/D converter unit 2, 12-bit D/A converter, comparator C, and temperature sensor.
	AVSS2	—	Analog ground pin for the 12-bit A/D converter unit 2, reference ground pin for the D/A converter, analog ground pin for the comparator C, and analog ground pin for the temperature sensor. Connect this pin to either of AVSS0 or AVSS1 when not using the 12-bit A/D converter unit 2, 12-bit D/A converter, comparator C, and temperature sensor.

Table 1.4 Pin Functions (6/6)

Classifications	Pin Name	I/O	Description
I/O ports	P00, P01	I/O	2-bit input/output pins.
	P10 to P17	I/O	8-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins.
	P40 to P47	I/O	8-bit input/output pins (P40 to P42, P44 to P46: input).
	P50 to P55	I/O	6-bit input/output pins.
	P60 to P65	I/O	6-bit input/output pins.
	P70 to P76	I/O	7-bit input/output pins.
	P80 to P82	I/O	3-bit input/output pins.
	P90 to P96	I/O	7-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC6	I/O	7-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE6	I/O	7-bit input/output pins (PE2: input).
	PF0 to PF3	I/O	4-bit input/output pins.
	PG0 to PG2	I/O	3-bit input/output pins.
	PH0 to PH7	I/O	8-bit input/output pins (PH0, PH4: input).
	PK0 to PK2	I/O	3-bit input/output pins.

Note: When not using any of the A/D converter, D/A converter, comparator C and temperature sensor, connect the AVCC0, AVCC1 and AVCC2 pins to VCC, and connect the AVSS0, AVSS1 and AVSS2 pins to VSS, respectively.

Note: When the pin functions have “-DS” appended to their names, they can also be used as triggers for release from deep software standby.

1.5 Pin Assignments

1.5.1 144-Pin LFQFP (with PGA pseudo-differential input and with USB pin)

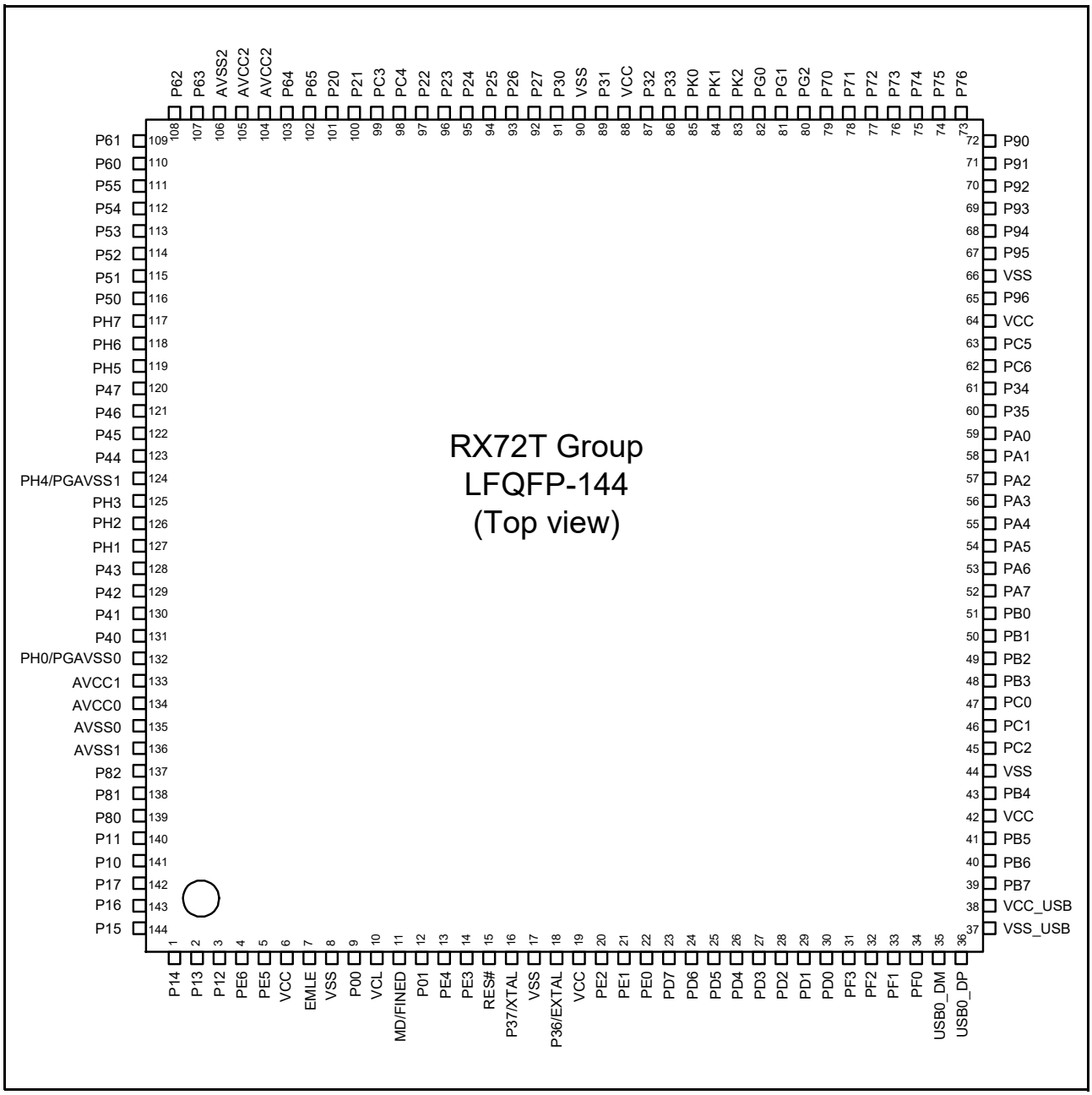


Figure 1.3 Pin Assignment (144-pin LFQFP) with PGA pseudo-differential input and with USB pin

1.5.2 100-Pin LFQFP (with PGA pseudo-differential input and with USB pin)

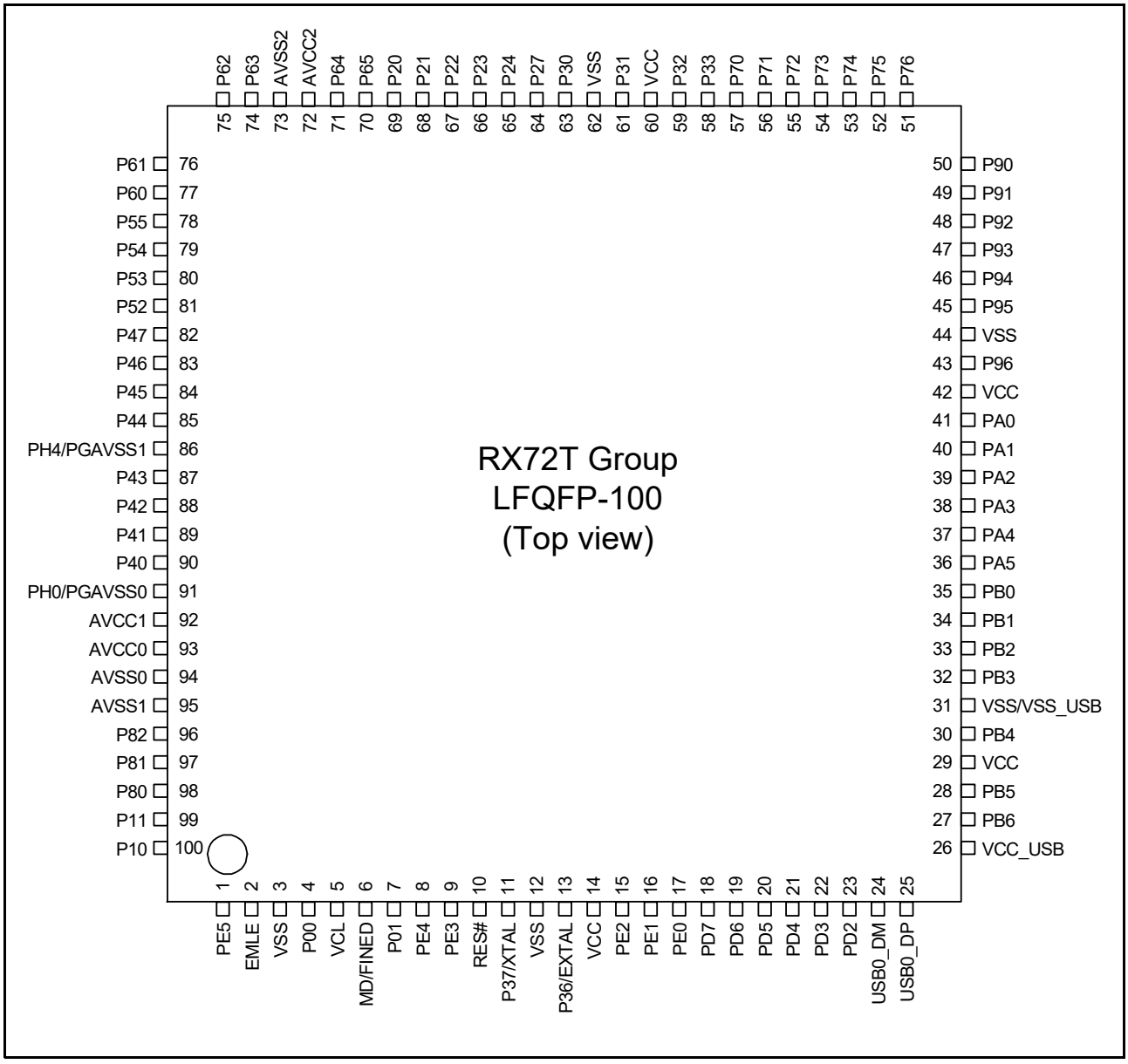


Figure 1.4 Pin Assignment (100-pin LFQFP) with PGA pseudo-differential input and with USB pin

1.5.3 100-Pin LFQFP (with PGA pseudo-differential input and without USB pin)

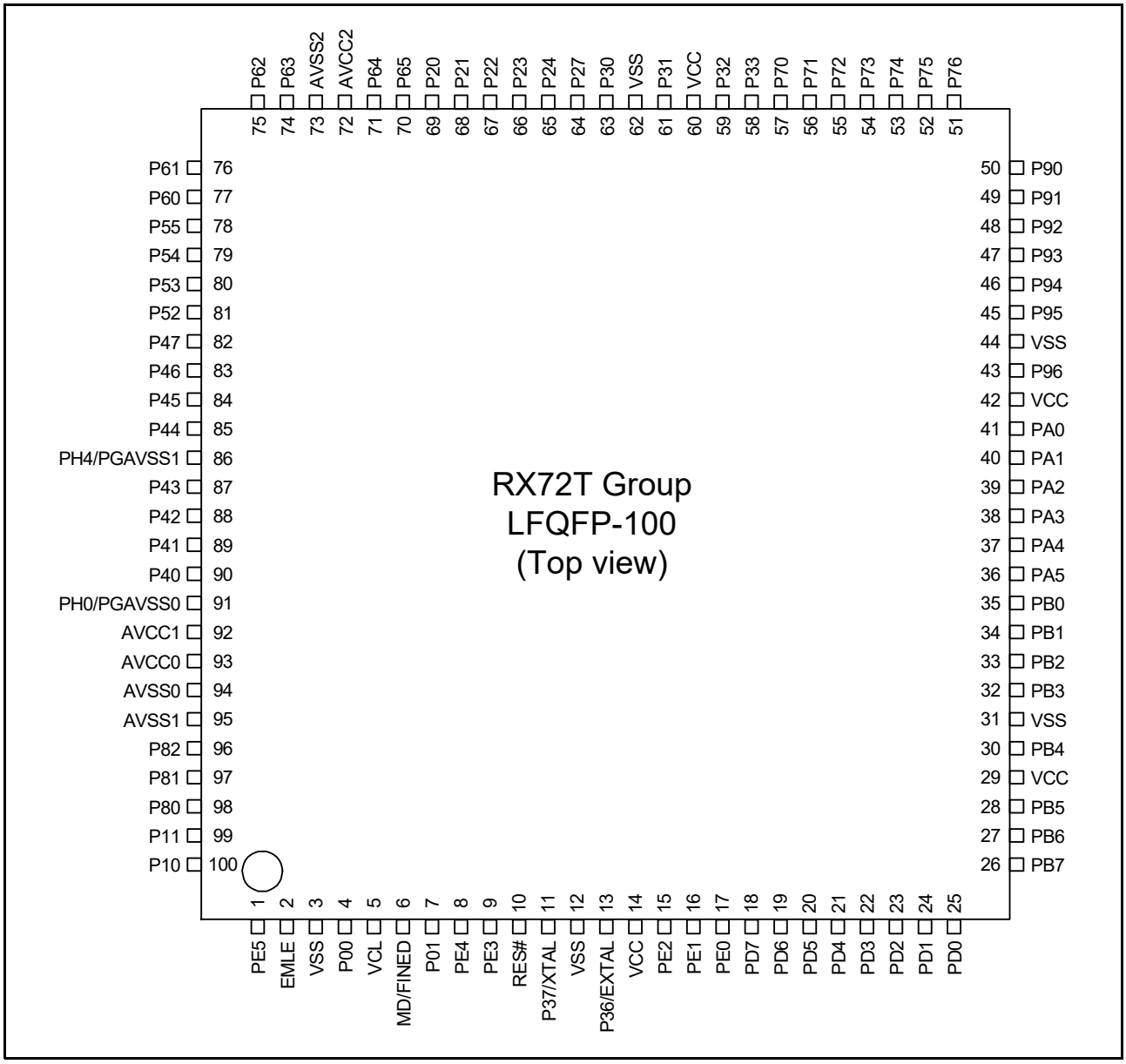


Figure 1.5 Pin Assignment (100-pin LFQFP) with PGA pseudo-differential input and without USB pin

1.5.4 100-Pin LFQFP (without PGA pseudo-differential input and without USB pin)

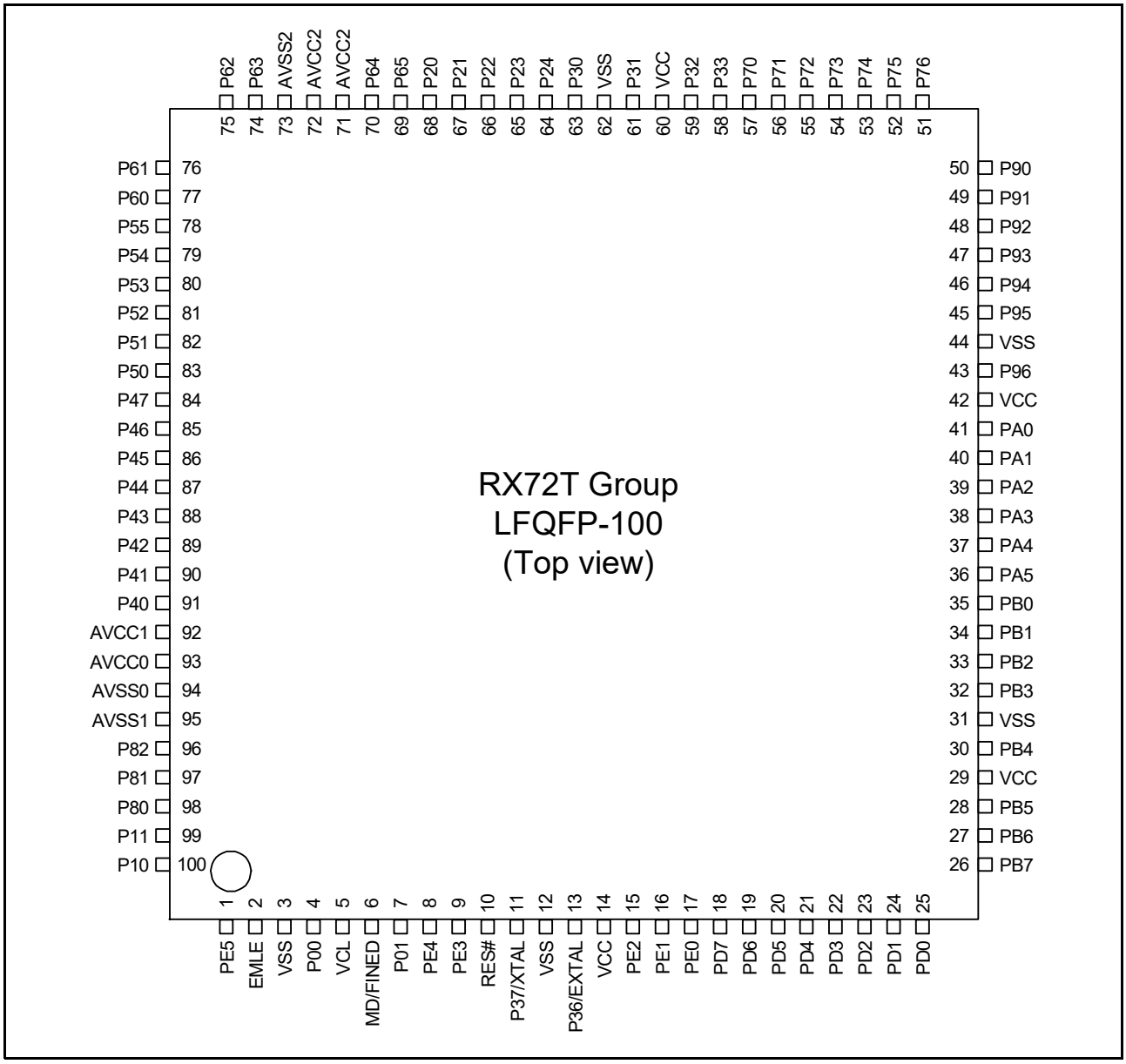


Figure 1.6 Pin Assignment (100-pin LFQFP) without PGA pseudo-differential input and without USB pin

1.6 List of Pin and Pin Functions

1.6.1 144-Pin LFQFP (with PGA pseudo-differential input and with USB pin)

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (1/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
1		P14		MTIOC4B/ MTIOC4B#/ GTIOC2A/GTIOC9A/ GTIOC2A#/ GTIOC9A#			IRQ11		
2		P13		MTIOC4A/ MTIOC4A#/ GTIOC1A/GTIOC8A/ GTIOC1A#/ GTIOC8A#			IRQ10		
3		P12		MTIOC3B/ MTIOC3B#/ GTIOC0A/GTIOC7A/ GTIOC0A#/ GTIOC7A#			IRQ9		
4		PE6	RD#	GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE10#			IRQ3		
5		PE5	BCLK	MTIOC9D/ MTIOC9D#/ GTIOC3A/ GTETRGB/ GTIOC3A#/ GTETRGD	SCK9/CTS9#/ RTS9#/SS9#		IRQ0		ADST0
6	VCC								
7	EMLE								
8	VSS								
9	UB	P00	A11	MTIOC9A/ MTIOC9A#/CACREF	RXD9/SMISO9/ SSCL9/RXD12/ SMISO12/SSCL12/ RXDX12		IRQ2		ADST1/ COMP0
10	VCL								
11	MD/FINED								
12		P01	A10	MTIOC9C/ MTIOC9C#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE12#	TXD9/SMOSI9/ SSDA9/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12		IRQ4		ADST2/ COMP1
13		PE4	A9	MTCLKC/MTCLKC#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE10#	SCK9		IRQ1		
14		PE3	A8	MTCLKD/MTCLKD#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE11#	CTS9#/RTS9#/ SS9#		IRQ2-DS		
15	RES#								
16	XTAL	P37							
17	VSS								
18	EXTAL	P36							
19	VCC								
20	UPSEL	PE2		POE10#			NMI		

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (2/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
21		PE1	WR0#/WR#	MTIOC9D/ MTIOC9D#/TMO5	CTS5#/RTS5#/ SS5#/CTS12#/ RTS12#/SS12#/ SSLA3		IRQ15		
22		PE0	WR1#/ BC1#/ WAIT#	MTIOC9B/ MTIOC9B#/TMCI1/ TMCI5	RXD5/SMISO5/ SSCL5/SSLA2/ CRX0	USB0_OVR CURB	IRQ7		
23	TRST#	PD7		MTIOC9A/ MTIOC9A#/ GTIOC0A/GTIOC3A/ GTIOC0A#/ GTIOC3A#/TMRI1/ TMRI5	TXD5/SMOSI5/ SSDA5/SSLA1/ CTX0		IRQ8		
24	TMS	PD6		MTIOC9C/ MTIOC9C#/ GTIOC0B/GTIOC3B/ GTIOC0B#/ GTIOC3B#/TMO1	CTS1#/RTS1#/ SS1#/CTS11#/ RTS11#/SS11#/ SSLA0		IRQ5		ADST0
25	TDI	PD5		GTIOC1A/ GTETRGA/ GTIOC1A#/TMRI0/ TMRI6	RXD1/SMISO1/ SSCL1/RXD11/ SMISO11/SSCL11		IRQ6		
26	TCK	PD4		GTIOC1B/ GTETRGB/ GTIOC1B#/TMCI0/ TMCI6	SCK1/SCK11		IRQ2		
27	TDO	PD3		GTIOC2A/ GTETRGC/ GTIOC2A#/TMO0	TXD1/SMOSI1/ SSDA1/TXD11/ SMOSI11/SSDA11				
28	TRCLK	PD2	A7	GTIOC2B/GTIOC0A/ GTIOC2B#/ GTIOC0A#/TMCI1/ TMO4	SCK5/SCK8/ MOSIA	USB0_VBUS			
29	TRDATA3	PD1	A6	GTIOC3A/GTIOC0B/ GTIOC3A#/ GTIOC0B#/TMO2	RXD8/SMISO8/ SSCL8/MISOA				
30	TRDATA2	PD0	A5	GTIOC3B/GTIOC1A/ GTIOC3B#/ GTIOC1A#/TMO6	TXD8/SMOSI8/ SSDA8/RSPCKA				
31	TRDATA7	PF3	A19/CS3#	GTETRGA/TMO7	CTS11#/RTS11#/ SS11#/CRX0		IRQ14		COMP0
32	TRDATA6	PF2	A18/CS2#	GTETRGB/TMO3	SCK11/CTX0		IRQ5		COMP1
33	TRDATA5	PF1	A17/CS1#	GTETRGC/TMO5	RXD11/SMISO11/ SSCL11		IRQ13		COMP2
34	TRDATA4	PF0	A0/BC0#	GTETRGD/TMO1	TXD11/SMOSI11/ SSDA11		IRQ12		COMP3
35						USB0_DM			
36						USB0_DP			
37	VSS_USB								
38	VCC_USB								
39	TRDATA1	PB7	A4	GTIOC1B/ GTIOC1B#	SCK5/SCK11/ SCK12	USB0_OVR CURB			
40	TRDATA0	PB6	A3	GTIOC2A/ GTIOC2A#	RXD5/SMISO5/ SSCL5/RXD11/ SMISO11/SSCL11/ RXD12/SMISO12/ SSCL12/RXDX12/ CRX0	USB0_OVR CURA	IRQ2		
41	TRSYNC	PB5	A2	GTIOC2B/ GTIOC2B#	TXD5/SMOSI5/ SSDA5/TXD11/ SMOSI11/SSDA11/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX0	USB0_VBUS EN			

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (3/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
42	VCC								
43	TRSYNC1	PB4	A1	GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE8#	CTS5#/RTS5#/ SS5#/SCK11/ CTS11#/RTS11#/ SS11#	USB0_OVR CURB	IRQ3-DS		
44	VSS								
45		PC2	CS1#	MTIOC0D/ MTIOC0D#/ GTADSM0	SCK8	USB0_ID/ USB0_OVR CURA	IRQ15		ADSM0/ COMP5
46		PC1	A16	MTIOC0C/ MTIOC0C#/ GTADSM1	TXD8/SMOSI8/ SSDA8	USB0_EXIC EN/ USB0_VBUS EN	IRQ13		ADSM1/ COMP4
47		PC0	CS0#	MTIOC0B/ MTIOC0B#	RXD8/SMISO8/ SSCL8	USB0_VBUS	IRQ12		COMP3
48		PB3	A7	MTIOC0A/ MTIOC0A#/CACREF	SCK6/RSPCKA		IRQ9		
49		PB2	A6	MTIOC0B/ MTIOC0B#/ GTADSM0/TMRI0	TXD6/SMOSI6/ SSDA6/SDA0				ADSM0
50		PB1	A5	MTIOC0C/ MTIOC0C#/ GTADSM1/TMCI0	RXD6/SMISO6/ SSCL6/SCL0		IRQ4		ADSM1
51		PB0	A0/BC0#/A4	MTIOC0D/ MTIOC0D#/TMO0	TXD6/SMOSI6/ SSDA6/CTS11#/ RTS11#/SS11#/ MOSIA		IRQ8		ADTRG2#
52		PA7	A15	MTCLKA/MTCLKC/ MTCLKA#/ MTCLKC#/ GTADSM0/TMO2	RXD11/SMISO11/ SSCL11/RXD12/ SMISO12/SSCL12/ RXDX12/CRX0				ADSM0
53		PA6	A14	MTCLKB/MTCLKD/ MTCLKB#/ MTCLKD#/ GTADSM1/TMO6	TXD11/SMOSI11/ SSDA11/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ CTX0		IRQ7		ADSM1
54		PA5	A3	MTIOC1A/ MTIOC1A#/TMCI3	RXD6/SMISO6/ SSCL6/RXD8/ SMISO8/SSCL8/ MISOA		IRQ1		ADTRG1#
55		PA4	A2	MTIOC1B/ MTIOC1B#/TMCI7	SCK6/TXD8/ SMOSI8/SSDA8/ RSPCKA				ADTRG0#
56		PA3	A1	MTIOC2A/ MTIOC2A#/ GTADSM0/TMRI7	TXD9/SMOSI9/ SSDA9/SCK8/ SSLA0				
57		PA2	A0/BC0#	MTIOC2B/ MTIOC2B#/ GTADSM1/TMO7	CTS6#/RTS6#/ SS6#/RXD9/ SMISO9/SSCL9/ SCK11/SSLA1				
58		PA1		MTIOC6A/ MTIOC6A#/TMO4	TXD9/SMOSI9/ SSDA9/RXD11/ SMISO11/SSCL11/ SSLA2/CRX0	USB0_ID/ USB0_OVR CURA	IRQ14-DS		ADTRG0#
59		PA0		MTIOC6C/ MTIOC6C#/TMO2	SCK9/TXD11/ SMOSI11/SSDA11/ SSLA3/CTX0	USB0_EXIC EN/ USB0_VBUS EN			
60		P35	A13	MTIOC2A/MTIOC9A/ MTIOC2A#/ MTIOC9A#/ GTADSM0/TMO0	CTS8#/RTS8#/ SS8#/TXD1/ SMOSI1/SSDA1		IRQ6		

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (4/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
61		P34	A12	MTIOC2B/MTIOC9B/ MTIOC2B#/ MTIOC9B#/ GTADSM1/ GTETRGB/TMO4	CTS9#/RTS9#/ SS9#/RXD1/ SMISO1/SSCL1	USB0_OVR CURB	IRQ3		
62		PC6		MTIOC1A/MTIOC9C/ MTIOC1A#/ MTIOC9C#	RXD11/SMISO11/ SSCL11/CRX0		IRQ11-DS		
63		PC5		MTIOC1B/MTIOC9D/ MTIOC1B#/ MTIOC9D#	TXD11/SMOSI11/ SSDA11/CTX0		IRQ10-DS		
64	VCC								
65		P96	CS0#/ WAIT#	GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE4#	CTS8#/RTS8#/ SS8#		IRQ4-DS		
66	VSS								
67		P95		MTIOC6B/ MTIOC6B#/ GTIOC4A/GTIOC7A/ GTIOC4A#/ GTIOC7A#					
68		P94		MTIOC7A/ MTIOC7A#/ GTIOC5A/GTIOC8A/ GTIOC5A#/ GTIOC8A#					
69		P93		MTIOC7B/ MTIOC7B#/ GTIOC6A/GTIOC9A/ GTIOC6A#/ GTIOC9A#					
70		P92		MTIOC6D/ MTIOC6D#/ GTIOC4B/GTIOC7B/ GTIOC4B#/ GTIOC7B#					
71		P91		MTIOC7C/ MTIOC7C#/ GTIOC5B/GTIOC8B/ GTIOC5B#/ GTIOC8B#					
72		P90		MTIOC7D/ MTIOC7D#/ GTIOC6B/GTIOC9B/ GTIOC6B#/ GTIOC9B#					
73		P76	D0 [A0/D0]	MTIOC4D/ MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/ GTIOC6B#					
74		P75	D1 [A1/D1]	MTIOC4C/ MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/ GTIOC5B#					
75		P74	D2 [A2/D2]	MTIOC3D/ MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/ GTIOC4B#					
76		P73	D3 [A3/D3]	MTIOC4B/ MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/ GTIOC6A#					

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (5/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
77		P72	D4 [A4/D4]	MTIOC4A/ MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/ GTIOC5A#					
78		P71	D5 [A5/D5]	MTIOC3B/ MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/ GTIOC4A#					
79		P70	D6 [A6/D6]	GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE0#	CTS9#/RTS9#/ SS9#		IRQ5-DS		
80		PG2	D11 [A11/ D11]	GTETRGA/ GTIOC0B/ GTIOC0B#	SCK9		IRQ2		COMP0
81		PG1	D12 [A12/ D12]	GTIOC0A/ GTIOC0A#	TXD9/SMOSI9/ SSDA9		IRQ1		COMP1
82		PG0	D13 [A13/ D13]	GTIOC1B/ GTIOC1B#	RXD9/SMISO9/ SSCL9		IRQ0		COMP2
83		PK2	D14 [A14/ D14]	GTIOC1A/ GTIOC1A#/POE12#	CTS9#/RTS9#/ SS9#/SCK5		IRQ9-DS		COMP3
84		PK1	D15 [A15/ D15]	GTIOC2B/ GTIOC2B#/POE13#	CTS8#/RTS8#/ SS8#/TXD5/ SMOSI5/SSDA5		IRQ8-DS		COMP4
85		PK0	CS1#	GTIOC2A/ GTIOC2A#/POE14#	RXD5/SMISO5/ SSCL5		IRQ15-DS		COMP5
86		P33	D7 [A7/D7]	MTIOC3A/MTCLKA/ MTIOC3A#/ MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0	SSLA3		IRQ13-DS		
87		P32	D8 [A8/D8]	MTIOC3C/MTCLKB/ MTIOC3C#/ MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6	SSLA2		IRQ12-DS		
88	VCC								
89		P31	D9 [A9/D9]	MTIOC0A/MTCLKC/ MTIOC0A#/ MTCLKC#/TMRI6	SSLA1		IRQ6		
90	VSS								
91		P30	D10 [A10/ D10]	MTIOC0B/MTCLKD/ MTIOC0B#/ MTCLKD#/TMCI6	SCK8/CTS8#/ RTS8#/SS8#/ SSLA0		IRQ7		COMP3
92		P27	CS3#	MTIOC1A/MTIOC0C/ MTIOC1A#/ MTIOC0C#/POE9#			IRQ15		
93		P26	CS2#	MTIOC9A/ MTIOC9A#	CTS1#/RTS1#/ SS1#		IRQ11		ADST0
94		P25	CS3#	MTIOC9C/ MTIOC9C#	SCK1		IRQ10		ADST1
95		P24	D11 [A11/ D11]	MTIC5U/MTIC5U#/ TMCI2/TMO6	CTS8#/RTS8#/ SS8#/SCK8/ RSPCKA		IRQ4		COMP0
96		P23	D12 [A12/ D12]	MTIC5V/MTIC5V#/ TMO2/CACREF	TXD8/SMOSI8/ SSDA8/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ MOSIA/CTX0		IRQ11		COMP1
97		P22	D13 [A13/ D13]	MTIC5W/MTCLKD/ MTIC5W#/ MTCLKD#/ MTIOC9B/TMRI2/ TMO4	RXD8/SMISO8/ SSCL8/RXD12/ SMISO12/SSCL12/ RXDX12/MISOA/ CRX0		IRQ10		ADTRG2#/ COMP2

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (6/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
98		PC4	A20	MTIOC9B/ MTIOC9B#	TXD1/SMOSI1/ SSDA1/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12				ADST2/ COMP5
99		PC3		MTIOC9D/ MTIOC9D#	RXD1/SMISO1/ SSCL1/RXD12/ SMISO12/SSCL12/ RXDX12		IRQ14		COMP4
100		P21	D14 [A14/ D14]	MTIOC9A/MTCLKA/ MTIOC9A#/ MTCLKA#/TMCI4	TXD8/SMOSI8/ SSDA8/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ MOSIA		IRQ6-DS	AN217	ADTRG1#/ COMP5
101		P20	D15 [A15/ D15]	MTIOC9C/MTCLKB/ MTIOC9C#/ MTCLKB#/TMRI4	CTS8#/RTS8#/ SS8#/SCK8/ RSPCKA		IRQ7-DS	AN216	ADTRG0#/ COMP4
102		P65	A12				IRQ9	AN211/ CMPC53/ DA1	
103		P64	A13				IRQ8	AN210/ CMPC33/ DA0	
104	AVCC2								
105	AVCC2								
106	AVSS2								
107		P63	A14/A12				IRQ7	AN209/ CMPC23	
108		P62	A15/A13				IRQ6	AN208/ CMPC43	
109		P61	A16/A14				IRQ5	AN207/ CMPC13	
110		P60	A17/A15				IRQ4	AN206/ CMPC03	
111		P55	A18/A16				IRQ3	AN203/ CMPC32	
112		P54	A19/A17				IRQ2	AN202/ CMPC22	
113		P53	A20/A18				IRQ1	AN201/ CMPC12	
114		P52					IRQ0	AN200/ CMPC02	
115		P51						AN205/ CMPC52	
116		P50						AN204/ CMPC42	
117		PH7						AN106/ CVREFC1	
118		PH6						AN105	
119		PH5						AN104	
120		P47						AN103	
121		P46						AN102/ CMPC50/ CMPC51	
122		P45						AN101/ CMPC40/ CMPC41	
123		P44						AN100/ CMPC30/ CMPC31	
124		PH4						AN107/ PGAVSS1	

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (7/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
125		PH3						AN006/ CVREFC0	
126		PH2						AN005	
127		PH1						AN004	
128		P43						AN003	
129		P42						AN002/ CMPC20/ CMPC21	
130		P41						AN001/ CMPC10/ CMPC11	
131		P40						AN000/ CMPC00/ CMPC01	
132		PH0						AN007/ PGAVSS0	
133	AVCC1								
134	AVCC0								
135	AVSS0								
136	AVSS1								
137		P82	ALE/WAIT#	MTIC5U/MTIC5U#/ TMO4	SCK6/SCK12		IRQ3		COMP5
138		P81	CS2#	MTIC5V/MTIC5V#/ TMCI4	TXD6/SMOSI6/ SSDA6/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12				COMP4
139		P80	CS1#	MTIC5W/MTIC5W#/ TMRI4	RXD6/SMISO6/ SSCL6/RXD12/ SMISO12/SSCL12/ RXDX12		IRQ5		COMP3
140		P11	RD#	MTIOC3A/MTCLKC/ MTIOC3A#/ MTCLKC#/ MTIOC9D/GTIOC3B/ GTETRGA/ GTIOC3B#/ GTETRGC/TMO3/ POE9#			IRQ1-DS		
141		P10		MTIOC9B/MTCLKD/ MTIOC9B#/ MTCLKD#/ GTETRGB/ GTETRGD/TMRI3/ POE12#	CTS6#/RTS6#/ SS6#		IRQ0-DS		
142		P17		MTIOC4D/ MTIOC4D#/ GTIOC2B/GTIOC9B/ GTIOC2B#/ GTIOC9B#			IRQ14		
143		P16		MTIOC4C/ MTIOC4C#/ GTIOC1B/GTIOC8B/ GTIOC1B#/ GTIOC8B#			IRQ13		
144		P15		MTIOC3D/ MTIOC3D#/ GTIOC0B/GTIOC7B/ GTIOC0B#/ GTIOC7B#			IRQ12		

1.6.2 100-Pin LFQFP (with PGA pseudo-differential input and with USB pin)

Table 1.6 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (1/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
1		PE5	BCLK	MTIOC9D/ MTIOC9D#/ GTIOC3A/ GTETRGB/ GTIOC3A#/ GTETRGD	SCK9/CTS9#/ RTS9#/SS9#		IRQ0		ADST0
2	EMLE								
3	VSS								
4	UB	P00	A11	MTIOC9A/ MTIOC9A#/CACREF	RXD9/SMISO9/ SSCL9/RXD12/ SMISO12/SSCL12/ RXDX12		IRQ2		ADST1/ COMP0
5	VCL								
6	MD/FINED								
7		P01	A10	MTIOC9C/ MTIOC9C#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE12#	TXD9/SMOSI9/ SSDA9/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12		IRQ4		ADST2/ COMP1
8		PE4	A9	MTCLKC/MTCLKC#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE10#	SCK9		IRQ1		
9		PE3	A8	MTCLKD/MTCLKD#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE11#	CTS9#/RTS9#/ SS9#		IRQ2-DS		
10	RES#								
11	XTAL	P37							
12	VSS								
13	EXTAL	P36							
14	VCC								
15	UPSEL	PE2		POE10#			NMI		
16		PE1	WR0#/WR#	MTIOC9D/ MTIOC9D#/TMO5	CTS5#/RTS5#/ SS5#/CTS12#/ RTS12#/SS12#/ SSLA3		IRQ15		
17		PE0	WR1#/ BC1#/ WAIT#	MTIOC9B/ MTIOC9B#/TMCI1/ TMCI5	RXD5/SMISO5/ SSCL5/SSLA2/ CRX0	USB0_OVR CURB	IRQ7		
18	TRST#	PD7		MTIOC9A/ MTIOC9A#/ GTIOC0A/GTIOC3A/ GTIOC0A#/ GTIOC3A#/TMRI1/ TMRI5	TXD5/SMOSI5/ SSDA5/SSLA1/ CTX0		IRQ8		
19	TMS	PD6		MTIOC9C/ MTIOC9C#/ GTIOC0B/GTIOC3B/ GTIOC0B#/ GTIOC3B#/TMO1	CTS1#/RTS1#/ SS1#/CTS11#/ RTS11#/SS11#/ SSLA0		IRQ5		ADST0
20	TDI	PD5		GTIOC1A/ GTETRGA/ GTIOC1A#/TMRI0/ TMRI6	RXD1/SMISO1/ SSCL1/RXD11/ SMISO11/SSCL11		IRQ6		

Table 1.6 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (2/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
21	TCK	PD4		GTIOC1B/ GTETRGB/ GTIOC1B#/TMCI0/ TMCI6	SCK1/SCK11		IRQ2		
22	TDO	PD3		GTIOC2A/ GTETRGC/ GTIOC2A#/TMO0	TXD1/SMOSI1/ SSDA1/TXD11/ SMOSI11/SSDA11				
23	TRCLK	PD2	A7	GTIOC2B/GTIOC0A/ GTIOC2B#/ GTIOC0A#/TMCI1/ TMO4	SCK5/SCK8/ MOSIA	USB0_VBUS			
24						USB0_DM			
25						USB0_DP			
26	VCC_USB								
27	TRDATA0	PB6	A3	GTIOC2A/ GTIOC2A#	RXD5/SMISO5/ SSCL5/RXD11/ SMISO11/SSCL11/ RXD12/SMISO12/ SSCL12/RXDX12/ CRX0	USB0_OVR CURA	IRQ2		
28	TRSYNC	PB5	A2	GTIOC2B/ GTIOC2B#	TXD5/SMOSI5/ SSDA5/TXD11/ SMOSI11/SSDA11/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX0	USB0_VBUS EN			
29	VCC								
30		PB4	A1	GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE8#	CTS5#/RTS5#/ SS5#/SCK11/ CTS11#/RTS11#/ SS11#	USB0_OVR CURB	IRQ3-DS		
31	VSS/VSS_USB								
32		PB3	A7	MTIOC0A/ MTIOC0A#/CACREF	SCK6/RSPCKA		IRQ9		
33		PB2	A6	MTIOC0B/ MTIOC0B#/ GTADSM0/TMRI0	TXD6/SMOSI6/ SSDA6/SDA0				ADSM0
34		PB1	A5	MTIOC0C/ MTIOC0C#/ GTADSM1/TMCI0	RXD6/SMISO6/ SSCL6/SCL0		IRQ4		ADSM1
35		PB0	A0/BC0#/A4	MTIOC0D/ MTIOC0D#/TMO0	TXD6/SMOSI6/ SSDA6/CTS11#/ RTS11#/SS11#/ MOSIA		IRQ8		ADTRG2#
36		PA5	A3	MTIOC1A/ MTIOC1A#/TMCI3	RXD6/SMISO6/ SSCL6/RXD8/ SMISO8/SSCL8/ MISOA		IRQ1		ADTRG1#
37		PA4	A2	MTIOC1B/ MTIOC1B#/TMCI7	SCK6/TXD8/ SMOSI8/SSDA8/ RSPCKA				ADTRG0#
38		PA3	A1	MTIOC2A/ MTIOC2A#/ GTADSM0/TMRI7	TXD9/SMOSI9/ SSDA9/SCK8/ SSLA0				
39		PA2	A0/BC0#	MTIOC2B/ MTIOC2B#/ GTADSM1/TMO7	CTS6#/RTS6#/ SS6#/RXD9/ SMISO9/SSCL9/ SCK11/SSLA1				
40		PA1		MTIOC6A/ MTIOC6A#/TMO4	TXD9/SMOSI9/ SSDA9/RXD11/ SMISO11/SSCL11/ SSLA2/CRX0	USB0_ID/ USB0_OVR CURA	IRQ14-DS		ADTRG0#

Table 1.6 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (3/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
41		PA0		MTIOC6C/ MTIOC6C#/TMO2	SCK9/TXD11/ SMOSI11/SSDA11/ SSLA3/CTX0	USB0_EXICEN/ USB0_VBUSEN			
42	VCC								
43		P96	CS0#/ WAIT#	GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE4#	CTS8#/RTS8#/ SS8#		IRQ4-DS		
44	VSS								
45		P95		MTIOC6B/ MTIOC6B#/ GTIOC4A/GTIOC7A/ GTIOC4A#/ GTIOC7A#					
46		P94		MTIOC7A/ MTIOC7A#/ GTIOC5A/GTIOC8A/ GTIOC5A#/ GTIOC8A#					
47		P93		MTIOC7B/ MTIOC7B#/ GTIOC6A/GTIOC9A/ GTIOC6A#/ GTIOC9A#					
48		P92		MTIOC6D/ MTIOC6D#/ GTIOC4B/GTIOC7B/ GTIOC4B#/ GTIOC7B#					
49		P91		MTIOC7C/ MTIOC7C#/ GTIOC5B/GTIOC8B/ GTIOC5B#/ GTIOC8B#					
50		P90		MTIOC7D/ MTIOC7D#/ GTIOC6B/GTIOC9B/ GTIOC6B#/ GTIOC9B#					
51		P76	D0 [A0/D0]	MTIOC4D/ MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/ GTIOC6B#					
52		P75	D1 [A1/D1]	MTIOC4C/ MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/ GTIOC5B#					
53		P74	D2 [A2/D2]	MTIOC3D/ MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/ GTIOC4B#					
54		P73	D3 [A3/D3]	MTIOC4B/ MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/ GTIOC6A#					
55		P72	D4 [A4/D4]	MTIOC4A/ MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/ GTIOC5A#					

Table 1.6 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (4/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
56		P71	D5 [A5/D5]	MTIOC3B/ MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/ GTIOC4A#					
57		P70	D6 [A6/D6]	GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/POE0#	CTS9#/RTS9#/ SS9#		IRQ5-DS		
58		P33	D7 [A7/D7]	MTIOC3A/MTCLKA/ MTIOC3A#/ MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0	SSLA3		IRQ13-DS		
59		P32	D8 [A8/D8]	MTIOC3C/MTCLKB/ MTIOC3C#/ MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6	SSLA2		IRQ12-DS		
60	VCC								
61		P31	D9 [A9/D9]	MTIOC0A/MTCLKC/ MTIOC0A#/ MTCLKC#/TMRI6	SSLA1		IRQ6		
62	VSS								
63		P30	D10 [A10/ D10]	MTIOC0B/MTCLKD/ MTIOC0B#/ MTCLKD#/TMCI6	SCK8/CTS8#/ RTS8#/SS8#/ SSLA0		IRQ7		COMP3
64		P27	CS3#	MTIOC1A/MTIOC0C/ MTIOC1A#/ MTIOC0C#/POE9#			IRQ15		
65		P24	D11 [A11/ D11]	MTIC5U/MTIC5U#/ TMCI2/TMO6	CTS8#/RTS8#/ SS8#/SCK8/ RSPCKA		IRQ4		COMP0
66		P23	D12 [A12/ D12]	MTIC5V/MTIC5V#/ TMO2/CACREF	TXD8/SMOSI8/ SSDA8/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ MOSIA/CTX0		IRQ11		COMP1
67		P22	D13 [A13/ D13]	MTIC5W/MTCLKD/ MTIC5W#/ MTCLKD#/ MTIOC9B/TMRI2/ TMO4	RXD8/SMISO8/ SSCL8/RXD12/ SMISO12/SSCL12/ RXDX12/MISOA/ CRX0		IRQ10		ADTRG2#/ COMP2
68		P21	D14 [A14/ D14]	MTIOC9A/MTCLKA/ MTIOC9A#/ MTCLKA#/TMCI4	TXD8/SMOSI8/ SSDA8/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ MOSIA		IRQ6-DS	AN217	ADTRG1#/ COMP5
69		P20	D15 [A15/ D15]	MTIOC9C/MTCLKB/ MTIOC9C#/ MTCLKB#/TMRI4	CTS8#/RTS8#/ SS8#/SCK8/ RSPCKA		IRQ7-DS	AN216	ADTRG0#/ COMP4
70		P65	A12				IRQ9	AN211/ CMPC53/ DA1	
71		P64	A13				IRQ8	AN210/ CMPC33/ DA0	
72	AVCC2								
73	AVSS2								
74		P63	A14/A12				IRQ7	AN209/ CMPC23	
75		P62	A15/A13				IRQ6	AN208/ CMPC43	
76		P61	A16/A14				IRQ5	AN207/ CMPC13	

Table 1.6 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (5/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Communications (USB)	Interrupt (IRQ, NMI)	Analog	Others
77		P60	A17/A15				IRQ4	AN206/ CMPC03	
78		P55	A18/A16				IRQ3	AN203/ CMPC32	
79		P54	A19/A17				IRQ2	AN202/ CMPC22	
80		P53	A20/A18				IRQ1	AN201/ CMPC12	
81		P52					IRQ0	AN200/ CMPC02	
82		P47						AN103	
83		P46						AN102/ CMPC50/ CMPC51	
84		P45						AN101/ CMPC40/ CMPC41	
85		P44						AN100/ CMPC30/ CMPC31	
86		PH4						AN107/ PGAVSS1	
87		P43						AN003	
88		P42						AN002/ CMPC20/ CMPC21	
89		P41						AN001/ CMPC10/ CMPC11	
90		P40						AN000/ CMPC00/ CMPC01	
91		PH0						AN007/ PGAVSS0	
92	AVCC1								
93	AVCC0								
94	AVSS0								
95	AVSS1								
96		P82	ALE/WAIT#	MTIC5U/MTIC5U#/ TMO4	SCK6/SCK12		IRQ3		COMP5
97		P81	CS2#	MTIC5V/MTIC5V#/ TMCI4	TXD6/SMOSI6/ SSDA6/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12				COMP4
98		P80	CS1#	MTIC5W/MTIC5W#/ TMRI4	RXD6/SMISO6/ SSCL6/RXD12/ SMISO12/SSCL12/ RXDX12		IRQ5		COMP3
99		P11	RD#	MTIOC3A/MTCLKC/ MTIOC3A#/ MTCLKC#/ MTIOC9D/GTIOC3B/ GTETRGA/ GTIOC3B#/ GTETRGC/TMO3/ POE9#			IRQ1-DS		
100		P10		MTIOC9B/MTCLKD/ MTIOC9B#/ MTCLKD#/ GTETRGB/ GTETRGD/TMRI3/ POE12#	CTS6#/RTS6#/ SS6#		IRQ0-DS		

1.6.3 100-Pin LFQFP (with PGA pseudo-differential input and without USB pin)

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin) (1/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
1		PE5	BCLK	MTIOC9D/MTIOC9D#/ GTIOC3A/GTETRGB/ GTIOC3A#/GTETRGD	SCK9/CTS9#/RTS9#/ SS9#	IRQ0		ADST0
2	EMLE							
3	VSS							
4	UB	P00	A11	MTIOC9A/MTIOC9A#/ CACREF	RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXDX12	IRQ2		ADST1/ COMP0
5	VCL							
6	MD/FINED							
7		P01	A10	MTIOC9C/MTIOC9C#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE12#	TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	IRQ4		ADST2/ COMP1
8		PE4	A9	MTCLKC/MTCLKC#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE10#	SCK9	IRQ1		
9		PE3	A8	MTCLKD/MTCLKD#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE11#	CTS9#/RTS9#/SS9#	IRQ2-DS		
10	RES#							
11	XTAL	P37						
12	VSS							
13	EXTAL	P36						
14	VCC							
15		PE2		POE10#		NMI		
16		PE1	WR0#/WR#	MTIOC9D/MTIOC9D#/ TMO5	CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/SSLA3	IRQ15		
17		PE0	WR1#/BC1#/ WAIT#	MTIOC9B/MTIOC9B#/ TMCI1/TMCI5	RXD5/SMISO5/SSCL5/ SSLA2/CRX0	IRQ7		
18	TRST#	PD7		MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/ GTIOC0A#/GTIOC3A#/ TMRI1/TMRI5	TXD5/SMOSI5/SSDA5/ SSLA1/CTX0	IRQ8		
19	TMS	PD6		MTIOC9C/MTIOC9C#/ GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ TMO1	CTS1#/RTS1#/SS1#/ CTS11#/RTS11#/ SS11#/SSLA0	IRQ5		ADST0
20	TDI	PD5		GTIOC1A/GTETRGA/ GTIOC1A#/TMRI0/ TMRI6	RXD1/SMISO1/SSCL1/ RXD11/SMISO11/ SSCL11	IRQ6		
21	TCK	PD4		GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/ TMCI6	SCK1/SCK11	IRQ2		
22	TDO	PD3		GTIOC2A/GTETRGC/ GTIOC2A#/TMO0	TXD1/SMOSI1/SSDA1/ TXD11/SMOSI11/ SSDA11			
23	TRCLK	PD2	A7	GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/ TMCI1/TMO4	SCK5/SCK8/MOSIA			
24	TRDATA3	PD1	A6	GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/ TMO2	RXD8/SMISO8/SSCL8/ MISOA			

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin) (2/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
25	TRDATA2	PD0	A5	GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/ TMO6	TXD8/SMOSI8/SSDA8/ RSPCKA			
26	TRDATA1	PB7	A4	GTIOC1B/GTIOC1B#	SCK5/SCK11/SCK12			
27	TRDATA0	PB6	A3	GTIOC2A/GTIOC2A#	RXD5/SMISO5/SSCL5/ RXD11/SMISO11/ SSCL11/RXD12/ SMISO12/SSCL12/ RXDX12/CRX0	IRQ2		
28	TRSYNC	PB5	A2	GTIOC2B/GTIOC2B#	TXD5/SMOSI5/SSDA5/ TXD11/SMOSI11/ SSDA11/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0			
29	VCC							
30		PB4	A1	GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE8#	CTS5#/RTS5#/SS5#/ SCK11/CTS11#/ RTS11#/SS11#	IRQ3-DS		
31	VSS							
32		PB3	A7	MTIOC0A/MTIOC0A#/ CACREF	SCK6/RSPCKA	IRQ9		
33		PB2	A6	MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0	TXD6/SMOSI6/SSDA6/ SDA0			ADSM0
34		PB1	A5	MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0	RXD6/SMISO6/SSCL6/ SCL0	IRQ4		ADSM1
35		PB0	A0/A4/BC0#	MTIOC0D/MTIOC0D#/ TMO0	TXD6/SMOSI6/SSDA6/ CTS11#/RTS11#/ SS11#/MOSIA	IRQ8		ADTRG2#
36		PA5	A3	MTIOC1A/MTIOC1A#/ TMCI3	RXD6/SMISO6/SSCL6/ RXD8/SMISO8/SSCL8/ MISOA	IRQ1		ADTRG1#
37		PA4	A2	MTIOC1B/MTIOC1B#/ TMCI7	SCK6/TXD8/SMOSI8/ SSDA8/RSPCKA			ADTRG0#
38		PA3	A1	MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7	TXD9/SMOSI9/SSDA9/ SCK8/SSLA0			
39		PA2	A0/BC0#	MTIOC2B/MTIOC2B#/ GTADSM1/TMO7	CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/ SCK11/SSLA1			
40		PA1		MTIOC6A/MTIOC6A#/ TMO4	TXD9/SMOSI9/SSDA9/ RXD11/SMISO11/ SSCL11/SSLA2/CRX0	IRQ14-DS		ADTRG0#
41		PA0		MTIOC6C/MTIOC6C#/ TMO2	SCK9/TXD11/SMOSI11/ SSDA11/SSLA3/CTX0			
42	VCC							
43		P96	CS0#/WAIT#	GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE4#	CTS8#/RTS8#/SS8#	IRQ4-DS		
44	VSS							
45		P95		MTIOC6B/MTIOC6B#/ GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#				
46		P94		MTIOC7A/MTIOC7A#/ GTIOC5A/GTIOC8A/ GTIOC5A#/GTIOC8A#				
47		P93		MTIOC7B/MTIOC7B#/ GTIOC6A/GTIOC9A/ GTIOC6A#/GTIOC9A#				
48		P92		MTIOC6D/MTIOC6D#/ GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#				

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin) (3/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
49		P91		MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC8B/ GTIOC5B#/GTIOC8B#				
50		P90		MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC9B/ GTIOC6B#/GTIOC9B#				
51		P76	D0 [A0/D0]	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B#				
52		P75	D1 [A1/D1]	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#				
53		P74	D2 [A2/D2]	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#				
54		P73	D3 [A3/D3]	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A#				
55		P72	D4 [A4/D4]	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A#				
56		P71	D5 [A5/D5]	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A#				
57		P70	D6 [A6/D6]	GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE0#	CTS9#/RTS9#/SS9#	IRQ5-DS		
58		P33	D7 [A7/D7]	MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/ GTIOC3B/GTIOC3B#/ TMO0	SSLA3	IRQ13-DS		
59		P32	D8 [A8/D8]	MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/ GTIOC3A/GTIOC3A#/ TMO6	SSLA2	IRQ12-DS		
60	VCC							
61		P31	D9 [A9/D9]	MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMRI6	SSLA1	IRQ6		
62	VSS							
63		P30	D10 [A10/D10]	MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/ TMCI6	SCK8/CTS8#/RTS8#/ SS8#/SSLA0	IRQ7		COMP3
64		P27	CS3	MTIOC1A/MTIOC0C/ MTIOC1A#/ MTIOC0C#/POE9#		IRQ15		
65		P24	D11 [A11/D11]	MTIC5U/MTIC5U#/ TMCI2/TMO6	CTS8#/RTS8#/SS8#/ SCK8/RSPCKA	IRQ4		COMP0
66		P23	D12 [A12/D12]	MTIC5V/MTIC5V#/ TMO2/CACREF	TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MOSIA/CTX0	IRQ11		COMP1
67		P22	D13 [A13/D13]	MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/ MTIOC9B/TMRI2/ TMO4	RXD8/SMISO8/SSCL8/ RXD12/SMISO12/ SSCL12/RXDX12/ MISOA/CRX0	IRQ10		ADTRG2#/ COMP2
68		P21	D14 [A14/D14]	MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMCI4	TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MOSIA	IRQ6-DS	AN217	ADTRG1#/ COMP5
69		P20	D15 [A15/D15]	MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMRI4	CTS8#/RTS8#/SS8#/ SCK8/RSPCKA	IRQ7-DS	AN216	ADTRG0#/ COMP4

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin) (4/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
70		P65	A12			IRQ9	AN211/ CMPC53/ DA1	
71		P64	A13			IRQ8	AN210/ CMPC33/ DA0	
72	AVCC2							
73	AVSS2							
74		P63	A12/A14			IRQ7	AN209/ CMPC23	
75		P62	A13/A15			IRQ6	AN208/ CMPC43	
76		P61	A14/A16			IRQ5	AN207/ CMPC13	
77		P60	A15/A17			IRQ4	AN206/ CMPC03	
78		P55	A16/A18			IRQ3	AN203/ CMPC32	
79		P54	A17/A19			IRQ2	AN202/ CMPC22	
80		P53	A18/A20			IRQ1	AN201/ CMPC12	
81		P52				IRQ0	AN200/ CMPC02	
82		P47					AN103	
83		P46					AN102/ CMPC50/ CMPC51	
84		P45					AN101/ CMPC40/ CMPC41	
85		P44					AN100/ CMPC30/ CMPC31	
86		PH4					AN107/ PGAVSS1	
87		P43					AN003	
88		P42					AN002/ CMPC20/ CMPC21	
89		P41					AN001/ CMPC10/ CMPC11	
90		P40					AN000/ CMPC00/ CMPC01	
91		PH0					AN007/ PGAVSS0	
92	AVCC1							
93	AVCC0							
94	AVSS0							
95	AVSS1							
96		P82	ALE/WAIT#	MTIC5U/MTIC5U#/ TMO4	SCK6/SCK12	IRQ3		COMP5
97		P81	CS2#	MTIC5V/MTIC5V#/ TMCI4	TXD6/SMOSI6/SSDA6/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12			COMP4

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin) (5/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
98		P80	CS1#	MTIC5W/MTIC5W#/ TMRI4	RXD6/SMISO6/SSCL6/ RXD12/SMISO12/ SSCL12/RXDX12	IRQ5		COMP3
99		P11	RD#	MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ MTIOC9D/GTIOC3B/ GTETRGA/GTIOC3B#/ GTETRGC/TMO3/ POE9#		IRQ1-DS		
100		P10		MTIOC9B/MTCLKD/ MTIOC9B#/MTCLKD#/ GTETRGB/GTETRGD/ TMRI3/POE12#	CTS6#/RTS6#/SS6#	IRQ0-DS		

1.6.4 100-Pin LFQFP (without PGA pseudo-differential input and without USB pin)

Table 1.8 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (1/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
1		PE5	BCLK	MTIOC9D/MTIOC9D#/ GTIOC3A/GTETRGB/ GTIOC3A#/GTETRGD	SCK9/CTS9#/RTS9#/ SS9#	IRQ0		ADST0
2	EMLE							
3	VSS							
4	UB	P00	A11	MTIOC9A/MTIOC9A#/ CACREF	RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXDX12	IRQ2		ADST1/ COMP0
5	VCL							
6	MD/FINED							
7		P01	A10	MTIOC9C/MTIOC9C#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE12#	TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	IRQ4		ADST2/ COMP1
8		PE4	A9	MTCLKC/MTCLKC#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE10#	SCK9	IRQ1		
9		PE3	A8	MTCLKD/MTCLKD#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE11#	CTS9#/RTS9#/SS9#	IRQ2-DS		
10	RES#							
11	XTAL	P37						
12	VSS							
13	EXTAL	P36						
14	VCC							
15		PE2		POE10#		NMI		
16		PE1	WR0#/WR#	MTIOC9D/MTIOC9D#/ TMO5	CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/SSLA3	IRQ15		
17		PE0	WR1#/BC1#/ WAIT#	MTIOC9B/MTIOC9B#/ TMCI1/TMCI5	RXD5/SMISO5/SSCL5/ SSLA2/CRX0	IRQ7		
18	TRST#	PD7		MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/ GTIOC0A#/GTIOC3A#/ TMRI1/TMRI5	TXD5/SMOSI5/SSDA5/ SSLA1/CTX0	IRQ8		
19	TMS	PD6		MTIOC9C/MTIOC9C#/ GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ TMO1	CTS1#/RTS1#/SS1#/ CTS11#/RTS11#/ SS11#/SSLA0	IRQ5		ADST0
20	TDI	PD5		GTIOC1A/GTETRGA/ GTIOC1A#/TMRI0/ TMRI6	RXD1/SMISO1/SSCL1/ RXD11/SMISO11/ SSCL11	IRQ6		
21	TCK	PD4		GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/ TMCI6	SCK1/SCK11	IRQ2		
22	TDO	PD3		GTIOC2A/GTETRGC/ GTIOC2A#/TMO0	TXD1/SMOSI1/SSDA1/ TXD11/SMOSI11/ SSDA11			
23	TRCLK	PD2	A7	GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/ TMCI1/TMO4	SCK5/SCK8/MOSIA			
24	TRDATA3	PD1	A6	GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/ TMO2	RXD8/SMISO8/SSCL8/ MISOA			

Table 1.8 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (2/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
25	TRDATA2	PD0	A5	GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/ TMO6	TXD8/SMOSI8/SSDA8/ RSPCKA			
26	TRDATA1	PB7	A4	GTIOC1B/GTIOC1B#	SCK5/SCK11/SCK12			
27	TRDATA0	PB6	A3	GTIOC2A/GTIOC2A#	RXD5/SMISO5/SSCL5/ RXD11/SMISO11/ SSCL11/RXD12/ SMISO12/SSCL12/ RXDX12/CRX0	IRQ2		
28	TRSYNC	PB5	A2	GTIOC2B/GTIOC2B#	TXD5/SMOSI5/SSDA5/ TXD11/SMOSI11/ SSDA11/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0			
29	VCC							
30		PB4	A1	GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE8#	CTS5#/RTS5#/SS5#/ SCK11/CTS11#/ RTS11#/SS11#	IRQ3-DS		
31	VSS							
32		PB3	A7	MTIOC0A/MTIOC0A#/ CACREF	SCK6/RSPCKA	IRQ9		
33		PB2	A6	MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0	TXD6/SMOSI6/SSDA6/ SDA0			ADSM0
34		PB1	A5	MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0	RXD6/SMISO6/SSCL6/ SCL0	IRQ4		ADSM1
35		PB0	A0/A4/BC0#	MTIOC0D/MTIOC0D#/ TMO0	TXD6/SMOSI6/SSDA6/ CTS11#/RTS11#/ SS11#/MOSIA	IRQ8		ADTRG2#
36		PA5	A3	MTIOC1A/MTIOC1A#/ TMCI3	RXD6/SMISO6/SSCL6/ RXD8/SMISO8/SSCL8/ MISOA	IRQ1		ADTRG1#
37		PA4	A2	MTIOC1B/MTIOC1B#/ TMCI7	SCK6/TXD8/SMOSI8/ SSDA8/RSPCKA			ADTRG0#
38		PA3	A1	MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7	TXD9/SMOSI9/SSDA9/ SCK8/SSLA0			
39		PA2	A0/BC0#	MTIOC2B/MTIOC2B#/ GTADSM1/TMO7	CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/ SCK11/SSLA1			
40		PA1		MTIOC6A/MTIOC6A#/ TMO4	TXD9/SMOSI9/SSDA9/ RXD11/SMISO11/ SSCL11/SSLA2/CRX0	IRQ14-DS		ADTRG0#
41		PA0		MTIOC6C/MTIOC6C#/ TMO2	SCK9/TXD11/SMOSI11/ SSDA11/SSLA3/CTX0			
42	VCC							
43		P96	CS0#/WAIT#	GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE4#	CTS8#/RTS8#/SS8#	IRQ4-DS		
44	VSS							
45		P95		MTIOC6B/MTIOC6B#/ GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#				
46		P94		MTIOC7A/MTIOC7A#/ GTIOC5A/GTIOC8A/ GTIOC5A#/GTIOC8A#				
47		P93		MTIOC7B/MTIOC7B#/ GTIOC6A/GTIOC9A/ GTIOC6A#/GTIOC9A#				
48		P92		MTIOC6D/MTIOC6D#/ GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#				

Table 1.8 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (3/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
49		P91		MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC8B/ GTIOC5B#/GTIOC8B#				
50		P90		MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC9B/ GTIOC6B#/GTIOC9B#				
51		P76	D0 [A0/D0]	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B#				
52		P75	D1 [A1/D1]	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#				
53		P74	D2 [A2/D2]	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#				
54		P73	D3 [A3/D3]	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A#				
55		P72	D4 [A4/D4]	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A#				
56		P71	D5 [A5/D5]	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A#				
57		P70	D6 [A6/D6]	GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE0#	CTS9#/RTS9#/SS9#	IRQ5-DS		
58		P33	D7 [A7/D7]	MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/ GTIOC3B/GTIOC3B#/ TMO0	SSLA3	IRQ13-DS		
59		P32	D8 [A8/D8]	MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/ GTIOC3A/GTIOC3A#/ TMO6	SSLA2	IRQ12-DS		
60	VCC							
61		P31	D9 [A9/D9]	MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMRI6	SSLA1	IRQ6		
62	VSS							
63		P30	D10 [A10/D10]	MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/ TMCI6	SCK8/CTS8#/RTS8#/ SS8#/SSLA0	IRQ7		COMP3
64		P24	D11 [A11/D11]	MTIC5U/MTIC5U#/ TMCI2/TMO6	CTS8#/RTS8#/SS8#/ SCK8/RSPCKA	IRQ4		COMP0
65		P23	D12 [A12/D12]	MTIC5V/MTIC5V#/ TMO2/CACREF	TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MOSIA/CTX0	IRQ11		COMP1
66		P22	D13 [A13/D13]	MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/ MTIOC9B/TMRI2/ TMO4	RXD8/SMISO8/SSCL8/ RXD12/SMISO12/ SSCL12/RXDX12/ MISOA/CRX0	IRQ10		ADTRG2#/ COMP2
67		P21	D14 [A14/D14]	MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMCI4	TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MOSIA	IRQ6-DS	AN217	ADTRG1#/ COMP5
68		P20	D15 [A15/D15]	MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMRI4	CTS8#/RTS8#/SS8#/ SCK8/RSPCKA	IRQ7-DS	AN216	ADTRG0#/ COMP4
69		P65	A12			IRQ9	AN211/ CMPC53/ DA1	

Table 1.8 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (4/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
70		P64	A13			IRQ8	AN210/ CMPC33/ DA0	
71	AVCC2							
72	AVCC2							
73	AVSS2							
74		P63	A12/A14			IRQ7	AN209/ CMPC23	
75		P62	A13/A15			IRQ6	AN208/ CMPC43	
76		P61	A14/A16			IRQ5	AN207/ CMPC13	
77		P60	A15/A17			IRQ4	AN206/ CMPC03	
78		P55	A16/A18			IRQ3	AN203/ CMPC32	
79		P54	A17/A19			IRQ2	AN202/ CMPC22	
80		P53	A18/A20			IRQ1	AN201/ CMPC12	
81		P52				IRQ0	AN200/ CMPC02	
82		P51					AN205/ CMPC52	
83		P50					AN204/ CMPC42	
84		P47					AN103	
85		P46					AN102/ CMPC50/ CMPC51	
86		P45					AN101/ CMPC40/ CMPC41	
87		P44					AN100/ CMPC30/ CMPC31	
88		P43					AN003	
89		P42					AN002/ CMPC20/ CMPC21	
90		P41					AN001/ CMPC10/ CMPC11	
91		P40					AN000/ CMPC00/ CMPC01	
92	AVCC1							
93	AVCC0							
94	AVSS0							
95	AVSS1							
96		P82	ALE/WAIT#	MTIC5U/MTIC5U#/ TMO4	SCK6/SCK12	IRQ3		COMP5
97		P81	CS2#	MTIC5V/MTIC5V#/ TMCI4	TXD6/SMOSI6/SSDA6/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12			COMP4

Table 1.8 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (5/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, GPTW, TMR, POE, POEG, CAC)	Communications (SCI, RSPI, RIIC, CAN)	Interrupt (IRQ, NMI)	Analog	Others
98		P80	CS1#	MTIC5W/MTIC5W#/ TMRI4	RXD6/SMISO6/SSCL6/ RXD12/SMISO12/ SSCL12/RXDX12	IRQ5		COMP3
99		P11	RD#	MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ MTIOC9D/GTIOC3B/ GTETRGA/GTIOC3B#/ GTETRGC/TMO3/ POE9#		IRQ1-DS		
100		P10		MTIOC9B/MTCLKD/ MTIOC9B#/MTCLKD#/ GTETRGB/GTETRGD/ TMRI3/POE12#	CTS6#/RTS6#/SS6#	IRQ0-DS		

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0V

Item			Symbol	Value	Unit
Power supply voltage*1			VCC	–0.3 to +6.5	V
USB power supply voltage*1			VCC_USB	–0.3 to +6.5	
Analog power supply voltage*1			AVCC0, AVCC1, AVCC2	–0.3 to +6.5	
Input voltage	PB1, PB2, PC0, and PD2		V_{in}	–0.3 to +6.5	
	P40 to P42, P44 to P46, PH0, and PH4	With negative input enabled*2		–1.0 to AVCC1 + 0.3 (up to 6.5)	
		With negative input disabled		–0.3 to AVCC1 + 0.3 (up to 6.5)	
	P43, P47, PH1 to PH3, and PH5 to PH7			–0.3 to AVCC1 + 0.3 (up to 6.5)	
	P50 to P55, and P60 to P65			–0.3 to AVCC2 + 0.3 (up to 6.5)	
	USB0_DP, USB0_DM			–0.3 to VCC_USB + 0.3 (up to 6.5)	
	Other than above			–0.3 to VCC + 0.3 (up to 6.5)	
Junction temperature		D version	T_j	–40 to +105	°C
		G version		–40 to +125	
Storage temperature			T_{stg}	–55 to +125	

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Insert capacitors with good frequency characteristics between each power supply pin and the ground. Specifically, place capacitors with a value around 0.1 µF as close as possible to every power supply pin, and use the shortest and thickest possible traces.

Note 2. When VOLSR.PGAVLS = 0 and ADPGADCR0.PxDEN = 1 (x = 000, 001, 002, 100, 101, 102).

2.2 Recommended operating conditions

Table 2.2 Recommended operating conditions (1)

Item			Symbol	Min.	Typ.	Max.	Unit
Power supply voltage			VCC*1	2.7	—	5.5	V
			VSS	—	0	—	
USB power supply voltage*2		When USB in use	VCC_USB*1	3.0	—	3.6	
			VSS_USB	—	0	—	
		When USB not in use	VCC_USB	—	VCC	—	
			VSS_USB	—	VSS	—	
Analog power supply voltage*3			AVCC0, AVCC1, AVCC2*1	3.0	—	5.5	
			AVSS0, AVSS1, AVSS2	—	0	—	
Input voltage	PB1, PB2, PC0, and PD2		V_{in}	–0.3	—	5.8	
	P40 to P42, and P44 to P46	With negative input enabled*4		–1.0	—	AVCC1 + 0.3	
		With negative input disabled		–0.3	—		
	PH0, PH4	With negative input enabled*4		–0.5	—	AVCC1 + 0.3	
		With negative input disabled		–0.3	—		
	P43, P47, PH1 to PH3, and PH5 to PH7			–0.3	—	AVCC1 + 0.3	
	P50 to P55, and P60 to P65			–0.3	—	AVCC2 + 0.3	
	USB0_DP, USB0_DM			–0.3	—	VCC_USB + 0.3	
	Other than above			–0.3	—	VCC + 0.3	
Operating temperature	D version		T_{opr}	–40	—	85	°C
	G version			–40	—	105	

Note 1. Comply with the following voltage condition: VCC_USB ≤ VCC ≤ AVCC0 = AVCC1 = AVCC2
Note 2. When the USB interface is not to be used, connect VCC_USB to VCC and VSS_USB to VSS, and set VOLSR.USBVON=0.
Note 3. When not using any of the12-bit A/D converter (unit 0 to 2), 12-bit D/A converter, comparator C, or temperature sensor, connect AVCC0, AVCC1, and AVCC2 to VCC, and AVSS0, AVSS1, and AVSS2 to VSS, respectively. For details, refer to section 39.6.10, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.
Note 4. When VOLSR.PGAVLS = 0 and ADPGADCR0.PxDEN = 1 (x = 000, 001, 002, 100, 101, 102).

Table 2.3 Recommended operating conditions (2)

Item	Symbol	Value
Decoupling capacitance for stabilizing the internal voltage	C_{VCL}	0.47 µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor with a nominal capacitance of 0.47 µF, for which the sum of the capacitance tolerance and change in the capacitance under the usage conditions will be no greater than ±30%.

2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin MTU input pin GPTW input pin POE input pin POEG input pin TMR input pin SCI input pin ADTRG# input pin RES#, NMI	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	IRQ input pin (except for P52 to P55, and P60 to P65)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	IRQ input pin (P52 to P55, and P60 to P65)	V_{IH}	0.8 × AVCC2	—	—		
		V_{IL}	—	—	0.2 × AVCC2		
		ΔV_T	0.06 × AVCC2	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	—		
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	Pins for 5 V tolerant (PB1, PB2, PC0, and PD2)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	Analog input pins (P40 to P47, and PH0 to PH7)	V_{IH}	0.8 × AVCC1	—	—		
		V_{IL}	—	—	0.2 × AVCC1		
	Analog input pins (P50 to P55, and P60 to P65)	V_{IH}	0.8 × AVCC2	—	—		
		V_{IL}	—	—	0.2 × AVCC2		
	Other input pins (pins other than those above)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
High-level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	0.9 × VCC	—	—	V	
	EXTAL, WAIT#, RSPI input pin		0.8 × VCC	—	—		
	D0 to D15		0.7 × VCC	—	—		
	RIIC (SMBus)		2.1	—	—		
Low-level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	—	—	0.1 × VCC	V	
	EXTAL, WAIT#, RSPI input pin		—	—	0.2 × VCC		
	D0 to D15		—	—	0.3 × VCC		
	RIIC (SMBus)		—	—	0.8		

Table 2.5 DC Characteristics (2)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High-level output voltage	P43, P47, PH1 to PH3, and PH5 to PH7	V_{OH}	AVCC1 – 0.5	—	—	V	I_{OH} = –1.0 mA
	P50 to P55, and P60 to P65		AVCC2 – 0.5	—	—		I_{OH} = –1.0 mA
	P90 to P95, P71 to P76, P81, PB5, and PD3		VCC – 1.0	—	—		I_{OH} = –5.0 mA (when the large current output is set)
	Other than above		VCC – 0.5	—	—		I_{OH} = –1.0 mA
Low-level output voltage	P43, P47, PH1 to PH3, and PH5 to PH7	V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
	P50 to P55, and P60 to P65		—	—	0.5		I_{OL} = 1.0 mA
	P90 to P95, P71 to P76, P81, PB5, and PD3		—	—	1.0		I_{OL} = 15 mA (when the large current output is set)
	RIIC pins		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	Other than above		—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, PE2, and EMLE*1	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
	P40 to P42, and P44 to P46		—	—	1.0		V_{in} = 0 V V_{in} = AVCC1
	PH0 and PH4		—	—	1.0		V_{in} = 0 V V_{in} = AVCC1 VOLSR.PGAVLS = 1
Three-state leakage current (off state)	RIIC pins	$\lvert I_{TSI} \rvert$	—	—	5.0		V_{in} = 0 V V_{in} = VCC
	Other than above		—	—	1.0		
Input pull-up resistors	P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65	R_{PU}	10	—	100	kΩ	AVCC1 = AVCC2 = 3.0 to 5.5 V V_{in} = 0 V
	Pins other than those above and PE2		10	—	100		VCC = 2.7 to 5.5 V V_{in} = 0 V
Input pull-down resistors	EMLE	R_{PD}	10	—	100		V_{in} = VCC = AVCC
Input capacitance	RIIC pins, PH0, and PH4	C_{in}	—	—	16	pF	V_{bias} = 0 V V_{amp} = 20 mV f = 1 MHz T_a = 25°C
	USB0_DP, and USB0_DM pins		—	—	16		
	Other than above		—	—	8		
Output voltage of the VCL pin		V_{CL}	—	1.25	—	V	

Note 1. The input leakage current value at the EMLE pin is only when V_{in} = 0 V.

Table 2.6 DC Characteristics (3) (D version)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item				Symbol	D version			Unit	Test Conditions
					Min.	Typ.	Max.		
Supply current*1	Normal operating mode	Full operation*2		I_{CC}*3	—	—	123	mA	ICLK = 200 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 200 MHz PCLKD = 50 MHz FCLK = 50 MHz BCLK = 50 MHz BCLK pin = 25 MHz
		Normal operation	Peripheral module clocks are supplied*4		—	28	—		
			Peripheral module clocks are stopped *4, *5		—	16	—		
		CoreMark	Peripheral module clocks are stopped *4, *5		—	27	—		
		Sleep mode: Peripheral module clocks are supplied*4			—	23	48		
		All module clock stop mode (reference value)			—	10.9	34		
		Increase current by BGO operation*6			—	14	—		
		Increase current by operating Trusted Secure IP			—	3.9	5.3		
	Software standby mode				—	0.9	13.9		VOLSR.PGAVLS = 1
	Deep software standby mode				—	15	21	µA	VOLSR.PGAVLS = 1

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).
Note 3. I_{CC} depends on f (ICLK) as follows.
(when ICLK : PCLKA : PCLKB : PCLKC : PCLKD : BCLK : BCLK pin = 8 : 4 : 2 : 8 : 2 : 2 : 1 and EXTAL = 20 MHz)
• D version product
I_{CC} Max. = 0.51 × f + 21 (full operation in normal operating mode)
I_{CC} Typ. = 0.115 × f + 5 (normal operation in normal operating mode)
I_{CC} Max. = 0.135 × f + 21 (sleep mode)
Note 4. This does not include operations as BGO (background operations). Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the frequencies of FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD, and the BCLK pin are the same.
Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Table 2.7 DC Characteristics (3) (G version)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item				Symbol	G version			Unit	Test Conditions
					Min.	Typ.	Max.		
Supply current*1	Normal operating mode	Full operation*2		I_{CC}*3	—	—	136	mA	ICLK = 200 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 200 MHz PCLKD = 50 MHz FCLK = 50 MHz BCLK = 50 MHz BCLK pin = 25 MHz
		Normal operation	Peripheral module clocks are supplied*4		—	28	—		
			Peripheral module clocks are stopped *4, *5		—	16	—		
		CoreMark	Peripheral module clocks are stopped *4, *5		—	27	—		
		Sleep mode: Peripheral module clocks are supplied*4			—	23	60		
		All module clock stop mode (reference value)			—	10.9	46		
		Increase current by BGO operation*6			—	14	—		
		Increase current by operating Trusted Secure IP			—	3.9	5.3		
	Software standby mode				—	0.9	22.1		VOLSR.PGAVLS = 1
	Deep software standby mode				—	15	28	µA	VOLSR.PGAVLS = 1

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).
Note 3. I_{CC} depends on f (ICLK) as follows.
(when ICLK : PCLKA : PCLKB : PCLKC : PCLKD : BCLK : BCLK pin = 8 : 4 : 2 : 8 : 2 : 2 : 1 and EXTAL = 20 MHz)
• G version product
I_{CC} Max. = 0.535 × f + 29 (full operation in normal operating mode)
I_{CC} Typ. = 0.115 × f + 5 (normal operation in normal operating mode)
I_{CC} Max. = 0.155 × f + 29 (sleep mode)
Note 4. This does not include operations as BGO (background operations). Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the frequencies of FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD, and the BCLK pin are the same.
Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Table 2.8 DC Characteristics (4)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	Unit 0	During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: enabled for all channels)	AI_{CC}	—	2.9	5.1	mA	IAVCC0_AD + SH + PGA
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: disabled for all channels)		—	1.9	2.9		IAVCC0_AD + SH
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: enabled for all channels)		—	2.0	4.0		IAVCC0_AD + PGA
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: disabled for all channels)		—	1.0	1.5		IAVCC0_AD
	Unit 1	During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: enabled for all channels)		—	2.9	5.1		IAVCC1_AD + SH + PGA
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: disabled for all channels)		—	1.9	2.9		IAVCC1_AD + SH
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: enabled for all channels)		—	2.0	4.0		IAVCC1_AD + PGA
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: disabled for all channels)		—	1.0	1.5		IAVCC1_AD
	Unit 2	During 12-bit A/D conversion with the temperature sensor operating		—	0.9	1.5		IAVCC2_AD + TEMP
		During 12-bit A/D conversion with the temperature sensor stopped		—	0.9	1.5		IAVCC2_AD
	Comparator (6 channels)			—	0.5	0.6		IAVCC2_CMP
	During 12-bit D/A conversion (2 channels)			—	0.6	0.8		IAVCC2_DA
	Waiting for 12-bit A/D, 12-bit D/A, Comparator C, and temperature sensor conversion (all units)			—	0.1	0.4		IAVCC0_AD + IAVCC1_AD + IAVCC2_AD + IAVCC2_DA
	12-bit A/D, 12-bit D/A, Comparator C, and temperature sensor are in module stop status (all units)			—	0.2	14.8	μA	IAVCC0_AD + IAVCC1_AD + IAVCC2_AD + IAVCC2_DA
USB operating current	Low speed		$I_{CCUSBLS}$	—	3.6	6.5	mA	VCC_USB = 3.0 to 3.6 V
	Full speed		$I_{CCUSBFS}$	—	4.1	10		VCC_USB = 3.0 to 3.6 V
RAM retention voltage			V_{RAM}	2.7	—	—	V	

Table 2.9 DC Characteristics (5)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC ramp rate at power-on	At normal startup	SrVCC	0.02	—	8	ms/V	
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	20		
VCC ramp rate at power fluctuation		dt/dVCC	1.0	—	—		When VCC change exceeds VCC ±10%

Note 1. When OFS1.LVDAS = 0.
Note 2. Settings of the OFS1 register are not read in boot mode or user boot mode, so turn on the power supply voltage with a ramp rate at normal startup.

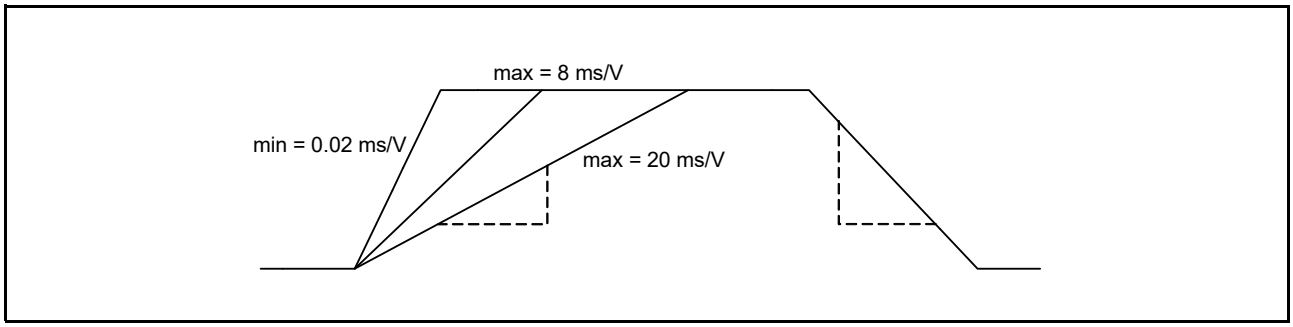


Figure 2.1 VCC Ramp Rate at Power-On

Table 2.10 Permissible Output Currents

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible low-level output current (average value per pin)	All output pins (except for RIIC pins, P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65)	Normal drive*1	I_{OL}	—	—	2.0	mA
		High drive*2		—	—	2.0	
		Large current output*3		—	—	15.0	
	RIIC pins	Standard mode		—	—	3	
		Fast mode		—	—	6	
	P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65			—	—	2.0	
Permissible low-level output current (max. value per pin)	All output pins (except for RIIC pins, P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65)	Normal drive*1		—	—	4.0	
		High drive*2		—	—	4.0	
		Large current output*3		—	—	15.0	
	RIIC pins	Standard mode		—	—	3	
		Fast mode		—	—	6	
	P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65			—	—	4.0	
Permissible low-level output current (total)	Total of all output pins		ΣI_{OL}	—	—	110	
Permissible high-level output current (average value per pin)	All output pins (except for P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65)	Normal drive*1	I_{OH}	—	—	–2.0	
		High drive*2		—	—	–2.0	
		Large current output*3		—	—	–5.0	
	P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65			—	—	–2.0	
Permissible high-level output current (max. value per pin)	All output pins (except for P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65)	Normal drive*1		—	—	–4.0	
		High drive*2		—	—	–4.0	
		Large current output*3		—	—	–5.0	
	P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65			—	—	–4.0	
Permissible high-level output current (total)	Total of all output pins		ΣI_{OH}	—	—	–35	

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when large current output is set with a pin for which large current output ability is selectable.

Table 2.11 Standard Output Characteristics (1)

Conditions: VCC = AVCC0 = AVCC1 = AVCC2 = 5.0 V, VCC_USB = 2.7 to 5.5 V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	Normal drive output (all output pins)	V_{OH}	—	4.97	—	V	I_{OH} = –0.5 mA
			—	4.94	—		I_{OH} = –1.0 mA
			—	4.87	—		I_{OH} = –2.0 mA
			—	4.74	—		I_{OH} = –4.0 mA
	High-drive output (P00, P01, P10 to P17, P20 to P27, P30 to P35, P70 to P76, P80 to P82, P90 to P96, PA0 to PA7, PB0 to PB7, PC0 to PC6, PD0 to PD7, PE0, PE1, PE3 to PE6, PF0 to PF3, PG0 to PG2, PK0 to PK2)		—	4.98	—		I_{OH} = –0.5 mA
			—	4.97	—		I_{OH} = –1.0 mA
			—	4.94	—		I_{OH} = –2.0 mA
			—	4.87	—		I_{OH} = –4.0 mA
	Large current output (P71 to P76, P81, P90 to P95, PB5, PD3)		—	4.99	—		I_{OH} = –0.5 mA
			—	4.98	—		I_{OH} = –1.0 mA
			—	4.96	—		I_{OH} = –2.0 mA
			—	4.92	—		I_{OH} = –4.0 mA
			—	4.91	—		I_{OH} = –5.0 mA
Output low voltage	Normal drive output (all output pins)	V_{OL}	—	0.02	—	V	I_{OL} = 0.5 mA
			—	0.04	—		I_{OL} = 1.0 mA
			—	0.09	—		I_{OL} = 2.0 mA
			—	0.18	—		I_{OL} = 4.0 mA
	High-drive output (P00, P01, P10 to P17, P20 to P27, P30 to P35, P70 to P76, P80 to P82, P90 to P96, PA0 to PA7, PB0 to PB7, PC0 to PC6, PD0 to PD7, PE0, PE1, PE3 to PE6, PF0 to PF3, PG0 to PG2, PK0 to PK2)		—	0.01	—		I_{OL} = 0.5 mA
			—	0.03	—		I_{OL} = 1.0 mA
			—	0.05	—		I_{OL} = 2.0 mA
			—	0.10	—		I_{OL} = 4.0 mA
	Large current output (P71 to P76, P81, P90 to P95, PB5, PD3)		—	0.01	—		I_{OL} = 0.5 mA
			—	0.02	—		I_{OL} = 1.0 mA
			—	0.04	—		I_{OL} = 2.0 mA
			—	0.07	—		I_{OL} = 4.0 mA
			—	0.09	—		I_{OL} = 5.0 mA
			—	0.18	—		I_{OL} = 10.0 mA
			—	0.28	—		I_{OL} = 15.0 mA

Table 2.12 Standard Output Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = AVCC2 = 3.3 V, VCC_USB = 2.7 to 3.3 V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	Normal drive output (all output pins)	V_{OH}	—	3.26	—	V	I_{OH} = –0.5 mA
			—	3.22	—		I_{OH} = –1.0 mA
			—	3.13	—		I_{OH} = –2.0 mA
			—	2.94	—		I_{OH} = –4.0 mA
	High-drive output (P00, P01, P10 to P17, P20 to P27, P30 to P35, P70 to P76, P80 to P82, P90 to P96, PA0 to PA7, PB0 to PB7, PC0 to PC6, PD0 to PD7, PE0, PE1, PE3 to PE6, PF0 to PF3, PG0 to PG2, PK0 to PK2)		—	3.28	—		I_{OH} = –0.5 mA
			—	3.26	—		I_{OH} = –1.0 mA
			—	3.22	—		I_{OH} = –2.0 mA
			—	3.13	—		I_{OH} = –4.0 mA
	Large current output (P71 to P76, P81, P90 to P95, PB5, PD3)		—	3.29	—		I_{OH} = –0.5 mA
			—	3.27	—		I_{OH} = –1.0 mA
			—	3.25	—		I_{OH} = –2.0 mA
			—	3.20	—		I_{OH} = –4.0 mA
			—	3.17	—		I_{OH} = –5.0 mA
Output low voltage	Normal drive output (all output pins)	V_{OL}	—	0.03	—	V	I_{OL} = 0.5 mA
			—	0.06	—		I_{OL} = 1.0 mA
			—	0.12	—		I_{OL} = 2.0 mA
			—	0.25	—		I_{OL} = 4.0 mA
	High-drive output (P00, P01, P10 to P17, P20 to P27, P30 to P35, P70 to P76, P80 to P82, P90 to P96, PA0 to PA7, PB0 to PB7, PC0 to PC6, PD0 to PD7, PE0, PE1, PE3 to PE6, PF0 to PF3, PG0 to PG2, PK0 to PK2)		—	0.02	—		I_{OL} = 0.5 mA
			—	0.03	—		I_{OL} = 1.0 mA
			—	0.07	—		I_{OL} = 2.0 mA
			—	0.13	—		I_{OL} = 4.0 mA
	Large current output (P71 to P76, P81, P90 to P95, PB5, PD3)		—	0.01	—		I_{OL} = 0.5 mA
			—	0.02	—		I_{OL} = 1.0 mA
			—	0.05	—		I_{OL} = 2.0 mA
			—	0.09	—		I_{OL} = 4.0 mA
			—	0.11	—		I_{OL} = 5.0 mA
			—	0.24	—		I_{OL} = 10.0 mA
			—	0.36	—		I_{OL} = 15.0 mA

Table 2.13 Thermal Resistance Value (Reference)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Package	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal resistance	144-pin LFQFP (PLQP0144KA-B)	θ_{ja}	—	—	32.4	°C/W	JESD51-2 and JESD51-7 compliant
	100-pin LFQFP (PLQP0100KB-B)		—	—	35.0		
	144-pin LFQFP (PLQP0144KA-B)	Ψ_{jt}	—	—	0.6	°C/W	JESD51-2 and JESD51-7 compliant
	100-pin LFQFP (PLQP0100KB-B)		—	—	0.8		

Note: The values are reference values when the 4-layer printed circuit board is used. Thermal resistance depends on the number of layers and size of the board. For details, refer to the JEDEC standards.

2.4 AC Characteristics

Table 2.14 Operating Frequency

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.*3	Unit	Test Conditions
System clock (ICLK)	f	—	—	200	MHz	
Peripheral module clock (PCLKA)		—	—	120		
Peripheral module clock (PCLKB)		—	—	60		
Peripheral module clock (PCLKC)		—	—	200		
Peripheral module clock (PCLKD)		8*1	—	60		AVCC0 = AVCC1 = AVCC2 ≥ 4.5 V
		8*1	—	40		AVCC0 = AVCC1 = AVCC2 < 4.5 V
Flash-IF clock (FCLK)		4*2	—	60		
External bus clock (BCLK)		—	—	60		
BCLK pin output		—	—	40		VCC ≥ 4.5 V, High-drive output is selected in the driving ability control register.
		—	—	32		
USB clock (UCLK)		—	48	—		

Note 1. This restriction is only applied when a 12-bit A/D converter is to be used.
Note 2. This restriction is only applied when flash memory is to be programmed or erased.
Note 3. The maximum frequencies of each clock based on the frequency of ICLK are listed below.
ICLK = 200 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 200 MHz, PCLKD = 50 MHz, FCLK = 50 MHz, BCLK = 50 MHz, BCLK pin output = 25 MHz
ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 120 MHz, PCLKD = 60 MHz, FCLK = 60 MHz, BCLK = 60 MHz, BCLK pin output = 30 MHz
ICLK = 160 MHz, PCLKA = 80 MHz, PCLKB = 40 MHz, PCLKC = 160 MHz, PCLKD = 40 MHz, FCLK = 40 MHz, BCLK = 40 MHz, BCLK pin output = 40 MHz

2.4.1 Reset Timing

Table 2.15 Reset Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2.0	—	—	ms	Figure 2.2
	Deep software standby mode	t_{RESWD}	0.6	—	—		Figure 2.3
	Software standby mode	t_{RESWS}	0.3	—	—		
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—		
Waiting time after release from the RES# pin reset		t_{RESWT}	62	—	63	t_{Lcyc}	Figure 2.2
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	108	—	116		

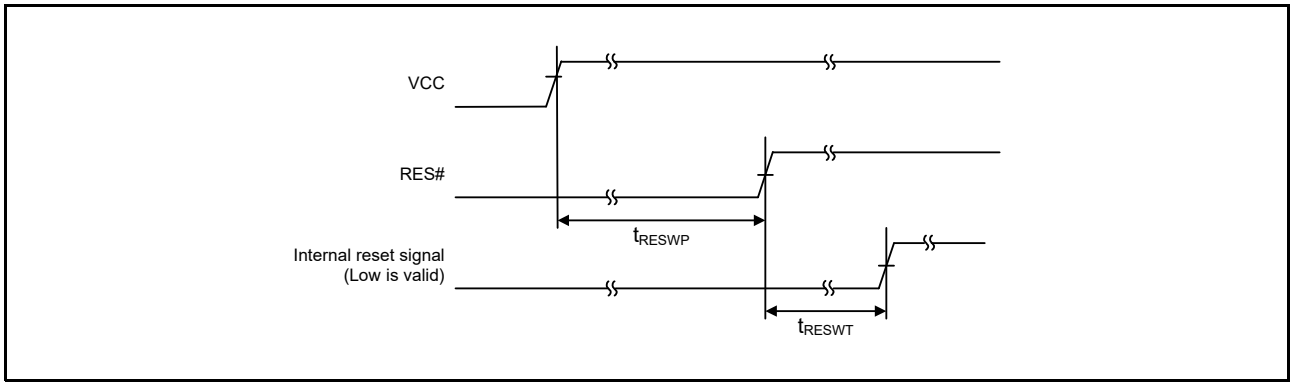


Figure 2.2 Reset Input Timing at Power-On

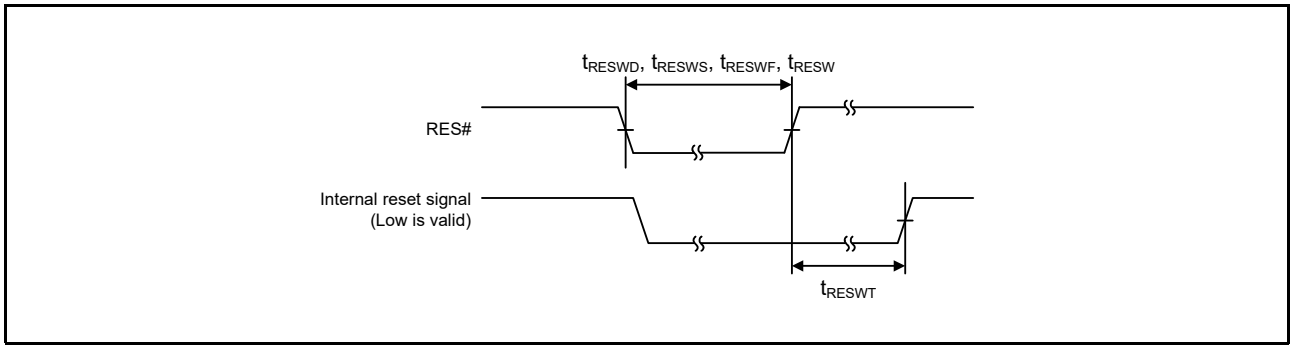


Figure 2.3 Reset Input Timing

2.4.2 Clock Timing

Table 2.16 BCLK Pin Output Clock Timing (1)

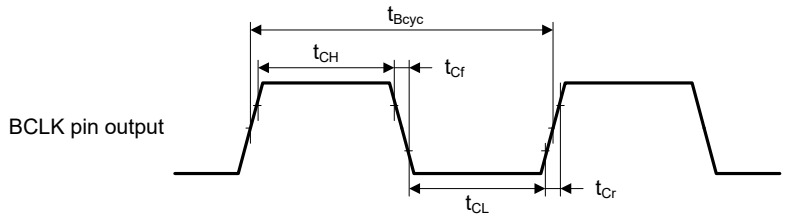
Conditions: 4.5 V ≤ VCC ≤ 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	25	—	—	ns	Figure 2.4
BCLK pin output high pulse width	t_{CH}	7.5	—	—		
BCLK pin output low pulse width	t_{CL}	7.5	—	—		
BCLK pin output rising time	t_{Cr}	—	—	5		
BCLK pin output falling time	t_{Cf}	—	—	5		

Table 2.17 BCLK Pin Output Clock Timing (2)

Conditions: 2.7 V ≤ VCC < 4.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	31.25	—	—	ns	Figure 2.4
BCLK pin output high pulse width	t_{CH}	10.625	—	—		
BCLK pin output low pulse width	t_{CL}	10.625	—	—		
BCLK pin output rising time	t_{Cr}	—	—	5		
BCLK pin output falling time	t_{Cf}	—	—	5		



Test conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF
High-drive output is selected by the driving ability control register.

Figure 2.4 BCLK Pin Output Timing

Table 2.18 EXTAL Clock Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 2.5
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—		
EXTAL external clock rising time	t_{EXr}	—	—	5		
EXTAL external clock falling time	t_{EXf}	—	—	5		

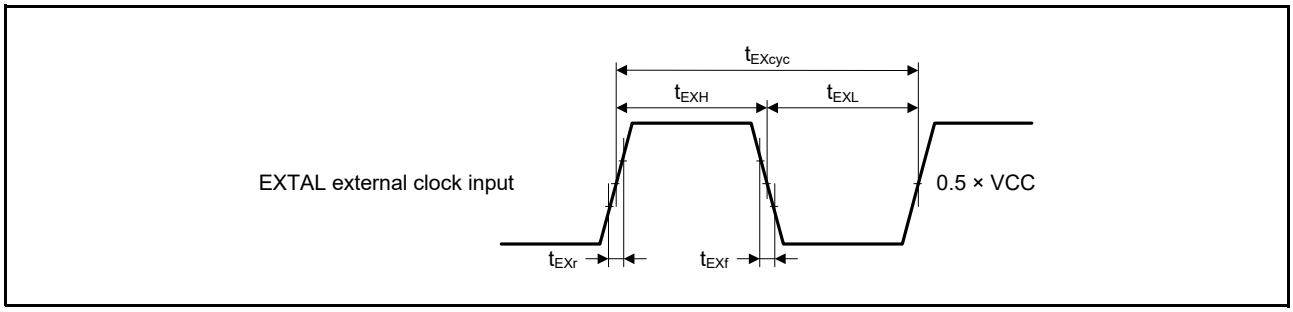


Figure 2.5 EXTAL External Clock Input Timing

Table 2.19 Main Clock Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 2.6
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCWT}$	—	—	—*2		

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.
$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 7] / f_{LOCO}

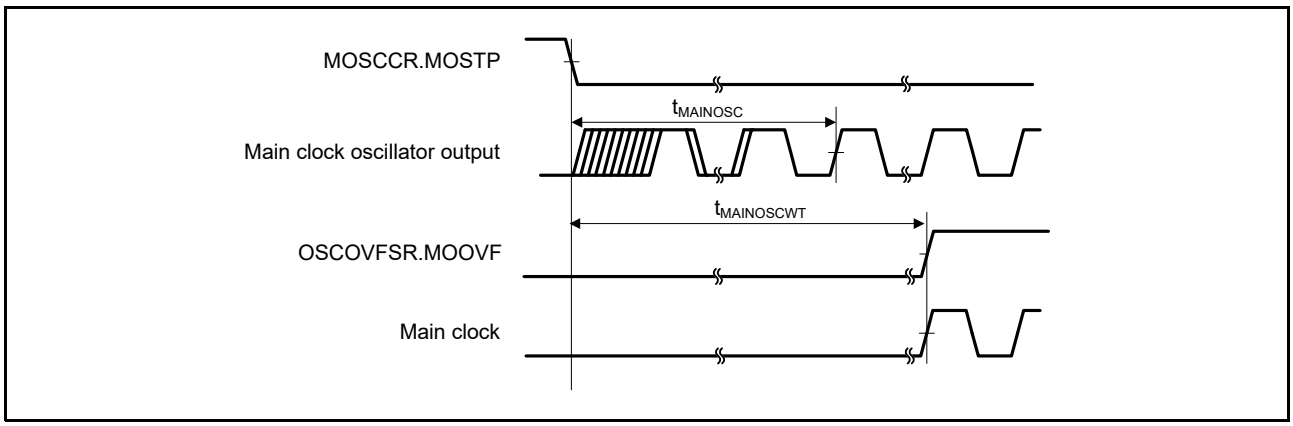


Figure 2.6 Main Clock Oscillation Start Timing

Table 2.20 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	3.78	4.16	4.63	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization time	t_{LOCOWT}	—	—	44	µs	Figure 2.7
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	7.57	8.33	9.26		
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108	120	132	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 2.8

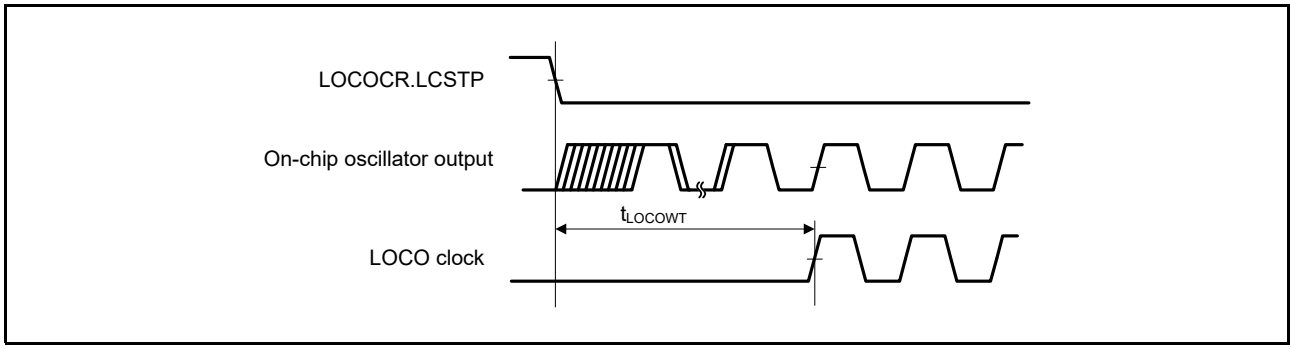


Figure 2.7 LOCO Clock Oscillation Start Timing

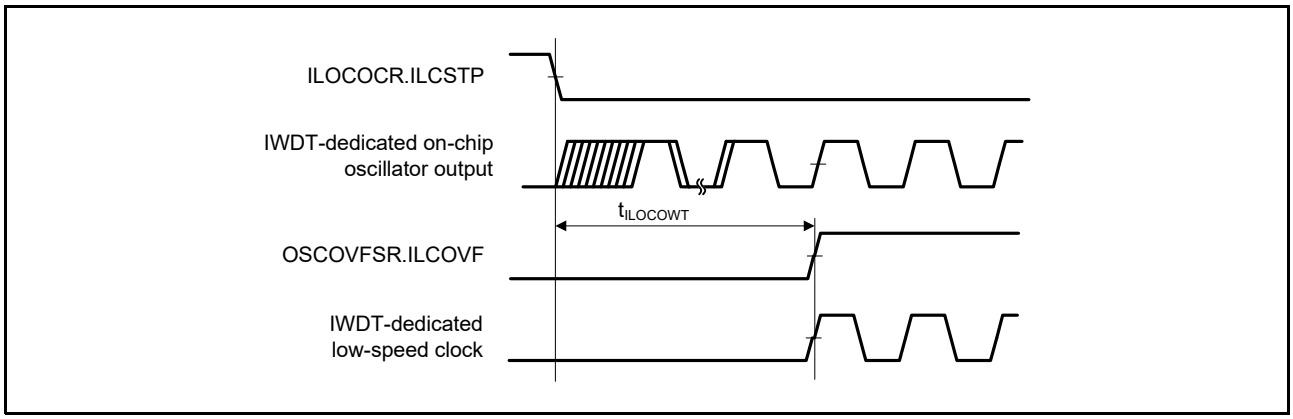


Figure 2.8 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 2.21 HOCO Clock Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.61	16	16.39	MHz	–20°C ≤ T_a ≤ 105°C
		17.56	18	18.44		
		19.52	20	20.48		
		15.52	16	16.48		–40°C ≤ T_a < –20°C
		17.46	18	18.54		
		19.40	20	20.60		
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	μs	Figure 2.9
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150		Figure 2.10

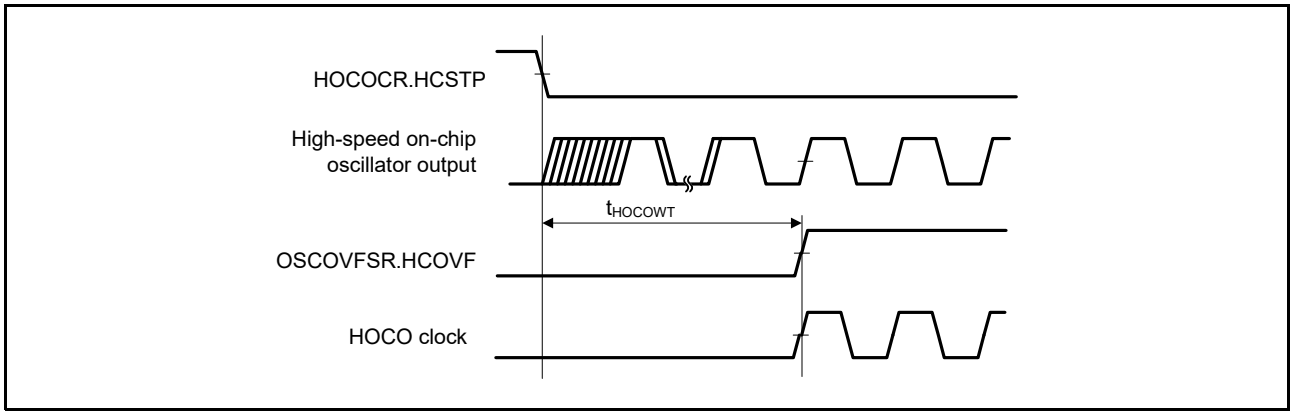


Figure 2.9 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

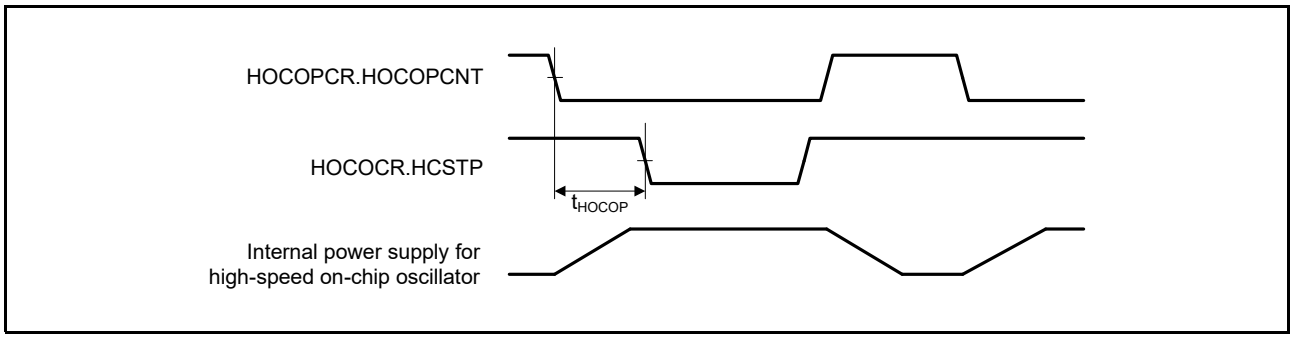


Figure 2.10 High-Speed On-Chip Oscillator Power Supply Control Timing

Table 2.22 PLL Clock Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL clock oscillation stabilization wait time	t_{PLLWT}	—	259	320	µs	Figure 2.11

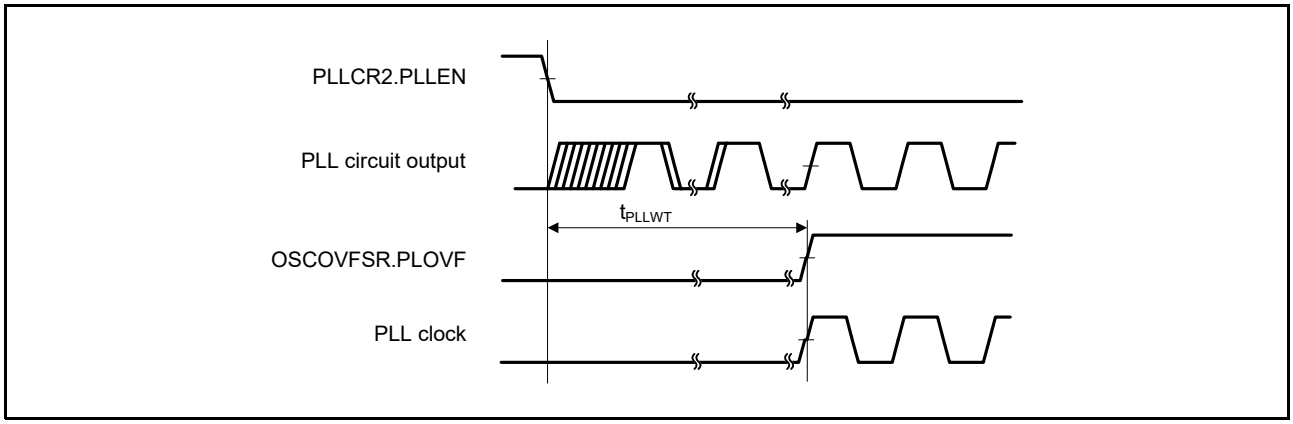


Figure 2.11 PLL Clock Oscillation Start Timing

2.4.3 Timing of Recovery from Low Power Consumption Modes

Table 2.23 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time after cancellation of software standby mode*1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	{(MSTS[7:0] bits × 32) + 76} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{MAIN}	µs	Figure 2.12
		Main clock oscillator and PLL circuit operating	t_{SBYPC}			{(MSTS[7:0] bits × 32) + 138} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}			352	100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}		
		Main clock oscillator and PLL circuit operating	t_{SBYPE}			639	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}			454	100 + 7 / f_{ICLK} + 2n / f_{HOCO}		
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}			741	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}			338	100 + 7 / f_{ICLK} + 2n / f_{LOCO}		

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when $f_{ICLK} : f_{FCLK}$ = 1 : 1, 2 : 1, or 4 : 1.

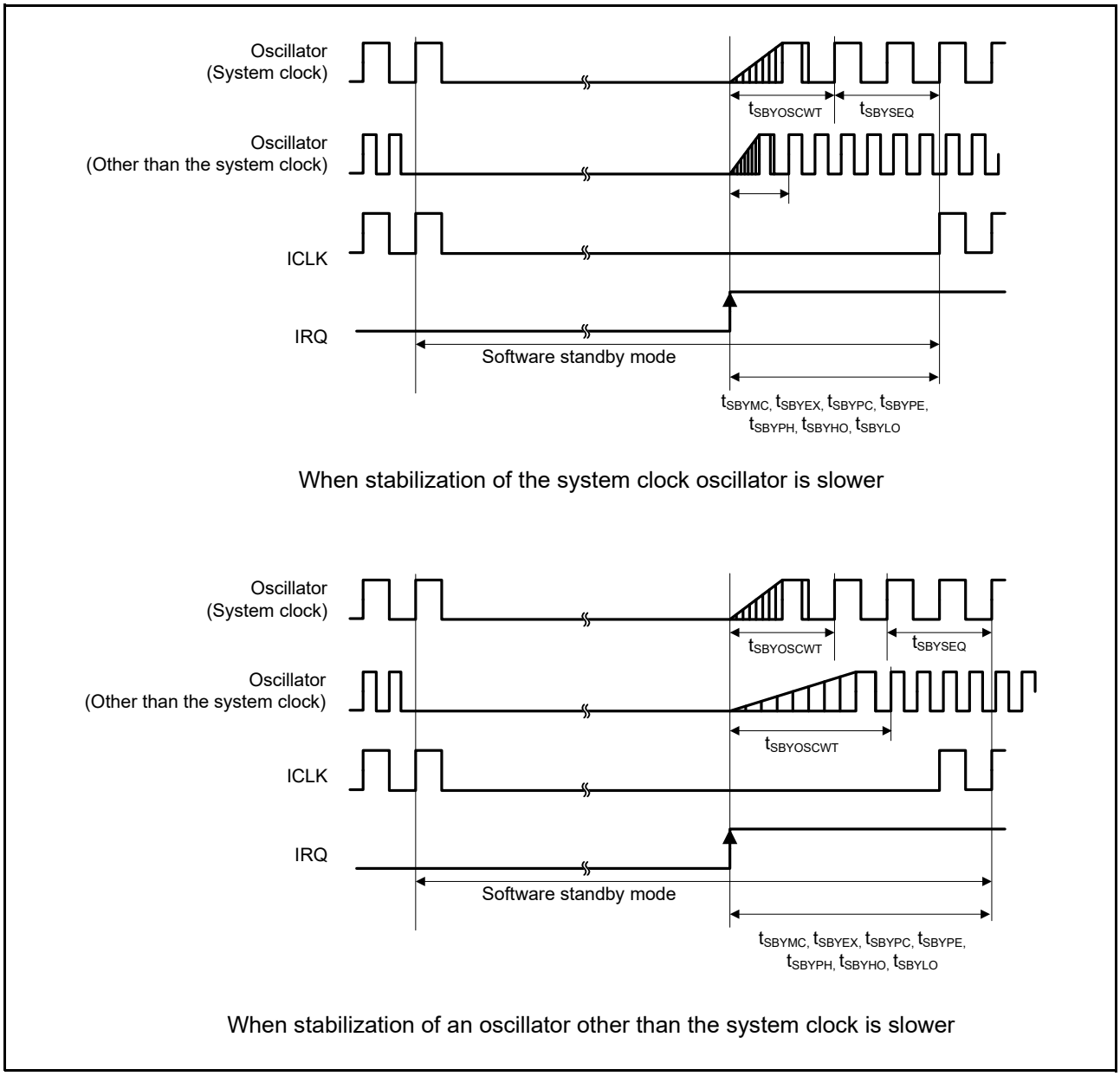


Figure 2.12 Software Standby Mode Cancellation Timing

Table 2.24 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 2.13
Wait time after cancellation of deep software standby mode	t_{DSBYWT}	31	—	32	t_{Lcyc}	

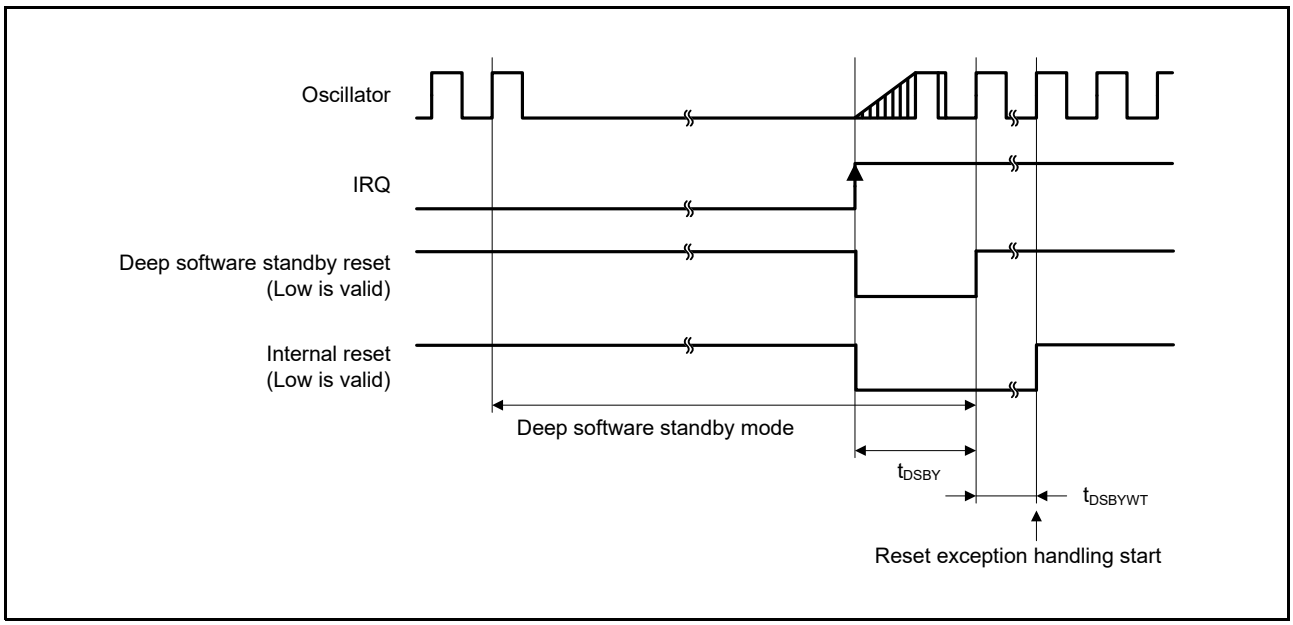


Figure 2.13 Deep Software Standby Mode Cancellation Timing

2.4.4 Control Signal Timing

Table 2.25 Control Signal Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	$2 \times t_{PBcyc} \leq 200$ ns, Figure 2.14
		$2 \times t_{PBcyc}$	—	—		$2 \times t_{PBcyc} > 200$ ns, Figure 2.14
IRQ pulse width	t_{IRQW}	200	—	—		$2 \times t_{PBcyc} \leq 200$ ns, Figure 2.15
		$2 \times t_{PBcyc}$	—	—		$2 \times t_{PBcyc} > 200$ ns, Figure 2.15

Note 1. t_{PBcyc}: PCLKB cycle

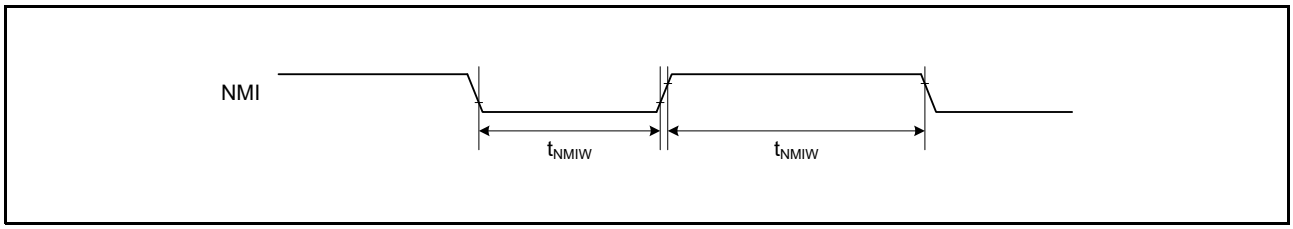


Figure 2.14 NMI Interrupt Input Timing

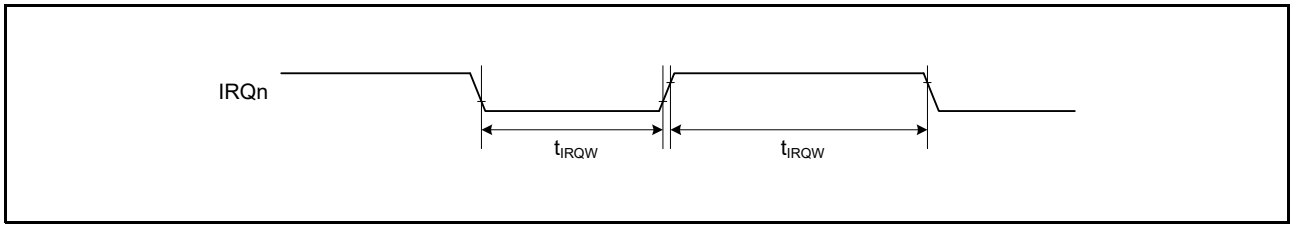


Figure 2.15 IRQ Interrupt Input Timing

2.4.5 Bus Timing

Table 2.26 Bus Timing (1)

Conditions: 4.5 V ≤ VCC ≤ 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	—	12.5	ns	Figure 2.16 to Figure 2.21
Byte control delay time	t_{BCD}	—	—	12.5		
CS# delay time	t_{CSD}	—	—	12.5		
ALE delay time	t_{ALED}	—	—	12.5		
RD# delay time	t_{RSD}	—	—	12.5		
Read data setup time	t_{RDS}	12.5	—	—		
Read data hold time	t_{RDH}	0	—	—		
WR# delay time	t_{WRD}	—	—	12.5		
Write data delay time	t_{WDD}	—	—	12.5		
Write data hold time	t_{WDH}	0	—	—		
WAIT# setup time	t_{WTS}	12.5	—	—		Figure 2.22
WAIT# hold time	t_{WTH}	0	—	—		

Table 2.27 Bus Timing (2)

Conditions: 2.7 V ≤ VCC < 4.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	—	25	ns	Figure 2.16 to Figure 2.21
Byte control delay time	t_{BCD}	—	—	25		
CS# delay time	t_{CSD}	—	—	25		
ALE delay time	t_{ALED}	—	—	25		
RD# delay time	t_{RSD}	—	—	25		
Read data setup time	t_{RDS}	25	—	—		
Read data hold time	t_{RDH}	0	—	—		
WR# delay time	t_{WRD}	—	—	25		
Write data delay time	t_{WDD}	—	—	25		
Write data hold time	t_{WDH}	0	—	—		
WAIT# setup time	t_{WTS}	25	—	—		Figure 2.22
WAIT# hold time	t_{WTH}	0	—	—		

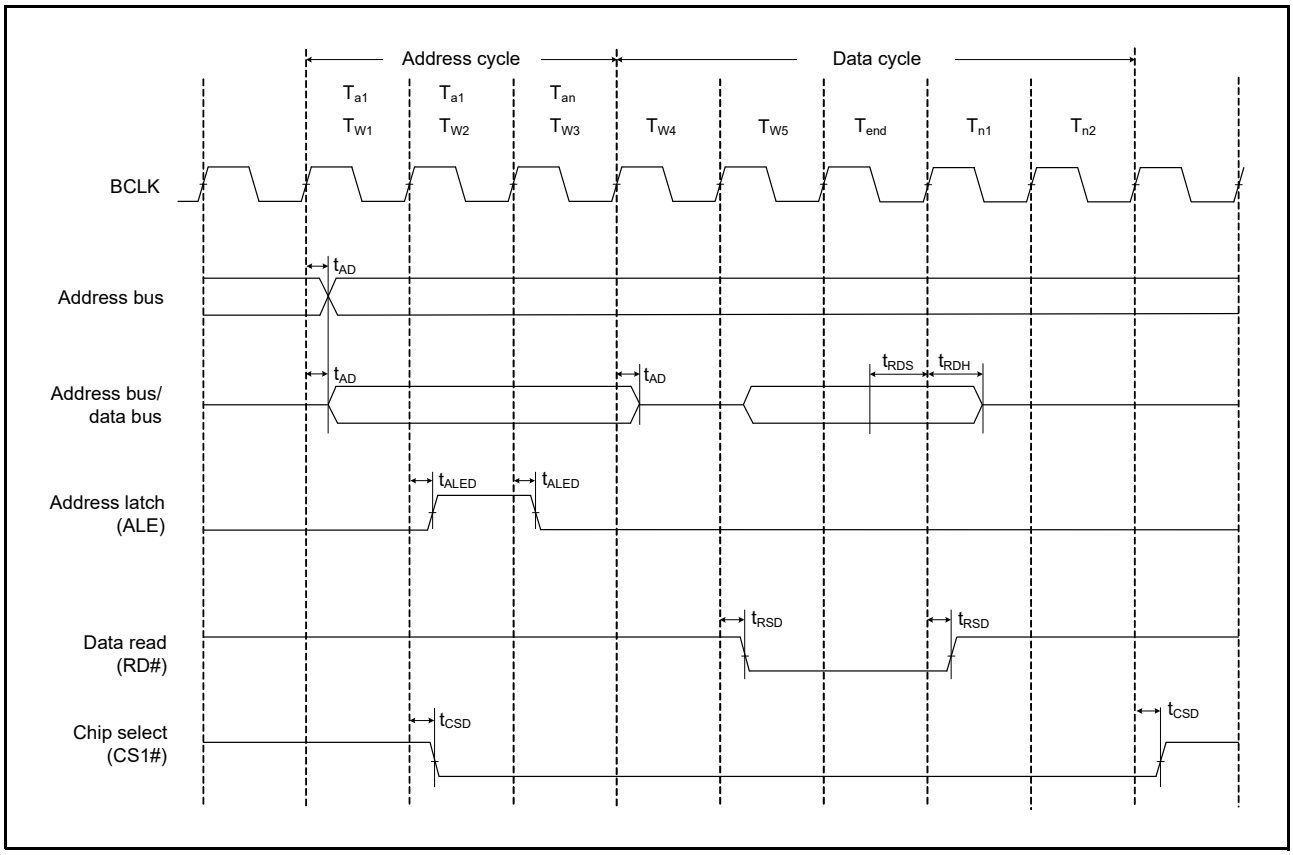


Figure 2.16 Address/Data Multiplexed Bus Read Access Timing

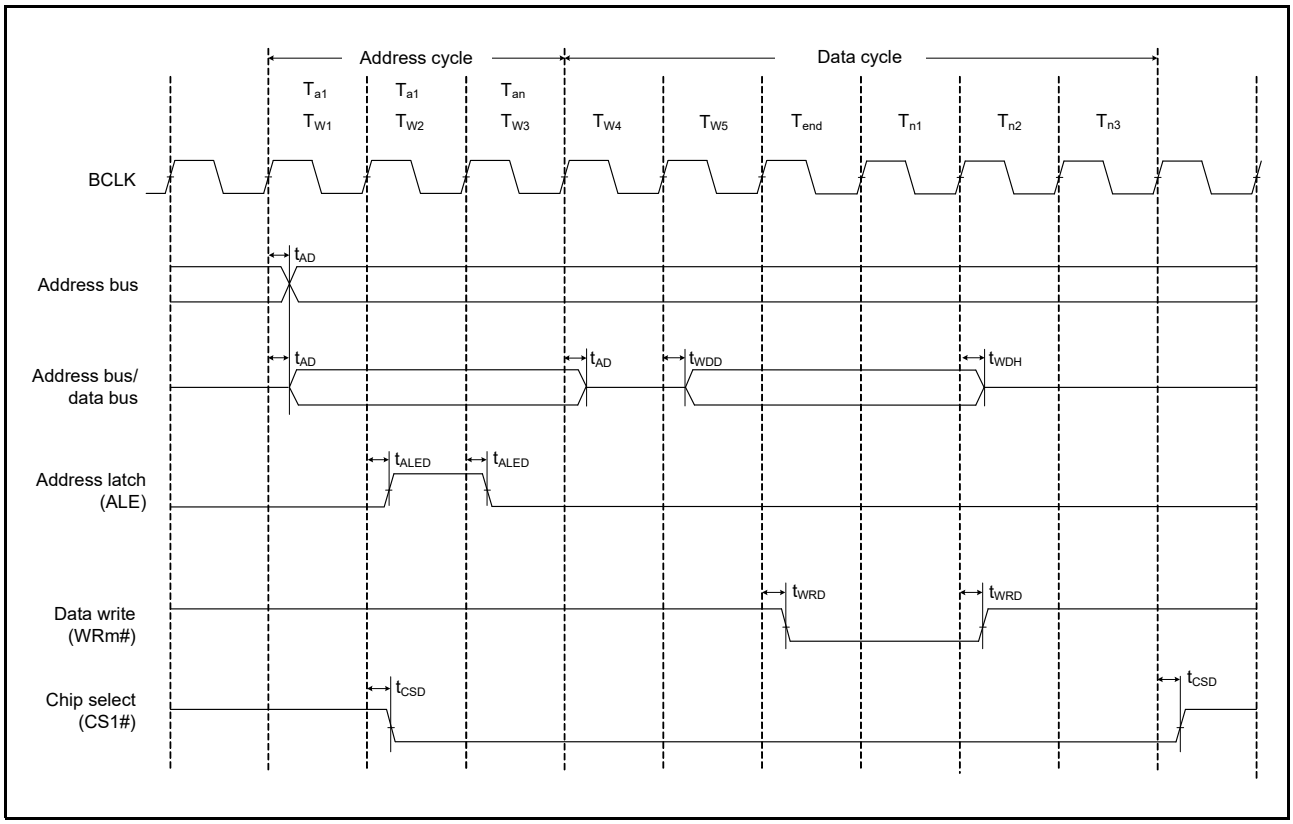


Figure 2.17 Address/Data Multiplexed Bus Write Access Timing

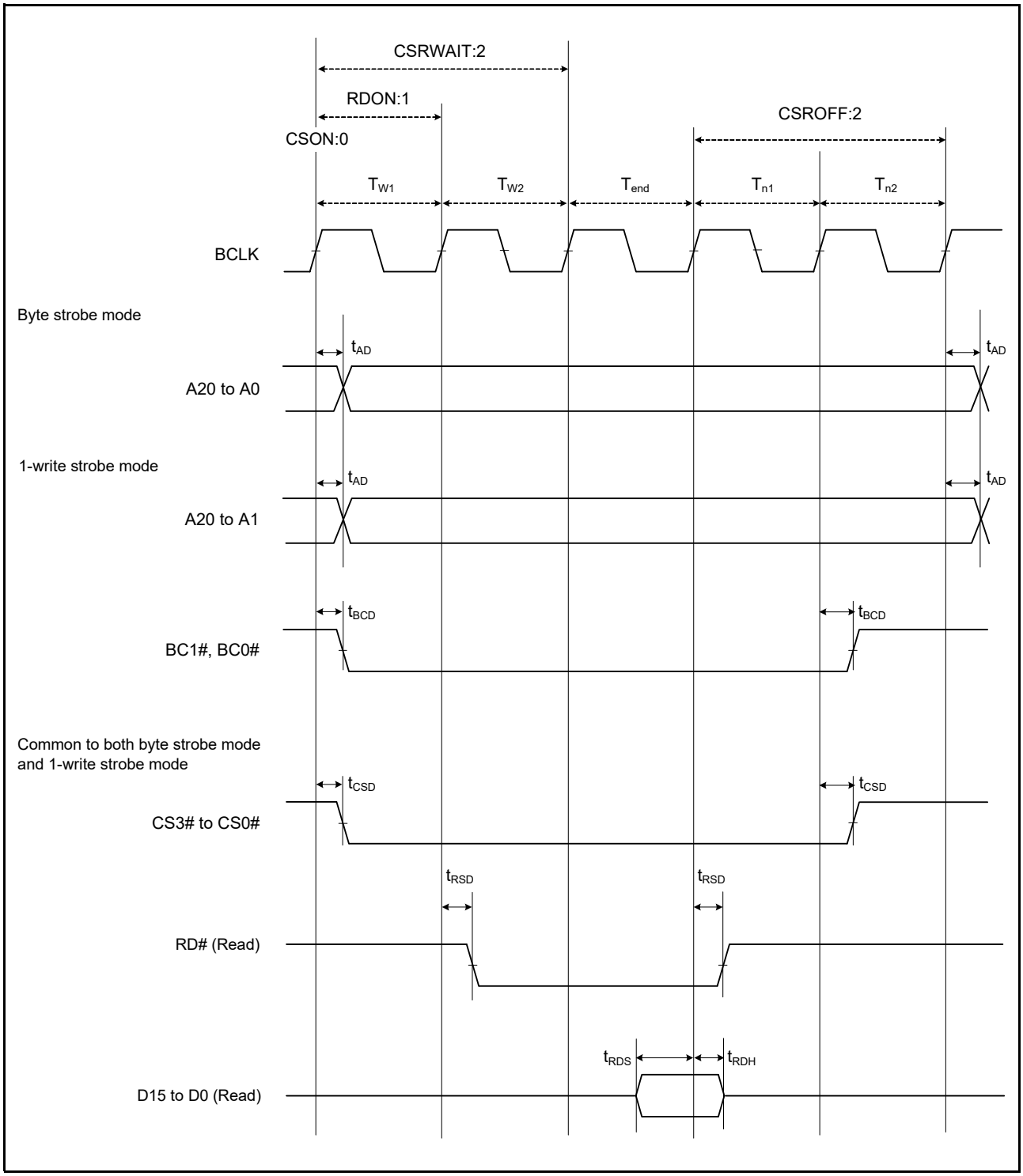
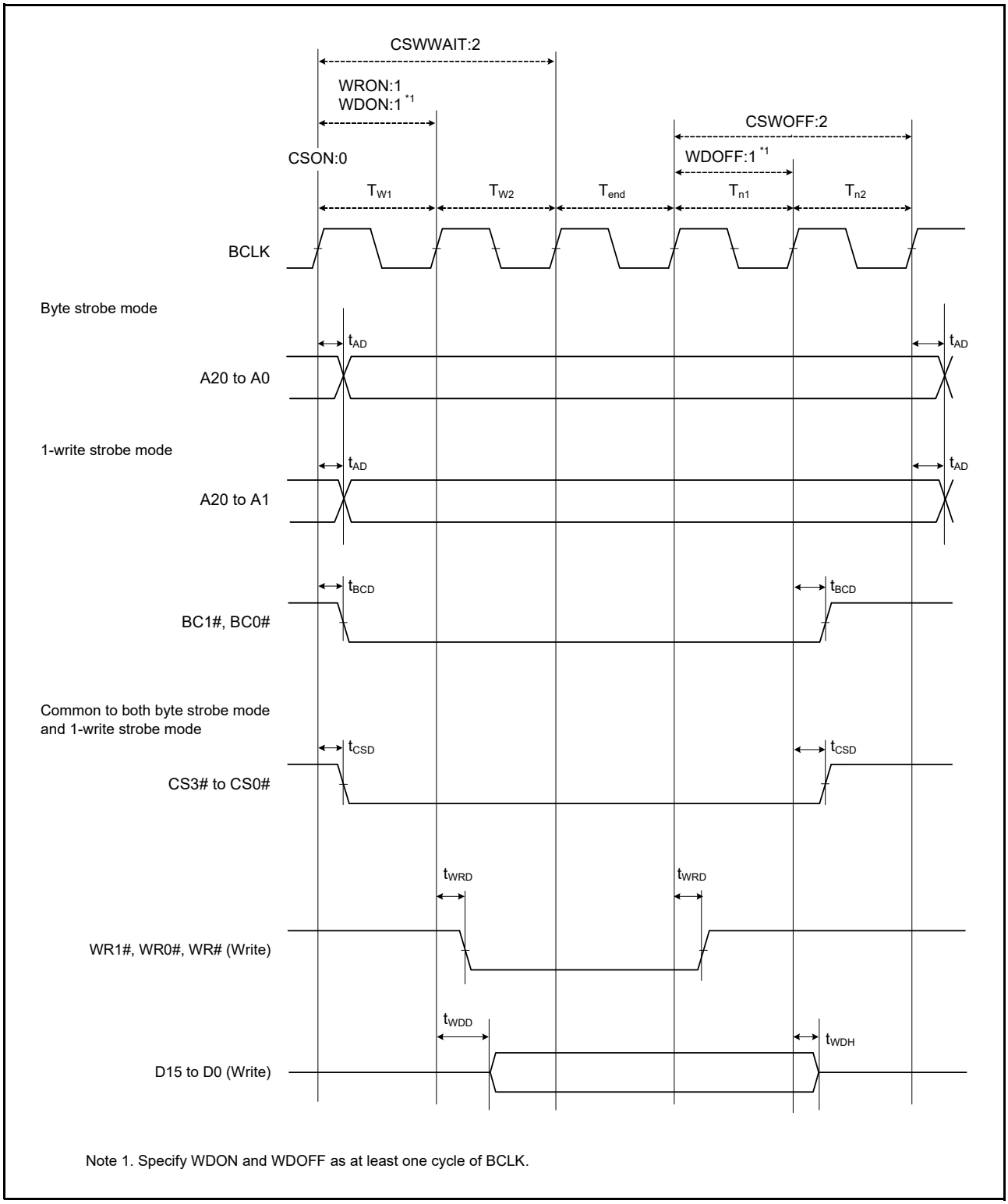


Figure 2.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Specify WDON and WDOFF as at least one cycle of BCLK.

Figure 2.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

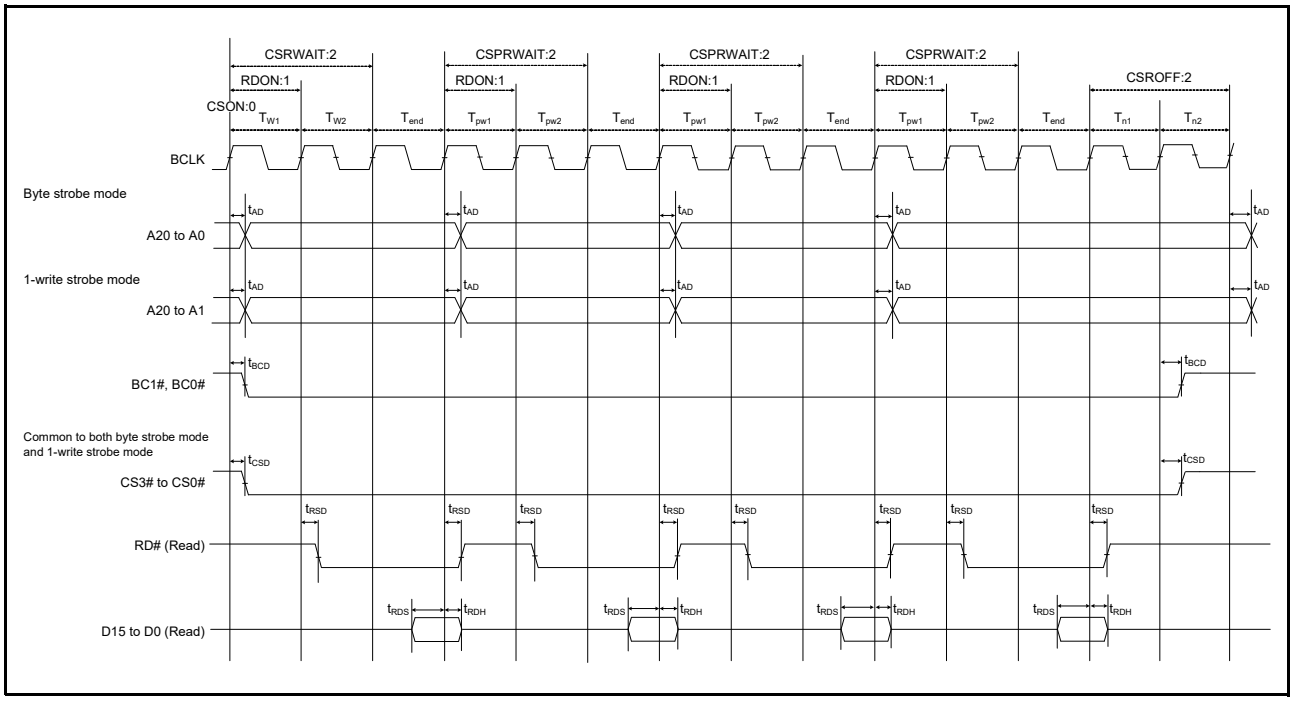


Figure 2.20 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

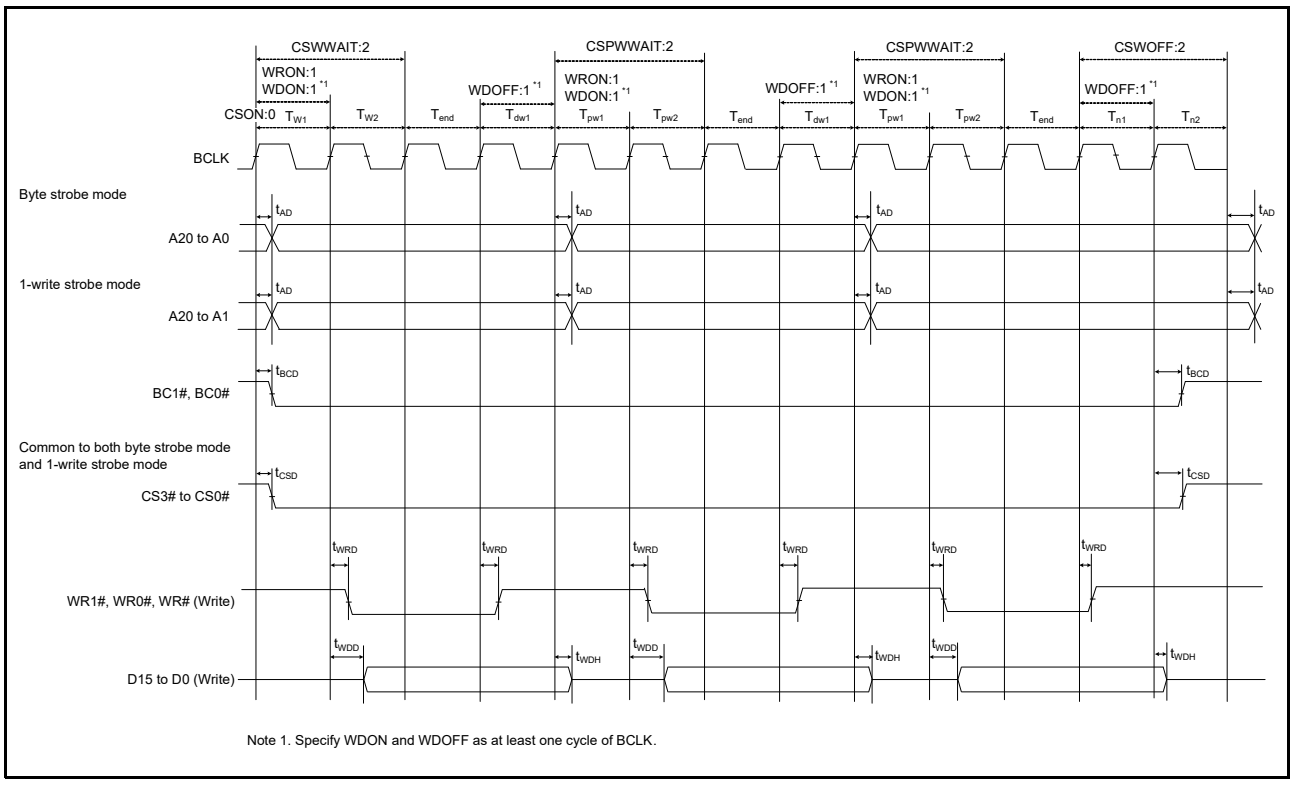


Figure 2.21 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

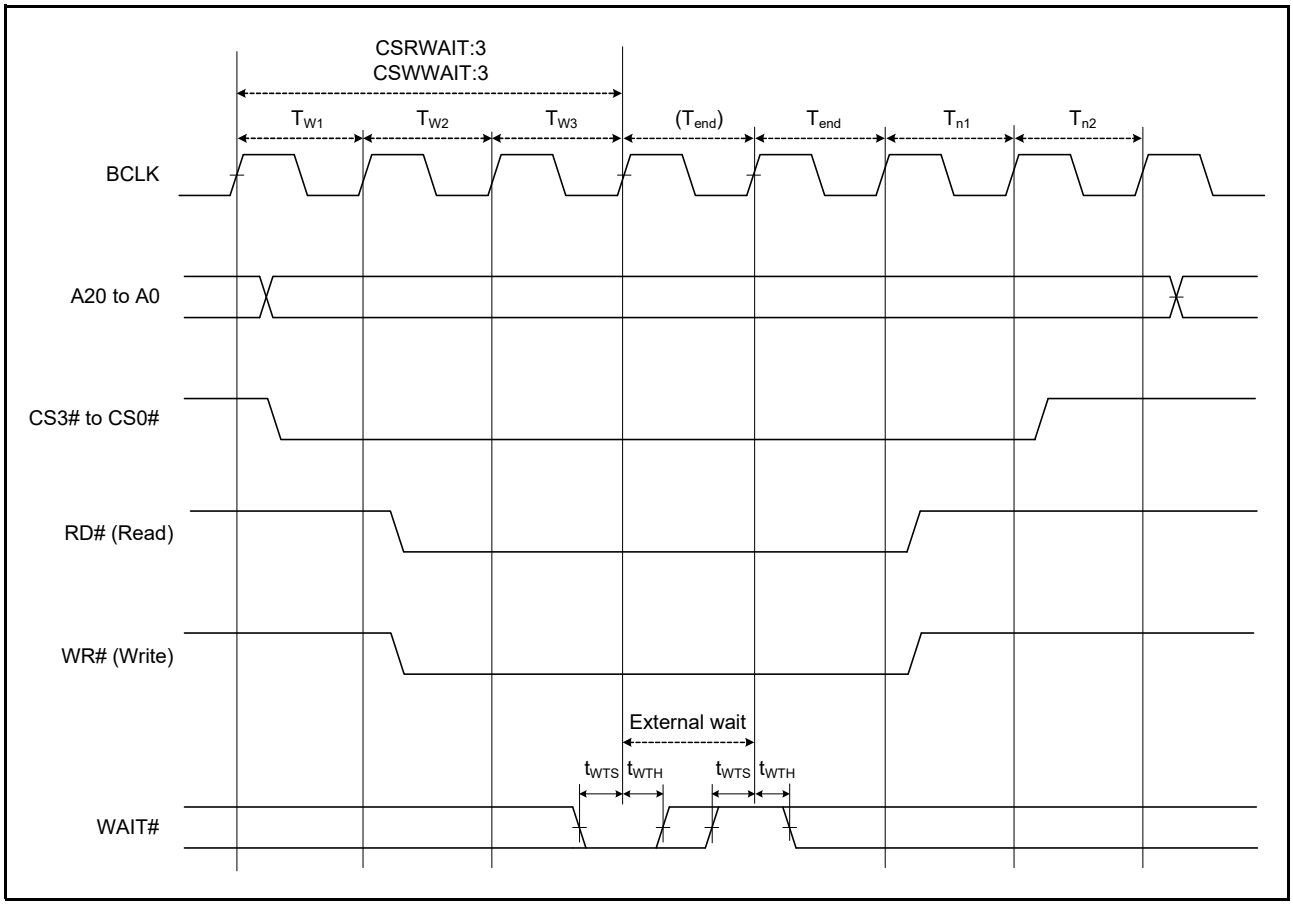


Figure 2.22 External Bus Timing/External Wait Control

2.4.6 Timing of On-Chip Peripheral Modules

2.4.6.1 I/O Port

Table 2.28 I/O Port Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.23

Note 1. t_{PBcyc}: PCLKB cycle

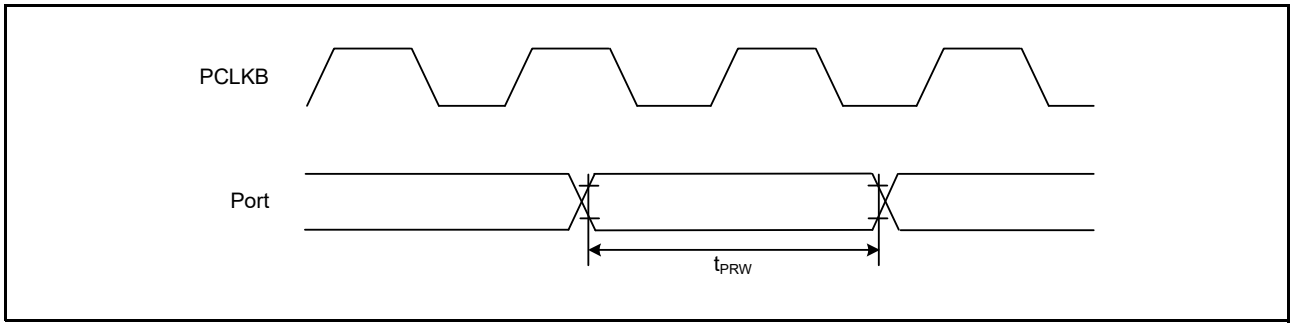


Figure 2.23 I/O Port Input Timing

2.4.6.2 TMR

Table 2.29 TMR Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 2.24
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

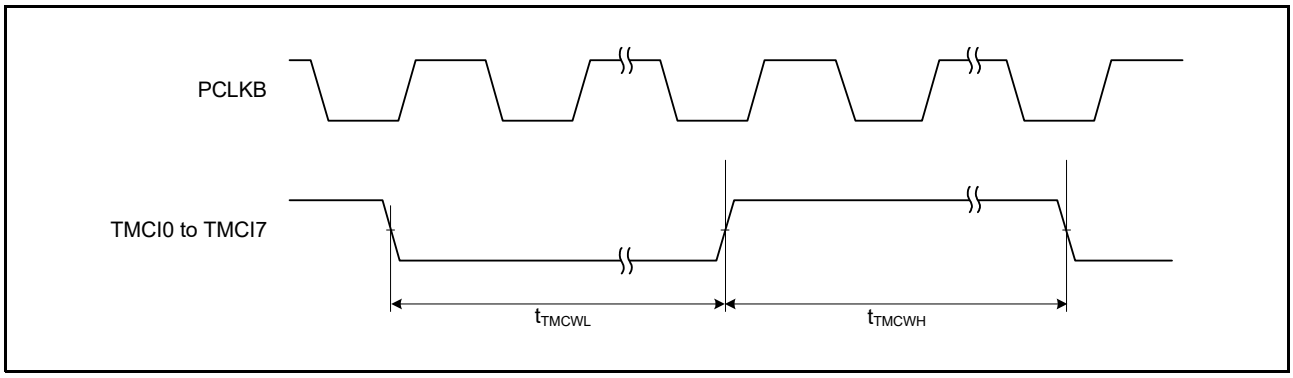


Figure 2.24 TMR Clock Input Timing

2.4.6.3 MTU

Table 2.30 MTU Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PCcyc}	Figure 2.25
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PCcyc}	Figure 2.26
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PCcyc}: PCLKC cycle

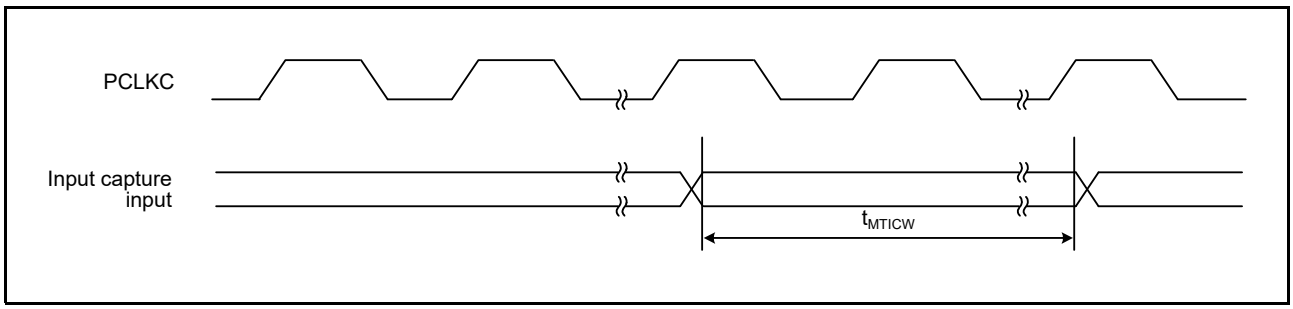


Figure 2.25 MTU Input Capture Input Timing

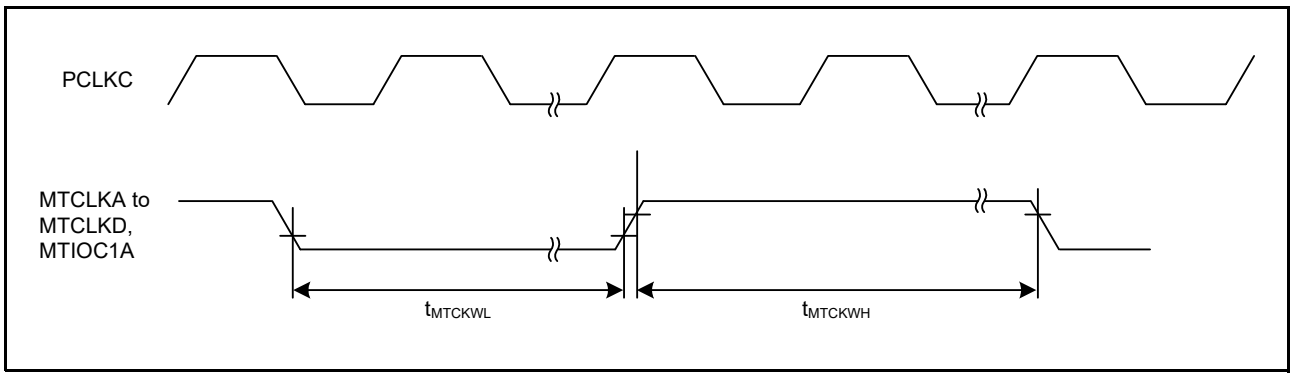


Figure 2.26 MTU Clock Input Timing

2.4.6.4 POE

Table 2.31 POE Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POE	POEn# input pulse width (n = 0, 4, and 8 to 14)		t_{POEW}	1.5	—	—	t_{PBcyc}	Figure 2.27
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	—	5 PCLKB + 0.24	µs	Figure 2.28 When detecting falling edges (ICSRm.POEnM[3:0] = 0000b (m = 1 to 5, 7 to 9, n = 0, 4, 8 to 14))
		Simultaneous conduction of output pins	t_{POEDO}	—	—	3 PCLKB + 0.2	µs	Figure 2.29
		Detection of comparator outputs	t_{POEDC}	—	—	5 PCLKB + 0.2	µs	Figure 2.30 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00b) and excludes the time for detection by comparator C.
		Register setting	t_{POEDS}	—	—	1 PCLKB + 0.2	µs	Figure 2.31 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	—	21	µs	Figure 2.32

Note 1. t_{PBcyc}: PCLKB cycle

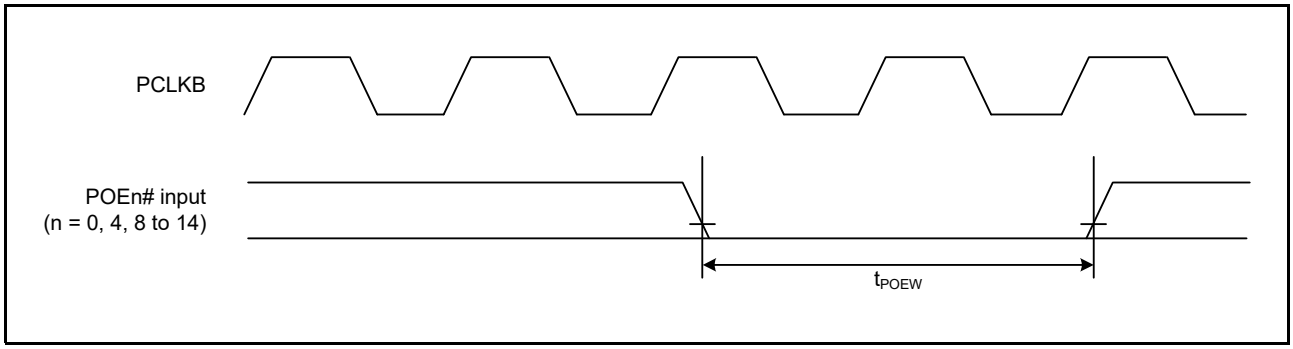


Figure 2.27 POE Input Timing

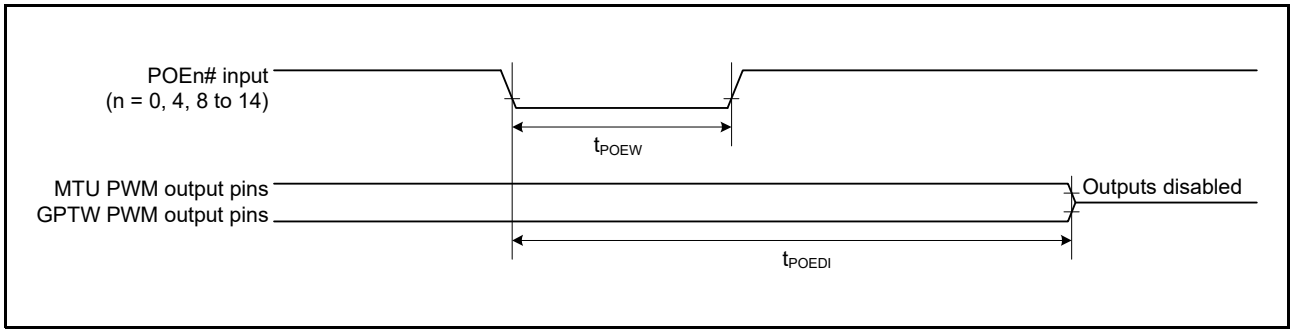
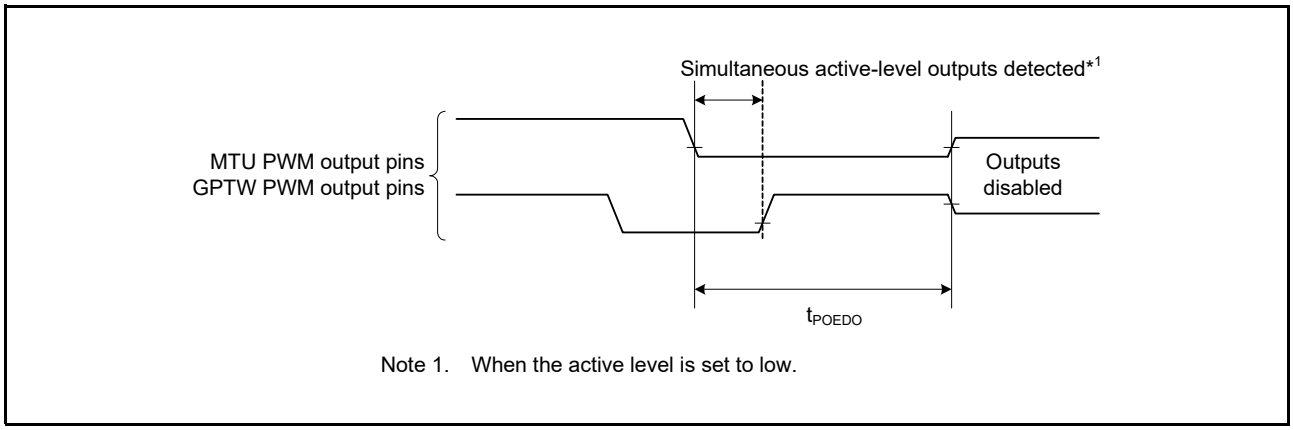


Figure 2.28 Output Disable Time for POE in Response to Transition of the POEn# Signal Level



Note 1. When the active level is set to low.

Figure 2.29 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

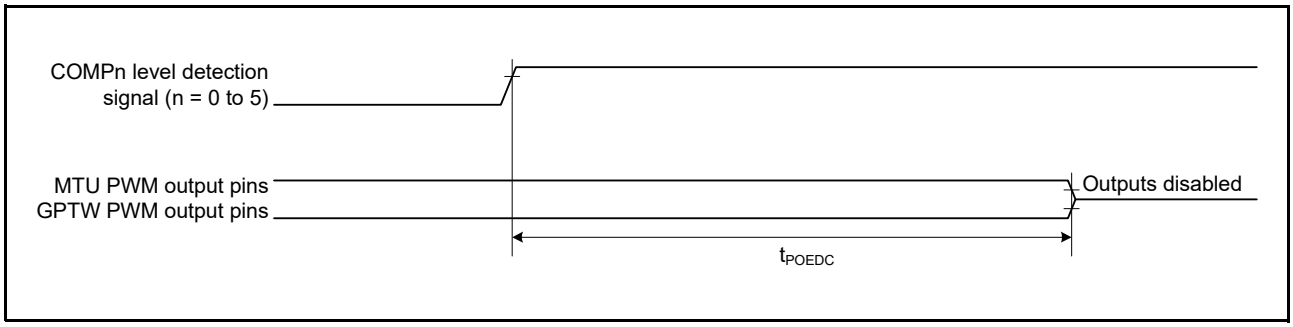


Figure 2.30 Output Disable Time for POE in Response to Detection of the Comparator Outputs

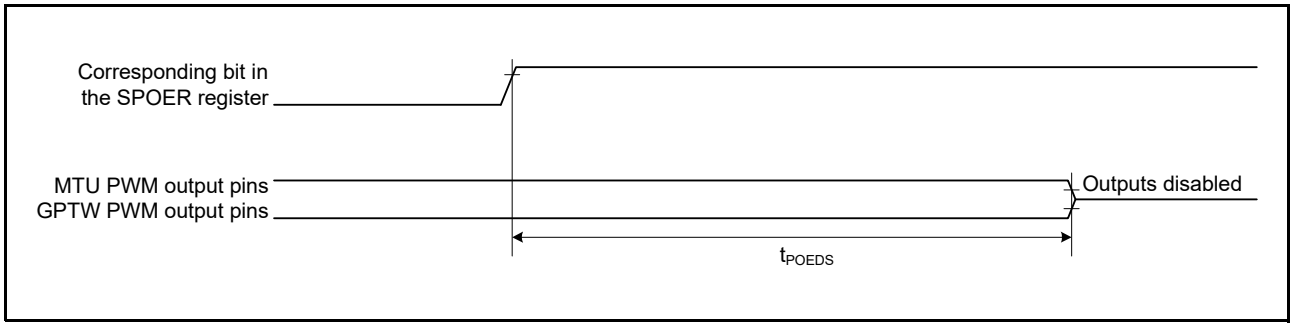


Figure 2.31 Output Disable Time for POE in Response to the Register Setting

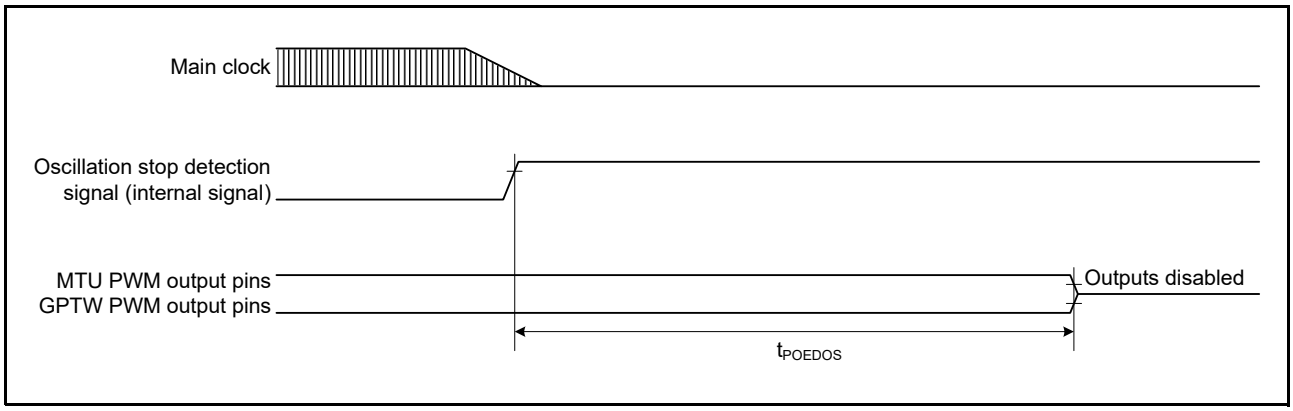


Figure 2.32 Output Disable Time for POE in Response to the Oscillation Stop Detection

2.4.6.5 POEG

Table 2.32 POE and POEG Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}	1.5	—	—	t_{PBcyc}	Figure 2.33
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	—	3 PCLKB + 0.34	µs	Figure 2.34 When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D))
		Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output)	t_{POEGDE}	—	—	0.5	µs	Figure 2.35
		Edge detection signal from a comparator	t_{POEGDC}	—	—	4 PCLKB + 0.5	µs	Figure 2.36 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00b) and excludes the time for detection by comparator C.
		Register setting	t_{POEGDS}	—	—	1 PCLKB + 0.3	µs	Figure 2.37 Time for access to the register is not included.
		Oscillation stop detection	$t_{POEGDOS}$	—	—	21	µs	Figure 2.38
		Input level detection of the GTETRGn pin (direct path)	$t_{POEGDDI}$	—	—	2 PCLKB + 1 PCLKC + 0.34	µs	Figure 2.39
		Level detection signal from a comparator	$t_{POEGDDC}$	—	—	3 PCLKB + 0.3	µs	Figure 2.40 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00b) and excludes the time for detection by comparator C.

Note 1. t_{PBcyc}: PCLKB cycle

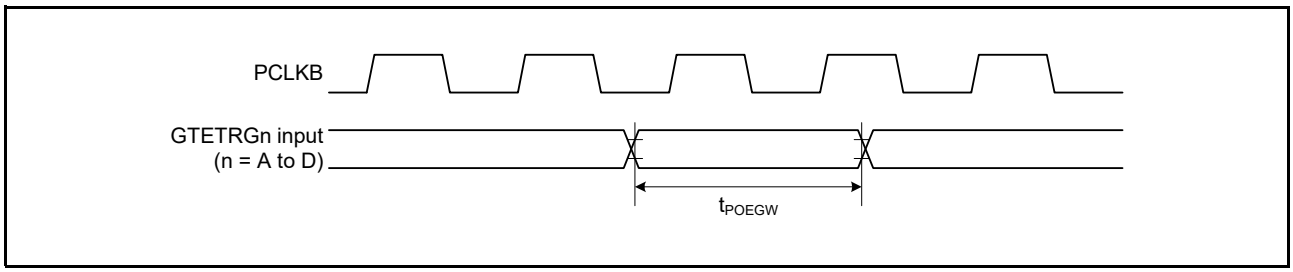


Figure 2.33 POEG Input Timing

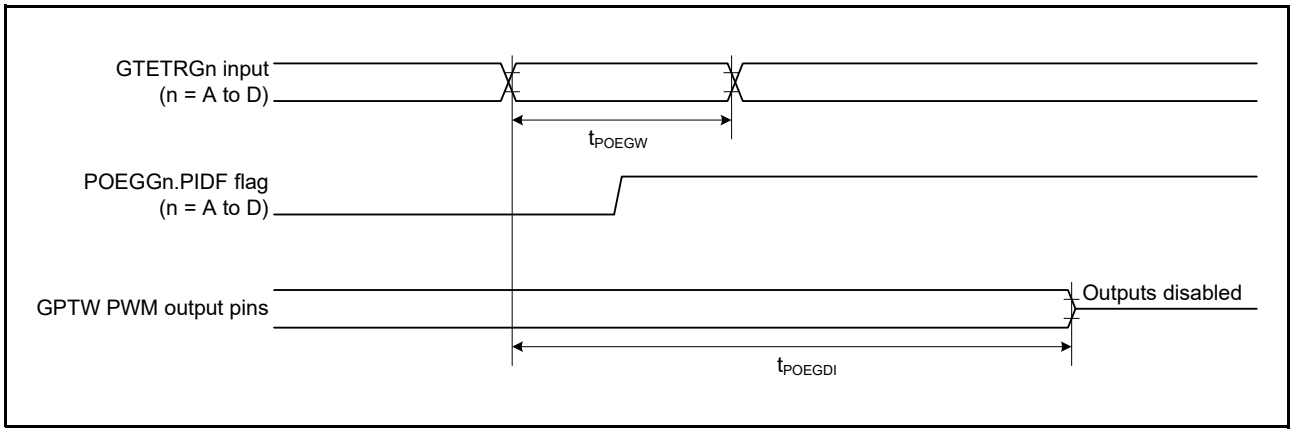
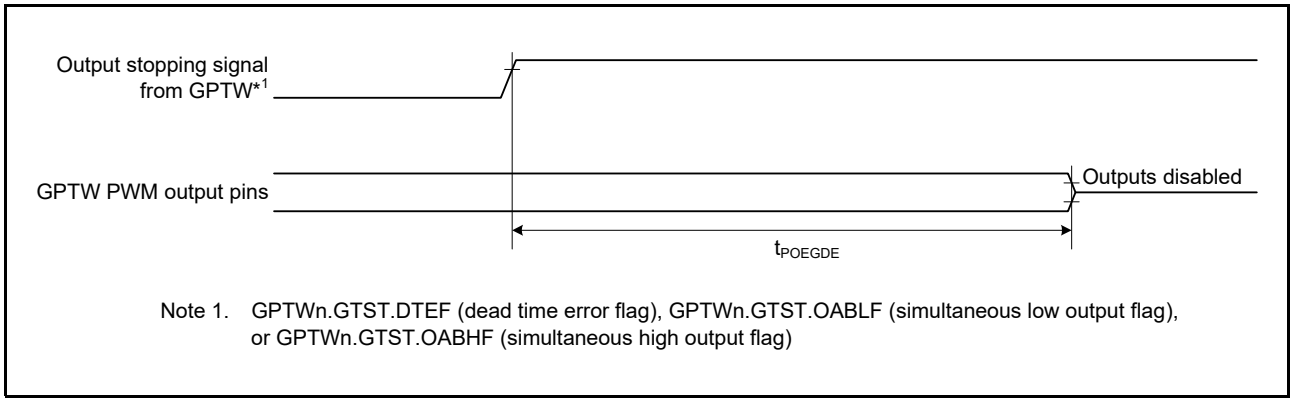


Figure 2.34 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin



Note 1. GPTWn.GTST.DTEF (dead time error flag), GPTWn.GTST.OABLF (simultaneous low output flag), or GPTWn.GTST.OABHF (simultaneous high output flag)

Figure 2.35 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPTW

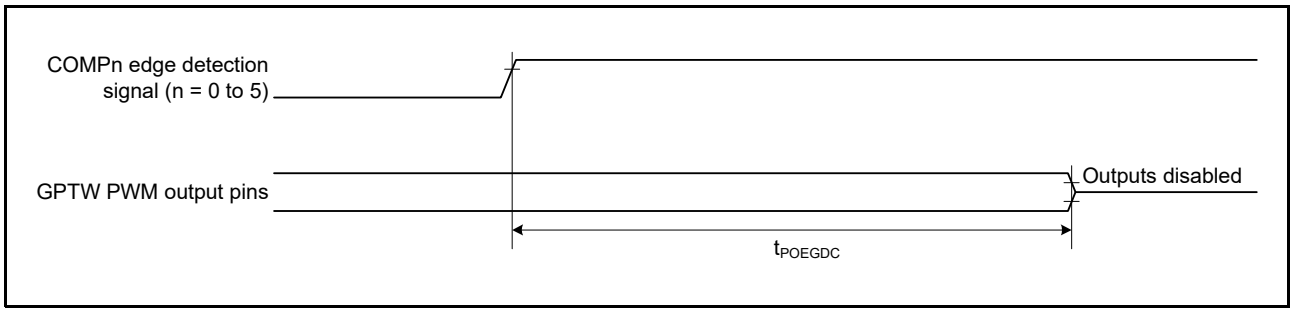


Figure 2.36 Output Disable Time for POEG in Response to Edge Detection Signal from a Comparator

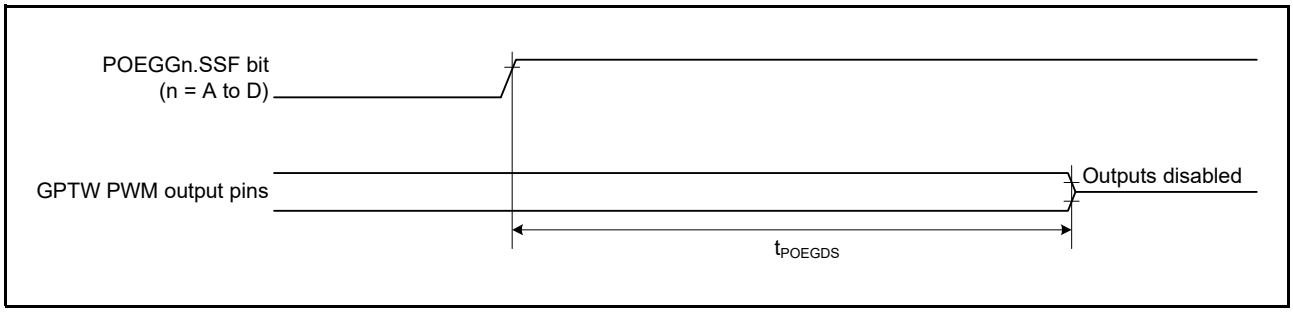


Figure 2.37 Output Disable Time for POEG in Response to the Register Setting

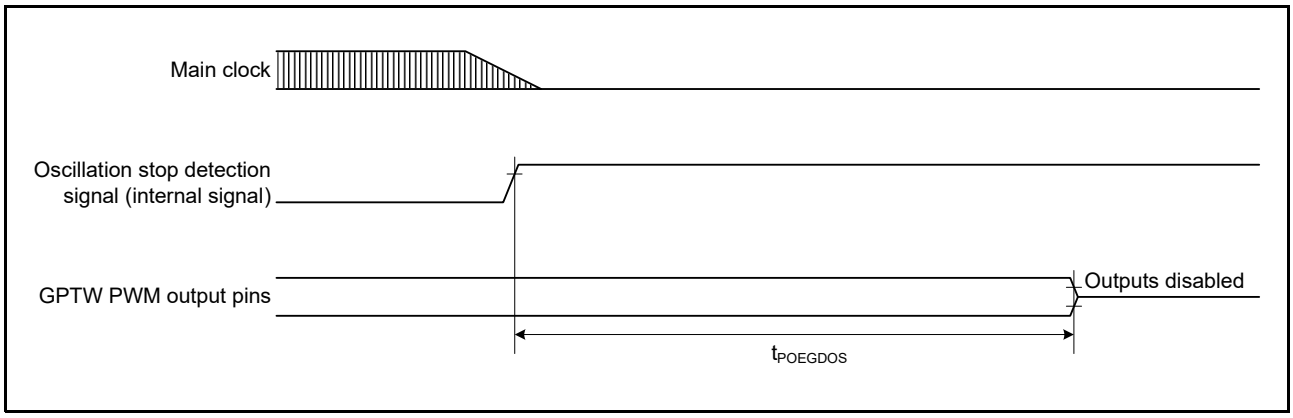


Figure 2.38 Output Disable Time of POEG in Response to the Oscillation Stop Detection

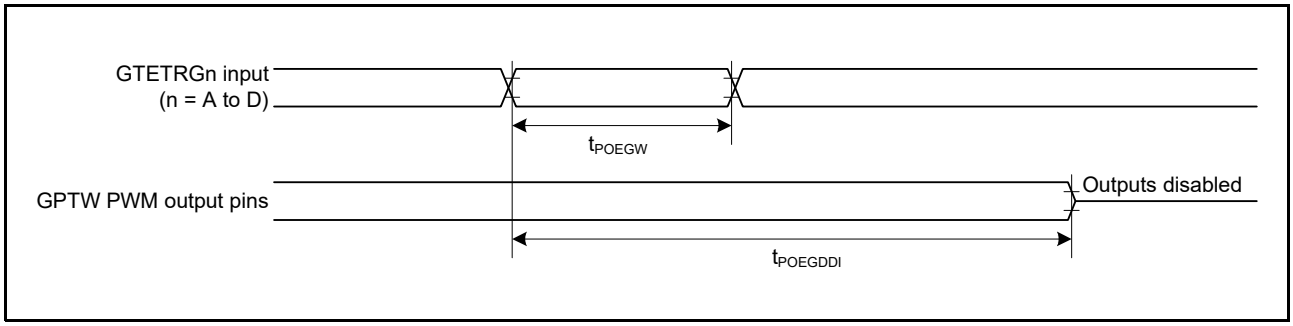


Figure 2.39 Output Disable Time for POEG in Direct Response to the Input Level Detection of the GTETRGn pin

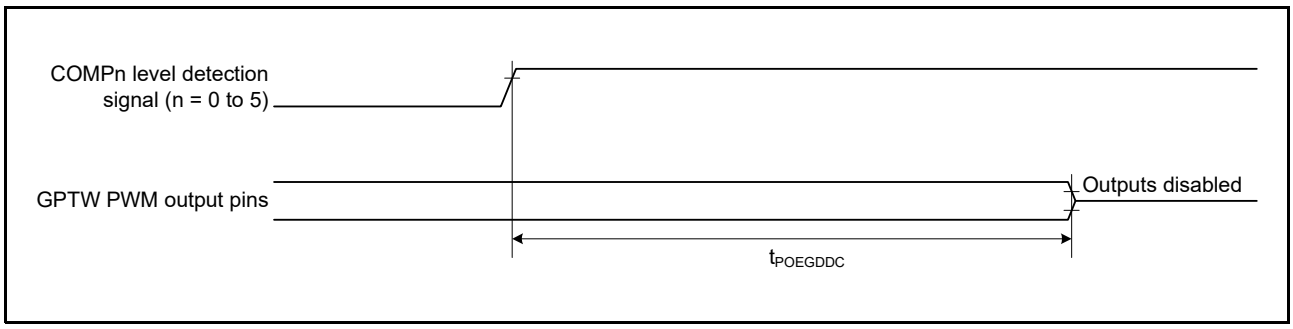


Figure 2.40 Output Disable Time for POEG in Response to Level Detection Signal from a Comparator

2.4.6.6 GPTW

Table 2.33 GPTW Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item			Symbol	Min.	Max.	Unit*1, *2	Test Conditions
GPTW	Input capture input pulse width	Single-edge setting	t_{GTICW}	1.5	—	t_{PCcyc}	Figure 2.41
		Both-edge setting		2.5	—		
	External trigger input pulse width	Single-edge setting	t_{GTEW}	1.5	—	t_{PBcyc}	Figure 2.42
		Both-edge setting		2.5	—		
	Timer clock pulse width		t_{GTCKWH}	1.5	—	t_{PBcyc}	Figure 2.43
			t_{GTCKWL}				

Note 1. t_{PCcyc}: PCLKC cycle
Note 2. t_{PBcyc}: PCLKB cycle

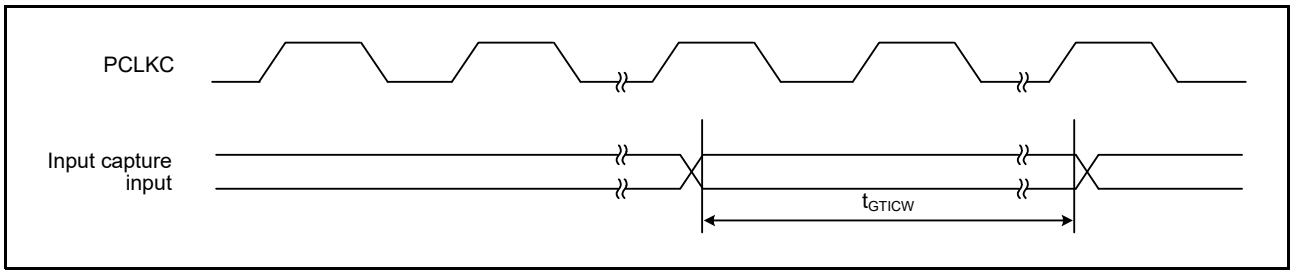


Figure 2.41 GPTW Input Capture Input Timing

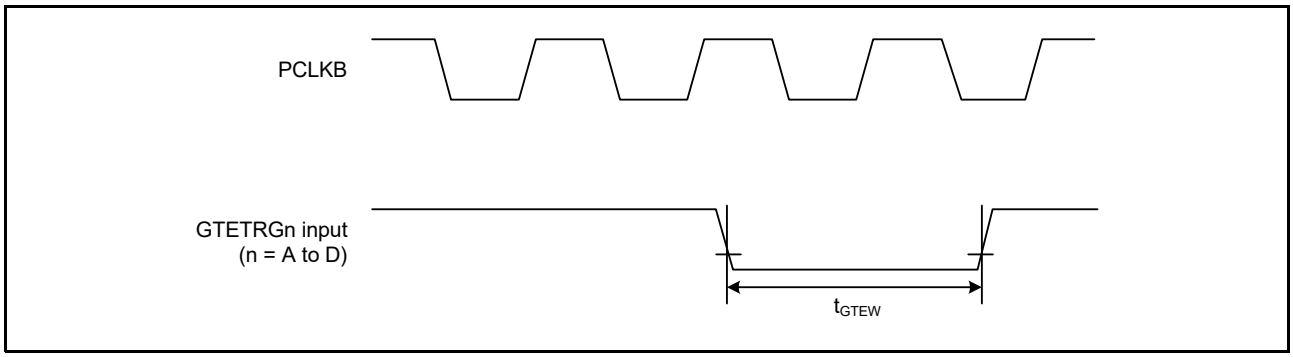


Figure 2.42 GPTW External Trigger Input Timing

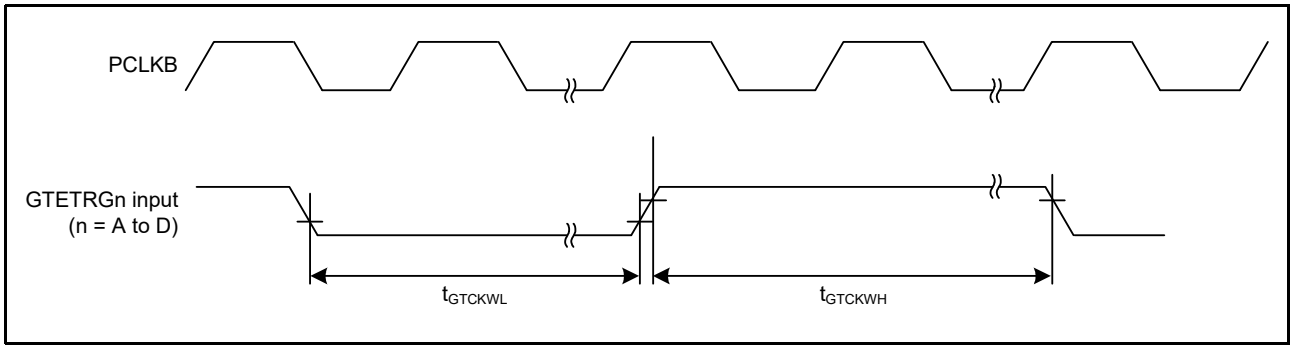


Figure 2.43 GPTW Clock Input Timing

2.4.6.7 A/D Converter Trigger

Table 2.34 A/D Converter Trigger Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 2.44

Note 1. t_{PBcyc}: PCLKB cycle

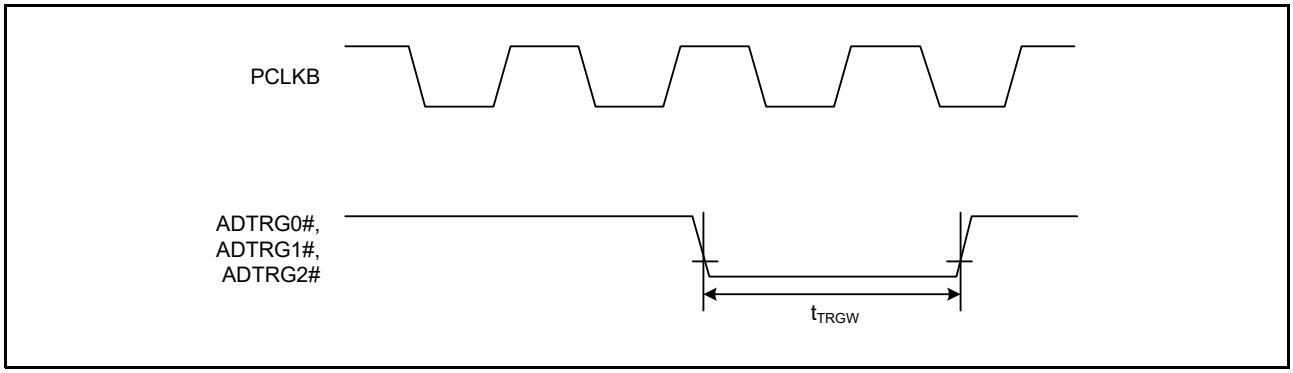


Figure 2.44 A/D Converter Trigger Input Timing

2.4.6.8 CAC

Table 2.35 CAC Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item*1, *2			Symbol	Min.*1, *2	Max.	Unit	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{cac}$	t_{CACREF}	4.5 t_{cac} + 3 t_{PBcyc}	—	ns	
		$t_{PBcyc} > t_{cac}$		5 t_{cac} + 6.5 t_{PBcyc}	—		

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{cac}: CAC count clock source cycle

2.4.6.9 SCI

Table 2.36 SCIj, SCIh, and SCIi Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item			Symbol	Min.	Max.	Unit*1	Test Conditions	
SCIj, SCIh	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PBcyc}	Figure 2.45	
		Clock synchronous		6	—			
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Input clock rise time		t_{SCKr}	—	5	ns		
	Input clock fall time		t_{SCKf}	—	5	ns		
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{PBcyc}		
		Clock synchronous		4	—			
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Output clock rise time		t_{SCKr}	—	5	ns		
	Output clock fall time		t_{SCKf}	—	5	ns		
	Transmit data delay time	Clock synchronous	t_{TXD}	—	28	ns	VCC ≥ 4.5 V	Figure 2.46
				—	33		VCC < 4.5 V	
	Receive data setup time	Clock synchronous	t_{RXS}	15	—	ns	VCC ≥ 4.5 V	Figure 2.46
				20	—		VCC < 4.5 V	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	Figure 2.46	
SCIi	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 2.45	
		Clock synchronous		6	—			
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Input clock rise time		t_{SCKr}	—	5	ns		
	Input clock fall time		t_{SCKf}	—	5	ns		
	Output clock cycle	Asynchronous*2	t_{Scyc}	6	—	t_{PAcyc}		
		Clock synchronous		4	—			
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Output clock rise time		t_{SCKr}	—	5	ns		
	Output clock fall time		t_{SCKf}	—	5	ns		
	Transmit data delay time	Master	t_{TXD}	—	15	ns	VCC ≥ 4.5 V	Figure 2.46
		Slave		—	28			
		Master		—	20		VCC < 4.5 V	
		Slave		—	33			
	Receive data setup time	Clock synchronous	t_{RXS}	15	—	ns	VCC ≥ 4.5 V	Figure 2.46
				20	—		VCC < 4.5 V	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	Figure 2.46	

Note 1. t_{PBcyc}: PCLKB cycle; t_{PAcyc}: PCLKA cycle
Note 2. When the SEMR.ABCS and SEMR.BGDM bits are set to 1

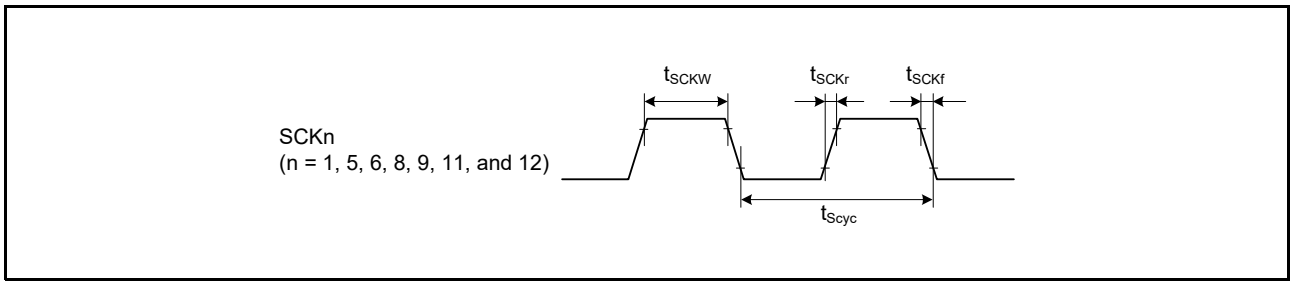


Figure 2.45 SCK Clock Input Timing

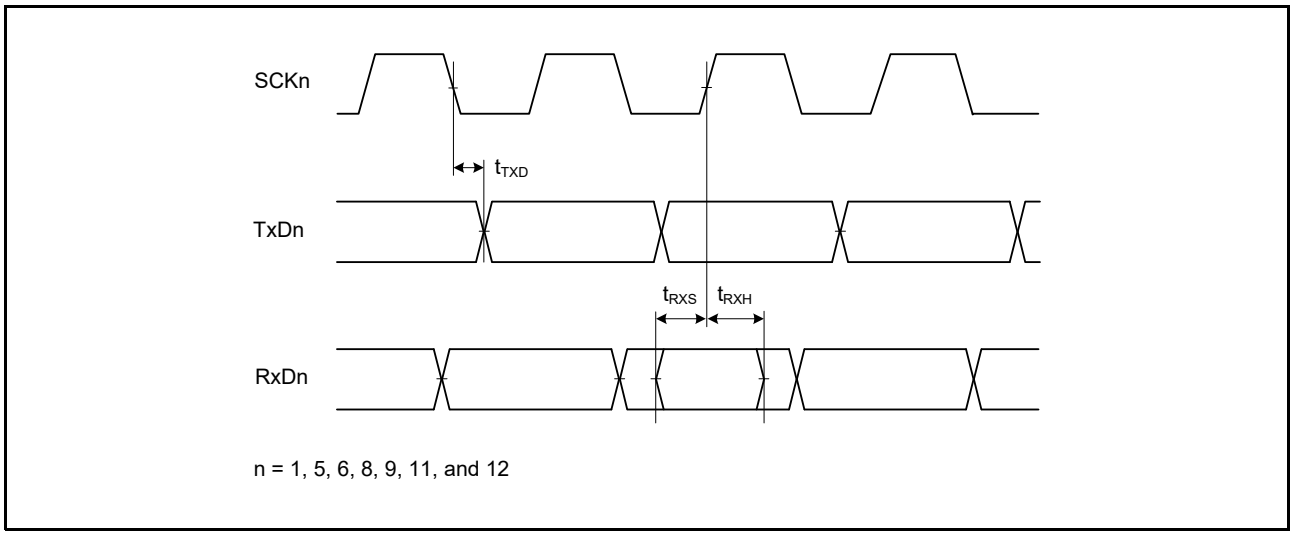


Figure 2.46 SCI Input/Output Timing: Clock Synchronous Mode

Table 2.37 Simple IIC Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item		Symbol*1	Min.	Max.*2	Unit	Test Conditions
Simple IIC (Standard-mode)	SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.47
	SSDA input fall time	t_{Sf}	—	300		
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}		
	Data input setup time	t_{SDAS}	250	—		
	Data input hold time	t_{SDAH}	0	—		
	SSCL, SSDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SSDA input rise time	t_{Sr}	—	300	ns	
	SSDA input fall time	t_{Sf}	—	300		
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}		
	Data input setup time	t_{SDAS}	100	—		
	Data input hold time	t_{SDAH}	0	—		
	SSCL, SSDA capacitive load	C_b	—	400	pF	

Note 1. Cb is the total capacitance of the bus lines.
Note 2. t_{Pcyc}: For SCI11, this is the period of PCLKA, and for SCI1, 5, 6, 8, 9, and 12, this is the period of PCLKB.

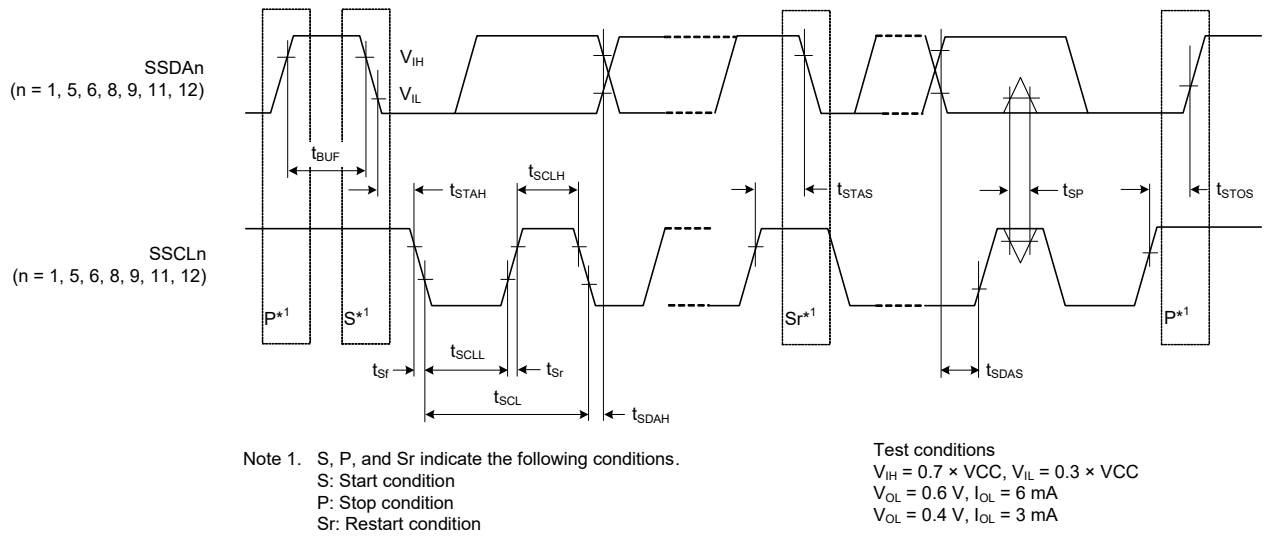


Figure 2.47 Simple IIC Bus Interface Input/Output Timing

Table 2.38 Simple SPI Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI (SCI11)	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{PAcyc}	Figure 2.48
	SCK clock cycle input (slave)		8	—		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 2.49 to Figure 2.52
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	7	t_{PAcyc}	Figure 2.51, Figure 2.52
	Slave output release time	t_{REL}	—	7	t_{PAcyc}	
Simple SPI (SCI1, SCI5, SCI6, SCI8, SCI9, SCI12)	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{PBcyc}	Figure 2.48
	SCK clock cycle input (slave)		8	—		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 2.49 to Figure 2.52
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	7	t_{PBcyc}	Figure 2.51, Figure 2.52
	Slave output release time	t_{REL}	—	7	t_{PBcyc}	

Note 1. t_{PAcyc}: PCLKA cycle, t_{PBcyc}: PCLKB cycle

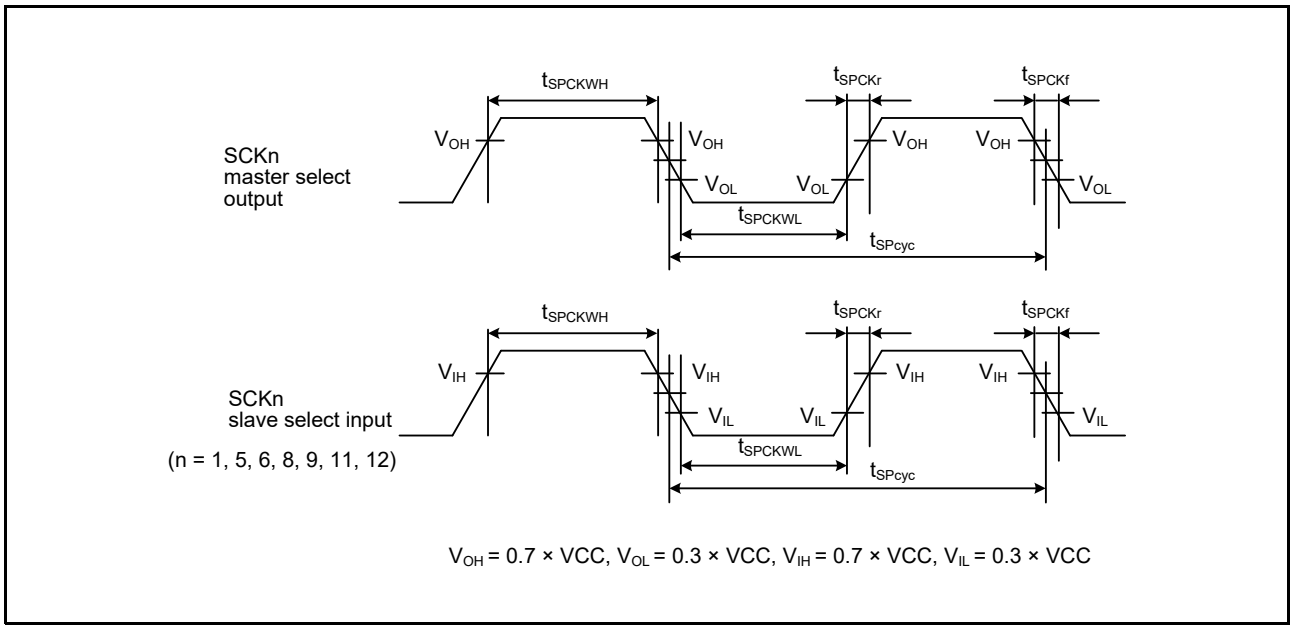


Figure 2.48 Simple SPI Clock Timing

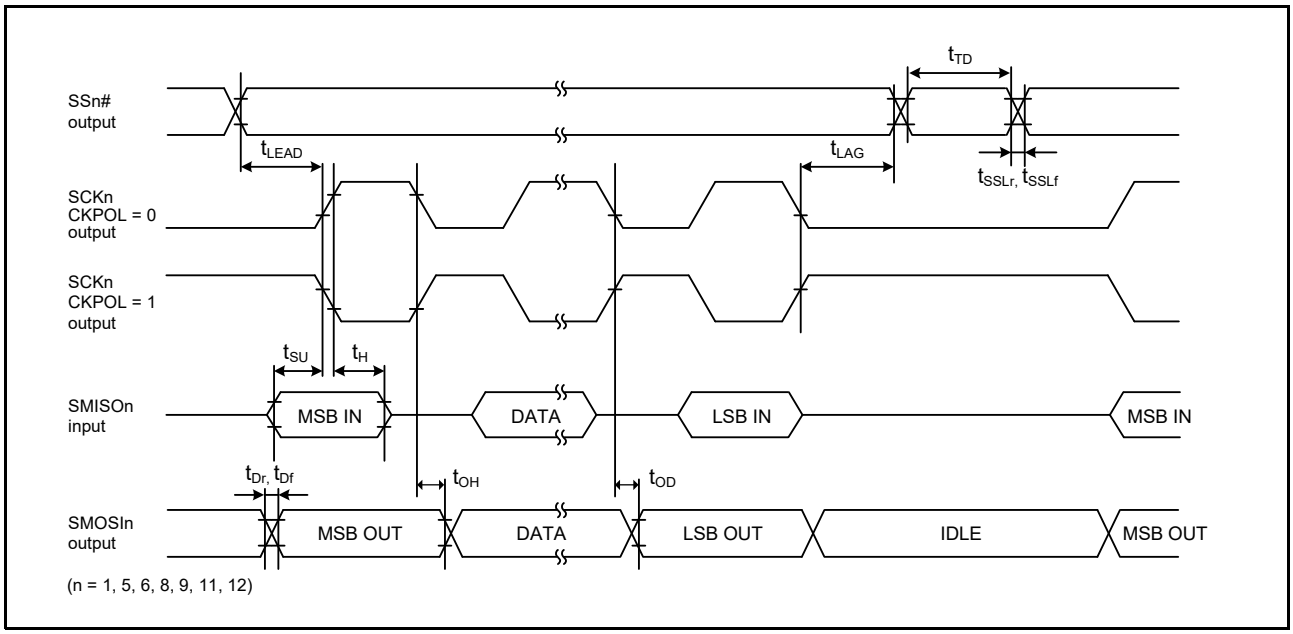


Figure 2.49 Simple SPI Timing (Master, CKPH = 1)

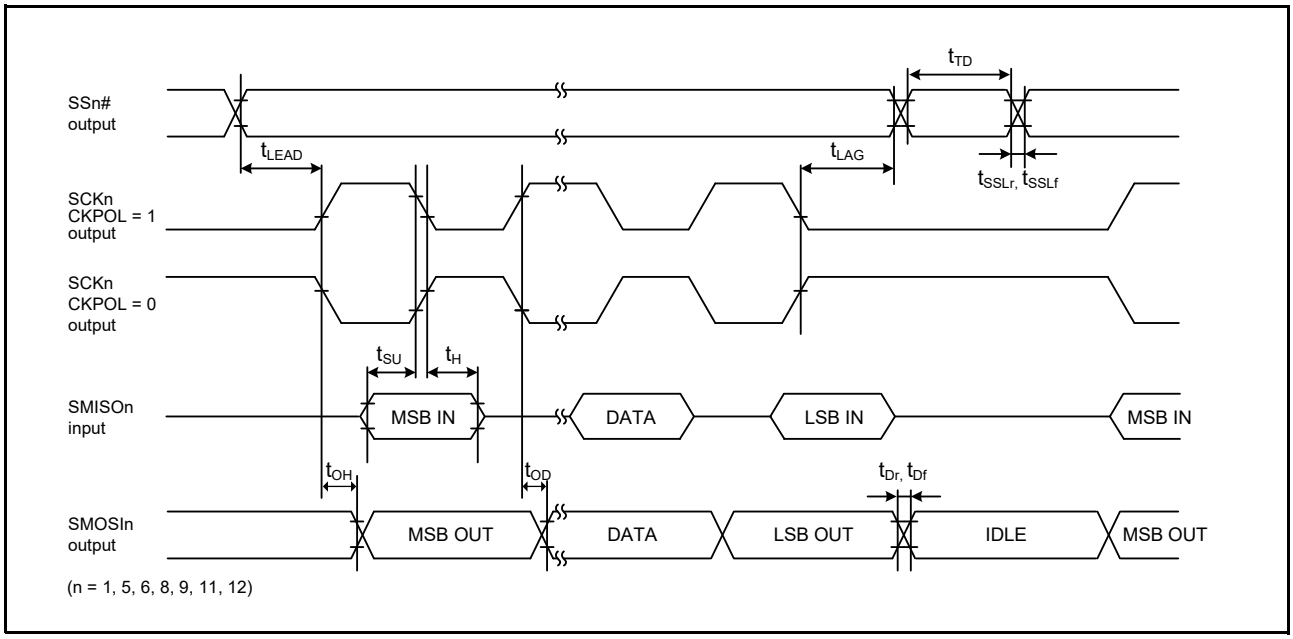


Figure 2.50 Simple SPI Timing (Master, CKPH = 0)

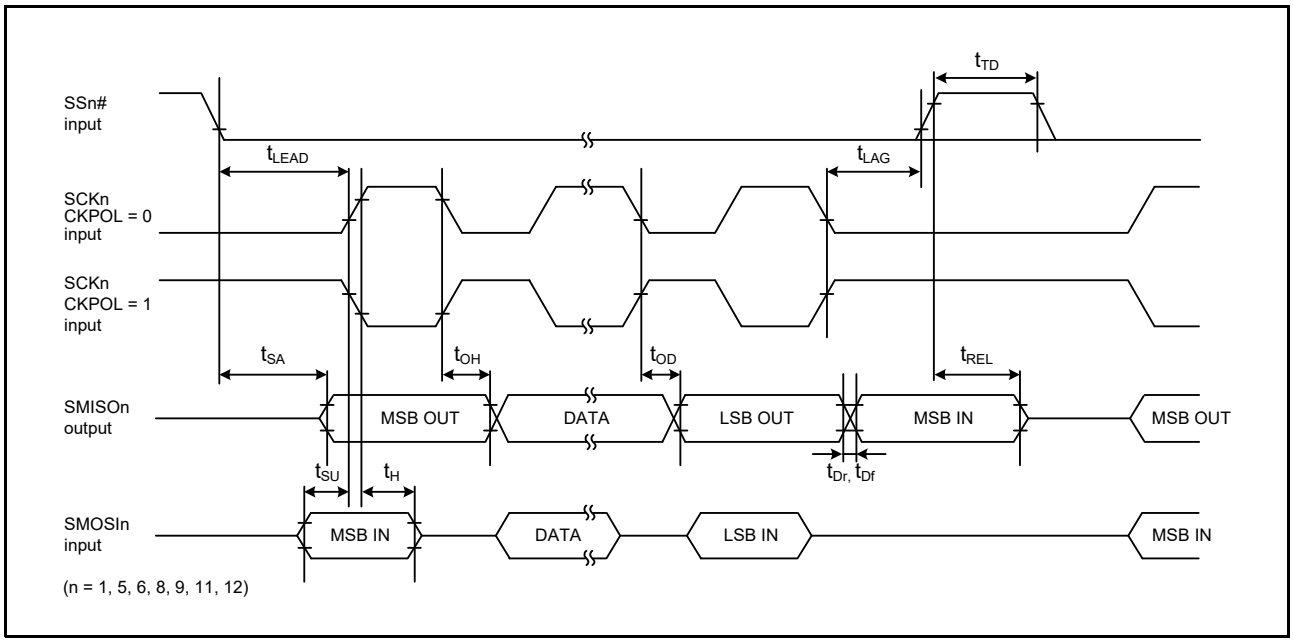


Figure 2.51 Simple SPI Timing (Slave, CKPH = 1)

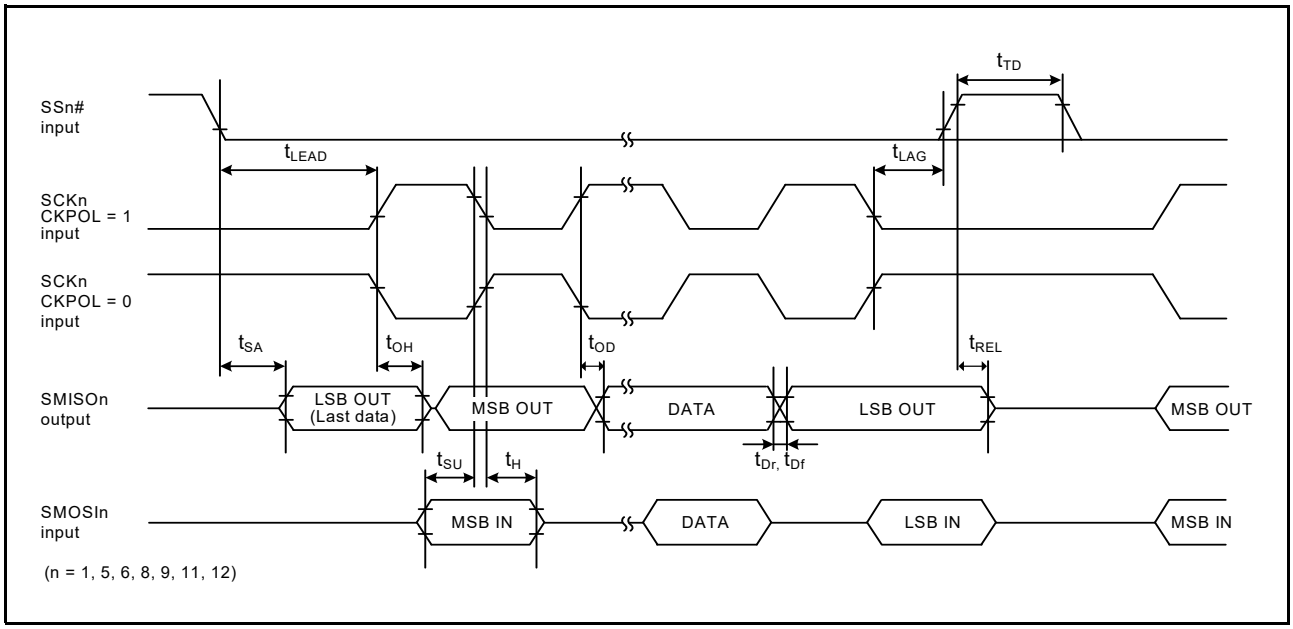


Figure 2.52 Simple SPI Timing (Slave, CKPH = 0)

2.4.6.10 RSPI

Table 2.39 RSPI Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item				Symbol	Min.*1	Max.*1	Unit*1	Test Conditions	
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{PAcyc}	Figure 2.53	
		Slave			4	—			
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—	ns		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—	ns		
	RSPCK clock rise/fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns		
		Input			—	1	µs		
	Data input setup time	Master		t_{SU}	6	—	ns	VCC ≥ 4.5 V	Figure 2.54 to Figure 2.59
					11	—		VCC < 4.5 V	
		Slave			8.3	—		Figure 2.54 to Figure 2.59	
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—	ns		
			PCLKA division ratio set to a value other than 1/2	t_H	t_{PAcyc}	—			
		Slave			8.3	—			
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}		
		Slave			6	—	t_{PAcyc}		
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}		
		Slave			6	—	t_{PAcyc}		
	Data output delay time	Master		t_{OD}	—	6.3	ns	VCC ≥ 4.5 V	Figure 2.54 to Figure 2.59
		Slave			—	28			
		Master			—	11.3	ns	VCC < 4.5 V	
		Slave			—	33			
	Data output hold time	Master		t_{OH}	0	—	ns	Figure 2.54 to Figure 2.59	
		Slave			0	—			
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns		
		Slave			$6 \times t_{PAcyc}$	—			
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	5	ns		
		Input			—	1	µs		
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	5	ns		
		Input			—	1	µs		
	Slave access time			t_{SA}	—	$2 \times t_{PAcyc} + 28$	ns	VCC ≥ 4.5 V	Figure 2.58, Figure 2.59
					—	$2 \times t_{PAcyc} + 33$		VCC < 4.5 V	
	Slave output release time			t_{REL}	—	$2 \times t_{PAcyc} + 28$	ns	VCC ≥ 4.5 V	
					—	$2 \times t_{PAcyc} + 33$		VCC < 4.5 V	

Note 1. t_{PAcyc}: PCLKA cycle

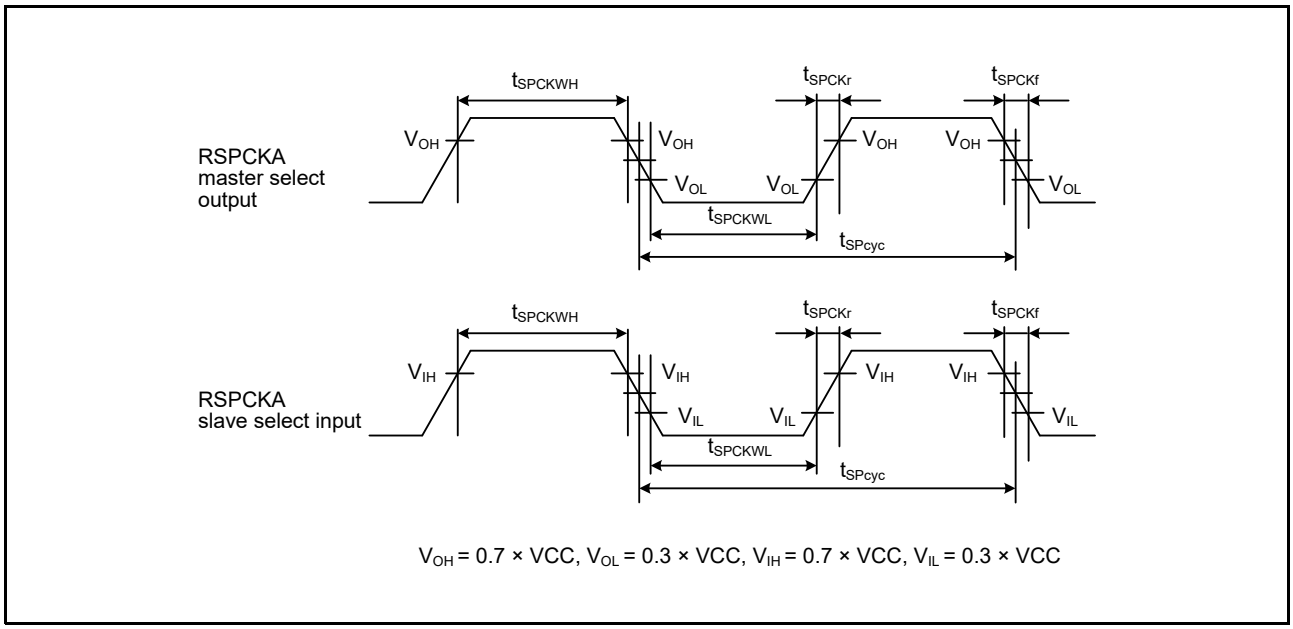


Figure 2.53 RSPI Clock Timing

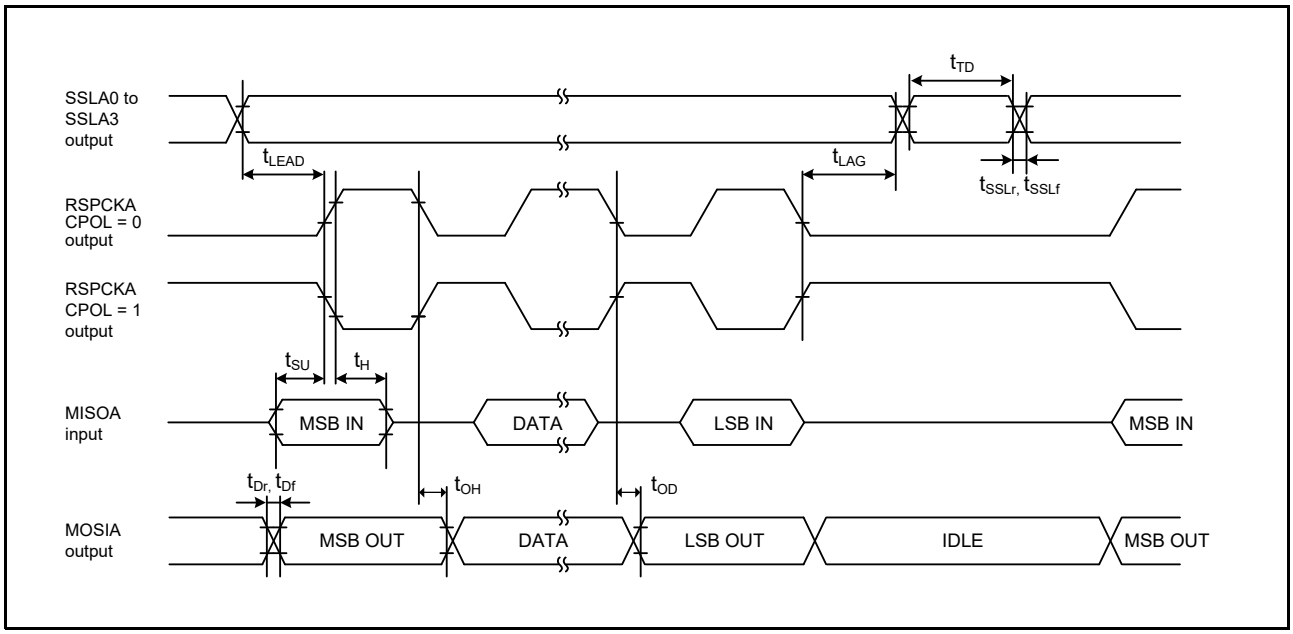


Figure 2.54 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

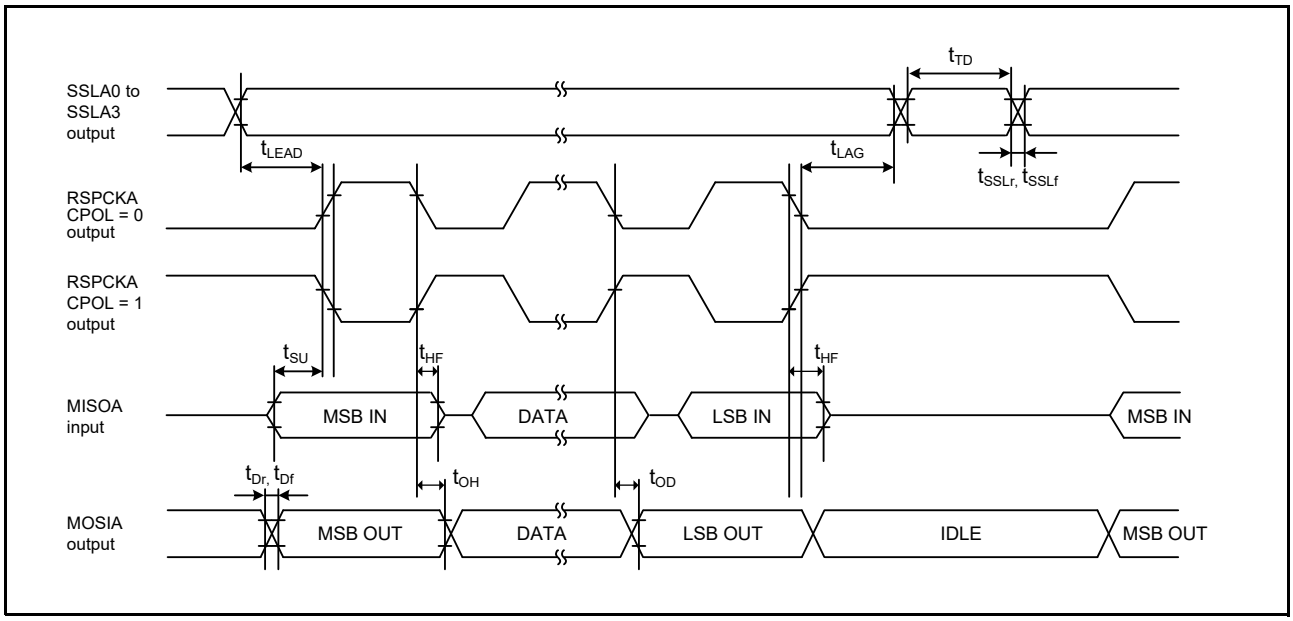


Figure 2.55 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

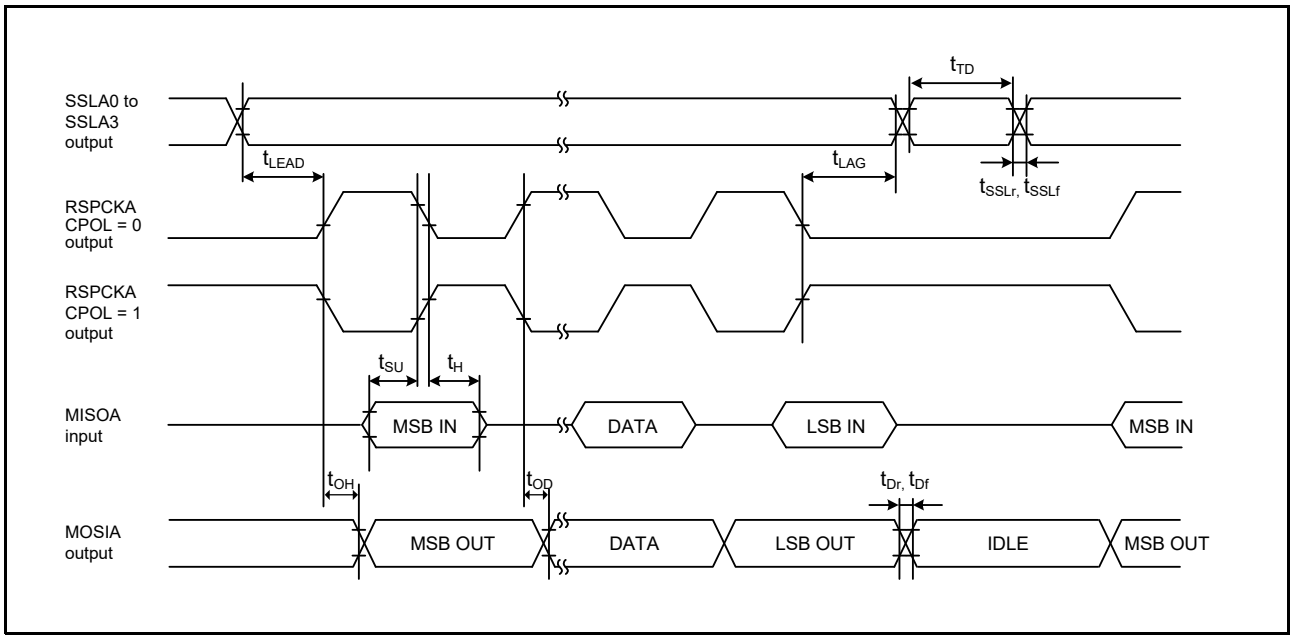


Figure 2.56 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

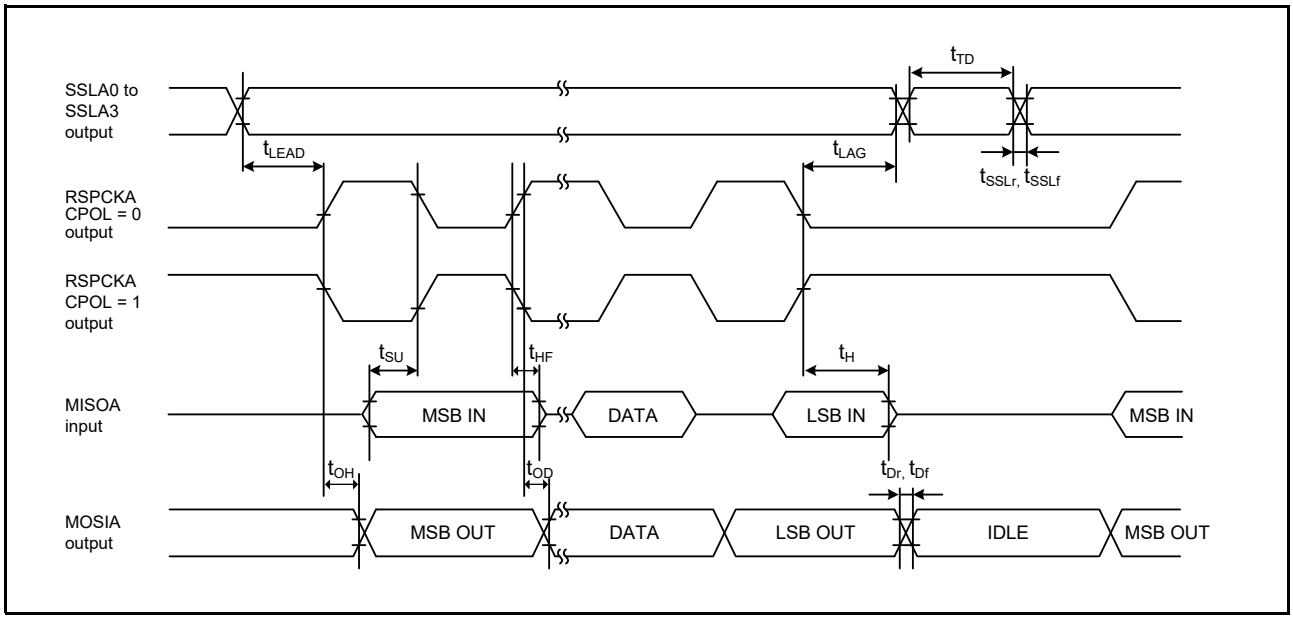


Figure 2.57 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

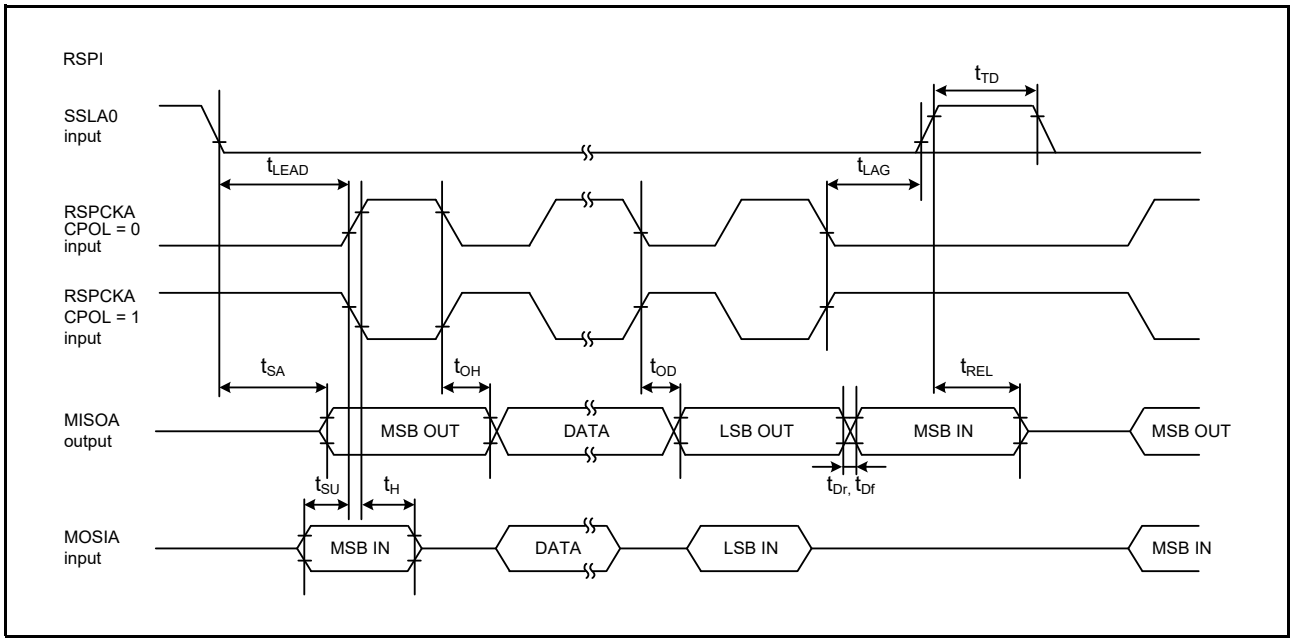


Figure 2.58 RSPI Timing (Slave, CPHA = 0)

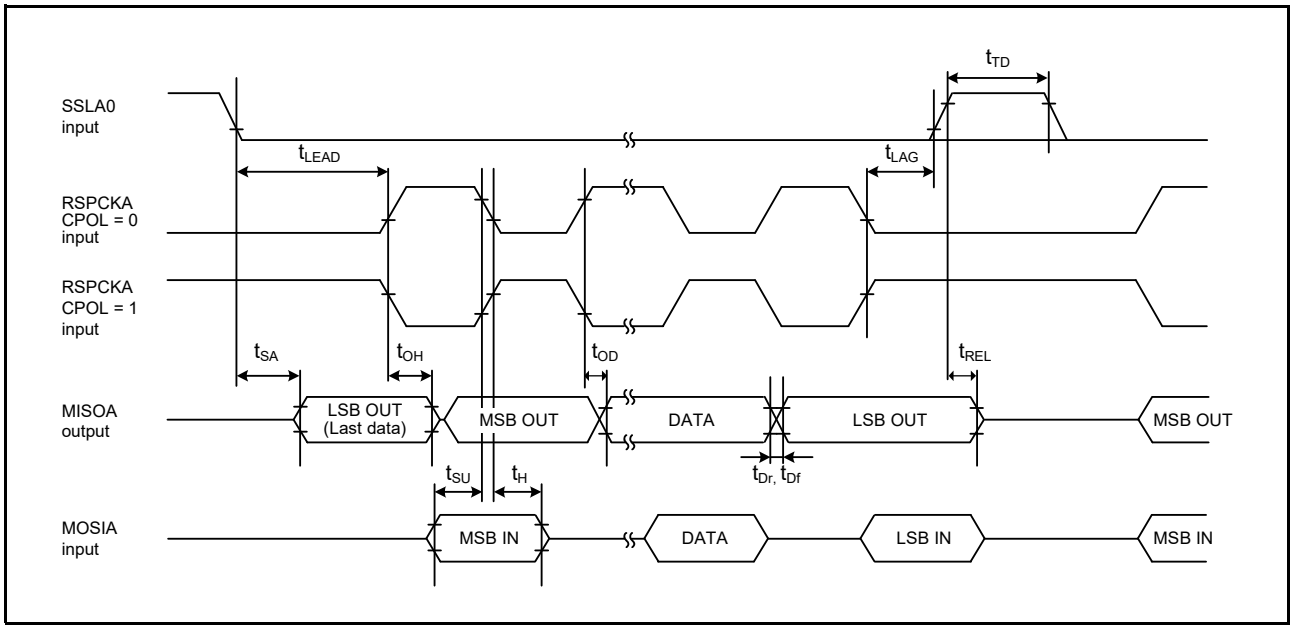


Figure 2.59 RSPI Timing (Slave, CPHA = 1)

2.4.6.11 RIIC

Table 2.40 RIIC Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item		Symbol *2	Min.*1	Max.*1	Unit	Test Conditions*3
RIIC (Standard-mode, SMBus)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.60
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—		
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—		
	SCL, SDA input rise time	t_{Sr}	—	1000		
	SCL, SDA input fall time	t_{Sf}	—	300		
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}		
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—		
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—		
	Restart condition input setup time	t_{STAS}	1000	—		
	Stop condition input setup time	t_{STOS}	1000	—		
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—		
	Data input hold time	t_{SDAH}	0	—		
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—		
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—		
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage/5.5V)	300		
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage/5.5V)	300		
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}		
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—		
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—		
	Restart condition input setup time	t_{STAS}	300	—		
	Stop condition input setup time	t_{STOS}	300	—		
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—		
	Data input hold time	t_{SDAH}	0	—		
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.
Note 3. When VCC ≥ 4.5V, VOLSR.RICVLS = 0
When VCC < 4.5V, VOLSR.RICVLS = 1

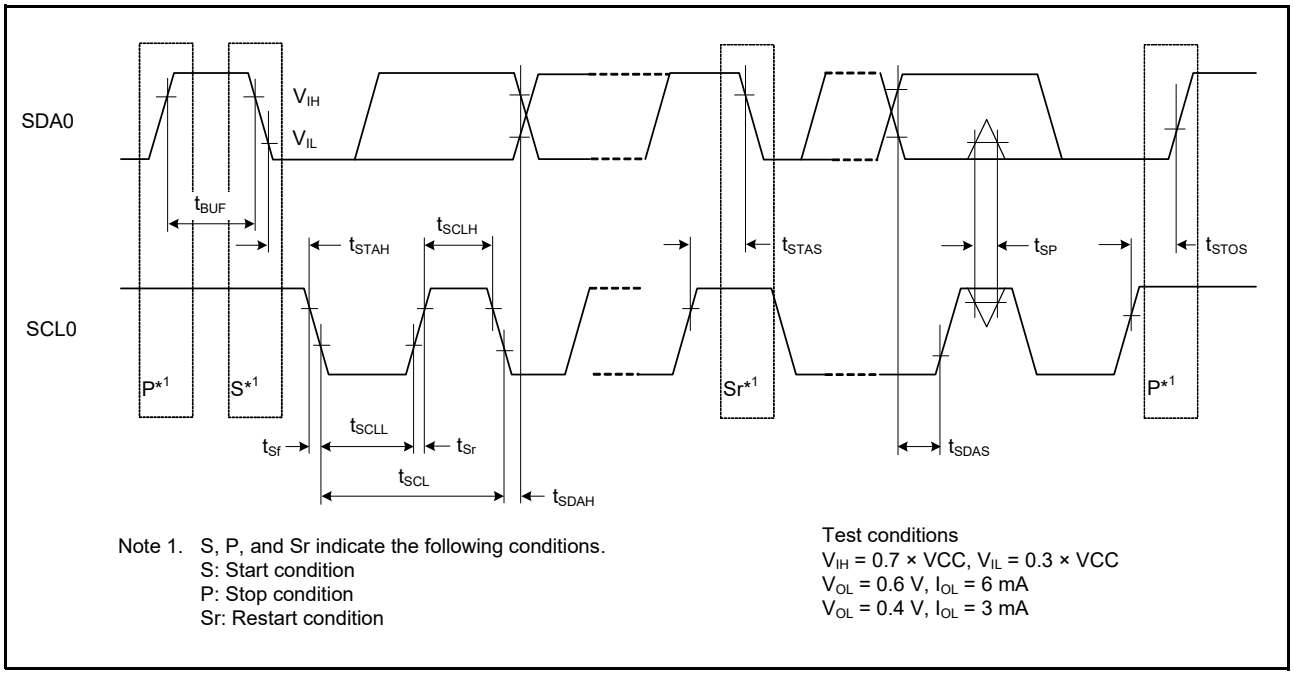


Figure 2.60 RIIC Bus Interface Input/Output Timing

2.4.6.12 HRPWM

Table 2.41 HRPWM Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 200 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 200 MHz, BCLK = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item	Min.	Typ.	Max.	Unit	Test Conditions
Input frequency (f_{IN})	80	—	160	MHz	
Resolution	—	195	—	ps	f_{IN} = 160 MHz
DNL*1	—	±2.0	—	LSB	

Note 1. The value is that difference from code to code normalized by the resolution (1 LSB).

2.5 USB Characteristics

Table 2.42 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 3.0 to 3.6 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
UCLK = 48 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz

Item		Symbol	Min.	Max.	Unit	Test Conditions
Input characteristics	Input high-level voltage	V_{IH}	2.0	—	V	
	Input low-level voltage	V_{IL}	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	2.5	V	
Output characteristics	Output high-level voltage	V_{OH}	2.8	3.6	V	I_{OH} = –200 µA
	Output low-level voltage	V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	2.0	V	Figure 2.61
	Rise time	t_{LR}	75	300	ns	
	Fall time	t_{LF}	75	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	125	%	t_{LR}/ t_{LF}
Pull-down characteristics	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	24.80	kΩ	

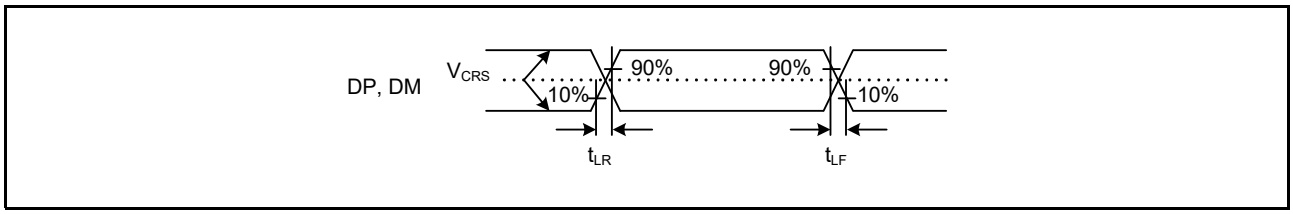


Figure 2.61 DP and DM Output Timing (Low Speed)

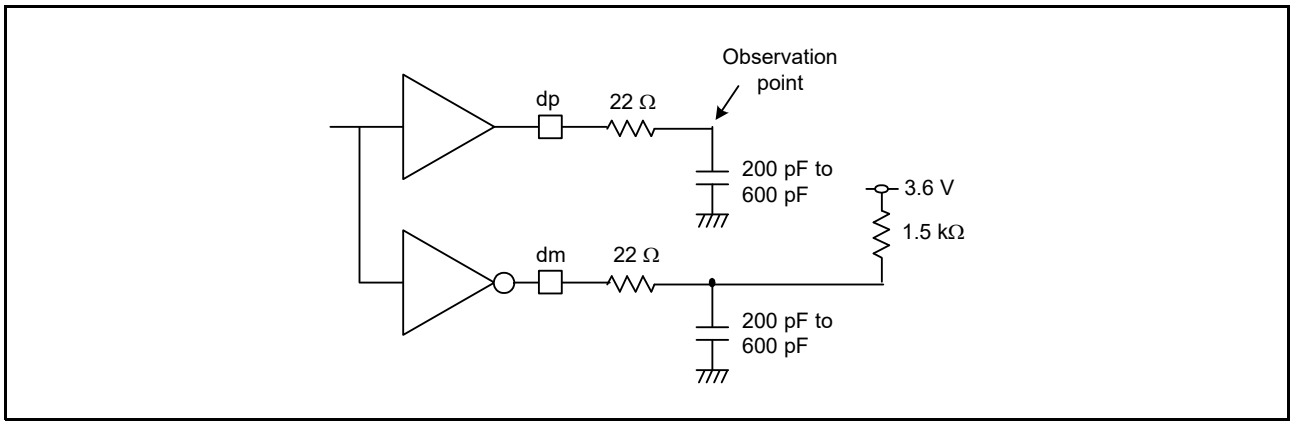


Figure 2.62 Test Circuit (Low Speed)

Table 2.43 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 3.0 to 3.6 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
UCLK = 48 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz

Item		Symbol	Min.	Max.	Unit	Test Conditions
Input characteristics	Input high-level voltage	V_{IH}	2.0	—	V	
	Input low-level voltage	V_{IL}	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	2.5	V	
Output characteristics	Output high-level voltage	V_{OH}	2.8	3.6	V	I_{OH} = –200 µA
	Output low-level voltage	V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	2.0	V	Figure 2.63
	Rise time	t_{FR}	4	20	ns	
	Fall time	t_{FF}	4	20	ns	
	Rise/fall time ratio	t_{FR} / t_{FF}	90	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	44	Ω	Rs = 22 Ω included
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	1.575	kΩ	Idle state
			1.425	3.090	kΩ	At transmission and reception
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	24.80	kΩ	

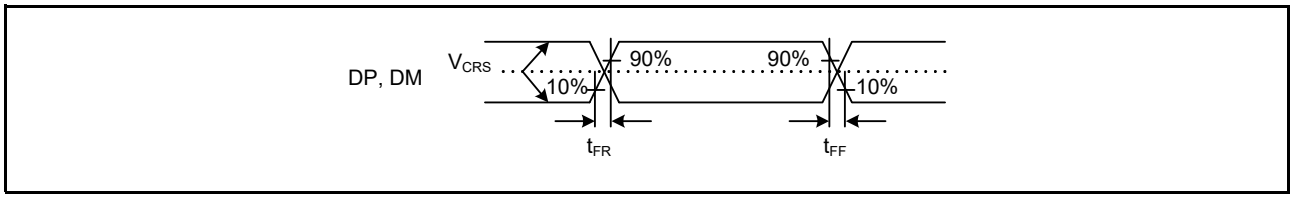


Figure 2.63 DP and DM Output Timing (Full-Speed)

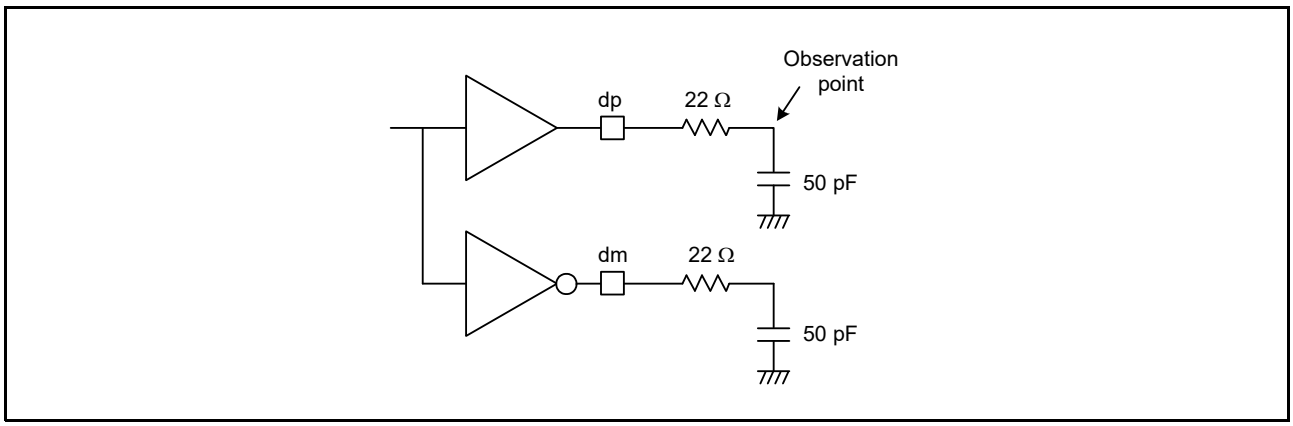


Figure 2.64 Test Circuit (Full-Speed)

2.6 A/D Conversion Characteristics

Table 2.44 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, 4.5 V ≤ AVCC0 = AVCC1 = AVCC2 ≤ 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 60 MHz*1,
Source impedance = 1.0 kΩ

Item				Min.	Typ.	Max.	Unit	Test Conditions
Resolution				12	12	12	Bit	
Analog input capacitance				—	—	30	pF	
Conversion time*2 (Operation at PCLKD = 60 MHz)	AN000 to AN002, AN100 to AN102	Channel-dedicated sample-and-hold circuits in use	Constant sampling enabled	1.00	—	—	μs	• Sampling time: 24 PCLKD
			Constant sampling disabled	1.40	—	—		• Sampling time of channel-dedicated sample-and-hold circuits: 24 PCLKD • Sampling time: 24 PCLKD
		Channel-dedicated sample-and-hold circuits not in use		0.90	—	—		• Sampling time: 30 PCLKD
	AN003 to AN006, AN103 to AN106			0.90	—	—		• Sampling time: 30 PCLKD
	AN007, AN107, AN200 to AN211			0.95	—	—		• Sampling time: 33 PCLKD
	AN216 to AN217			1.05	—	—		• Sampling time: 39 PCLKD
Offset error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±6.0	LSB	AN000 to AN002, AN100 to AN102 = 0.2 V
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±5.0		
Full-scale error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±5.5		AN000 to AN002 = AVCC0 – 0.2 V AN100 to AN102 = AVCC1 – 0.2 V
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±4.5		
Quantization error		Channel-dedicated sample-and-hold circuits in use		—	±0.5	—		
		Channel-dedicated sample-and-hold circuits not in use		—	±0.5	—		
Absolute accuracy	AN000 to AN002, AN100 to AN102	Channel-dedicated sample-and-hold circuits in use		—	±3.0	±6.0		
		Channel-dedicated sample-and-hold circuits not in use		—	±2.5	±5.5		
	AN003 to AN007, AN103 to AN107			—	±2.5	±5.5		
	AN200 to AN211			—	±2.5	±5.5		
	AN216 to AN217			—	±2.5	±6.5		
DNL differential nonlinearity error		Channel-dedicated sample-and-hold circuits in use		—	±1.0	±2.5		
		Channel-dedicated sample-and-hold circuits not in use		—	±1.0	±1.5		
INL integral nonlinearity error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±4.0		
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±2.5		
Holding time of the channel-dedicated sample-and-hold circuit				—	—	20	μs	
Dynamic range	AN000 to AN002	Channel-dedicated sample-and-hold circuits in use		0.2	—	AVCC0 – 0.2	V	
	AN100 to AN102	Channel-dedicated sample-and-hold circuits in use		0.2	—	AVCC1 – 0.2		

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. When PCLKD was higher than 40 MHz, 0.01-μF capacitors were placed in parallel with the 0.1-μF capacitors between AVCC0 and AVSS0, AVCC1 and AVSS1, and AVCC2 and AVSS2 for measurement of the A/D conversion characteristics.

Note 2. The conversion time is the sum of the sampling time and the comparison time. The numbers of sampling-clock cycles are indicated as the test conditions.

Table 2.45 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (2)

Conditions: VCC = 2.7 to 4.5 V, VCC_USB = 2.7 to 4.5 V, 3.0 V ≤ AVCC0 = AVCC1 = AVCC2 < 4.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 40 MHz,
Source impedance = 1.0 kΩ

Item				Min.	Typ.	Max.	Unit	Test Conditions
Resolution				12	12	12	Bit	
Analog input capacitance				—	—	30	pF	
Conversion time*1 (Operation at PCLKD = 40 MHz)	AN000 to AN002, AN100 to AN102	Channel-dedicated sample-and-hold circuits in use	Constant sampling enabled	1.35	—	—	μs	• Sampling time: 18 PCLKD
			Constant sampling disabled	1.80	—	—		• Sampling time of channel-dedicated sample-and-hold circuits: 18 PCLKD • Sampling time: 18 PCLKD
		Channel-dedicated sample-and-hold circuits not in use		1.13	—	—		• Sampling time: 21 PCLKD
	AN003 to AN006, AN103 to AN106			1.13	—	—		• Sampling time: 21 PCLKD
	AN007, AN107, AN200 to AN211			1.20	—	—		• Sampling time: 24 PCLKD
	AN216 to AN217			1.28	—	—		• Sampling time: 27 PCLKD
Offset error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±7.5	LSB	AN000 to AN002, AN100 to AN102 = 0.2 V
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±6.5		
Full-scale error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±7.5		AN000 to AN002 = AVCC0 – 0.2 V AN100 to AN102 = AVCC1 – 0.2 V
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±6.5		
Quantization error		Channel-dedicated sample-and-hold circuits in use		—	±0.5	—		
		Channel-dedicated sample-and-hold circuits not in use		—	±0.5	—		
Absolute accuracy	AN000 to AN002, AN100 to AN102	Channel-dedicated sample-and-hold circuits in use		—	±4.0	±8.0		
		Channel-dedicated sample-and-hold circuits not in use		—	±2.5	±7.0		
	AN003 to AN007, AN103 to AN107			—	±2.5	±7.0		
	AN200 to AN211			—	±2.5	±7.0		
	AN216 to AN217			—	±2.5	±8.0		
DNL differential nonlinearity error		Channel-dedicated sample-and-hold circuits in use		—	±1.0	±4.5		
		Channel-dedicated sample-and-hold circuits not in use		—	±1.0	±3.5		
INL integral nonlinearity error		Channel-dedicated sample-and-hold circuits in use		—	±2.0	±5.0		
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±3.5		
Channel-dedicated sample-and-hold characteristics of hold circuits				—	—	20	μs	
Dynamic range	AN000 to AN002	Channel-dedicated sample-and-hold circuits in use		0.2	—	AVCC0 – 0.2	V	
	AN100 to AN102	Channel-dedicated sample-and-hold circuits in use		0.2	—	AVCC1 – 0.2		

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The numbers of sampling-clock cycles are indicated as the test conditions.

Table 2.46 A/D Internal Reference Voltage Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 60 MHz

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.20	1.25	1.30	V	

Note: The above specification values apply during normal operations.

2.7 Programmable Gain Amplifier Characteristics

Table 2.47 Programmable Gain Amplifier Characteristics (single-ended input)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input offset voltage	V_{IO}	—	3	8	mV	
Single-ended input voltage range	V_{ISR}	V_{OR} (min)/G	—	V_{OR} (min)/G	V	
Output voltage range	V_{OR}	0.10 × AVCCn	—	0.90 × AVCCn		G = 2.000 to 3.636
		0.15 × AVCCn	—	0.85 × AVCCn		G = 4.000 to 6.667
		0.20 × AVCCn	—	0.80 × AVCCn		G = 8.000 to 20.000
Gain	G	2.000	—	20.000	Linear gain	
Gain error	E_G	—	±0.5	±2.0	%	G = 2.000
		—	±0.5	±2.0		G = 2.500
		—	±0.5	±2.0		G = 3.077
		—	±0.5	±2.0		G = 3.636
		—	±0.6	±2.0		G = 4.000
		—	±0.6	±2.0		G = 4.444
		—	±0.7	±2.0		G = 5.000
		—	±0.7	±3.0		G = 6.667
		—	±0.7	±3.0		G = 8.000
		—	±0.7	±4.0		G = 10.000
		—	±1.1	±4.0		G = 13.333
		—	±1.3	±4.0		G = 20.000
Slew rate	SR	10	—	—	V/µs	
Operation stabilization time	t_{start}	—	—	5	µs	

n = 0 and 1

Table 2.48 Programmable Gain Amplifier Characteristics (pseudo-differential input)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions*1
Input offset voltage	V_{IO}	—	10	20	mV	
Differential input voltage range	V_{IDR}	–0.28 × AVCCn / G	—	0.28 × AVCCn / G	V	
Output voltage range	V_{OR}	0.22 × AVCCn	—	0.78 × AVCCn		
Input voltage range (PGAVSSn)	$V_{I(PGAVSS)}$	–0.5	—	0.3		AVCCn < 4.3V
		–0.5	—	0.6		AVCCn ≥ 4.3 V
Gain error	E_G	—	±0.5	±2.0	%	G = 1.500
		—	±0.5	±2.0		G = 4.000
		—	±0.8	±3.0		G = 7.000
		—	±1.2	±4.0		G = 12.333
Slew rate	SR	10	—	—	V/µs	
Operation stabilization time	t_{start}	—	—	5	µs	

n = 0 and 1

Note 1. When AVCC0 = AVCC1 = AVCC2 ≥ 4.0 V, VOLSR.PGAVLS = 0
When AVCC0 = AVCC1 = AVCC2 < 4.0 V, VOLSR.PGAVLS = 1

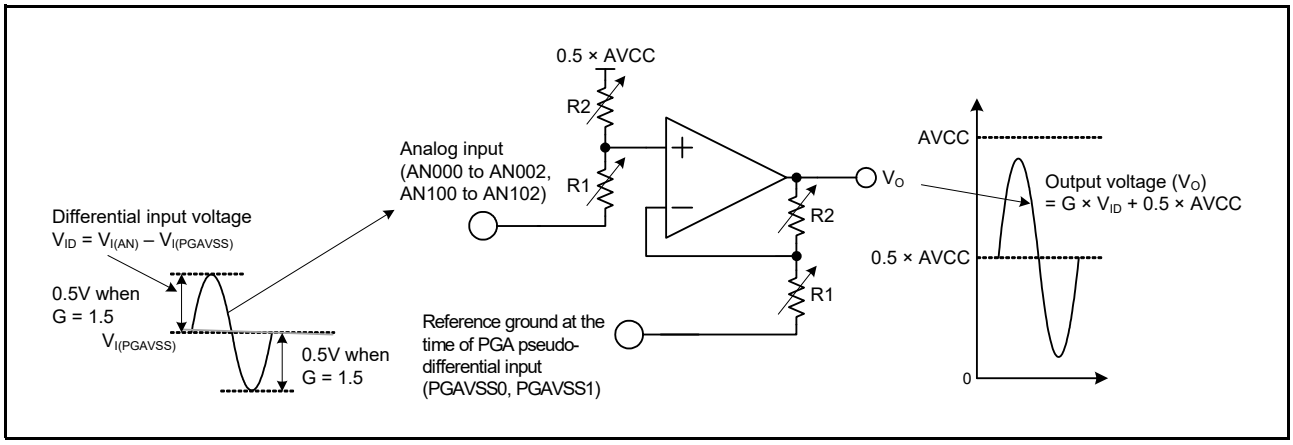


Figure 2.65 Input and Output Signal Levels with the PGA's Pseudo-Differential Setting

2.8 Comparator Characteristics

Table 2.49 Comparator Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input offset voltage	V_{IO}	—	8	40	mV	
Reference input voltage range	V_{ref}	0	—	AVCC1	V	CMPSEL1.CVRS[3:0] = 0100b, 1000b
		0	—	AVCC2		CMPSEL1.CVRS[3:0] = 0001b, 0010b
Response time	$t_{tot(r)}$	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS[1:0] = 00b
	$t_{tot(f)}$	—	—	200		
Waiting time for stabilization following switching of the input	t_{cwait}	300	—	—		
Operation stabilization time	t_{cmp}	—	—	1	µs	

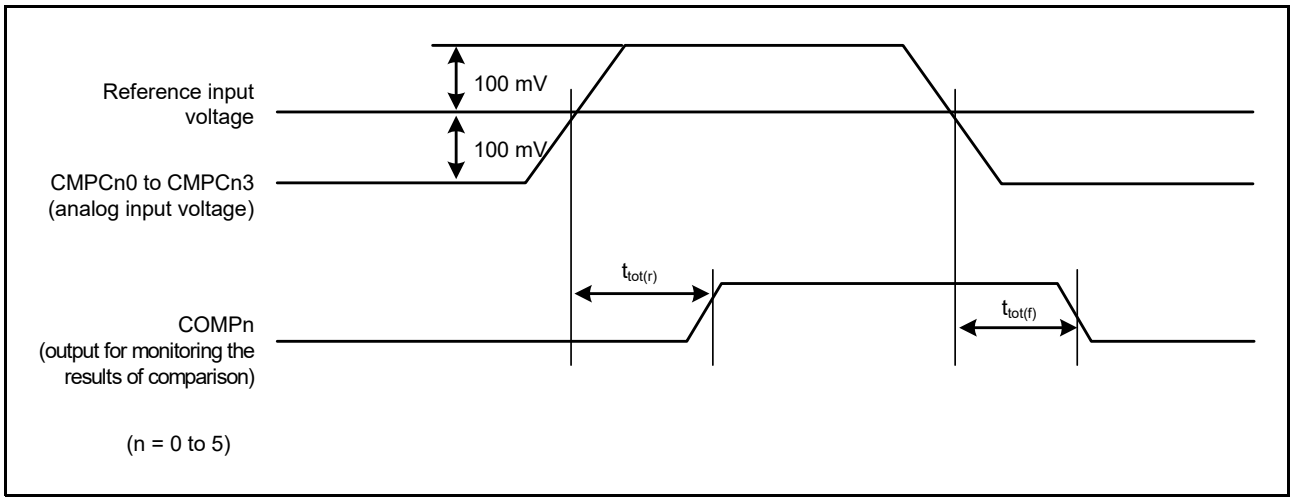


Figure 2.66 Comparator Response Time

2.9 D/A Conversion Characteristics

Table 2.50 D/A Conversion Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	12	12	12	Bit	
Absolute accuracy	—	—	±6.0	LSB	2-MΩ resistive load, 10-bit conversion
Differential nonlinearity error (DNL)	—	±1.0	±2.0	LSB	2-MΩ resistive load
Output resistance (R_o)	—	5.7	—	kΩ	
Conversion time	—	—	3	µs	20-pF capacitive load

2.10 Temperature Sensor Characteristics

Table 2.51 Temperature Sensor Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKB = PCLKD = 8 to 60 MHz

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1.0	—	°C	
Temperature slope	—	–2.0	—	mV/°C	
Output voltage	—	0.63	—	V	T_a = 25°C
Temperature sensor start time	—	—	200	µs	
Sampling time*1	3	—	—	µs	

Note 1. Set the S12AD2.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

2.11 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.52 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.46	2.58	2.70	V	Figure 2.67
	Voltage detection circuit (LVD0)	V_{det0_1}	4.04	4.22	4.40		Figure 2.68
		V_{det0_2}	2.71	2.83	2.95		
	Voltage detection circuit (LVD1)	V_{det1_0}	4.39	4.57	4.75		Figure 2.69
		V_{det1_1}	4.29	4.47	4.65		
		V_{det1_2}	4.14	4.32	4.50		
		V_{det1_3}	2.81	2.93	3.05		
		V_{det1_4}	2.76	2.88	3.00		
	Voltage detection circuit (LVD2)	V_{det2_0}	4.39	4.57	4.75		Figure 2.70
		V_{det2_1}	4.29	4.47	4.65		
		V_{det2_2}	4.14	4.32	4.50		
		V_{det2_3}	2.81	2.93	3.05		
		V_{det2_4}	2.76	2.88	3.00		
Internal reset time	Power-on reset time	t_{POR}	—	13.7	—	ms	Figure 2.67
	LVD0 reset time	t_{LVD0}	—	0.70	—		Figure 2.68
	LVD1 reset time	t_{LVD1}	—	0.57	—		Figure 2.69
	LVD2 reset time	t_{LVD2}	—	0.57	—		Figure 2.70
Minimum VCC down time		t_{VOFF}	200	—	—	μs	Figure 2.67, Figure 2.68
Response delay time		t_{det}	—	—	200	μs	Figure 2.67 to Figure 2.70
LVD operation stabilization time (after LVD is enabled)		$T_{d(E-A)}$	—	—	20	μs	Figure 2.69, Figure 2.70
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

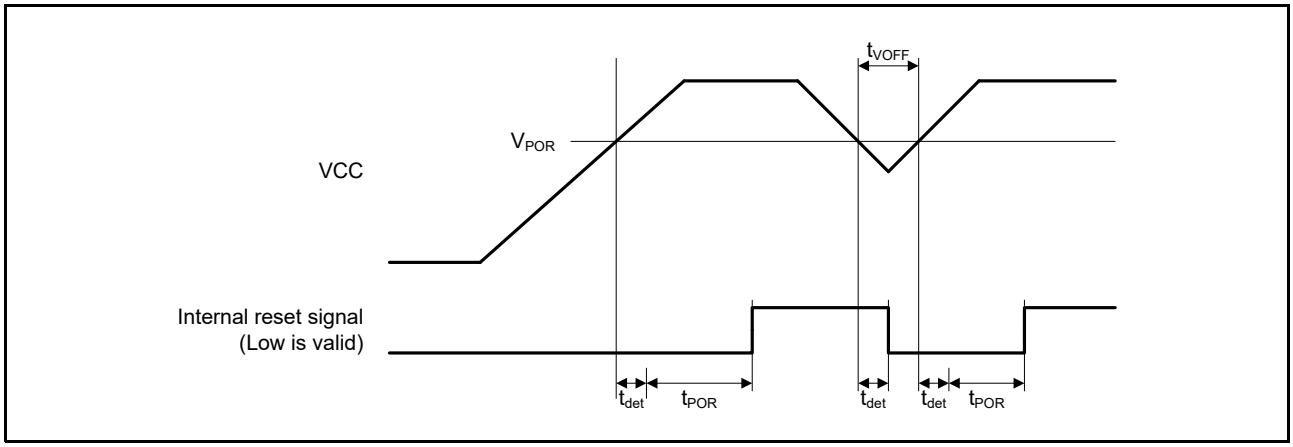


Figure 2.67 Power-on Reset Timing

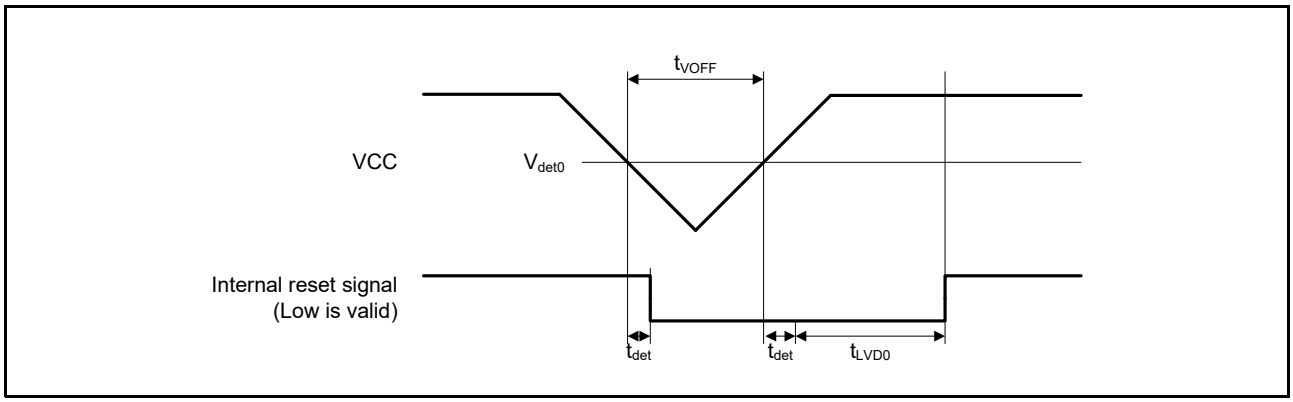


Figure 2.68 Voltage Detection Circuit Timing (V_{det0})

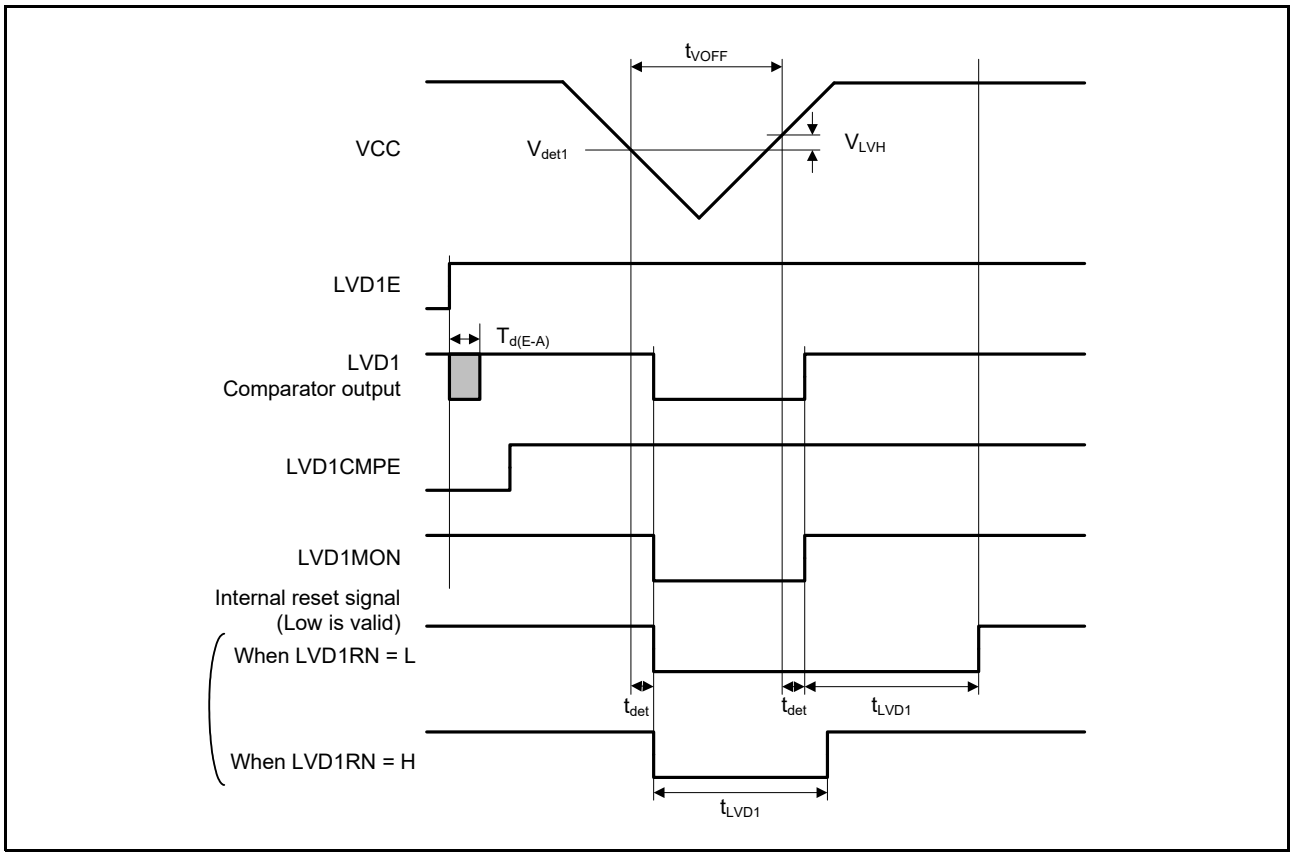


Figure 2.69 Voltage Detection Circuit Timing (V_{det1})

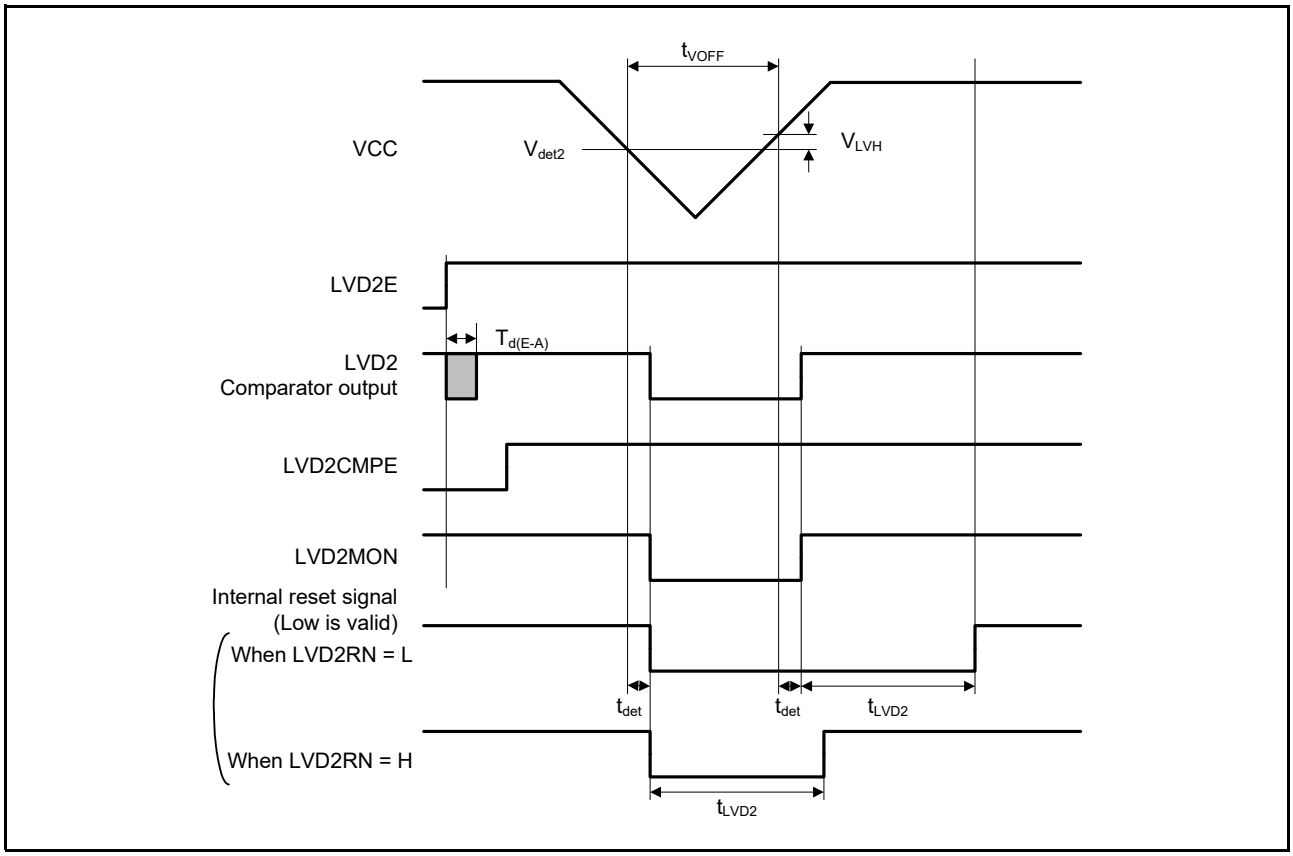


Figure 2.70 Voltage Detection Circuit Timing (V_{det2})

2.12 Oscillation Stop Detection Timing

Table 2.53 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.71

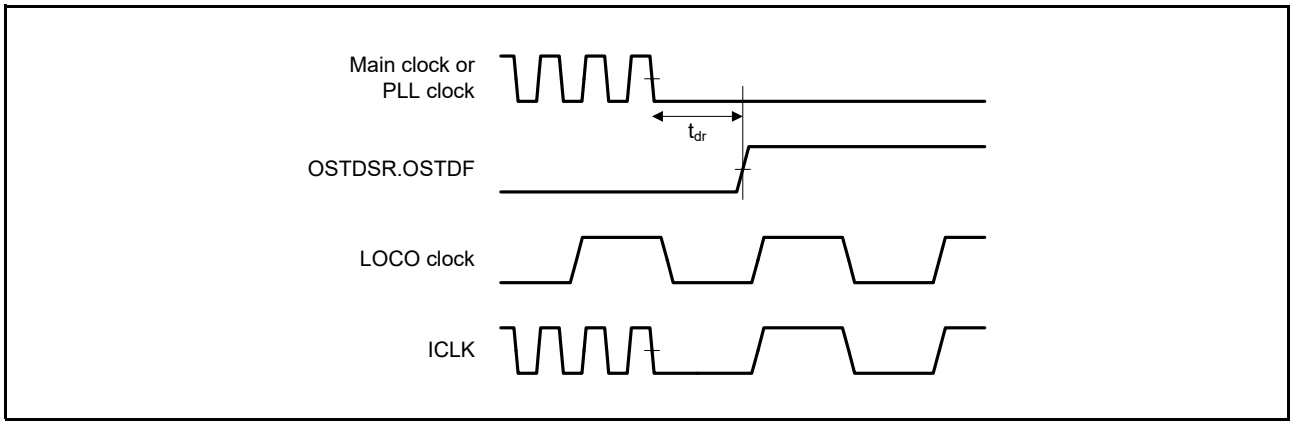


Figure 2.71 Oscillation Stop Detection Timing

2.13 Flash Memory Characteristics

Table 2.54 Code Flash Memory Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
Temperature range for program/erase: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Program time (N_{PEC} ≤ 100 cycles)	256 bytes	t_{P256}	—	0.9	13.2	—	0.4	6	ms	
	8 Kbytes	t_{P8K}	—	29	176	—	13	80		
	32 Kbytes	t_{P32K}	—	116	704	—	52	320		
Program time (N_{PEC} > 100 cycles)	256 bytes	t_{P256}	—	1.1	15.8	—	0.5	7.2		
	8 Kbytes	t_{P8K}	—	35	212	—	16	96		
	32 Kbytes	t_{P32K}	—	140	848	—	64	384		
Erase time (N_{PEC} ≤ 100 cycles)	8 Kbytes	t_{E8K}	—	71	216	—	39	120		
	32 Kbytes	t_{E32K}	—	254	864	—	141	480		
Erase time (N_{PEC} > 100 cycles)	8 Kbytes	t_{E8K}	—	85	260	—	47	144		
	32 Kbytes	t_{E32K}	—	304	1040	—	169	576		
Program/erase cycles*1		N_{PEC}	1000*2	—	—	1000*2	—	—	Cycles	
Program suspend latency		t_{SPD}	—	—	264	—	—	120	µs	
Primary erase suspend latency in suspend priority mode		t_{SESD1}	—	—	216	—	—	120		
Secondary erase suspend latency in suspend priority mode		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Erase suspend latency in erase priority mode		t_{SEED}	—	—	1.7	—	—	1.7		
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data retention*3, *4		t_{DRP}	20	—	—	20	—	—	Year	T_a ≤ 85°C
			10	—	—	10	—	—		T_a ≤ 105°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 256-byte program is performed 32 times for different addresses in 8-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

Table 2.55 Data Flash Memory Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
Temperature range for program/erase: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Program time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
Erase time	64 bytes	t_{DE64}	—	3.1	18	—	1.7	10		
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	30	µs	
	64 bytes	t_{DBC64}	—	—	280	—	—	100		
	2 Kbytes	t_{DBC2K}	—	—	6160	—	—	2200		
Program/erase cycles*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	Cycles	
Program suspend latency		t_{DSPD}	—	—	264	—	—	120	µs	
Primary erase suspend latency in suspend priority mode		t_{DSESD1}	—	—	216	—	—	120		
Secondary erase suspend latency in suspend priority mode		t_{DSESD2}	—	—	300	—	—	300		
Erase suspend latency in erase priority mode		t_{DSEED}	—	—	300	—	—	300		
Forced stop command		t_{FD}	—	—	32	—	—	20		
Data retention*3, *4		t_{DDRP}	20	—	—	20	—	—	Year	$T_a \leq 85°C$
			10	—	—	10	—	—		$T_a \leq 105°C$

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 512 times for different addresses in 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

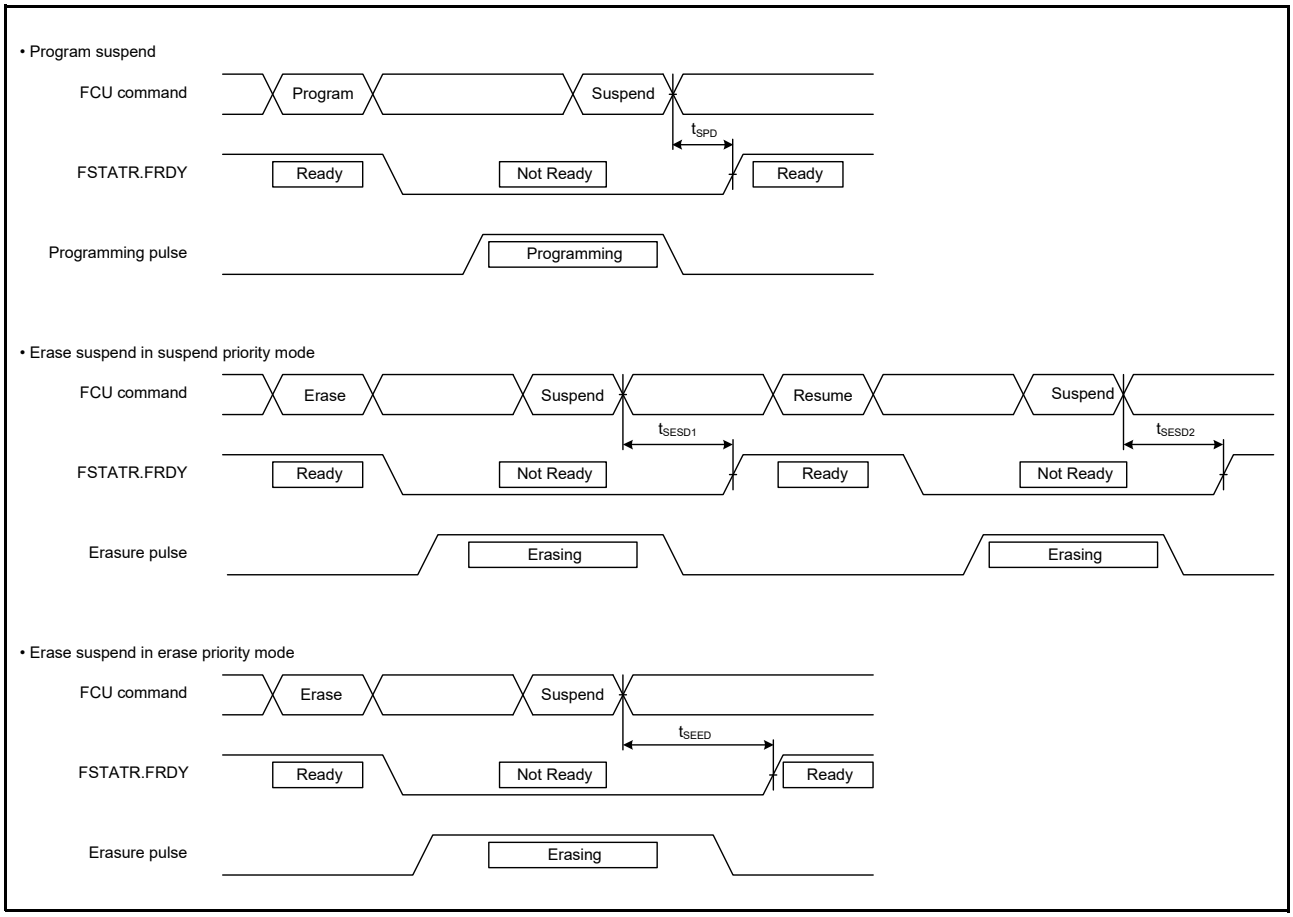


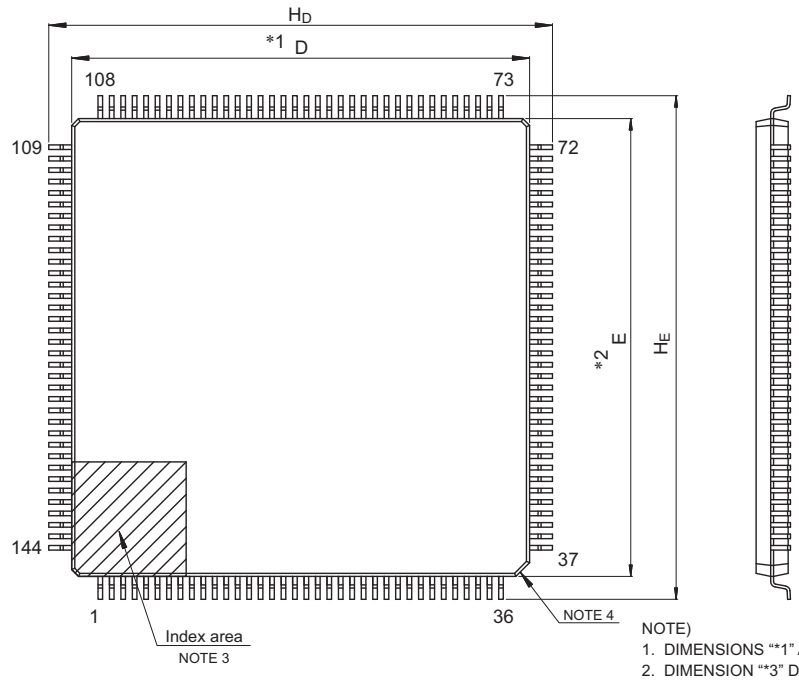
Figure 2.72 Flash Memory Program/Erase Suspend Timing

Appendix 1. Package Dimensions

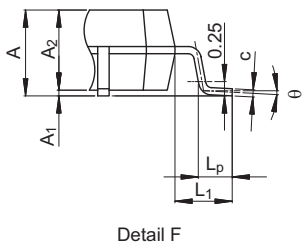
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm



NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



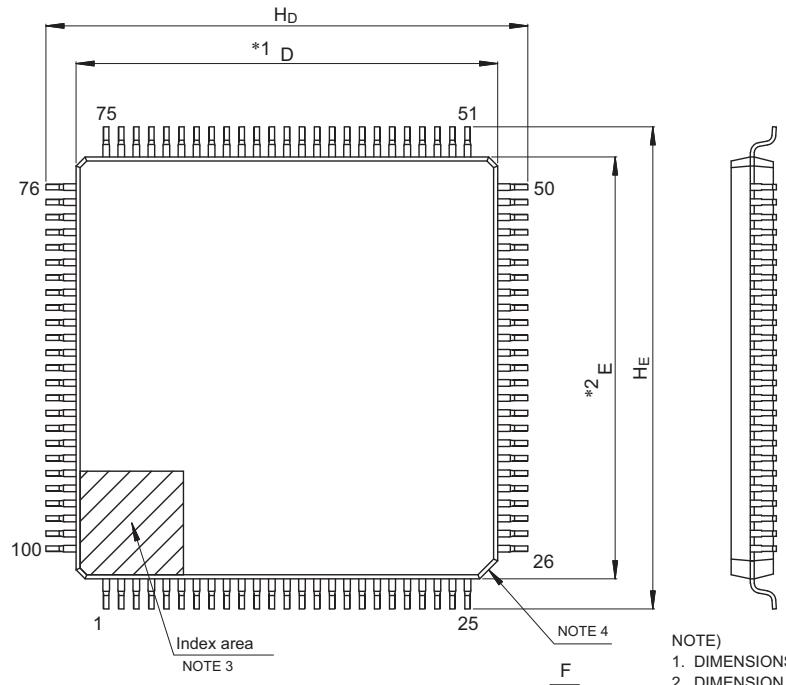
Detail F

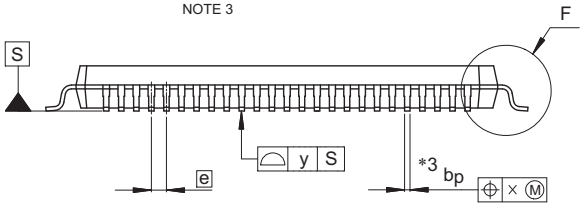
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
L_p	0.45	0.6	0.75
L_1	—	1.0	—

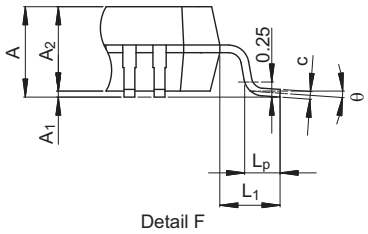
Figure A 144-Pin LFQFP (PLQP0144KA-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure B 100-Pin LFQFP (PLQP0100KB-B)

REVISION HISTORY	RX72T Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

1

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Feb 08, 2019	—	First edition, issued	
1.10	Oct 06, 2023	All	Changed the chapter structure	
		1. Overview		
		8	Table 1.1 Outline of Specifications (7/9), changed	
		13	Table 1.3 List of Products, changed	
		14	Figure 1.1 How to Read the Product Part Number, changed	
		16	Table 1.4 Pin Functions (1/6), changed	
		2. Electrical Characteristics		
		49	Table 2.3 Recommended operating conditions (2), changed	TN-RX*-A0270A/E
		57	Table 2.11 Standard Output Characteristics (1), added	TN-RX*-A0219A/E
		58	Table 2.12 Standard Output Characteristics (2), added	
		105	Table 2.47 Programmable Gain Amplifier Characteristics (single-ended input), changed	
			Table 2.48 Programmable Gain Amplifier Characteristics (pseudo-differential input), changed	
		113	Table 2.54 Code Flash Memory Characteristics, changed	TN-RX*-A0249A/E
		114	Table 2.55 Data Flash Memory Characteristics, changed	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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