XGS Family

XGS 12000, XGS 9400 and XGS 8000 Global Shutter CMOS Image Sensors

ON Semiconductor®

www.onsemi.com

Description

The XGS CMOS image sensor family provides high resolution, high performance global shutter image capture. The family comes in different resolutions in a single package; 8.8, 9.4 and 12.6 Megapixels with up to 1−inch optical format. The 21 mm x 20 mm package makes the XGS family particularly suited for integration in 29 mm x 29 mm camera formats. The high speed, 12−bit output maximally leverages interfaces such as USB 3.2, Thunderbolt™ 2 and 10 GigE.

Image data is read out through a column ADC architecture and then transferred over a HiSPi interface. On−chip logic, programmable via the serial interface, generates internal timing for integration and readout control. Up to three register configurations can be programmed and sequentially enabled (frame by frame) using a single command over the control interface.

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Typical Value	
Optical Format	XGS 12000	1−inch (16.4 mm Diagonal)
	XGS 9400	1/1.2−inch (13.9 mm Diagonal)
	XGS 8000	1/1.1−inch (14.8 mm Diagonal)
Active Pixels	XGS 12000	4096 (H) x 3072 (V)
	XGS 9400	3072 (H) x 3072 (V)
	XGS 8000	4096 (H) x 2160 (V)
Pixel Size	3.2 μm	
Color Filter Array	Monochrome, Bayer	
Shutter Type	Global Shutter	
Input Clock	32.4 MHz	
Output Interface	HiSPi (24 Lanes − 777.6 Mbps/lane)	
Frame Rate (12−bit)	24 Lanes (−X1)	
	XGS 12000	90 fps
	XGS 9400	90 fps
	XGS 8000	128 fps
	12 Lanes (−X2)	
	XGS 9400	56 fps
	XGS 8000	80 fps
	6 Lanes (−X3)	
	XGS 12000	28 fps
Read Noise	< 4 e− (1x), 1.9 e^- (4x)	
SNR_{MAX}	40 dB	
Dynamic Range	68 dB	
Supply Voltages	1.2V, 2.8 V, 3 V (0.4 V, 1.8 V Optional)	
Power Consumption	1 W (Full Speed, Full Resolution)	
Operating Temp.	−40°C to 85°C (Junction)	
Package	163−pin CLGA (Ceramic Land Grid Array)	

Features

- On−chip 12−bit Column ADCs
- Companding Mode for 60 fps (12−lane) and 30 fps (6−lane) at Full Resolution
- Data Interface: 24−lane HiSPi (Scalable Low−Voltage Signaling)
- Configurable Number of HiSPi Lanes: 24, 18, 12 or 6 Lanes
- Two−Wire (I^2C) and Four−Wire (SPI) Serial Interface
- Triggered Integration and Readout Control
- Programmable Control for up to 8 Regions of Interest (ROI)
- Context Switching
- These Devices are Pb−Free, Halogen Free/ BFR Free and are RoHS Compliant

Applications

- Machine Vision
- Security
- Intelligent Transportation Systems (ITS)
- Broadcasting
- Medical
- Scientific

ORDERING INFORMATION

Table 2. ORDERABLE PART NUMBERS (Note 1, Note 2)

Part Number	Product Description		Speed Grade	Resolution (H x V)
NOIX1SN012KB−LTI	12.6 Mp	Mono	24 lanes	4096 x 3072
NOIX1SE012KB−LTI	12.6 Mp	Color		
NOIX3SN012KB−LTI	12.6 Mp	Mono	6 lanes	
NOIX3SE012KB−LTI	12.6 Mp	Color		
NOIX1SN9400B−LTI	9.4 MP	Mono	24 lanes	3072 x 3072
NOIX1SE9400B−LTI	9.4 MP	Color		
NOIX2SN9400B−LTI	9.4 MP	Mono	12 lanes	
NOIX2SE9400B−LTI	9.4 MP	Color		
NOIX1SN8000B−LTI	8.8 Mp	Mono	24 lanes	4096 x 2160
NOIX1SE8000B−LTI	8.8 Mp	Color		
NOIX2SN8000B−LTI	8.8 Mp	Mono	12 lanes	
NOIX2SE8000B−LTI	8.8 Mp	Color		

1. See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.
2. All devices listed in Table 2 are equipped with microlenses and optimized for a 0° Chief Ray Angle (zero−shift placement).

Table 3. ORDERING INFORMATION EVALUATION KITS

Part Number	Product Description	Additional Information
NOIX1SN012KBLFB−GEVB	Sensor Headboard (12.6 Mp, Mono, 24−Lane)	Demo Kit Headboard (incl. NOIX1SN012KB−LTI) (Note 3)
NOIX1SE012KBLFB−GEVB	Sensor Headboard (12.6 Mp, Color, 24−Lane)	Demo Kit Headboard (incl. NOIX1SE012KB−LTI) (Note 3)
AGBAN6CS−GEVK	Frame Buffer Demo Board	AP21088 including Power Adapter
AGB1N0CS−GEVK	Demo 3 Board	FPGA Base Board including USB Cable and Tripod

3. Sensors are soldered to the headboard.

GENERAL DESCRIPTION

The XGS family from ON Semiconductor covers three resolutions: 12.6 Mp, 9.4 Mp and 8.8 Mp and three speed grades (24, 12 or 6 HiSPi lanes). Refer to Table 2 for an overview of the available combinations of resolution and speed. Various operating modes enable flexible sensor operation to meet application specific requirements such as reduced data rate implemented by HiSPi lane multiplexing.

FUNCTIONAL OVERVIEW

The XGS family features global shutter technology for accurate capture of moving objects. Global shutter requires all pixels to simultaneously integrate light although the subsequent readout is sequential. Note that integration and readout can occur in parallel; while reading out one frame, integration of the next frame can start (i.e. *pipelined operation*). The core of the sensor is the 12.6 Mp active pixel array.

Figure 1 gives an overview of the major functional blocks of the XGS sensor.

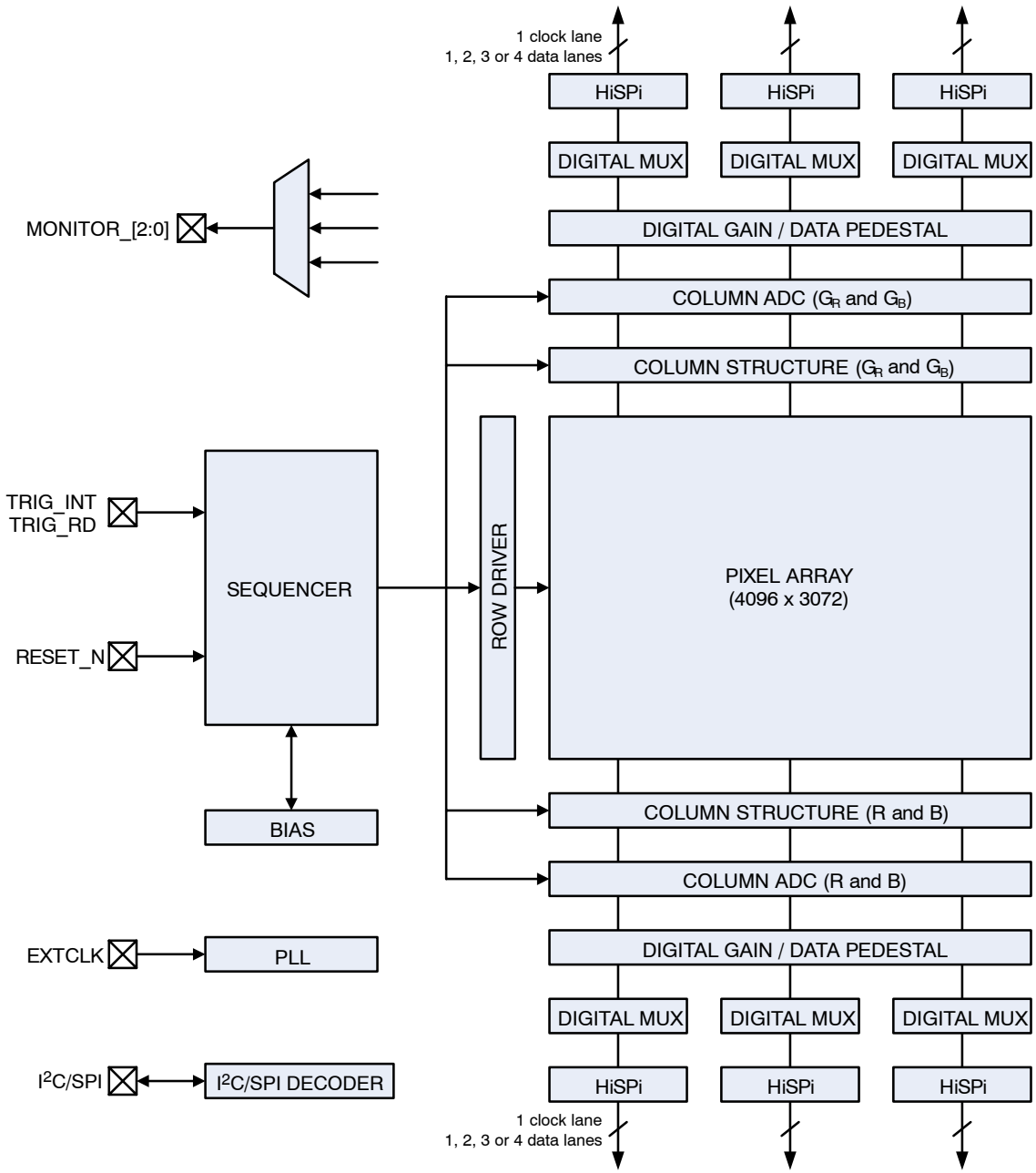


Figure 1. Functional Block Diagram (XGS 12000)

The on−chip logic, programmable through the Two−Wire (I^2C) or Four−Wire (SPI) Serial Interface, generates all internal timing for integration control and frame readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing coarse analog gain) and then through a 12−bit column ADC. The data from the ADCs is first stored in the on−chip column memory bank prior to being processed by the digital data path (which provides additional data processing including digital gain and offset). The digital multiplexer can be configured to reduce the number of active data lanes. The maximum output pixel rate on a single lane is 64.8 Megapixel per second, corresponding to a clock rate of 32.4 MHz.

Advanced trigger functions enable synchronization to external events (triggered master and slave mode) but also allow synchronizing image readout with the host (receiver) on a frame or line basis (triggered frame or line readout). The sensor supports configuration of up to eight independent ROIs and up to three register configurations (*contexts*) can be programmed and sequentially applied (frame by frame) with a single command over the control interface.

Refer to Figure 1 for the functional blocks described hereafter.

- Two−Wire Serial Interface (I^2C)
  I^2C−compatible, two−wire serial interface enables user interaction with sensor.
- (Four−Wire) Serial Peripheral Interface (SPI)
  The Four−Wire serial interface can be used as an alternative to the two−wire interface. The SPI enables faster sensor (re−)configuration compared to the two−wire serial interface.
- EXTCLK
  The nominal input−clock frequency is 32.4 MHz. This clock serves as the base clock for the derived clock domains required by the internal sub−blocks and HiSPi output interface.
- Phase−locked Loop (PLL)
  The on−chip phase−locked loop generates all the internal system clocks, including the HiSPi clock.
- Bias Generator
  The bias generator generates the required reference currents used by the on−chip blocks.
- Sequencer
  The sequencer generates the sensor timing and controls the image core which contains all pixels, driving and readout circuits. It controls the ADC circuits and provides the necessary information to the digital data path. The sequencer operating and readout modes (ROI readout, subsampling...) can be configured through the SPI interface. The readout parameters are synchronized to frame boundaries to support dynamic reconfiguration without generating any corrupted images.
- Row Driver
  The row drivers generate the reset and select signals used to operate the pixel array.
- Monitor Pins
  The sequencer can communicate its internal states through the monitor output pins.
- Column Structure
  The column structure contains the analog circuits necessary to ensure a proper transfer of the signal to the column ADC. This structure includes the column amplifiers which can be used to apply analog gain to the signal before these are converted by the ADCs. The sensor supports analog gain of 1x, 2x and 4x. The analog gain is applied globally to all pixels.
- Column ADC
  For each column, a 12−bit ADC converts the analog signal into a digital value.
- Digital Gain
  A linear, digital gain ranging from 1/32x up to 2x can be configured separately for each color channel in steps of 1/32.
- Data Pedestal
  This block adds a user programmable, per color channel digital offset to the pixel values.
- Digital Mux
  This block handles the lane multiplexing which can be used to reduce the number of output lanes.
- HiSPi
  The 24 HiSPi lanes are laid out in six identical HiSPi blocks. Each block consists of four data lanes and one clock lane. The number of active data lanes (1, 2, 3 or 4) depends on the selected multiplex mode.

PIXEL DATA FORMAT

PIXEL ARRAY STRUCTURE

The XGS 12000 active pixel array consists of 4096 columns by 3072 rows of optically active pixels. The active resolution of XGS 8000 and XGS 9600 can be found in Table 1. As shown in Figures 2 through 4, the active array is surrounded by a four−pixel wide collar of interpolation pixels for color interpolation purposes. The entire active array (including interpolation pixels) is isolated from the black reference pixels by a collar of dummy pixels. The purpose of these dummy pixels is to improve the image uniformity within the active area. The complete pixel array, including all dummy, black and interpolation pixels, consists of a total of 4176 columns and 3102 rows (2190 rows for XGS 8000). The sensor's active pixel array is shown with the first pixel in the bottom left corner (refer to Figures 2 through 4).

The color version of the sensor has a Bayer Color Filter Array (CFA) placed on top of the pixels. The mapping of the CFA with respect to the active pixel array is shown in Figure 2 through 4.

PIXEL ARRAY READOUT

The electrical black reference lines are read out at the start of every frame. The number of lines to be read out is configurable through the M lines configuration (configurable for each context). The ROI configurations are processed after the black reference lines. The lines accessible through the window configurations are limited to the active area region, including interpolation rows. Note that the windows are configured in logical kernel addresses. A kernel contains four image lines and the kernel with logical address 0 corresponds to the lines with physical addresses:

– 15:18 for XGS 12000 and XGS 9400

– 471:474 for XGS 8000

Each window configuration consists of two parameters: a start address and window height. The configured windows are reordered such that the ROI with the smallest start address is read out first. After completion of the readout of the first ROI, the line address pointer will be initialized to the start address of the next ROI. For overlapping windows, the sequencer will just continue the readout. Note that the overlapping part is read out only once.

Lines are read out from left to right and each line contains different types of pixels. A line starts with 4 dummy pixels followed by 24 electrical black reference pixels. The regular image pixels are preceded and followed by 4 dummy pixels. Dummy pixels are identical to the regular pixels, but may deviate in performance. Therefore the dummy pixels should be discarded. Each line is ended by another 32 black reference pixels followed by 4 dummy pixels.

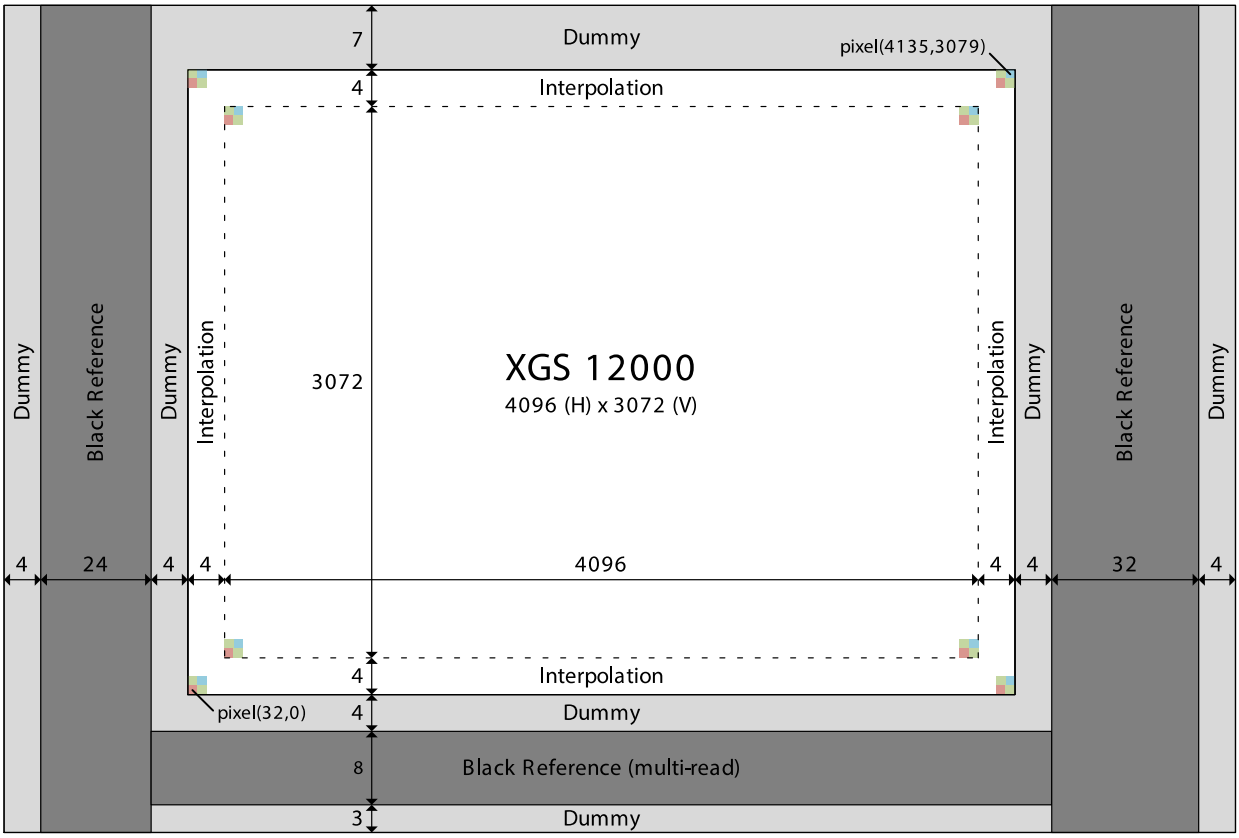


Figure 2. XGS 12000 Pixel Array

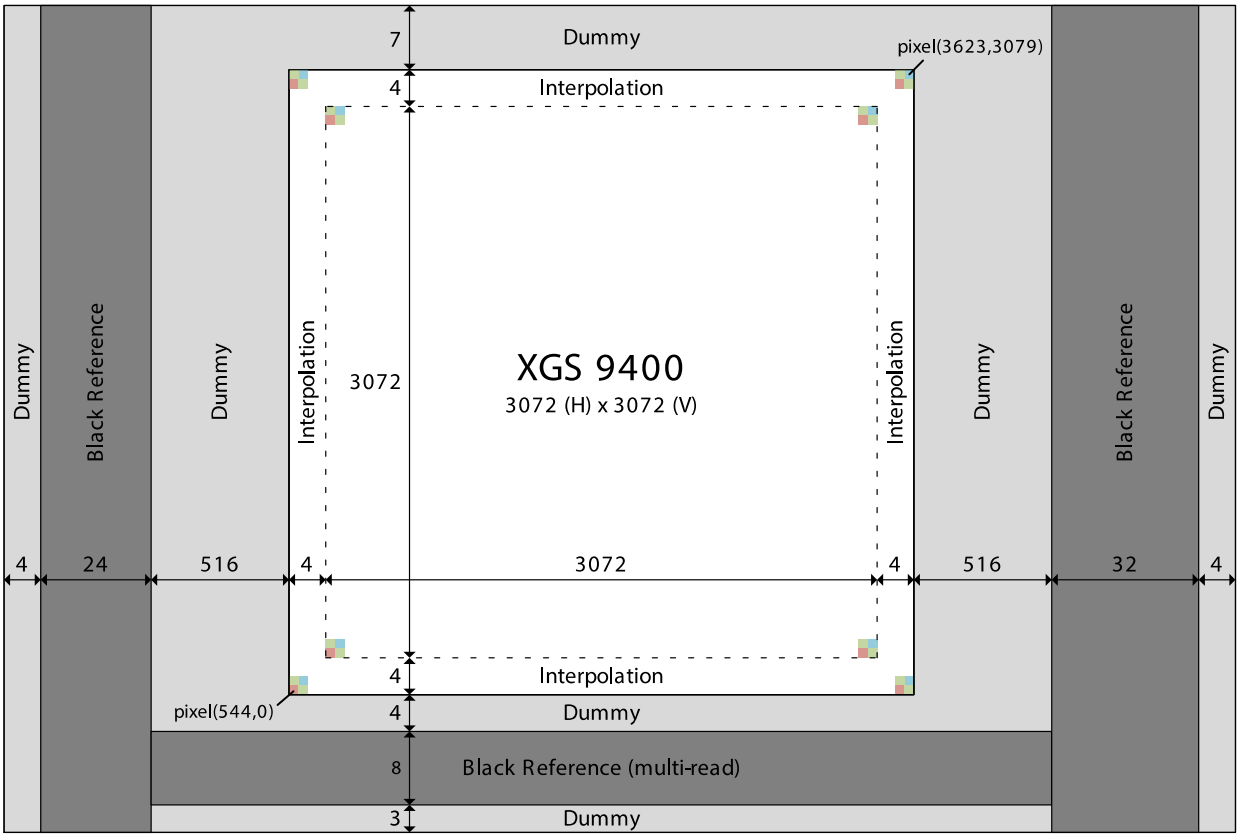


Figure 3. XGS 9400 Pixel Array

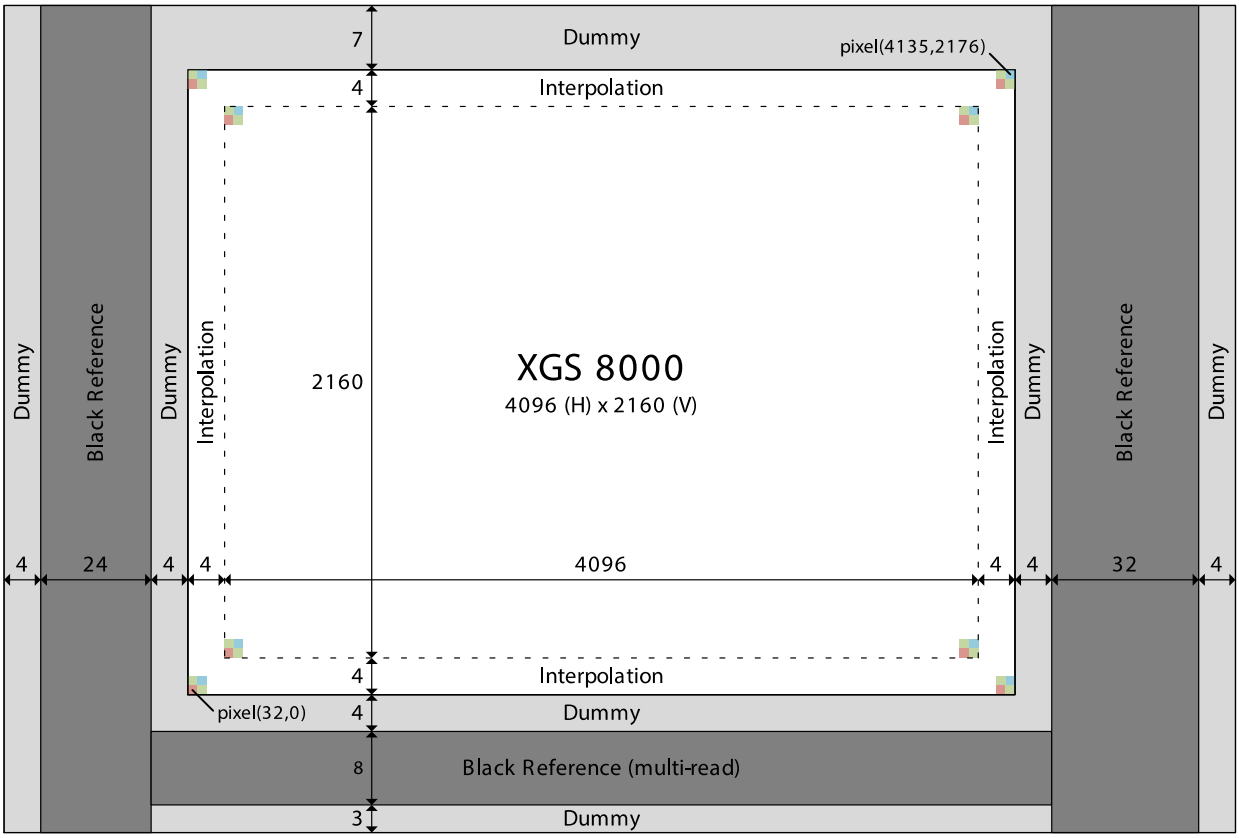


Figure 4. XGS 8000 Pixel Array

Readout Order

Frame readout starts by setting the read address to the first row of the configured ROI. Once the row is read, the read address is incremented and the next row is read. This cycle continues until the last row of the ROI has been read. The incremental addressing scheme is depicted in Figure 5.

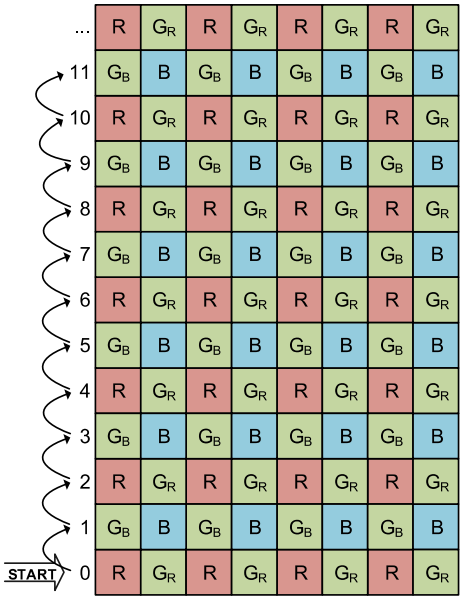


Figure 5. Incremental Row Addressing Sequence

Subsampled Readout

During subsampled readout only a subset of the pixel array is read out, enabling faster read out with the same field of view but at the expense of reduced image resolution. In order to support subsampling on both monochrome and color sensors, XGS supports two different subsampling schemes:

1. Read One Skip One
   In this mode, one out of four pixels is selected for readout by selecting every other line and column in the image array. The Read−One−Skip−One mode is depicted in Figure 6 below. This subsampling mode does not preserve the Bayer pattern so it is recommended for monochrome devices only.

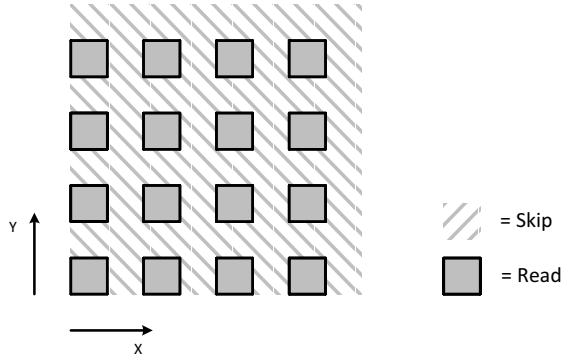


Figure 6. Monochrome Subsampling (Read−1−Skip−1)

2. Read Two Skip Two
   The Read−Two−Skip−Two subsampling scheme is recommended for color sensors as it preserves the Bayer pattern. When using the Read−Two−Skip−Two scheme, the sensor first reads two rows and then skips two rows. From each row being read, first two adjacent pixels will be read, then two will be skipped. This readout scheme is depicted in Figure 7.

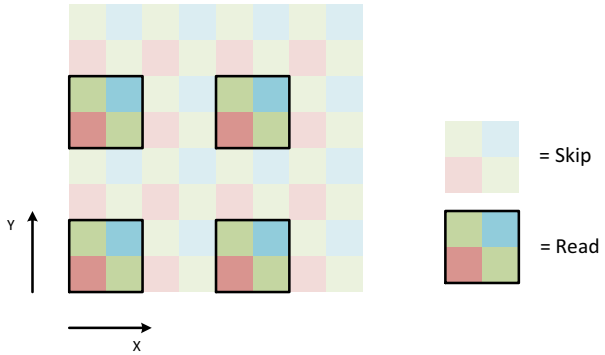


Figure 7. Color Subsampling (Read−2−Skip−2)

Reverse Readout

XGS supports reverse readout in the vertical (Y−) direction. If *active_config_reg.active_reversed* is set to 1, the ROIs will be read top to bottom instead of the default (*active_config_reg.active_reversed* = 0) bottom to top readout direction.

CONFIGURATION AND PINOUT

TYPICAL CONFIGURATIONS

Two possible configuration examples are depicted in the figures below. The first example (Figure 8) uses the Four−Wire Serial Interface while the second example (Figure 9) depicts a typical Two−Wire Serial Interface implementation. Pin connections to (and from) the sensor and power supply configurations are shown in the figures below. The recommended decoupling capacitors are listed in Table 4.

Configuration Example:

- V_{DD}_SLVS = 1.2 V (or 0.4 V); V_{DD} = 1.2 V; V_{DD}_IO = 2.8 V (or 1.8 V); V_{DD}_PLL = 2.8 V;
- V_{AA} = 2.8 V; V_{AA}_PIX = 3.0 V; V_{AA}_RD = 3.0 V; V_{AA}_PIX_BST = 3.0 V
- 24 data lanes + 2 clock lanes

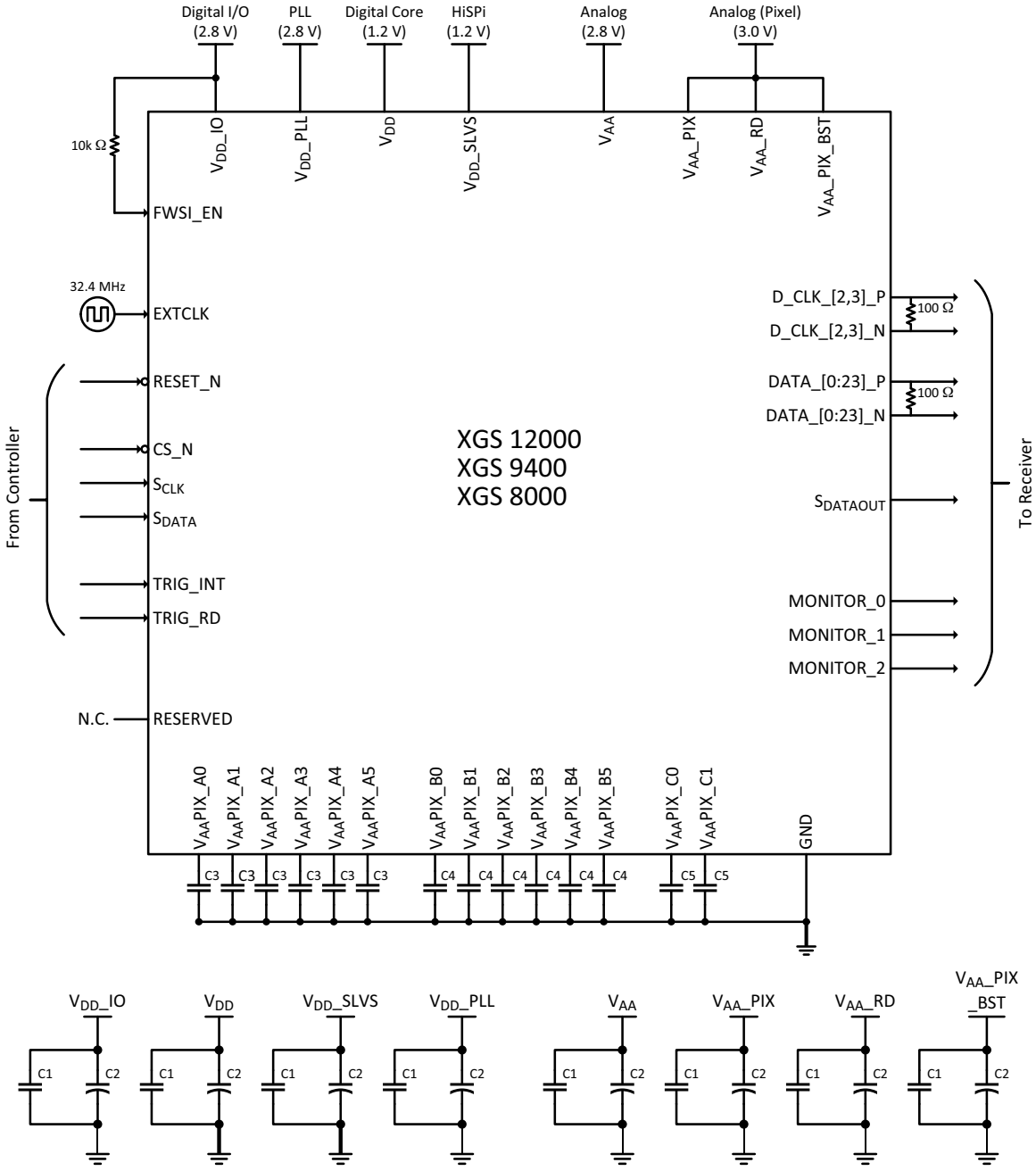


Figure 8. Typical Configuration (Four−Wire Serial Interface)

1. All power supplies must be adequately decoupled (see Table 4) Decoupling.
2. In this example, only 2 (out of 6) HiSPi clock lanes are used; D_CLK_2 to sample data on the even data lanes (top readout) and D_CLK_3 to sample data on the odd data lanes (bottom readout).
3. The active HiSPi lanes need to be terminated using 100 Ω resistors placed as close to the receiver as possible.
4. Unused HiSPi outputs (data and/or clock lanes) must be left floating.
5. It is highly recommended to route the monitor signals to the receiver (FPGA) for debugging purposes. If the MONITOR outputs are not used, they must be left floating.
6. If the TRIGGER inputs are not used, tie them to GND.
7. No distinction is made between analog and digital ground (internally shorted).
8. FWSI_EN must be connected to V_{DD}_IO through a 10 kΩ resistor (enable Four−Wire Serial Interface).
9. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.
10. Digital inputs RESET_N and CS_N are both active low.

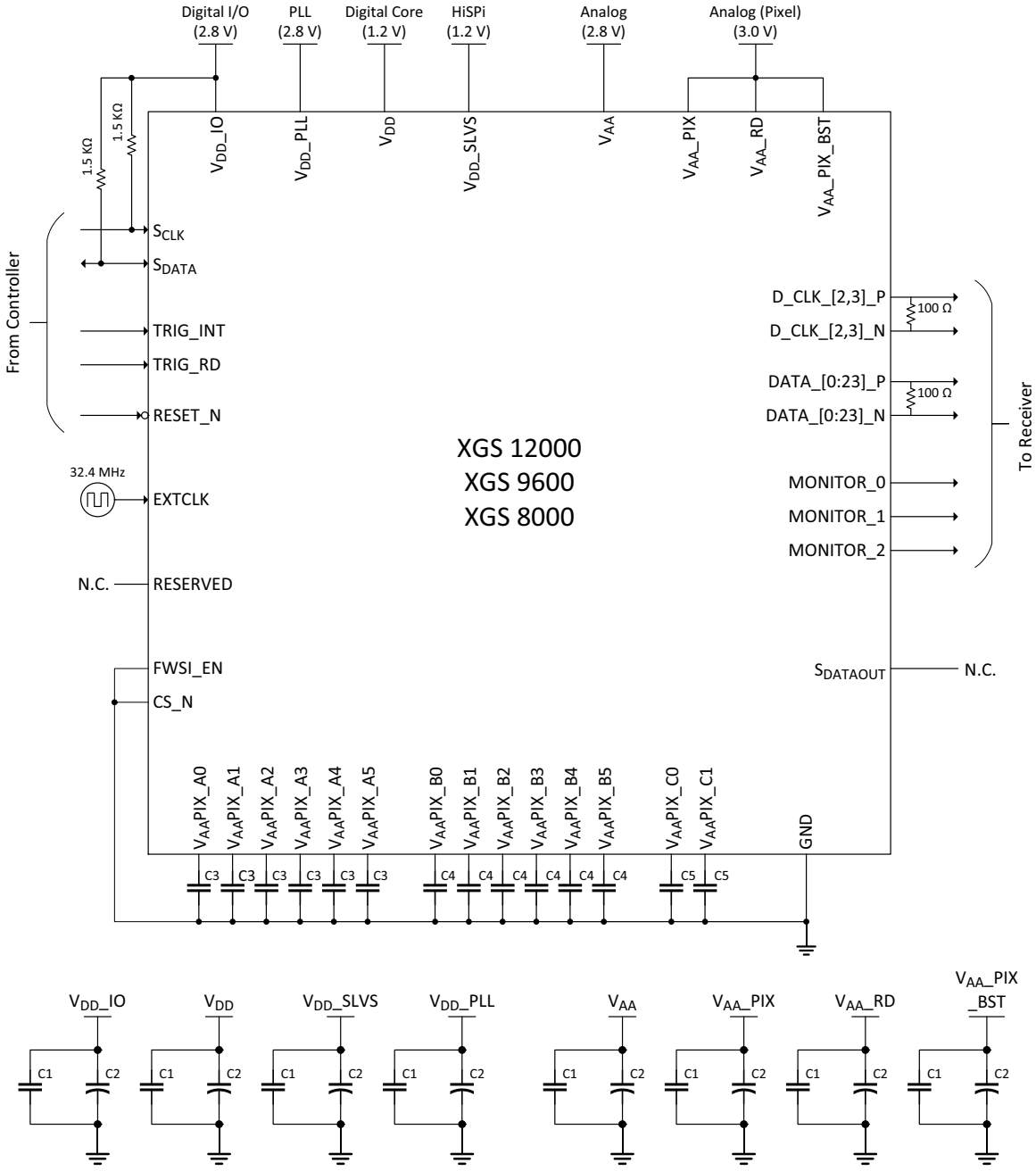


Figure 9. Typical Configuration (Two−Wire Serial Interface)

1. All power supplies must be adequately decoupled (see Table 4) Decoupling.
2. In this example, only 2 (out of 6) HiSPi clock lanes are used; D_CLK_2 to sample data on the even data lanes (top readout) and D_CLK_3 to sample data on the odd data lanes (bottom readout).
3. The active HiSPi lanes need to be terminated using 100 Ω resistors placed as close to the receiver as possible.
4. Unused HiSPi outputs (data and/or clock lanes) must be left floating.
5. It is highly recommended to route the monitor signals to the receiver (FPGA) for debugging purposes. If the MONITOR outputs are not used, they must be left floating.
6. If the TRIGGER inputs are not used, tie them to GND.
7. No distinction is made between analog and digital ground (internally shorted).
8. FWSI_EN and CS_N must be tied to GND when using the Two−Wire Serial Interface. $S_{dataout}$ can be left floating.
9. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.
10. Digital input RESET_N is active low.
11. ON Semiconductor recommends using a 1.5 kΩ pull−up resistor to V_{DD}_IO on both Sclk and Sdata.

Table 4. DECOUPLING RECOMMENDATIONS

Capacitor	Recommended Capacitor Value (μF)	Capacitor	Recommended Capacitor Value (μF)
C1, C5	0.1	C3	0.1 + 4.7
C2	10	C4	0.1 + 2.2

PINOUT

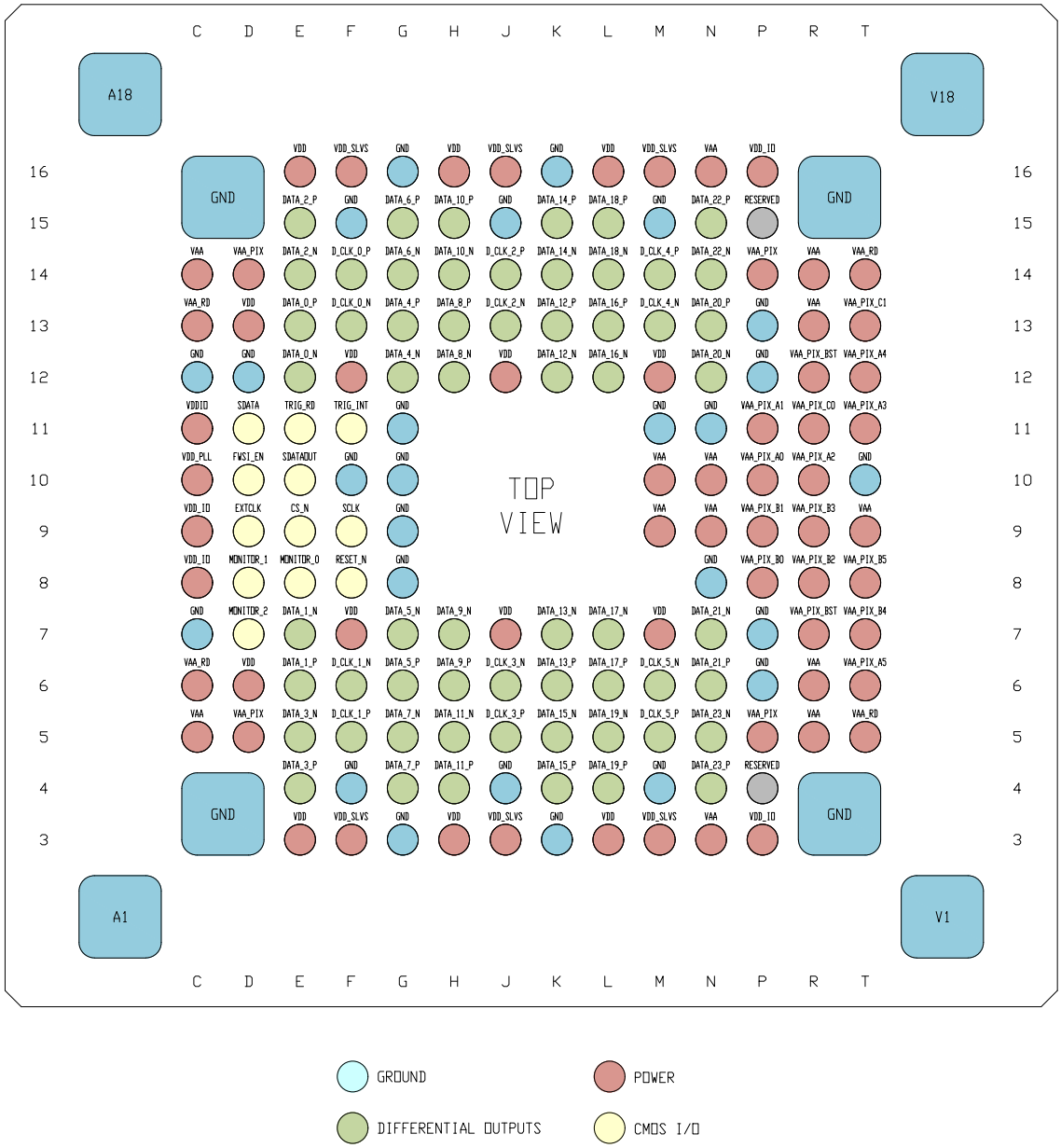


Figure 10. XGS CLGA Package Pinout (Top View; Pads Down)

PIN LIST

Table 5. PIN DESCRIPTIONS (163−PIN LGA PACKAGE)

Name	LGA Pin Name	Type	Description
GND	A1, A18, C3, C7, C12, C16, F4, F15, G3, G16, J4, J15, K3, K16, M4, M11, M15, N8, N11, P7, P12, T3, T10, T16, V1, V18, D12, F10, G8, G9, G10, G11, P6, P13	Ground	Ground
V_{DD}_PLL	C10	Power	PLL Power Supply
V_{AA}	C5, C14, M9, M10, N3, N9, N10, N16, R5, R6, R13, R14, T9	Power	Analog Supply
V_{AA}_RD	C6, C13, T5, T14	Power	Analog Supply for Row Driver
V_{DD}_IO	C8, C9, C11, P3, P16	Power	I/O Supply
FWSI_EN	D10	Input	'HIGH' −> Four−Wire Serial Interface (SPI) 'LOW' −> Two−Wire Serial Interface (I^2C)
S_{DATA}	D11	Input/ Output	Four−Wire Serial Interface (SPI): SPI Slave In Two−Wire Serial Interface (I^2C): Serial Data Input/ Output
V_{AA}_PIX	D5, D14, P5, P14	Power	Pixel Supply
V_{DD}	D6, D13, E3, E16, F7, F12, H3, H16, J7, J12, L3, L16, M7, M12	Power	Digital Supply
MONITOR_2	D7	Output	Monitor Output 2. If unused, do not connect.
MONITOR_1	D8	Output	Monitor Output 1. If unused, do not connect.
EXTCLK	D9	Input	External Clock Input
$S_{DATAOUT}$	E10	Output	Four−Wire Serial Interface (SPI): SPI Slave Out Two−Wire Serial Interface (I^2C): Do not connect
TRIG_RD	E11	Input	Trigger Input for Readout Control. If unused, connect to ground.
DATA_0_N	E12	HiSPi	Differential Data Channel [0], Negative
DATA_0_P	E13	HiSPi	Differential Data Channel [0], Positive
DATA_2_N	E14	HiSPi	Differential Data Channel [2], Negative
DATA_2_P	E15	HiSPi	Differential Data Channel [2], Positive
DATA_3_P	E4	HiSPi	Differential Data Channel [3], Positive
DATA_3_N	E5	HiSPi	Differential Data Channel [3], Negative
DATA_1_P	E6	HiSPi	Differential Data Channel [1], Positive
DATA_1_N	E7	HiSPi	Differential Data Channel [1], Negative
MONITOR_0	E8	Output	Monitor Output 0. If unused do not connect.
CS_N	E9	Input	Four−Wire Serial Interface (SPI): SPI Chip Select (active low) Two−Wire Serial Interface (I^2C): Connect to GND
TRIG_INT	F11	Input	Trigger Input for Integration Control. If unused, connect to ground.
D_CLK_0_N	F13	HiSPi	Differential Clock [0], Negative
D_CLK_0_P	F14	HiSPi	Differential Clock [0], Positive
V_{DD}_SLVS	F3, F16, J3, J16, M3, M16	Power	HiSPi Supply
D_CLK_1_P	F5	HiSPi	Differential Clock [1], Positive
D_CLK_1_N	F6	HiSPi	Differential Clock [1], Negative
RESET_N	F8	Input	Asynchronous Hard Reset (Active Low)
S_{CLK}	F9	Input	Serial Interface Clock Input

Table 5. PIN DESCRIPTIONS (163−PIN LGA PACKAGE)

Name	LGA Pin Name	Type	Description
DATA_4_N	G12	HiSPi	Differential Data Channel [4], Negative
DATA_4_P	G13	HiSPi	Differential Data Channel [4], Positive
DATA_6_N	G14	HiSPi	Differential Data Channel [6], Negative
DATA_6_P	G15	HiSPi	Differential Data Channel [6], Positive
DATA_7_P	G4	HiSPi	Differential Data Channel [7], Positive
DATA_7_N	G5	HiSPi	Differential Data Channel [7], Negative
DATA_5_P	G6	HiSPi	Differential Data Channel [5], Positive
DATA_5_N	G7	HiSPi	Differential Data Channel [5], Negative
DATA_8_N	H12	HiSPi	Differential Data Channel [8], Negative
DATA_8_P	H13	HiSPi	Differential Data Channel [8], Positive
DATA_10_N	H14	HiSPi	Differential Data Channel [10], Negative
DATA_10_P	H15	HiSPi	Differential Data Channel [10], Positive
DATA_11_P	H4	HiSPi	Differential Data Channel [11], Positive
DATA_11_N	H5	HiSPi	Differential Data Channel [11], Negative
DATA_9_P	H6	HiSPi	Differential Data Channel [9], Positive
DATA_9_N	H7	HiSPi	Differential Data Channel [9], Negative
D_CLK_2_N	J13	HiSPi	Differential Clock [2], Negative
D_CLK_2_P	J14	HiSPi	Differential Clock [2], Positive
D_CLK_3_P	J5	HiSPi	Differential Clock [3], Positive
D_CLK_3_N	J6	HiSPi	Differential Clock [3], Negative
DATA_12_N	K12	HiSPi	Differential Data Channel [12], Negative
DATA_12_P	K13	HiSPi	Differential Data Channel [12], Positive
DATA_14_N	K14	HiSPi	Differential Data Channel [14], Negative
DATA_14_P	K15	HiSPi	Differential Data Channel [14], Positive
DATA_15_P	K4	HiSPi	Differential Data Channel [15], Positive
DATA_15_N	K5	HiSPi	Differential Data Channel [15], Negative
DATA_13_P	K6	HiSPi	Differential Data Channel [13], Positive
DATA_13_N	K7	HiSPi	Differential Data Channel [13], Negative
DATA_16_N	L12	HiSPi	Differential Data Channel [16], Negative
DATA_16_P	L13	HiSPi	Differential Data Channel [16], Positive
DATA_18_N	L14	HiSPi	Differential Data Channel [18], Negative
DATA_18_P	L15	HiSPi	Differential Data Channel [18], Positive
DATA_19_P	L4	HiSPi	Differential Data Channel [19], Positive
DATA_19_N	L5	HiSPi	Differential Data Channel [19], Negative
DATA_17_P	L6	HiSPi	Differential Data Channel [17], Positive
DATA_17_N	L7	HiSPi	Differential Data Channel [17], Negative
D_CLK_4_N	M13	HiSPi	Differential Clock [4], Negative
D_CLK_4_P	M14	HiSPi	Differential Clock [4], Positive
D_CLK_5_P	M5	HiSPi	Differential Clock [5], Positive
D_CLK_5_N	M6	HiSPi	Differential Clock [5], Negative
DATA_20_N	N12	HiSPi	Differential Data Channel [20], Negative
DATA_20_P	N13	HiSPi	Differential Data Channel [20], Positive

Table 5. PIN DESCRIPTIONS (163−PIN LGA PACKAGE)

Name	LGA Pin Name	Type	Description
DATA_22_N	N14	HiSPi	Differential Data Channel [22], Negative
DATA_22_P	N15	HiSPi	Differential Data Channel [22], Positive
DATA_23_P	N4	HiSPi	Differential Data Channel [23], Positive
DATA_23_N	N5	HiSPi	Differential Data Channel [23], Negative
DATA_21_P	N6	HiSPi	Differential Data Channel [21], Positive
DATA_21_N	N7	HiSPi	Differential Data Channel [21], Negative
V_{AA}_PIX_A0	P10	Decoupling	External Noise Decoupling (0.1 μF + 4.7 μF to GND)
V_{AA}_PIX_A1	P11	Decoupling	External Noise Decoupling (0.1 μF + 4.7 μF to GND)
V_{AA}_PIX_A2	R10	Decoupling	External Noise Decoupling (0.1 μF + 4.7 μF to GND)
V_{AA}_PIX_A3	T11	Decoupling	External Noise Decoupling (0.1 μF + 4.7 μF to GND)
V_{AA}_PIX_A4	T12	Decoupling	External Noise Decoupling (0.1 μF + 4.7 μF to GND)
V_{AA}_PIX_A5	T6	Decoupling	External Noise Decoupling (0.1 μF + 4.7 μF to GND)
V_{AA}_PIX_B0	P8	Decoupling	External Noise Decoupling (0.1 μF + 2.2 μF to GND)
V_{AA}_PIX_B1	P9	Decoupling	External Noise Decoupling (0.1 μF + 2.2 μF to GND)
V_{AA}_PIX_B2	R8	Decoupling	External Noise Decoupling (0.1 μF + 2.2 μF to GND)
V_{AA}_PIX_B3	R9	Decoupling	External Noise Decoupling (0.1 μF + 2.2 μF to GND)
V_{AA}_PIX_B4	T7	Decoupling	External Noise Decoupling (0.1 μF + 2.2 μF to GND)
V_{AA}_PIX_B5	T8	Decoupling	External Noise Decoupling (0.1 μF + 2.2 μF to GND)
V_{AA}_PIX_C0	R11	Decoupling	External Noise Decoupling (0.1 μF to GND)
V_{AA}_PIX_C1	T13	Decoupling	External Noise Decoupling (0.1 μF to GND)
V_{AA}_PIX_BST	R7, R12	Power	Pixel Booster Supply
RESERVED	P4, P15	N/A	Reserved (do not connect)

SENSOR STATES

After Power−Up and while the RESET_N pin is driven low, the image sensor enters a RESET state until the RESET_N signal is de−asserted.

Once the RESET_N pin is driven high, the sensor will start loading the default configuration, stored in the on−chip memory, into its configuration registers. As soon as *sensor_status_reg (R0x3706)* returns value *0xEB*, the sensor passed all basic initialization steps and, while waiting for user interaction, enters a SLEEP state. While the sensor is in the SLEEP state, the registers can be programmed using the serial interface. To exit the SLEEP state and enter STANDBY mode, the *reset_register_reg (R0x3700)* needs to be set to *0x001C*. This register upload enables all analog blocks (including the on−chip PLL) and moves the sensor state to STANDBY.

When in STANDBY mode and upon user intervention the training patterns or IDLE words can be sent over the video interface allowing receiver locking. Once the host is ready to receive image data, the sensor's sequencer can be enabled. Depending on the configured operation mode, the sensor will either wait for user interaction or start grabbing images autonomously (CAPTURE). Disabling the sequencer moves the sensor state back to STANDBY. When disabling the PLL and analog blocks while in STANDBY state, the state machine will transition back to the SLEEP state. Asserting the RESET_N pin forces the sensor to enter the RESET state, regardless of the current state.

The sensor state diagram is shown in Figure 11.

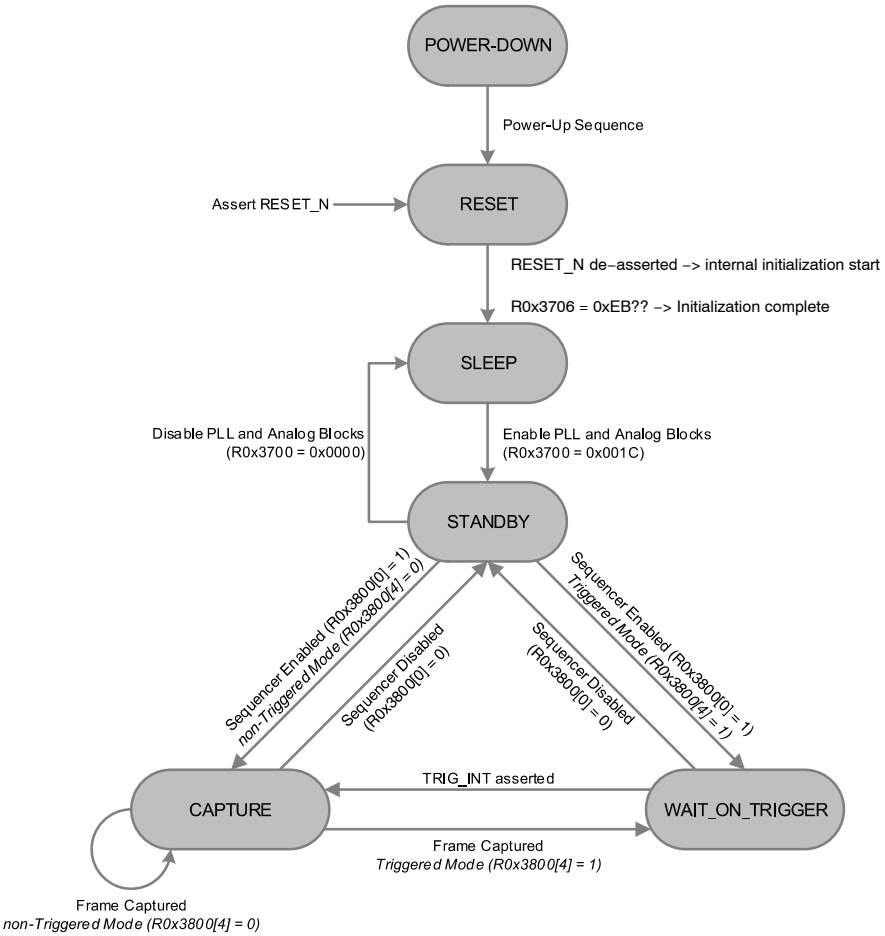


Figure 11. Sensor State Diagram

Table 6. TYPICAL TRANSITION TIMES

Sensor State	Transition Time	Description
POWER−DOWN	25 ms	Time required to transition from POWER−DOWN to CAPTURE state.
SLEEP	10 ms	Time required to transition from SLEEP to CAPTURE state.
STANDBY	< 16 line times	Time required to transition from STANDBY to CAPTURE state.
WAIT_ON_TRIGGER	2 line times + Synchroniza-tion Delay (< 50 ns)	Time required to transition from WAIT_ON_TRIGGER to CAPTURE (upon trigger action). A minimum delay of one line time will be added.

POWER−UP AND POWER−DOWN SEQUENCE

POWER−UP SEQUENCE

The recommended Power−Up sequence for the XGS sensor is shown in Figure 12. The available power supplies (V_{DD}_IO, V_{DD}_PLL, V_{DD}, V_{AA}, V_{AA}_PIX, V_{AA}_PIX_BST, V_{AA}_RD and V_{DD}_SLVS) must have the separation specified below.

1. Turn on V_{DD}_IO power supply.
2. After 0−100 μs, turn on V_{DD}_PLL power supply.
3. After 0−100 μs, turn on V_{DD} power supply.
4. After 0−100 μs, turn on V_{AA} power supply.
5. Once V_{AA} is stable, power up V_{AA}_PIX, V_{AA}_PIX_BST and V_{AA}_RD.
6. Once V_{AA}_PIX, V_{AA}_PIX_BST and V_{AA}_RD are stable, power up V_{DD}_SLVS.
7. After V_{DD}_SLVS is stable, enable EXTCLK.
8. After EXTCLK has settled, hold RESET_N low (active) for at least 30 EXTCLK cycles before de−asserting the reset signal.
9. The sensor then loads the default register values from its on−chip memory. As soon as RESET_N is pulled up (released), the sensor starts loading the default register values from it internal memory. When loading is done (*sensor_status_reg R0x3706 −> 0xEB*), the sensor is ready to accept user uploads. the sensor is ready to accept user uploads (e.g. to configure a special mode).
10. Enable PLL and initialize sensor's internal analog blocks (*reset_register_reg = 0x001C*).
11. Once the analog blocks are initialized, the sensor transitions to STANDBY state and is ready to start image operations.
12. Enable the sequencer to transition to the CAPTURE state (*general_config0_reg[0] = 1*).

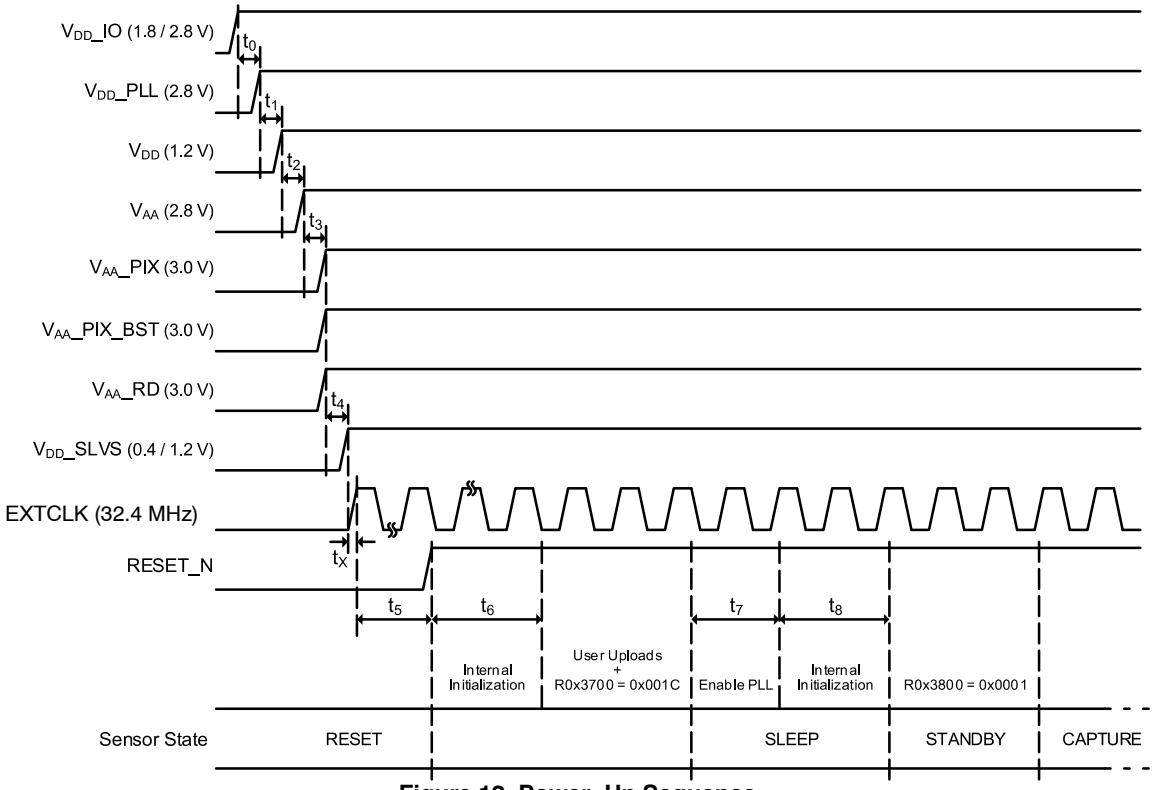


Figure 12. Power−Up Sequence

Table 7. POWER−UP SEQUENCE

Symbol	Definition	Min	Typ	Max	Unit
t_0	V_{DD}_IO to V_{DD}_PLL	0 (Note 5)	100		μs
t_1	V_{DD}_PLL to V_{DD}	0 (Note 5)	100		μs
t_2	V_{DD} to V_{AA}	0 (Note 5)	100		μs
t_3	V_{AA} to V_{AA}_PIX/V_{AA}_PIX_BST/V_{AA}_RD	0 (Note 5)	100		μs
t_4	V_{AA}_PIX/V_{AA}_PIX_BST/V_{AA}_RD to V_{DD}_SLVS	0 (Note 5)	100		μs
t_X	EXTCLK Settling Time	0.5	30 (Note 4)		ms
t_5	Hard Reset	30			EXTCLK cycles
t_6	Internal Initialization (ready once R0x3706 reads back 0xEB)	1.5			ms
t_7	PLL Lock Time	10	70		μs
t_8	Internal Initialization		6.5		ms

4. The EXTCLK settling time is component−dependent.
5. The minimum time does not include the settling time of the power supply.

POWER−DOWN SEQUENCE

The recommended Power−Down sequence for the XGS sensor is shown in Figure 13. The available power supplies must have the separation specified below.

1. Disable CAPTURE if output is active by disabling the sequencer (*general_config0_reg[0] = 0*).
2. Issue a sensor STANDBY request (*reset_register_reg[2] = 0*). By default, the transition to STANDBY state happens either after completion of current row (or frame) readout or instantly (configurable).
3. In STANDBY mode, activate reset by pulling down the RESET_N line for at least 30 EXTCLKs.
4. EXTCLK can be stopped 0.5 ms after RESET_N.
5. Turn off power supplies one by one. Wait at least until the supplies are stable before turning off the next supply. (reverse order of Power−Up Sequence).

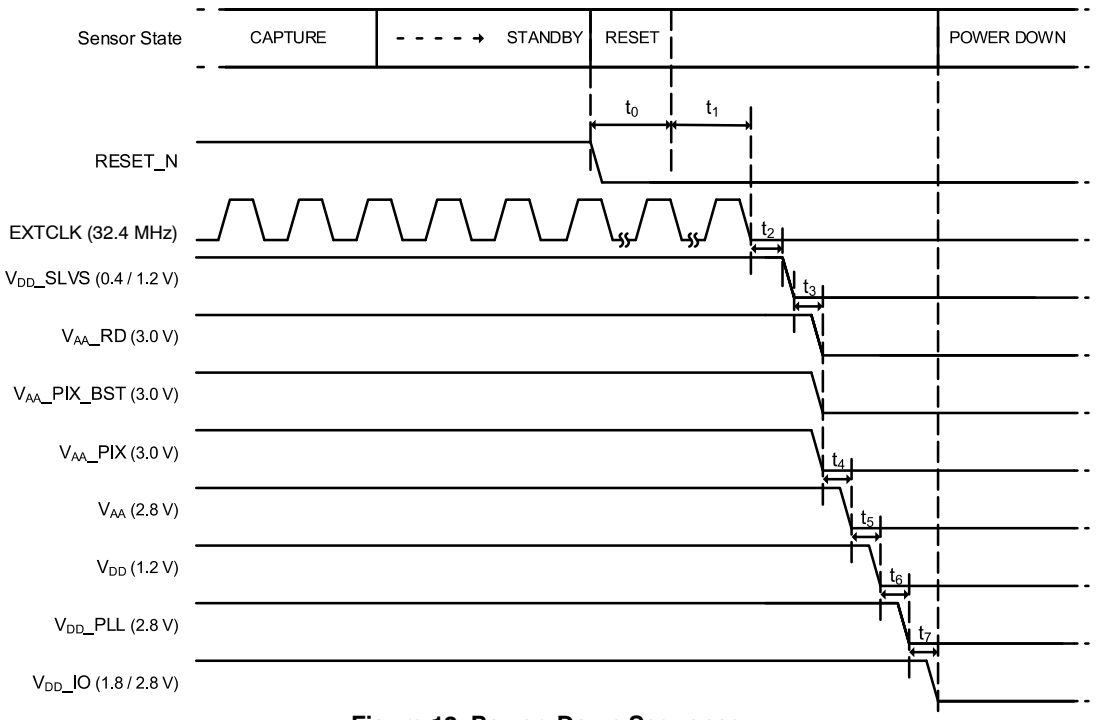


Figure 13. Power−Down Sequence

Table 8. POWER−DOWN SEQUENCE

Symbol	Definition	Min	Typ	Max	Unit
t_0	Hard Reset	30			EXTCLK cycles
t_1	Reset to Disable EXTCLK	0.5			ms
t_2	V_{AA}_RD / V_{AA}_PIX_BST / V_{AA}_PIX to V_{AA}	0 (Note 6)			µs
t_3	V_{DD}_SLVS to V_{AA}_RD / V_{AA}_PIX_BST / V_{AA}_PIX	0 (Note 6)			µs
t_4	V_{AA}_RD / V_{AA}_PIX_BST / V_{AA}_PIX to V_{AA}	0 (Note 6)			µs
t_5	V_{AA} to V_{DD}	0 (Note 6)			µs
t_6	V_{DD} to V_{DD}_PLL	0 (Note 6)			µs
t_7	V_{DD}_PLL to V_{DD}_IO	0 (Note 6)			µs

6. The minimum time does not include the settling time of the power supply.

INTEGRATION MODES

In a global shutter sensor, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 14 shows the integration and readout sequence for the global shutter. All pixels are light sensitive during the same period of time.

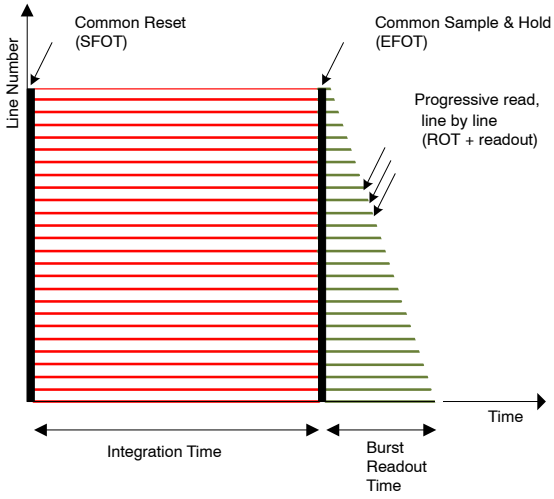


Figure 14. Global Shutter Operation

The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled at the same time on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that Figure 14 shows a configuration where integration and readout operations are not pipelined. In a pipelined configuration, integration and readout are performed simultaneously.

Pipelined Global Shutter Mode

In pipelined shutter mode, the integration and readout are active concurrently. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead time (EFOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the Frame Overhead Time, the sensor is read out line per line. Image array operations and readout are pipelined. The image array operations are performed in the Row Overhead Time (ROT). During the ROT sequence, an image row is selected for readout.

At the start of the integration the sequencer schedules another global operation on the pixel array. This sequence is referred to as Start of integration frame overhead sequence (SFOT). During this SFOT, the readout shall be halted temporarily.

MASTER MODE (NON−TRIGGERED)

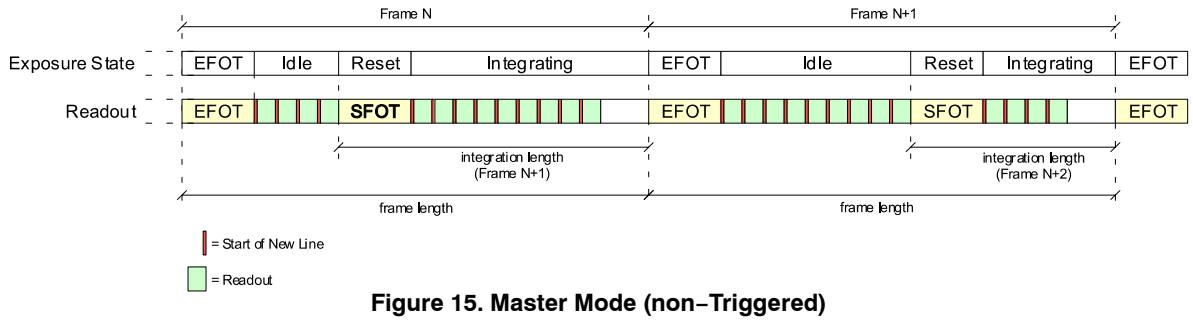


Figure 15. Master Mode (non−Triggered)

In this operation mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction as shown in Figure 15.

On a high level, the frame time consists of a non−integrating time and integration time (during which the pixels are light sensitive and integrating light). The sum of both parameters is the frame time, which is configured in multiple of line periods. Within this total frame time, the Sequencer schedules the frame operations required to initiate and terminate the light integration. The integration period is started with a Start−of−Integration FOT (SFOT) sequence and is ended with an End−of−Integration FOT (EFOT) sequence. Note that both SFOT and EFOT operations take some time during which the readout will be halted. This will be reflected in an idle period on the sensor's interface. The parameters defining the frame and integration properties are listed in Table 9 below.

Table 9. INTEGRATION AND FRAME TIMING PARAMETERS

Name	Description
line_time	Duration of one line, expressed in logic clock cycles. The minimum line time shall be dictated by the A/D conversion time and readout time (whichever is larger).
frame_length	Defines the total frame time as frame_length * line_time logic clock periods. This parameter needs to be configured large enough such that both the integration control operations (i.e. SFOT, EFOT and configured integration time) and the readout operations (ROI readout + black lines) can happen.
integration_coarse	Defines the coarse part of the integration time. Total integration time in logic clock periods is integration_coarse * line_time + integration_fine
integration_fine	Defines the fine part of the integration time. Total integration time in logic clock periods is integration_coarse * line_time + integration_fine
integration_offset_coarse	Offset between the Sequencer induced SFOT period and the start of the SFOT, expressed in line periods. The total integration offset time, expressed in logic clock cycles, is defined as (integration_offset_coarse + overhead) * line_time. This parameter allows to increase the latency between a trigger event and the effective start of integration in triggered modes.

The frame parameters and their relations are depicted in Figure 16 below. Note that the green area depicts the readout of regular lines (black reference / ROI defined image lines), while the grey area represents the access to dummy lines (no image data). The shaded green part represents the line periods during which the control and datapath pipeline is flushed.

Minimum integration time limitations are listed in Table 10.

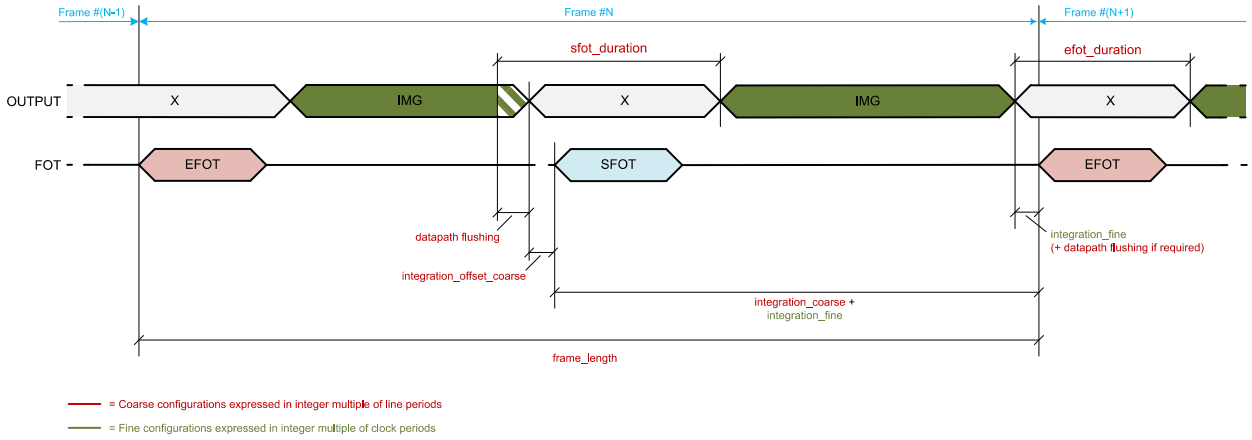


Figure 16. Frame Timing and Exposure Parameters

MASTER MODE (TRIGGERED)

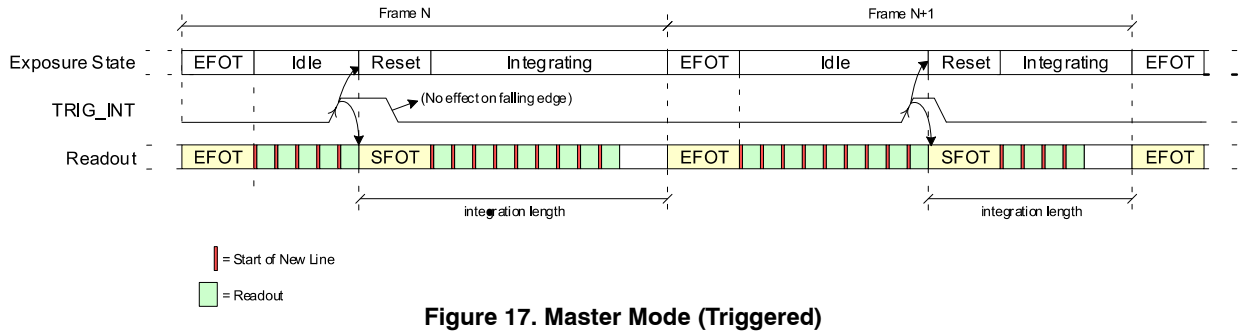


Figure 17. Master Mode (Triggered)

In Triggered Master Mode, a rising edge on the TRIG_INT pin is used to trigger the start of integration as shown in Figure 17. The integration time is defined by register configuration (*integration_coarse*, *integration_fine*). The sensor shall autonomously integrate during this predefined time, after which the EFOT operation starts and the image array is read out sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge.

Figure 18 below shows the pipelined operation in triggered master mode (i.e. trigger assertion during frame readout).

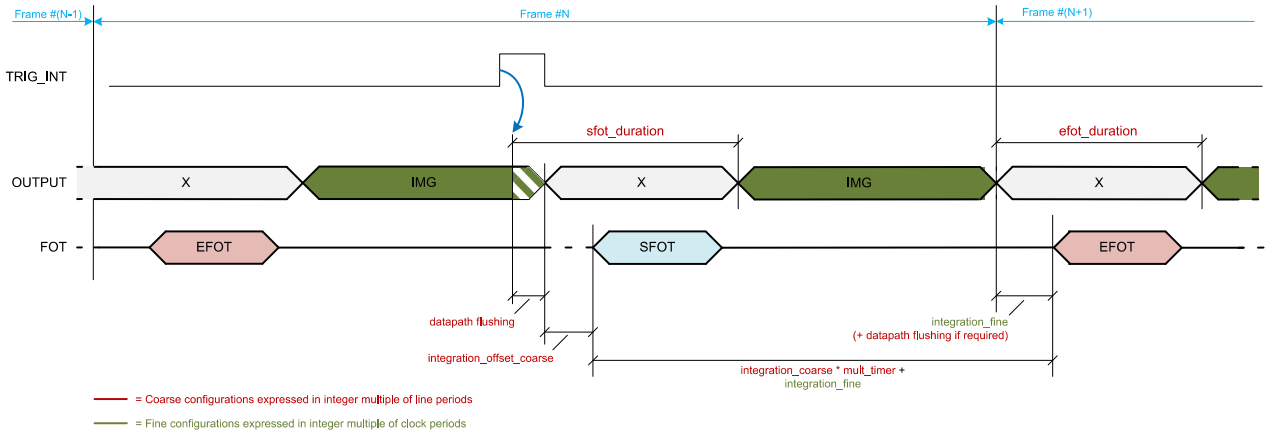


Figure 18. Integration Control in Triggered Master Mode

Note that each trigger reads out only one image.

The latency between a trigger event and the start of the SFOT operation is constant and predictable. It is defined by the coarse offset configuration + overhead.

NOTES:

- The trigger is an asynchronous signal which is synchronized in the SCU. As a consequence, synchronization jitter can be observed.
- The polarity of the TRIG_INT pin is controlled by *trig_int_polarity*. The operation described above corresponds to *trig_int _polarity* = ‘0’.
- The response time between a rising edge of TRIG_INT and the start of integration is fixed, besides the synchronization uncertainty and jitter.

The following register is not used in this mode and has no influence (implicitly defined by the trigger):

- *frame_length*

Minimum integration time limitations are listed in Table 10.

SLAVE MODE (TRIGGERED)

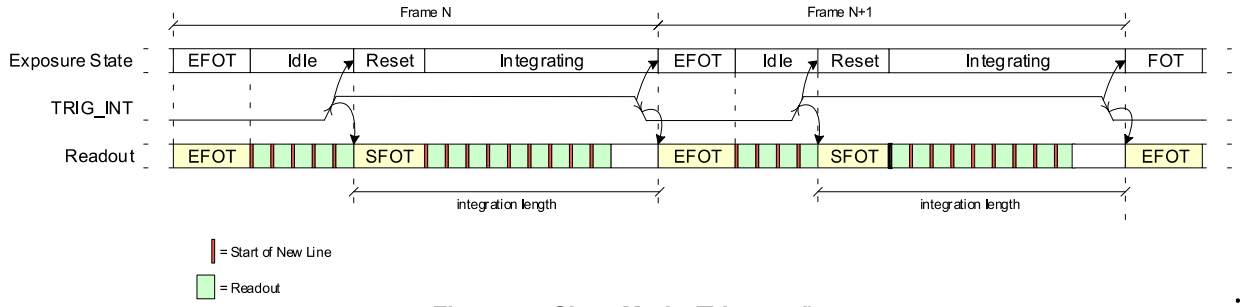


Figure 19. Slave Mode (Triggered)

The slave mode depicted in Figure 19 adds more manual control to the sensor. The integration time registers (*frame_length* and *integration*) are ignored in this mode and the integration time is rather controlled by an external pin. As soon as the control pin is asserted, the Sequencer schedules the SFOT operations. The integration continues until the external pin is deasserted by the user/system. Now, the image is sampled and the readout is initiated.

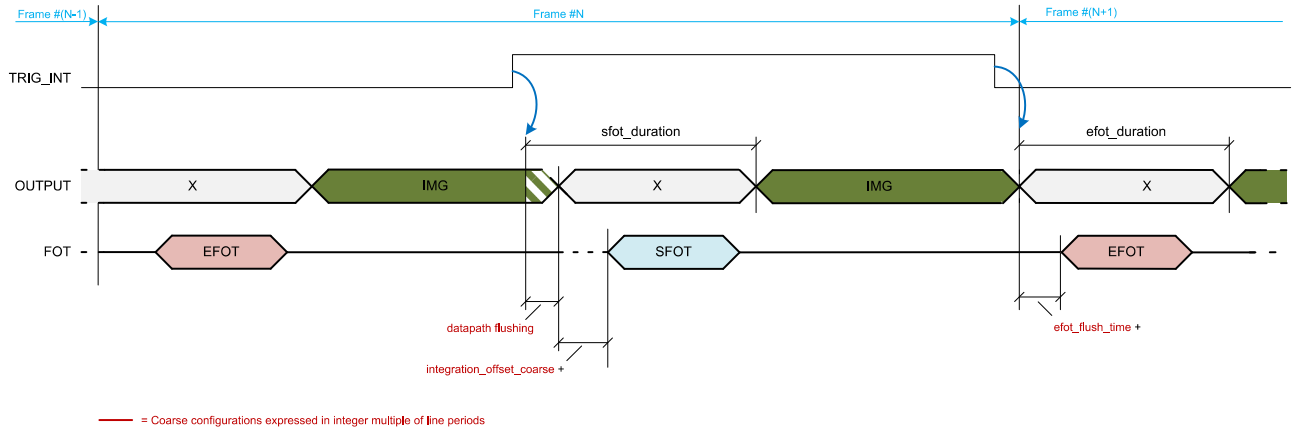


Figure 20. Integration Control in Slave Mode (Triggered)

The latency between the trigger events and the SFOT/EFOT operations respectively is fixed and predictable. The latency between a trigger assertion and the SFOT operation is controlled through *integration_offset_coarse*.

NOTES:

- The trigger is an asynchronous signal which is synchronized in the Sequencer. As a consequence, synchronization jitter can be observed.
- The response time between a TRIG_INT event and the start/end of integration shall be constant, besides the synchronization uncertainty and jitter.
- The following registers are not used in this mode and do not have any influence (implicitly defined by the trigger):
  - *integration_coarse*,
  - *integration_fine*,
  - *frame_length*

  Minimum integration time limitations are listed in Table 10 below.

Table 10. MINIMUM INTEGRATION TIME LIMITATIONS (Note 7)

Number of Output Lanes	Minimum Integration Time (in μs)	
	Non−Triggered	Triggered
6	10	60
12	10	30
24	10	20

7. The minimum integration time depends on the configured line time. The values in this table assume the minimum recommended line time is used.
8. Refer to the XGS 12000 Developer Guide for more information on the minimum integration times.

READOUT MODES

By default, the readout of the pixel array does not require any user interaction. The sequencer initiates the readout as soon as integration ends and the entire readout is done autonomously. This is the default readout mode.

Optionally, the frame readout can be controlled externally. This requires configuring the TRIG_RD input as a frame or line trigger. Table 11 below lists the parameters that control the triggered readout operation.

Table 11. TRIGGERED READOUT PARAMETERS

Register Name	Description
frame_trigger_en	Start the frame readout upon assertion of TRIG_RD when enabled. This configuration has priority over line_trigger_en.
frame_trigger_mode	Only valid for frame triggered readout modes. '0': Regular frame triggered mode: The sensor starts the readout of one frame upon a rising trigger edge '1': The sequencer continues frame grabbing as long as the trigger is asserted.
line_trigger_en	Start the readout of one line upon assertion of TRIG_RD when enabled. Only one line is read out for each trigger assertion.

Note that *contexts_reg.frames* determines how many frames can be read out. This implies that the sequencer will not accept any new trigger once the number of *contexts_reg.frames* have been read out. If this is not desired, frames should be configured to 0.

FRAME TRIGGERED READOUT

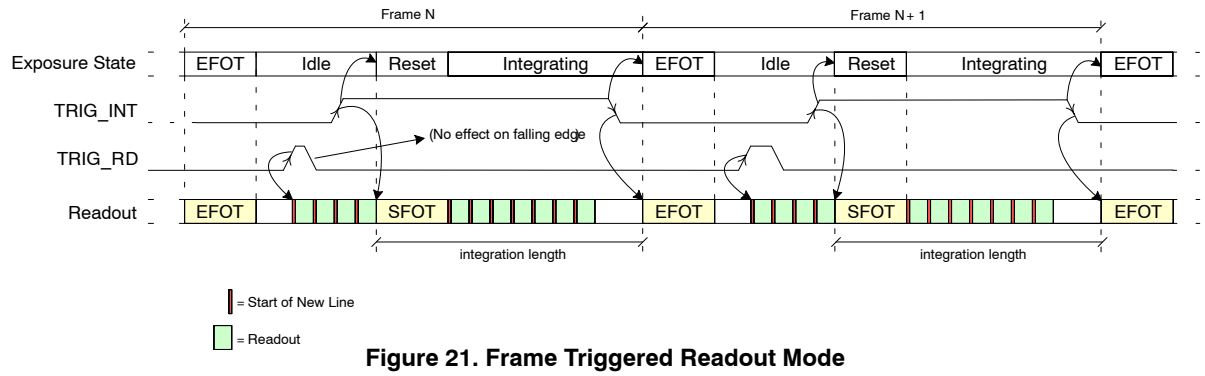


Figure 21. Frame Triggered Readout Mode

XGS 12000 supports two frame triggered readout options, configurable in the *frame_trigger_mode* register (refer to Table 11).

frame_trigger_mode = 0

In a global shutter mode, the integration is ended by the EFOT. In a non−triggered readout mode, the readout is initiated automatically after the EFOT operations. In frame triggered mode, the Sequencer will not start the readout, but instead it waits until the frame−trigger gets asserted. Once an event (rising of falling depending on the configured polarity) is detected the readout starts and the image is read out line after line.

Note that the trigger assertion is latched and served at the first coming internal new line reference (internal time base). As a consequence one may observe a trigger latency up to a line time.

Frame triggered readout can be combined with triggered integration modes.

frame_trigger_mode = 1

In this mode, the trigger acts as an external sequencer enable signal. An event (rising or falling depending on the configured polarity) starts the frame readout. After this first frame, the sequencer continues running, cycling through the active contexts, if more than one context is enabled. The end condition depends on the value given in *contexts_reg.frames*:

- *contexts_reg.frame*s > 0: The Sequencer continues running and reads out the given amount of frames, after which it returns to the WAIT_ON_TRIGGER state. After the readout, the sequencer is waiting for another trigger, after which a new sequence is initiated. Note that a new batch of frames shall be read out in case the trigger is asserted at the end of the previous batch.
- *contexts_reg.frames* = 0: The Sequencer continues running as long as the TRIG_RD is asserted. Once the trigger is deasserted, the Sequencer returns to the

WAIT_ON_TRIGGER state, in which it is ready to accept a new trigger event.

Note that this mode is available for both triggered and non−triggered global shutter modes and it can be combined with the use of multiple contexts. When using multiple contexts it is also possible to configure the number of desired frames per context. The sequencer cycles through the active contexts and generates as many frames as configured per context. When retriggered, the sequencer reinitializes the frame properties and starts the readout from a fresh state (i.e. does not continue from where it ended in the previous batch).

LINE TRIGGERED READOUT

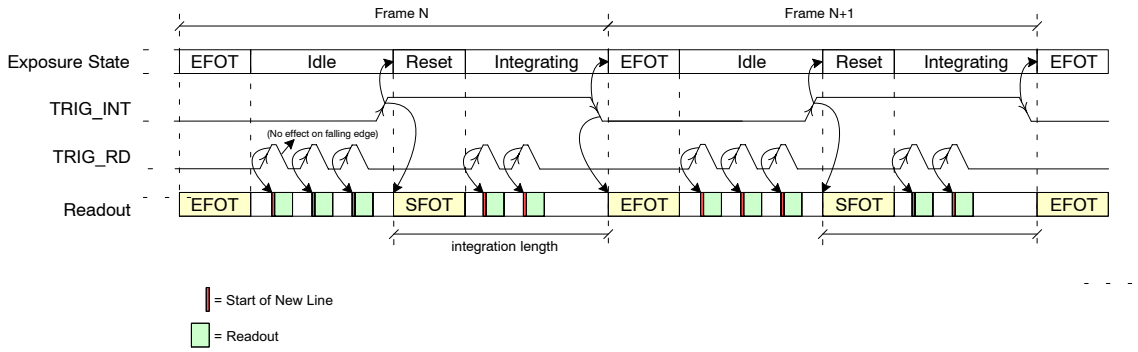


Figure 22. Line Triggered Readout

The line triggered readout mode is enabled when *line_trigger_en* is asserted and *frame_trigger_en* is deasserted. The line triggered readout mode is comparable to frame triggered readout, but in this mode only one line is read out for each trigger. Note that a trigger is latched and interpreted during the following line period if the sensor is retriggered during readout.

Line triggered readout is to be used in conjunction with triggered integration modes.

Features Overview

The XGS family has a wide array of features to enhance functionality or to increase versatility. A summary of features follows.

RESET

The RESET_N input (pin F8) is an active low control input for asynchronous hard reset. During the power−up period, RESET_N must be asserted, then must be deasserted after the power supplies are settled. The minimum RESET_N assert time is 30 EXTCLK cycles.

MONITOR OUTPUTS

The XGS sequencer provides three monitor outputs (pins E8, D8 and D7) which can be used to monitor the internal states of the sequencer. The monitor signals can be configured separately for each monitor output.

CONTEXT SWITCHING

XGS supports up to three contexts which allow the user to program a number of configurations and let the sensor cycle through these. Switching from one context to another is done at the start of a frame and cannot corrupt the ongoing readout. The registers that control the switching are grouped in the *contexts_reg*. The active context switching can be done manually by changing the value in the *active_contexts* register or the sequencer can take control. If programmed, the sequencer will cycle through two or three contexts sequentially as depicted in Figures 23 and 24.

- Two Context Switching
  (*context_reg.active_contexts* = 0x3)
  context 0 → context 1 → context 0...

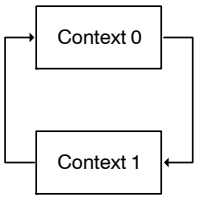


Figure 23. Two Context Switching

- Three Context Switching
  (*context_reg.active_contexts* = 0x7)
  context 0 → context 1 → context 2 → context 0...

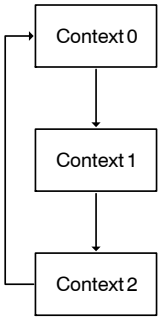


Figure 24. Three Context Switching

- Multiple Frame Context Switching
  In addition to defining up to three contexts, the number

of frames per context can be configured for each context separately. In the example configuration depicted in Figure 25, the sensor first generates three frames using *context 0* settings followed by a single *context 1* frame and two *context 2* frames. The sensor loops through this sequence until the sequencer is disabled. The number of frames per context switch is configured in *contexts_reg.frames_ctxt0* (for context0).

3 x context 0 → context 1 → 2 x context 2 → 3 x context 0...

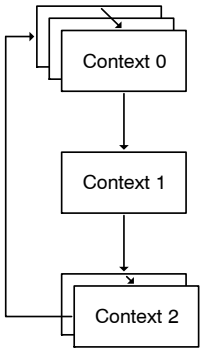


Figure 25. Multiple Frame Context Switching

TEST PATTERN

The XGS sensor has the capability of injecting a number of test patterns into the datapath. As the test pattern generator is placed at the beginning of the digital datapath, it can be used to check the functions of the digital blocks or to test the frame grabber or receiver operation. The test patterns can be configured in the *test_pattern_mode_reg.test_pattern_mode* and only one pattern can be activated at a given point in time.

DATA PEDESTAL

The data pedestal is a constant offset that is added to the pixel values at the end of the datapath. The pedestal or offset value can be configured separately for each color channel (G_R, G_B, R and B) and for each context. The offset is a 12−bit value.

GAIN STAGES

Analog Gain

A column−based analog gain of 1x, 2x or 4x can be applied to the output signal.

Digital Gain

As opposed to the analog gain stage, the digital gain can be configured to separate levels for each color channel (G_R, G_B, R and B). The digital gain factor ranges from 1/32 to 2 in steps of 1/32 (64 steps) and its configuration can be represented by the equation below:

$$\text{Digital gain} = \text{Dg\_factor}/2^5 \qquad \text{(eq. 1)}$$

COMPANDING MODE

The companding mode can be used to compress 12−bit pixel data into 10−bit values. The line time remains the time required to convert a 12−bit ADC sample; gain is only achieved when, due to lane multiplexing, the system becomes I/O limited. In that situation, being able to send out 12−bit pixels using only 10 bits, can be useful to boost the frame rate. When companding mode is enabled, the precision of the digital output is 1 Least Significant Bit (LSB) in the low light area, but towards the upper region, the granularity gradually increases to 2, 4, and 8 LSBs as shown in Figure 26. In all cases the ADC quantization steps will be less than the photon shot noise performance of the pixel.

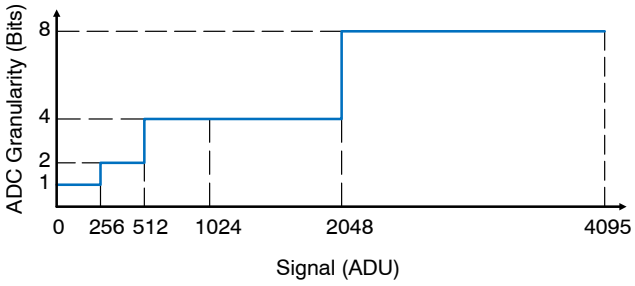


Figure 26. ADC Granularity − Companding Mode

FRAME RATE

Assuming the readout of a frame takes longer than the integration, the frame rate can be influenced by changing one or more of the following parameters:

- Vertical resolution (number of lines in ROI)
- Number of data output lanes (24 / 18 / 12 / 6) or mux mode (4:4 / 4:3 / 4:2 / 4:1)

The frame rate scales linearly with the number of lines (vertical direction) but not with the number of columns (horizontal direction) due to the column ADC architecture. Using the sensor with a reduced number of data lanes will lower the frame rate.

Alternatively, the frame time can be configured through *line_time* and *frame_time*. The line time should be large enough in order to process a full line and the frame time should be configured such that at least all ROIs can be read out and that the maximum integration can be scheduled in. When one of the two conditions are violated the sensor gives either priority to the readout or the integration (*int_priority*).

LANE MULTIPLEXING

The lane multiplexing function can be used to reduce the number of output data lanes and thus the output data rate. This can be useful in case the receiver cannot accept all 24 data lanes or the backend is unable to process the sensor's full data rate. The sensor has one multiplexer for each PHY; six in total. Each multiplexer connects 4 datapath outputs to one PHY and can be configured to distribute the data from the 4 datapath inputs over either 1, 2, 3 or 4 outputs; i.e. the sensor supports 4 multiplexing schemes:

- 4:4 multiplexing: no multiplexing; each datapath lane is connected to a HiSPi lane (total of 24 lanes).
- 4:3 multiplexing: four datapath lanes are multiplexed to three HiSPi lanes (total of 18 lanes).
- 4:2 multiplexing: four datapath lanes are multiplexed to two HiSPi lanes (total of 12 lanes).
- 4:1 multiplexing: four datapath lanes are multiplexed to a single HiSPi lane (total of 6 lanes).

The four different multiplexing schemes are illustrated in Figures 27 to 30. The pixel readout order for each multiplexing mode is depicted in Figures 31 to 34.

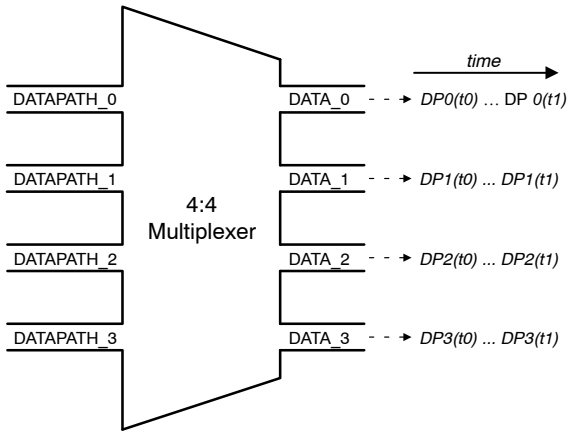


Figure 27. 4:4 Multiplexing (24 Lanes)

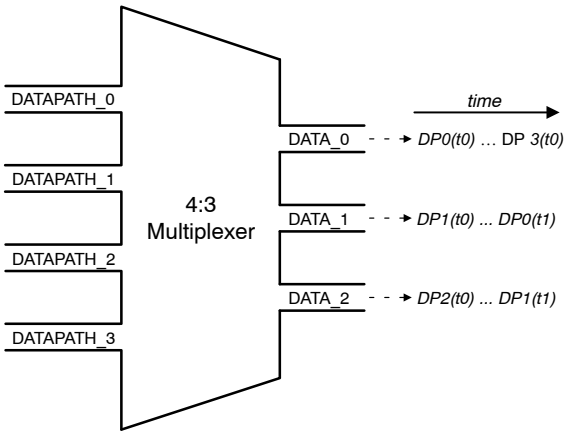


Figure 28. 4:3 Multiplexing (18 Lanes)

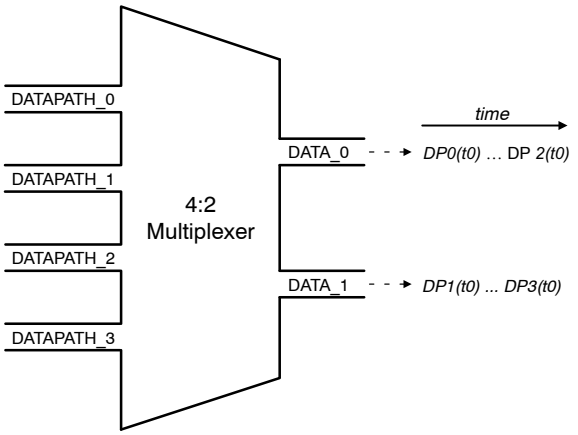


Figure 29. 4:2 Multiplexing (12 Lanes)

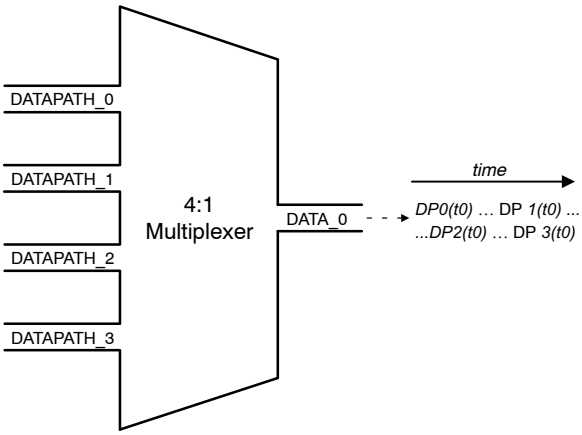


Figure 30. 4:1 Multiplexing (6 Lanes)

Table 14 lists the active data lanes in function of the multiplexing scheme. As depicted in Table 14, HiSPi lane 0 is the lane that is always active, regardless of the selected multiplex scheme.

Table 12. ACTIVE DATA LANES IN PHY0 IN FUNCTION OF MUX MODE

Mux Mode	Lane_0	Lane_2	Lane_4	Lane_6
4:4	X	X	X	X
4:3	X	X	X	
4:2	X	X		
4:1	X			

NOTE: Lane usage is illustrated using the first four lanes only (i.e. for a single PHY).

The data output on each lane within a single PHY, depending on the multiplexing scheme, is represented in Figures 31 to 34. The numbers in the squares represent the actual column address in the pixel array.

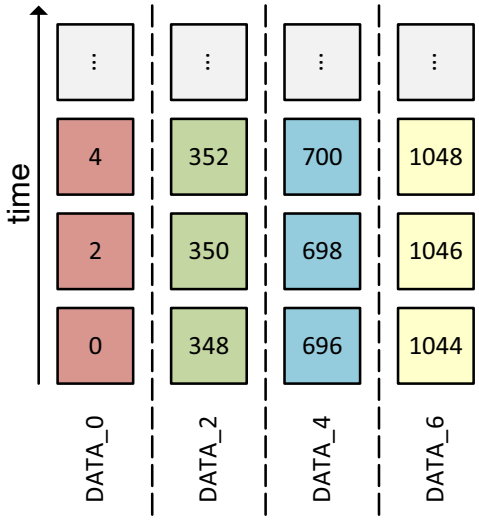


Figure 31. Column Output with 4:4 Multiplexing

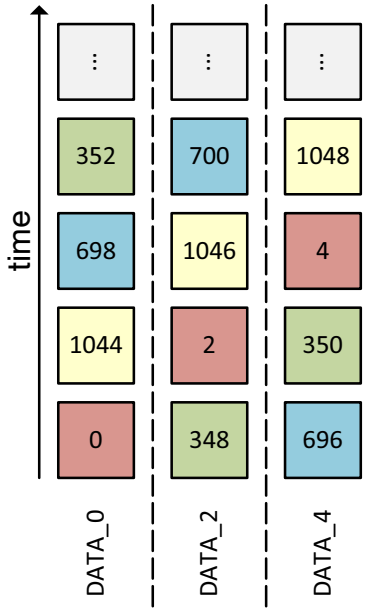


Figure 32. Column Output with 4:3 Multiplexing

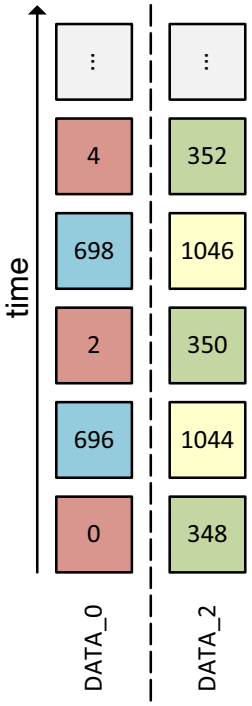


Figure 33. Column Output with 4:2 Multiplexing

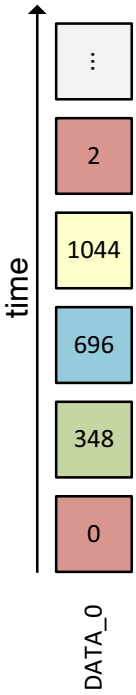


Figure 34. Column Output with 4:1 Multiplexing

Figure 35 shows on which output lane columns are sent in case a row with an even address is read and the sensor is configured to have G_R and G_B pixels sent out on top (even numbered lanes) and R and B pixels to the bottom (odd numbered lanes). Figure 36 shows the column output in case a row with an odd address is read.

EVEN ROW	DATA_0 (G_R)	SYNC	SOF	1, 3, 5··· 345, 347	EOL	BLANK
	DATA_1 (R)	SYNC	SOF	0, 2, 4··· 344, 346	EOL	BLANK
	DATA_2 (G_R)	SYNC	SOF	349, 351, 353··· 693, 695	EOL	BLANK
	DATA_3 (R)	SYNC	SOF	348, 350, 352··· 692, 694	EOL	BLANK
	⋮	⋮	⋮	⋮	⋮	⋮
	DATA_22 (G_R)	SYNC	SOF	··· 4173, 4175	EOL	BLANK
	DATA_23 (R)	SYNC	SOF	··· 4172, 4174	EOL	BLANK

Figure 35. Column Output Sequence (Even Row Address)

ODD ROW	DATA_0 (G_B)	SYNC	SOF	0, 2, 4··· 344, 346	EOL	BLANK
	DATA_1 (B)	SYNC	SOF	1, 3, 5··· 345, 347	EOL	BLANK
	DATA_2 (G_B)	SYNC	SOF	348, 350, 352··· 692, 694	EOL	BLANK
	DATA_3 (B)	SYNC	SOF	349, 351, 353··· 693, 695	EOL	BLANK
	⋮	⋮	⋮	⋮	⋮	⋮
	DATA_22 (G_B)	SYNC	SOF	··· 4172, 4174	EOL	BLANK
	DATA_23 (B)	SYNC	SOF	··· 4173, 4175	EOL	BLANK

Figure 36. Column Output Sequence (Odd Row Address)

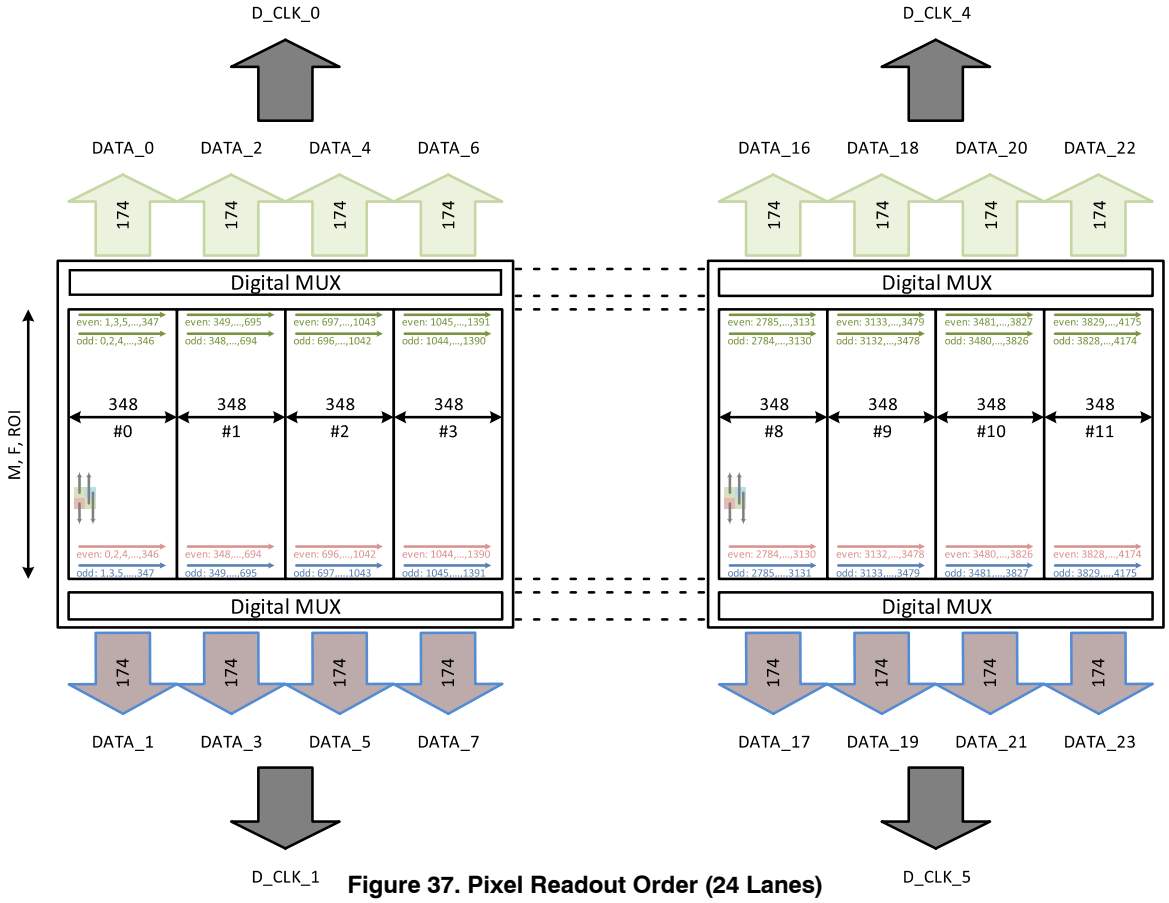


Figure 37. Pixel Readout Order (24 Lanes)

SENSOR CONTROL INTERFACE

The sensor's configuration registers are accessible through either the Two−Wire (I^2C) or Four−Wire (SPI) Serial Interface. At the cost of speed, the two−wire serial interface can be considered as a simple and cost−efficient alternative to the faster, but more complex, four−wire serial interface. The four−wire serial interface is recommended for applications requiring fast and frequent sensor (re−)configuration. As shown in Figure 38 below, the type of user interface can be selected through the external FWSI_EN pin ('LOW' = two−wire, 'HIGH' = four−wire).

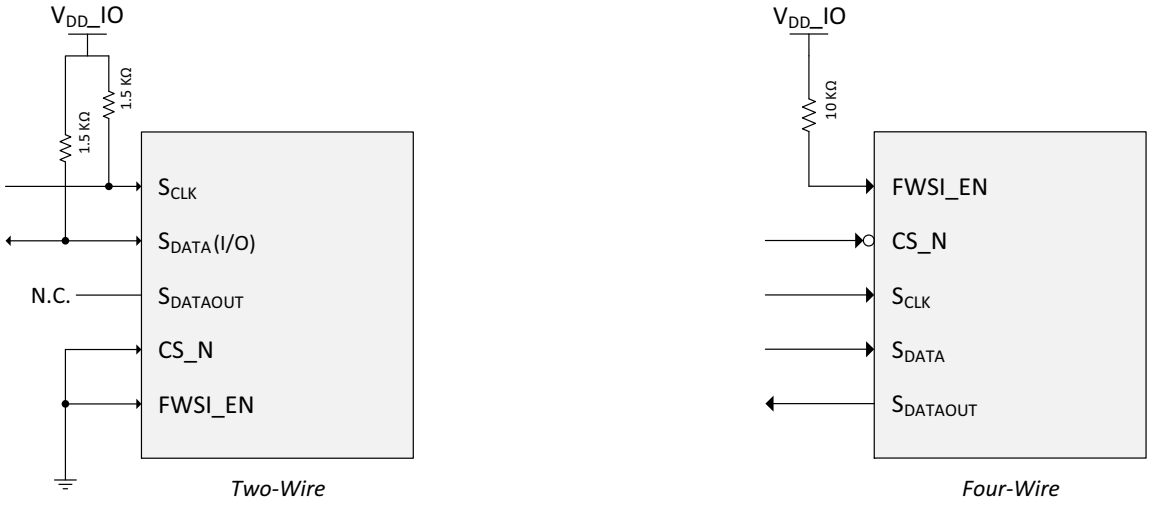


Figure 38. Serial Interface Selection

TWO−WIRE SERIAL INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the sensor.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (S_{CLK}) that is an input to the sensor and is used to synchronize transfers.

Data is transferred between the master and the slave on a bidirectional signal (S_{DATA}). S_{DATA} is pulled up to V_{DD}_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive S_{DATA} LOW − the interface protocol determines which device is allowed to drive S_{DATA} at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive S_{CLK} LOW; the sensor uses S_{CLK} as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements:

- a (repeated) start condition
- a slave address/data direction byte
- an (a no) acknowledge bit
- a message byte
- a stop condition

The bus is idle when both S_{CLK} and S_{DATA} are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on S_{DATA} while S_{CLK} is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a "repeated start" or "restart" condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on S_{DATA} while S_{CLK} is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each S_{CLK} clock period. S_{DATA} can change when S_{CLK} is LOW and must be stable while S_{CLK} is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A '0' in bit [0] indicates a WRITE, and a '1' indicates a READ.

The default slave addresses used by the sensor are 0x20 (write address) and 0x21 (read address).

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the S_{CLK} clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases S_{DATA}. The receiver indicates an acknowledge bit by driving S_{DATA} LOW. As for data transfers, S_{DATA} can change when S_{CLK} is LOW and must be stable while S_{CLK} is HIGH.

No−Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive S_{DATA} LOW during the S_{CLK} clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a ’0’ indicates a write and a ’1’ indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

This sequence (Figure 39) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. Figure 39 shows how the internal register address maintained by the sensor is loaded and incremented as the sequence proceeds.

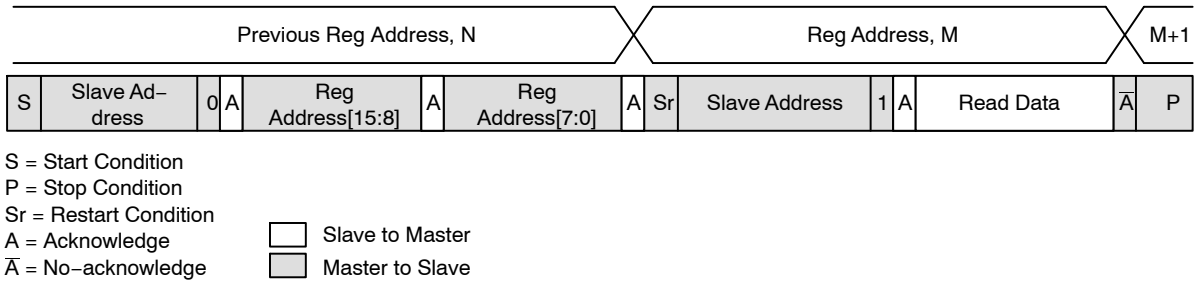


Figure 39. Single READ from Random Location

Single READ from Current Location

This sequence (Figure 40) performs a read using the current value of the sensor’s internal register address. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

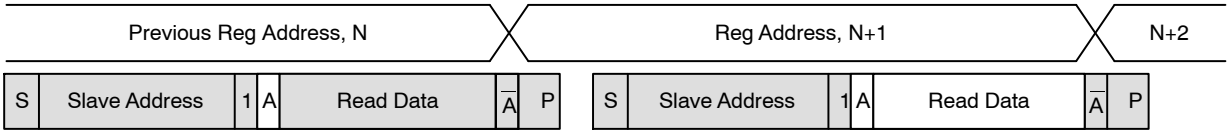


Figure 40. Single READ from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 41) starts in the same way as the single READ from random location (Figure 39). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

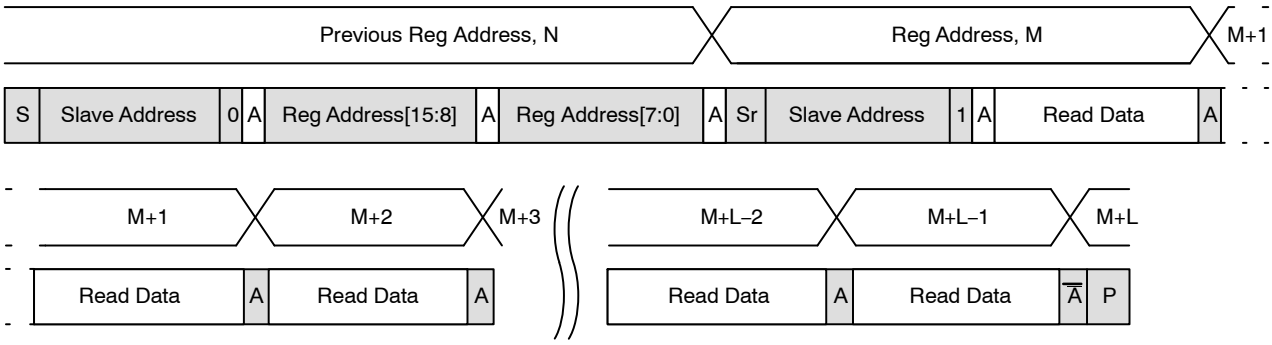


Figure 41. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 42) starts in the same way as the single READ from current location (Figure 40). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READS until ‘L’ bytes have been read.

Figure 42. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 43) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

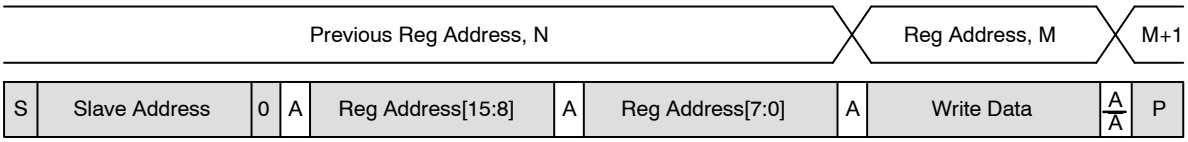


Figure 43. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 44) starts in the same way as the single WRITE to random location (Figure 43). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until ‘L’ bytes have been written. The WRITE is terminated by the master generating a stop conditions.

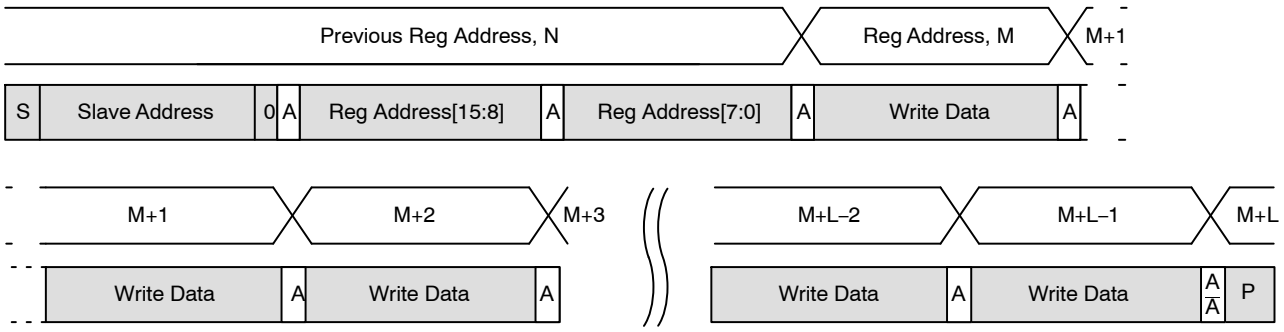


Figure 44. Sequential WRITE, Start at Random Location

FOUR−WIRE SERIAL INTERFACE

The sensor's configuration registers are accessible through a Four−Wire or Serial Peripheral Interface (SPI). The SPI is a full−duplex, synchronous interface and uses four wires:

- CS_N: Chip Select (*active low*)
- S_{CLK}: Serial Input Clock
- S_{DATA}: Serial Data Input
- $S_{DATAOUT}$: Serial Data Output

The SPI interface uses a master−slave setup in which the sensor is the slave. Every read or write access is initiated by the master by pulling down the CS_N line. The master then sends a 15−bit register address followed by a single read/write bit. If the read/write bit is set to 1, the slave *reads* the 16−bit data stored at the specified register address and returns it to the master over the $S_{DATAOUT}$ line. A single SPI read operation is shown in Figure 45. In case the read/write bit is set to '0', the master sends another 16 bits of data for the slave to *write* to the previously specified register address. A single SPI write transaction is depicted in Figure 46.

Both address and register data is sent serially and synchronous to the S_{CLK}. A single SPI transaction consists of 32 bits. In order to speed up the SPI communication, a 32 sequential read and write is possible. The sequential register access is illustrated in Figure 47 and 48.

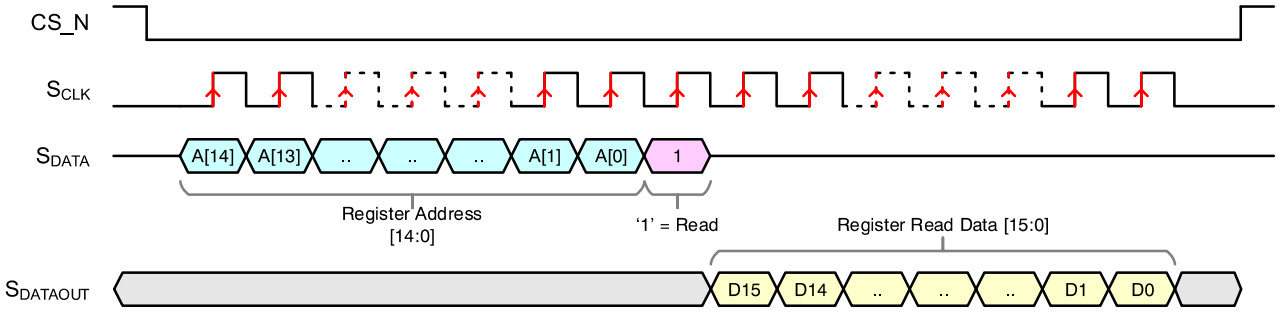


Figure 45. Single SPI Read

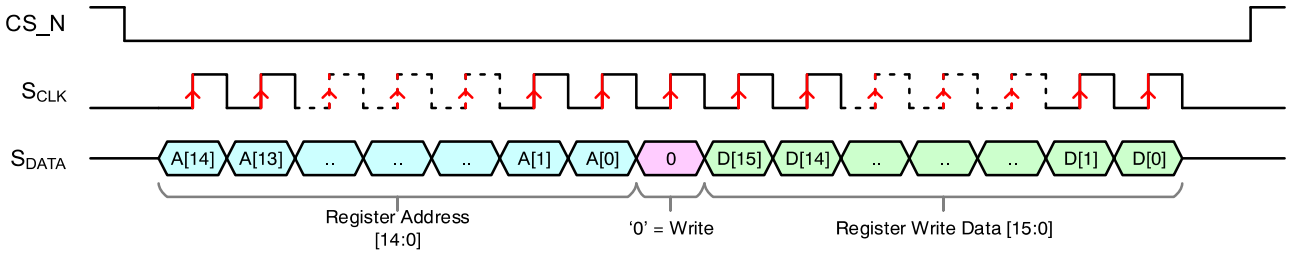


Figure 46. SPI Single Write

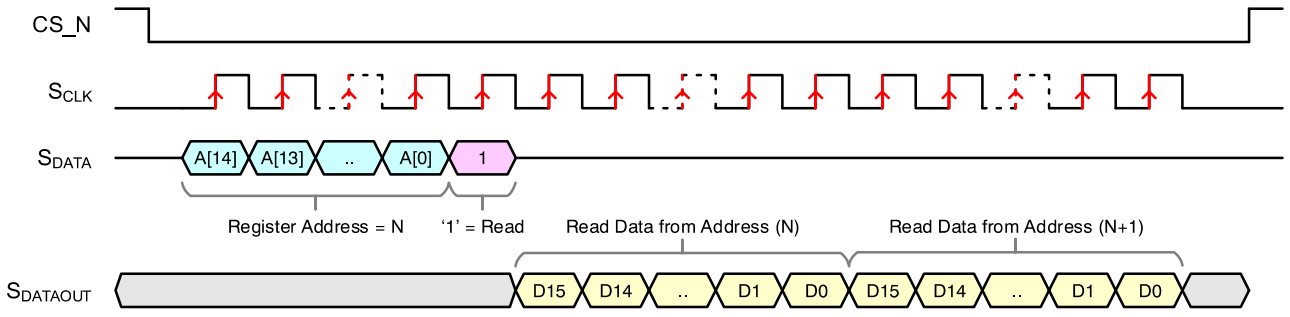


Figure 47. SPI Sequential Read

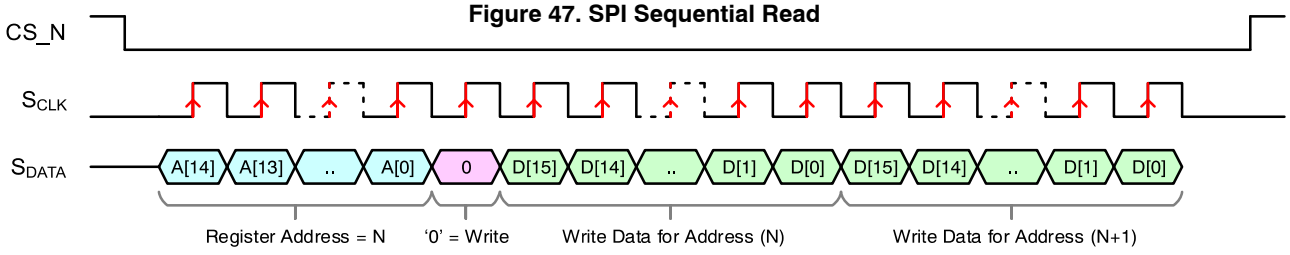


Figure 48. SPI Sequential Write

ELECTRICAL SPECIFICATIONS

Unless stated otherwise, the following specifications apply to the following conditions:

V_{AA}_PIX = V_{AA}_PIX_BST = V_{AA}_RD = 3.0 V;

V_{AA} = V_{DD}_PLL = 2.8 V;

V_{DD}_IO = 1.8 V;

V_{DD} = 1.2 V;

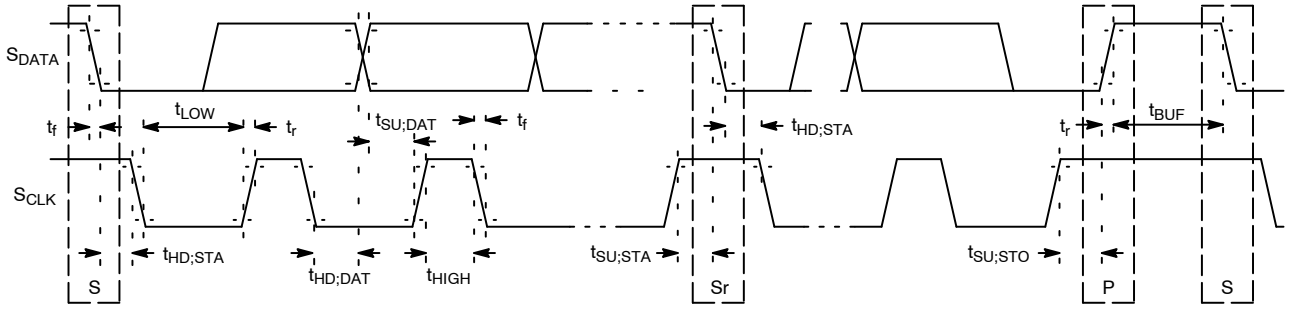
V_{DD}_SLVS = 1.2 V;

EXTCLK = 32.4 MHz;

T_A = 25°C;

TWO−WIRE SERIAL REGISTER INTERFACE

The electrical characteristics of the two−wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 49 and Table 13.



NOTE: Read sequence: For an 8−bit READ, read waveforms start after WRITE command and register address are issued.

Figure 49. Two−Wire Serial Bus Timing Parameters

Table 13. TWO−WIRE SERIAL BUS CHARACTERISTICS

Parameter	Symbol	Standard Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
S_{CLK} Clock Frequency	fSCL	0	100	0	400	kHz
Hold Time (Repeated) START Condition	tHD;STA	4.0	–	0.6	–	μs
LOW Period of the S_{CLK} Clock	tLOW	4.7	–	1.3	–	μs
HIGH Period of the S_{CLK} Clock	tHIGH	4.0	–	0.6	–	μs
Set−up Time for a Repeated START Condition	tSU;STA	4.7	–	0.6	–	μs
Data Hold Time	tHD;DAT	0 (Note 12)	3.45 (Note 13)	0 (Note 14)	0.9 (Note 13)	μs
Data Set−up Time	tSU;DAT	250	–	100 (Note 14)	–	ns
Rise Time of both S_{DATA} and S_{CLK} Signals	t_r	–	1000	20 + 0.1Cb (Note 15)	300	ns
Fall Time of both S_{DATA} and S_{CLK} Signals	t_f	–	300	20 + 0.1Cb (Note 15)	300	ns
Set−up Time for STOP Condition	tSU;STO	4.0	–	0.6	–	μs
Bus Free Time between a STOP and START Condition	tBUF	4.7	–	1.3	–	μs
Capacitive Load for each Bus Line	Cb	–	400	–	400	pF
Serial Interface Input Pin Capacitance	CIN_SI	–	3.3	–	3.3	pF
S_{DATA} Max Load Capacitance	C_{LOAD}_SD	–	30	–	30	pF
S_{DATA} Pull−up Resistor	RSD	1.5	4.7	1.5	4.7	kΩ

9. This table is based on I^2C standard (v2.1 January 2000). Philips Semiconductor.
10. Two−wire control is I^2C−compatible.
11. All values referred to V_{IH}min = 0.9 V_{DD}_IO and V_{IL}max = 0.1 V_{DD}_IO levels. Sensor EXTCLK = 32.4 MHz.
12. A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the undefined region of the falling edge of S_{CLK}.
13. The maximum tHD;DAT has only to be met if the device does not stretch the LOW period (tLOW) of the S_{CLK} signal.
14. A Fast−mode I^2C−bus device can be used in a Standard−mode I^2C−bus system, but the requirement tSU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard mode I^2C−bus specification) before the S_{CLK} line is released.
15. Cb = total capacitance of one bus line in pF.

FOUR−WIRE SERIAL INTERFACE

The electrical characteristics of the of the Serial Peripheral Interface (SPI) or Four−Wire interface (CS_N, S_{CLK}, S_{DATA} and $S_{DATAOUT}$) are shown in Figures 50, 51 and 55. The timing parameters are listed in Table 14.

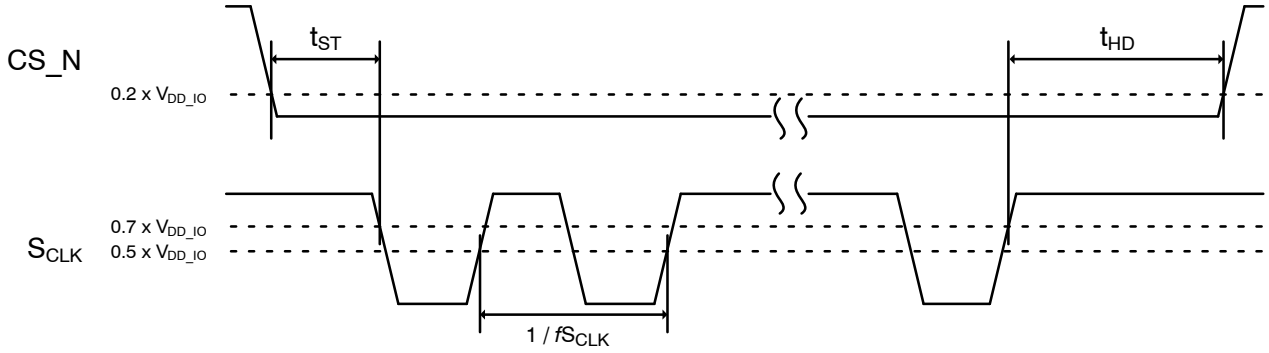


Figure 50. SPI Timing Diagram − Chip Select

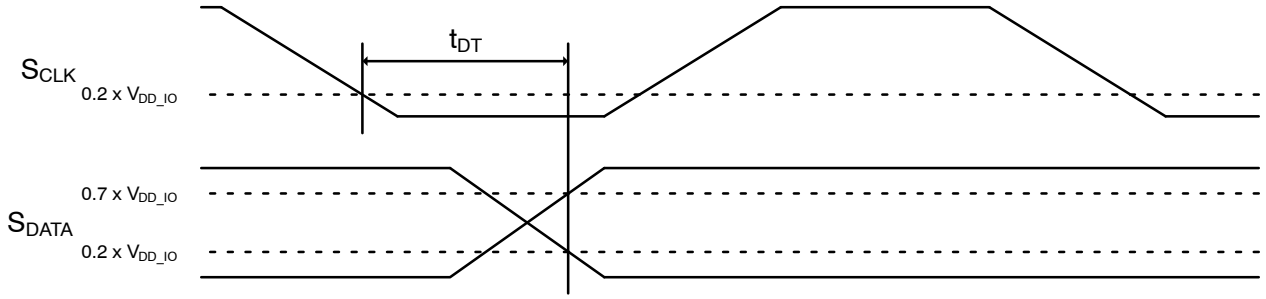


Figure 51. SPI Timing Diagram − Data Input

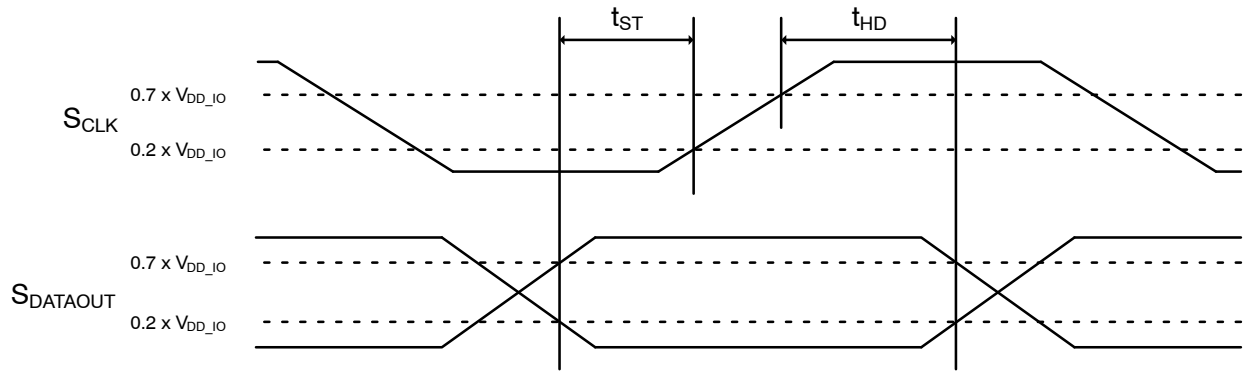


Figure 52. SPI Timing Diagram − Data Output

Table 14. SPI TIMING PARAMETERS

Parameter	Symbol	Min	Typ	Max	Unit
SPI Read Frequency (PLL disabled / PLL enabled)	fS_{CLK}		3.5 / 6.1		MHz
SPI Write Frequency (PLL disabled / PLL enabled)	fS_{CLK}		12.5 / 25		MHz
Setup Time	t_{ST}	$(1/fS_{CLK})*0.1$			ns
Hold Time	t_{HD}	$(1/fS_{CLK})*0.1$			ns
Transfer Delay Time	t_{DT}			$(1/fS_{CLK})*0.5$	ns

I/O TIMING

External Clock

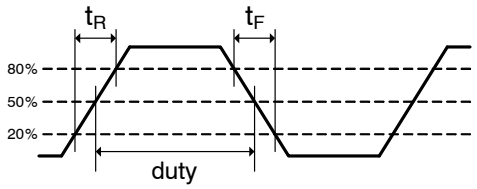


Figure 53. External Clock Timing

Table 15. EXTERNAL CLOCK SPECIFICATIONS

Parameter	Name	Min	Typ	Max	Unit
Clock Frequency	EXTCLK	29 (Note 16)	32.4	36 (Note 16)	MHz
Duty Cycle	Duty	45	50	55	%
Jitter	Jitter	–	–	100	ps
Rise Time	T_R	–	–	5	ns
Fall Time	T_F	–	–	5	ns

16. Any deviation from the typical EXTCLK frequency needs to be compensated by reconfiguring the internal PLL (guidelines available upon request).

Trigger Input

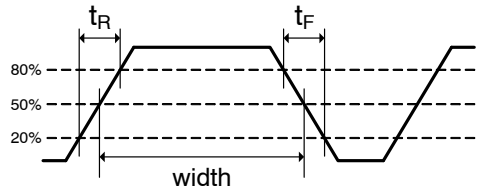


Figure 54. Trigger Input Pulse Timing

Table 16. TRIGGER INPUT PULSE SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
Pulse Width	width	100	–	–	ns
Rise Time	T_R	–	–	5	ns
Fall Time	T_F	–	–	5	ns

DC ELECTRICAL CHARACTERISTICS

The DC electrical characteristics of the XGS 12000/8000 sensor are listed in Tables 17 through 28.

Table 17. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core Digital Voltage		1.1	1.2	1.3	V
V_{DD}_IO	I/O Digital Voltage		1.7 / 2.7	1.8 / 2.8	1.9 / 2.9	V
V_{AA}	Analog Voltage	Dedicated Power Supply	2.7	2.8	2.9	V
V_{AA}_PIX	Pixel Supply Voltage		2.9	3	3.1	V
V_{AA}_PIX_BST	Pixel Booster Supply		2.9	3	3.1	V
V_{AA}_RD	Row Driver Supply		2.9	3	3.1	V
V_{DD}_SLVS	HiSPi Supply Voltage		0.3 / 1.1	0.4 / 1.2	0.5 / 1.3	V
V_{DD}_PLL	PLL Supply Voltage		2.7	2.8	2.9	V
V_{IH}	Input HIGH Voltage		V_{DD}_IO * 0.7	–	V_{DD}_IO + 0.5	V
V_{IL}	Input LOW Voltage		–0.5	–	V_{DD}_IO * 0.3	V
V_{OH}	Output HIGH Voltage		V_{DD}_IO – 0.3	–	–	V
V_{OL}	Output LOW voltage	V_{DD}_IO = 2.8V	–	–	0.4	V

CAUTION: Stresses greater than those listed in Table 18 below may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
ABS V_{DD}_SLVS	ABS Rating for 0.4 V/1.2 V Supply	–0.5	1.5	V
ABS V_{DD}	ABS Rating for 1.2 V Supply	–0.5	1.5	V
ABS V_{DD}_IO	ABS Rating for 1.8 V/2.8 V Supply	–0.5	3.2	V
ABS V_{DD}_PLL	ABS Rating for 2.8 V Supply	–0.5	3.2	V
ABS V_{AA}	ABS Rating for 2.8 V Supply	–0.5	3.2	V
ABS V_{AA}_PIX, V_{AA}_RD, V_{AA}_PIX_BST	ABS Rating for 3.0 V Supply	–0.5	3.6	V
T_{STG}	ABS Storage Temperature Range	–40	+150	°C
	ABS Storage Humidity Range at 85°C		85	%RH
Electrostatic Discharge (ESD) (ANSI / ESDA / JEDEC Standard)	Human Body Model (HBM): JS–001–2014	2000		V
	Charged Device Model (CDM): JS–002–2014	500		
LU	Latch–Up: JESD–78	100		mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

17. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
18. Operating ratings are conditions in which operation of the device is intended to be functional.
19. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625□A. Refer to (AN52561/D). Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
20. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

Table 19. OPERATING CURRENT CONSUMPTION (XGS 12000−X1)
(V_{AA}_PIX = V_{AA}_PIX_BST = V_{AA}_RD = 3.0 V; V_{AA} = V_{DD}_PLL = 2.8 V; V_{DD}_IO = 1.8 V; V_{DD} = 1.2 V; V_{DD}_SLVS = 0.4 V / 1.2 V; T_A = 25°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Digital Operating Current	90 fps @ 4096 x 3072 Resolution	–	180	240	mA
I_{DD}_IO	I/O Digital Operating Current	90 fps @ 4096 x 3072 Resolution	–	5	10	mA
I_{AA}	Analog Operating Current	90 fps @ 4096 x 3072 Resolution	–	140	180	mA
I_{AA}_PIX	Pixel Supply Current	90 fps @ 4096 x 3072 Resolution	–	25	40	mA
I_{AA}_PIX_BST	Pixel Booster Supply Current	90 fps @ 4096 x 3072 Resolution	–	15	35	mA
I_{AA}_RD	Row Driver Supply Current	90 fps @ 4096 x 3072 Resolution	–	0	10	mA
I_{DD}_SLVS	HiSPi Supply Current	90 fps @ 4096 x 3072 Resolution – V_{DD}_SLVS = 0.4 / 1.2 V	–	65 / 120	85 / 150	mA
I_{DD}_PLL	PLL Supply Current	90 fps @ 4096 x 3072 Resolution	–	10	20	mA

Table 20. OPERATING CURRENT CONSUMPTION (XGS 12000−X3)
(V_{AA}_PIX = V_{AA}_PIX_BST = V_{AA}_RD = 3.0 V; V_{AA} = V_{DD}_PLL = 2.8 V; V_{DD}_IO = 1.8 V; V_{DD} = 1.2 V; V_{DD}_SLVS = 0.4 V / 1.2 V; T_A = 25°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Digital Operating Current	28 fps @ 4096 x 3072 Resolution	–	125	240	mA
I_{DD}_IO	I/O Digital Operating Current	28 fps @ 4096 x 3072 Resolution	–	5	10	mA
I_{AA}	Analog Operating Current	28 fps @ 4096 x 3072 Resolution	–	65	180	mA
I_{AA}_PIX	Pixel Supply Current	28 fps @ 4096 x 3072 Resolution	–	10	40	mA
I_{AA}_PIX_BST	Pixel Booster Supply Current	28 fps @ 4096 x 3072 Resolution	–	20	35	mA
I_{AA}_RD	Row Driver Supply Current	28 fps @ 4096 x 3072 Resolution	–	0	10	mA
I_{DD}_SLVS	HiSPi Supply Current	28 fps @ 4096 x 3072 Resolution – V_{DD}_SLVS = 0.4 / 1.2 V	–	60 / 115	85 / 150	mA
I_{DD}_PLL	PLL Supply Current	28 fps @ 4096 x 3072 Resolution	–	10	20	mA

Table 21. OPERATING CURRENT CONSUMPTION (XGS 9400−X1)
(V_{AA}_PIX = VAA_PIX_BST = V_{AA}_RD = 3.0 V; V_{AA} = V_{DD}_PLL = 2.8 V; V_{DD}_IO = 1.8 V; V_{DD} = 1.2 V; V_{DD}_SLVS = 0.4 V / 1.2 V; T_A = 25ºC)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Digital Operating Current	90 fps @ 3072 x 3072 Resolution	–	180	240	mA
I_{DD}_IO	I/O Digital Operating Current	90 fps @ 3072 x 3072 Resolution	–	5	10	mA
I_{AA}	Analog Operating Current	90 fps @ 3072 x 3072 Resolution	–	140	180	mA
I_{AA}_PIX	Pixel Supply Current	90 fps @ 3072 x 3072 Resolution	–	25	40	mA
I_{AA}_PIX_BST	Pixel Booster Supply Current	90 fps @ 3072 x 3072 Resolution	–	15	35	mA
I_{AA}_RD	Row Driver Supply Current	90 fps @ 3072 x 3072 Resolution	–	0	10	mA
I_{DD}_SLVS	HiSPi Supply Current	90 fps @ 3072 x 3072 Resolution (V_{DD}_SLVS = 0.4 / 1.2 V)	–	65 / 120	85 / 150	mA
I_{DD}_PLL	PLL Supply Current	90 fps @ 3072 x 3072 Resolution	–	10	20	mA

Table 22. OPERATING CURRENT CONSUMPTION (XGS 9400−X2)
(V_{AA}_PIX = V_{AA}_PIX_BST = V_{AA}_RD = 3.0 V; V_{AA} = V_{DD}_PLL = 2.8 V; V_{DD}_IO = 1.8 V; V_{DD} = 1.2 V; V_{DD}_SLVS = 0.4 V / 1.2 V; T_A = 25°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Digital Operating Current	56 fps @ 3072 x 3072 Resolution	–	145	240	mA
I_{DD}_IO	I/O Digital Operating Current	56 fps @ 3072 x 3072 Resolution	–	5	10	mA
I_{AA}	Analog Operating Current	56 fps @ 3072 x 3072 Resolution	–	100	180	mA
I_{AA}_PIX	Pixel Supply Current	56 fps @ 3072 x 3072 Resolution	–	20	40	mA
I_{AA}_PIX_BST	Pixel Booster Supply Current	56 fps @ 3072 x 3072 Resolution	–	20	35	mA
I_{AA}_RD	Row Driver Supply Current	56 fps @ 3072 x 3072 Resolution	–	0	10	mA
I_{DD}_SLVS	HiSPi Supply Current	56 fps @ 3072 x 3072 Resolution (V_{DD}_SLVS = 0.4 / 1.2 V)	–	60 / 115	85 / 150	mA
I_{DD}_PLL	PLL Supply Current	56 fps @ 3072 x 3072 Resolution	–	10	20	mA

Table 23. OPERATING CURRENT CONSUMPTION (XGS 8000−X1)
(V_{AA}_PIX = V_{AA}_PIX_BST = V_{AA}_RD = 3.0 V; V_{AA} = V_{DD}_PLL = 2.8 V; V_{DD}_IO = 1.8 V; V_{DD} = 1.2 V; V_{DD}_SLVS = 0.4 V / 1.2 V; T_A = 25ºC)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Digital Operating Current	128 fps @ 4096 x 2160 Resolution	–	180	240	mA
I_{DD}_IO	I/O Digital Operating Current	128 fps @ 4096 x 2160 Resolution	–	5	10	mA
I_{AA}	Analog Operating Current	128 fps @ 4096 x 2160 Resolution	–	140	180	mA
I_{AA}_PIX	Pixel Supply Current	128 fps @ 4096 x 2160 Resolution	–	25	40	mA
I_{AA}_PIX_BST	Pixel Booster Supply Current	128 fps @ 4096 x 2160 Resolution	–	20	35	mA
I_{AA}_RD	Row Driver Supply Current	128 fps @ 4096 x 2160 Resolution	–	0	10	mA
I_{DD}_SLVS	HiSPi Supply Current	128 fps @ 4096 x 2160 Resolution – V_{DD}_SLVS = 0.4 / 1.2 V	–	65 / 125	85 / 150	mA
I_{DD}_PLL	PLL Supply Current	128 fps @ 4096 x 2160 Resolution	–	10	20	mA

Table 24. OPERATING CURRENT CONSUMPTION (XGS 8000−X2)
(V_{AA}_PIX = V_{AA}_PIX_BST = V_{AA}_RD = 3.0 V; V_{AA} = V_{DD}_PLL = 2.8 V; V_{DD}_IO = 1.8 V; V_{DD} = 1.2 V; V_{DD}_SLVS = 0.4 V / 1.2 V; T_A = 25°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Digital Operating Current	80 fps @ 4096 x 2160 Resolution	–	145	240	mA
I_{DD}_IO	I/O Digital Operating Current	80 fps @ 4096 x 2160 Resolution	–	5	10	mA
I_{AA}	Analog Operating Current	80 fps @ 4096 x 2160 Resolution	–	100	180	mA
I_{AA}_PIX	Pixel Supply Current	80 fps @ 4096 x 2160 Resolution	–	20	40	mA
I_{AA}_PIX_BST	Pixel Booster Supply Current	80 fps @ 4096 x 2160 Resolution	–	20	35	mA
I_{AA}_RD	Row Driver Supply Current	80 fps @ 4096 x 2160 Resolution	–	0	10	mA
I_{DD}_SLVS	HiSPi Supply Current	80 fps @ 4096 x 2160 Resolution – V_{DD}_SLVS = 0.4 / 1.2 V	–	60 / 115	85 / 150	mA
I_{DD}_PLL	PLL Supply Current	80 fps @ 4096 x 2160 Resolution	–	10	20	mA

Table 25. STANDBY CURRENT CONSUMPTION
(V_{AA}_PIX = V_{AA}_PIX_BST = V_{AA}_RD = 3.0 V; V_{AA} = V_{DD}_PLL = 2.8 V; V_{DD}_IO = 1.8 V; V_{DD} = 1.2 V; V_{DD}_SLVS = 0.4 V / 1.2 V; T_A = 25°C)

Sensor State	Condition	Min	Typ	Max	Unit
WAIT_ON_TRIGGER	V_{DD}_SLVS (0.4 V / 1.2 V)	–	75 / 135	–	μA
	V_{DD} (1.2 V)	–	170	–	μA
	V_{DD}_IO (1.8 V)	–	5	–	μA
	V_{DD}_PLL (2.8 V)	–	10	–	μA
	V_{AA} (2.8 V)	–	130	–	μA
	V_{AA}_PIX (3.0 V)	–	25	–	μA
	V_{AA}_PIX_BST (3.0 V)	–	30	–	μA
	V_{AA}_RD (3.0 V)	–	5	–	μA
STANDBY	V_{DD}_SLVS (0.4 V / 1.2 V)	–	75 / 135	–	μA
	V_{DD} (1.2 V)	–	170	–	μA
	V_{DD}_IO (1.8 V)	–	5	–	μA
	V_{DD}_PLL (2.8 V)	–	10	–	μA
	V_{AA} (2.8 V)	–	20	–	μA
	V_{AA}_PIX (3.0 V)	–	0	–	μA
	V_{AA}_PIX_BST (3.0 V)	–	15	–	μA
	V_{AA}_RD (3.0 V)	–	0	–	μA
SLEEP	V_{DD}_SLVS (0.4 V / 1.2 V)	–	55 / 100	–	μA
	V_{DD} (1.2 V)	–	40	–	μA
	V_{DD}_IO (1.8 V)	–	5	–	μA
	V_{DD}_PLL (2.8 V)	–	0	–	μA
	V_{AA} (2.8 V)	–	0	–	μA
	V_{AA}_PIX (3.0 V)	–	0	–	μA
	V_{AA}_PIX_BST (3.0 V)	–	0	–	μA
	V_{AA}_RD (3.0 V)	–	0	–	μA
RESET	V_{DD}_SLVS (0.4 V / 1.2 V)	–	55 / 100	–	μA
	V_{DD} (1.2 V)	–	10	–	μA
	V_{DD}_IO (1.8 V)	–	5	–	μA
	V_{DD}_PLL (2.8 V)	–	0	–	μA
	V_{AA} (2.8 V)	–	0	–	μA
	V_{AA}_PIX (3.0 V)	–	0	–	μA
	V_{AA}_PIX_BST (3.0 V)	–	0	–	μA
	V_{AA}_RD (3.0 V)	–	0	–	μA

HISPI ELECTRICAL SPECIFICATION

The XGS sensor from ON Semiconductor supports SLVS mode only. SLVS is typically meant only for short transmission line connections, with the advantage that SLVS drivers consume less power. Refer to the HiSPi Physical Layer Specification v2.00.00 (AND9509/D) for additional electrical definitions, specifications and timing information. Note that the V_{DD}_SLVS supply in this datasheet corresponds to V_{DD}_TX in the HiSPi Physical Layer Specification. Similarly, V_{DD}_IO is equivalent to V_{DD}_HiSPi as referenced in the specification.

Table 4 in the HiSPi Physical Layer specification v2.00.00 (AND9509/D) document sets the maximum PHY−to−PHY skew to 2.1 UI. The XGS products adhere to this specification when looking at all HiSPi data and HiSPi clock lanes on the same side of the sensor. The maximum PHY−to−PHY skew between any odd clock lane and any odd data lane is 2.1 UI. The same holds for the skew between any even clock lane and any even data lane.

However the maximum PHY−to−PHY skew between any odd clock lane and any even data lane, or between any even clock lane and any odd data lane, can be maximum 4 pixels. The maximum value for this depends on the mux mode that is used. In 4:4 mux mode, the maximum is 1 pixel. In 4:2 mux mode, the maximum is 2 pixels. And in 4:1 mux mode, the maximum is 4 pixels.

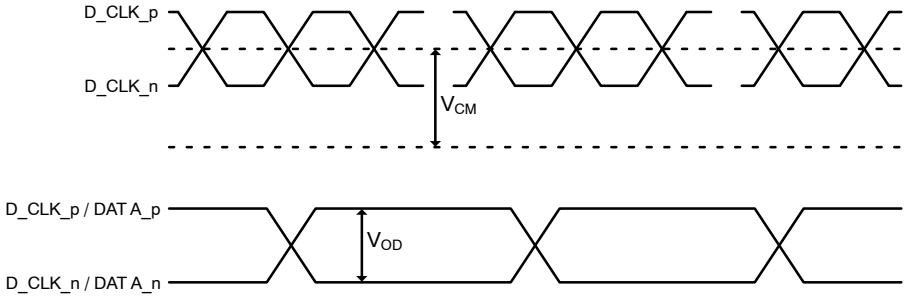


Figure 55. HiSPi DC Parameters

Table 26. HISPI DC SPECIFICATIONS (V_{DD}_SLVS = 0.4 V)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}_SLVS	HiSPi Power Supply	0.35	0.4	0.45	V
V_{OD}	Input Differential Voltage (R_{IN} = 100 Ω)	0.4 * V_{DD}_SLVS	0.5 * V_{DD}_SLVS	0.6 * V_{DD}_SLVS	V
V_{CM}	Input Common Mode Range (R_{IN} = 100 Ω)	0.45 * V_{DD}_SLVS	0.5 * V_{DD}_SLVS	0.55 * V_{DD}_SLVS	V
R_{IN}	Termination Resistor		100		Ω
Output Impedance	Output Impedance per Pin	35	50	70	Ω

Table 27. DIFFERENTIAL DATA OUTPUT DC SPECIFICATIONS (V_{DD}_SLVS = 1.2 V)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}_SLVS	HiSPi Power Supply	1.1	1.2	1.3	V
V_{OD}	Input Differential Voltage (R_{IN} = 100 Ω)	0.3	0.35	0.4	V
V_{CM}	Input Common Mode Range (R_{IN} = 100 Ω)	0.3	0.35	0.4	V
R_{IN}	Termination Resistor		100		Ω
Output Impedance	Output Impedance per Pin	35	50	70	Ω

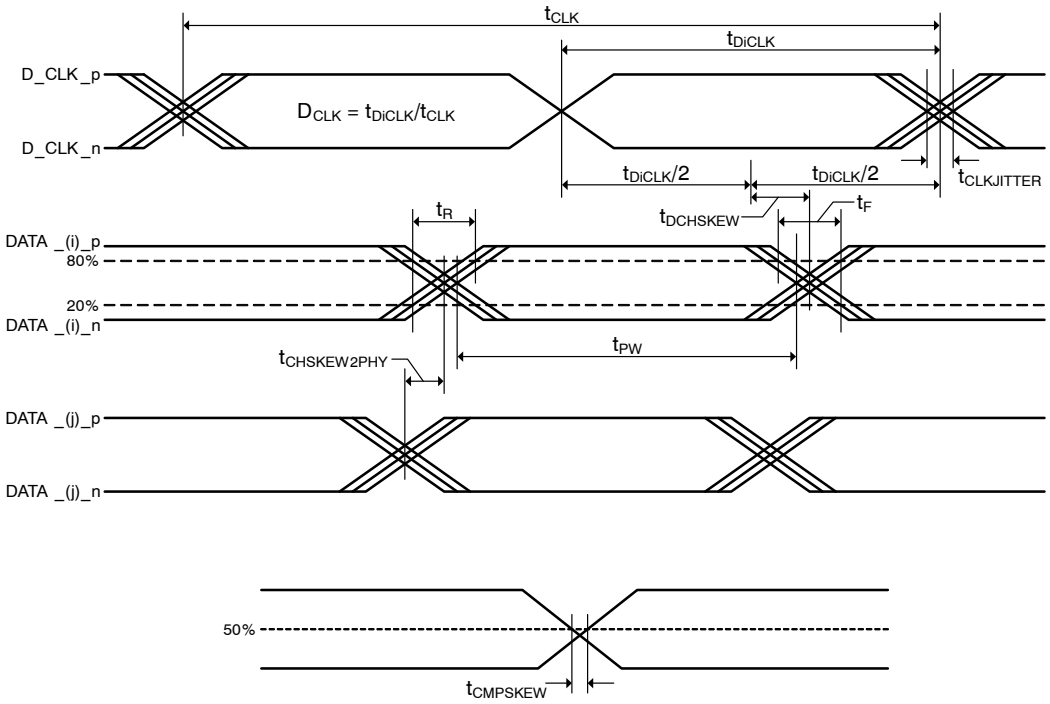


Figure 56. Differential Data Output AC Parameters

Table 28. DIFFERENTIAL DATA OUTPUT AC SPECIFICATIONS (V_{DD}_SLVS = 0.4 V, 1.2 V)

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate	$1/t_{DiCLK}$	–	777.6	–	Mbps
Clock Period	t_{CLK}	–	2.57	–	ns
Data Period	t_{DiCLK}	–	1.28	–	ns
Data Eye Width	t_{PW}	0.6	0.8	–	UI
Clock Jitter	$t_{CLKJITTER}$	–	40	50	ps
Rise Time	t_R	–	310	–	ps
Fall Time	t_F	–	310	–	ps
Clock Duty	D_{CLK}	42	–	58	%
Clock to Data Skew within any PHY	$t_{DCHSKEW}$	−0.1	–	0.1	UI
Skew between any Two PHY Clocks	$t_{CHSKEW2PHY}$	−2.3	–	2.3	UI
Complementary Skew in Differential Pair	$t_{CMPSKEW}$	−100	–	100	ps

21.1 UI is defined as the normalized mean time between one edge and the following edge of the clock.

IMAGE SENSOR CHARACTERISTICS

ELECTRO−OPTICAL SPECIFICATIONS

An overview of the XGS key electro−optical specifications can be found in Table 29. Unless otherwise noted, all measurements were done using the recommended configuration and default operation mode.

SPECTRAL RESPONSE

Quantum efficiency curves are measured using a monochromator with step size of 5 nm. The curves for monochrome and color devices are shown in Figure 57.

Table 29. ELECTRO−OPTICAL SPECIFICATIONS

Parameter	Specification
Quantum Efficiency (Note 22)	63% (monochrome)
	60% (color)
Dark Current	85 e^- / s (T_j = 60°C)
DSNU	1.76 e^- (T_j = 60°C, Tint = 5 ms)
PRNU	0.5%
Shutter Efficiency	1/3600
MTF (@ 530nm)	66.5% (vertical)
	67.4% (horizontal)

22. Measured on devices with cover glass (typical transmittance cover glass = 91%).

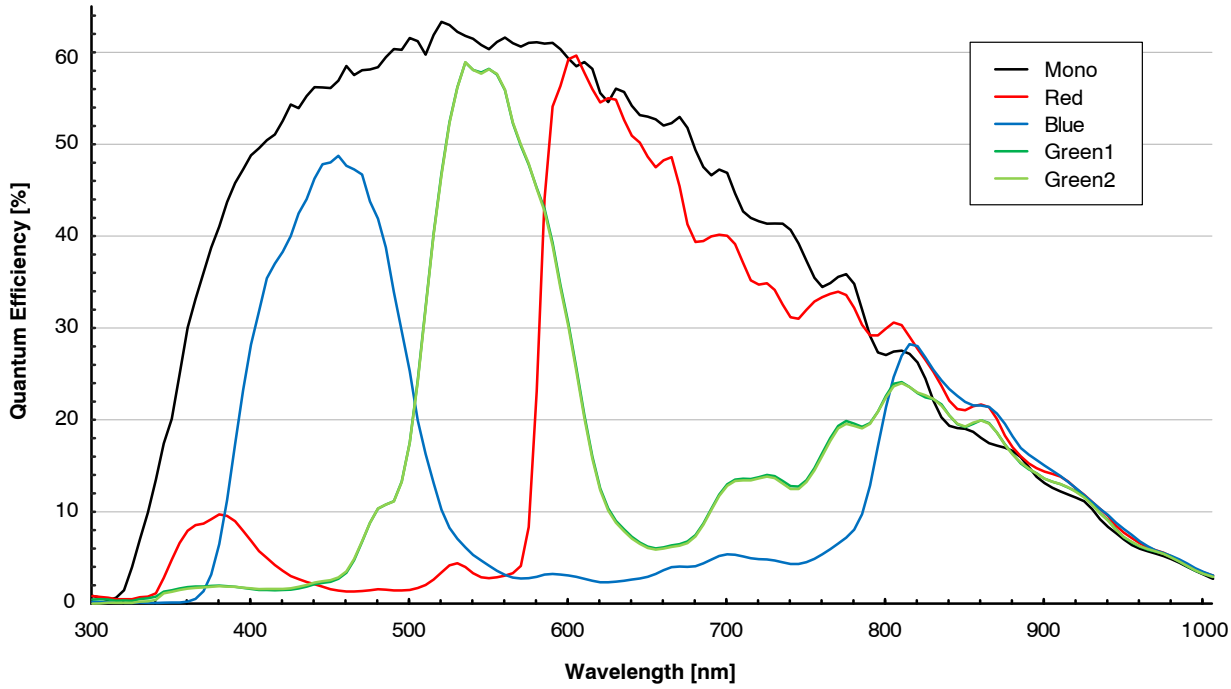


Figure 57. Quantum Efficiency

COVER GLASS

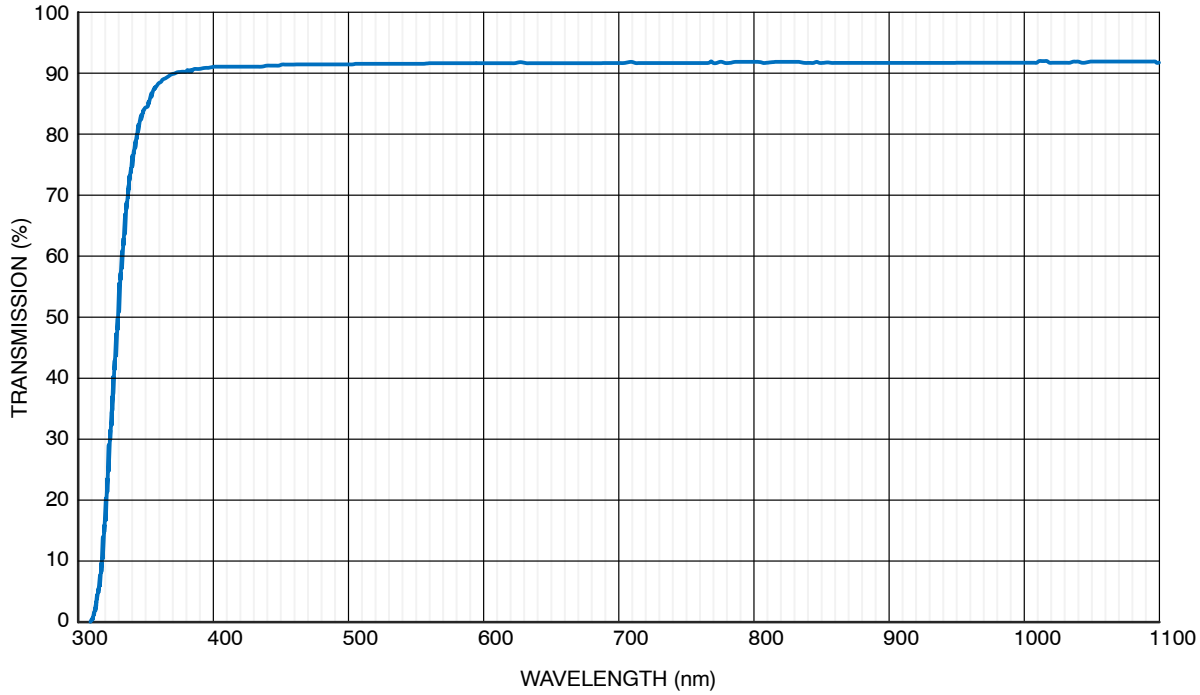


Figure 58. Cover Glass Transmission Curve

Table 30. COVER GLASS SPECIFICATIONS

Parameter	Specification
Material	D263 T−ECO
Refractive Index (@ 550 nm)	1.5255
Luminous Transmittance (@ D65)	91% (*0.55 mm Thickness*)
Density (@ 40°C)	2.51 g/cm^3
Linear Thermal Coefficient (20°C – 300°C)	7.2 x 10^{-6}/K

PACKAGING

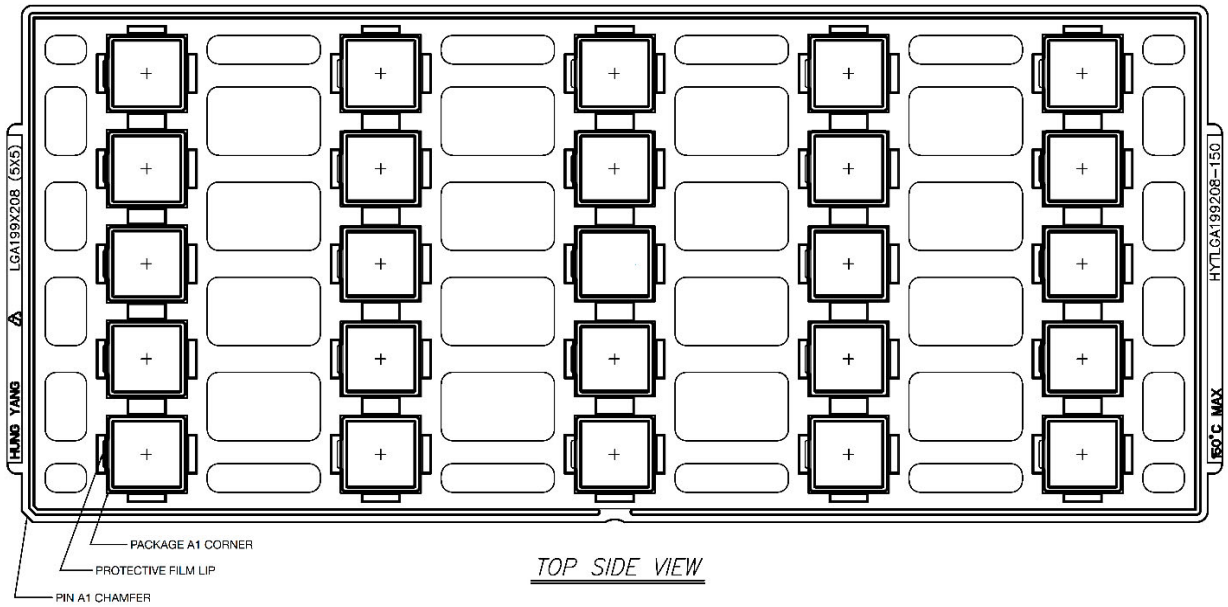


Figure 59. XGS 12000 Shipping Tray − Top View

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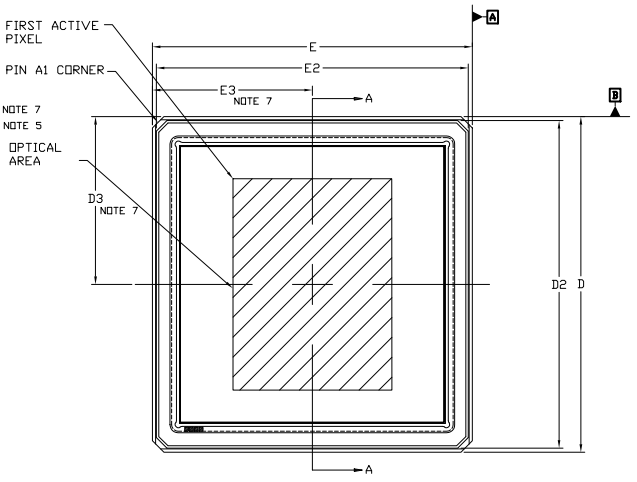
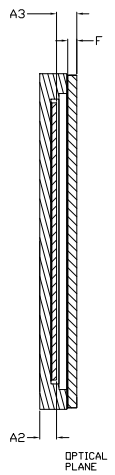
AND9509/D. (n.d.). *High−Speed Serial Pixel (HiSPi) Interface Physical Layer v2.00.00*
AND9510/D. (n.d.). *High−Speed Serial Pixel (HiSPi) Interface Protocol*
TND310/D. (n.d.). *Device Nomenclature (Naming Convention for Image Sensors)*

CLGA163 20.88x19.9, 1P
CASE 621AB
ISSUE A

DATE 11 SEP 2018

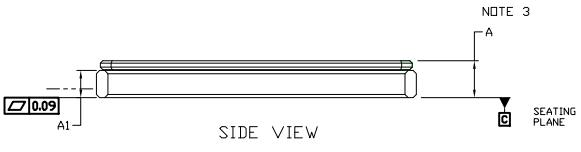


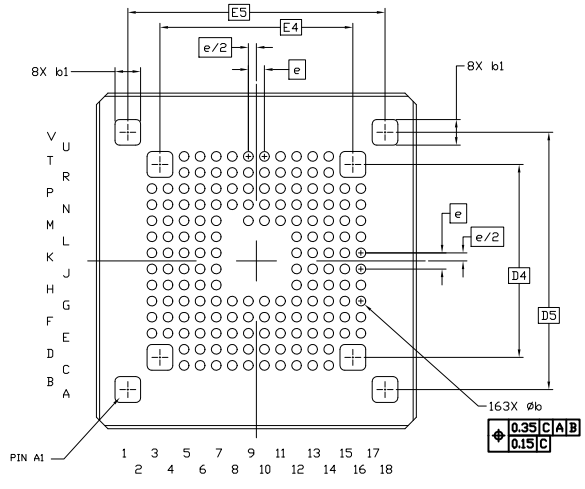


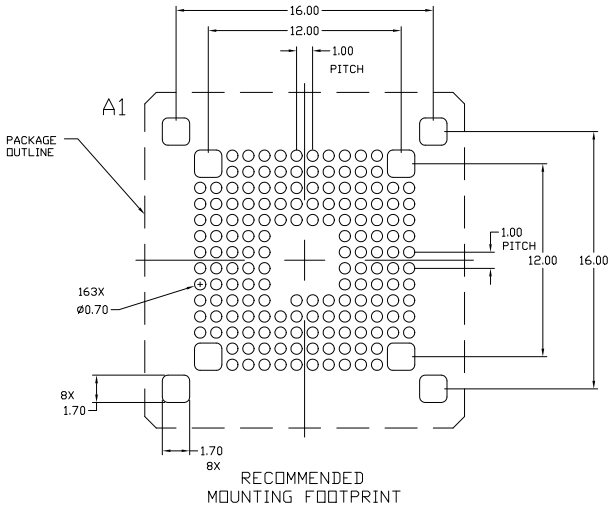
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT DOES NOT INCLUDE HEATSINKS OR OTHER ATTACHED FEATURES.
4. THE LID DEFINED BY DIMENSIONS D2 AND E2 MUST BE LOCATED WITHIN DIMENSIONS D AND E.
5. MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES JOINING AT A1 CORNER, WILL BE 0.7°. OPTICAL AREA IS IS DEFINED BY THE ACTIVE PIXEL ARRAY. REFER TO THE DEVICE DATA SHEET FOR TOTAL ARRAY AND FIRST PIXEL DEFINITIONS.
6. PARALLELISM APPLIES ONLY TO THE OPTICAL AREA.
7. OPTICAL CENTER OFFSET WITH RESPECT TO THE PACKAGE CENTER IS X= 12.345 MICRONS, Y= 77.63 MICRONS ±200 MICRONS.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	2.54
A1	1.61	1.89
A2	0.91	1.19
A3	1.05	1.45
b	0.55	0.65
b1	1.60 REF	
D	20.76	21.00
D2	20.30	20.46
D3	10.16	10.56
D4	12.00 BSC	
D5	16.00 BSC	
E	19.80	20.00
E2	19.32	19.48
E3	9.76	10.16
E4	12.00 BSC	
E5	16.00 BSC	
e	1.00 BSC	
F	0.50	0.60







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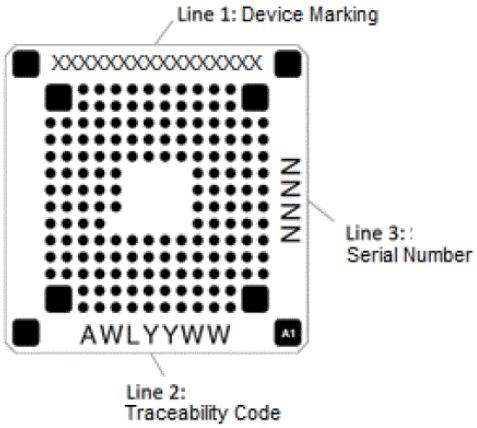
CLGA163 20.88x19.9, 1P
CASE 621AB
ISSUE A

DATE 11 SEP 2018

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
NN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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