AR0330CS

AR0330CS and AR0330SR 1/3-Inch CMOS Digital Image Sensor

ON Semiconductor®

General Description

The AR0330CS can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 2304 x 1296 image at 30 frames per second (fps). The sensor outputs 10− or 12−bit raw data, using either the parallel or serial (MIPI) output ports.

The ON Semiconductor AR0330CS is a 1/3−inch CMOS digital image sensor with an active−pixel array of 2304 (H) x1536 (V). It can support 3.15 megapixel (2048H x 1536 V) digital still image capture and a 1080p30 +20%EIS (2304H x 1296 V) digital video mode. It incorporates sophisticated on−chip camera functions such as windowing, mirroring, column and row subsampling modes, and snapshot modes.
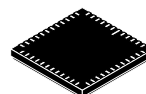
PLCC48
11.43x11.43
CASE 776AM

ODCSP64
6.278x6.648
CASE 570BH

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Table 1. KEY PARAMETERS

Parameter		Typical Value
Optical Format		1/3−inch (6.0 mm) Entire Array: 6.09 mm Still Image: 5.63 mm (4:3) HD Image: 5.82 mm (16:9)
Active Pixels		2304(H) x 1536(V): (Entire Array): 5.07 mm (H) x 3.38 mm (V) 2048(H) x 1536(V) (4:3, Still Mode) 2304(H) x 1296(V) (16:9, sHD Mode)
Pixel Size		2.2 μm x 2.2 μm
Color Filter Array		RGB Bayer
Shutter Type		ERS and GRR
Input Clock Range		6 − 27 MHz
Output Clock Maximum (CLK_OP)		98 Mp/s (Parallel, MIPI)
Responsivity		2.0 V/lux−sec
Power Consumption		1080P30 MIPI Mode: 282 mW
		1080P30 Parallel Mode: 252 mW
SNR_{MAX}		39 dB
Dynamic Range		69.5 dB
Supply Voltage	I/O/Digital	1.7−1.9 V (1.8 V Nominal) or 2.4−3.1 V (2.8 V Nominal)
	Digital	1.7−1.9 V (1.8 V Nominal)
	Analog	2.76−2.9 V
Operating Temperature (junction) −T_J		−30°C to + 70° C
Package Options		6.28 mm x 6.65 mm CSP 11.43 mm x 11.43 mm PLCC

Features (continued)

- 2.2 μm Pixel with ON Semiconductor A−Pix™ technology
- Superior Low−light Performance
- 3.5 Mp Active Array, 2.9 Mp (16:9) Video 3.4 Mp (3:2) and 3.15 Mp (4:3) Still Images
- Support for External Mechanical Shutter
- Support for External LED or Xenon Flash
- Data Interfaces: Two−lane Serial MIPI or Parallel Interface
- On−chip phase−locked Loop (PLL) Oscillator
- Integrated Position−based Color and Lens Shading Correction
- Simple Two−wire Serial Interface
- Auto Black Level Calibration
- 12−to−10 bit Output A−Law Compression
- Slave Mode for Precise Frame−rate Control and for Synchronizing Two Sensors

Applications

- 1080P30 High−definition Digital Video Camcorder
- Web Cameras and Video Conferencing Cameras
- Security

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0330CS1C12SPKA0−CP	3.5 MP, 1/3−inch, 12 Deg CRA, Parallel, MIPI, CSP	Tray, Protective Film
AR0330CS1C12SPKA0−CR	3.5 MP, 1/3−inch, 12 Deg CRA, Parallel, MIPI, CSP	Tray, No Protective Film
AR0330CSSC12SPBA0−DR	3.5 MP, 1/3−inch, 12 Deg CRA, Parallel, PLCC	Tray, No Protective Film
AR0330SR1C00SUKA0−CP	3.5 MP, 1/3−inch, 0 Deg CRA, Parallel, CSP	Tray, Protective Film
AR0330SR1C00SUKA0−CR	3.5 MP, 1/3−inch, 0 Deg CRA, Parallel, CSP	Tray, No Protective Film
AR0330CS1C12SPKAH3−GEVB	3.5 MP, 1/3− inch, 12 Deg CRA, Parallel, MIPI, CSP	Evaluation board

FUNCTIONAL OVERVIEW

The AR0330CS is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) that can generate all internal clocks from a single master input clock running between 6 and 27 MHz. The maximum CLK_OP is 98 Mp/s using MIPI serial interface and 98 Mp/s using the parallel interface.
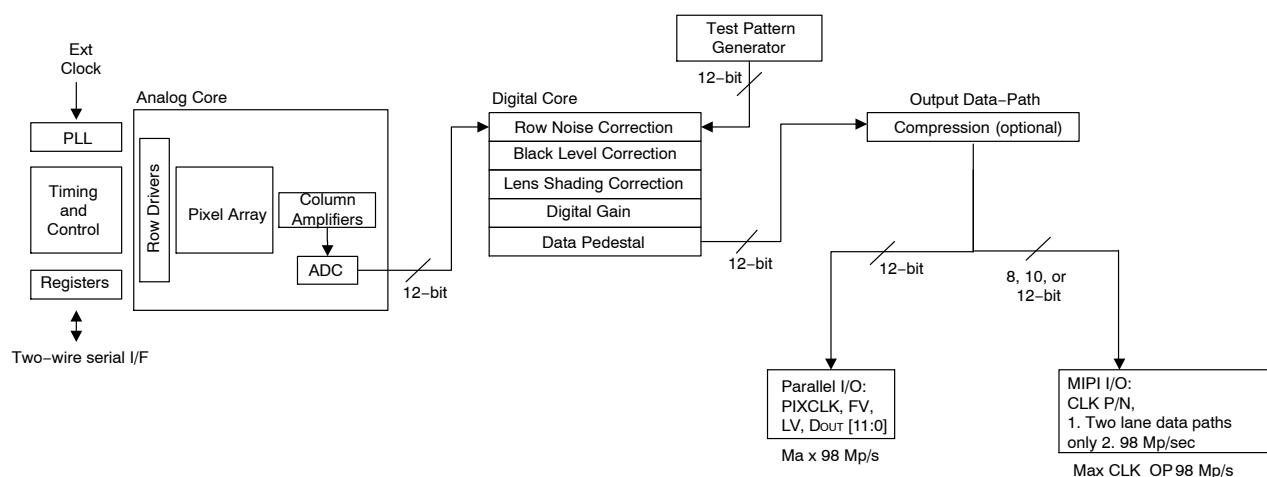

Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 3.5 Mp active− pixel sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the signal from the column is amplified in a column amplifier and then digitized in an analog−to−digital converter (ADC). The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain).

WORKING MODES

The AR0330CS sensor working modes are specified from the following aspect ratios:

Table 3. AVAILABLE ASPECT RATIOS IN THE AR0330CS SENSOR

| Aspect Ratio		Sensor Array Usage
3:2	Still Format #1	2256(H) x 1504(V)
4:3	Still Format #2	2048 (H) x 1536 (V)
16:10	Still Format #3	2256 (H) x 1440 (V)
16:9	FHD Format	2304 (H) x 1296 (V)

The AR0330CS supports the following working modes. To operate the sensor at full speed 98Mp/s the sensor must use 2−Lane MIPI or parallel interface. The sensor will operate at full−speed (98 Mp/s) when using the parallel interface.

Table 4. AVAILABLE WORKING MODES IN THE AR0330CS SENSOR

Mode	Aspect Ratio	Active Readout Window	Sensor Output Resolution	FPS (2 lane MIPI, 12 bit)	FPS (Parallel Interface)	Subsampling	FOV
1080p + EIS	16:9	2304 x 1296	2304 x 1296	30	30	–	100%
3M Still	4:3	2048 x 1536	2048 x 1536	30	25	–	100%
	3:2	2256 x 1504	2256 x 1504	30	25	–	100%
WVGA + EIS	16:9	2304 x 1296	1152 x 648	60	60	2 x 2	100%

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Figure 2. Typical Configuration: Serial MIPI
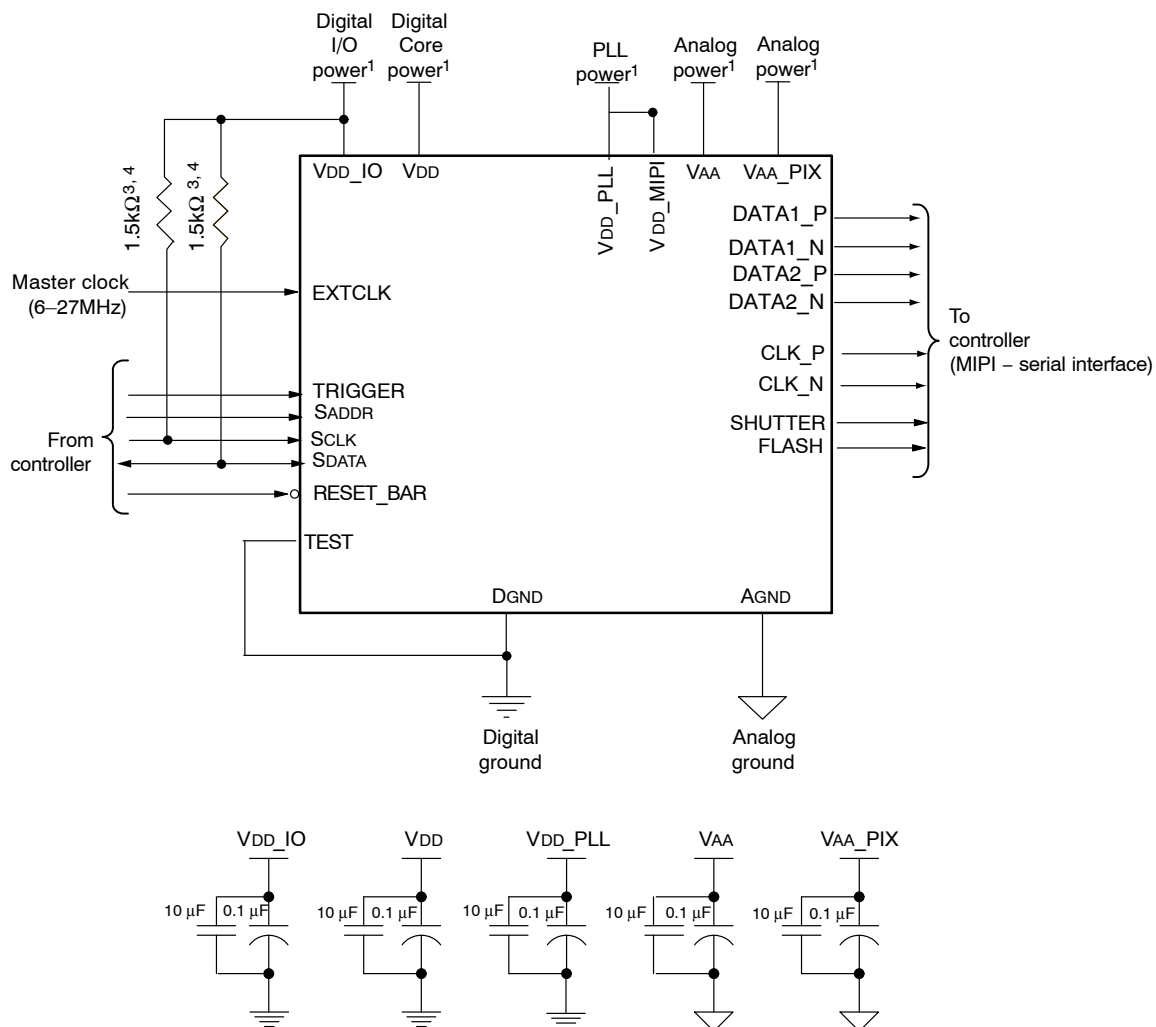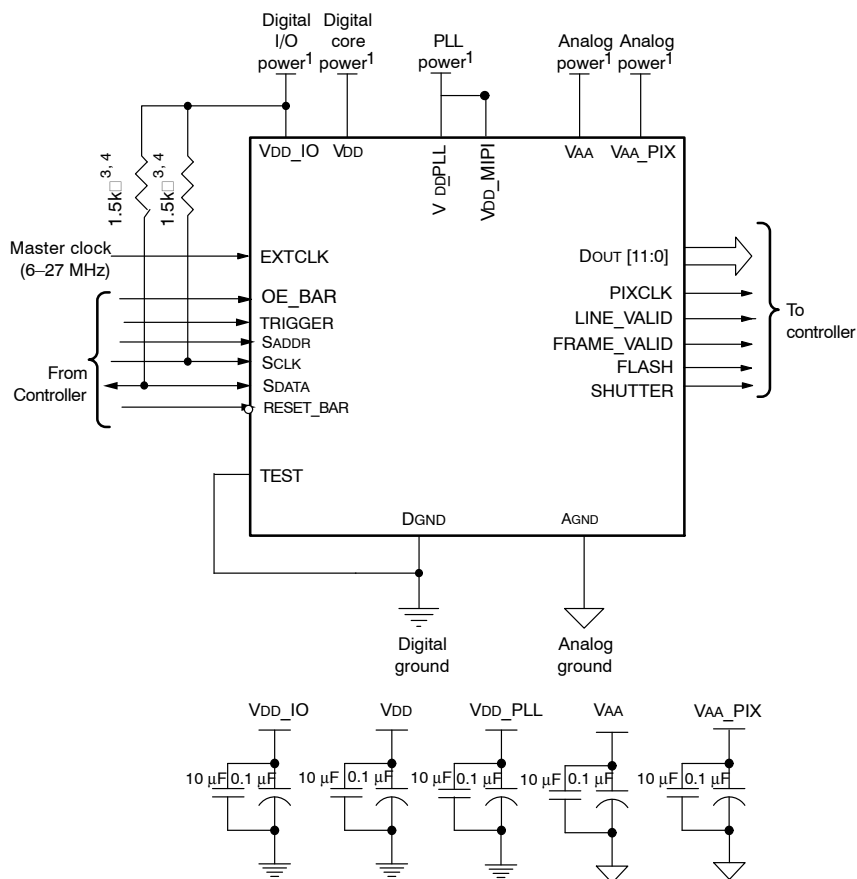
1. All power supplies must be adequately decoupled. ON Semiconductor recommends having 10 μF and 0.1 μF decoupling capacitors for every power supply. If space is a concern, then priority must be given in the following order: V_{AA}, V_{AA}_PIX, V_{DD}_PLL, V_{DD}_MIPI, V_{DD}_IO, and V_{DD}. Actual values and results may vary depending on layout and design considerations.
2. To allow for space constraints, ON Semiconductor recommends having 0.1 μF decoupling capacitor inside the module as close to the pads as possible. In addition, place a 10 μF capacitor for each supply off−module but close to each supply.
3. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
4. The pull−up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. TEST pin must be tied to D_{GND} for the MIPI configuration.
7. ON Semiconductor recommends that GND_MIPI be tied to D_{GND}.
8. V_{DD}_MIPI is tied to V_{DD}_PLL in the CSP package. ON Semiconductor strongly recommends that V_{DD}_MIPI must be connected to a V_{DD}_PLL in a module design since V_{DD}_PLL and V_{DD}_MIPI are tied together in the die.
9. The package pins or die pads used for the parallel interface must be left floating.
10. If the SHUTTER or FLASH pins or pads are not used, then they must be left floating.
11. If the TRIGGER or OE_BAR pin or pad is not used, then it should be tied to D_{GND}.

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12. All power supplies must be adequately decoupled. ON Semiconductor recommends having 10 μF and 0.1 μF decoupling capacitors for every power supply. If space is a concern, then priority must be given in the following order: V_{AA}, V_{AA}_PIX, V_{DD}_PLL, V_{DD}_IO, and V_{DD}. Actual values and results may vary depending on layout and design considerations.
13. To allow for space constraints, ON Semiconductor recommends having 0.1 μF decoupling capacitor inside the module as close to the pads as possible. In addition, place a 10 μF capacitor for each supply off−module but close to each supply.
14. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
15. The pull−up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
16. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
17. TEST pin should be tied to the ground.
18. The data and clock package pins or die pads used for the MIPI interface must be left floating.
19. The V_{DD}_MIPI package pin and sensor die pad should be connected to a 2.8 V supply as it is tied to the V_{DD}_PLL supply both in the package routing and also within the sensor die itself.
20. If the SHUTTER or FLASH pins or pads are not used, then they must be left floating.
21. If the TRIGGER or OE_BAR pin or pad is not used, then it should be tied to D_{GND}.

Figure 3. Typical Configuration: Parallel Pixel Data Interface

PIN DESCRIPTIONS

Table 5. PIN DESCRIPTIONS

Name	Type	Description
RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default
EXTCLK	Input	Master input clock, range 6 – 27 MHz
TRIGGER	Input	Receives slave mode VD signal for frame rate synchronization and trigger to start a GRR frame
S$_{ADDR}$	Input	Two−wire serial address select
S$_{CLK}$	Input	Two−wire serial clock input
TEST	Input	Enable manufacturing test modes. Tie to D$_{GND}$ for normal sensor operation
OE_BAR	Input	Parallel port output enable, active low
S$_{DATA}$	I/O	Two−wire serial data I/O
PIXCLK	Output	Pixel clock out. D$_{OUT}$ is valid on rising edge of this clock
D$_{OUT}$[11:0]	Output	Parallel pixel data output
FLASH	Output	Flash output. Synchronization pulse for external light source. Can be left floating if not used
FRAME_VALID	Output	Asserted when D$_{OUT}$ data is valid
LINE_VALID	Output	LINE_VALID output asserted when D$_{OUT}$ data is valid
SHUTTER	Output	Control for external mechanical shutter. Can be left floating if not used
DATA1_P	Output	MIPI serial data, lane 1, differential P
DATA1_N	Output	MIPI serial data, lane 1, differential N
DATA2_P	Output	MIPI serial data, lane 2, differential P
DATA2_N	Output	MIPI serial data, lane 2, differential N
CLK_P	Output	Output MIPI serial clock, differential P
CLK_N	Output	Output MIPI serial clock, differential N
V$_{DD}$_MIPI	Power	MIPI power supply
V$_{AA}$HV_NPIX	Power	Power supply pin used to program the sensor OTPM (one−time programmable memory). This pin should be open if OTPM is not used
V$_{DD}$	Power	Digital power
V$_{DD}$_IO	Power	IO supply power
V$_{DD}$_PLL	Power	PLL power supply
D$_{GND}$	Power	Digital GND
V$_{AA}$	Power	Analog power
V$_{AA}$_PIX	Power	Pixel power
A$_{GND}$	Power	Analog GND

Table 6. AR0330CS CSP (PARALLEL/MIPI) PACKAGE PINOUT

	1	2	3	4	5	6	7	8
A	V_{AA}	$V_{AA}HV\_NPIX$	A_{GND}	NC	V_{AA}_PIX	V_{AA}	V_{DD}_IO	V_{DD}
B	V_{DD}	S_{DATA}	FRAME_VALID	D_{GND}	A_{GND}	D_{GND}	TEST	SHUTTER
C	S_{ADDR}	FLASH	LINE_VALID	D_{GND}	D_{GND}	D_{GND}	TRIGGER	RESET_BAR
D	S_{CLK}	V_{DD}_IO	$D_{OUT}10$	D_{GND}	V_{DD}_IO	V_{DD}_IO	EXTCLK	DATA_N
E	PIXCLK	$D_{OUT}11$	$D_{OUT}9$	$D_{OUT}7$	V_{DD}_IO	D_{GND}	CLK_N	DATA_P
F	–	–	$D_{OUT}8$	$D_{OUT}6$	$D_{OUT}4$	V_{DD}_IO	CLK_P	V_{DD}_PLL
G	D_{GND}	V_{DD}	$D_{OUT}5$	$D_{OUT}3$	$D_{OUT}1$	$D_{OUT}0$	DATA2_N	V_{DD}
H	–	D_{GND}	D_{GND}	$D_{OUT}2$	V_{DD}_IO	V_{DD}_MIPI	DATA2_P	V_{DD}_MIPI

22. NC = Do not connect. For manufacturing test purpose only.

Table 7. AR0330SR CSP (PARALLEL) PACKAGE PINOUT

	1	2	3	4	5	6	7	8
A	V_{AA}	$V_{AA}HV\_NPIX$	A_{GND}	NC	V_{AA}_PIX	V_{AA}	V_{DD}_IO	V_{DD}
B	V_{DD}	S_{DATA}	FRAME_VALID	D_{GND}	A_{GND}	D_{GND}	TEST	SHUTTER
C	S_{ADDR}	FLASH	LINE_VALID	D_{GND}	D_{GND}	D_{GND}	TRIGGER	RESET_BAR
D	S_{CLK}	V_{DD}_IO	$D_{OUT}10$	D_{GND}	V_{DD}_IO	V_{DD}_IO	EXTCLK	–
E	PIXCLK	$D_{OUT}11$	$D_{OUT}9$	$D_{OUT}7$	V_{DD}_IO	D_{GND}	–	–
F	–	–	$D_{OUT}8$	$D_{OUT}6$	$D_{OUT}4$	V_{DD}_IO	–	V_{DD}_PLL
G	D_{GND}	V_{DD}	$D_{OUT}5$	$D_{OUT}3$	$D_{OUT}1$	$D_{OUT}0$	–	V_{DD}
H	–	D_{GND}	D_{GND}	$D_{OUT}2$	V_{DD}_IO	V_{DD}_PLL	–	V_{DD}_PLL

23. NC = Do not connect. For manufacturing test purpose only.

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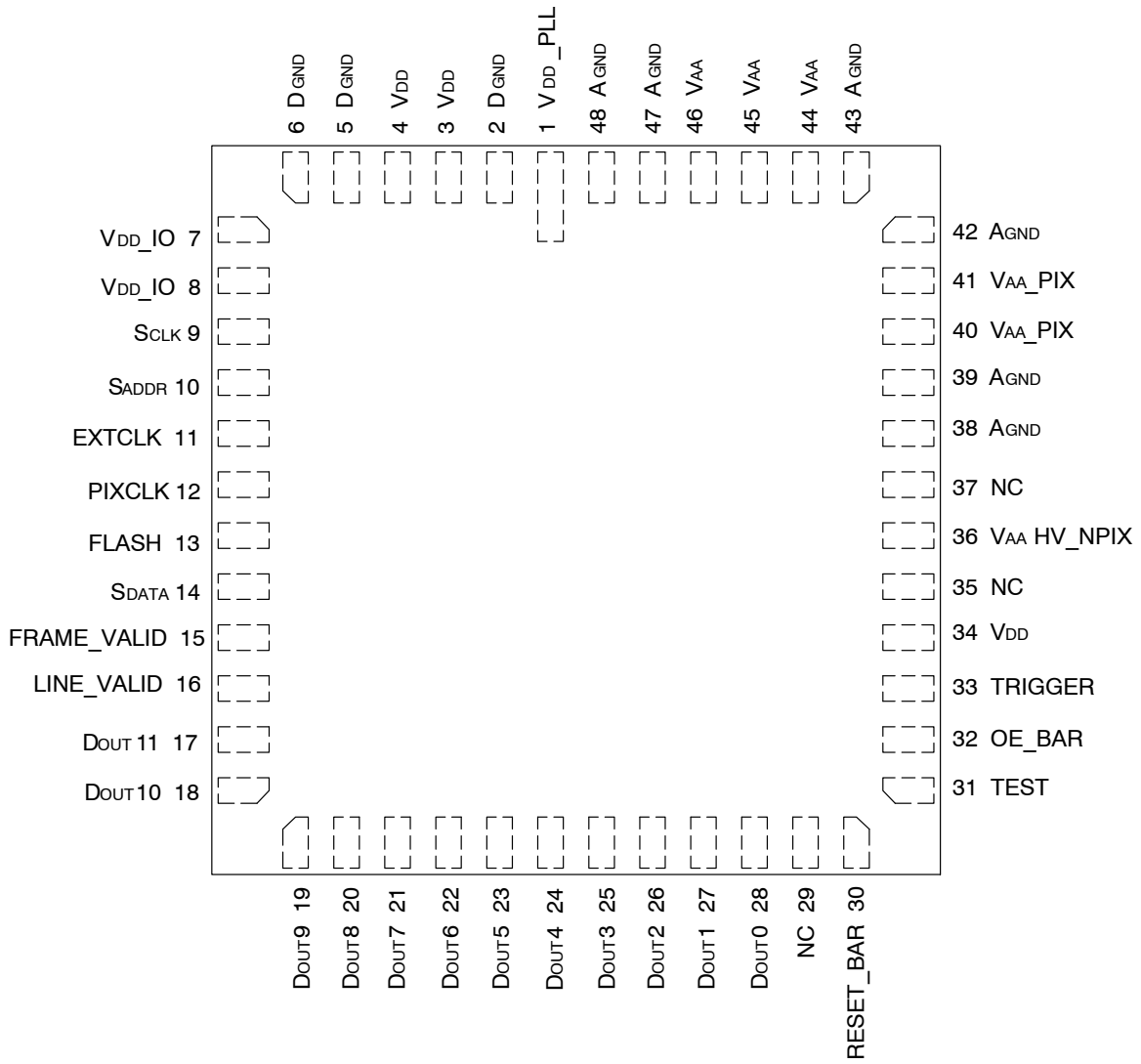
TOP VIEW

Figure 4. PLCC Pinout

Table 8. AR0330CS PLCC PACKAGE THERMAL RESISTANCE

|	Using JEDEC 1S0P Board	Using JEDEC 2S2P Board
Junction to ambient air thermal resistance (θJA) (°C/W)	51.47	36.92
Junction to board thermal resistance (θJB) (°C/W)	22.16	21.73

SENSOR INITIALIZATION

Power−Up Sequence

The recommended power−up sequence for the AR0330CS is shown in Figure 5. The available power supplies (VDD_IO, VDD_PLL, VDD_MIPI, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VDD_PLL and VDD_MIPI power supplies
2. After 100 μs, turn on VAA and VAA_PIX power supply
3. After 100 μs, turn on VDD power supply
4. After 100 μs, turn on VDD_IO power supply
5. After the last power supply is stable, enable EXTCLK
6. Assert RESET_BAR for at least 1ms

7. Wait 150,000 EXTCLKs (for internal initialization into software standby
8. Write R0x3052 = 0xA114 to configure the internal register initialization process
9. Write R0x304A = 0x0070 to start the internal register initialization process
10. Wait 150,000 EXTCLK periods
11. Configure PLL, output, and image settings to desired values
12. Wait 1 ms for the PLL to lock
13. Set streaming mode (R0x301A[2] = 1)
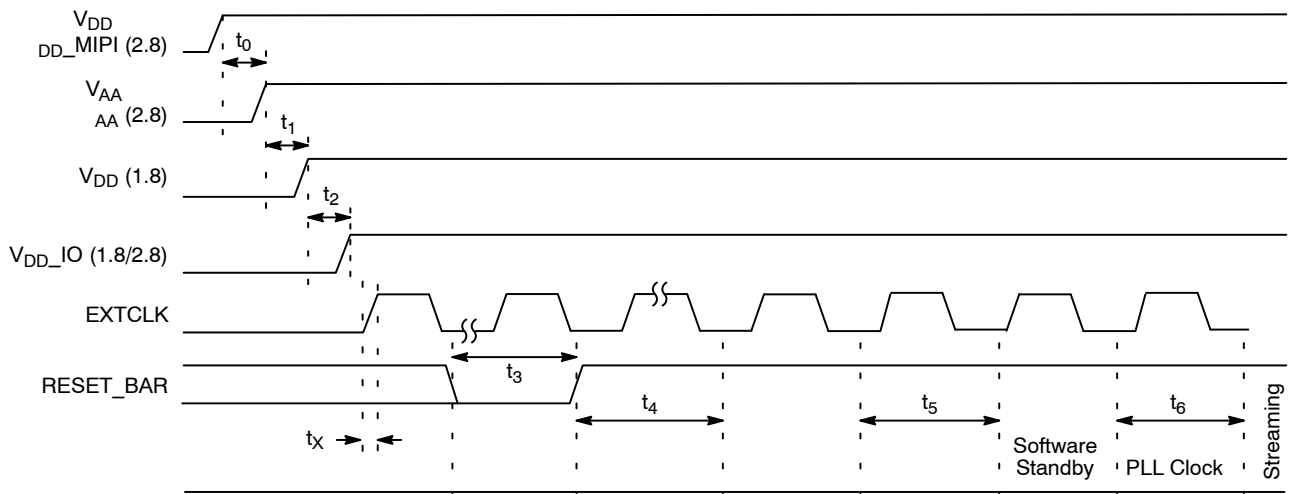
24. A software reset (R0x301A[0] = 1) is not necessary after the procedure described above since a Hard Reset will automatically triggers a software reset. Independently executing a software reset, should be followed by steps seven through thirteen above
25. The sensor must be receiving the external input clock (EXTCLK) before the reset pin is toggled. The sensor will begin an internal initialization sequence when the reset pin toggle from LOW to HIGH. This initialization sequence will run using the external input clock. Power on default state is software standby state, need to apply two−wire serial commands to start streaming. Above power up sequence is a general power up sequence. For different interface configurations, MIPI, and Parallel, some power rails are not needed. Those not needed power rails should be ignored in the general power up sequence..

Figure 5. Power Up

Table 9. POWER−UP SEQUENCE

Definition	Symbol	Min	Typ	Max	Unit
VDD_PLL, VDD_MIPI to VAA/VAA_PIX (Note 28)	t0	0	100	−	μs
VAA/VAA_PIX to VDD	t1	0	100	−	μs
VDD to VDD_IO	t2	0	100	−	μs
External clock settling time	tx	−	30 (Note 26)	−	ms
Hard Reset	t3	1 (Note 27)	−	−	ms
Internal Initialization	t4	150000	−	−	EXTCLKs
Internal Initialization	t5	150000	−	−	EXTCLKs
PLL Lock Time	t6	1	−	−	ms

26. External clock settling time is component−dependent, usually taking about 10 − 100 ms.
27. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
28. It is critical that V_{DD}_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that V_{DD}_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.
29. V_{DD}_MIPI is tied to V_{DD}_PLL in the CSP package and must be powered to 2.8 V.

Power−Down Sequence

The recommended power−down sequence for the AR0330CS is shown in Figure 6. The available power supplies (V_{DD}_IO, V_{DD}_PLL, V_{DD}_MIPI., V_{AA}, V_{AA}_PIX) must have the separation specified below.

    1. Disable streaming if output is active by setting standby R0x301a[2] = 0

2. The soft standby state is reached after the current row or frame, depending on configuration, has ended
3. Turn off V_{DD}_IO
4. Turn off V_{DD}
5. Turn off V_{AA}/V_{AA}_PIX
6. Turn off V_{DD}_PLL, V_{DD}_MIPI
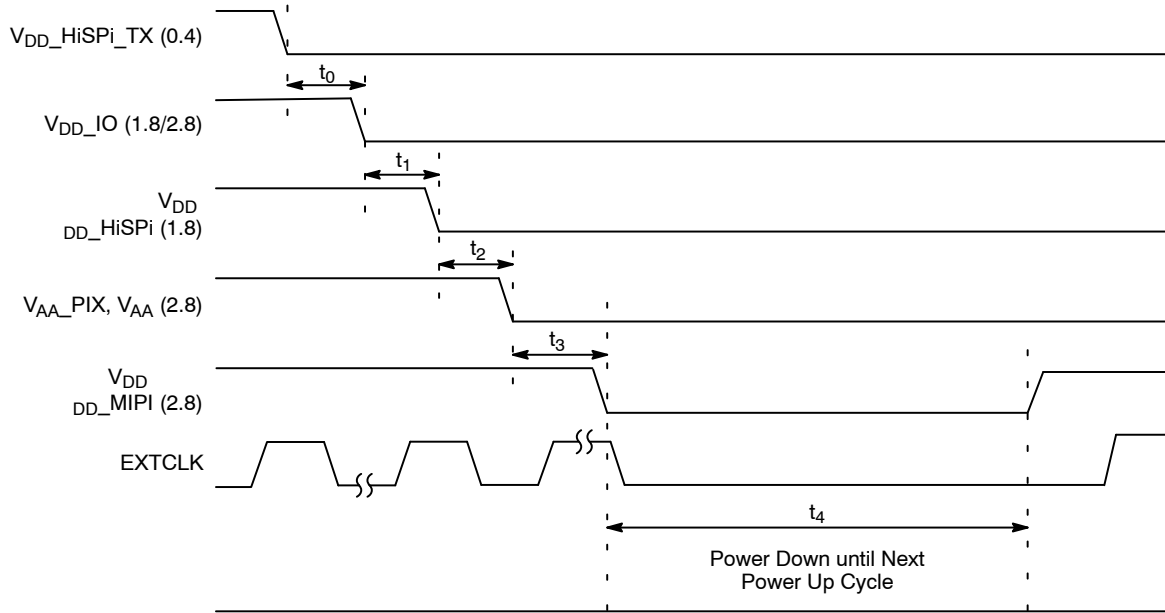
Figure 6. Power Down

Table 10. POWER−DOWN SEQUENCE

Definition	Symbol	Minimum	Typical	Maximum	Unit
V_{DD}_IO	t0	0	–	–	μs
V_{DD}_IO to V_{DD}	t1	0	–	–	μs
V_{DD} to V_{AA}/V_{AA}_PIX	t2	0	–	–	μs
V_{AA}/V_{AA}_PIX to V_{DD}_PLL	t3	0	–	–	μs
PwrDn until Next PwrUp Time	t4	100	–	–	ms

30. t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

STANDBY MODE

Soft Standby
1. Disable streaming by setting standby R0x301a[2] = 0
2. Delay 10 ms
3. Stop EXTCLK; pull EXTCLK pin LOW

Hard Standby
1. Disable streaming by setting standby R0x301a[2] = 0
2. Delay 10 ms
3. Pull RESET_BAR to LOW

ELECTRICAL CHARACTERISTICS

Table 11. DC Electrical Definitions and Characteristics (MIPI Mode)

^{f}EXTCLK = 24 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V;
V_{DD}_PLL = 2.8 V; Output load = 68.5 pF; T_J = 60°C; Data Rate = 588 Mbps; DLL set to 0; 2304 x 1296 at 30 fps

Definition	Symbol	Min	Typ	Max	Unit
Core digital voltage	V_{DD}	1.7	1.8	1.9	V
I/O digital voltage	V_{DD}_IO	1.7	1.8	1.9	V
		2.4	2.8	3.1	V
Analog voltage	V_{AA}	2.76	2.8	2.9	V
Pixel supply voltage	V_{AA}_PIX	2.76	2.8	2.9	V
PLL supply voltage	V_{DD}_PLL	2.7	2.8	2.9	V
MIPI supply voltage	V_{DD}_MIPI	2.7	2.8	2.9	V
Digital operating current		–	114	–	mA
I/O digital operating current		–	0	–	mA
Analog operating current		–	41	–	mA
Pixel supply current		–	9.9	–	mA
PLL supply current		–	15	–	mA
MIPI digital operating current		–	35	–	mA

Table 12. DC Electrical Definitions and Characteristics (Parallel Mode)

f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V;
V_{DD}_PLL = 2.8 V; Output load = 68.5 pF; T_J = 60°C; 2304 x 1296 at 30 fps

Definition	Symbol	Min	Typ	Max	Unit
Core digital voltage	V_{DD}	1.7	1.8	1.9	V
I/O digital voltage	V_{DD}_IO	1.7	1.8	1.9	V
		2.4	2.8	3.1	V
Analog voltage	V_{AA}	2.76	2.8	2.9	V
Pixel supply voltage	V_{AA}_PIX	2.76	2.8	2.9	V
PLL supply voltage	V_{DD}_PLL	2.7	2.8	2.9	V
Digital operating current	I(V_{DD})		66.5	75	mA
I/O digital operating current	I(V_{DD}_IO)		24	35	mA
Analog operating current	I(V_{AA})		36	44	mA
Pixel supply current	I(V_{AA}_PIX)		10.5	18	mA
PLL supply current	I(V_{DD}_PLL)		6	11	mA

Table 13. STANDBY POWER

f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD_IO} = 1.8 V; V_{AA} = 2.8 V; V_{AA_PIX} = 2.8 V;
V_{DD_PLL} = 2.8 V; Output load = 68.5 pF; T_J = 60°C

	Power	Typical	Max	Unit
Hard Standby (CLK OFF)	Digital	19.8	35.8	μA
	Analog	5.8	7.0	μA
Soft Standby (CLK OFF)	Digital	23.5	39.7	μA
	Analog	5.4	5.9	μA
Soft Standby (CLK ON)	Digital	15700	16900	μA
	Analog	5.5	5.7	μA

Table 14. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Unit
V_{DD}_MAX	Core digital voltage	−0.3	2.4	V
V_{DD}_IO_MAX	I/O digital voltage	−0.3	4	V
V_{AA}_MAX	Analog voltage	−0.3	4	V
V_{AA}_PIX	Pixel supply voltage	−0.3	4	V
V_{DD}_PLL	PLL supply voltage	−0.3	4	V
V_{DD}_MIPI	MIPI supply voltage	−0.3	4	V
t_{ST}	Storage temperature	−40	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

31. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
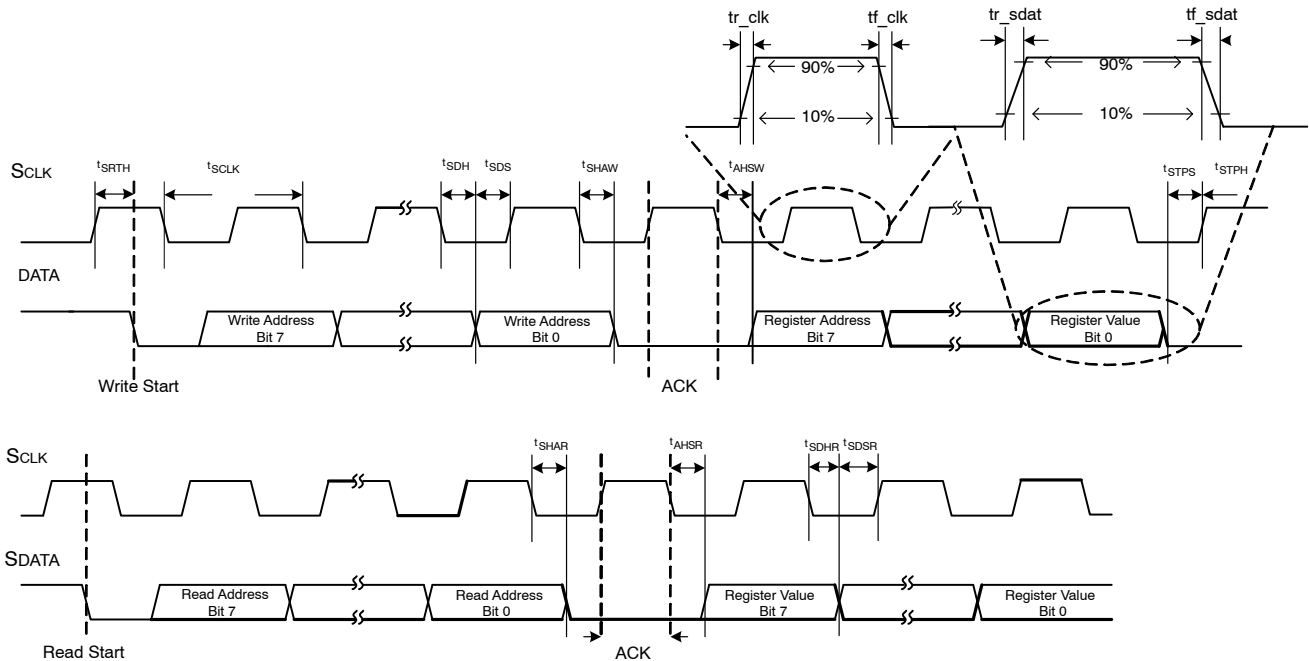
Figure 7. Two−Wire Serial Bus Timing Parameter

Table 15. TWO−WIRE SERIAL BUS CHARACTERISTICS

f_{EXTCLK} = 27 MHz; V_{DD} = 1.8 V; V_{DD_IO} = 2.8 V; V_{AA} = 2.8 V; V_{AA_PIX} = 2.8 V; V_{DD_PLL} = 2.8 V; T_A = 25°C

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
S$_{CLK}$ Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	μs
LOW period of the S$_{CLK}$ clock	t_{LOW}	4.7	–	1.3	–	μs
HIGH period of the S$_{CLK}$ clock	tHIGH	4.0	–	0.6	–	μs
Set−up time for a repeated START condition	tSU;STA	4.7	–	0.6	–	μs
Data hold time	tHD;DAT	0[4]	3.45[5]	0[6]	0.9[5]	μs
Data set−up time	tSU;DAT	250	–	100[6]	–	ns
Rise time of both S$_{DATA}$ and S$_{CLK}$ signals	tr	–	1000	20 + 0.1Cb[7]	300	ns
Fall time of both S$_{DATA}$ and S$_{CLK}$ signals	tf	–	300	20 + 0.1Cb[7]	300	ns
Set−up time for STOP condition	tSU;STO	4.0	–	0.6	–	?s
Bus free time between a STOP and START condition	tBUF	4.7	–	1.3	–	?s
Capacitive load for each bus line	Cb	–	400	–	400	pF
Serial interface input pin capacitance	C_{IN_SI}	–	3.3	–	3.3	pF
S$_{DATA}$ max load capacitance	C_{LOAD_SD}	–	30	–	30	pF
S$_{DATA}$ pull−up resistor	RSD	1.5	4.7	1.5	4.7	K?

32. This table is based on I^{2}C standard (v2.1 January 2000). Philips Semiconductor.
33. Two−wire control is I^{2}C−compatible.
34. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1V_{DD} levels. Sensor EXCLK = 27 MHz.
35. A device must internally provide a hold time of at least 300 ns for the S$_{DATA}$ signal to bridge the undefined region of the falling edge of S$_{CLK}$.
36. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the S$_{CLK}$ signal.
37. A Fast−mode I^{2}C−bus device can be used in a Standard−mode I^{2}C−bus system, but the requirement ^{t}SU; DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S$_{CLK}$ signal. If such a device does stretch the LOW period of the S$_{CLK}$ signal, it must output the next data bit to the S$_{DATA}$ line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard−mode I^{2}C−bus specification) before the S$_{CLK}$ line is released.
38. Cb = total capacitance of one bus line in pF.

Table 16. I/O PARAMETERS

^{f}EXTCLK = 24 MHz; V_{DD} = 1.8V; V_{AA} = 2.8 V; V_{AA_PIX} = 2.8 V; V_{DD_PLL} = 2.8 V; Output load = 68.5 pF; T_J = 60°C; CLK_OP = 98 MPixel/s

Symbol	Definition	Conditions	Min	Max	Units
V$_{IH}$	Input HIGH voltage	V_{DD}_IO = 1.8 V	1.4	V_{DD}_IO + 0.3	V
		V_{DD}_IO = 2.8 V	2.4		
V$_{IL}$	Input LOW voltage	V_{DD}_IO = 1.8 V	GND − 0.3	0.4	
		V_{DD}_IO = 2.8 V	GND − 0.3	0.8	
I$_{IN}$	Input leakage current	No pull−up resistor; V$_{IN}$ = V$_{DD}$ OR D$_{GND}$	−20	20	μA
V$_{OH}$	Output HIGH voltage	At specified I$_{OH}$	V_{DD}_IO − 0.4V	–	V
V$_{OL}$	Output LOW voltage	At specified I$_{OL}$	–	0.4	V
I$_{OH}$	Output HIGH current	At specified V$_{OH}$	–	−12	mA
I$_{OL}$	Output LOW current	At specified V$_{OL}$	–	9	mA
I$_{OZ}$	Tri−state output leakage current		–	10	μA
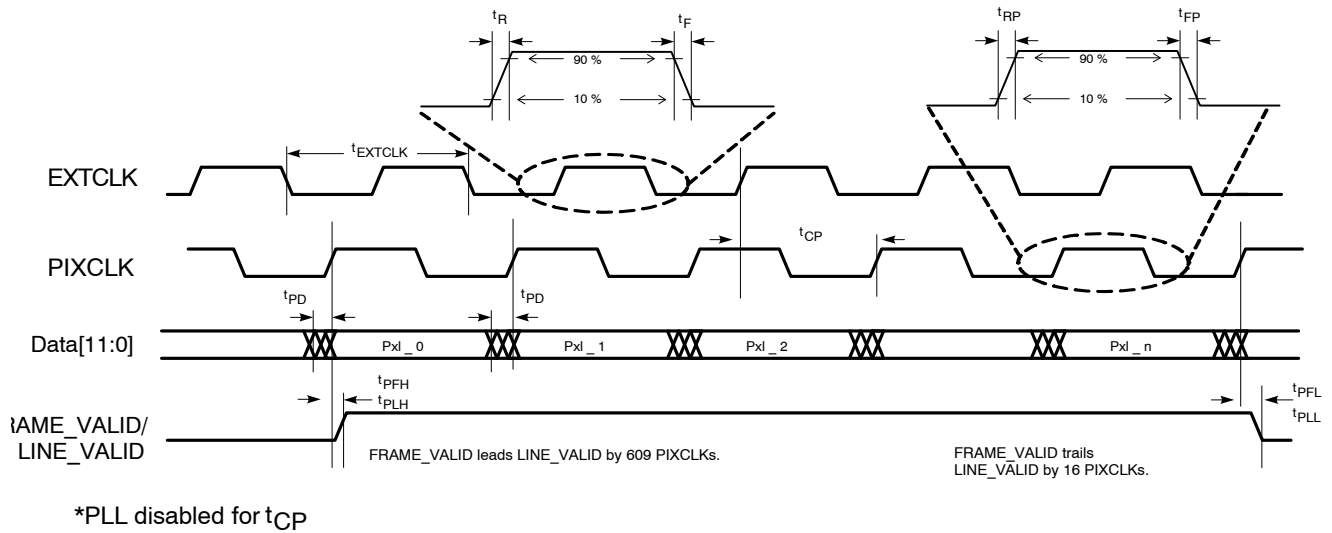
Figure 8. I/O Timing Diagram (Parallel Mode)

Table 17. I/O TIMING

fEXTCLK = 24 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V;
Output load = 68.5 pF; T_J = 60°C; CLK_OP = 98 MPixel/s

Symbol	Definition	Conditions	Min	Typ	Max	Units
fEXTCLK	Input clock frequency	PLL enabled	6	24	27	MHz
tEXTCLK	Input clock period	PLL enabled	166	41	20	ns
tR	Input clock rise time		0.1	–	1	V/ns
tF	Input clock fall time		0.1	–	1	V/ns
	Clock duty cycle		45	50	55	%
tJITTER	Input clock jitter		–	–	0.3	ns
Output pin slew	Fastest	C$_{LOAD}$ = 15 pF	–	0.7	–	V/ns
fPIXCLK	PIXCLK frequency	Default	–	80	–	MHz
tPD	PIXCLK to data valid	Default	–	–	3	ns
tPFH	PIXCLK to FRAME_VALID HIGH	Default	–	–	3	ns
tPLH	PIXCLK to LINE_VALID HIGH	Default	–	–	3	ns
tPFL	PIXCLK to FRAME_VALID LOW	Default	–	–	3	ns
tPLL	PIXCLK to LINE_VALID LOW	Default	–	–	3	ns

Table 18. PARALLEL I/O RISE SLEW RATE

fEXTCLK = 24 MHz; V_{DD} = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; Output load = 68.5 pF;
T_J = 60°C; CLK_OP = 98 MPixel/s

	Parallel Slew Rate (R0x306E[15:13])								
V$_{DD}$_IO	0	1	2	3	4	5	6	7	Units
1.70V	0.069	0.115	0.172	0.239	0.325	0.43	0.558	0.836	V/ns
1.80V	0.078	0.131	0.195	0.276	0.375	0.507	0.667	1.018	
1.95V	0.093	0.156	0.233	0.331	0.456	0.62	0.839	1.283	
2.50V	0.15	0.252	0.377	0.539	0.759	1.07	1.531	2.666	
2.80V	0.181	0.305	0.458	0.659	0.936	1.347	1.917	3.497	
3.10V	0.212	0.361	0.543	0.78	1.114	1.618	2.349	4.14	

ELECTRICAL DEFINITIONS

Figure 9 is the diagram defining differential amplitude V_{OD}, V_{CM}, and rise and fall times. To measure V_{OD} and V_{CM} use the DC test circuit shown in Figure 10 and set the MIPI PHY to constant Logic 1 and Logic 0. Measure V_{oa}, V_{ob} and V_{CM} with voltmeters for both Logic 1 and Logic 0.

Single−ended signal
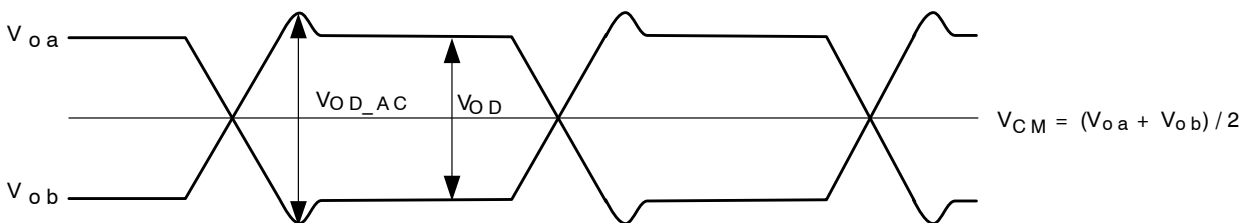
Differential signal
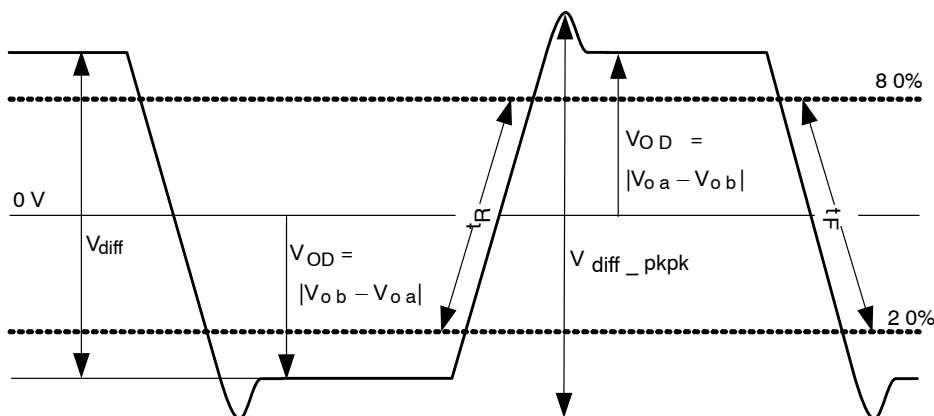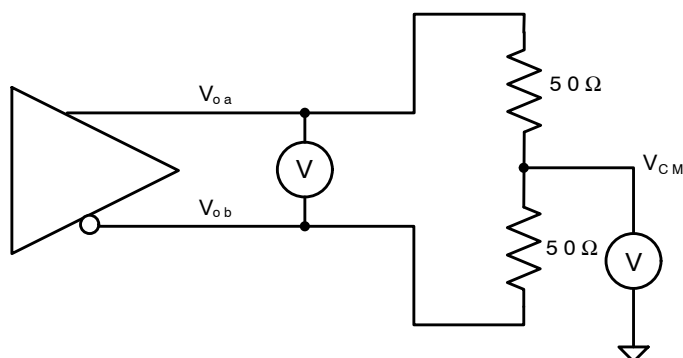
Figure 9. Single−Ended and Differential Signals

Figure 10. DC Test Circuit

$$V_{OD}(m) = \left| V_{oa}(m) - V_{ob}(m) \right| \text{ where 'm' is either ''1'' for logic 1 or ''0'' for logic 0} \tag{eq. 1}$$

$$V_{OD} = \frac{V_{OD}(1) + V_{OD}(0)}{2} \tag{eq. 2}$$

$$V_{diff} = V_{OD}(1) + V_{OD}(0) \tag{eq. 3}$$

$$\Delta V_{OD} = \left| V_{OD}(1) - V_{OD}(0) \right| \tag{eq. 4}$$

$$V_{CM} = \frac{V_{CM}(1) + V_{CM}(0)}{2} \tag{eq. 5}$$

$$\Delta V_{CM} = \left| V_{CM}(1) - V_{CM}(0) \right| \qquad \text{(eq. 6)}$$

Both V_{OD} and V_{CM} are measured for all output channels. The worst case ΔV_{OD} is defined as the largest difference in V_{OD} between all channels regardless of logic level. And the worst case ΔV_{CM} is similarly defined as the largest difference in V_{CM} between all channels regardless of logic level.

Timing Definitions
1. Timing measurements are to be taken using the Square Wave test mode
2. Rise and fall times are measured between 20% to 80% positions on the differential waveform, as shown in Figure 9: "Single−Ended and Differential Signals"
3. Mean Clock−to−Data skew should be measured from the 0V crossing point on Clock to the 0V crossing point on any Data channel regardless of edge, as shown in Figure 11. This time is compared with the ideal Data transition point of 0.5UI with the difference being the Clock−to−Data Skew (see Equation 7)
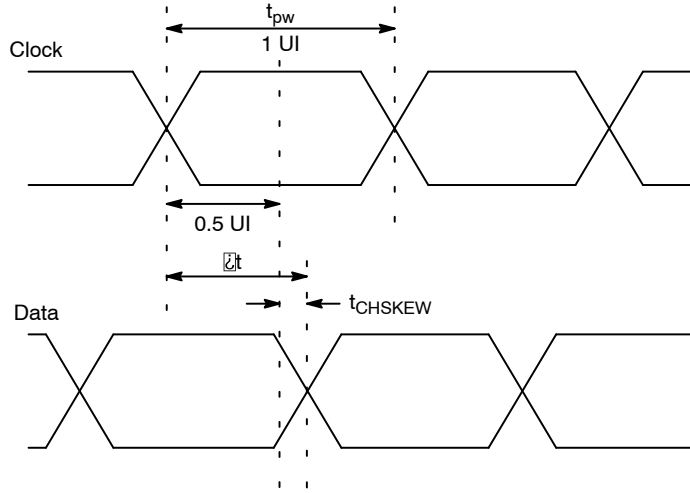
Figure 11. Clock−to−Data Skew Timing Diagram

$$t_{CHSKEW}(ps) = \Delta t - \frac{t_{pw}}{2} \qquad \text{(eq. 7)}$$

$$t_{CHSKEW}(UI) = \frac{\Delta t}{t_{pw}} - 0.5 \qquad \text{(eq. 8)}$$

4. The differential skew is measured on the two single−ended signals for any channel. The time is taken from a transition on V_{oa} signal to corresponding transition on V_{ob} signal at V_{CM} crossing point
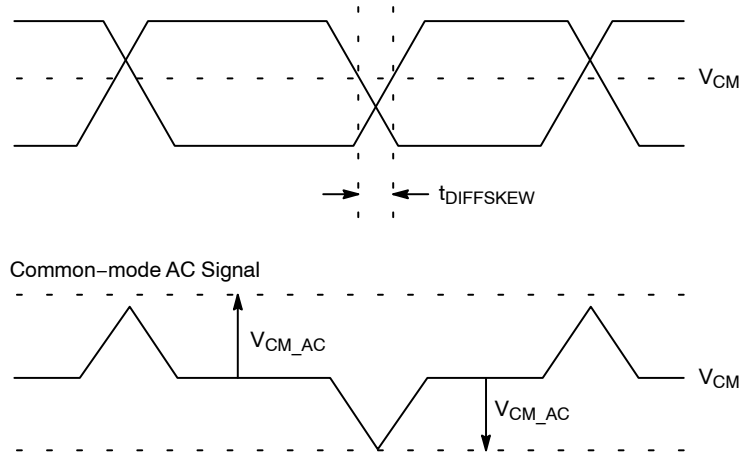
Figure 12. Differential Skew

Figure 12 also shows the corresponding AC V_{CM} common−mode signal. Differential skew between the V_{oa} and V_{ob} signals can cause spikes in the common−mode, which the receiver needs to be able to reject. V_{CM_AC} is measured as the absolute peak deviation from the mean DC V_{CM} common−mode.

Transmitter Eye Mask
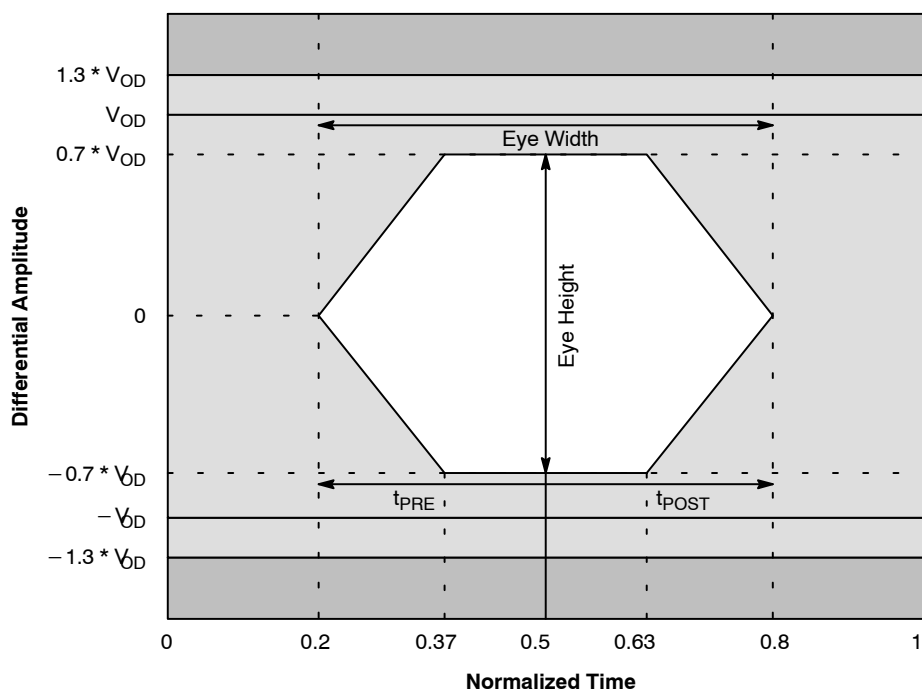
Figure 13. Transmitter Eye Mask

Figure 13 defines the **eye mask** for the transmitter. 0.5 UI point is the instantaneous crossing point of the Clock. The area in white shows the area Data is prohibited from crossing into. The **eye mask** also defines the minimum eye height, the data **t$_{pre}$** and **t$_{post}$** times, and the **total jitter pk−pk +mean skew (t$_{TJSKEW}$)** for Data.

Clock Signal

t_{HCLK} is defined as the high clock period, and t_{LCLK} is defined as the low clock period as shown in Figure 14. The clock duty cycle D_{CYC} is defined as the percentage time the clock is either high (t_{HCLK}) or low (t_{LCLK}) compared with the clock period T.
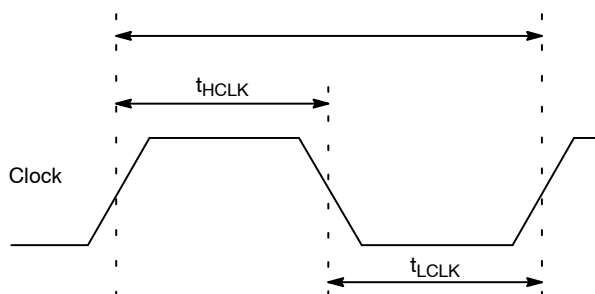
Figure 14. Clock Duty Cycle

$$D_{CYC}(1) = \frac{t_{HCLK}}{T} \qquad \text{(eq. 9)}$$

$$D_{CYC}(0) = \frac{t_{LCLK}}{T} \qquad \text{(eq. 10)}$$

$$t_{pw} = \frac{T}{2} \quad \text{(i.e, 1 UI)} \qquad \text{(eq. 11)}$$

$$\text{Bitrate} = \frac{1}{t_{pw}} \qquad \text{(eq. 12)}$$

Figure 15 shows the definition of clock jitter for both the period and the cycle−to−cycle jitter.
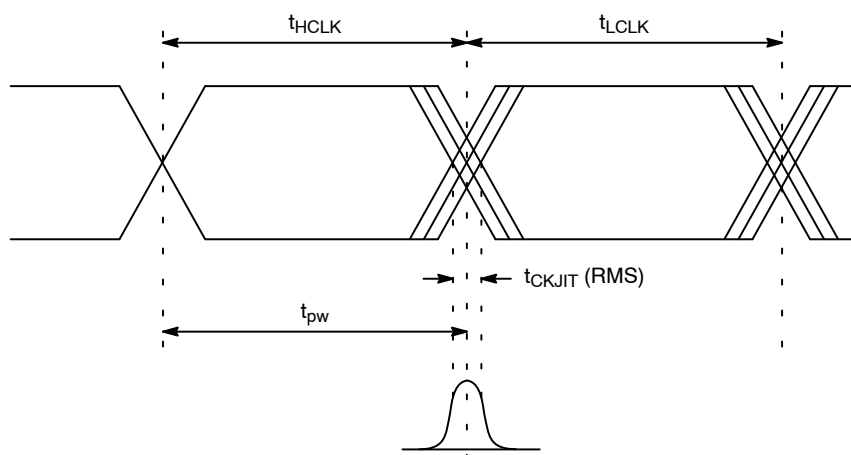
Figure 15. Clock Jitter

Period Jitter (t_{CKJIT}) is defined as the deviation of the instantaneous clock t_{PW} from an ideal 1UI. This should be measured for both the clock high period variation Δt_{HCLK}, and the clock low period variation Δt_{LCLK} taking the RMS or 1−sigma standard deviation and quoting the worse case jitter between Δt_{HCLK} and Δt_{LCLK}.

If pk−pk jitter is also measured, this should be limited to ±3−sigma.

SEQUENCER

The sequencer digital block determines the order and timing of operations required to sample pixel data from the array during each row period. It is controlled by an instruction set that is programmed into RAM from the sensor OTPM (One Time Programmable Memory). The OTPM is configured during production.

The instruction set determines the length of the sequencer operation that determines the "ADC Readout Limitation" (Equation 5) listed in the Sensor Frame−Rate section. The instruction set can be shortened through register writes in order to achieve faster frame rates. Instructions for shortening the sequencer can be found in the AR0330CS Developer Guide.

The sequencer digital block can be reprogrammed using the following instructions:

Program a new sequencer.
1. Place the sensor in standby
2. Write 0x8000 to R0x3088 ("seq_ctrl_port")
3. Write each instruction incrementally to R0x3086 Each write must be 16−bit consisting of two bytes {Byte[N], Byte[N+1]}
4. If the sequencer consists of an odd number of bytes, set the last byte to "0"

Read the instructions stored in the sequencer.
1. Place the sensor in standby
2. Write 0xC000 to R0x3088 ("seq_ctrl_port")
3. Sequentially read 2−bytes at a time from R0x3086

SENSOR PLL

VCO

EXTCLK (6–27 MHz) → pre_pll_clk_div 2 (1–64) → pll_multiplier 58 (32–384) → F_{VCO}
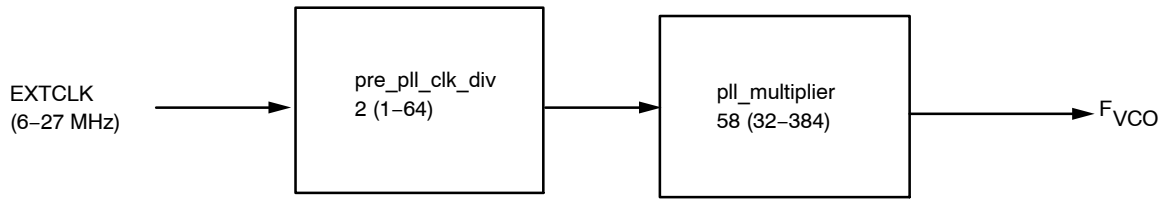
Figure 16. Relationship Between Readout Clock and Peak Pixel Rate

The sensor contains a phase−locked loop (PLL) that is used for timing generation and control. The required VCO clock frequency is attained through the use of a pre−PLL clock divider followed by a multiplier. The multiplier is followed by set of dividers used to generate the output clocks required for the sensor array, the pixel analog and digital readout paths, and the output parallel and serial interfaces.

Dual Readout Paths

There are two readout paths within the sensor digital block.

Pixel Rate = 2 x CLK_PIX
= # data lanes x CLK_OP (Parallel or MIPI)
= CLK_OP (Parallel)
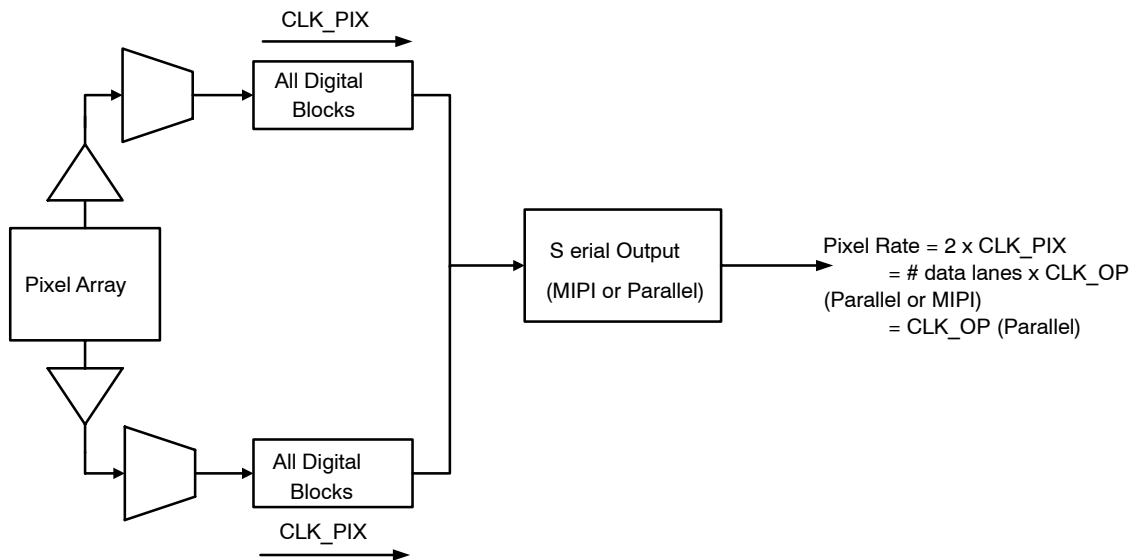
Figure 17. Sensor Dual Readout Paths

The sensor row time calculations refers to each data−path individually. For example, the sensor default configuration uses 1248 clocks per row (line_length_pck) to output 2304 active pixels per row. The aggregate clocks per row seen by the receiver will be 2496 clocks (1248 x 2 readout paths).

Parallel PLL Configuration

EXTCLK (6–27 MHz) → pre_pll_clk_div 2 (1–64) → pll_multiplier 58 (32 – 384) → F_{VCO} → vt_sys_clk_div 1 (1, 2, 4, 6, 8, 10, 12, 14, 16) → vt_pix_clk_div 6 (4–16) → CLK_OP (Max 98 MPixel/s)
→ 1/2 → CLK_PIX (Max 49 MPixels/s)
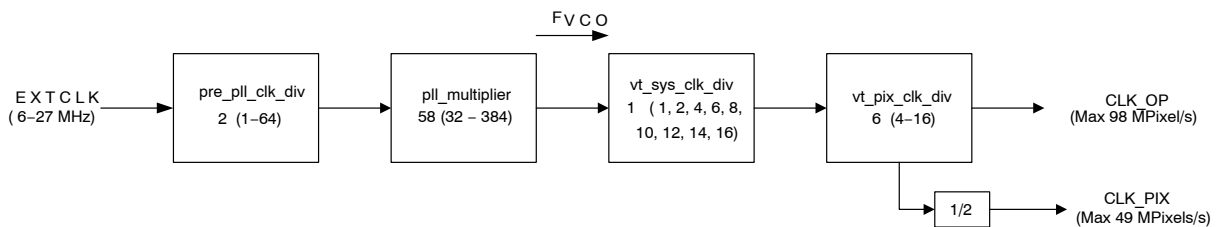
Figure 18. PLL for the Parallel Interface

The maximum output of the parallel interface is 98 Mpixel/s (CLK_OP). This will limit the readout clock (CLK_PIX) to 49 MHz. The sensor will not use the F_{SERIAL}, F_{SERIAL_CLK} when configured to use the parallel interface.
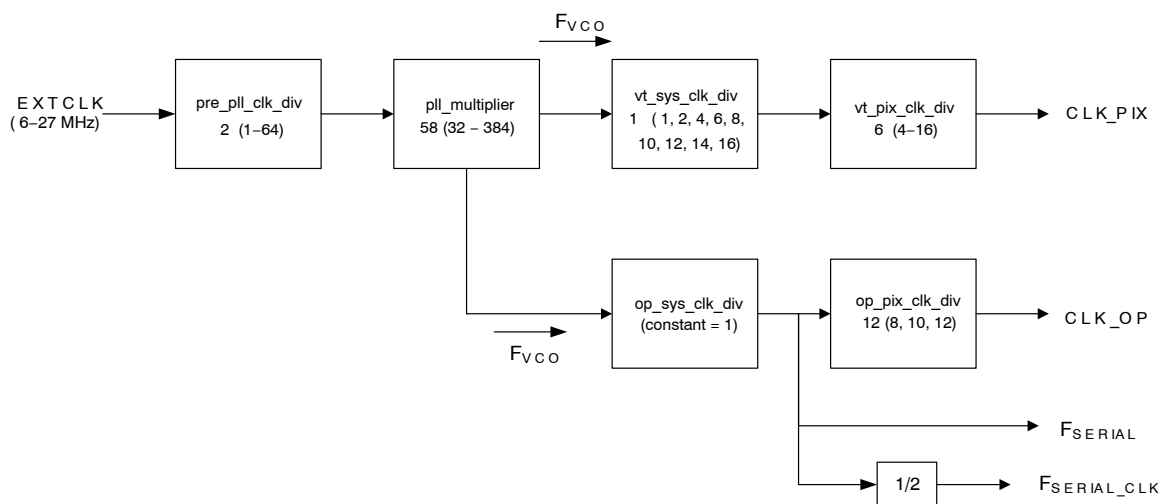
Table 19. PLL PARAMETERS FOR THE PARALLEL INTERFACE

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	27	MHz
VCO Clock	F_{VCO}	384	768	MHz
Readout Clock	CLK_PIX		49	MHz
Output Clock	CLK_OP		98	Mpixel/s

Table 20. EXAMPLE PLL CONFIGURATION FOR THE PARALLEL INTERFACE

Parameter	Value	Output
F_{VCO}		588 MHz (Max)
vt_sys_clk_div	1	
vt_pix_clk_div	6	
CLK_PIX		49 MHz (CLK_OP/2)
CLK_OP		98 Mpixel/s (= 588 MHz / 6)
Output pixel rate		98 MPixel/s

Serial PLL Configuration

Figure 19. PLL for the Serial Interface

The sensor will use op_sys_clk_div and op_pix_clk_div to configure the output clock per lane (CLK_OP). The configuration will depend on the number of active lanes (1 or 2) configured. To configure the sensor protocol and number of lanes, refer to "Serial Configuration".

Table 21. PLL PARAMETERS FOR THE SERIAL INTERFACE

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	27	MHz
VCO Clock	F_{VCO}	384	768	MHz
Readout Clock	CLK_PIX		98	MHz
Output Clock	CLK_OP		98	Mpixel/s
Output Serial Data Rate Per Lane	F_{SERIAL}	384 (MIPI)	768 (MIPI)	Mbps
Output Serial Clock Speed Per Lane	F_{SERIAL_CLK}	192 (MIPI)	384 (MIPI)	MHz

The serial output should be configured so that it adheres to the following rules:
- The maximum data−rate per lane (F_{SERIAL}) is 768 Mbps/lane (MIPI)

- The output pixel rate per lane (CLK_OP) should be configured so that the sensor output pixel rate matches the peak pixel rate (2 x CLK_PIX)
  - 2−lane: 2 x CLK_OP = 2 x CLK_PIX = Pixel Rate
  - 1−lane: 1 x CLK_OP = 2 x CLK_PIX = Pixel Rate

Table 22. EXAMPLE PLL CONFIGURATIONS FOR THE SERIAL INTERFACE

Parameter	2−lane		1−lane			Notes
	12−bit	10−bit	12−bit	10−bit	8−bit	
F_{VCO}	768	760	768	768	768	MHz
vt_sys_clk_div	2	2	4	4	4	
vt_pix_clk_div	6	5	6	5	4	
op_sys_clk_div	1	1	1	1	1	
op_pix_clk_div	12	10	12	10	8	
F_{SERIAL}	768	760	768	768	768	MHz
F_{SERIAL_CLK}	384	380	384	384	384	MHz
CLK_PIX	64	76	32	38.4	48	MHz
CLK_OP	64	76	64	76.8	96	Mpixel/s
Pixel Rate	128	144	64	76.8	96	Mpixel/s

PIXEL OUTPUT INTERFACES

Parallel Interface

The parallel pixel data interface uses these output−only signals:
- FV
- LV
- PIXCLK
- $D_{OUT}[11:0]$

The parallel pixel data interface is disabled by default at power up and after reset. It can be enabled by programming R0x301A. Table 24 shows the recommended settings.

When the parallel pixel data interface is in use, the serial data output signals can be left unconnected. Set reset_register[12] to disable the serializer while in parallel output mode.

Output Enable Control

When the parallel pixel data interface is enabled, its signals can be switched asynchronously between the driven and High−Z under pin or register control, as shown in Table 23.

Table 23. OUTPUT ENABLE CONTROL

OE_BAR Pin	Drive Signals R0x301A–B[6]	Description
Disabled	0	Interface High–Z
Disabled	1	Interface driven
1	0	Interface High–Z
X	1	Interface driven
0	X	Interface driven

Configuration of the Pixel Data Interface

Fields in R0x301A are used to configure the operation of the pixel data interface. The supported combinations are shown in Table 23.

Table 24. CONFIGURATION OF THE PIXEL DATA INTERFACE

Serializer Disable R0x301 A–B[12]	Parallel Enable R0x301A–B[7]	Standby End–of–Frame R0x301A–B[4]	Description
0	0	1	Power up default. Serial pixel data interface and its clocks are enabled. Transitions to soft standby are synchronized to the end of frames on the serial pixel data interface
1	1	0	Parallel pixel data interface, sensor core data output. Serial pixel data interface and its clocks disabled to save power. Transitions to soft standby are synchronized to the end of the current row readout on the parallel pixel data interface
1	1	1	Parallel pixel data interface, sensor core data output. Serial pixel data interface and its clocks disabled to save power. Transitions to soft standby are synchronized to the end of frames in the parallel pixel data interface

MIPI Interface

The serial pixel data interface uses the following output–only signal pairs:
- DATA1_P
- DATA1_N
- DATA2_P
- DATA2_N
- CLK_P
- CLK_N

The signal pairs use both single–ended and differential signaling, in accordance with the the MIPI Alliance Specification for D–PHY v1.00.00. The serial pixel data interface is enabled by default at power up and after reset.

The DATA0_P, DATA0_N, DATA1_P, DATA1_N, CLK_P and CLK_N pads are set to the Ultra Low Power State (ULPS) if the serial disable bit is asserted (R0x301A–B[12] = 1) or when the sensor is in the hardware standby or soft standby system states.

When the serial pixel data interface is used, the LINE_VALID, FRAME_VALID, PIXCLK and Dout[11:0] signals (if present) can be left unconnected.

Serial Configuration

The serial format should be configured using R0x31AC. This register should be programmed to 0x0C0C when using the parallel interface.

The R0x0112–3 register can be programmed to any of the following data format settings that are supported:
- 0x0C0C – Sensor supports RAW12 uncompressed data format
- 0x0C0A – The sensor supports RAW12 compressed format (10–bit words) using 12–10 bit A–LAW Compression. See "Compression"
- 0x0A0A – Sensor supports RAW10 uncompressed data format. This mode is supported by discarding all but the upper 10 bits of a pixel value
- 0x0808 – Sensor supports RAW8 uncompressed data format. This mode is supported by discarding all but the upper 8 bits of a pixel value (MIPI only)

The serial_format register (R0x31AE) register controls which serial interface is in use when the serial interface is

enabled (reset_register[12] = 0). The following serial formats are supported:

- 0x0201 – Sensor supports single−lane MIPI operation
- 0x0202 – Sensor supports dual−lane MIPI operation

The MIPI timing registers must be configured differently for 10−bit or 12−bit modes. These modes should be configured when the sensor streaming is disabled. See Table 25.

- 0x0A0A – Sensor supports RAW10 uncompressed data format. This mode is supported by discarding all but the upper 10 bits of a pixel value
- 0x0808 – Sensor supports RAW8 uncompressed data format. This mode is supported by discarding all but the upper 8 bits of a pixel value (MIPI only)

The serial_format register (R0x31AE) register controls which serial interface is in use when the serial interface is enabled (reset_register[12] = 0). The following serial formats are supported:

- 0x0201 – Sensor supports single−lane MIPI operation
- 0x0202 – Sensor supports dual−lane MIPI operation

The MIPI timing registers must be configured differently for 10−bit or 12−bit modes. These modes should be configured when the sensor streaming is disabled. See Table 25.

Table 25. RECOMMENDED MIPI TIMING CONFIGURATION

Register	Configuration		Description
	10−bit, 490 Mbps/lane	12−bit, 588 Mbps/lane	
	Clocking: Continuous		
0x31B0	40	36	Frame Preamble
0x31B2	14	12	Line Preamble
0x31B4	0x2743	0x2643	MIPI Timing 0
0x31B6	0x114E	0x114E	MIPI Timing 1
0x31B8	0x2049	0x2048	MIPI Timing 2
0x31BA	0x0186	0x0186	MIPI Timing 3
0x31BC	0x8005	0x8005	MIPI Timing 4
0x31BE	0x2003	0x2003	MIPI Config Status

PIXEL SENSITIVITY

Row Integration

($T_{INTEGRATION}$)

Row Reset

(Start of integration)

Row Readout
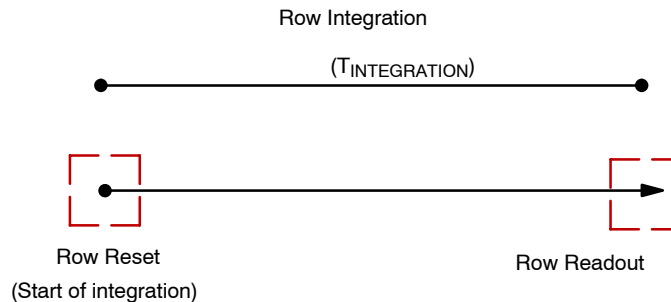
Figure 20. Integration Control in ERS Readout

A pixel's integration time is defined by the number of clock periods between a row's reset and read operation. Both the read followed by the reset operations occur within a row period (T_{ROW}) where the read and reset may be applied to different rows. The read and reset operations will be applied to the rows of the pixel array in a consecutive order.

The integration time in an ERS frame is defined as:

$$T_{INTEGRATION} = T_{COARSE} - T_{FINE} \qquad \text{(eq. 13)}$$

The coarse integration time is defined by the number of row periods (T_{ROW}) between a row's reset and the row read. The row period is the defined as the time between row read operations (see Sensor Frame Rate).

$$T_{COARSE} = T_{ROW} \times \text{coarse\_inegration\_time} \qquad \text{(eq. 14)}$$
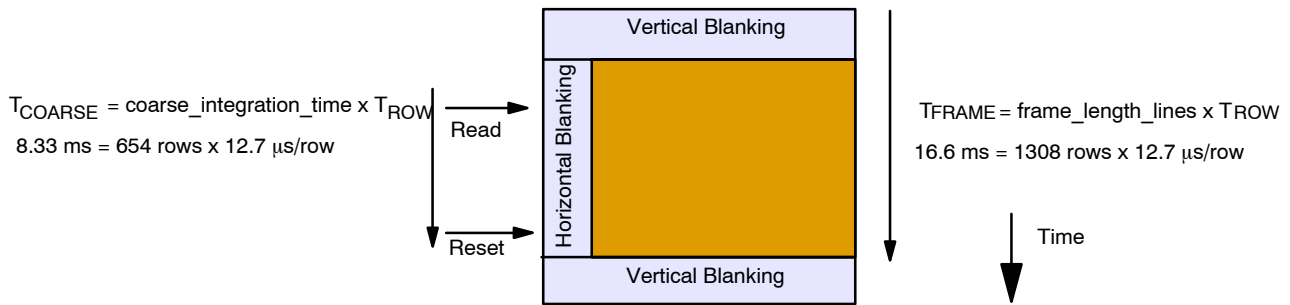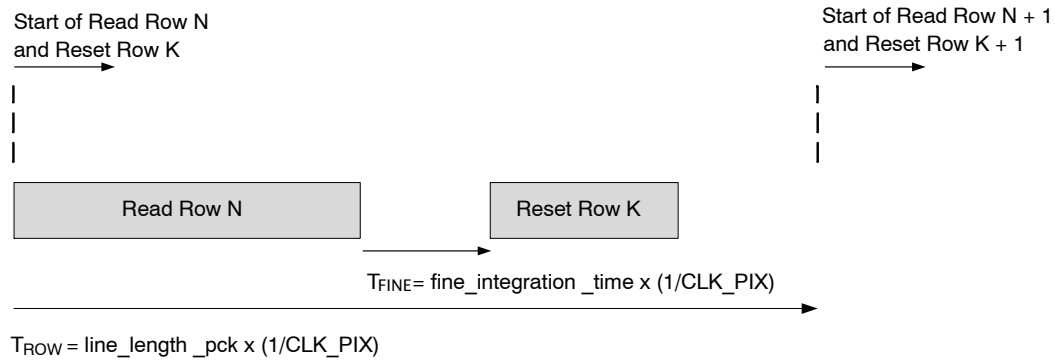
Figure 21. Example of 8.33 ms Integration in 16.6 ms Frame

The fine integration is then defined by the number of pixel clock periods between the row reset and row read operation within T_{ROW}. This period is defined by the *fine_integration_time* register.
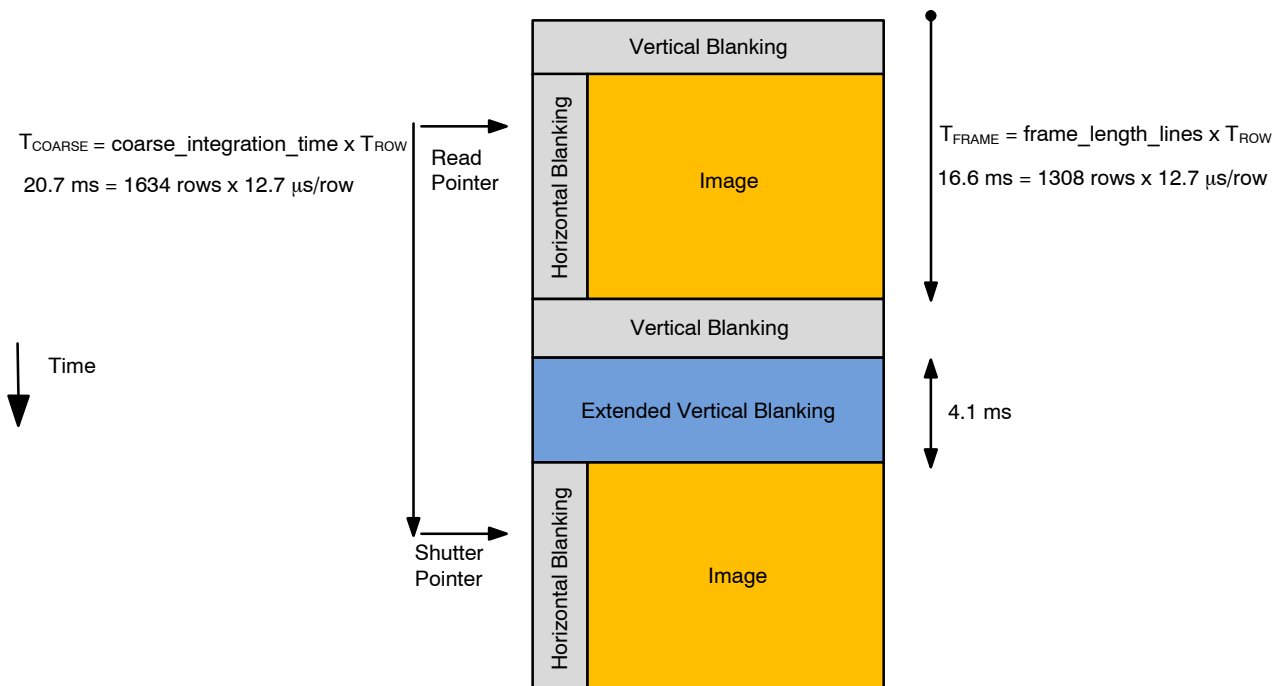

Figure 22. Row Read and Row Reset Showing Fine Integration

$$T_{FINE} = fine\_inegration\_time/clk\_pix \qquad \text{(eq. 15)}$$

The maximum allowed value for fine_integration_time is *line_length_pck − 1204*.

ON Semiconductor recommends that the fine_integration_time in the AR0330CS be left at zero.

Figure 23. The Row Integration Time is Greater Than the Frame Readout Time

The minimum frame−time is defined by the number of row periods per frame and the row period. The sensor frame−time will increase if the *coarse_integration_time* is set to a value equal to or greater than the f*rame_length_lines*. The maximum integration time can be limited to the frame time by setting R0x30CE[5] to 1.

GAIN STAGES

The analog gain stages of the AR0330CS sensor are shown in Figure 24. The sensor analog gain stage consists of column amplifiers and a variable ADC reference. The sensor will apply the same analog gain to each color channel. Digital gain can be configured to separate levels for each color channel.

Coarse Gain:
1x, 2x, 4x, 8x
Fine Gain:
1–2x: 16 steps
2–4x: 8 steps
4–8x: 4 steps

ADC Reference

Digital Gain with Dithering

1x to 15.992x
(128 steps per 6dB)
"xxxx.Yyyy"
xxxx(15–0)
yyyyyyy(127/128 to 0)
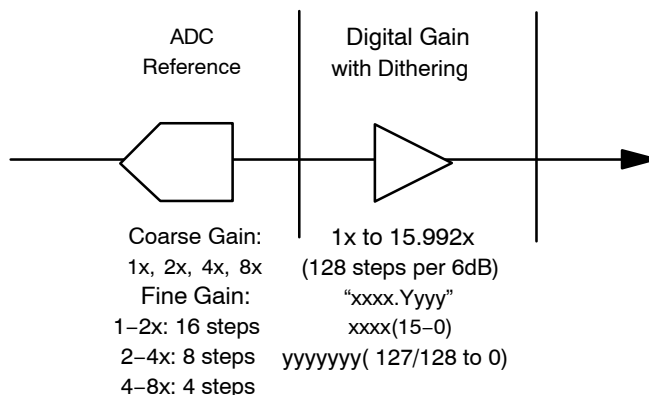
Figure 24. Gain Stages in AR0330CS Sensor

The level of analog gain applied is controlled by the coarse_gain and fine_gain registers. The analog readout can be configured differently for each gain level. The recommended gain tables are listed in Table 26. It is recommended that these registers are configured before streaming images.

Table 26. RECOMMENDED SENSOR ANALOG GAIN TABLES

COARSE_GAIN		FINE_GAIN		Total Gain		COARSE_GAIN		FINE_GAIN		Total Gain	
R0x3060 [5:4]	Gain (x)	R0x3060[3:0]	Gain (x)	(x)	(dB)	R0x3060 [5:4]	Gain (x)	R0x3060 [3:0]	Gain (x)	(x)	(dB)
0	1	0	1.00	1.00	0.00	0	1x	15	1.88	1.88	5.49
0	1	1	1.03	1.03	0.26	1	2x	0	1.00	2.00	6.00
0	1	2	1.07	1.07	0.56	1	2x	2	1.07	2.13	6.58
0	1	3	1.10	1.10	0.86	1	2x	4	1.14	2.29	7.18
0	1	4	1.14	1.14	1.16	1	2x	6	1.23	2.46	7.82
0	1	5	1.19	1.19	1.46	1	2x	8	1.33	2.67	8.52
0	1	6	1.23	1.23	1.80	1	2x	10	1.45	2.91	9.28
0	1	7	1.28	1.28	2.14	1	2x	12	1.60	3.20	10.10
0	1	8	1.33	1.33	2.50	1	2x	14	1.78	3.56	11.02
0	1	9	1.39	1.39	2.87	2	4x	0	1.00	4.00	12.00
0	1	10	1.45	1.45	3.25	2	4x	4	1.14	4.57	13.20
0	1	11	1.52	1.52	3.66	2	4x	8	1.33	5.33	14.54
0	1	12	1.60	1.60	4.08	2	4x	12	1.60	6.40	16.12
0	1	13	1.68	1.68	4.53	3	8x	0	1.00	8.00	18.00
0	1	14	1.78	1.78	5.00						

Each digital gain can be configured from a gain of 0 to 15.992. The digital gain supports 128 gain steps per 6dB of gain. The format of each digital gain register is "xxxx.yyyyyyy" where "xxxx" refers an integer gain of 1 to 15 and "yyyyyyy" is a fractional gain ranging from 0/128 to 127/128.

The sensor includes a digital dithering feature to reduce quantization resulting from using digital gain can be implemented by setting R0x30BA[5] to 1. The default value is 0. Refer to "Real−Time Context Switching" for the analog and digital gain registers in both context A and context B modes.

Refer to "Real−Time Context Switching" for the analog and digital gain registers in both context A and context B modes.

DATA PEDESTAL

The data pedestal is a constant offset that is added to pixel values at the end of datapath. The default offset is 168 and is a 12−bit offset. This offset matches the maximum range used by the corrections in the digital readout path.

The data pedestal value can be changed if the lock register bit (R0x301A[3]) is set to "0". This bit is set to "1" by default.

SENSOR READOUT

Image Acquisition Modes

The AR0330CS supports two image acquisition modes:
1. Electronic rolling shutter (ERS) mode
   This is the normal mode of operation. When the AR0330CS is streaming; it generates frames at a fixed rate, and each frame is integrated (exposed) using the ERS. When the ERS is in use, timing and control logic within the sensor sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and subsequently reading that row, the pixels in the row integrate incident light. The integration (exposure) time is controlled by varying the time between row reset and row readout. For each row in a frame, the time between row reset and row readout is the same, leading to a uniform integration time across the frame. When the integration time is changed (by using the two−wire serial interface to change register settings), the timing and control logic controls the transition from old to new integration time in such a way that the stream of output frames from the AR0330CS switches cleanly from the old integration time to the new while only generating frames with uniform integration. See "Changes to Integration Time" in the AR0330CS Register Reference
2. Global reset mode
   This mode can be used to acquire a single image at the current resolution. In this mode, the end point of the pixel integration time is controlled by an external electromechanical shutter, and the AR0330CS provides control signals to interface to that shutter.
   The benefit of using an external electromechanical shutter is that it eliminates the visual artifacts associated with ERS operation. Visual artifacts arise in ERS operation, particularly at low frame rates, because an ERS image effectively integrates each row of the pixel array at a different point in time

Window Control

The sequencing of the pixel array is controlled by the x_addr_start, y_addr_start, x_addr_end, and y_addr_end registers. The x_addr_start equal to 6 is the minimum setting value. The y_addr_start equal to 6 is the minimum setting value. Please refer to Table 27 and Table 28 for details.

Table 27. PIXEL COLUMN CONFIGURATION

Column Address	Number	Type	Notes
0–5	6	Active	Border columns
6–2309	2304	Active	Active columns
2310–2315	6	Active	Border columns

Table 28. PIXEL ROW CONFIGURATION

Row Address	Number	Type	Notes
2–5	4	Active	Not used in case of "edge effects"
6–1549	1544	Active	Active rows
1550–1555	6	Active	Not used in case of "edge effects"

AR0330CS

Readout Modes

Horizontal Mirror

When the horizontal_mirror bit (R0x3040[14]) is set in the image_orientation register, the order of pixel readout within a row is reversed, so that readout starts from x_addr_end + 1 and ends at x_addr_start. Figure 25 shows a

sequence of 6 pixels being read out with R0x3040[14] = 0 and R0x3040[14] = 1. Changing R0x3040[14] causes the Bayer order of the output image to change; the new Bayer order is reflected in the value of the pixel_order register.
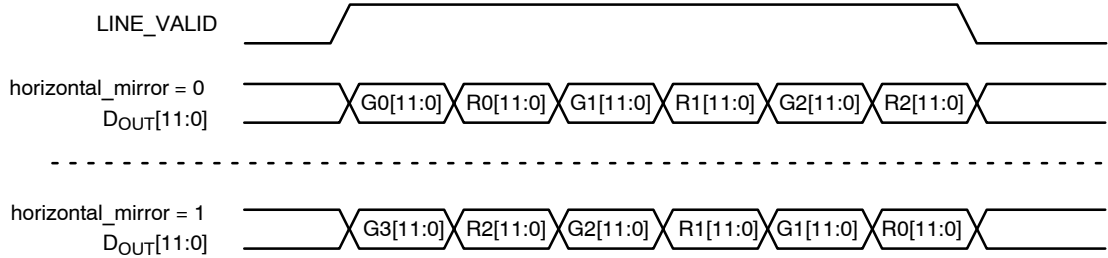
Figure 25. Effect of Horizontal Mirror on Readout Order

Vertical Flip

When the vertical_flip bit (R0x3040[15]) is set in the image_orientation register, the order in which pixel rows are read out is reversed, so that row readout starts from y_addr_end and ends at y_addr_start. Figure 30 shows a

sequence of 6 rows being read out with R0x3040[15] = 0 and R0x3040[15] = 1. Changing this bit causes the Bayer order of the output image to change; the new Bayer order is reflected in the value of the pixel_order register.
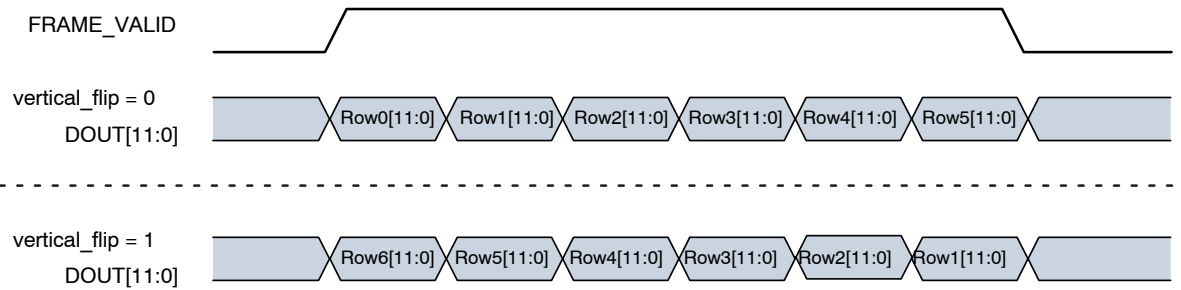
Figure 26. Effect of Vertical Flip on Readout Order

SUBSAMPLING

The AR0330CS supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping or binning pixels within the readout window.

The working modes described in the data sheet that use subsampling are configured to use either 2x2 or 3x3 subsampling.
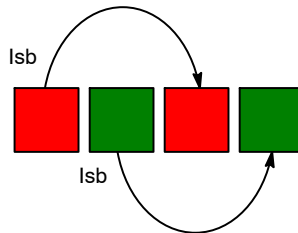
Figure 27. Horizontal Binning in the AR0330CS Sensor

Horizontal binning is achieved either in the pixel readout or the digital readout. The sensor will sample the combined 2x or 3x adjacent pixels within the same color plane.
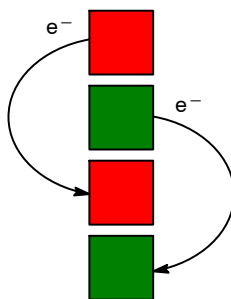
Figure 28. Vertical Row Binning in the AR0330CS Sensor

Vertical row binning is applied in the pixel readout. Row binning can be configured of 2x rows within the same color plane.

Pixel skipping can be configured up to 2x and 3x in both the x−direction and y−direction. Skipping pixels in the x−direction will not reduce the row time. Skipping pixels in the y−direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing.

The sensor increments its x and y address based on the x_odd_inc and y_odd_inc value. The value indicates the addresses that are skipped after each pair of pixels or rows has been read.

The sensor will increment x and y addresses in multiples of 2. This indicates that a GreenR and Red pixel pair will be read together. As well, that the sensor will read a Gr−R row first followed by a B−Gb row.

$$x \text{ subsampling factor } = \frac{1 + x\_odd\_inc}{2} \qquad \text{(eq. 16)}$$

$$y \text{ subsampling factor } = \frac{1 + y\_odd\_inc}{2} \qquad \text{(eq. 17)}$$

A value of 1 is used for x_odd_inc and y_odd_inc when no pixel subsampling is indicated. In this case, the sensor is incrementing x and y addresses by 1 + 1 so that it reads consecutive pixel and row pairs. To implement a 2x skip in the x direction, the x_odd_inc is set to 3 so that the x address increment is 1 + 3, meaning that sensor will skip every other Gr−R pair.

Table 29. CONFIGURATION FOR HORIZONTAL SUBSAMPLING

	x_odd_inc	Restrictions:
No subsampling	x_odd_inc = 1 skip = (1 + 1) × 0.5 = 1x	The horizontal FOV must be programmed to meet the following rule: $$\frac{x\_addr\_end - x\_addr\_start + 1}{(x\_odd\_inc + 1)/2} = \text{even number}$$
Skip 2x	x_odd_inc = 3 skip = (1 + 3) × 0.5 = 2x	
Skip 3x	x_odd_inc = 5 skip = (1 + 5) × 0.5 = 3x	
Analog Bin 2x	x_odd_inc = 3 skip = (1 + 3) × 0.5 = 2x col_sf_bin_en = 1	
Digital Bin 2x	x_odd_inc = 3 skip = (1+3) × 0.5 = 2x col_bin = 1	
Digital Bin 3x	x_odd_inc = 5 skip = (1 + 5) × 0.5 = 3x col_bin = 1	

Table 30. CONFIGURATION FOR VERTICAL SUBSAMPLING

	y_odd_inc	Restrictions:
No subsampling	y_odd_inc = 1 skip = (1 + 1) × 0.5 = 1x row_bin = 0	The horizontal FOV must be programmed to meet the following rule: $$\frac{y\_addr\_end - y\_addr\_start + 1}{(y\_odd\_inc + 1)/2} = \text{even number}$$
Skip 2x	y_odd_inc = 3 skip = (1 + 3) × 0.5 = 2x row_bin = 0	
Skip 3x	y_odd_inc = 5 skip = (1 + 5) × 0.5 = 3x row_bin = 0	
Analog Bin 2x	y_odd_inc = 3 skip = (1 + 3) × 0.5 = 2x row_bin = 1	

SENSOR FRAME RATE

The time required to read out an image frame (T_{FRAME}) can be derived from the number of clocks required to output each image and the pixel clock.

The frame−rate is the inverse of the frame period.

$$fps = 1/T_{FRAME} \qquad \text{(eq. 1)}$$

The number of clocks can be simplified further into the following parameters:

- The number of clocks required for each sensor row (*line_length_pck*)

This parameter also determines the sensor row period when referenced to the sensor readout clock. (T_{ROW} = line_length_pck x 1/CLK_PIX)

- The number of row periods per frame (*frame_length_lines*)
- An extra delay between frames used to achieve a specific output frame period (*extra_delay*)

$$T_{FRAME} = 1/(CLK\_PIX) \times [frame\_length\_lines \times line\_lenght\_pck + extra\_delay) \qquad \text{(eq. 2)}$$
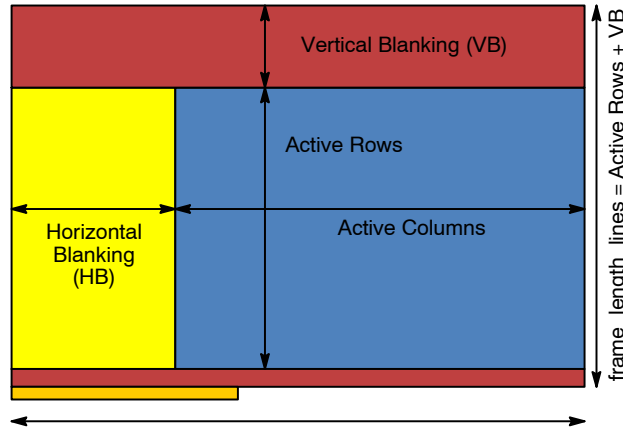
Figure 29. Frame Period Measured in Clocks

Row Period (T_{ROW})

The *line_length_pck* will determine the number of clock periods per row and the row period (T_{ROW}) when combined with the sensor readout clock. The *line_length_pck* includes both the active pixels and the horizontal blanking time per row. The sensor utilizes two readout paths, as seen in Figure 17, allowing the sensor to output two pixels during each pixel clock.

The minimum *line_length_pck* is defined as the maximum of the following three equations:

ADC Readout Limitation:

$$\begin{array}{c} 1204(ADC\_HIGH\_SPEED) = 0 \\ or \\ 1116(ADC\_HIGH\_SPEED) = 1 (0) \end{array} \qquad \text{(eq. 3)}$$

Options to modify this limit, as mentioned in the "Sequencer" section, can be found in the AR0330CS Developer Guide.

Digital Readout Limitation:

$$\frac{1}{3} \times \left[\frac{x\_addr\_end - x\_addr\_start}{(x\_odd\_inc + 1) \times 0.5} \right] \qquad \text{(eq. 4)}$$

Output Interface Limitations:

$$\frac{1}{2} \times \left[\frac{x\_addr\_end - x\_addr\_start}{(x\_odd\_inc + 1) \times 0.5} \right] \qquad \text{(eq. 5)}$$

Row Periods Per Frame

The *frame_length_lines* determines the number of row periods (T_{ROW}) per frame. This includes both the active and blanking rows. The *minimum_vertical_blanking* value is defined by the number of OB rows read per frame, two embedded data rows, and two blank rows.

$$Minimum frame\_length\_lines = \frac{y\_addr\_end - y\_addr\_start}{(y\_odd\_inc + 1)/2} + minimum\_vertical\_blanking \qquad \text{(eq. 6)}$$

The sensor is configured to output frame information in two embedded data rows by setting R0x3064[8] to 1 (default). If R0x3064[8] is set to 0, the sensor will instead output two blank rows. The data configured in the two embedded rows is defined in MIPI CSI−2 Specification V1.00.

Table 31. Minimum Vertical Blanking Configuration

R0x3180[0x00F0]	OB Rows	minimum_vertical_blanking
0x8 (Default)	8 OB Rows	8 OB + 4 = 12
0x4	4 OB Rows	4 OB + 4 = 8
0x2	2 OB Rows	2 OB + 4 = 6

The locations of the OB rows, embedded rows, and blank rows within the frame readout are identified in Figure 30: "Slave Mode Active State and Vertical Blanking" .

SLAVE MODE

The slave mode feature of the AR0330CS supports triggering the start of a frame readout from a VD signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates. The VD signal is input to the trigger pin. Both the GPI_EN (R0x301A[8]) and the SLAVE_MODE (R0x30CE[4]) bits must be set to "1" to enable the slave mode.
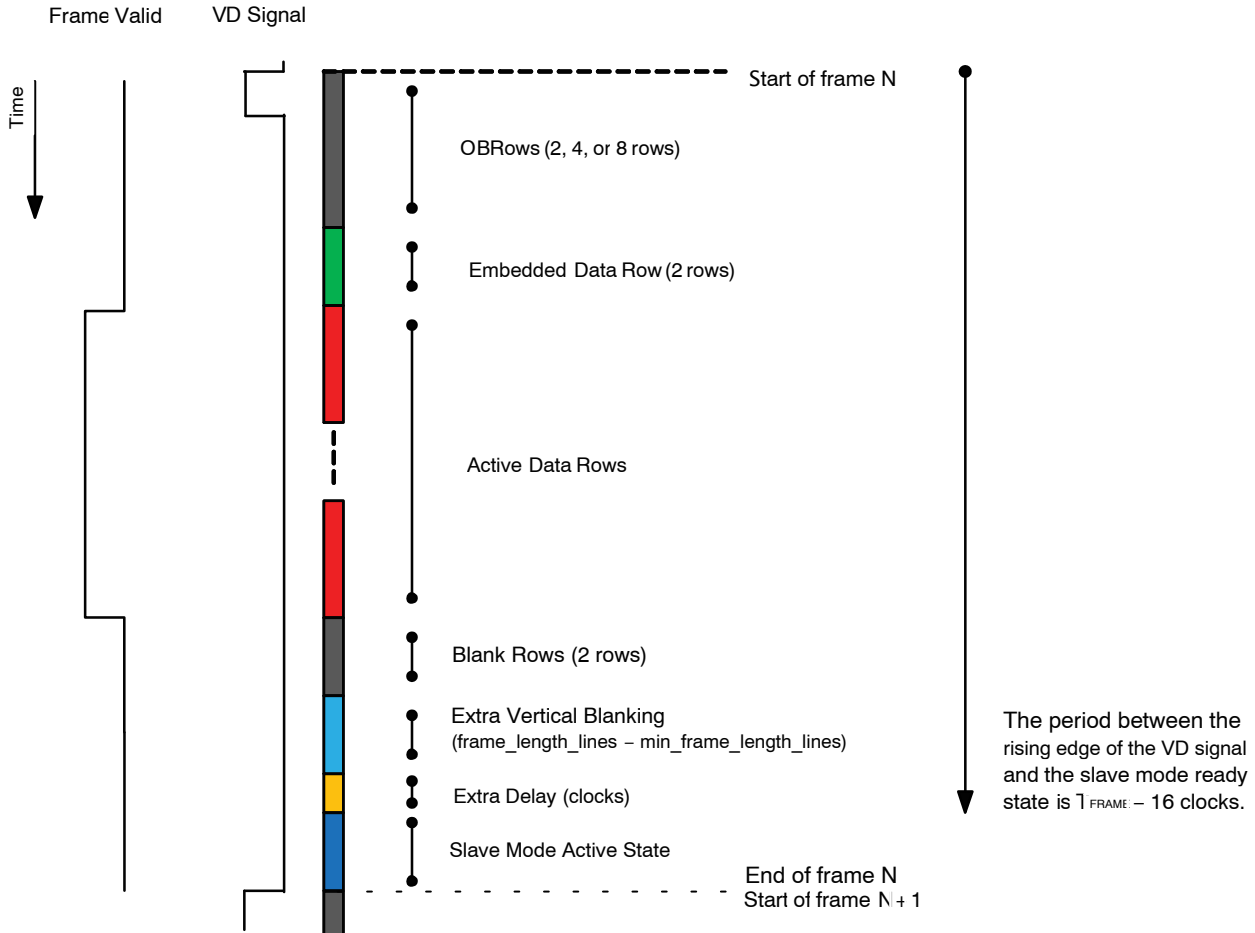
Figure 30. Slave Mode Active State and Vertical Blanking

If the slave mode is disabled, the new frame will begin after the extra delay period is finished.

The slave mode will react to the rising edge of the input VD signal if it is in an active state. When the VD signal is received, the sensor will begin the frame readout and the slave mode will remain inactive for the period of one frame time minus 16 clock periods ($T_{FRAME} - (16 / CLK\_PIX)$). After this period, the slave mode will re−enter the active state and will respond to the VD signal.
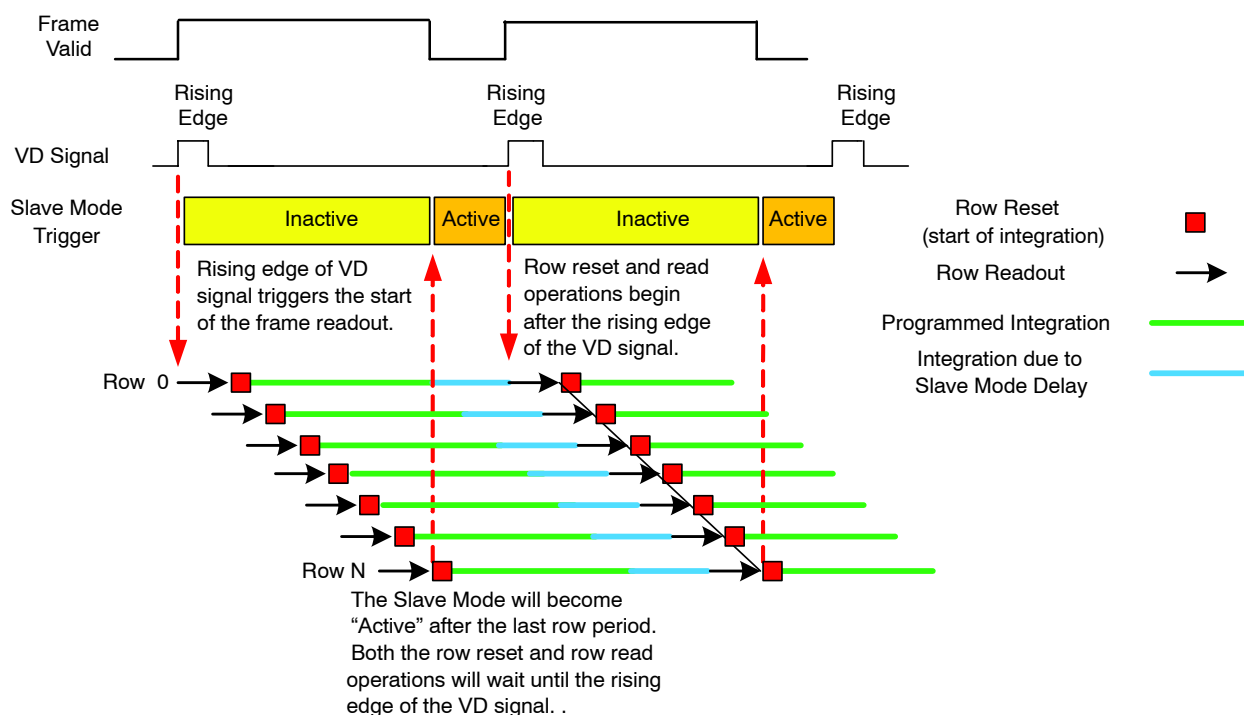
Figure 31. Slave Mode Example with Equal Integration and Frame Readout Periods

The integration of the last row is therefore started before the end of the programmed integration for the first row.

The row shutter and read operations will stop when the slave mode becomes active and is waiting for the VD signal. The following should be considered when configuring the sensor to use the slave mode:

1. The frame period (T_{FRAME}) should be configured to be less than the period of the input VD signal. The sensor will disregard the input VD signal if it appears before the frame readout is finished

2. If the sensor integration time is configured to be less than the frame period, then the sensor will not have reset all of the sensor rows before it begins waiting for the input VD signal. This error can be minimized by configuring the frame period to be as close as possible to the desired frame rate (period between VD signals)
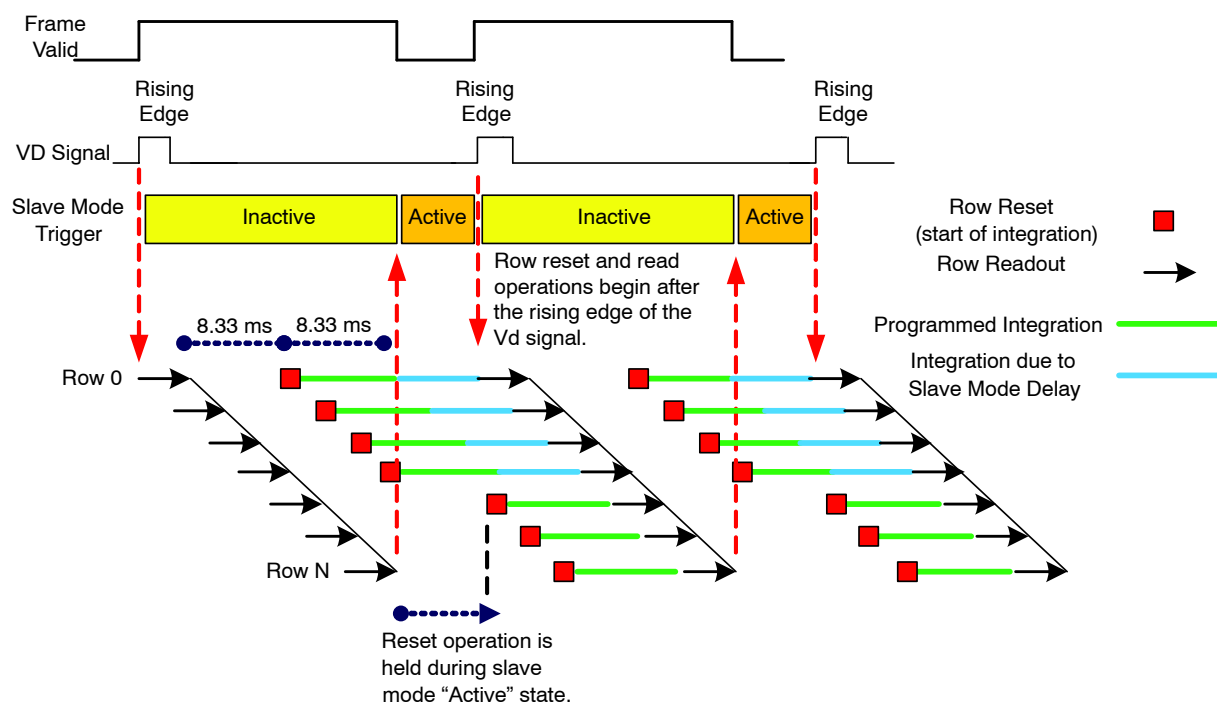
Figure 32. Slave Mode Example Where the Integration Period is Half of the Frame Readout Period

The sensor read pointer will have paused at row 0 while the shutter pointer pauses at row N/2. The extra integration caused by the slave mode delay will only be seen by rows 0 to N/2. The example below is for a frame readout period of 16.6 ms while the integration time is configured to 8.33 ms.

When the slave mode becomes active, the sensor will pause both row read and row reset operations.

NOTE: The row integration period is defined as the period from row reset to row read.

When the AR0330CS is working in slave mode, the external trigger signal VD must have accurately controlled timing to avoid uneven exposure in the output image. The VD timing control should make the slave mode "wait period" less than 32 pixel clocks.

To avoid uneven exposure, programmed integration time cannot be larger than VD period. To increase integration time more than current VD period, the AR0330CS must be configured to work at a lower frame rate and read out image with new VD to match the new timing.

The period between slave mode pulses must also be greater than the frame period. If the rising edge of the VD pulse arrives while the slave mode is inactive, the VD pulse will be ignored and will wait until the next VD pulse has arrived.

FRAME READOUT

The sensor readout begins with vertical blanking rows followed by the active rows. The frame readout period can be defined by the number of row periods within a frame (*frame_length_lines*) and the row period (*line_length_pck*). The sensor will read the first vertical blanking row at the beginning of the frame period and the last active row.

Table 32. SERIAL SYNC CODES INCLUDED WITH EACH PROTOCOL INCLUDED WITH THE AR0330CS SENSOR

Interface/Protocol	Start of Vertical Blanking Row (SOV)	Start of Frame (SOF)	Start of Active Line (SOA)	End of Line (EOL)	End of Frame (EOF)
Parallel	Parallel interface uses FRAME VALID(FV) and LINE VALID (LV) outputs to denote start and end of line and frame.				
MIPI	No SYNC Code	Yes	Yes	Yes	Yes

Figure illustrates how the sensor active readout time can be minimized while reducing the frame rate.

CHANGING SENSOR MODES

Register Changes

All register writes are delayed by 1x frame. A register that is written to during the readout of frame *n* will not be updated to the new value until the readout of frame *n + 2*. This includes writes to the sensor gain and integration registers.

Real–Time Context Switching

In the AR0330CS, the user may switch between two full register sets A and B by writing to a context switch change bit in R0x30B0[13]. When the context switch is configured to context A the sensor will reference the "Context A Registers". If the context switch is changed from A to B during the readout of frame *n*, the sensor will then reference the context B *coarse_integration_time* registers in frame *n + 1* and all other context B registers at the beginning of reading frame *n + 2*. The sensor will show the same behavior when changing from context B to context A.

Table 33. LIST OF CONFIGURABLE REGISTERS FOR CONTEXT A AND CONTEXT B

Context A		Context B	
Register Description	Address	Register Description	Address
Coarse_integration_time	0x3012	Coarse_integration_time_CB	0x3016
Fine_integration_time	0x3014	Fine_integration_time_CB	0x3018
Line_length_pck	0x300C	Line_length_pck_CB	0x303E
Frame_length_lines	0x300A	Frame_length_lines_CB	0x30AA
COL_SF_BIN_EN	0x3040[9]	COL_SF_BIN_EN_CB	0x3040[8]
ROW_BIN	0x3040[12]	ROW_BIN_CB	0x3040[10]
COL_BIN	0x3040[13]	COL_BIN_CB	0x3040[11]
FINE_GAIN	0x3060[3:0]	FINE_GAIN_CB	0x3060[11:8]
COARSE_GAIN	0x3060[5:4]	COARSE_GAIN_CB	0x3060[13:12]
x_addr_start	0x3004	x_addr_start_CB	0x308A
y_addr_start	0x3002	y_addr_start_CB	0x308C
x_addr_end	0x3008	x_addr_end_CB	0x308E
y_addr_end	0x3006	y_addr_end_CB	0x3090
Y_odd_inc	0x30A6	Y_odd_inc_CB	0x30A8
X_odd_inc	0x30A2	X_odd_inc_CB	0x30AE
ADC_HIGH_SPEED	0x30BA[6]	ADC_HIGH_SPEED_CB	0x30BA[7]
GREEN1_GAIN	0x3056	GREEN1_GAIN_CB	0x30BC
BLUE_GAIN	0x3058	BLUE_GAIN_CB	0x30BE
RED_GAIN	0x305A	RED_GAIN_CB	0x30C0
GREEN2_GAIN	0x305C	GREEN2_GAIN_CB	0x30C2
GLOBAL_GAIN	0x305E	GLOBAL_GAIN_CB	0x30C4

39. ON Semiconductor recommends leaving fine_integration_time at 0.
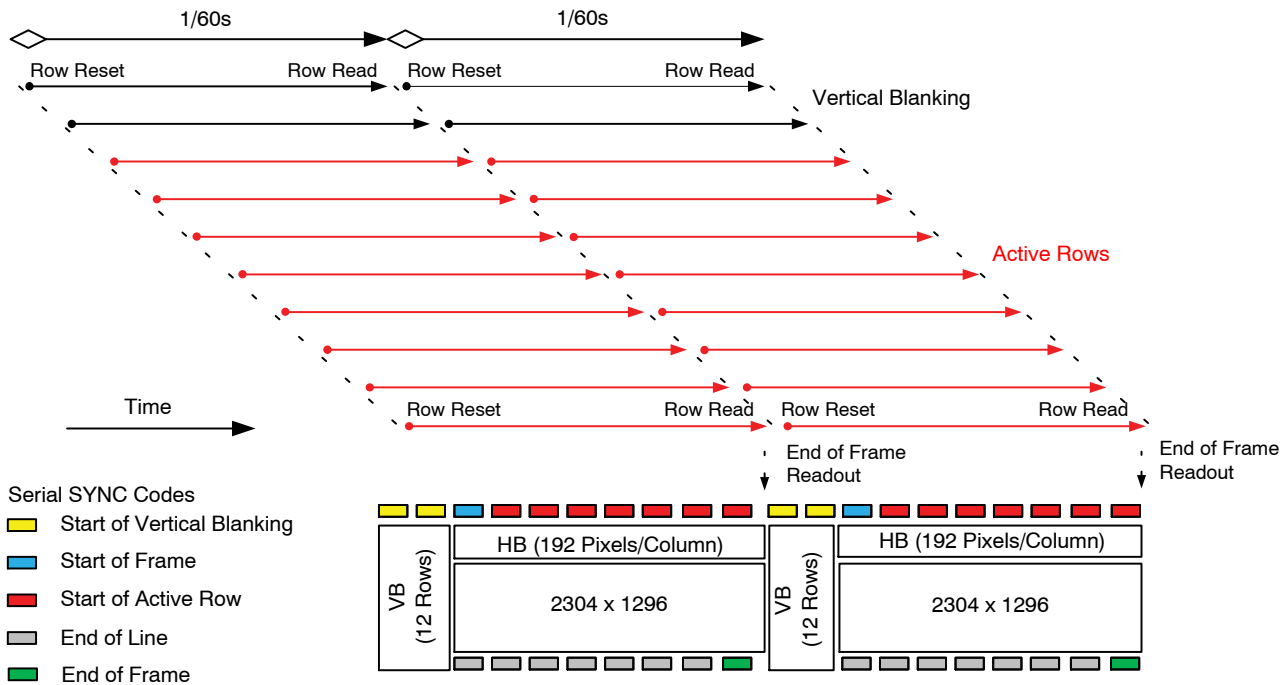
Figure 33. Example of Changing the Sensor from Context A to Context B

COMPRESSION

The sensor can optionally compress 12−bit data to 10−bit using A−law compression. The compression is applied after the data pedestal has been added to the data. See Figure 1: "Block Diagram".

The A−law compression is disabled by default and can be enabled by setting R0x31D0 from "0" to "1".

Table 34. A−LAW COMPRESSION TABLE FOR 12−10 BITS

Input Range	Input Values												Compressed Codeword									
	11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0 to 127	0	0	0	0	0	a	b	c	d	e	f	g	0	0	0	a	b	c	d	e	f	g
128 to 255	0	0	0	0	1	a	b	c	d	e	f	g	0	0	1	a	b	c	d	e	f	g
256 to 511	0	0	0	1	a	b	c	d	e	f	g	X	0	1	0	a	b	c	d	e	f	g
512 to 1023	0	0	1	a	b	c	d	e	f	g	X	X	0	1	1	a	b	c	d	e	f	g
1024 to 2047	0	1	a	b	c	d	e	f	g	h	X	X	1	0	a	b	c	d	e	f	g	h
2048 to 4095	1	a	b	c	d	e	f	g	h	X	X	X	1	1	a	b	c	d	e	f	g	h

TEST PATTERNS

The AR0330CS has the capability of injecting a number of test patterns into the top of the datapath to debug the digital logic. With one of the test patterns activated, any of the datapath functions can be enabled to exercise it in a deterministic fashion. Test patterns are selected by Test_Pattern_Mode register (R0x3070). Only one of the test patterns can be enabled at a given point in time by setting the Test_Pattern_Mode register according to Table 35. When test patterns are enabled the active area will receive the value specified by the selected test pattern and the dark pixels will receive the value in Test_Pattern_Green (R0x3074 and R0x3078) for green pixels, Test_Pattern_Blue (R0x3076) for blue pixels, and Test_Pattern_Red (R0x3072) for red pixels.

Table 35. Test Pattern Modes

Test_Pattern_Mode	Test Pattern Output
0	No test pattern (normal operation)
1	Solid Color
2	100% Vertical Color Bars
3	Fade−to−Gray Vertical Color Bars
256	Walking 1s test pattern (12−bit)

Solid Color

When the color field mode is selected, the value for each pixel is determined by its color. Green pixels will receive the value in Test_Pattern_Green, red pixels will receive the value in Test_Pattern_Red, and blue pixels will receive the value in Test_Pattern_Blue.

Vertical Color Bars

When the vertical color bars mode is selected, a typical color bar pattern will be sent through the digital pipeline.

Walking 1 s

When the walking 1s mode is selected, a walking 1 s pattern will be sent through the digital pipeline. The first value in each row is 1.

TWO−WIRE SERIAL REGISTER INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the AR0330CS. This interface is designed to be compatible with the electrical characteristics and transfer protocols of the I²C specification.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW−the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive S<small>CLK</small> LOW; the AR0330CS uses S<small>CLK</small> as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no−) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both S<small>CLK</small> and S<small>DATA</small> are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on S<small>DATA</small> while S<small>CLK</small> is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a "repeated start" or "restart" condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on S<small>DATA</small> while S<small>CLK</small> is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for both the slave address/data direction byte and for message bytes.

One data bit is transferred during each S<small>CLK</small> clock period. S<small>DATA</small> can change when S<small>CLK</small> is LOW and must be stable while S<small>CLK</small> is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a WRITE, and a "1" indicates a READ. The default slave addresses used by the AR0330CS sensor are 0x20 (write address) and 0x21 (read address). Alternate slave addresses of 0x30 (WRITE address) and 0x31 (READ address) can be selected by asserting the S<small>ADDR</small> signal (tie HIGH).

Alternate slave addresses can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the S<small>CLK</small> clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases S<small>DATA</small>. The receiver indicates an acknowledge bit by driving S<small>DATA</small> LOW. As for data transfers, S<small>DATA</small> can change when S<small>CLK</small> is LOW and must be stable while S<small>CLK</small> is HIGH.

No−Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive S<small>DATA</small> LOW during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ From Random Location

This sequence (Figure 34) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. Figure 34 shows how the internal register address maintained by the AR0330CS is loaded and incremented as the sequence proceeds.

S = Start Condition
P = Stop Condition
Sr = Restart Condition
A = Acknowledge
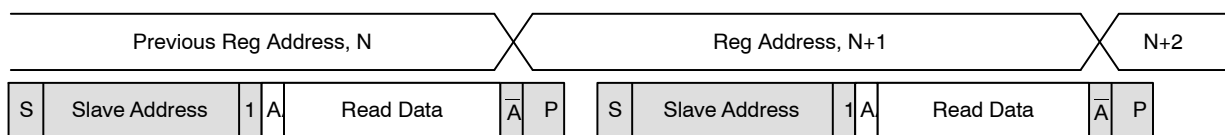$\overline{A}$ = No−acknowledge

☐ Slave to Master
▨ Master to Slave
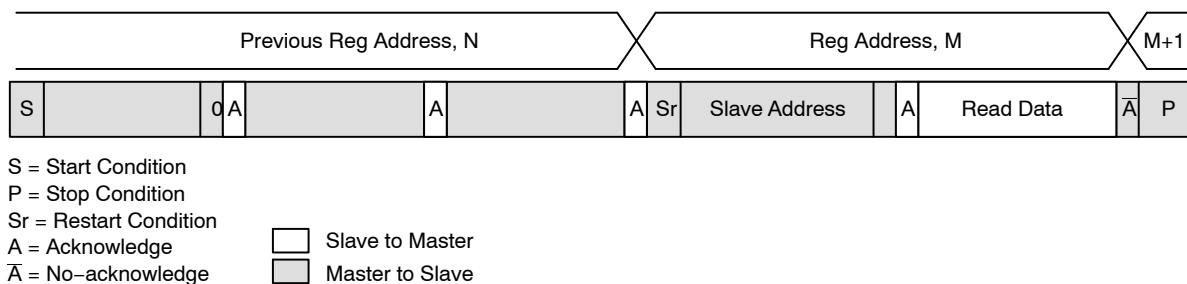
Figure 34. Single READ From Random Location

Single READ From Current Location

This sequence (Figure 35) performs a read using the current value of the AR0330CS internal register address.

The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

Figure 35. Single READ From Current Location

Sequential READ, Start From Random Location

This sequence (Figure 36) starts in the same way as the single READ from random location (Figure 34). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.
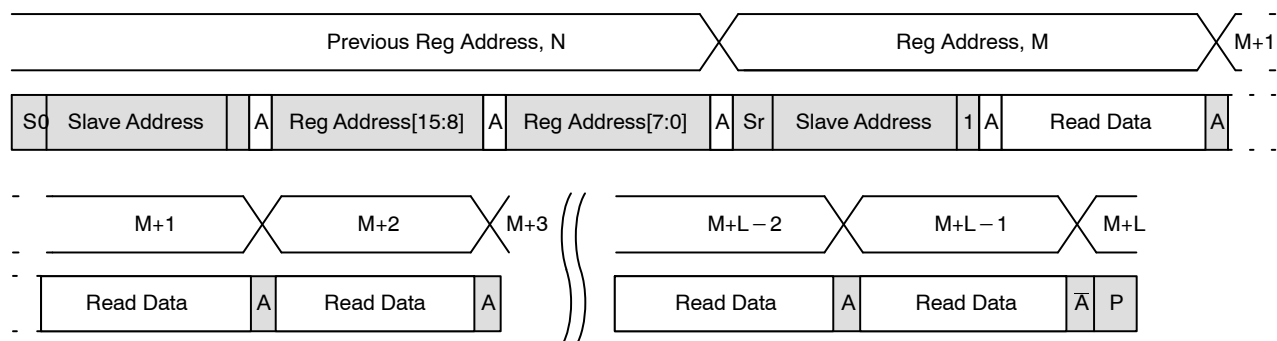
Figure 36. Sequential READ, Start From Random Location

Sequential READ, Start From Current Location

This sequence (Figure 37) starts in the same way as the single READ from current location (Figure 35). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.
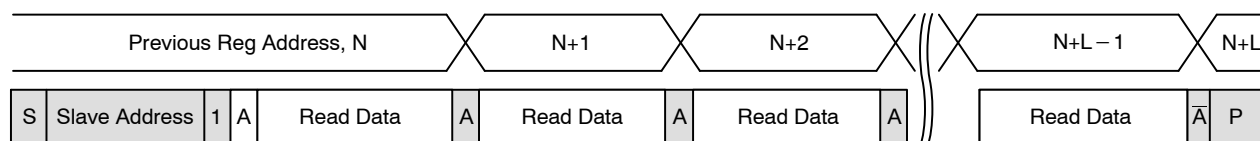
Figure 37. Sequential READ, Start From Current Location

Single WRITE to Random Location

This sequence (Figure 38) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

Figure 38. Single WRITE to Random Location

SPECTRAL CHARACTERISTICS
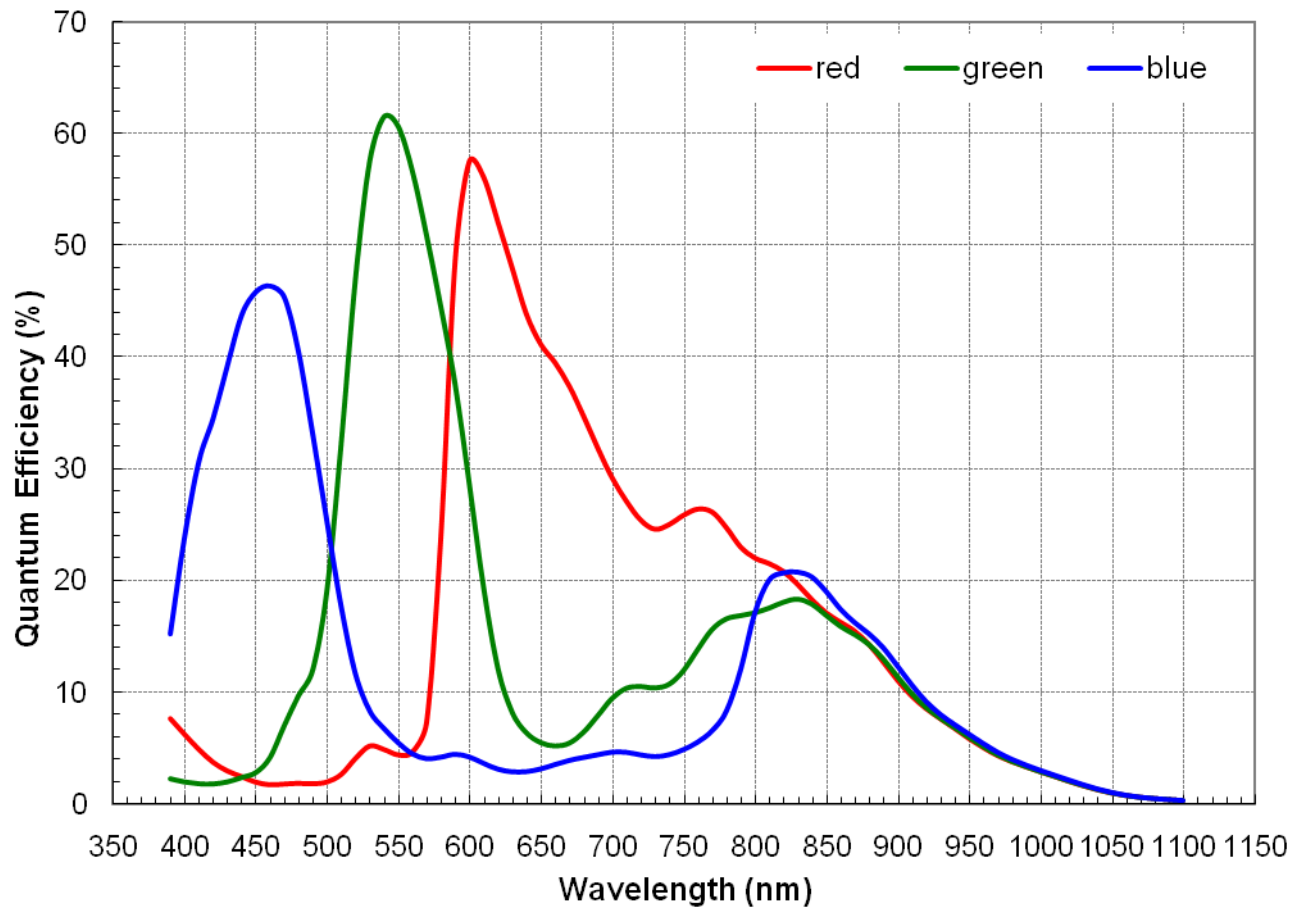
Figure 39. Bare Die Quantum Efficiency

Table 36. CHIEF RAY ANGLE (CRA) 12 °

Image Height		CRA
%	mm	deg.
0	0	0
5	0.152	.80
10	0.305	1.66
15	0.457	2.54
20	0.609	3.42
25	0.761	4.28
30	0.914	5.11
35	1.066	5.94
40	1.218	6.75
45	1.371	7.57
50	1.523	8.37
55	1.675	9.16
60	1.828	9.90
65	1.980	10.58
70	2.132	11.15
75	2.284	11.57
80	2.437	11.80
85	2.589	11.78
90	2.741	11.48
95	2.894	10.88
100	3.046	9.96
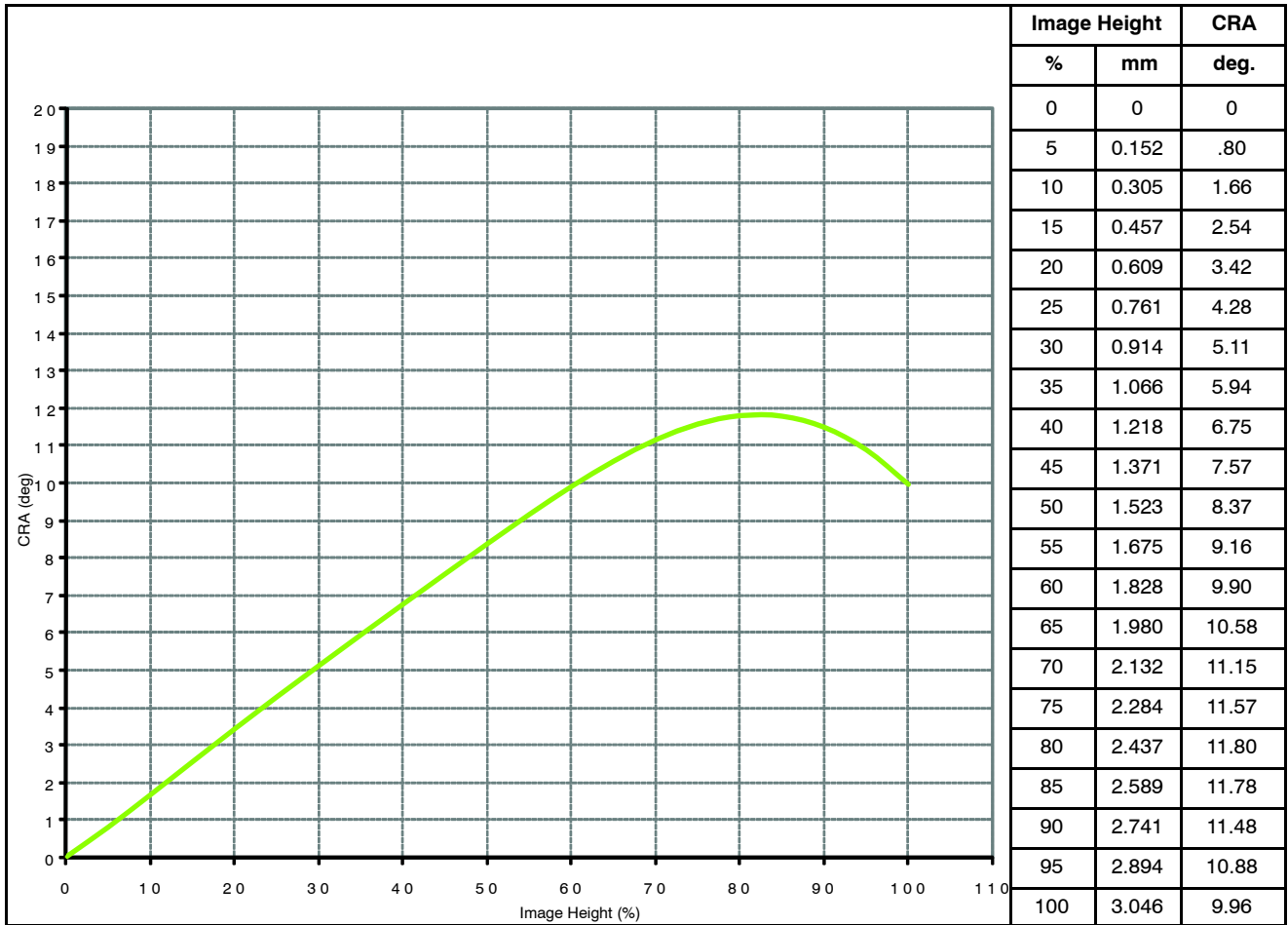
40. The CRA listed in the advanced data sheet described the 2048x1536 field of view (2.908 mm image height). This information was sufficient for configuring the sensor to read both the 4:3 (2048x1536) and 16:9 (2304x1296) aspect ratios. The CRA information listed in the data sheet has now been updated to represent the entire pixel array (2304x1536).

PACKAGE ORIENTATION IN CAMERA DESIGN

In a camera design, the package should be placed in a PCB so that the first clear pixel is located at the bottom left of the package (look at the package). This orientation will ensure that the image captured using a lens will be oriented correctly.

The package is oriented so that the first clear pixel is located in bottom left.
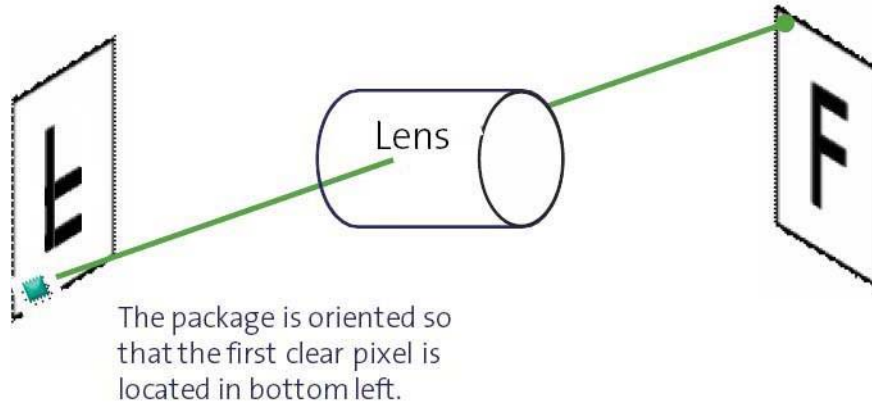
Figure 40. Image Orientation With Relation To Camera Lens

ODCSP61 6.3x6.6
CASE 570BF
ISSUE A

DATE 18 OCT 2019

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS [mm].
3. SOLDER BALL DIAMETER IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. GLASS: 0.400 [mm] THICKNESS; REFRACTIVE INDEX = 1.52.
7. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.041 THICKNESS.
8. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
9. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ±0.1°.
10. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
11. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (-0.290, 0.230).
12. PACKAGE CENTER (X, Y) = (0.000, 0.000).

TOP VIEW

SECTION A-A

DETAIL B

BOTTOM VIEW

RECOMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE
STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD
THE ON SEMICONDUCTOR SOLDERING AND MOUNTING
TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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PLCC48 11.43x11.43
CASE 776AM
ISSUE O

DATE 30 DEC 2014

SECTION A−A

PIN 1 ID

FIRST CLEAR PIXEL

PACKAGE CENTER = OPTICAL CENTER (0,0)

OPTICAL AREA
(2304H X 1536V)
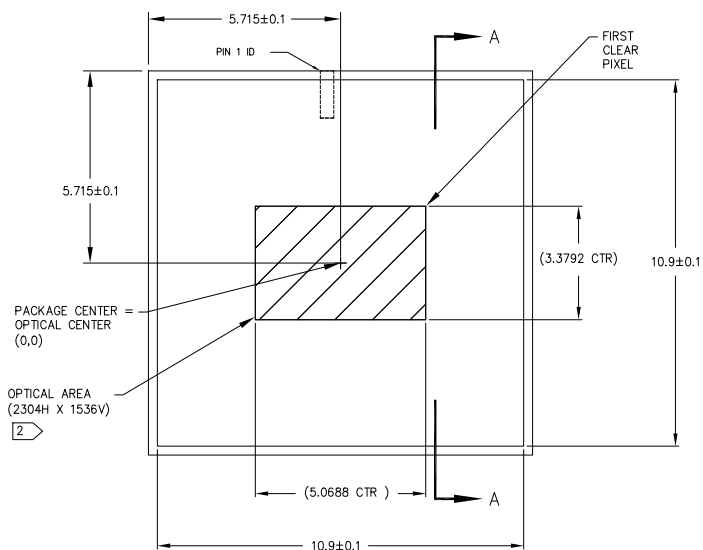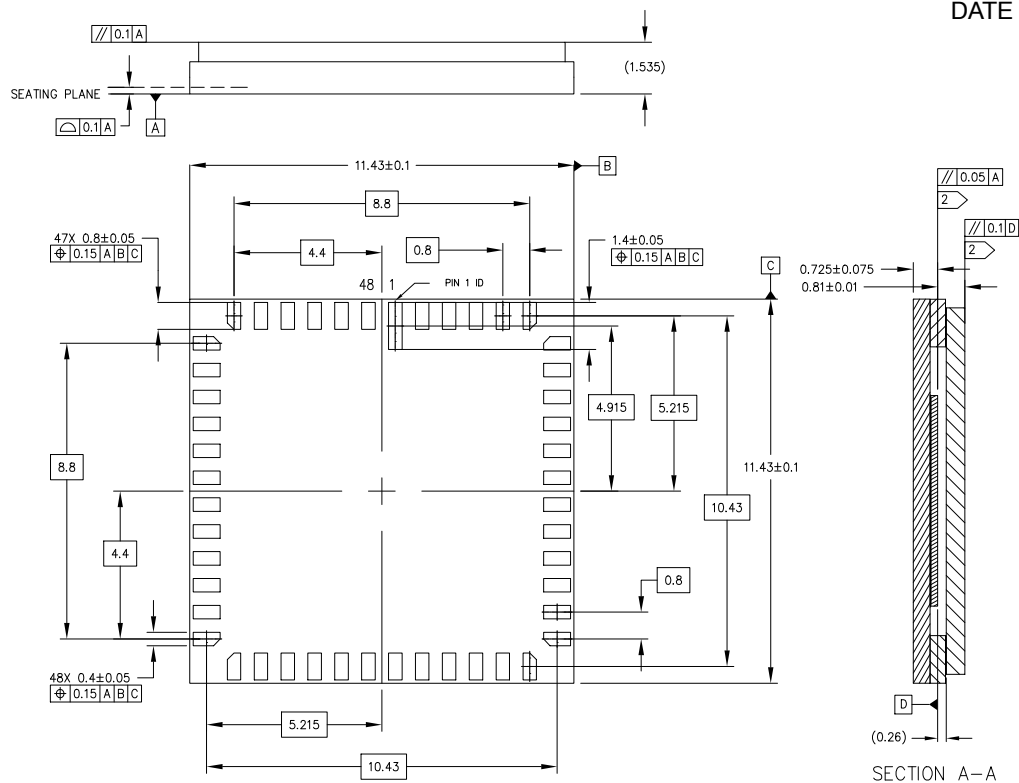
NOTES
1. DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
2. MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE A : 50 MICRONS. MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE D : 100 MICRONS.

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DESCRIPTION:	PLCC48 11.43X11.43		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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