8-bit Microcontroller

KM101EF93G
Datasheet

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www.nuvoton.co.jp

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1. Overview

1.1 Overview

The KM101E series of 8-bit single-chip microcontrollers incorporate multiple types of peripheral functions. This chip series is well suited for camera, TV, CD, printer, telephone, home appliance, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcontroller applications flexible, optimized hardware configurations and a simple efficient instruction set. KM101EF93G have an internal 128 KB of ROM and 6 KB of RAM. Peripheral functions include 5 external interrupts, including NMI, 9 timer counters, 4 types of serial interfaces, A/D converter, watchdog timer and buzzer output. The system configuration is suitable for system control microcontroller.

With 3 oscillation systems (internal frequency: 16 MHz, high-speed crystal/ceramic frequency: max. 10 MHz, low-speed crystal/ceramic frequency: 32.768 kHz) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode) or PLL input (PLL mode), or low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has NORMAL mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in NORMAL mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50ns (maximum).

1.2 Product Summary

This datasheet describes the following model.

Table: 1.1 Product Summary

Model	ROM Size	RAM Size	Classification	Package
KM101EF93G	128 KB	6 KB	Flash EEPROM version	LQFP 80-pin

2. Hardware Functions

- Memory Capacity
  ROM 128 KB
  RAM 6 KB
- Package
  LQFP 80-pin (14 mm × 14 mm / 0.65 mm pitch)
- Machine Cycle
  High-speed mode 0.05 μs / 20 MHz (4.0 V to 5.5 V)
  Low-speed mode 62.5 μs / 32 kHz (4.0 V to 5.5 V)
- Oscillation circuit
  3 channel oscillation circuit
  Internal oscillation (frc): 16 MHz
  Crystal/ceramic (fosc): Maximum 10 MHz
  Crystal/ceramic (fx): Maximum 32.768 kHz
- Clock Multiplication circuit (PLL Circuit)
  PLL circuit output clock (fpll):
  fosc multiplied by 2, 3, 4, 5, 6, 8, 10,
  1/2 × frc multiplication by 4, 5 enable
- Clock Gear for System Clock
  System Clock (fs): fpll divided by 1, 2, 4, 16, 32, 64, 128
- Clock Gear for control clock of peripheral function
  Control clock of peripheral function (fpll-div): stop or fpll divided by 1, 2, 4, 8, 16
- Memory Bank
  Expands data memory space by the bank system (by 64 KB, 16 banks)
  Source address bank / Destination address bank
- Operation Mode
  NORMAL mode (High-speed mode)
  SLOW mode (Low-speed mode)
  HALT mode
  STOP mode
  (The operation clock can be switched in each mode.)
- Operating Voltage
  4.0 V to 5.5 V
- Operation ambient temperature
  -40 °C to +85 °C

- Interrupt

25 levels

<Non-maskable interrupt>
- Non-maskable interrupt and Watchdog timer overflow interrupt

<Timer interrupts>
- Timer 0 interrupt
- Timer 1 interrupt
- Timer 2 interrupt
- Timer 3 interrupt
- Timer 6 interrupt
- Time base timer interrupt
- Timer 7 interrupt
- Timer 7 compare register 2 match interrupt
- Timer 8 interrupt
- Timer 8 compare register 2 match interrupt

<Serial Interface interrupts>
- Serial interface 0 interrupt
- Serial interface 0 UART reception interrupt
- Serial interface 1 interrupt
- Serial interface 1 UART reception interrupt
- Serial interface 2 interrupt
- Serial interface 2 UART reception interrupt
- Serial interface 4 interrupt
- Serial interface 4 stop condition interrupt

<A/D interrupt>
-A/D conversion interrupt

<External interrupts>
- IRQ0: Edge selectable, noise filter connection available
- IRQ1: Edge selectable, noise filter connection available
- IRQ2: Edge selectable, noise filter connection available, both edges interrupt
- IRQ3: Edge selectable, noise filter connection available, both edges interrupt
- IRQ4: Edge selectable, noise filter connection available, both edges interrupt, Key scan interrupt

- Timer Counter

9 timers

8-bit timer for general use × 4 sets
16-bit timer for general use × 2 sets
8-bit free-run timer × 1 set
Time base timer × 1 set
Baud rate timer × 1 set

Timer 0 (8-bit timer for general use)
- Square wave output (Timer pulse output)
- Added pulse (2-bit) type PWM output can be output to large current pin TM0IOA
- Event count
- Simple pulse measurement
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fx, External clock, Timer A output

Timer 1 (8-bit timer for general use)
- Square wave output (Timer pulse output) can be output to large current pin TM1IOA
- Event count
- 16-bit cascade connected (with Timer 0)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fx, External clock, Timer A output

- Timer Counter (contonued)

Timer 2 (8-bit timer for general use)
- Square wave output (Timer pulse output)
- Added pulse (2-bit) type PWM output can be output to large current pin TM2IOA
- Event count
- Simple pulse measurement
- 24-bit cascade connected (with Timer 0 and Timer 1)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128,
  fs/2, fs/4, fs/8, fx, External clock, Timer A output

Timer 3 (8-bit timer for general use)
- Square wave output (Timer pulse output) can be output to large current pin TM3IOA
- Event count
- 16-bit cascade connected (with Timer 2)
- 32-bit cascade connected (with Timer 0 and Timer 1 and Timer 2)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/128,
  fs/2, fs/4, fs/8, fx, External clock, Timer A output

Timer 6 (8-bit free-run timer, Time base timer)
8-bit free-run timer
- Clock source
  fpll-div, fpll-div/212, fpll-div/213, fs, fx, fx/22, fx/23, fx/212, fx/213

Time base timer
- Interrupt generation cycle
  fpll-div/2^7, fpll-div/2^8, fpll-div/2^9, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15},
  fx/2^7, fx/2^8, fx/2^9, fx/2^{10}, fx/2^{13}, fx/2^{15}

Timer 7 (16-bit timer for general use)
- Square wave output (Timer pulse output)
- High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOA
- Event count
- Input capture function (Both edges can be operated)
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,
  Timer A divided by 1, 2, 4, 16,
  External clock divided by 1, 2, 4, 16

Timer 8 (16-bit timer for general use)
- Square wave output (Timer pulse output)
- High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM8IOA
- Event count
- Input capture function (Both edges can be operated)
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,
  Timer A divided by 1, 2, 4, 16,
  External clock divided by 1, 2, 4,
  16 Timer A (Baud rate timer)
- Clock output for peripheral functions
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/16, fpll-div/32, fs/2, fs/4

Timer A (Baud rate timer)
- Clock output for peripheral functions
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/16, fpll-div/32, fs/2, fs/4

- Watchdog timer

  Time-out cycle can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
  On detection of 2 errors, forcibly hard reset inside LSI.
  Operation start timing is selectable. (At reset release or write to register)

- Buzzer Output/ Reverse Buzzer Output

  Output frequency can be selected from $fpll\text{-}div/2^{9}$, $fpll\text{-}div/2^{10}$, $fpll\text{-}div/2^{11}$, $fpll\text{-}div/2^{12}$, $fpll\text{-}div/2^{13}$, $fpll\text{-}div/2^{14}$, $fx/2^{3}$, $fx/2^{4}$

- A/D Converter

  10-bit × 12 channels

- Serial Interface

  4 channels

  Serial 0: UART (full duplex)/ Clock synchronous
  Clock synchronous serial interface
  - Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 2 to 8 bits are selectable.
  - Sequence transmission, reception or both are available

  Full duplex UART
  - Baud rate timer, selected from Timer 0 to 3 or Timer A
  - Parity check, overrun error/ framing error detection
  - Transfer size 7 to 8 bits can be selected

  Serial 1: UART (full duplex)/ Clock synchronous
  Clock synchronous serial interface
  - Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 2 to 8 bits are selectable.
  - Sequence transmission, reception or both are available.

  Full duplex UART
  - Baud rate timer, selected from Timer 0 to 3 or Timer A
  - Parity check, overrun error/ framing error detection
  - Transfer size 7 to 8 bits can be selected

  Serial 2: UART (full duplex)/ Clock synchronous
  Clock synchronous serial interface
  - Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 2 to 8 bits are selectable.
  - Sequence transmission, reception or both are available.

  Full duplex UART
  - Baud rate timer, selected from Timer 0 to 3 or Timer A
  - Parity check, overrun error/ framing error detection
  - Transfer size 7 to 8 bits can be selected

- Serial Interface (continued)

Serial 4: Multi master IIC/ Clock synchronous

Clock synchronous serial interface
- Transfer clock source
  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/32, fs/2, fs/4,
  Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 2 to 8 bits are selectable.
- Sequence transmission, reception or both are available.

Multi master IIC
- 7-bit slave address is settable.
- General call communication mode is supported.

- Automatic Reset

Power detection level: 4.3 V (at rising), 4.2 V (at falling)

- LED Driver

8 pins (Port A)

- Ports

I/O ports	72 pins
Serial Interface pins	21 pins
Timer I/O	11 pins
Buzzer output pins	2 pins
A/D input pins	12 pins
External Interrupt pins	5 pins
LED (large current) driver	8 pins
High-speed oscillation	2 pins
Low-speed oscillation	2 pins
Special pins	8 pins
Operation mode input pins	3 pins
Reset input pin	1 pin
Analog reference voltage input pin	1 pin
Power pins	3 pins

3 Pin Description

3.1 Pin configuration

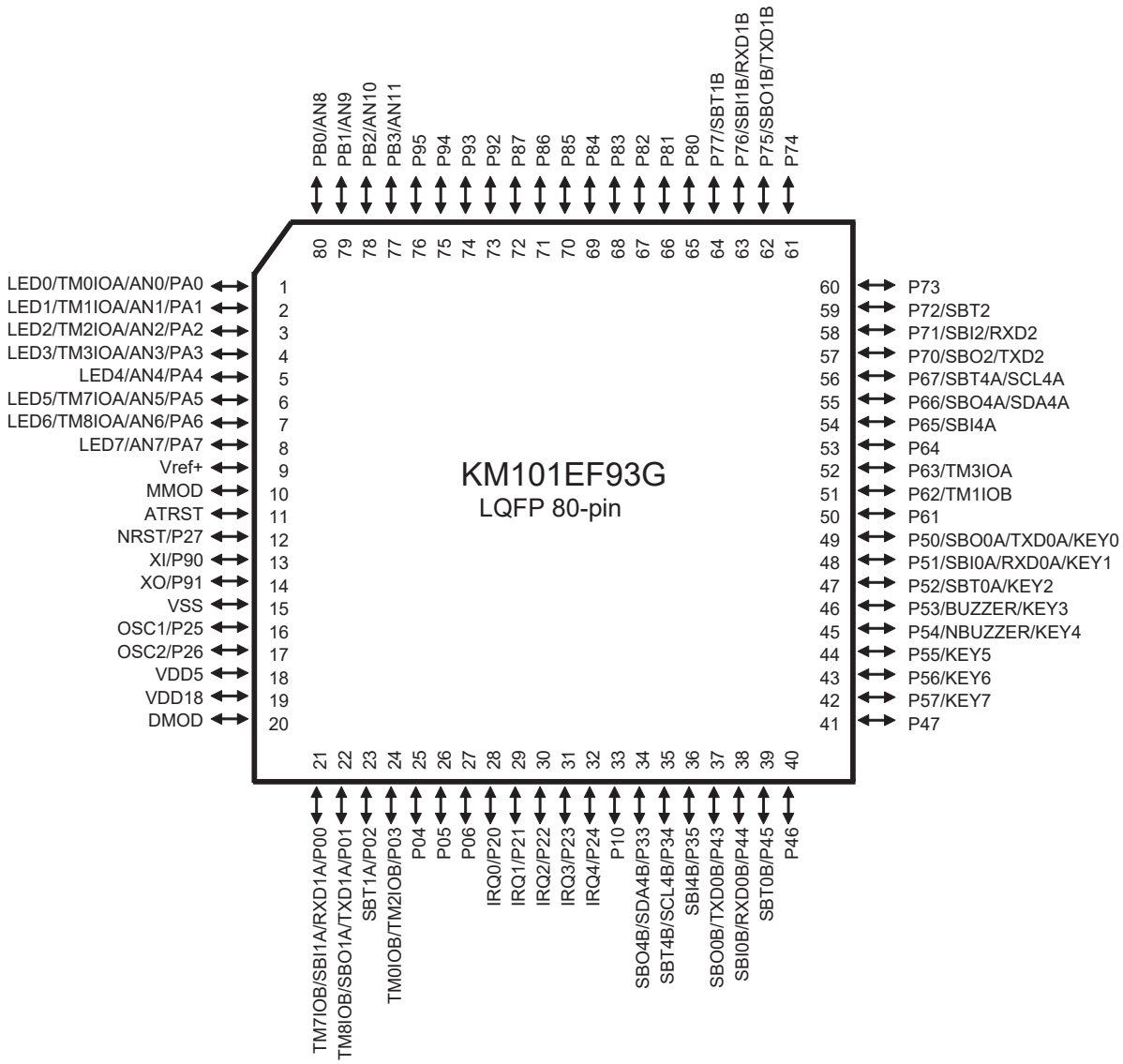

Figure: 3.1 Pin Configuration (LQFP 80-pin)

3.2. Pin Functions

Table: 3.1 Pin Functions

Pins	Pin NO	I/O	Function	Description
VDD5 VSS	18 15	- -	Power connect pins	Apply 4.0 V to 5.5 V to VDD5 and 0 V connect 0.1 μF + 1 μF or larger bypass capacitor for internal power stabilization.
VDD18	19	-	Internal power output pin	This pin is output 1.8 V from internal power circuit. Don't use the power supply to external device. For internal power circuit output stability, connect at least 0.1 μF + 1 μF one bypass capacitor between VDD18 and VSS.
OSC1	16	Input	High speed operation clock input pin	Connect these oscillation pins to ceramic or crystal oscillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using STOP mode.
OSC2	17	Output	High speed operation clock output pin	
NRST	12	I/O	Reset pin [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Typ. 50 kΩ). Setting this pin low initialize the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. If a capacitor is to be inserted between NRST and VSS, it is recommended that a discharge diode be placed between NRST and VDD5.
ATRST	11	input	Auto reset setting pin	Input "High" to enable auto reset function and "Low" to disable this function
P00 P01 P02 P03 P04 P05 P06	21 22 23 24 25 26 27	I/O	I/O port 0	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P0DIR register. A pull-up resistor for each bit can be selected individually by P0PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P10	33	I/O	I/O port 1	1-bit CMOS tri-state I/O port. It can be set as either an input or output by P1DIR register. A pull-up resistor can be selected by P1PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P20 P21 P22 P23 P24 P25 P26	28 29 30 31 32 16 17	I/O	I/O port 2	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P2DIR register. A pull-up resistor for each bit can be selected individually by P2PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance)
P27	12	input	input port 2	P27 has an N-channel open-drain configuration.
P33 P34 P35	34 35 36	I/O	I/O port 3	3-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P3DIR register. A pull-up resistor for each bit can be selected individually by P3PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P43 P44 P45 P46 P47	37 38 39 40 41	I/O	I/O port 4	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P4DIR register. A pull-up resistor for each bit can be selected individually by P4PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).

Pins	Pin NO	I/O	Function	Description
P50 P51 P52 P53 P54 P55 P56 P57	49 48 47 46 45 44 43 42	I/O	I/O port 5	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P5DIR register. A pull-up resistor for each bit can be selected individually by P5PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P61 P62 P63 P64 P65 P66 P67	50 51 52 53 54 55 56	I/O	I/O port 6	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P6DIR register. A pull-up resistor for each bit can be selected individually by P6PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P70 P71 P72 P73 P74 P75 P76 P77	57 58 59 60 61 62 63 64	I/O	I/O port 7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P7DIR register. A pull-up resistor for each bit can be selected individually by P7PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P80 P81 P82 P83 P84 P85 P86 P87	65 66 67 68 69 70 71 72	I/O	I/O port 8	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P8DIR register. A pull-up resistor for each bit can be selected individually by P8PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P90 P91 P92 P93 P94 P95	13 14 73 74 75 76	I/O	I/O port 9	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P9DIR register. A pull-up resistor for each bit can be selected individually by P9PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	1 2 3 4 5 6 7 8	I/O	I/O port A	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by PADIR register. A pull-up resistor for each bit can be selected individually by PAPLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).

Pins	Pin NO	I/O	Function	Description
PB0 PB1 PB2 PB3	80 79 78 77	I/O	I/O port B	4-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by PBDIR register. A pull-up resistor for each bit can be selected individually by PBPLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
SBO0A SBO0B SBO1A SBO1B SBO2 SBO4A SBO4B	49 37 22 62 57 55 34	Output	Serial interface transmission data output pins	Transmission data output pins for serial interface 0,1,2,4. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P3ODC, P4ODC, P5ODC, P6ODC and P7ODC registers. Pull-up resistor can be selected in P0PLU, P3PLU, P4PLU, P5PLU, P6PLU, and P7PLU registers. Select output mode in P0DIR, P3DIR, P4DIR, P5DIR, P6DIR, and P7DIR registers and set serial data output mode in serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC4MD1). These can be used as normal I/O pins when serial interface is not used.
SBI0A SBI0B SBI1A SBI1B SBI2 SBI4A SBI4B	48 38 21 63 58 54 36	Input	Serial interface reception data input pins	Reception data input pins for serial interface 0,1,2,4. Pull-up resistor can be selected in P0PLU, P3PLU, P4PLU, P5PLU, P6PLU and P7PLU registers. Select the output mode in P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and select serial data input mode in serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC4MD1). These can be used as normal I/O pins when serial interface is not used.
SBT0A SBT0B SBT1A SBT1B SBT2 SBT4A SBT4B	47 39 23 64 59 56 35	I/O	Serial interface Clock I/O pins	Clock I/O pins for serial interface 0,1,2,4. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P3ODC, P4ODC, P5ODC, P6ODC and P7ODC registers. Pull-up resistor can be selected in P0PLU, P3PLU, P4PLU, P5PLU, P6PLU and P7PLU registers. Select clock I/O in P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC4MD1) with the communication mode. These can be used as normal I/O pins when serial interface is not used.
TXD0A TXD0B TXD1A TXD1B TXD2	49 37 22 62 57	Output	UART transmission data output pins	In serial interface 0,1,2 in UART mode, this pin is configured as the transmission data output pin. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P4ODC, P5ODC, P6ODC and P7ODC registers. Pull-up resistor can be selected by P0PLU, P4PLU, P5PLU(D), P6PLU and P7PLU registers. Select the output mode in P0DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and select serial data output mode in serial mode register 1 (SC0MD1, SC1MD1, SC2MD1). These can be used as normal I/O pins when serial interface is not used.
RXD0A RXD0B RXD1A RXD1B RXD2	48 38 21 63 58	Input	UART reception data output pins	In serial interface 0,1,2 in UART mode, this pin is configured as the reception data input pin. Pull-up resistor can be selected in P0PLU, P4PLU, P5PLU(D), P6PLU and P7PLU registers. Select the input mode in P0DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and select serial input in serial mode register 1 (SC0MD1, SC1MD1, SC2MD1). These can be used as normal I/O pins when serial interface is not used.
SDA4A SDA4B	55 34	I/O	IIC data I/O pins	In serial interface 4 in IIC mode, this pin is configured as the data I/ O pin. For the output configuration, select Nch open-drain in P3ODC and P6ODC register and set pull-up resistor in P3PLU and P6PLU register. Select the output mode in P0DIR register and P6DIR register select serial data I/O mode by serial mode register 1 (SC4MD1). These can be used as normal I/O pin when serial interface is not used.

Pins	Pin NO	I/O	Function	Description
SCL4A SCL4B	56 35	I/O	IIC clock I/O pins	In serial interface 4 in IIC mode, this pin is configured as the clock I/O pin. For the output configuration, select Nch open-drain in P0ODC and P6ODC register and set pull-up resistor by P0PLU and P6PLU register. Select the output mode at P0DIR register and P6DIR register select serial clock I/O mode in serial mode register 1 (SC4MD1). These can be used as normal I/O pin when serial interface is not used
TM0IOA TM0IOB TM1IOA TM1IOB TM2IOA TM2IOB TM3IOA TM3IOB	1 24 2 51 3 24 4 52	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 3. To use this pin as event clock input, configure it as input by P0DIR, P6DIR and PADIR register. In the input mode, pull-up resistor can be selected in P0PLU, P6PLU, and PAPLU registers. For timer output, PWM signal output, select the special function pin in P0OMD1, P0OMD2, P6OMD and PAOMD registers, and set to the output mode in P0DIR, P6DIR and PADIR registers. These can be used as normal I/O pins when Timer I/O pin is not used.
BUZZER NBUZZER	46 45	Output	Buzzer output pins	Piezoelectric buzzer driving pin. Buzzer output is available to Port 5. The driving frequency can be set in DLYCTR register. In order to select Buzzer output, select the special function pin in P5OMD register, and set P5DIR register to the output mode. At the same time, select Buzzer output in oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when Buzzer output is not used.
TM7IOA TM7IOB TM8IOA TM8IOB	6 21 7 22	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer7and 8. To use this pin as event clock input, configure it as input with P0DIR and PADIR registers. In the input mode, pull-up resistor can be selected by P0PLU and PAPLU registers. For timer output, PWM signal output, select the special function pin in P0OMD1 and PAOMD registers, and set to the output mode in P0DIR and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins.
VREF+	9	-	A/D reference voltage input pin	Reference power supply pin for A/D converter. Normally, the values of VREF+ = VDD5 is used.
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7 AN8 AN9 AN10 AN11	1 2 3 4 5 6 7 8 80 79 78 77	input	Analog input pins	Analog input pins for 12-channel, 10-bit A/D converter. Select the analog input by PAIMD, PBIMD register. When not used for analog input, these pins can be used as normal input pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4	28 29 30 31 32	Input	External interrupt	External interrupt input pins. Select the external interrupt input enable by IRQCNT register. The valid edge for IRQ0 to 4 can be selected with IRQnICR register. IRQ2 to 4 can be set at both edges at pin voltage level. When not used for interrupts, these can be used as normal input pins.

Pins	Pin NO	I/O	Function	Description
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	49 48 47 46 45 44 43 42	Input	Key interrupt input pins	Input pins for KEY interrupt based on OR condition result of pin inputs. These can be set to key input pins by 1-bit with KEY interrupt control register (KEYT3_1IMD, KEY3_2_IMD). When not used for KEY input, these pins can be used as normal I/O pins.
LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7	1 2 3 4 5 6 7 8	Output	LED drive pins	Large current output pins. Select the large current output by LEDCNT registers. When not used for LED output, these pins can be used as normal I/O pins.
DMOD	20	Input	Mode switch input pins	Set always to VDD5.
MMOD	10	Input	ROM area switch input pins at start	Set always to VSS.

For the MMOD setup in rewriting the flash memory, refer to Technical Reference Manual.

4 Block Diagram

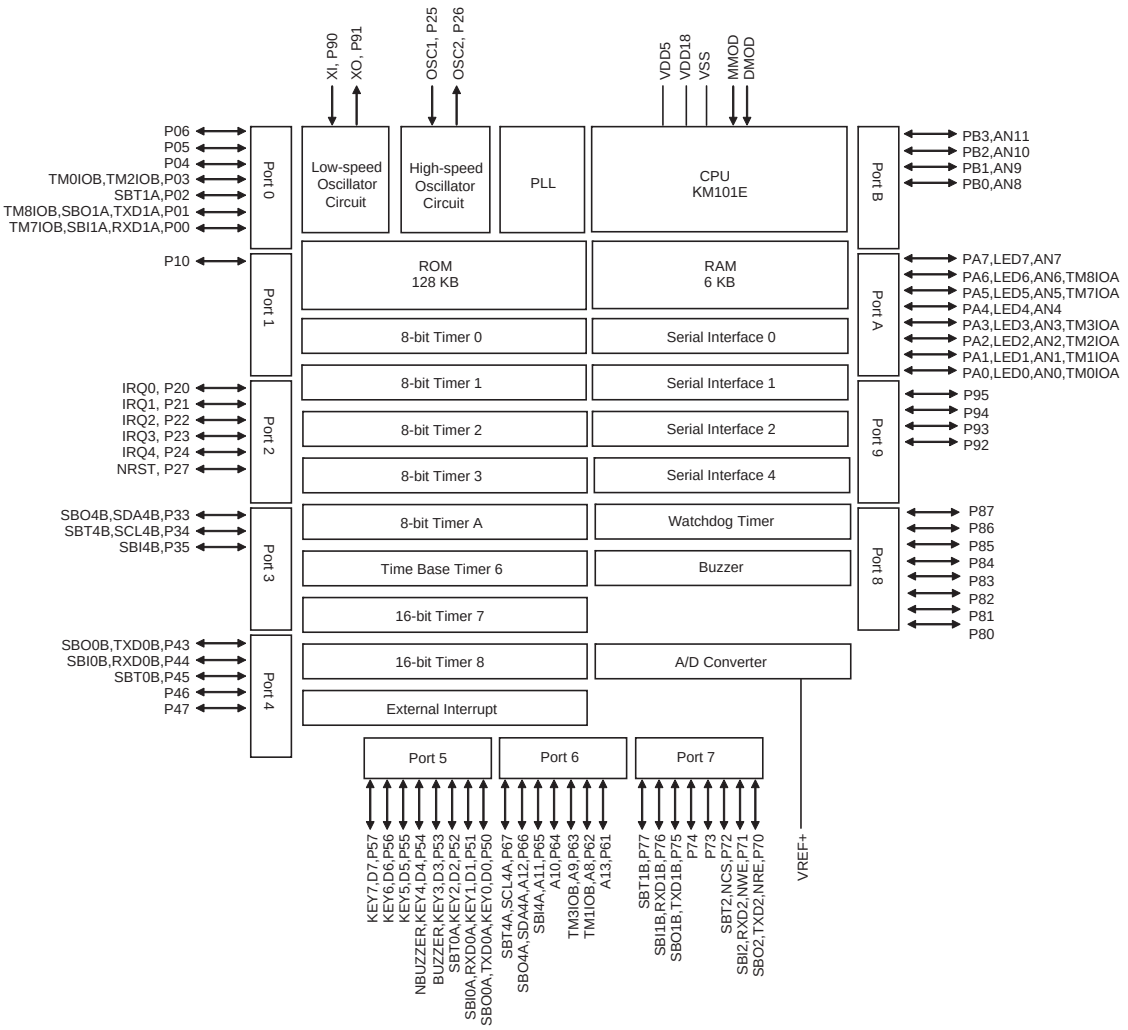

Figure: 4.1 Block Diagram

5 Electrical Characteristics

When using this LSI, consult our sales offices for the product specifications.

Structure	CMOS integrated circuit
Application	General-purpose
Function	CMOS 8-bit single chip microcomputer

5.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings *2 *3 *4 V_{SS} = 0 V

Parameter			Symbol	Rating	Unit
A1	Power supply voltage		V_{DD5}	-0.3 to +7.0	V
A2	Power supply voltage		V_{DD18}	-0.3 to +2.5	
A3	Input pin voltage		V_I	-0.3 to V_{DD5} +0.3 (upper limit: 7.0 V)	
A4	Output pin voltage		V_O	-0.3 to V_{DD5} +0.3 (upper limit: 7.0 V)	
A5	I/O pin voltage		V_{IO1}	-0.3 to V_{DD5} +0.3 (upper limit: 7.0 V)	
A6	Peak output current	LED output	I_{OL1} (peak)	30	mA
A7		Other than LED output	I_{OL2} (peak)	20	
A8		All pins	I_{OH} (peak)	-10	
A9	Average output current *1	LED output	I_{OL1} (avg)	20	
A10		Other than LED output	I_{OL2} (avg)	15	
A11		All pins	I_{OH} (avg)	-5	
A12	Power dissipation		P_D	400	mW
A13					
A14					
A15					
A16	Operating ambient temperature		T_{opr}	-40 to +85	°C
A17	Storage temperature		T_{STG}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 0.1 μF + 1.0 μF or larger between VDD5 pin and GND for the internal power voltage stabilization.

*3 Connect appropriate capacitor about 0.1 μF + 1.0 μF between VDD18 pin and VSS pin, near the microcontroller according to the Figure:1.5.1 shown below for the internal power supply stabilization.

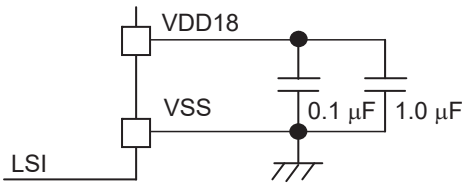

Figure: 5.1 Capacitor Connection between VDD18 and VSS Pins

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

5.2 Operating Conditions

B. Operating Conditions

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *5							
B1	Power supply voltage	V_{DD1}		4.0		5.5	V
B2	RAM retention power supply voltage	V_{DD2}	During STOP mode	2.2		5.5	V
Operating speed *6							
B3	Instruction execution time fs	t_{c1}	V_{DD5} = 4.0 V to 5.5 V (When ROMHND flag of HANDSHAKE register is “1”.)	0.05			µs
B4		t_{c2}	V_{DD5} = 4.0 V to 5.5 V (When ROMHND flag of HANDSHAKE register is “0”.)	0.10			µs
B5		t_{c3}	V_{DD5} = 4.0 V to 5.5 V	61			µs

*5 fs: Machine clock frequency

*6 tc1 to 2 : when the machine clock is selected from external high-speed oscillation, internal high-speed oscillation, or both the oscillations multiplied by PLL.

External Oscillator 1 Figure: 5.2

B6	Frequency	f_{hosc1}	V_{DD5} is within the specified operating power supply voltage range. (Refer to the ratings of B1 to B2 for the operating supply voltage range)	2.0		10	MHz
B7	Internal feedback resistor	R_{f10}	V_{DD5} = 5.0 V		980		kΩ

External Oscillator 2 Figure: 5.3

B8	Frequency	f_{sosc1}	V_{DD5} = 4.0 V to 5.5 V		32.768		kHz
B9	Internal feedback resistor	R_{f20}	V_{DD5} = 5.0 V		6.2		MΩ

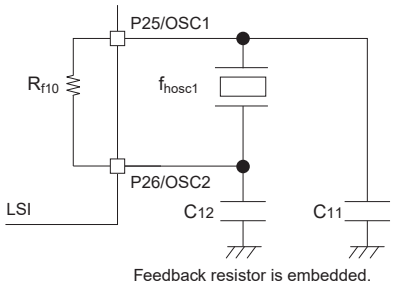

Figure: 5.2 External Oscillator 1

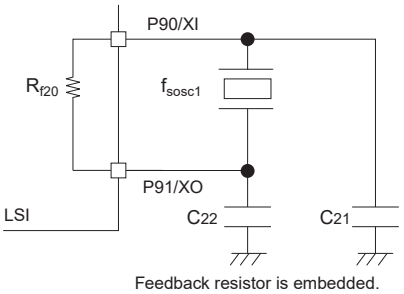

Figure: 5.3 External Oscillator 2

Connect external capacitors suited for the used oscillator.
The reference value denotes external capacity value based on our matching result.
When crystal oscillator or ceramic oscillator is used, the oscillation frequency is changed depending on the value of capacitor. For external capacity value, please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

V_{DD5} = 4.0 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
B10	Clock frequency	f_{hosc2}		2		10.0	MHz
B11	High-level pulse width *7	t_{wh1}	Figure:1.5.4	45			ns
B12	Low-level pulse width *7	t_{wl1}		45			
B13	Rising time	t_{wr1}	Figure:1.5.4	0		5.0	
B14	Falling time	t_{wf1}		0		5.0	

*7 The clock duty ratio should be 45 % to 55 %

External clock input 2 XI (XO is unconnected)

B15	Clock frequency	f_{sosc2}			32.768		kHz
B16	High-level pulse width *7	t_{wh2}	Figure:1.5.5		4.5		µs
B17	Low-level pulse width *7	t_{wl2}			4.5		µs
B18	Rising time	t_{wr2}	Figure:1.5.5	0		20	ns
B19	Falling time	t_{wf2}		0		20	ns

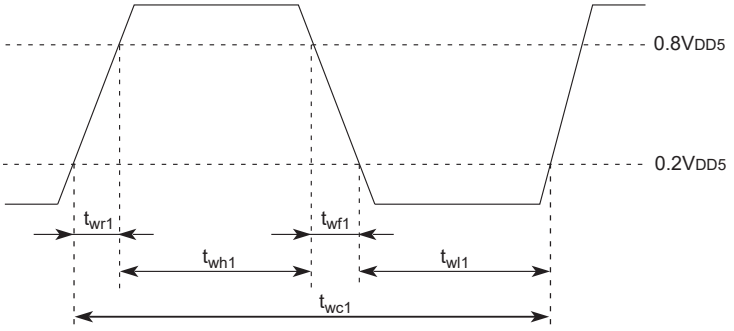

Figure: 5.4 OSC1 Timing Chart

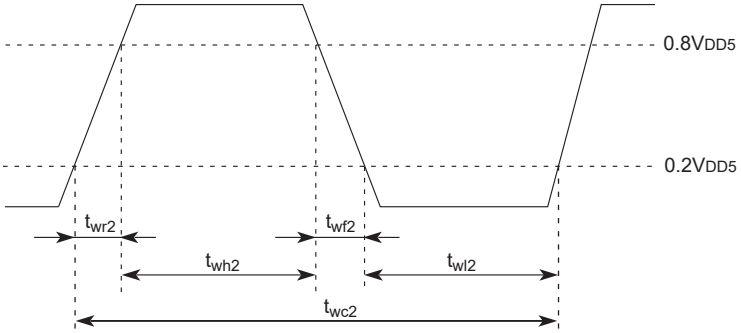

Figure: 5.5 XI Timing Chart

5.3 DC Characteristics

C. DC Characteristics

V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current *8							
C1	Power supply current during operation	I_{DD1}	V_{DD5}=5 V fosc=10 MHz [Double-speed mode: fs=fosc] (PLL is not used) *9		5	14	mA
C2		I_{DD2}	V_{DD5}=5 V fosc=10 MHz [Multiplied by 2, Divided by 2: fs=fosc] (PLL is used) *9		6	18	
C3		I_{DD3}	V_{DD5}=5 V fosc=10 MHz [Multiplied by 2: fs=20 MHz] (PLL is used) *9		9	20	
C4		I_{DD4}	V_{DD5}=5 V frc=16 MHz [Double-speed mode: fs=16 MHz] (PLL is not used) *9		6	15	
C5	Power supply current during operation	I_{DD5}	V_{DD5}=5 V fx=32.768 kHz [fs=fx/2]		200	400	µA
C6	Power supply current during STOP mode	I_{DD6}	V_{DD5}=5 V		145	245	µA

*8 Measured without loading (pull-up and pull-down resistors are not connected.)

To measure the power supply current during operation I_{DD1} to I_{DD4};
1. Set all I/O pins to input mode,
2. Set the CPU mode to “NORMAL mode”,
3. Fix pin MMOD to V_{SS} level and input pins to V_{DD5} level
4. Input the rectangular wave of 10 MHz with amplitude of V_{DD5} and V_{SS}, from pin OSC1.

To measure the power supply current during SLOW mode I_{DD5};
1. Set all I/O pins to input mode
2. Set the CPU mode to "SLOW mode"
3. Fix the MMOD to V_{SS} level and input pins to V_{DD5} level

To measure the power supply current during STOP mode I_{DD6};
1. Set the CPU mode to “STOP mode”,
2. Fix pin MMOD to V_{SS} level and input pin to V_{DD5} level
3. Open pin OSC1.

*9 When ROMHND flag of HANDSHAKE register is set to “1”

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 ATRST, MMOD							
C7	Input high voltage	V_{IH1}		0.8V_{DD5}		V_{DD5}	V
C8	Input low voltage	V_{IL1}		0		0.2V_{DD5}	
C9	Input leakage current	I_{LK1}	V_{IN} = 0 V to V_{DD5}			± 2	μA
Input pin 2 P27/NRST							
C10	Input high voltage	V_{IH2}		0.8V_{DD5}		V_{DD5}	V
C11	Input low voltage	V_{IL2}		0		0.15V_{DD5}	
C12	Pull-up resistor	R_{RH2}	V_{DD5}=5 V, V_{IN}= V_{SS}	10	50	100	kΩ
I/O pin 3 P00 to P06, P10, P20 to P26, P62 to P67, P70 to P77, P80 to P87							
C13	Input high voltage	V_{IH3}		0.8V_{DD5}		V_{DD5}	V
C14	Input low voltage	V_{IL3}		0		0.2V_{DD5}	
C15	Input leakage current	I_{LK3}	V_{IN}=0 V to V_{DD5}			± 2	μA
C16	Pull-up resistor	R_{RH3}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C17	Output high voltage	V_{OH3}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C18	Output low voltage	V_{OL3}	V_{DD5}=5.0 V, I_{OL}=1.0 mA			0.5	
I/O pin 4 PA0 to PA7							
C19	Input high voltage	V_{IH4}		0.8V_{DD5}		V_{DD5}	V
C20	Input low voltage	V_{IL4}		0		0.2V_{DD5}	
C21	Input leakage current	I_{LK4}	V_{IN}=0 V to V_{DD5}			± 2	μA
C22	Pull-up resistor	R_{RH4}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C23	Output high voltage	V_{OH4}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C24	Output low voltage 1	V_{OL41}	V_{DD5}=5.0 V, I_{OL}=1.0 mA LED output OFF			0.5	
C25	Output low voltage 2	V_{OL42}	V_{DD5}=5.0 V, IOL=15.0 mA LED output ON			1.0	

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 5 P50 to P57, P90, P91, P94							
C26	Input high voltage	V_{IH5}		$0.8V_{DD5}$		V_{DD5}	V
C27	Input low voltage	V_{IL5}		0		$0.2V_{DD5}$	
C28	Input leakage current	I_{LK5}	V_{IN}=0 V to V_{DD5}			± 2	μA
C29	Pull-up resistor	R_{RH5}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C30	Pull-down resistor	R_{RL5}	V_{DD5}=5.0 V, V_{IN}=V_{DD5} Pull-down resistor ON	10	50	100	
C31	Output high voltage	V_{OH5}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C32	Output low voltage	V_{OL5}	V_{DD5}=5.0 V, I_{OL}=1.0 mA			0.5	
Input pin 6 DMOD							
C33	Input high voltage	V_{IH6}		$0.8V_{DD5}$		V_{DD5}	V
C34	Input low voltage	V_{IL6}		0		$0.2V_{DD5}$	
C35	Pull-up resistor	R_{RH6}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ

5.4 A/D Converter Characteristics

D. A/D Converter Characteristics *10

V_{DD5} = 5.0 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D1	Resolution					10	Bits
D2	Non-linearity error 1		V_{DD5}=5.0 V, V_{SS}=0 V V_{REF+}=5.0 V T_{AD}=800 ns			± 3	LSB
D3	Differential non-linearity error 1					± 3	
D4	Zero transition voltage		V_{DD5}=5.0 V, V_{SS}=0 V V_{REF+}=5.0 V T_{AD}=800 ns		10	30	mV
D5	Full-scale transition voltage			4970	4990		
D6	A/D conversion time		T_{AD}=800 ns	12.93			µs
D7	Sampling time		T_{AD}=800 ns	1.6			
D8	Reference voltage	V_{REF+}	Note)	4.0		V_{DD5}	V
D9	Analog input voltage			V_{SS}		V_{REF+}	
D10	Analog input leakage current		Channel OFF V_{ADIN}=V_{SS} to V_{DD5}			± 2	µA
D11	Reference voltage pin input leakage current		Ladder resistance OFF V_{SS} ≤ V_{REF+} ≤ V_{DD5}			± 5	
D12	Ladder resistance	R_{LADD}	V_{DD5}=5.0 V	15	40	80	kΩ

*11 T_{AD} is A/D conversion clock cycle.
The specification values of D2 to D5 are guaranteed on the condition of V_{DD5}=V_{REF+}=5 V, V_{SS}=0 V.

Even if A/D function is not used, the voltage of VREF+ pin must be set between 4.0 V and V_{DD5}.

5.5 Auto Reset Characteristics

E. Auto Reset Characteristics

$V_{DD5} = V_{RST}$ to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
E1	Operating supply voltage	V_{DD7}	Auto reset is used	V_{RST}		5.5	V
Power supply voltage							
E2	Power detection level	V_{RST1}	At rising	4.10	4.30	4.50	V
E3	Power detection level	V_{RST2}	At falling	4.00	4.20	4.40	
E4	Supply voltage change rate	$\Delta t/\Delta V$		2			ms/V

5.6 Internal High-speed Oscillation Circuit

F. Internal High-speed Oscillation Circuit

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
F1	Internal high-speed oscillation circuit frequency	f_{rc}	Ta = -40 °C to +85 °C		16		MHz
F2	Temperature dependence of oscillation frequency	f_{rc3}	Ta = 25 °C	-5.0		5.0	%
F3		f_{rc4}	Ta = -40 °C to +85 °C				

5.7 Flash EEPROM Program Conditions

G. Flash EEPROM Program Conditions

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V*11
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
G1	Programming supply voltage	V_{DDEW}		4.0		5.5	V
G2	Programming/Erasing times of 32KB, 20KB Sector *2	E_{MAX1}		1000			Times
G3	Programming/Erasing times of 4KB Sector *2	E_{MAX2}		10000			Times
G4	Data retention period of 32KB, 20KB Sector *1	T_{HOLD1}	Ta= 85°C, P/E times ≤ 1000	20			Years
G5	Data retention period of 4KB Sector *1	T_{HOLD2}	Ta= 85°C, P/E times ≤ 1000 *2	20			Years
		T_{HOLD3}	Ta= 65°C, P/E times ≤ 10000 *2	20			Years

*1 Contain the period when power supply voltage is not supplied.

*2 Programming/Erasing times(P/E Times) is counted by the number of time a sector is erased. It is controlled on sector basis. For example, if writing 1 byte of data in any sector for hundred of times and then erasing the sector, a single rewriting is counted. Also, the number of times of rewriting in another sector, in which erasing is not performed, is not counted. Overwriting data is disabled. To rewrite data, write the data after erasing sectors.

6 Package Dimension

■ LQFP 80-pin (14 mm × 14 mm / 0.65 mm pitch)

Unit: mm

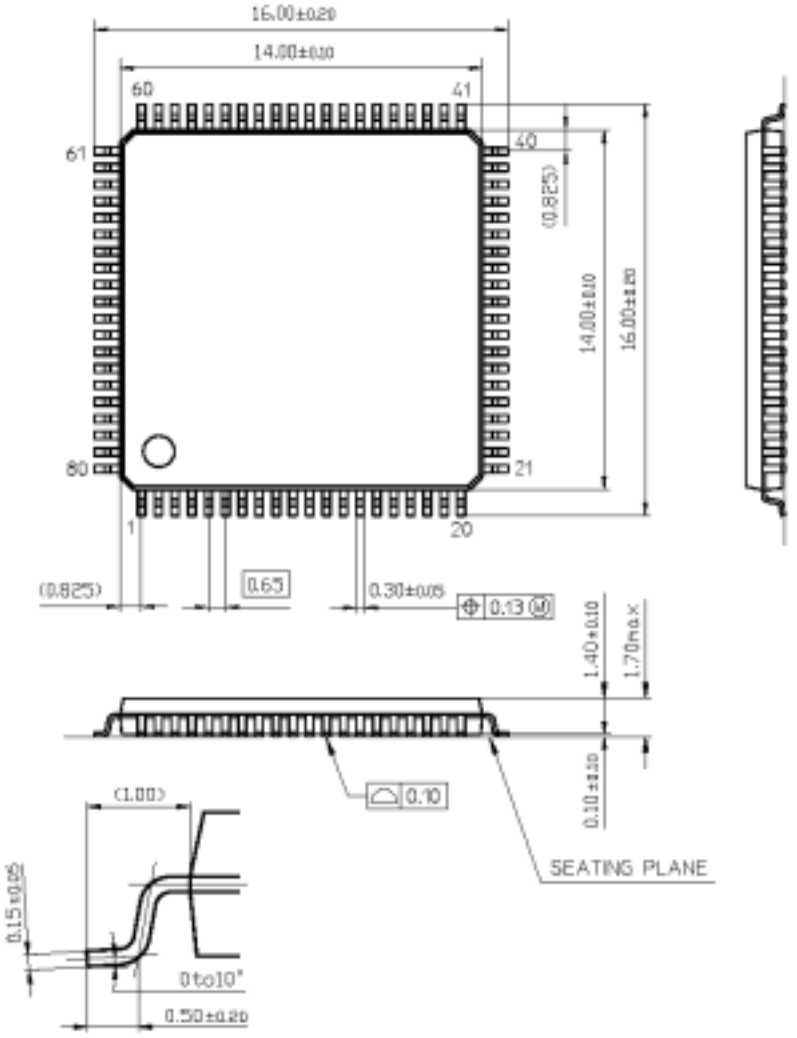

Figure: 6.1 LQFP 80-pin Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

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