



- +1500W continuous output power (no derating across full DC input range)
- 93% efficiency
- 12V Main output
- 3.3V; 5V or 12V Standby voltage options
- 1U height: 2.15" x 12.65" x 1.57"
- > 35 Watts per cubic inch density
- N+1 redundancy, hot plug/swap (up to 8 modules in parallel)
- Active current sharing on 12V main output; Integral ORing /isolation device MOSFET
- Internal cooling fan (variable speed) Overvoltage, overcurrent, overtemperature protection
- PMBus™/I²C interface with LED status indicator
- RoHS compliant
- Two Year Warranty

PRODUCT OVERVIEW

D1U54-D-1500-12-HxxC series of 1500 watt DC-DC highly efficient front end power converter modules provide a 12V main and a standby output. The power module is able to current share with up to eight (8) other power converter modules of the same type operating in parallel or N+1 redundancy. This series may be hot plugged and include integral output isolation devices, and are fully protected from overload and overvoltage and auto-recover from temperature faults. A Status LED is provided on the front panel and additional control and status reporting is provided by hardware logic signals and via a PMBus™ digital interface.

The low profile sub 1U height enclosure with power density of >35W/in³ make this an excellent choice for delivering reliable, efficient power to servers, workstations, storage systems and other 12V distributed power systems including direct operation from intermediate bus converters.

ORDERING GUIDE*

Part Number	Internal MPN	Power Output	Main Output	Standby Output	Airflow
D1U54-D-1500-12-HC4C	M1900	1500W -48 to -60Vdc 45°C	12V	3.3V	Back to Front
D1U54-D-1500-12-HA4C	M1897			5V	
D1U54-D-1500-12-HB4C	M1903			12V	
D1U54-D-1500-12-HC3C	M1901			3.3V	Front to Back
D1U54-D-1500-12-HA3C	M1898			5V	
D1U54-D-1500-12-HB3C	M1902			12V	

*See www.murata.com/products/power for model-specific availability.

INPUT CHARACTERISTICS

Parameter	Conditions	Min	Nom.	Max	Units
DC Input Voltage Operating Range		-40	-48 - -60	-72	Vdc
Turn-on Input Voltage	Ramp Up	-39	-40	-41	
Turn-off Input Voltage	Ramp Down	-35	-36	-37	
Maximum Current	1500W, Vin = -48Vdc to -60Vdc			44	Adc
DC Input Inrush Peak Current	Cold start between 0 to 200ms	-48Vdc		50	Apk
		-72Vdc		100	
Efficiency ⁴	20% FL	91.5	92		%
	50% FL	92.5	93		
	100% FL	88	90		
Reverse polarity protection	Withstand Reversed input cables; no internal/external fuse failure	+40		+72	Vdc

OUTPUT VOLTAGE CHARACTERISTICS

Output Voltage	Parameter	Conditions	Min.	Nom.	Max.	Units
Main 12V	Voltage Set Point			12		Vdc
	Line & Load Regulation	Combined, measured at remote sense	-1		+1.5	%
	Ripple & Noise ^{1,2}	20MHz Bandwidth			120	mV P-P
	Output Current	-40Vdc to -72Vdc DC input	0		125A	A
	Load Capacitance				30,000	µF
3.3 VSB	Voltage Set Point			3.3		Vdc
	Line & Load Regulation	Combined regulation	3.14		3.46	Vdc
	Ripple Voltage & Noise ^{1,3}	20MHz Bandwidth			120	mV P-P
	Output Current		0		4	A
	Load Capacitance				3,000	µF
5 VSB	Voltage Set Point			5.0		Vdc
	Line & Load Regulation		4.76		5.24	Vdc
	Ripple Voltage & Noise ^{1,3}	20MHz Bandwidth			120	mV P-P
	Output Current		0		4	A
	Load Capacitance				3,000	µF
12 VSB	Voltage Set Point			12.0		Vdc
	Line & Load Regulation		11.4		12.6	Vdc
	Ripple Voltage & Noise ^{1,3}	20MHz Bandwidth			120	mV P-P
	Output Current		0		2.5	A
	Load Capacitance				1,000	µF

¹ Ripple and noise are measured with 0.1 µF of ceramic capacitance and 10 µF of tantalum capacitance on each of the power supply outputs. A short coaxial cable to the measurement 'scope input, is used.

² Minimum load 5A

³ Minimum load 0.25A

⁴ Vin: -48Vdc; Fan is off; Tambient = 25°C



For full details go to
www.murata-ps.com/rohs



Self-declared to LVD



OUTPUT CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Remote Sense (Main Output)	Overall compensation at full load; +VE & -VE connections			120	mV
Output Rise (Monotonic)	10% to 95% rise time	No positive voltage excursion above set point			
Startup Time	DC Ramp Up			3	s
	PS_ON activation		200		ms
Transient Response	12V, 10%-60% and 50-100% or 60%-10% and 100-50% step load; 1A/μs slew rate		±600		mV
	3.3/5VSB 50-100% or 100-50% step load 1A/μs slew rate		±165/±250		
Current Sharing Accuracy (between sharing modules; up to 8 in parallel)	At 100% load			±10	%
Hot Swap Transients				5	%
Hold Up Time ¹	FL (Full Load); 48VDC nominal input prior to hold up	1			ms
	HL (Half Load); 48VDC nominal input prior to hold up	2			ms

¹ Assumes deployment within systems utilizing dual redundant "A" and "B" DC input feeds

ENVIRONMENTAL CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Storage Temperature Range	Non-Condensing	-40		70	°C
Operating Temperature Range ¹	1500W Output Power; See Derating Curve	-5		45	
Operating Humidity	Non-Condensing	5		90	%
Storage Humidity		5		95	
Altitude (no derating ≤40°C)				3000	m
Shock	Non-Operating			30	G
Sinusoidal Vibration	Non-operating, 0.5G; 5-500Hz				
MTBF (Target)	Telcordia SR-332 M1C1 @ 40°C	452			K Hours
Safety Approvals (Standards)	CAN/CSA-C22.2 No. 60950-1-07, Amendment 1:2011, Amendment 2:2014 (MOD) [CSA] ANSI/UL Std. No. 60950-1-2014 - Information Technology Equipment – Safety – Part 1: General Requirements [CSA] IEC 60950-1:2005, IEC 60950-1:2005/AMD1:2009, IEC 60950-1:2005/AMD2:2013 [CSA] EN 60950-1:2006+A11:2009+A1:2010+A12:2011+A2:2013 [SELF-DECLARATION]				
	CAN/CSA-C22.2 No. 62368-1:14 [CSA] UL 62368-1 2nd Ed. [CSA] IEC 62368-1:2014 [CSA] EN 62368-1:2014 [SELF-DECLARATION]				
Input Fusing	GB17625.1-2012, GB4943.1-2011, GB/T9254-2008 (Class A) [CQC] IS 13252(Part 1):2010/ IEC 60950-1 : 2005 [BIS] K60950-1(2011-12) [KCC] AS/NZS 60950.1:2015 [RCM] ДСТУ EN 60950-1:2015 (Safety) & ДСТУ EN 55032:2014, ДСТУ EN 61000-4-2:2008, ДСТУ IEC 61000-4-3:2007 (EMC) [UKRAINE]				
	Internal 60A/170VDC fast blow fuse on the DC line input				
Weight				2.314/1.05	lbs/kg

¹ Intake air temperature, based on stand-alone power supply module operated in free airflow environment. Airflow conditions imposed by host/system may impact result

ISOLATION CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Insulation Safety Rating/Test Voltage	Input to Outputs		1500		Vdc
Isolation	Output to Chassis (Ground), functional		500		Vdc

PROTECTION CHARACTERISTICS

Output Voltage	Parameter	Conditions	Min.	Typ.	Max.	Units
12V (Main)	Over-Temperature ^{1,2,3}	Air inlet temperature; Auto re-start	60		82	°C
	Over-Voltage	Latching; toggle PS_ON or recycle DC input to reset	13		14	V
	Over-Current	For slow overload events a constant current will be sustained for 1sec followed by a latch off that will auto reset in 5secs.	140		160	A
		For hard (short circuit) events the output will shut down within 50ms and auto restart within 200ms. This cycle will be repeated ten times at which point the output will permanently latch off. The power module will require to be reset by recycling the incoming DC source or by "toggling" PS_ON.				
3.3VSB	Over-Voltage	Latching; toggle PS_ON or recycle DC input to reset	3.4		4.0	V
	Over-Current	Shutdown followed by auto-recovery	4.5		6	A
5VSB	Over-Voltage	Latching; toggle PS_ON or recycle DC input to reset	5.4		6.0	V
	Over-Current	Shutdown followed by auto-recovery	4.5		6	A
12VSB	Over-Voltage	Latching; toggle PS_ON or recycle DC input to reset	13.0		14.5	V
	Over-Current	Shutdown followed by auto-recovery	2.75		3.75	A

¹ As detected and reported by the PMBus™ air intake temperature sensor, operated as a component in free air. Airflow conditions imposed by Host/System may impact results. A gradient between PMBus™ intake air temperature reported and that of an external thermocouple may be observed due to the difference in sensor locations. Refer to ACAN-67 PMBus™ application notes for additional details.

² Warning indication (PMBus™ status register bits, SMB_ALERT and Amber LED status) occurs at approximately 75°C and recovers at approximately 70°C as detected by the PMBus™ intake air temperature sensor; fault indication and shutdown engages at approximately 80°C nominal and recovers at approximately 75°C nominal

³ Operating the power supply above the maximum operating temperature specified in "ENVIRONMENTAL CHARACTERISTICS" is considered an abnormal condition and may negatively impact power supply life and is not recommended.

EMISSIONS AND IMMUNITY

Characteristic	Standard	Compliance
Conducted Emissions	FCC 47 CFR Part 15 CSIPR 22/EN55022	Class A with 6dB margin
ESD Immunity	IEC/EN 61000-4-2;	Level 4; Criteria A
Radiated Field Immunity	IEC/EN 61000-4-3	Level 2; Criteria B
Electrical Fast Transients/Burst Immunity	IEC/EN 61000-4-4	Level 2; Criteria A
Surge Immunity	IEC/EN 61000-4-5	Level 2; Criteria A
RF Conducted Immunity	IEC/EN 61000-4-6	Level 2; Criteria A
Magnetic Field Immunity	IEC/EN 61000-4-8	3A/m; Criteria B
Voltage Dips & Interruptions	NEBS GR-1089-CORE Issue	Relevant sections and compliance levels TBD

LED STATUS INDICATOR

A single bi-colour (Amber/Green) LED provides hardware status indication of following conditions:

Condition	Green led status (power) led status	Amber led status (fault)
No incoming DC supply present; power module is completely off.	LED not illuminated	LED not illuminated
Standby Rail ON; Main Output OFF; DC input present & correct	Blinking	-
Standby Rail ON; Main Output ON	Solid Green	-
Main Output overcurrent; undervoltage, overvoltage warning	-	Solid Amber
FAN_FAULT; overtemperature; standby rail overcurrent, Main Output overcurrent or overvoltage	-	Solid Amber
Power Module Warning Event	-	Blinking

ADDR ADDRESS SELECTION

ADDR pin (A3) resistor to GND (Kohm ±5%)	Power Supply Main Controller PMbus Slave address	Power Supply External EEPROM PMbus Slave address
0.82	0xB0	0xA0
2.7	0xB2	0xA2
5.6	0xB4	0xA4
8.2	0xB6	0xA6
15	0xB8	0xA8
27	0xBA	0xAA
56	0xBC	0xAC
180	0xBE	0xAE

STATUS AND CONTROL SIGNALS

Signal Name	I/O	Description	Interface Details
INPUT_OK (DC Source)	Output	The signal output is driven high when the input source is available and within acceptable limits. The output is driven low to indicate loss of input power. There is a minimum of 0.5ms pre-warning time before the signal is driven low prior to the PWR_OK signal going low. The power supply must ensure that this interface signal provides accurate status when input source is lost.	Pulled up internally via 10K to VDD ¹ . A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
PW_OK (Output OK)	Output	The signal is asserted (driven high) by the power supply to indicate that all outputs are valid. If any of the outputs fail then this output will be hi-Z or driven low. The output is driven low to indicate that the Main output is outside of lower limit of regulation (11.4Vdc).	Pulled up internally via 10K to VDD ¹ . A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
SMB_ALERT (FAULT/WARNING)	Output	The signal output is driven low to indicate that the power supply has detected a warning or fault and is intended to alert the system. This output must be driven high when the power is operating correctly (within specified limits). The signal will revert to a high level when the warning/fault stimulus (that caused the alert) is removed.	Pulled up internally via 10K to VDD ¹ . A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
PRESENT_L (Power Supply Absent)	Output	The signal is used to detect the presence (installed) of a module by the host system. The signal is connected to PSU logic SGND within the power module.	Passive connection to +VSB_Return. A logic low <0.8Vdc
PS_ON (Power Supply Enable/Disable)	Input	This signal is pulled up internally to the internal housekeeping supply (within the power supply). The power supply main 12Vdc output will be enabled when this signal is pulled low to +VSB_Return. In the low state the signal input shall not source more than 1mA of current. The 12Vdc output will be disabled when the input is driven higher than 2.4V, or open circuited. Cycling (toggling) this signal shall clear latched fault conditions.	Pulled up internally via 10K to VDD ¹ . A logic high >2.0Vdc A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer.
PS_KILL	Input	This signal is used internally by power module during hot swap to disable both outputs when module is extracted during hot swap. The signal is provided on a short (lagging pin) and should be permanently connected to +VSB_Return within the host/system	Pulled up internally via 10K to VDD ¹ . A logic high >2.0Vdc A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer.
ADDR (Address Select)	Input	An analog input that is used to set the address of the internal slave devices (EEPROM and microprocessor) used for digital communications. Connection of a suitable resistor to +VSB_Return, in conjunction with an internal resistor divider chain, will configure the required address.	DC voltage between the limits of 0 and +3.3Vdc.
SCL (Serial Clock)	Both	A serial clock line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. No additional internal capacitance is added that would affect the speed of the bus. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered.	VIL is 0.8V maximum VOL is 0.4V maximum when sinking 3mA VIH is 2.1V minimum
SDA (Serial Data)	Both	A serial data line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered,	VIL is 0.8V maximum VOL is 0.4V maximum when sinking 3mA VIH is 2.1V minimum
V1_SENSE V1SENSE_RTN	Input	Remote sense connections intended to be connected at and sense the voltage at the point of load. The voltage sense will interact with the internal module regulation loop to compensate for voltage drops due to connection resistance between the output connector and the load. If remote sense compensation is not required then the voltage can be configured for local sense by: 1. V1_SENSE directly connected to power blades 6 to 10 (inclusive) 2. V1_SENSE_RTN directly connected to power blades 1 to 5 (inclusive)	Compensation for up to 0.12Vdc total connection drop (output and return connections).
ISHARE	Bi-Directional Bus	The current sharing signal is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage; however a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% load (module capability). For two identical units sharing the same 100% load this would read 4VDC for perfect current sharing (i.e. 50% module load capability per unit).	Analogue voltage: +8V maximum; 10K to +12V_RTN

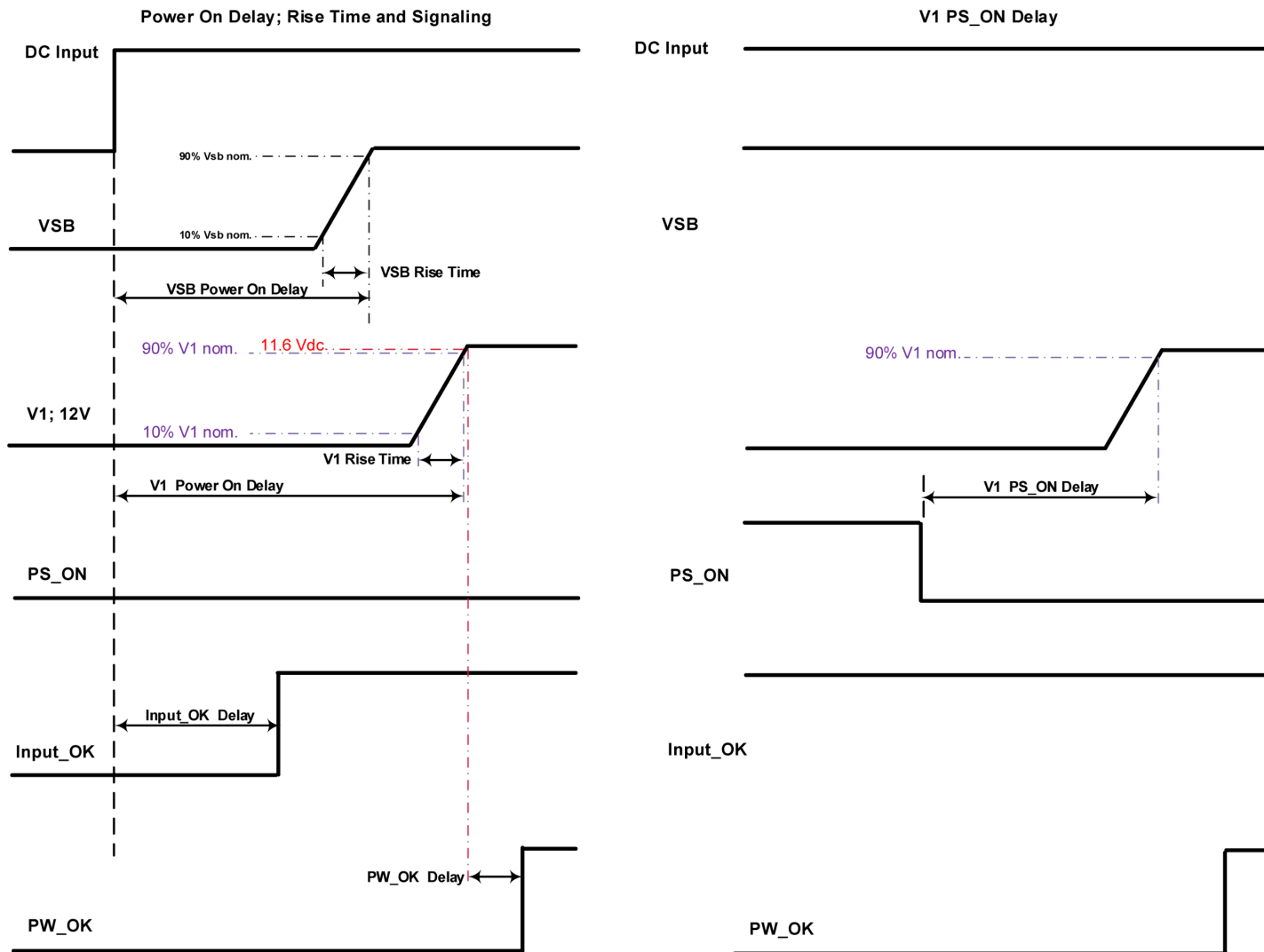
¹ VDD is an internal voltage rail derived from VSB and an internal housekeeping rail ("diode ORed"); this rail is compatible with the voltage levels of TTL and CMOS logic families.

TIMING SPECIFICATIONS

Unless otherwise specified, the following notes apply to all timing specifications:

1. $T_a = 25^\circ\text{C}$, V_{in} & $V_{in\text{ nom.}}$ = -48V
2. Resistive load, 100% full load, both outputs

Turn-On Delay & Output Rise Time:



Time	Description	Min.	Max.
Vsb Rise time	Vsb rising from 10% to 90% Vsb nom.	15ms	100ms
V1 Rise time	V1 rising from 10% to 90% V1 nom.	100ms	220ms
Vsb Power-on-delay	From application of $V_{in\text{ nom.}}$ to Vsb reaching 90% Vsb, nom.; See Figure 7	-	1400ms
V1 Power-on-delay	From application of V_{in} to V1 reaching 90% of $V_{out\text{ nom.}}$	500ms	1750ms
V1 PS_ON delay	From PS_ON signal edge to V1 reaching 90% of $V_{out\text{ nom.}}$; See Figure 9	-	500ms
V1 PW_OK delay	From V1 reaching 11.6V (Typ.) to asserted PW_OK signal; See Figure 3	50ms	500ms
Input_OK delay	From application of V_{in} to assertion of Input_OK Signal edge; See Figure 1	500ms	1200ms

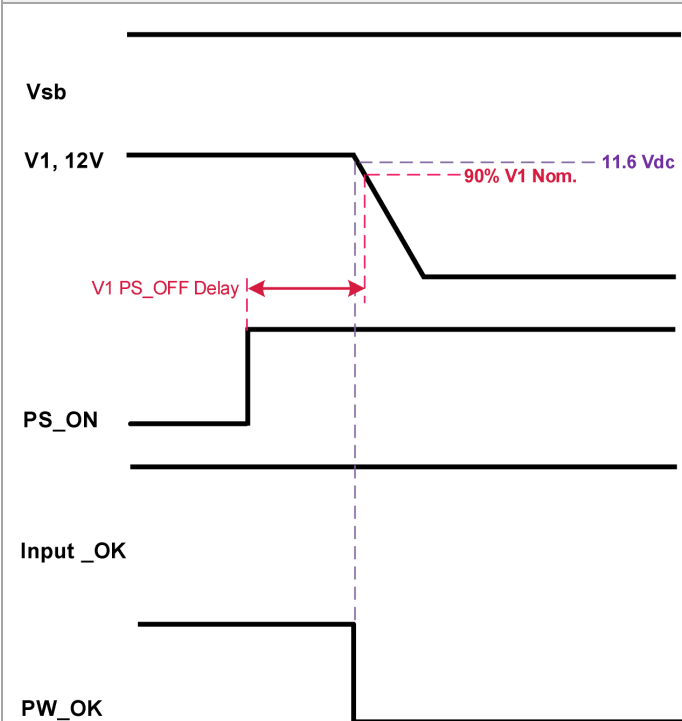
(CONTINUED)

TIMING SPECIFICATIONS

Unless otherwise specified, the following notes apply to all timing specifications:

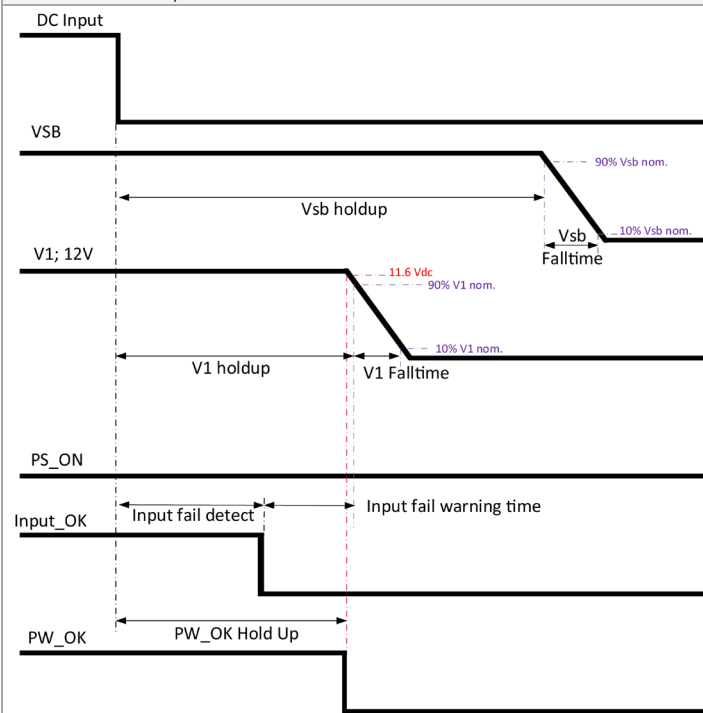
1. $T_a = 25^\circ\text{C}$, V_{in} & $V_{in\text{ nom.}} = -48\text{V}$
2. Resistive load, 100% full load, both outputs

Turn-Off (Shutdown by PS_ON)



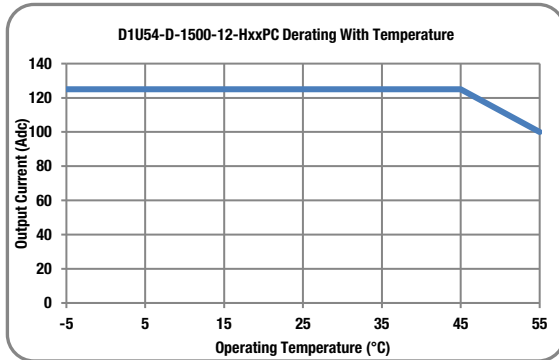
Turn-Off Timing	Description	Min.	Typ.	Max.
V1 PS_OFF delay	From the rising edge of PS_ON signal to V1 falling below 90% V1 nom. See Figure 10	0ms	2.5ms	6ms

Power Removal Holdup



Power Removal Timing	Description	Min	Max
Vsb holdup	From loss of V_{in} to Vsb falling to 90% Vsb nom.; See Figure 8	3ms	-
V1 holdup (Total Effective)	From loss of V_{in} to V1 falling to 90% Vout nom.; See Figure 6	1ms	-
Input fail detect	From loss of V_{in} to falling edge of Input_OK signal; See Figure 4	-	2ms
Input fail warning time	From falling edge of Input_fail detect to V1 falling to 90% Vout nom.; See Figure 5	250us	-
PW_OK Hold Up	Negates when V1 falls to 11.6V (Typ.)	1ms	-

DERATING CURVE



NOTE: The D1U54-D-1500-12-HxxPC power supply has an internal variable speed, automatically controlled to achieve the required cooling airflow based on strategically located internal airflow and hotspot sensors prevailing operating temperature/conditions and output loading. The fan speed can also be manually controlled via PMBus™, refer to the PMBus™ ACAN for additional details

TYPICAL PERFORMANCE CURVES

Timing Plots: $T_a = 25^\circ\text{C}$, $V_{in \text{ nom.}} = -48\text{V}$, 100% load, constant current load setting 100% full load, both outputs



Figure 1: Turn-on by Vin; input to Input_OK signal; [Back](#)



Figure 2: Turn-on by Vin; Input_OK to Output V1 Delay



Figure 3: Turn-on by Vin; Vout to PW_OK delay; [Back](#)

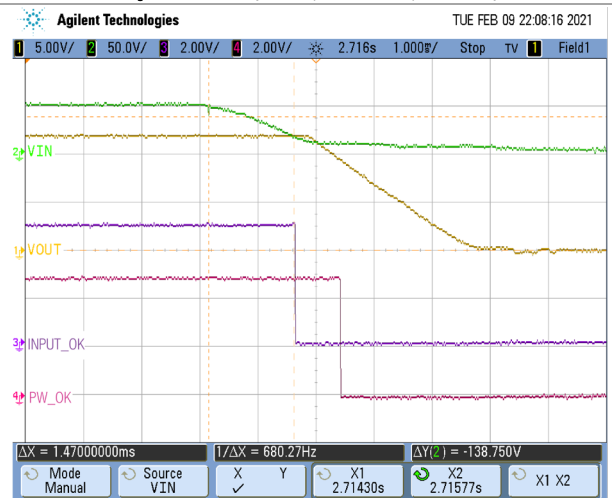


Figure 4: Turn-off by Vin removal; Input to Input_OK delay; [Back](#)

TYPICAL PERFORMANCE CURVES

Timing Plots: Ta= 25°C, Vin nom. = -48V, 100% load, constant current load setting 100% full load, both outputs

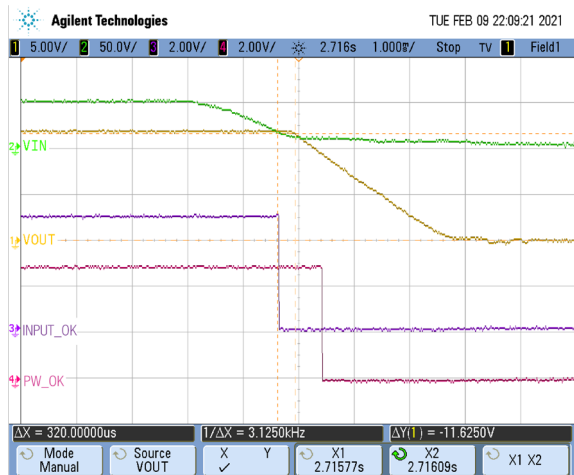


Figure 5: Turn off by Vin removal; Input_OK to Vout Delay; [Back](#)

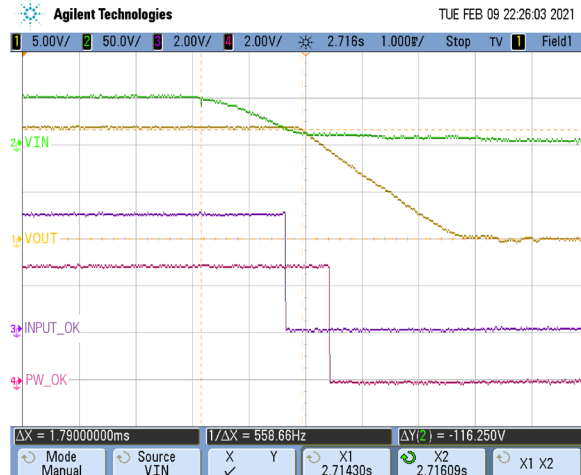


Figure 6: Hold-up time V1; [Back](#)

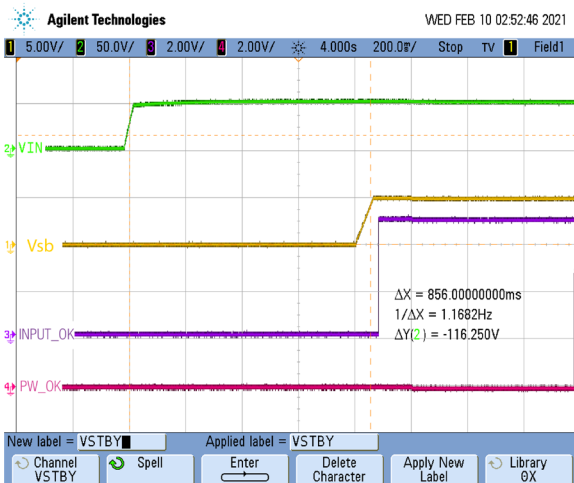


Figure 7: Turn-on Delay; Vin to Vsb delay; [back](#)

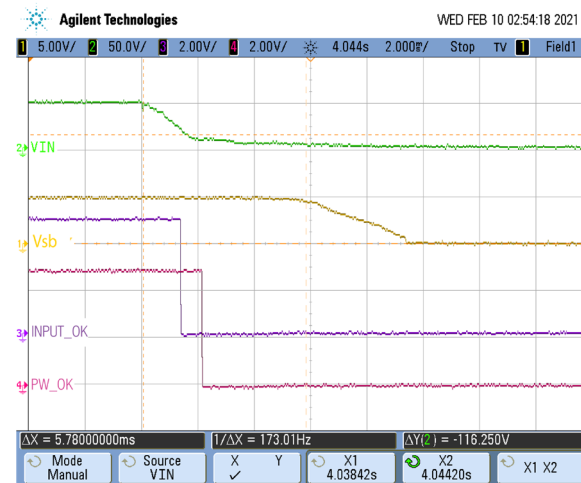


Figure 8: Vsb hold-up time; [Back](#)



Figure 9: Turn-on by PS_ON Delay; [Back](#)

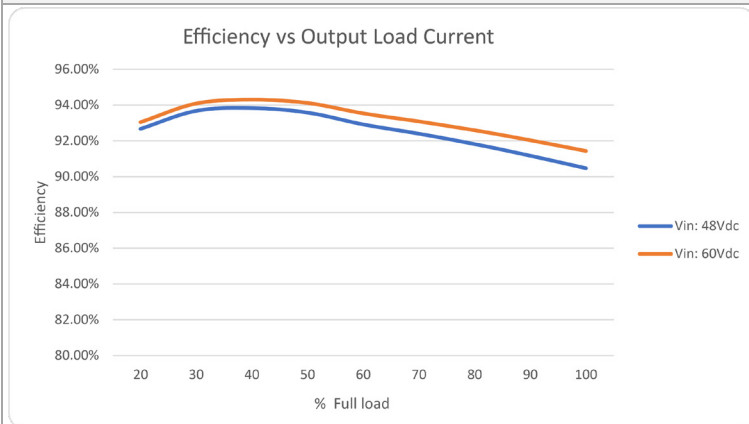


Figure 10: Turn-off by PS_ON Delay; [Back](#)

(CONTINUED):

TYPICAL PERFORMANCE CURVES

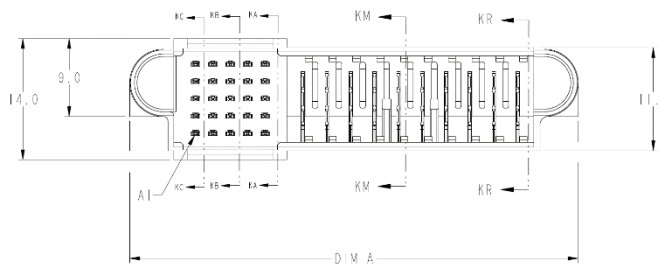
Efficiency; Ta: 25°C, Fan speed commanded to 0% duty cycle



OUTPUT CONNECTOR SPECIFICATION

Power Converter Side: FCI P/N 10122460-005LF:

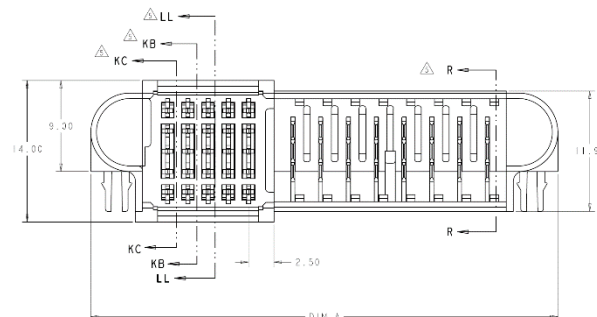
PART NUMBER	ROWS	SIGNALS					POWERS									
		1	2	3	4	5	1	2	3	4	5	6	7	8	9	10
10122460-005LF 25S + 10P	E															
	D															
	C															
	B															
	A															



Note "2" refers to the longest signal pin/power blade & "3" is the "shortest" signal pin such that the "shortest" is the "last to make, first to break" in the mating sequence.

Alternate Power Converter Side: connector TE Connectivity P/N 1926734-2:

PART NUMBER	ROWS	SIGNALS					POWERS									
		1	2	3	4	5	1	2	3	4	5	6	7	8	9	10
1926734-2 25S X 10P	E															
	D															
	C															
	B															
	A															



Note "2" refers to the longest signal pin/power blade & "1" is the "shortest" signal pin such that the "shortest" is the "last to make, first to break" in the mating sequence.

Mating (system side) Part Numbers:

FCI 10108888-R10253SLF

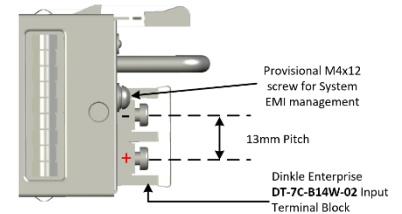
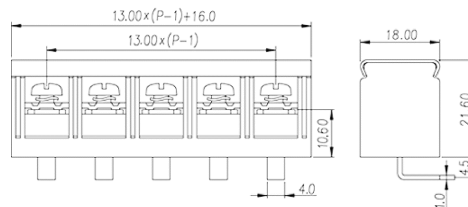
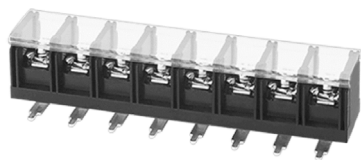
TE Connectivity PN 2-1926739-5

CONNECTOR INTERFACE PIN ASSIGNMENTS, POWER CONVERTER SIDE

Pin	Function	Description	Pin	Function	Description
6, 7, 8, 9, 10	V1 (+12VOUT)	+12V Main Output	C3	SDA	I2C Serial Data Line
1, 2, 3, 4, 5	+12V RTN/PGND	+12V Main Output Return	D3	V1_SENSE_R	Remote Sense Return (-VE)
A1	+VSB	Standby Output	E3	V1_SENSE	Remote Sense (+VE)
B1	+VSB	Standby Output	A4	SCL	I2C Serial Clock Line
C1	+VSB	Standby Output	B4	PS_ON_L	Remote On/Off (Enable/Disable)
D1	+VSB	Standby Output	C4	SMBALERT#	Alert signal to host system
E1	+VSB	Standby Output	D4	Unused	No End User Connection
A2	+VSB_Return	Standby Output Return	E4	INPUT_OK	DC Input Source Present & "OK"
B2	+VSB_Return	Standby Output Return	A5	PS_KILL	Power Supply "kill"; short pin
C2	Unused	No End User Connection	B5	ISHARE	Current Share bus; short pin
D2	Unused	No End User Connection	C5	PW_OK	Power "OK"; short pin
E2	Unused	No End User Connection	D5	Unused	No End User Connection
A3	ADDR	I2C Address	E5	PRESENT_L	Power Module Present; short pin
B3	Unused	No End User Connection			

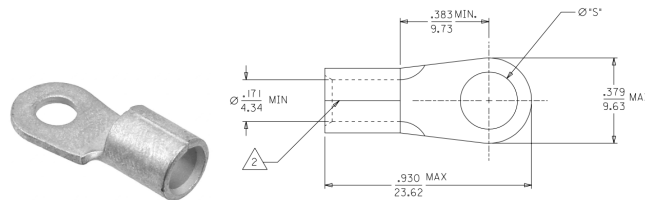
POWER SUPPLY INPUT TERMINAL BLOCK

Dinkle Enterprise DT-7C-B14W-02 (2 Position)



Compatible Mating Ring Terminals¹

Molex 0191930200



MATERIAL NUMBER	ENGINEERING NUMBER	STUD SIZE	*5" ±.003/(0.08)	PACKAGING
191930198	D-356-06	6	.146/(3.70)	LOOSE PIECE
191930200	D-356-08	8	.173/(4.39)	
191930202	D-356-10	10	.198/(5.03)	
191930204	D-356-14	14	.265/(6.73)	
191930199	D-356-06T	6	.146/(3.70)	TAPE
191930201	D-356-08T	8	.173/(4.39)	
191930203	D-356-10T	10	.198/(5.03)	
191930205	D-356-14T	14	.265/(6.73)	

HUBBELL (Burdny)
YA8CLNT8_{xx}

XX=BEND ANGLE OPTION:
45=45° and 90=90°

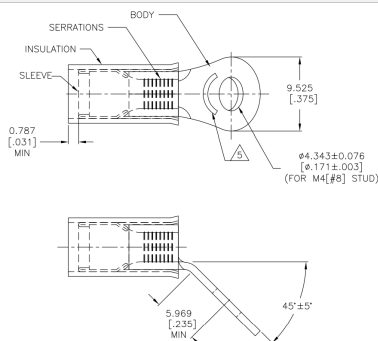


(CONTINUED):

POWER SUPPLY INPUT TERMINAL BLOCK

Dinkle Enterprise DT-7C-B14W-02 (2 Position)

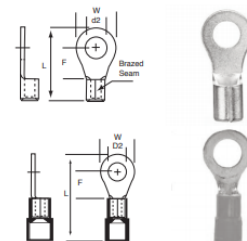
TE Connectivity 195845-1



8 AWG RING TERMINALS (8 mm²)

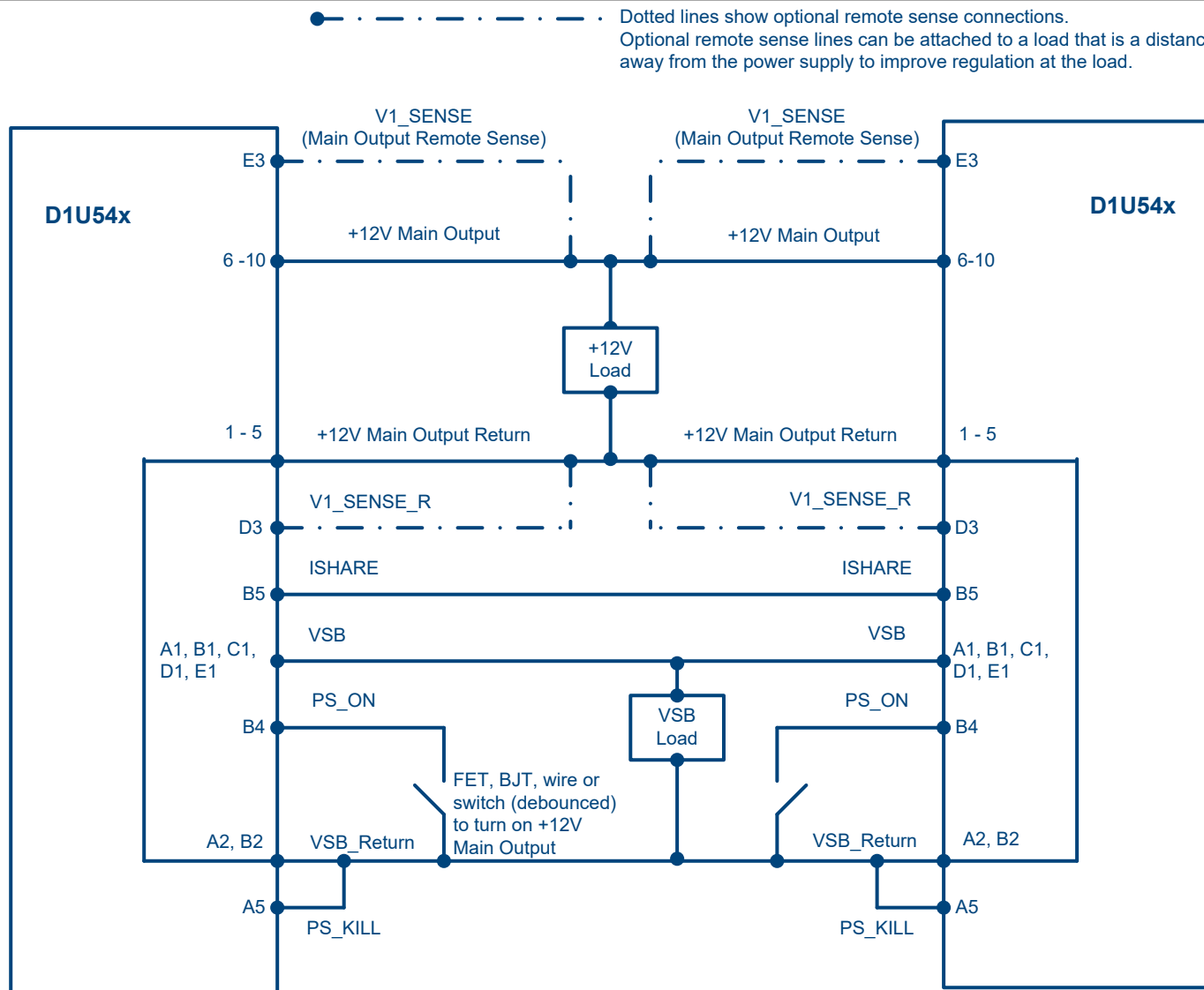
Etlin Daniels 8-NK4

DIMENSIONS					NON-INSULATED			NYLON INSULATED		
STUD SIZE	TONGUE WIDTH (W)		STUD CLEAR (F)		BRAZED SEAM	LENGTH (L)		WITH TIN PLATED COPPER SLEEVE	LENGTH (L)	
(d2)	in	mm	in	mm	PART NUMBER	in	mm	PART NUMBER	in	mm
#8	0.35	8.6	0.22	5.4	8-NK4	0.65	15.9	FN8-NK4	1.15	28.2
#8	0.47	11.5	0.36	8.8	8-S4	0.93	22.8	FN8-S4	1.35	33.1
#10	0.35	8.6	0.22	5.4	8-NK5	0.65	15.9	FN8-NK5	1.15	28.2
#10	0.47	11.5	0.36	8.8	8-S5	0.93	22.8	FN8-S5	1.35	33.1
1/4"	0.47	11.5	0.36	8.8	8-S6	0.93	22.8	FN8-S6	1.58	38.7
5/16"	0.59	14.5	0.54	13.2	8-8	1.17	28.7	FN8-8	1.58	38.7
3/8"	0.59	14.5	0.54	13.2	8-9	1.17	28.7	FN8-9	1.58	38.7
1/2"	0.78	19.1	0.59	14.5	8-13	1.32	38.5	FN8-13	1.73	42.4



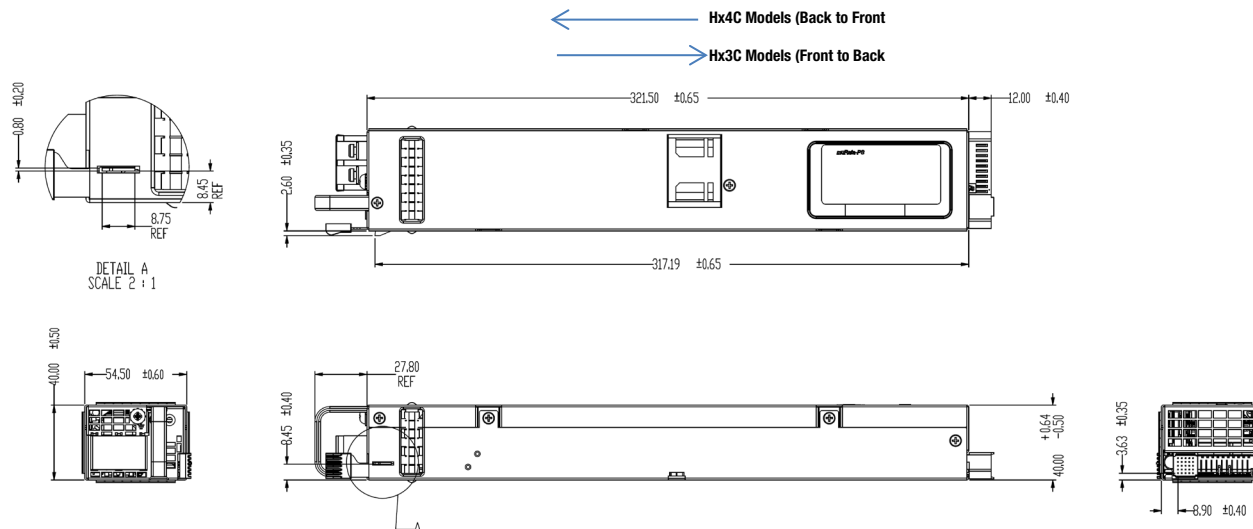
¹Wire selection for the DC source to power converter input terminal is dependent upon several factors that may vary with each deployment location, application to application. Factors that should be considered by end user when selecting the wire include the distance from power converter module to DC source (impacts voltage drop and therefore gauge), strand count, and insulation requirements including material or type, temperature and voltage ratings, and applicable local safety standards. The ring terminal options listed above are intended to provide a helpful starting point for the end user / system designer in selecting the wire that best meets the needs of each application, and any applicable local safety requirements.

WIRING DIAGRAM



1. Main 12VDC Output: Active share bus. The ISHARE bus (Pin B5 or D4) must be connected on all sharing modules. It is not required that the SENSE signals are connected to the remote load for current share to operate correctly.
2. Up to eight (8) power modules can be connected in parallel (non-redundant) or N+1 configuration. The current share bus is bi-directional (can source or sink current from the ISHARE bus).
3. The voltage of the bus would measure approximately 8VDC for a single power module at 100% load; for two (2) modules sharing a common load the ISHARE bus voltage would be approximately 4V for a perfect 50/50 current share scenario.
4. The VSB (Standby Output) output of the power module can also be connected in parallel; internal output isolation devices are provided however the combined available power is limited to that available from a single power module (3.3V @ 13.2W or 5V @ 20W; 12V @ 30W) irrespective of the number of modules connected in parallel.
5. The maximum output current during power-up should not exceed that of a single unit during power up. After PWOK signal is driven high the load can be increased.

MECHANICAL DIMENSIONS



1. This drawing is only for mechanical dimensions; a graphic representation of actual product and may not show all fine details, patterns, colours such as screw face pattern, fan surface detail.
2. The M4 pan head screw connection (located above terminal block) intended for host/System EMI connection.
3. Reference File: D1U54-D-1500_SPEC, 7/22/2019

OPTIONAL ACCESSORIES

Description	Part Number
D1U54P-12-CONC Output Interface Connector Card	D1U54P-12-CONC

APPLICATION NOTES

Document Number	Description	Link
ACAN-64	D1U54P-12-CONC Output Interface Connector Card	URL Link to the document
ACAN-67	D1U54-D-12 Communications Protocol	URL Link to the document

Murata Power Solutions, Inc.
129 Flanders Rd. Westborough,
Ma 01581, USA.
ISO 9001 and 14001 REGISTERED



This product is subject to the following operating requirements and the Life and Safety Critical Application Sales Policy: Refer to: <https://www.murata-ps.com/requirements/>

Murata Power Solutions, Inc. makes no representation that the use of its products in the circuits described herein, or the use of other technical information contained herein, will not infringe upon existing or future patent rights. The descriptions contained herein do not imply the granting of licenses to make, use, or sell equipment constructed in accordance therewith. Specifications are subject to change without notice.

©2021 Murata Power Solutions, Inc.