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Data Sheet

SCR2200-D13
Single axis gyroscope with digital SPI interface

Features

- ±125°/s Z-axis angular rate measurement range
- −40°C…+125°C operating range
- 3.0V…3.6V supply voltage
- SPI digital interface
- Extensive self diagnostics features
- Size 15.0 x 8.5 x 4.3 mm (l × w × h)
- Qualified according to AEC-Q100 standard
- RoHS compliant robust SOIC plastic package suitable for lead free soldering process and SMD mounting
- ISO26262 compliant, ASIL-B
- Proven capacitive 3D-MEMS technology

Applications

SCR2200-D13 is targeted at applications demanding high stability with tough environmental requirements. Typical applications include:

- Electronic Stability Control (ESC)
- Navigation
- Motion and position measurements
- Platform stabilization
- Inertial Measurement Units (IMUs) for highly demanding environments

Overview

The SCR2200-D13 is a high performance Z-axis angular rate sensor component. Angular rate sensor is based on Murata's proven capacitive 3D-MEMS technology. Signal processing is done in mixed signal ASIC that provides angular rate output via flexible SPI digital interface. Sensor element and ASIC are packaged to 24 pin premolded plastic housing that guarantees reliable operation over product's lifetime.

The SCR2200-D13 is designed, manufactured and tested for high stability, reliability and quality requirements. The component has extremely stable output over wide range of temperature, humidity and vibration. It is qualified according to AEC-Q100 standard and has several advanced self diagnostics features. The component is suitable for SMD mounting and is compatible with RoHS and ELV directives.

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1 Introduction

This document contains essential technical information about the SCR2200-D13 sensor including specifications, SPI interface descriptions, user accessible register details, electrical properties and application information. This document should be used as a reference when designing in SCR2200-D13 component.

2 Specifications

Table 1, Table 2, and Table 3 specifies the performance of SCR2200-D13 component. Critical Characteristics (CC) and Significant Characteristics (SC) are noted for each applicable parameter.

2.1 Definition of Critical Characteristics

Product or process characteristics which affect regulatory compliance or safe product function. Even a small exceeding of the tolerances is safety critical. Process capabilities must be continuously monitored. If the process is not capable enough (CPK < 2.0), 100% measurement or inspection must be applied.

2.2 Definition of Significant Characteristics

Product or process characteristics where reduction in variation within the specification tolerance is in manufacturers own interest or affects significantly customer satisfaction. The product or process characteristics are not, however, safety critical, unless the tolerances are exceeded significantly. Process capabilities must be continuously monitored. If the process is not capable enough (CPK 1.67), 100% measurement or inspection must be applied.

2.3 Abbreviations

ASIC	Application Specific Integrated Circuit
SPI	Serial Peripheral Interface
RT	Room Temperature
DPS	Degrees per second
FS	Full scale
CSB	Chip Select
SCK	Serial Clock
MOSI	Master Out Slave In
MISO	Master In Slave Out
MCU	Microcontroller

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2.4 General Specifications

General specifications for SCR2200-D13 component are presented in Table 1. All analog voltages are related to the potential at AVSS and all digital voltages are related to the potential at DVSS.

Table 1. General specifications.

Parameter	Condition		Min	Typ	Max	Unit
Analog supply voltage: AVDD			3.0	3.3	3.6	V
Analog supply current: I_AVDD	Temperature range -40 ... +125 °C	CC		15.2	18	mA
Digital supply voltage: DVDD			3.0	3.3	3.6	V
Digital supply current: I_DVDD	Temperature range -40 ... +125 °C	CC		3.3	4.5	mA
Boost supply voltage (optional)	Option to reduce current consumption (by 2mA) with 5V Vin_Boost input voltage, see section 7.1 for more details.		4.5	5	5.5	V
Boost supply current: I_L1 (current through inductor L1, see Figure 15)	VBOOST = 20V Vin_Boost = 3.3V, L1 = 47µH Mean value Peak value, T < 1µs Max. value during startup (T≤0.4ms)			4.5	6.5 110 60	mA mA mA
	VBOOST = 20V Optional Vin_Boost = 5.0V, L1=100µH Mean value Peak value, T < 1µs Max. value during startup (T≤0.4ms)				6 70 75	mA mA mA
Total current, I_TOTAL	I_AVDD + I_DVDD + I_L1			22	29	mA
Total current reset	Total average current during reset				5	mA
Rise/fall time: AVDD, DVDD, Vin_Boost (see Figure 15)					200	ms
Output update rate	Gyro Temperature sensor			F_prim/4 F_prim/64		Hz Hz
POR_TH_H	Threshold of Power On Reset (POR) for rising AVDD and DVDD		2.7	2.8	2.9	V
POR_TH_L	Threshold of Power On Reset (POR) for falling AVDD and DVDD		2.5	2.6	2.8	V
TRESD_r	For rising supply voltages and rising EXTRESN input signal Delay time if all reset levels are above their thresholds. Applies also for SPI HardReset command.		15		20	ms
SPI start-up time					25	ms

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2.5 Performance Specifications for Gyroscope

Table 2. Gyro performance specifications (VDD = 3.3 V, room temperature and ODR=2.3kHz unless otherwise specified).

Parameter	Condition		Min	Typ	Max	Unit
Operating range	Measurement axis Z		-125		125	°/s
Total offset error A)	-40 °C ... +125 °C	CC	-1.3		1.3	°/s
Offset drift over temperature B)	-40 °C ... +125 °C		0		0.6	°/s
Offset drift velocity	2.5K /min		-0.1		0.1	°/s /min
Sensitivity C)				50		LSB/°/s
Total sensitivity error A)	-40 °C ... +125 °C	CC	-3		3	%
Linearity error D)	-40 °C ... +125 °C		-0.5		0.5	°/s
Microlinearity E)	Step width ≥2.5°/s		-5		5	%
Noise (RMS)	10Hz filter, -40 °C ... +125 °C				0.12	°/s
	60Hz filter, -40 °C ... +125 °C				0.2	°/s
Cross-axis sensitivity F)		SC			1.7	%
Amplitude response −3 dB frequency	10Hz filter			10		Hz
	60Hz filter			60		Hz
Power on start-up time	10Hz filter				750	ms
	60Hz filter				620	ms
Recommended ODR G)				2300		Hz
F_prim	Nominal operation frequency of the sensor element. All ASIC internal clocks are derived from a multiple of this frequency	CC	7	8	9	kHz
Output update rate	Gyroscope			F_prim/4		Hz
Mechanical Range (Headroom)			-30000		30000	°/s
Electrical Dynamic Range (Headroom)	Output signal		-655		655	°/s
G sensitivity(1g x,y,z axis)	For DC gravity input				0.2	(°/s)/G

A) Includes error from calibration, temperature, supply voltage and drift over lifetime.

B) Offset drift over temperature is determined by ((maximum offset value over temperature) - (minimum offset value over temperature)) / 2.

C) Sensitivity is defined as

$$Sensitivity = \frac{AR_{meas}(\Omega_{max}) - AR_{meas}(\Omega_{min})}{\Omega_{max} - \Omega_{min}}$$

Where

Ω_{max}=applied angular rate at maximum operating range

Ω_{min}=applied angular rate at minimum operating range

$AR_{meas}(\Omega_n)$=measured angular rate at Ω_n [LSB]

D) Linearity is the maximum deviation from the straight line defined by the measured values at the operating range end points.

E) Microlinearity is defined as follows: The transfer function is measured over the whole operating range in angular rate steps of a predefined step width. The deviation of the gradient between two neighboring points to the measured scale factor must not exceed the specified limits.

$$Microlinearity = \left(\frac{AR_{meas}(\Omega_{(n+1)}) - AR_{meas}(\Omega_n)}{stepwidth} - 1 \right) \times 100\%$$

Where

Ω_n=applied angular rate (Ω_{n+1} ≤max. operating range)

$AR_{meas}(\Omega_n)$=measured angular rate at Ω_n [°/s]

F) Cross axis sensitivity is the ratio between the sensitivity of the sensing axis and the two orthogonal axes.

$$Cross-axis(X) = \frac{Sensitivity(X)}{Sensitivity(Z)} \times 100\% \; ; \; Cross-axis(Y) = \frac{Sensitivity(Y)}{Sensitivity(Z)} \times 100\%$$

Where

Sensitivity(X)= Sensitivity when angular rate is applied in X direction

Sensitivity(Y)= Sensitivity when angular rate is applied in Y direction

Sensitivity(Z)= Sensitivity when angular rate is applied in Z direction

G) ODR = Output Data Rate, see section 5.1.7 for more details.

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2.6 Performance Specification for Temperature Sensor

Table 3. Temperature sensor performance specifications.

Parameter	Condition	Min.	Typ	Max.	Unit
Temperature signal range		-50		+150	°C
Temperature signal sensitivity	Temperature sensor output in 2's complement format		14.5		LSB/°C
Output update rate	Temperature sensor		F_prim/ 64		

Temperature is converted to °C with following equation:

$$\text{Temperature [°C]} = 60 + (\text{TEMP} / 14.5),$$

where TEMP is temperature sensor output register content in decimal format.

2.7 Absolute Maximum Ratings

Within the maximum ratings (Table 4), no damage to the component shall occur. Parametric values may deviate from specification, yet no functional deviation shall occur. All analog voltages are related to the potential at AVSS, all digital voltages are related to DVSS.

Table 4. Absolute maximum ratings.

Parameter	Remark	Min.	Typ	Max.	Unit
AVDD	Supply voltage analog circuitry	-0.3		4.3	V
DVDD	Supply voltage digital circuitry	-0.3		4.3	V
AIN/AOUT	Maximum voltage at analog input and output pins	-0.3		2.1	V
DIN/DOUT	Maximum voltage at digital input and output pins	-0.3		DVDD+0.3	V
TESTIN / TESTOUT	Maximum voltage at pins	-0.3		2.1	V
VBoost, LBoost	Maximum voltage at high voltage input and output pins	-0.3		40	V
Topr	Operating temperature range	-40		125	°C
Tstg	Storage temperature range	-40		150	°C
ESD_HBM	ESD according Human Body Model (HBM), Q100-002	±2000			V
ESD_MM	ESD according Machine Model (MM), Q100-003	±200			V
ESD_CDM	ESD according Charged Device Model (CDM), Q100-011	±500 ±750 (corner pins)			V
US	Ultrasonic agitation (cleaning, welding, etc)	Prohibited			

2.8 Pin Description

The pinout for SCR2200-D13 is presented in Figure 1, while the pin descriptions can be found in Table 5.

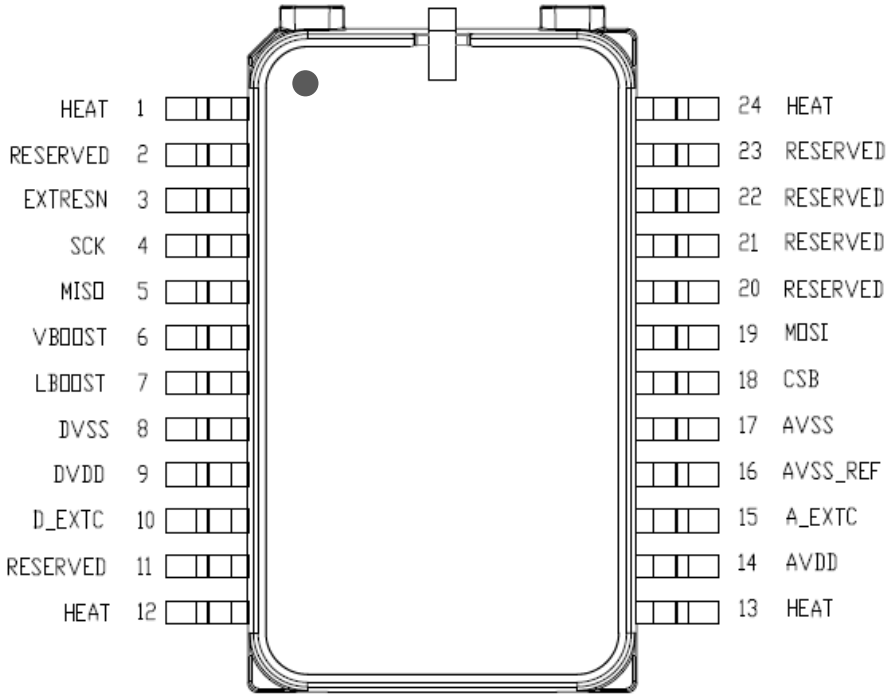

Figure 1. Pinout for SCR2200-D13.

Table 5. SCR2200-D13 pin descriptions.

Pin#	Name	Type	Description
1, 12, 13, 24	HEAT	-	Heat sink connection, connect externally to AVSS
2	RESERVED	-	Factory use only, leave floating
3	EXTRESN	DIN	External Reset, 3.3V logic compatible Schmitt-trigger input with internal pull-up, LOW-HIGH transition causes system restart. Minimum low time 100us.
4	SCK	DIN	CLK signal of SPI Interface
5	MISO	DOUT	Data Out of SPI Interface
6	VBOOST	AOUT_HV	External capacitor connection for high voltage analog supply, high voltage pad ≈20V
7	LBOOST	AIN_HV	Connection for inductor for high voltage generation, high voltage pad ≈20V
8	DVSS	GND	Digital Supply Return, connect externally to AVSS
9	DVDD	SUPPLY	Digital Supply Voltage
10	D_EXTC	AOUT	External capacitor connection for digital core (typ. 1.8V)
11	RESERVED	-	Factory use only, leave floating
14	AVDD	SUPPLY	Analog Supply voltage
15	A_EXTC	AOUT	External capacitor connection for positive reference voltage
16	AVSS_REF	GND	Analog reference ground, connect externally to AVSS
17	AVSS	GND	Analog Supply Return, connect externally to DVSS
18	CSB	DIN	Chip Select of SPI Interface, 3.3V logic compatible Schmitt-trigger input
19	MOSI	DIN	Data In of SPI Interface, 3.3V logic compatible Schmitt-trigger input
20	RESERVED	TESTIN	Factory use only, connect to GND or leave floating
21	RESERVED	TESTIN	Factory use only, connect to GND or leave floating
22	RESERVED	TESTOUT	Factory use only, leave floating
23	RESERVED	TESTOUT	Factory use only, leave floating

2.9 Digital I/O Specification

Table 6 describes the DC characteristics of SCR2200-D13 sensor SPI I/O pins. Supply voltage is 3.3 V unless otherwise specified. Current flowing into the circuit has a positive value.

Table 6. SPI DC characteristics.

Symbol	Description	Min.	Nom.	Max.	Unit
Serial Clock SCLK					
VinHigh	Input high voltage	2		DVDD+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.3			V
Ileak	Input leakage current, 0V ≤ Vin ≤ DVDD	-1		1	µA
Cin	Input capacitance			15	pF

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Symbol	Description	Min.	Nom.	Max.	Unit
Chip select CSB (Pull Up), low active					
VinHigh	Input high voltage	2		DVDD+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.3			V
Isource	Input current source (Pull Up), Vin = 0V	10		60	µA
Cin	Input capacitance			15	pF
Vin_open	Open circuit output voltage	2			V
Serial data input MOSI (Pull Down)					
VinHigh	Input high voltage	2		DVDD+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.3			V
Isource	Input current source (Pull Up), Vin = DVDD	10		60	µA
Cin	Input capacitance			15	pF
Vin_open	Open circuit output voltage			0.3	V
Serial data output MISO (Tri state)					
VoutHigh_-1mA	Output high voltage, Iout = -1mA	DVDD-0.5			V
VoutHigh_-50µA	Output high voltage, Iout = -50µA	DVDD-0.2			V
VinHigh_1mA	Output low voltage, Iout = +1mA			0.55	V
VinHigh_50µA	Output low voltage, Iout = +50µA			0.3	V
Iout_Hz	High impedance output current, 0V < VMISO < DVDD	-1		1	µA
Cld_miso	Capacitive load. The slope of the MISO output signal may need to be controlled to meet EMI requirements under specified load conditions.			200	pF

Table 7. EXTRESN pin characteristics.

Symbol	Description	Min.	Nom.	Max.	Unit
Digital pin EXTRESN					
VinHigh	Input high voltage	2		DVDD+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.3			V
Isource	Start-up indication phase inactive Start-up indication phase active	10 10		80 60	µA µA
ΔISource	Pull up current reduction during Start-up indication	5		40	µA
Tstind	Duration start-up indication phase Note: StartUp indication starts with StateMon changing to 00h.		1		ms

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2.10 SPI AC Characteristics

The AC characteristics of SCR2200-D13 are defined in Figure 2 and Table 8.

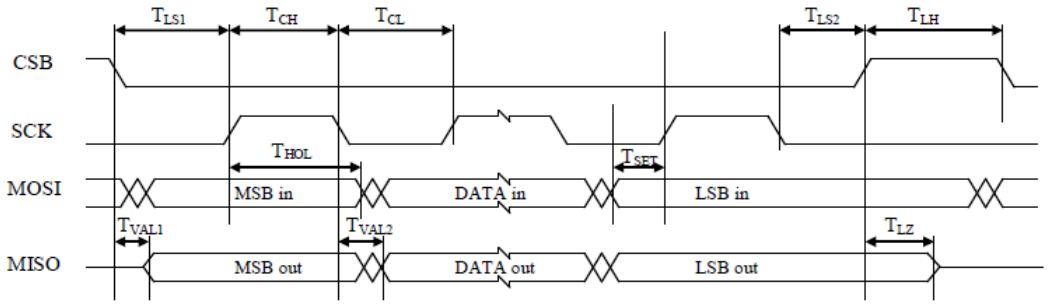

Figure 2. Timing diagram of SPI communication.

Table 8. SPI AC electrical characteristics.

Symbol	Description	Min.	Nom.	Max.	Unit
F_{SPI}	It is recommended to use maximum SCK frequency, see section 5.1.7 for more details.	0.1		8	MHz
T_{SPI}			$1/F_{SPI}$		
T_{CH}	High time: duration of logical high level at SCLK	45	$T_{SPI}/2$		ns
T_{CL}	Low time: duration of logical low level at SCLK	45	$T_{SPI}/2$		ns
T_{LS1}	Setup time CSB: time between the falling edge of CSB and the rising edge of SCLK	45	$T_{SPI}/2$		ns
T_{VAL1}	Delay time: time delay from the falling edge of CSB to data valid at MISO			30	ns
T_{SET}	Setup time at MOSI: setup time of MOSI before the rising edge of SCLK	15			ns
T_{HOL}	MOSI data hold time	30			ns
T_{VAL2}	Delay time: time delay from falling edge of SCLK to data valid at MISO			30	ns
T_{LS2}	Hold time of CSB: time between the falling edge of SCLK and the rising edge of CSB	45	$T_{SPI}/2$		ns
T_{LZ}	Tri-state delay time: time between the rising edge of CSB to MISO in Tri-state			15	ns
T_{LH}	Time between SPI cycles: minimum high time of CSB between two consecutive transfers	172			ns

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2.11 Measurement Axis and Directions

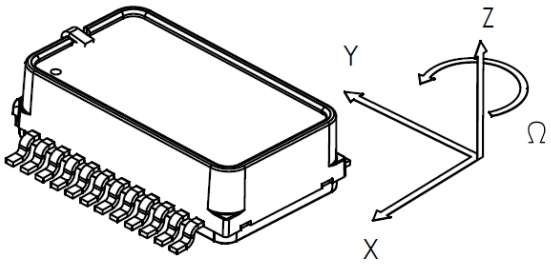

Figure 3. SCR2200-D13 measurement directions.

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2.12 Package Characteristics

2.12.1 Package Outline Drawing

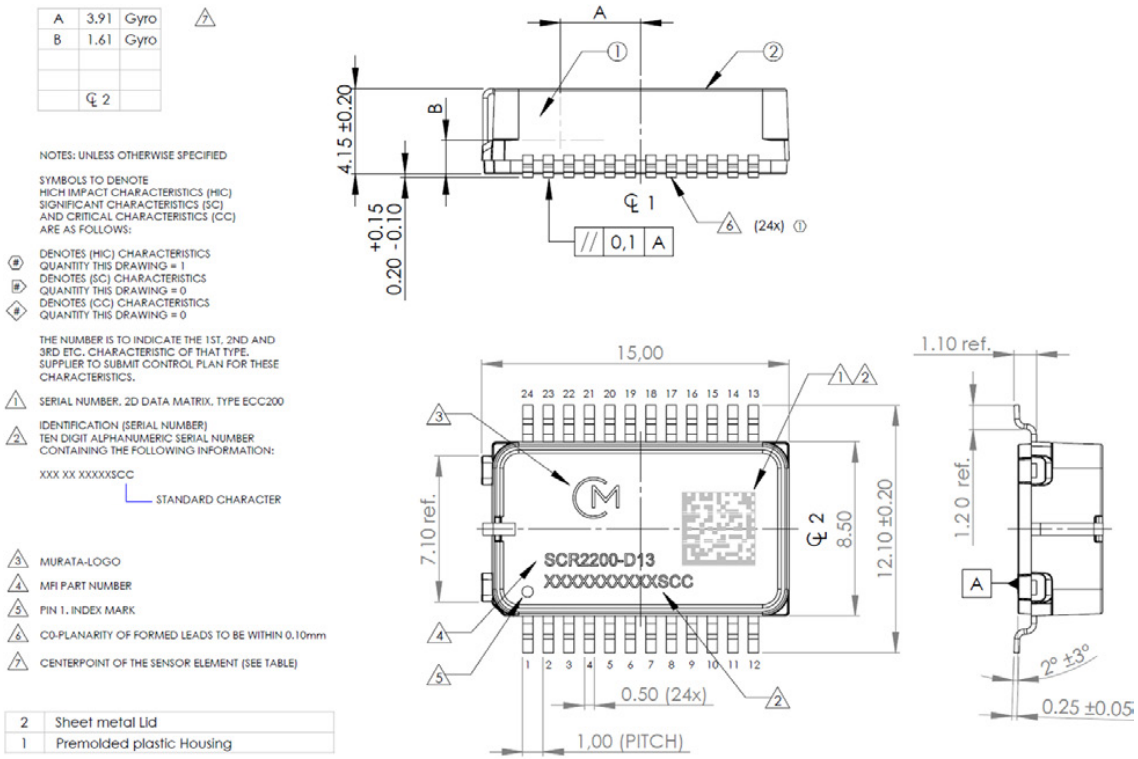

Figure 4. Package outline. The tolerances are according to ISO2768-f (see Table 9).

Table 9. Limits for linear measures (ISO2768-f).

Tolerance class	Limits in mm for nominal size in mm			
	0.5 to 3	Above 3 to 6	Above 6 to 30	Above 30 to 120
f (fine)	±0.05	±0.05	±0.1	±0.15

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2.13 PCB Footprint

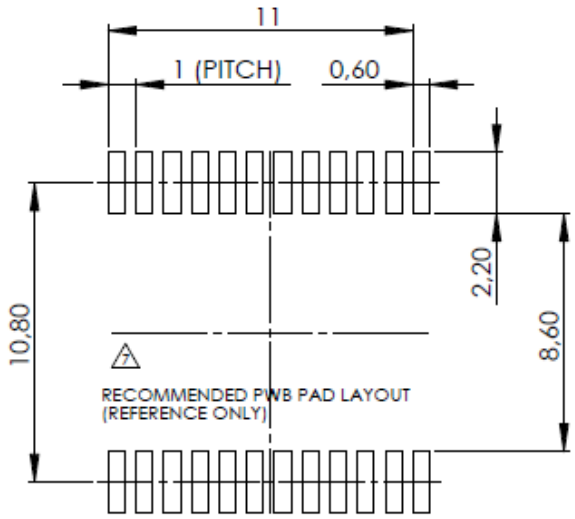

Figure 5. Recommended PWB pad layout for SCR2200-D13. The tolerances are according to ISO2768-f (see Table 9).

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3 General Product Description

3.1 Component block diagram

The SCR2200-D13 sensor consists of angular rate sensing element and Application-Specific Integrated Circuit (ASIC) used to sense and control the gyro element. SCR2200-D13 utilizes the same ASIC as Murata's other high performance gyro accelerometer combo products (SCC2000 series). With SCR2200-D13 the ASIC's the accelerometer functionality is powered down. Figure 6 contains an upper level block diagram of the component. The ASIC provides SPI interface used to control and read the gyroscope.

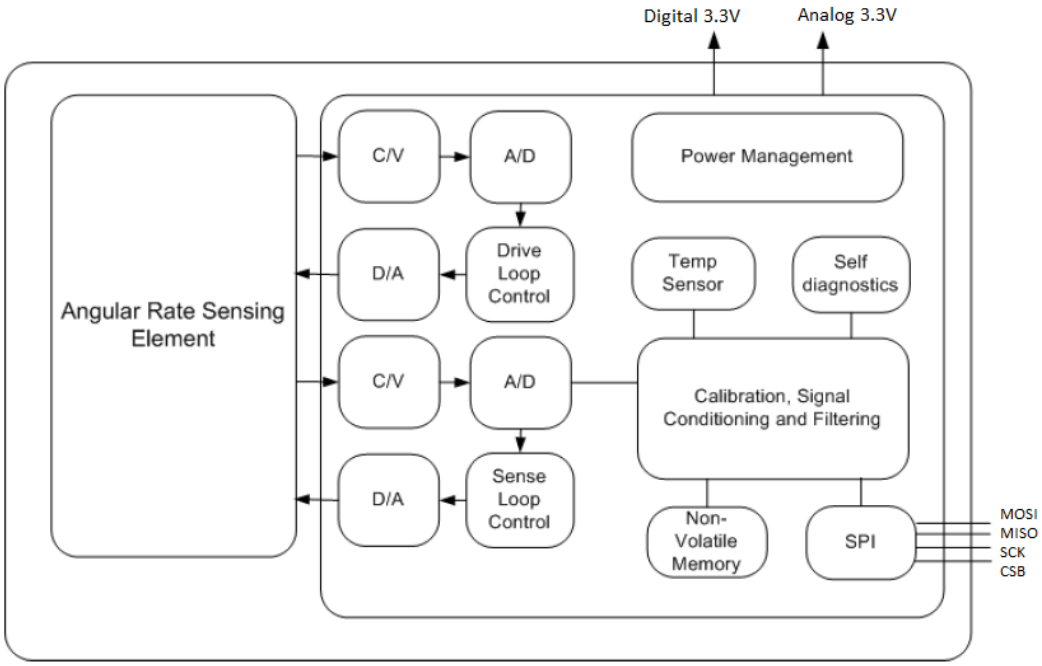

Figure 6. SCR2200-D13 component block diagram.

The angular rate sensing element is manufactured using Murata proprietary High Aspect Ratio (HAR) 3D-MEMS process, which enables making robust, extremely stable and low noise capacitive sensors.

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3.2 Angular rate sensing element

The angular rate sensing (Figure 7) element consists of moving masses that are purposely exited to in-plane drive motion. Rotation in sensitive direction causes in-plane movement that can be measured as capacitance change with the signal conditioning ASIC.

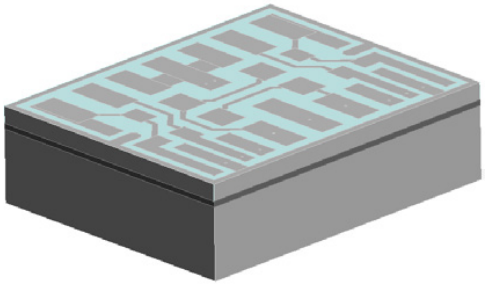

Figure 7. Angular rate sensing element.

3.3 Factory Calibration

SCR2200-D13 sensors are factory calibrated. No separate calibration is required in the application. Gyroscope offset and sensitivity parameters are trimmed during production. Fail safe monitoring signals are also calibrated. Parameters are calibrated with 2nd order polynomial at -40°C, +25°C and +125°C. Calibration parameters are stored to non-volatile memory during manufacturing. The parameters are read automatically from the internal non-volatile memory during the start-up.

It should be noted that assembly can cause minor offset/bias errors to the sensor output. If best possible offset/bias accuracy is required, system level offset/bias calibration (zeroing) after assembly is recommended.

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4 Component Operation, Reset and Power Up

4.1 Component Operation

The SCR2200-D13 component has internal power-on reset circuit. It releases the internal reset-signal once the power supplies are within the specified range. After the reset, the sensor performs an internal startup sequence. During the startup sequence SCR2200-D13 reads configuration and calibration data from the non-volatile memory to volatile registers. 620ms after the power on or reset, sensor shall be able to provide valid angular rate data, separate measurement mode activation is not needed.

SCR2200-D13 sensor uses 60Hz low pass filter setting by default. In case the optional 10Hz low pass filter is used the filter setting can be set by writing the FLT bits to 01b in Status Summary register. See section 6.2.9 for more information on Status Summary register. Section 5.1.4 shows full SPI write frames for filter settings.

SCR2200-D13 component has extensive internal failsafe diagnostics to detect over range and possible internal failures. If the internal failsafe diagnostics is used it should be enabled by clearing the status registers during component power up by following the sequence shown in section 4.2 (Figure 8).

4.2 Reset and Power Up Sequence For Enabling Internal Failsafe Diagnostics

Reset and power up sequence for enabling component internal failsafe diagnostics is shown below in Figure 8. After the reset, the sensor performs an internal startup sequence. 25ms after the reset, the SPI bus becomes accessible and the output filter can be set to a desired value. If the filter is not set to a valid value (60Hz or 10Hz setting), the default setting (00b = 60Hz) is used and the S_OK_C flag in Status Summary Register will indicate a failure. In 750ms (10Hz filter setting) or in 620ms (60Hz filter selection) the gyro shall be able to deliver valid data.

If external reset is used during start-up, the EXTRESN pin must be pulled low in 50ms after power on to avoid gyroscope oscillation and possibility to skip self-test (Figure 8). The possibility for skipping the self-test occurs, if gyro oscillation has exceeded the internal threshold value.

During the startup sequence the sensor performs a series of internal tests that will set various error flags in the sensor status registers and to clear them it is necessary to read all status registers after the startup sequence is complete.

Once startup sequence is completed, normal operation is indicated with Status Summary register content of 0041h. In case of failure Common Status register is read, then sensor should be reset and re-started. Number of reset retries depends on application requirements but max 1 repeat cycle is the recommendation in general.

After startup sequence completion the SPI frame Return Status bits (RS bits) indicate sensor operation status, for more information on the Return Status bits, please see section 5.1.5.

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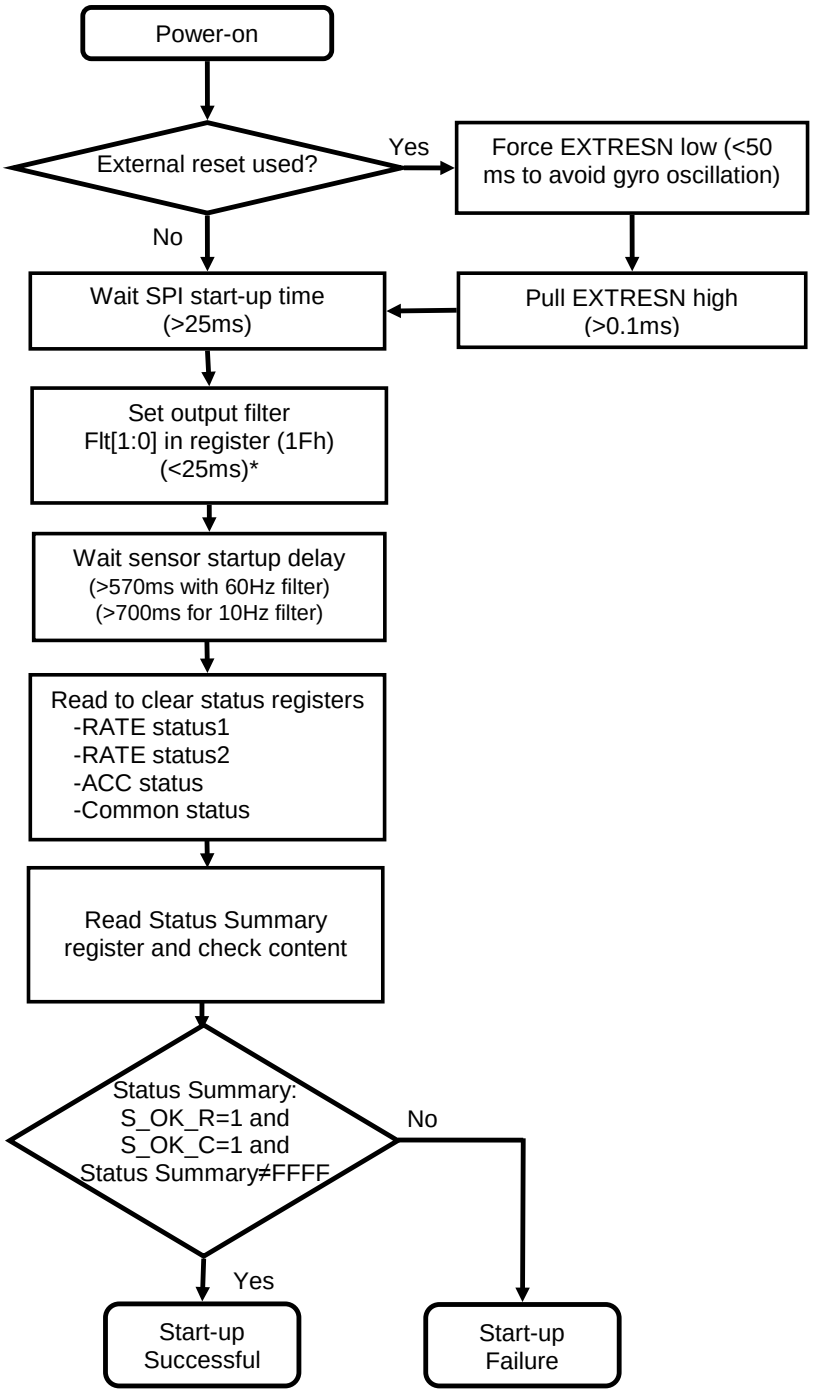

Figure 8. Reset and power up sequence for enabling internal failsafe diagnostics. Timing from previous step indicated.

* Depending on actual application implementation (HW-layout, SPI transitions, detailed SPI Timing) it may occur that in case of SPI traffic within the time period of 50... 280ms after RESET, the PLL does not lock. If possible SPI traffic during this time frame shall be prevented or at least reduced to a minimum.

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5 Component Interfacing

5.1 SPI Interface

5.1.1 General

The SCR2200-D13 has SPI interface for the angular rate sensor. SPI communication transfers data between the SPI master and registers of the SCR2200-D13 ASIC. The SCR2200-D13 always operates as a slave device in master-slave operation mode. 3-wire SPI connection cannot be used.

SPI interface pins:

CSB	Chip Select (active low)	MCU → ASIC
SCK	Serial Clock	MCU → ASIC
MOSI	Master Out Slave In	MCU → ASIC
MISO	Master In Slave Out	ASIC → MCU

5.1.2 Protocol

SPI communication uses off-frame protocol so each transfer has two phases.

The first phase contains the SPI command (Request) and the data (Response) of the previous command. The second phase contains the next Request and the Response to the Request of the first phase, see Figure 9.

Data word length is 32 bits, the data is transferred MSB first. The first response after reset is undefined and shall be discarded.

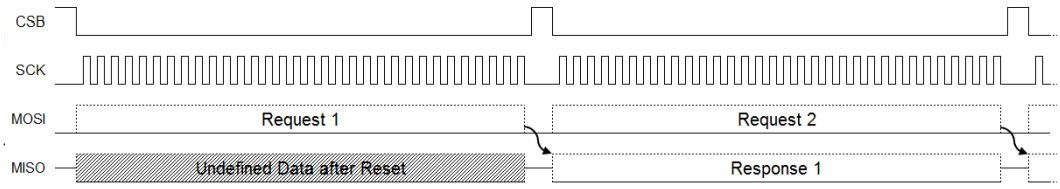

Figure 9. SPI protocol example.

The interleaved Request - Response cycle then continues as shown in Figure 10.

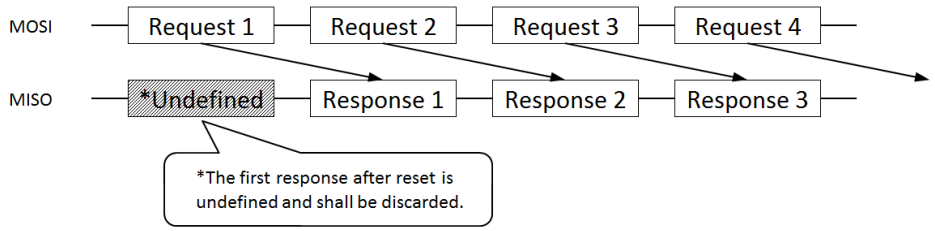

Figure 10. Request – Response frame relationship.

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The SPI transmission is always started with the CSB falling edge and terminated with the CSB rising edge. The data is captured on the SCK's rising edge (MOSI line) and it is propagated on the SCK's falling edge (MISO line). This equals to SPI Mode 0 (CPOL = 0 and CPHA = 0), see Figure 11.

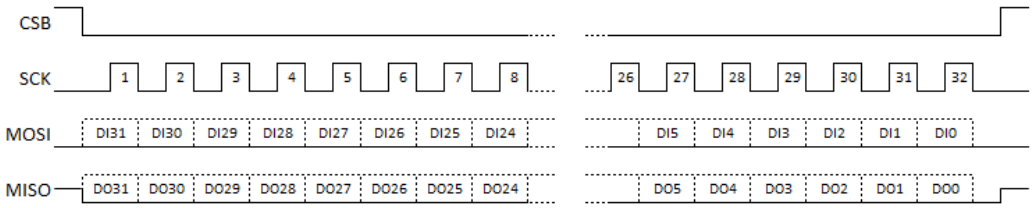

Figure 11. SPI Frame Format.

5.1.3 General Instruction format

The SPI frame is divided into four parts (See Figure 12 and Table 10):

1. Operation Code (OP)
2. Return status (RS, in MISO)
3. Data (DI, DO)
4. Checksum (CRC)

Unused bits shall be set to 0, this is important for the checksum calculation.

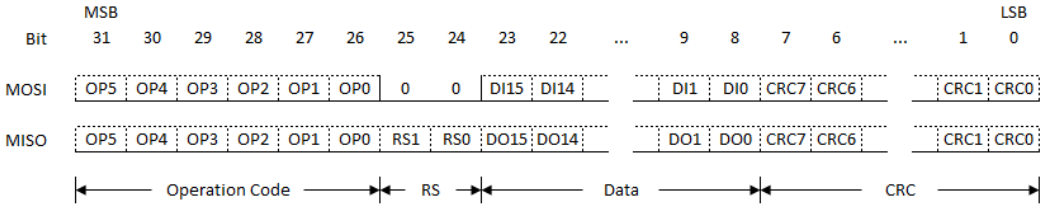

Figure 12. SPI instruction format.

Table 10. SPI bit definitions.

Bits	Name	MOSI	MISO
OP[5:0]	Operation code	Requested operation: • OP5: Write =1 / Read = 0 • OP[4:0] = Register address	Performed operation: • OP5: Write = 1 / Read = 0 • OP[4:0] = Register address
RS[1:0]	Return status	n.a.	Sensor status
D[15:0]	Data	Data to be written	Return data
CR[7:0]	Checksum	Checksum of MOSI bits [31:8]	Checksum of MISO bits [31:8]

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5.1.4 Operations

Table 11. Operations and their equivalent SPI frames.

Operation	Register	SPI Frame Binary (OP, RS, Data, CRC)	SPI Frame Hex
Read RATE	RATE (01h)	000001 00 0000000000000000 11110111	040000F7h
Read TEMP	TEMP (07h)	000111 00 0000000000000000 11100011	1C0000E3h
Read RATE Status 1	RATE Status 1 (09h)	001001 00 0000000000000000 11000111	240000C7h
Read RATE Status 2	RATE Status 2 (0Ah)	001010 00 0000000000000000 11001101	280000CDh
Read ACC Status	ACC Status (0Fh)	001111 00 0000000000000000 11010011	3C0000D3h
Write Reset Control HardReset	Reset Control (16h)	110110 00 0000000000000100 00110001	D8000431h
Write Reset Control MonitorST	Reset Control (16h)	110110 00 0000000000001000 10101101	D80008ADh
Read Serial ID0	Serial ID0 (18h)	011000 00 0000000000000000 10100001	600000A1h
Read Serial ID1	Serial ID0 (19h)	011001 00 0000000000000000 10100111	640000A7h
Read Common Status	Common Status (1Bh)	011011 00 0000000000000000 10101011	6C0000ABh
Read Status Summary	Status Summary (1Fh)	011111 00 0000000000000000 10110011	7C0000B3h
Write Flt[1:0] =10b	Status Summary (1Fh)	111111 00 0010000000000000 00000110	FC200006h
Write Flt[1:0] =01b	Status Summary (1Fh)	111111 00 0001000000000000 11000111	FC1000C7h

5.1.5 Return Status

SPI frame Return Status bits (RS bits) indicate the functional status of the sensor, see Return Status definitions in Table 12 and in Figure 13.

Table 12. Return Status definitions.

RS[1]	RS[0]	Description
0	0	Initialization running
0	1	Normal operation of selected channel
1	0	Selftest of selected channel
1	1	Reserved, not existing or acceleration related register addressed, error of selected channel or common failure (see Status Summary Register bits S_OK_C, S_OK_R, S_OK_A). • Reading ACC: o S_OK_A = 0 OR S_OK_C = 0 • Reading RATE: o S_OK_R = 0 OR S_OK_C = 0 • Read/Write others: o S_OK_R = 0 OR S_OK_A = 0 OR S_OK_C = 0 OR reserved or not existing register addressed

The priority of the return status states is from high to low: 10 → 00 → 11 → 01.

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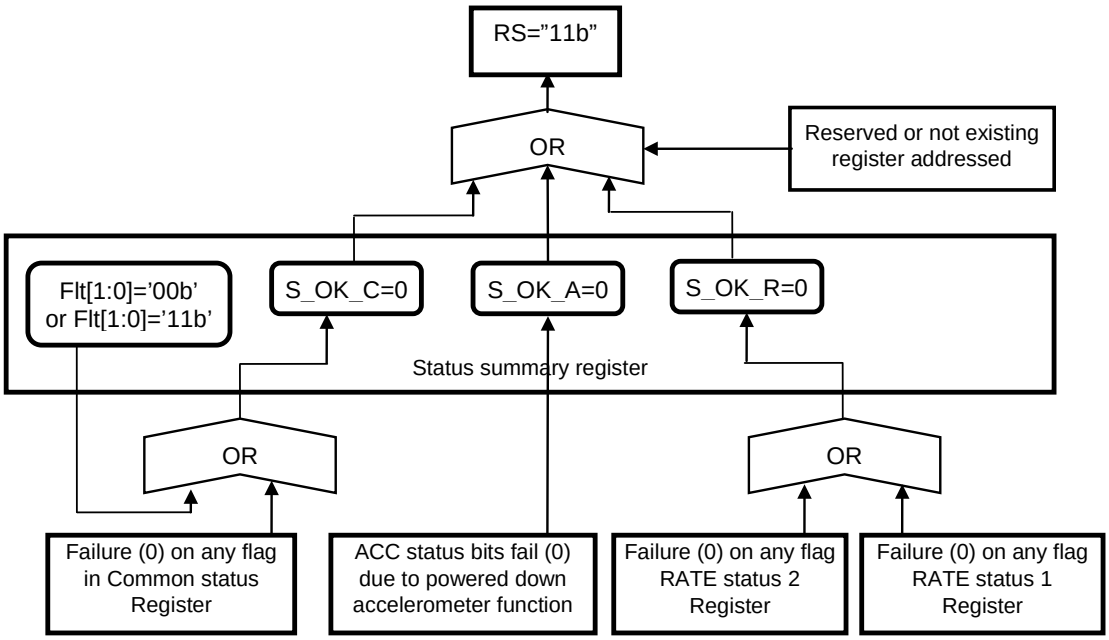

Figure 13. Return Status (RS) condition description.

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5.1.6 Checksum (CRC)

For SPI transmission error detection a Cyclic Redundancy Check (CRC) is implemented, for details see Table 13.

Table 13. SPI CRC definition.

Parameter	Value
Name	CRC-8
Width	8 bit
Poly	1Dh (generator polynom: X8+X4+X3+X2+1)
Init	FFh (initialization value)
XOR out	FFh (inversion of CRC result)

The CRC value used in system level software has to be initialized with FFh to ensure a CRC failure in case of stuck-at-0 and stuck-at-1 error on the SPI bus. C-programming language example for CRC calculation is presented in Figure 14. It can be used as is in an appropriate programming context.

```
// Calculate CRC for 24 MSB's of the 32 bit dword
// (8 LSB's are the CRC field and are not included in CRC calculation)
uint8_t CalculateCRC(uint32_t Data)
{
  uint8_t BitIndex;
  uint8_t BitValue;
  uint8_t CRC;

  CRC = 0xFF;
  for (BitIndex = 31; BitIndex > 7; BitIndex--)
  {
    BitValue = (uint8_t)((Data >> BitIndex) & 0x01);
    CRC = CRC8(BitValue, CRC);
  }
  CRC = (uint8_t)~CRC;
  return CRC;
}

static uint8_t CRC8(uint8_t BitValue, uint8_t CRC)
{
  uint8_t Temp;

  Temp = (uint8_t)(CRC & 0x80);
  if (BitValue == 0x01)
  {
    Temp ^= 0x80;
  }
  CRC <<= 1;
  if (Temp > 0)
  {
    CRC ^= 0x1D;
  }
  return CRC;
}
```

Figure 14. C-programming language example for CRC calculation.

CRC calculation example:
Read RATE register (01h) -> SPI[31:8] = 040000h -> CRC [7:0] -> F7h.
Further examples can be found in Table 11.

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5.1.7 Recommendation for the SPI interface implementation

All SPI communication activity (including other sensors connected to same SPI bus) may interfere with the measured angular rate signal due to sensor internal capacitive coupling. If the harmonic overtones of the SPI communication activity are close to gyro operational frequency, the SPI cross talk can be seen as increased noise level in angular rate signal.

Cross talk can be eliminated by choosing the output data rate (sample rate) in a suitable way, i.e. avoiding the overtones on the gyro operation frequency. For optimum performance it is recommended that 2.3kHz or 3.2kHz output data rate is used with maximum serial clock (SCK) frequency (8MHz). The design performance should be verified carefully.

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6 Register Definition

Table 14. Address space overview.

Reg (hex)	R/W	Register Name
00h	NA	Reserved
01h	R	RATE
02h	NA	Reserved
03h	NA	Reserved
04h	R	Reserved
05h	R	Reserved
06h	R	Reserved
07h	R	TEMP
08h	NA	Factory Use Only
09h	R	RATE Status 1
0Ah	R	RATE Status 2
0Bh	NA	Reserved
0Ch	NA	Reserved
0Dh	NA	Reserved
0Eh	NA	Reserved
0Fh	R	ACC Status
10h	NA	Reserved
11h	NA	Factory Use Only
12h	NA	Factory Use Only
13h	NA	Factory Use Only
14h	NA	Factory Use Only
15h	R/W	Test Register
16h	R/W	Reset Control
17h	NA	Factory Use Only
18h	R	Serial ID0
19h	R	Serial ID1
1Ah	NA	Reserved
1Bh	R	Common Status
1Ch	NA	Reserved
1Dh		Identification Register
1Eh	NA	Factory Use Only
1Fh	R/W	Status Summary

R/W operation to Reserved registers sets RS bits to ‘11’. Also acceleration output register read operation will result in to RS bit failure. However, R/W to Factory Use Only registers does not normally set RS bits to ‘11’. User should not access to Factory Use Only Registers. It should be noted that writing 1 to 17h D3 will freeze all sensor data. Thus, user should be careful not write to this register.

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6.1 Sensor Data Block

Table 15. Sensor data block.

Addr OP[4:0]	Bits	Register Name	No. of Bits	Read/ Write	Description
01h	[15:0]	RATE	16	R	Rate output in 2's complement format
04h	[15:0]	ACC_X	16	R	Reserved, accelerometer function is powered down
05h	[15:0]	ACC_Y	16	R	Reserved, accelerometer function is powered down
06h	[15:0]	ACC_Z	16	R	Reserved, accelerometer function is powered down
07h	[11:0]	TEMP	12	R	Temperature sensor output in 2's complement sign-extended format. See section 2.6 for temperature conversion example.

SPI read frames with CRC content for these registers are shown in Table 11.

6.1.1 Example of Angular Rate Data Conversion

For example, if RATE register read results: RATE = **05FFE08B**h, the register content is converted to angular rate as follows:

- 05h = 000001 01b
  - 000001b = operation code = Read RATE
  - 01b = return status (RS bits) = no error
- FFE0h = 1111 1111 1110 0000b = RATE register content
  - FFE0h in 2's complement format = -32d
  - Angular rate = -32LSB / sensitivity = -32LSB / (50LSB/(°/s)) = -0.64°/s
- 8Bh = CRC of 05FFE0h

6.1.2 Example of Temperature Data Conversion

For example, if TEMP register read results: TEMP = **1DFE6F4E**h, the register content is converted to temperature as follows:

- 1Dh = bin 000111 01b
  - bin 000111b = operation code = Read TEMP
  - 01 = return status (RS bits) = no error
- FE6Fh = bin 1111 1110 0110 1111 = TEMP register content
  - FE6Fh in 2's complement format = -401d
  - Temperature = 60 + (TEMP / 14.5) = 60 + [-401/14.5] = +32.3°C
  - See section 2.6 for temperature conversion equation
- 4Eh = CRC of 1DFE6Fh

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6.2 Sensor Status Block

Table 16. Sensor status block.

Addr OP[4:0]	Bits	Register Name	No. of Bits	Read/ Write	Description
09h	[15:0]	RATE Status 1	16	R	Gyro sensor status
0Ah	[15:0]	RATE Status 2	16	R	Gyro sensor status
0Fh	[15:0]	ACC Status	16	R	Accelerometer status Note: accelerometer functionality is powered down, This register is read during sensor power up sequence, see more details in section 4.
15h	[15:0]	Test	16	R/W	R/W register for SPI communication checking
16h	[15:0]	Reset Control	16	R/W	Reset status and trigger bits
18h	[15:0]	Serial ID0	16	R	Component serial number least significant bits
19h	[15:0]	Serial ID1	16	R	Component serial number most significant bits
1Bh	[15:0]	Common Status	16	R	Status of common blocks
1Dh	[15:0]	Identification	16	R	Product type identification
1Fh	[15:0]	Status Summary	16	R/W	Status overview

Note:
R/W for the register means, that the content of the register can be read, and that it is also possible to over write the content of the register in normal mode operation. The following signal blocks will then operate with the value written to the register. After a write cycle to the register, the register will keep its value until another write cycle or reset occurs.

SPI read and write frames with CRC content for these registers are shown in Table 11.

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6.2.1 RATE Status 1 Register (09h)

Table 17. RATE Status 1 register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-								-	-	-	-	-	-	Write
VCMF_OK	Vboost_OK	Reserved[7:0]								SDM_D_OK	dQ_Amp_OK	dDR_Amp_OK	Q_AmpCtrl_OK	DR_Amp_Ctrl_OK	OF_R_OK	Read

RATE Status 1 register indicates saturation or failure in gyroscope. Failure is indicated by setting OK flag to 0, the condition will be latched until a read cycle on the register.

Table 18. RATE Status 1 register bit description.

Register Bit	Description
OF_R_OK	This bit indicates signal path saturation and overflow conditions
DR_AmpCtrl_OK	Status of drive amplitude control
Q_AmpCtrl_OK	Status of compensation signal amplitude control
dDR_Amp_OK	Status of drive amplitude
dQ_Amp_OK	Status of compensation signal amplitude
SDM_D_OK	Status of drive path stability
VBoost_OK	Status of VBoost voltage
VCMF_OK	Status of biasing voltage

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6.2.2 RATE Status 2 Register (0Ah)

Table 19. RATE Status 2 register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-								-	-	-	-	-	-	-	-	Write
Reserved[7:0]								S_N_OK	S_P_OK	D_N_OK	D_P_OK	SI_N_OK	SI_P_OK	DI_N_OK	DI_P_OK	Read

RATE Status 2 register indicates saturation or failure in gyroscope. Failure is indicated by setting OK flag to 0, the condition will be latched until a read cycle on the register.

Table 20. RATE Status 2 register bit description.

Register Bit	Description
DI_P_OK	Indicates saturation or failure condition
DI_N_OK	Indicates saturation or failure condition
SI_P_OK	Indicates saturation or failure condition
SI_N_OK	Indicates saturation or failure condition
D_P_OK	Indicates saturation or failure condition
D_N_OK	Indicates saturation or failure condition
S_P_OK	Indicates saturation or failure condition
S_N_OK	Indicates saturation or failure condition

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6.2.3 ACC Status Register (0Fh)

ACC Status register indicates accelerometer related failures. The accelerometer functionality is powered down in SCR2200-D13.

6.2.4 Test Register (15h)

16bit read/write register which can be used to check the accessibility of the device or if multiple devices are connected to the SPI bus, to check if the CS signals are working properly. The test register can be used by writing any 16bit value to data bits D[15:0] and then reading the test register twice (off frame protocol). In Table 21 1234h (0001 0010 0011 0100b) is used as an example but as stated, any 16bit value can be used.

Table 21. Example of Test register use.

Operation	MOSI (hex)	MISO	
		RS	DATA (hex)
Write 1234h to Test Register	D51234D2h	01b**	NA*
Read Test Register	5400008Fh	01b**	NA***
Read Test Register	5400008Fh	01b**	1234h

*Previous register values (off frame protocol)
**During normal operation should be ‘01b’. However, failure in other registers sets also Test Register RS bits to ‘11b’. See Table 12.
***Test register data value before writing 1234h. Default is 0000h.

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6.2.5 Reset Control Register (16h)

Table 22. Reset Control register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
Reserved[11:0]												MonitorST	HardReset	SoftReset	Reserved	Write
												-	-	-		Read

Table 23. Reset Control register bit description.

Register Bit	Description
SoftReset	Writing this bit to 1 generates a pulse typ. 10ms length to reset the logic core. User should not write to this bit.
HardReset	Writing this bit to 1 generates an EXTRESN compatible signal. Thus it is possible to generate hardware reset via SPI interface. With HardReset it is not possible to keep the ASIC in reset state, but reset starts after reset delay. With EXTRESN low it is possible to keep the ASIC in reset state. Reset delay (TRESD_r) applies to HardReset.
MonitorST	Writing this bit to 1 initiates self test of internal monitoring circuit Note: This signal is not allowed to be used during operation within the application.

6.2.6 Serial ID0 and Serial ID1 Registers (18h and 19h)

SCR2200-D13 serial number is laser marked on top of component lid and stored in to Serial ID0 and Serial ID1 registers. Serial number is in 32bit unsigned integer format. Serial number register bit descriptions are shown below in Table 24 and Table 25.

Table 24. Serial ID0 (18h) register (serial number LSB word).

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
ID0[15:0]																Read

Table 25. Serial ID1 (19h) register (serial number MSB word).

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
ID1[15:0]																Read

Example serial number conversion shown below:

- Serial ID0 register content: 8612h = bin 1000 0110 0001 0010
- Serial ID1 register content: 8FB9h = bin 1000 0110 0001 0010
- Full serial number: 8FB9 8612h = 2411300370
- Serial number laser marked on lid is 2411300370SCC

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6.2.7 Common Status Register(1Bh)

Table 26. Common Status register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
NMode_OK	MonCheck_OK	CRC_OTP_OK	CRC_SPI_OK	OF_C_OK	StateMon[3:0]				LOOPF_OK	TEMP_Mon_OK	VBG2_0P9V_OK	Reserved	VDDD_OK	VBG1_0P9V_OK	DVDD_OK	Read

Common Status register indicates failure in common signals/blocks. Failure is indicated by setting OK flag to 0, the condition will be latched until a read cycle on the register.

Table 27. Common Status register bit description.

Register Bit	Description
DVDD_OK	Status of DVDD digital 3.3V supply voltage
VBG1_0P9V_OK	Status of internal reference voltage
VDDD_OK	Status of digital core supply voltage
VBG2_0P9V_OK	Status of internal reference voltage
TEMP_Mon_OK	Status of temperature sensor signal
LOOPF_OK	Status of loop filter
StateMon[3:0]	Status of state machine for self test of monitoring circuit.
OF_C_OK	This bit indicates signal path saturation and overflow conditions related to common signals/blocks
CRC_SPI_OK	This bit indicates CRC failure in SPI communication
CRC_OTP_OK	This bit indicates CRC failure in OTP memory
MonCheck_OK	Result of the monitoring circuit self test
NMode_OK	Bit = 0 : ASIC test mode activated Bit = 1 : ASIC is in normal mode

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6.2.8 Identification Register (1Dh)

A special identification value for each part number of the SCC2000 product family is stored in to this register. Identification register can be used to identify the part number.

Table 28. Identification register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-				-				-			-					Write
Reserved [3:0]				ID RATE [3:0]				Reserved[2:0]			ID_ACC[4:0]					Read

Table 29. Identification register bit description.

Register Bit	Description	SCR2200-D13				
ID_ACC[4:0]	Identification of accelerometer configuration	D4	D3	D2	D1	D0
		0	0	0	0	0
ID_RATE[3:0]	Identification of gyro configuration	D11	D10	D9	D8	
		1	0	0	1	

6.2.9 Status Summary Register (1Fh)

Table 30. Status Summary register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-			-					-	-		-	-		-	Write
STC_EN	SelfTestDis	Flt[1:0]		Reserved[4:0]					S_OK_C	Reserved[1:0]		S_OK_A	Reserved[1:0]		S_OK_R	Read

Table 31. Status Summary register bit description.

Register Bit	Description
S_OK_R	Sensor status summary flag: gyro
S_OK_A	Sensor status summary flag: accelerometer Note: since accelerometer functionality is powered down, S_OK_A flag shows always error (S_OK_A='0')
S_OK_C	Status summary flag for common blocks and functionalities
Flt[1:0]	Output Filter Selection: 00b: 60Hz filter active for GYRO signal (default after reset), with Flt default setting S_OK_C is set to 0 01b: 10Hz filter active for GYRO signals 10b: 60Hz filter active for GYRO signal 11b: Reserved
SelfTestDis	SelfTestDis='1' indicates that the self test of the monitoring circuit is disabled.
STC_EN	STC_EN='1' indicates that the accelerometer self test is enabled.

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7 Application information

7.1 Application Circuitry and External Component Characteristics

See Figure 15 and Table 32 for specification of the external components. The PCB layout example is shown in Figure 16.

There is an option to reduce current consumption by 2mA with external 5V Vin_boost input voltage to L1 inductor. In this case the size of inductor L1 should be changed from 47µH (nom) to 100µH (nom).

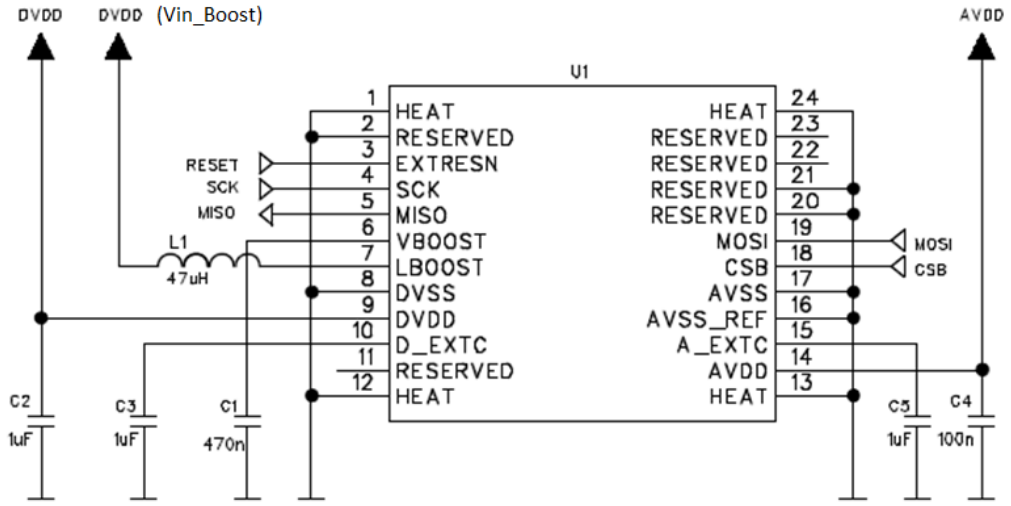

Figure 15. Application schematic.

Detailed pin description is shown in Table 5. Please note that pins 20 and 21 can be also left floating.

Table 32. External component description for SCR2200-D13.

Symbol	Description	Min.	Nom.	Max.	Unit
C1	High voltage capacitor. Voltage rating ESR@1MHz Recommended component: Murata GCM21BR71H474KA55, 0805, 470N, 50V, X7R	376 30	470	564 100	nF V mΩ
C2	Decoupling capacitor between DVDD and DVSS ESR@1MHz Recommended component: Murata GCM21BR71C105KA58, 0805, 1U, 16V, X7R	700	1000	1300 100	nF mΩ
C3	Decoupling capacitor between D_EXTC and DVSS ESR@1MHz Recommended component: Murata GCM21BR71C105KA58, 0805, 1U, 16V, X7R	700	1000	1300 100	nF mΩ
C4	Decoupling capacitor between AVDD and AVSS ESR@1MHz Recommended component: Murata GCM188R71C104KA37, 0603, 100N, 16V, X7R	70	100	130 100	nF mΩ
C5	Decoupling capacitor between A_EXTC and AVSS ESR@1MHz Recommended component: Murata GCM21BR71C105KA58, 0805, 1U, 16V, X7R	700	1000	1300 100	nF mΩ

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L1	If Vin_Boost = 3.0V...3.6V Inductance for high voltage generation from Vin_Boost ESR	37	47	57 5	µH Ω
	If Vin_Boost = 4.5V...5.5V Inductance for high voltage generation from Vin_Boost ESR Note that only one L1 is needed, the value is dependent on the input voltage of the Vin_Boost.	90	100	110 15	µH Ω

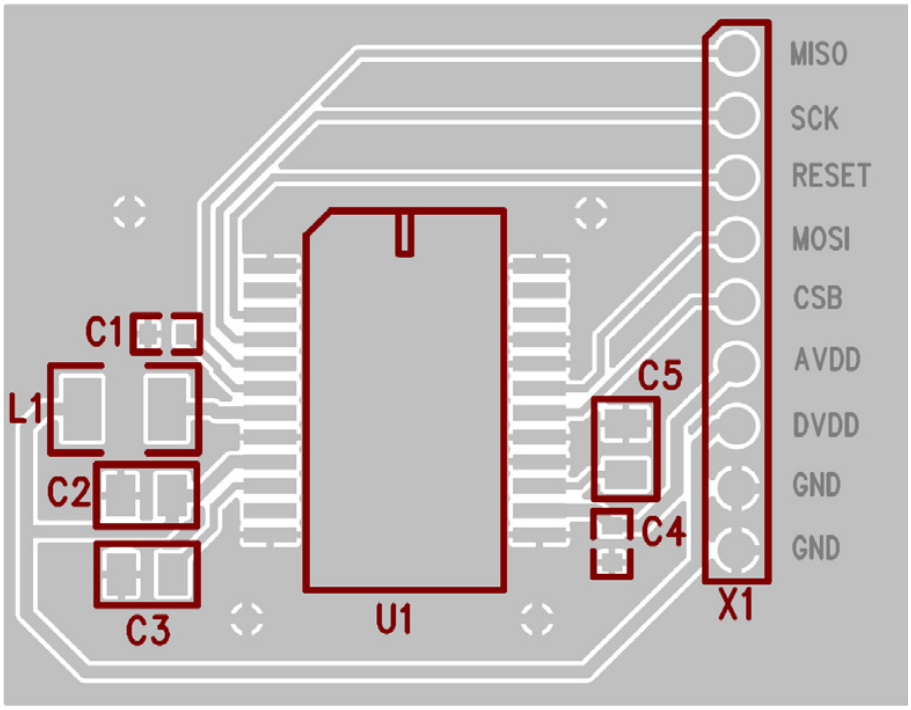

Figure 16. Application PCB layout.

General circuit diagram and PCB layout recommendations for SCR2200-D13 (refer to Figure 15 and Figure 16):

1. Connect decoupling SMD capacitors (C1 - C5) right next to respective component pins.
2. Locate ground plate under component.
3. Do not route signals or power supplies under the component on top layer.
4. Minimize the trace length between the L1 inductor and LBOOST pin (pin 7).
5. Ensure good ground connection of DVSS, AVSS_REF and AVSS pins (pins 8, 15, 16).

7.2 Assembly Instructions

Usage of PCB coating materials may have an effect on component performance. The coating material and coating process used has to be validated. Sealing of the component lid is prohibited. Additional assembly related guidelines in the document “APP2845 Assembly Instructions for SCC2000 Series” have to be followed. This document is available from Murata’s website.

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8 Order information

Table 33. SCR2200-D13 order codes with packing quantity.

Order code	Description	Packing	Qty
SCR2200-D13-004	Gyro (Z-axis ±125dps) with digital SPI i/f	Bulk	4pcs
SCR2200-D13-05	Gyro (Z-axis ±125dps) with digital SPI i/f	T&R	50pcs
SCR2200-D13-6	Gyro (Z-axis ±125dps) with digital SPI i/f	T&R	600pcs

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