LX3301A

Inductive Sensor Interface IC with Embedded MCU

Features

- Built-In Oscillator for Driving Primary Coil
- Two Independent Analog Channels with Demodulation
- 32-bit CORTUS APS3 RISC MCU with 12 Kbytes of Program Memory
- 128-Byte SRAM
- 32-Byte EEPROM
- Two Programmable Gain Amplifiers
- Two Anti-Alias Filters
- Two 13-Bit ADCs
- Selection of SINC and FIR Digital Filters
- One 12-Bit DAC
- One 16-Bit PWM
- Multiple Faults Detection and Protection
- Reverse Power Protection
- Digital Calibration with Nonvolatile Configuration Storage (EEPROM)
- Protected Watchdog Timer (WDT)
- Low Temperature Drift
- -40°C to +125°C Operation
- TD, PWM (Push-Pull), PWM (OD) Output
- Excellent Long-Term Stability
- AEC-Q100 Certification
- ISO26262 ASIL B Support

Applications

- Automotive Control
- Medical Equipment
- ATE Equipment
- Industrial Process Control
- Smart Energy Saving Control

Description

The LX3301A is a highly integrated programmable data conversion IC designed for interfacing to and managing of inductive sensors. The device includes an integrated oscillator circuit for driving the primary coil of an inductive sensor, along with two independent analog conversion paths for conditioning, converting, and processing of sine and cosine analog signals from the secondary coils of the sensor. Each path includes an EMI filter, demodulator, anti-alias filter, programmable amplifier, and a 13-bit Sigma-Delta Analog-to-Digital Converter (ADC).

Each analog signal path includes digital calibration capability which allows the complete analog path (including the external sensors) to be calibrated during the system manufacturing process. The calibration information is written to the internal EEPROM resulting in improved production yields and in-line system upgrades.

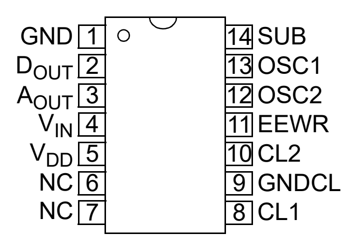
The LX3301A integrates a 32-bit RISC processor which provides programmable digital filtering and signal processing functions. The MCU resources include 12 Kbytes of program memory, 128 bytes of SRAM, and 32 bytes of user-programmable EEPROM. The program memory is available as mask-programmed ROM.

System interfaces include programmable PWM output and a 12-bit ADC analog buffed output.

The LX3301A is available in a 14-lead TSSOP package. The device is specified over a temperature range of -40°C to +125°C making it suitable for a wide range of commercial, industrial, medical, and/or automotive sensor applications.

Package Types

14-Pin TSSOP
(Top View)



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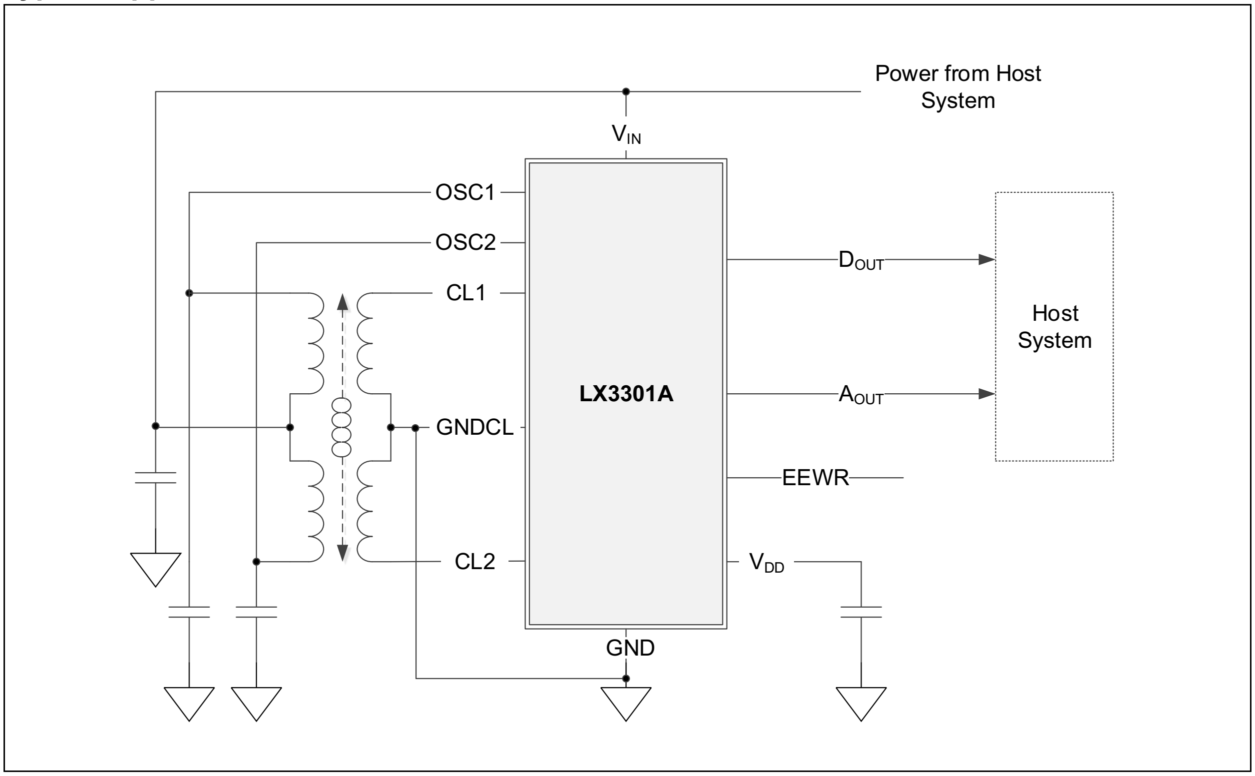
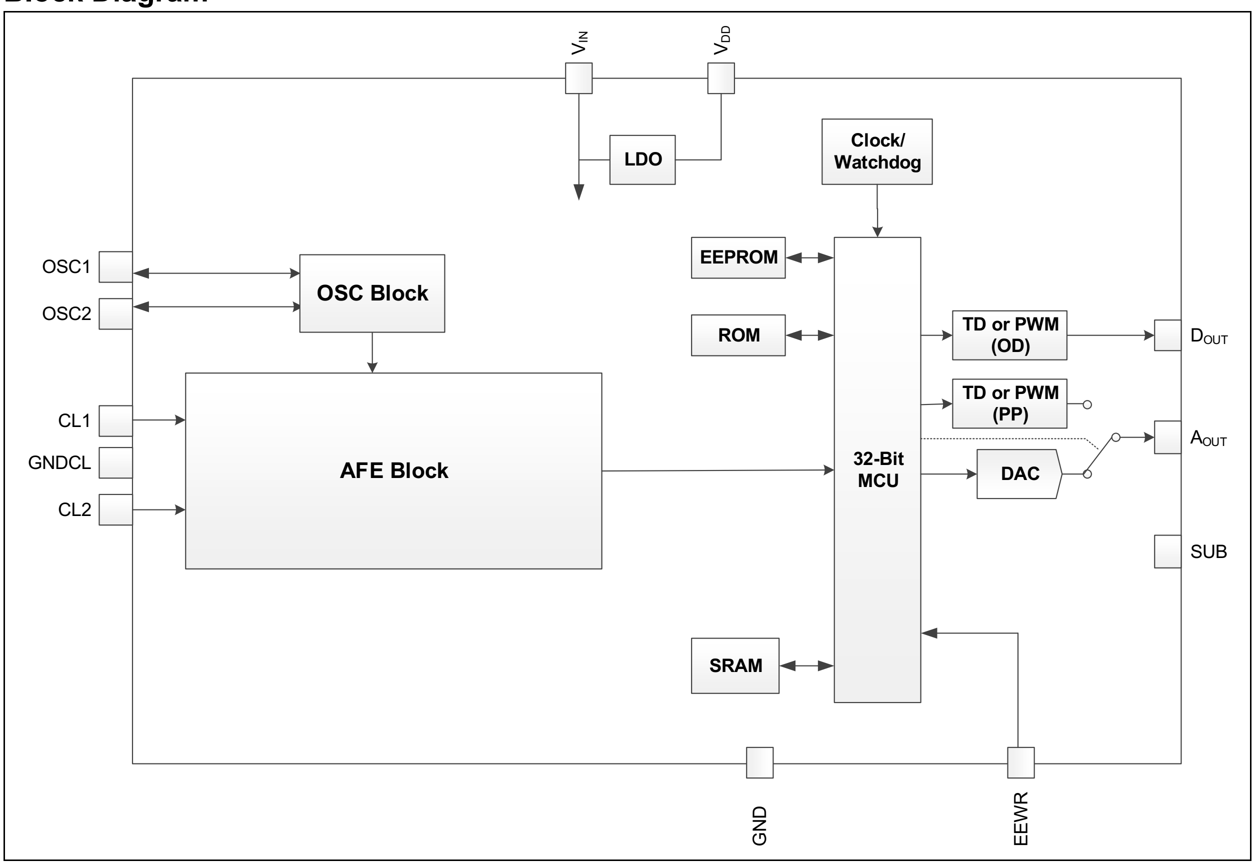
Typical Application



Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings †

Supply Input Voltage Pin (V_{IN}) .... -7V to 20V
Load Current on V_{DD} Pin .... -1 mA to 15 mA
Voltage on OSC1 and OSC2 Pins .... -0.3V to 16V
Voltage on CL1, CL2, EEWR Pins .... -0.5V to 3.6V
Voltage on A_{OUT}, D_{OUT} Pins .... -0.5V to 16V
Operating Humidity (non-condensing) .... 0% to 95%
Operating Temperature .... -40°C to +125°C
Storage Temperature .... -40°C to +150°C
Lead Temperature (soldering, 10 seconds) .... +300°C
Package Peak Temperature for Solder Reflow (40 seconds exposure) .... +260°C
ESD Rating – HBM (AEC-Q100-002D) .... ±2 kV
ESD Rating – Pin8, Pin14 – CDM (AEC-Q100-011) 750V
ESD Rating – Other Pins – CDM (AEC-Q100-011) 500V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability. All voltages are with respect to GND. All voltages on ESD are with respect to SUB.

Recommended Operating Range

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{IN}	4.4	5.0	5.6	V	For normal operation
V_{IN} EEPROM Program High	VIN_PH	—	—	17	V	
Supply Current	I_{IN}	—	—	10	mA	For normal operation, excluding oscillator tail current
Output Current	I_{AOUT0}	-15	—	-8	mA	A_{OUT} = 0V
	I_{AOUT5}	6	—	15	mA	A_{OUT} = 5V
	I_{DOUT0}	—	—	35	mA	D_{OUT} = 0V
Internal Clock Frequency	F_{OSC}	8.0	8.2	8.4	MHz	
Operating Temperature	T_{OP}	-40	—	+125	°C	

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Electrical Characteristics

Electrical Specifications: Unless otherwise indicated, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ +125°C and the following test conditions: V_{IN} = 5V, V_{DD} = 3.5V, I_{DD} = 5 mA, $I_{I/O}$ = 0 mA. Typical values are at +25°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power						
V_{IN} Input Voltage	V_{IN}	4.4	5.0	5.6	V	For normal operation
V_{IN} Supply Current	I_{IN}	—	8	10	mA	For normal operation, excluding oscillator tail current, I_{DD} = 0 mA, $I_{I/O}$ = 0 mA, f = 8.2 MHz
V_{IN} UV High Threshold	VIN_UV_HI	4.1	—	4.3	V	
V_{IN} UV Low Threshold	VIN_UV_LO	3.6	3.75	4.1	V	A_{OUT} goes low
V_{DD} Reference Voltage						
Output Voltage	V_{DD}	3.45	3.5	3.55	V	I_{DD} = 10 mA, trimmed
Output Current	I_{DD}	—	—	10	mA	Additional current sourced to external load(s)
V_{DD} UVLO	VDD_UVLO	2.9	—	3.4	V	Rising edge
Oscillator						
Middle Tap Voltage	V_{TAP}	—	5	—	V	V_{IN} = 5V
Total Tank DC Driving Current	ITK	0	—	10	mA	V_{TAP} = 5V
Swing Voltage of OSC1 and 2	V_{OSC}	3	—	9.5	V_{pp}	V_{TAP} = 5V
Typical Swing Voltage of OSC1	$V_{OSC1TYP}$	—	6.5	—	V_{pp}	V_{TAP} = 5V, Target at typical air gap distance. Set by external capacitor.
Reference Frequency Range	F_{OSC}	1	—	5	MHz	V_{TAP} = 5V
Frequency Variation	F_{OSCTOL}	-5	—	5	%	V_{TAP} = 5V
Reference Inductance	L_{OSC}	—	6	—	µH	V_{TAP} = 5V, Inductor connected to OSC1, 2 pins
Tank Circuit Quality Factor	Q_{OSC}	15	25	—	—	V_{TAP} = 5V
Harmonics	H_{OSC}	—	—	2	%	V_{TAP} = 5V, GBNT
Resistance between OSC1 and V_{IN}	ROSC1_VIN	1	—	—	MΩ	V_{IN} = 5V, OSC1 = GND, Measure Current from OSC1 to GND
Resistance between OSC2 and V_{IN}	ROSC2_VIN	1	—	—	MΩ	V_{IN} = 5V, OSC2 = GND, Measure Current from OSC2 to GND
Resistance between OSC1 and GND	ROSC1_GND	1	—	—	MΩ	V_{IN} = 0V, OSC1 = 5V, Measure Current from OSC1 to 5V
Resistance between OSC2 and GND	ROSC2_GND	1	—	—	MΩ	V_{IN} = 0V, OSC2 = 5V, Measure Current from OSC2 to 5V
Resistance between OSC1 and OSC2	ROSC1&2_HI	500	—	—	kΩ	OSC1 = 1V_{pp}, OSC2 = GND
ADC 1 and 2						
ADC Resolution	ADC01	13	—	—	bits	
Integral Nonlinearity	ADC03	-1	—	1	LSB	GBNT

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Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ +125°C and the following test conditions: V_{IN} = 5V, V_{DD} = 3.5V, I_{DD} = 5 mA, $I_{I/O}$ = 0 mA. Typical values are at +25°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
SINC, SINC + FIR Filter 1 and 2						
Data Update Rate	DUR00	—	2	—	kHz	REFRESH = 00, (SINC, INC + FIR)
	DUR01	—	1	—	kHz	REFRESH = 01, (SINC, SINC + FIR)
	DUR02	—	500	—	Hz	REFRESH = 10, (SINC, SINC + FIR)
	DUR03	—	250	—	Hz	REFRESH = 11, (SINC, SINC + FIR)
Filter SNR	FLTRSNR	—	-86	-73	dB	GBNT
Crosstalk Rejection	CTR	—	-44	—	dB	GBNT
Power Supply Rejection Ratio	PSRR	—	-86	—	dB	GNBT
Internal Clock						
Clock Frequency	FCLK	8	8.2	8.4	MHz	After trimming
Processing Resources						
MCU Data Bus	MCU01	—	32	—	bits	
MCU Instruction Size	MCU02	16	—	32	bits	
ROM Size	MCU03	—	12	—	Kbytes	32-bit words
SRAM Size	MCU04	—	128	—	bytes	Application data, 32-bit words
EEPROM Write Endurance	MCU05	100	—	—	cycles	
EEPROM Size	MCU06	—	16	—	words	16-bit words
Watchdog Timer						
Power-Up Watchdog Timer	TPUWT	—	16.3	—	ms	
D_{OUT} (PWM, Open-Drain)						
Frequency	D_{OUT01}	1.945	2	2.055	kHz	Refresh = 2 kHz, after trimming, +25°C
Minimum PWM Duty	D_{OUT02}	—	0.125	—	%	HCLMP = 1023, LCLMP = 0, ORIGIN = 0, Frequency = 2 kHz
Maximum PWM Duty	D_{OUT03}	—	—	100	%	No clamped output
PWM Jitter	D_{OUT04}	—	0.2	—	%P	%P = % Period
Maximum Sink Current	D_{OUT05}	—	—	-35	mA	D_{OUT} = OD PWM or TD
A_{OUT} (As Address Selection)						
High-Level Input Voltage	AOUT_VIH	2.0	—	—	V	
Low-Level Input Voltage	AOUT_VLO	—	—	0.3	V	
A_{OUT} (Analog Output)						
A_{OUT} Analog Range	AOUT_R	0	—	V_{IN}	V	
A_{OUT} Low Voltage	VAOUT_LO	—	—	4	$\%V_{IN}$	RL_AOUT = 10 kΩ to V_{IN}
A_{OUT} High Voltage	VAOUT_HI	96	—	—	$\%V_{IN}$	RL_AOUT = 10 kΩ to GND
A_{OUT} Output Load	RL_AOUT	1	10	—	kΩ	
A_{OUT} Sink Current	I_{AOUT0}	—	—	-8	mA	A_{OUT} = 0V
A_{OUT} Source Current	I_{AOUT5}	6	—	15	mA	A_{OUT} = 5V

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Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ +125°C and the following test conditions: V_{IN} = 5V, V_{DD} = 3.5V, I_{DD} = 5 mA, $I_{I/O}$ = 0 mA. Typical values are at +25°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
A_{OUT} Slew Rate	AOUTSR1	—	0.2	—	V/µs	C_{LOAD} = 22 nF
	AOUTSR2	—	0.1	—		C_{LOAD} = 100 nF
Ratiometric Error	$V_{RatioErr}$	-0.2	0	0.2	%V_{IN}	
Fault Output Low Level	VAOUT_FL10K	—	—	1	%V_{IN}	RL_AOUT = 10 kΩ to V_{IN}
	VAOUT_FL1K	—	—	1.5		RL_AOUT = 1 kΩ to V_{IN}
Fault Output High Level	VAOUT_FH10K	98	—	—	%V_{IN}	RL_AOUT = 10 kΩ to GND
	VAOUT_FH1K	97	—	—		RL_AOUT = 1 kΩ to GND
Ground Off Output Low Level	VAOUT_GF10K	—	—	4	%V_{IN}	Broken GND, 10 kΩ ≤ RL_AOUT ≤ 20 kΩ to external ground, T_A ≤ +125°C
	VAOUT_GF20K	—	—			Broken GND, 20 kΩ < RL_AOUT ≤ 220 kΩ to external ground, T_A ≤ +105°C
	VAOUT_GF3K	—	—			Broken GND, 1 kΩ ≤ RL_AOUT < 10 kΩ to external ground. With assist pull-up on board between V_{IN} and GND
Ground Off Output High Level	VAOUT_GF1K	99	100	—	%V_{IN}	Broken GND, RL_AOUT ≥ 1 kΩ to V_{IN}
V_{IN} Open Output Low Level	VAO_VIN1K	—	0	1	%V_{IN}	Broken V_{IN}, RL_AOUT ≥ 1 kΩ to GND
A_{OUT} (PWM Output)						
High-Level Output Voltage	V_{OH}	95	—	100	%V_{IN}	Duty = 50%, 10 kΩ pull-down to GND
Low-Level Output Voltage	V_{OL}	0	—	200	mV	Duty = 50%, 10 kΩ pull-up to V_{IN}
Rise Time	AOUT_TR	—	10	—	µs	Duty = 50%
Fall Time	AOUT_TF	—	10	—	µs	Duty = 50%
Minimum Duty	D_{min}_A_{OUT}	—	—	4	%	PWM (PP)
Maximum Duty	D_{max}_A_{OUT}	94	—	—	%	PWM (PP)
Max. Drive/Sink Current	IAOUTP	-35	—	35	mA	A_{OUT} = PWM
Output CLAMP						
Clamp High Output Level	HCLMP	0	—	99.9	%V_{IN}	Pull-up Output to V_{IN}
Clamp Low Output Level	LCLMP	0	—	99.9	%V_{IN}	Pull-up Output to V_{IN}
EEPROM Programming						
Program Low	VIN_PL	9.5	10	10.5	V	For EEPROM programming mode
Program Idle	VIN_PI	11.75	13	13.5	V	For EEPROM programming mode
Program High	VIN_PH	14.75	16	17	V	For EEPROM programming mode
Duration Time	td	20	—	—	µs	Duration time for each voltage state

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Temperature Specifications[1]

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Thermal Resistance, Junction to Ambient	θ_{JA}	—	+117	—	°C/W	
Thermal Resistance, Junction to Case	θ_{JC}	—	+22	—	°C/W	

Note 1: The θ_{JA} numbers assume no forced airflow. Junction temperature is calculated using the formula: $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the Printed Circuit Board (PCB) construction. The stated number above is for a four-layer board in accordance with JESD-51-7 (JEDEC®).

NOTES:

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN DESCRIPTIONS

14-Lead TSSOP	Symbol	Description
1	GND	Analog and Digital Power Ground pin.
2	D_{OUT}	Digital Out pin. This pin can be programmed to open-drain PWM with current limit or the threshold detector (TD) output.
3	A_{OUT}	Analog Out pin. This pin can be programmed to provide an analog output (DAC), threshold detector, or a PWM output. PWM will be the push-pull operation. This pin can be used as an address pin for EEMODE.
4	V_{IN}	Power Supply and Internal EEPROM Programming pin. DC input power is applied to this pin for normal operation. It is also used for EEPROM programming. Bypass this pin to GND pin with a low-ESR capacitor. The recommended value is between 100 nF and 1 µF. A larger capacitance will affect the EEPROM programming.
5	V_{DD}	Regulator Output pin. This is the output of the internal voltage regulator providing power to the analog and digital blocks. Bypass this pin to GND pin with a low-ESR capacitor not lower than 1 µF.
6, 7	NC	Not Connected. These pins are not internally connected.
8	CL1	Sensor Signal from Secondary Coil 1 of Inductive Sensor pin.
9	GNDCL	Reference Ground for CL1 and CL2 pins. Connect CL1 and CL2 coils to GNDCL and connect the GNDCL to GND directly.
10	CL2	Sensor Signal from Secondary Coil 2 of Inductive Sensor pin.
11	EEWR	EEWR is active-low. When EEWR is low, it prohibits change to the internal EEPROM contents. The pin contains an internal pull-down so it can be left floating for normal use. If an external pull-down is desired, the SUB pin must be used as reference, and not GND. To unlock when the LOCK bits are set to '1', pull this pin to V_{DD} with 10 kΩ.
12	OSC2	Oscillator Pin 2. It connects to the second side of the primary inductor coil. An external capacitor is connected between this pin and GND as part of the LC tank circuit. The external capacitor should be low-ESR, C0G or NP0, or equivalent, rated voltage 50V.
13	OSC1	Oscillator Pin 1. It connects to the first side of the primary inductor coil. An external capacitor is connected between this pin and GND as part of the LC tank circuit. The external capacitor should be low-ESR, C0G or NP0, or equivalent, rated voltage 50V.
14	SUB	Substrate pin. It is used for ground failure protection. It should not be connected to GND. For normal applications, leave this pin open.

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NOTES:

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3.0 EEPROM CONFIGURATION

The LX3301A integrates a 16 words by 16 bits (256 bits), user-programmable EEPROM for storing calibration and configuration parameters. The calibration parameters enable the production sensor assembly to be customer-factory calibrated assuring consistent unit to unit performance.

Table 3-1 itemizes the LX3301A Configuration EEPROM contents and Table 3-2 shows the LX3301A EEPROM Configuration map. Note that EEPROM contents of ID and FACTORY shall be kept as original value when EEPROM is reprogrammed.

TABLE 3-1: LX3301A EEPROM CONFIGURATION

Name	Description	Size (bits)	Words and Bits (MSb:LSb)	Sign	Min. Value	Max. Value	Default Value
ID	Customer Part ID	18	W0[15:0] W1[15:14]	No	0	3FFFF	Serial #
REFRESH	Refresh Rate	2	W1[13:12]	No	0	3	0
FACTORY	Factory Programming	12	W1[11:0]	No	—	—	—
CHKSUM	4-bit Checksum Value	4	W2[15:12]	No	0	—	—
S5	Slope of Sixth Segment	12	W2[11:0]	No	0	4095	511
OUTSEL	Output Setup	4	W3[15:12]	No	—	—	1011B
S0	Slope of First Segment	12	W3[11:0]	No	0	4095	511
ORIGIN	Origin	12	W4[15:12] W5[15:12] W6[15:12]	No	0	4095	0
Y5	Linearization Point 5 Y-Coordinate	12	W4[11:0]	No	0	4095	3413
X5	Linearization Point 5 X-Coordinate	12	W5[11:0]	No	0	4095	3413
Y3	Linearization Point 3 Y-Coordinate	12	W6[11:0]	No	0	4095	2047
OSCOMP	OSC Voltage Compensation	8	W7[15:12] W8[15:12]	No	0	255	255
X3	Linearization Point 3 X-Coordinate	12	W7[11:0]	No	0	4095	2047
Y1	Linearization Point 1 Y-Coordinate	12	W8[11:0]	No	0	4095	683
FILTER	Select Digital Filter	1	W9[15]	No	0	1	1
TDHYST	Threshold Detect Hysteresis	3	W9[14:12]	No	0	112	111B
X1	Linearization Point 1 X-Coordinate	12	W9[11:0]	No	0	4095	683
TD	Threshold Detect	12	W10[15:10] W11[15:10]	No	0	4095	3685
LCLMP	Low Clamp	10	W10[9:0]	No	0	1023	1
HCLMP	High Clamp	10	W11[9:0]	No	0	1023	1023
Y2	Linearization Point 2 Y-Coordinate	6	W12[15:10]	Yes	-31	31	0
DSIN	Dynamic Sine Offset	10	W12[9:0]	Yes	-511	511	0
Y4	Linearization Point 4 Y-Coordinate	6	W13[15:10]	Yes	-31	31	0
SSIN	Static Sine Offset	10	W13[9:0]	Yes	-511	511	0
IOSC	OSC Current Source	2	W14[15:14]	No	0	3	0
DEBUG	Debug	1	W14[13]	No	0	1	0
TDPOL	TD Polarity	1	W14[12]	No	0	1	0
CLSEL	CL1, 2 Input Select	1	W14[11]	No	0	1	0
EELOCK	EEPROM Write Protection	1	W14[10]	No	0	1	0
DCOS	Dynamic Cosine Offset Correction	10	W14[9:0]	Yes	-511	511	0
GMTCH	Gain Match	6	W15[15:10]	Yes	-12.09%	12.09%	0
SCOS	Static Cosine Offset Correction	10	W15[9:0]	Yes	-511	511	0

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TABLE 3-2: LX3301A EEPROM CONFIGURATION MAP

<table>
<tr><td></td><td colspan="8">MSb</td><td colspan="8">LSb</td></tr>
<tr><td></td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>WORD0</td><td colspan="16">ID[17..2]</td></tr>
<tr><td>WORD1</td><td colspan="2">ID[1..0]</td><td colspan="2">REFRESH</td><td colspan="12">FACTORY[11..0]</td></tr>
<tr><td>WORD2</td><td colspan="4">CHKSUM[3..0]</td><td colspan="12">S5[11..0]</td></tr>
<tr><td>WORD3</td><td colspan="4">OUTSEL[3..0]</td><td colspan="12">S0[11..0]</td></tr>
<tr><td>WORD4</td><td colspan="4">ORIGIN[11..8]</td><td colspan="12">Y5[11..0]</td></tr>
<tr><td>WORD5</td><td colspan="4">ORIGIN[7..4]</td><td colspan="12">X5[11..0]</td></tr>
<tr><td>WORD6</td><td colspan="4">ORIGIN[3..0]</td><td colspan="12">Y3[11..0]</td></tr>
<tr><td>WORD7</td><td colspan="4">OSCOMP[7..4]</td><td colspan="12">X3[11..0]</td></tr>
<tr><td>WORD8</td><td colspan="4">OSCOMP[3..0]</td><td colspan="12">Y1[11..0]</td></tr>
<tr><td>WORD9</td><td colspan="2">FILTER</td><td colspan="2">TDHYST[2..0]</td><td colspan="12">X1[11..0]</td></tr>
<tr><td>WORD10</td><td colspan="6">TD[11..6]</td><td colspan="10">LCLMP[9..0]</td></tr>
<tr><td>WORD11</td><td colspan="6">TD[5..0]</td><td colspan="10">HCLMP[9..0]</td></tr>
<tr><td>WORD12</td><td colspan="6">Y2[5..0]</td><td colspan="10">DSIN[9..0]</td></tr>
<tr><td>WORD13</td><td colspan="6">Y4[5..0]</td><td colspan="10">SSIN[9..0]</td></tr>
<tr><td>WORD14</td><td colspan="2">IOSC[1..0]</td><td>FMSK</td><td>TDPOL</td><td>CLSEL</td><td>EELOCK</td><td colspan="10">DCOS[9..0]</td></tr>
<tr><td>WORD15</td><td colspan="6">GMTCH[5..0]</td><td colspan="10">SCOS[9..0]</td></tr>
</table>

3.1 ID

This is the ID field. The Customer Part ID is an 18-bit field containing customer part identification information.

3.2 CHKSUM

This 4-bit value is a 4-bit cyclic redundancy check (CRC) to check the rest of content reliability through lifetime. The CRC calculation is based on the code as shown in Example 3-1. Sum2 is 4-bit checksum.

3.3 FACTORY

The FACTORY bits contain factory trimmed information. Do not change.

3.4 TD, TDHYST and TDPOL

The TD output is enabled using OUTSEL. The output polarity of TD is set by TDPOL. When TDPOL is set to '1', the output pin goes low when the Input signal exceeds the 2 × TD value. The output pin goes high when the Input signal exceeds the 2 × TD – 16 × TDHYST value. If TDPOL is set to '0', the output pin goes high when the Input signal exceeds the 2 × TD value. The output pin goes low when the Input signal is lower than the 2 × TD – 16 × TDHYST value. TDHYST is used to set the hysteresis value of the TD level. See Figure 3-1.

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EXAMPLE 3-1:

```
uint16_t data[16];
#define GENPOLY 0x0013U /* x^4 + x + 1 */
uint32_t makecrc4(uint32_t b)
 /*
 * Takes b as input, which should be the information vector already multiplied by x^4 (ie. shifted
 * over 4 bits), and returns the crc for this input based on the defined generator polynomial GENPOLY
 */
{
 uint32_t i;
 i=1U;
 while (b>=16U) { /* >= 2^4, so degree(b) >= degree(genpoly) */
  if ((((b >> (20U-i))) & 0x1U) == 1U)
  {
   b ^= GENPOLY << (16U-i); /* reduce with GENPOLY */
  }
  i++;
 }
 return b;
}
void Calculate_CRC(void)
{
 int sum2=0,sum1=0;
 for (uint8_t counter = 0U; counter <= 16U; counter++) {
  if (counter != 2U) {
   sum1 += data[counter];
  } else {
   sum1 += data[counter] & 0x0FFFU;
  }
 }
 sum2 = makecrc4(((sum1 >> 16)^(sum1&0xFFFFU)) << 4);
 cout<< " IC CRC :"<<sum2<<endl<<endl;
}
```

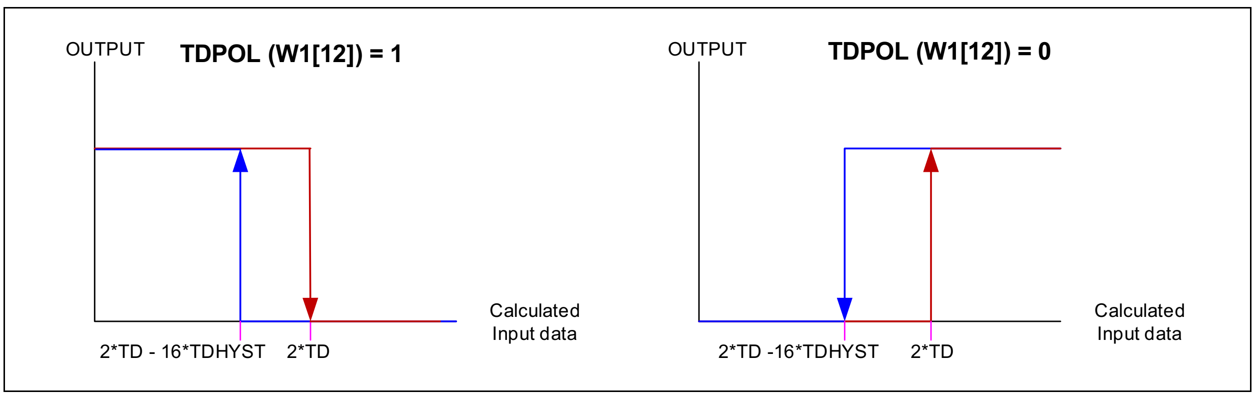

FIGURE 3-1: *TD, TDHYST and TDPOL Configuration.*

3.5 FILTER

This bit selects the digital filter type. Setting the bit to '0' will set the filter type to SINC and setting the bit to '1' will set the filter to SINC + FIR. See Table 3-3.

TABLE 3-3: FILTER CONFIGURATION

Filter Bit	Filter Type
0	SINC
1	SINC + FIR

3.6 REFRESH

This parameter sets the value of the refresh rate of the ADC update. If the PWM output is selected, the PWM frequency is always equal to the ADC update rate. See Table 3-4.

TABLE 3-4: REFRESH BIT CONFIGURATION

Bit Value	Refresh Rate
0	2 kHz
1	1 kHz
2	500 Hz
3	250 Hz

3.7 IOSC

These two bits set the oscillator tail current value. See Table 3-5.

TABLE 3-5: IOSC CONFIGURATION

IOSC Bits	Tail Current	Feedback
00	Full Range	Enabled
01	1/2	Enabled
10	1/4	Enabled
11	1/8	Enabled

3.8 EELOCK

There are two control signals: one is from the EEWR pin (if set to Active-Low, it disables to write EEPROM at EEMODE) and the other is for the EELOCK bits on the Configuration EEPROM (W14[10]). If the EELOCK bit is set to '1' and the EEWR pin is pulled to low, the EEPROM cannot be written. The default value of W14[10] is '0'.

3.9 OUTSEL

The OUTSEL bits provide the various output selection options. See Table 3-6.

TABLE 3-6: OUTSEL BITS CONFIGURATION

Output Configuration				Remarks
Bit 1, Bit 0	A_{OUT}	Bit 3, Bit 2	D_{OUT}	
00	TD	00	TD	
01	Reserved	01	Reserved	
10	PWM (PP)	10	OD_PWM	PP = Push-Pull, OD = Open-Drain
11	Analog	11	Reserved	

3.10 SCOS

Static offset correction of the CL1 input channel used in input correction calculations.

3.11 DCOS

Dynamic offset correction of the CL1 input channel used in input correction calculations.

3.12 SSIN

Offset correction of the CL2 input channel used in input correction calculations.

3.13 DSIN

Dynamic offset correction of the CL2 input channel used in input correction calculations.

3.14 GMTCH

Value of the input channel gain mismatch correction used in input correction calculations.

3.15 OSCOMP

Maximum amplitude of the oscillator swing used in the input correction calculations. The maximum value of the OSCOMP is 255, Step 1. Multiplied by 4, it converts as internal OSCOMP data.

3.16 ORIGIN

Offset value of the system origin relative to fore-and-after position. This is not a DC output offset adjustment. Verify that the LCLMP and HCLMP parameters are not limiting the output range. Multiplied by 2, it converts as internal ORIGIN data.

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3.17 HCLMP

This parameter sets the output high clamp level. The output is clamped at this value if the output swing can go above this level. The HCLMP value used in calculations is 8 × (value + 1) – 1 on W11[9:0]. It reduces the maximum output swing. Maximum level is achieved with HP = 1023.

3.18 LCLMP

This parameter sets the output low clamp level. The output is clamped at this level if the output swing can go below this level. The LCLMP value raises the minimum output value from 0. The LCLMP value used in calculations is 8 × (value – 1) on W10[9:0]. An output value of 0 is achieved with LCLMP = 1. The LCLMP setting value overrides the HCLMP setting if both settings are crossed over.

3.19 S0

This parameter sets the slope of the first linearization segment.

3.20 X1 and Y1

The value of the X and Y coordinates for the first linearization point. Multiplied by 2, it converts as internal data.

3.21 X3 and Y3

The value of the X and Y coordinates for the third linearization point. Multiplied by 2, it converts as internal data.

3.22 X5 and Y5

The value of the X and Y coordinates for the fifth (and last) linearization point. Multiplied by 2, it converts as internal data.

3.23 S5

This parameter sets the slope of the last linearization segment.

3.24 Y2

The value of X2 is calculated by X1 and X3 parameters as X2 = (X1 + X3)/2. The Y2 value is the value that can adjust the coordinates for the second linearization point. The Y2 value has polarity and the calculated value of the second coordinate (y) at X2 is y = (Y1 + Y3)/2 + Y2. Multiplied by 2, it converts as internal data.

3.25 Y4

The value of X4 is calculated by X3 and X5 parameters as X4 = (X3 + X5)/2. The Y4 value is the value that can adjust the coordinates for the fourth linearization point. The Y4 value has polarity and the calculated value of the fourth coordinate (y) at X4 is y = (Y3 + Y5)/2 + Y4. Multiplied by 2, it converts as internal data.

3.26 CLSEL

The CLSEL bit selects the CL1 or CL2 inputs as sine or cosine inputs. When CLSEL is set to ‘1’, the CL1 input is selected as a sine value and the CL2 input is selected as a cosine input. When CLSEL is set to ‘0’, the CL1 input is selected as a cosine value and the CL2 input is selected as a sine value.

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NOTES:

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4.0 THEORY OF OPERATION

4.1 General Information

The LX3301A is a highly integrated programmable data conversion IC designed for interfacing to and managing of inductive sensors. The device includes an integrated oscillator circuit for driving the primary coil of an inductive sensor, along with two independent analog conversion paths for conditioning, converting, and processing of two analog signals from the secondary coils of the PCB sensor. Each path includes an EMI filter, demodulator, anti-alias filter, programmable amplifier, and a 13-bit Sigma-Delta Analog-to-Digital Converter before the signal processing unit. The signal processing unit peripherals include programmable PWM controller and a 12-bit digital-to-analog converter.

4.2 Oscillator

The on-chip oscillator provides a carrier signal for driving the primary coil of the inductive sensor via pins OSC1 and OSC2. The carrier signal is generated by an internal current source which resonates with the primary inductors and external capacitors (which form a tank circuit). The oscillator operates over a frequency range from 1 MHz to 5 MHz as shown in Equation 4-1.

EQUATION 4-1:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Where:

L = Inductance of coil

C = Tanking capacitance

The value of the inductor L is the most critical element in the cross-coupled LC tank oscillator. Because the inductance is relatively low, the parasitic resistance of L can dominate and impact the ability to maintain oscillation. As such, the value of the inductor L should be as large as possible and with a high Q factor. The external capacitor should be low-ESR, C0G or NP0, or equivalent and 50V rated.

In most applications, the inductor L is implemented as traces on a PCB. Depending on the processing of the PCB, the height and width of the trace will vary, resulting in a variation of the inductance L and of the parasitic resistance. Because these variations will change from PCB to PCB, it is necessary to calibrate each PCB sensor independently. Care should be taken to select a PCB source which can achieve the manufacturing tolerances required by a given set of system requirements.

The amplitude of the carrier signal is a function of the primary coil tank circuit configuration and feedback of the secondary coil signals from the CL1 and CL2 inputs. The shoulder signals of the tank circuit are detected by an internal circuit. It will distort the sinusoidal waveform if the tank circuit and the secondary coil feedback signal are not within design limits.

In order to detect system Faults, the IC monitors the amplitude of the carrier signal on pin OSC1. When the amplitude is above or below the specified amplitude (see OSCILLATOR: Swing Voltage of OSC1 and 2, V_{OSC}, in the **Electrical Characteristics** section), the A_{OUT} output pin is forced to 0V. This output level indicates a system Fault. When initially calibrating a sensor, the voltage on OSC1 should be monitored in order to verify that the amplitude is within the specified range.

The optimal level of OSC1 is about 6.5 V_{PP}, with target at typical air gap distance. If the OSC1 voltage is too high, the signal levels at CL1 and CL2 may be too low. If the OSC1 voltage is too low, the signal levels at CL1 and CL2 may be too high.

4.3 Input Amplifier and Signal Conditioning

Pins CL1 and CL2 are the inputs to analog front-end (AFE) block paths.

The front-end gain amplifier can be programmed with 4 bits, where the `0000b` default gain value is 3.125. Bit value percentage changes can be done as shown in Table 4-1.

TABLE 4-1: PROGRAMMABLE GAIN AMPLIFICATION SETTING

Bit #	Function
0	Amplification +3%
1	Amplification +6%
2	Amplification +12%
3	Amplification -24%

The output of the front-end gain amplifier is then passed through an anti-aliasing filter prior to input to the Sigma-Delta ADC.

4.4 Sigma-Delta ADC with Digital Filters

Each analog path includes a 4th-order 13-bit Sigma-Delta ADC with precision internal voltage reference, which produces true 12-bit measurement results. The sampling frequency for the ADC is derived from the main clock and selected by REFRESH in the configuration EEPROM. See Table 4-2.

TABLE 4-2: SAMPLING FREQUENCY

REFRESH	Function
00	ADC clock = Main clock/8
01	ADC clock = Main clock/16
10	ADC clock = Main clock/32
11	ADC clock = Main clock/64

The ADC decimation filter includes a SINC filter and a half-band FIR filter. The SINC filter provides -40 dB of stop-band attenuation. Because the SINC filter does not provide the same sharp response as a finite/infinite filter response, a half-band FIR filter is also provided. The drawback of the FIR filter is that it adds delay to the input signal and this delay depends on the number of coefficients and the output data rate. The filter can be selected by the Filter setting in the configuration EEPROM.

4.5 Embedded MCU

The LX3301A includes an embedded 32-bit microcontroller core, which is used to perform filtering and math functions on the digitized samples from the ADC. The device includes a set of preprogrammed filtering and math functions, which can be selected by setting the appropriate bits in the on-chip configuration EEPROM. Also, system calibration and linearization coefficient bits are included in the on-chip configuration EEPROM.

4.6 Configuration EEPROM

The LX3301A includes a user-programmable 16 x 16 bits EEPROM for storing configuration parameters into nonvolatile memory. The device is placed into EEPROM Programming mode (EEMODE) by increasing the voltage on the V_{IN} pin to 13V. Note that the data can be clocked only after t_2 > 4 ms from last power-on, and the maximum t_2 time is less than 10 ms. To protect the chip from accidentally entering the EE mode, the V_{IN} voltage must be above 10V continuously for at least t_1 > 25 µs. The data is modulated to V_{IN} by either increasing or decreasing the voltage. To clock a '1', V_{IN} must be increased to 16V, whereas to clock a '0', V_{IN} must be decreased to 10V. Between each data, V_{IN} must return to 13V. Each state must have a minimum duration of 20 µs (t_2) and a maximum of 110 µs (t_4). VEETH is 9V typical. See Figure 4-1.

4.6.1 LX3301A EEMODE COMMANDS

There are four commands provided for accessing the LX3301A either by writing or reading the EEPROM or ADCs for testing. Other commands are reserved. See Table 4-3.

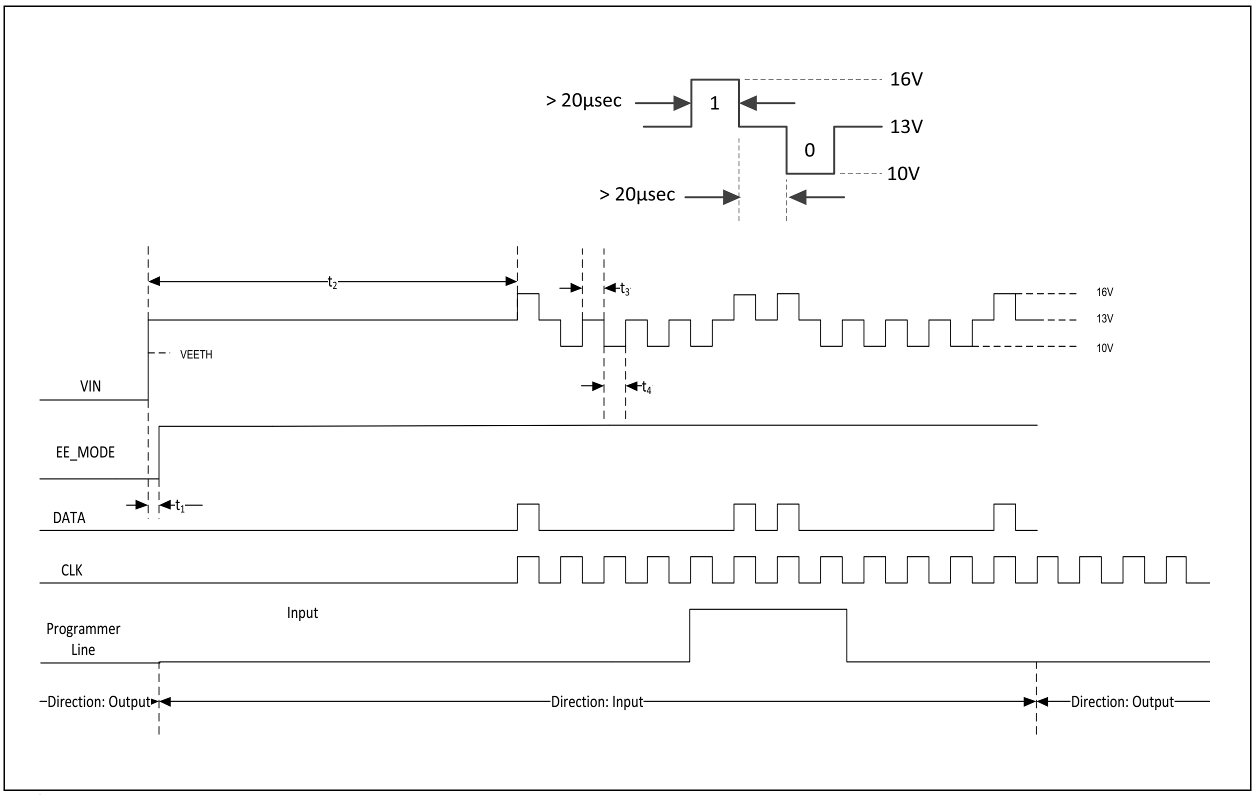

FIGURE 4-1: *V_{IN} Programming Timing Diagram.*

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TABLE 4-3: LX3301A EEMODE COMMANDS

Bit												Command	Description	Remarks
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**			
1	0	0	0	0	CS	CS	0	0	0	0	1	Writing mode, data A_{OUT} and (D_{OUT})	Send 12 bits command then 256 EEPROM bits and 20-bit checksum. A_{OUT} is CS input.	CS = 00 or 11
0	1	0	0	0	CS	CS	0	0	0	1	0	Writing mode, data on D_{OUT} only	Send 12 bits command then 256 EEPROM bits and 20-bit checksum. A_{OUT} is CS input.	CS = 00 or 11
1	0	1	0	0	CS	CS	0	0	1	0	1	EEPROM Read out to A_{OUT} and D_{OUT}	Send 12 bits command then 256 EEPROM bits and 20-bit checksum. A_{OUT} is CS input.	CS = 00 or 11
0	0	0	0	1	0	0	1	0	0	0	0	Read out ADCs on A_{OUT} and D_{OUT}	Send 12 bits command then Drop V_{IN} to 21 Refresh rate cycles then 36 clocks (ADC1 + ADC2 + ADC10) to read back date on A_{OUT} and D_{OUT}.	Need Unlock command
0	1	0	1	1	0	0	1	1	0	1	0	Unlock command		
Others												Reserved		

4.6.2 EEPROM WRITING WITH A_{OUT}

To enter the EEPROM Writing mode with A_{OUT}, the user must enter the EEMODE and send the12-bit command as shown in Example 4-1. Enter command 10000XX00001 then followed by 16 Words starting from LSB of the WORD0 and finishing with the MSB of the WORD15 and 20-bit checksum of the 16 Words. If the checksum is wrong, the EEPROM will not be erased or written. The address input is A_{OUT} pin. Note that the command starts from B0, B1, B2, B3, B4, Addr, Addr, B4, B3, B2, B1, B0 and so on. Figure 4-2 shows examples of EEPROM Writing with A_{OUT} and CS = 11.

EXAMPLE 4-1:

Command					Addr	Addr	Command					WORD0			WORD1			...	WORD15			Checksum		
B0	B1	B2	B3	B4			B4	B3	B2	B1	B0	B0	...	B15	B0	...	B15	...	B0	...	B15	B0	...	B19
1	0	0	0	0	0/1	0/1	0	0	0	0	1	0/1	...	0/1	0/1	...	0/1	...	0/1	...	0/1	0/1	...	0/1

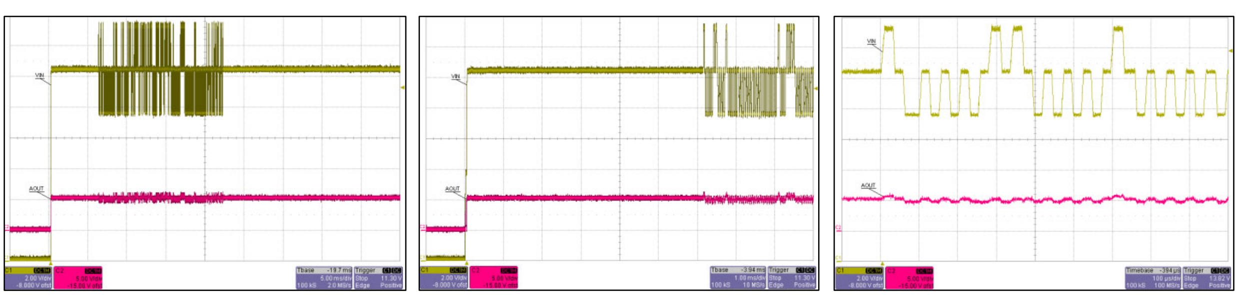

FIGURE 4-2: *EEPROM Writing with A_{OUT} and CS = 11.*

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4.6.3 EEPROM WRITING WITH D_{OUT} ONLY

To enter the EEPROM Writing mode with D_{OUT}, the user must enter the EEMODE and send the 12-bit command as shown in Example 4-2. Enter command `01000XX00010` then followed by 16 Words starting from LSB of the WORD0 and finishing with the MSB of the WORD15 and 20-bit checksum of the 16 Words. If the checksum is wrong, the EEPROM will not be erased or written. The address input is A_{OUT} pin. Note that the command starts from B0, B1, B2, B3, B4, Addr, Addr, B4, B3, B2, B1, B0 and so on. It is also required to connect A_{OUT} through 100K resistor (R4) from D_{OUT} as shown in Figure 4-3.

Figure 4-4 shows examples of EEPROM Writing with D_{OUT} and CS = `00`.

EXAMPLE 4-2:

Command					Addr	Addr	Command					WORD0			WORD1			...	WORD15			Checksum		
B0	B1	B2	B3	B4			B4	B3	B2	B1	B0	B0	...	B15	B0	...	B15	...	B0	...	B15	B0	...	B19
0	1	0	0	0	0/1	0/1	0	0	0	1	0	0/1	...	0/1	0/1	...	0/1	...	0/1	...	0/1	0/1	...	0/1

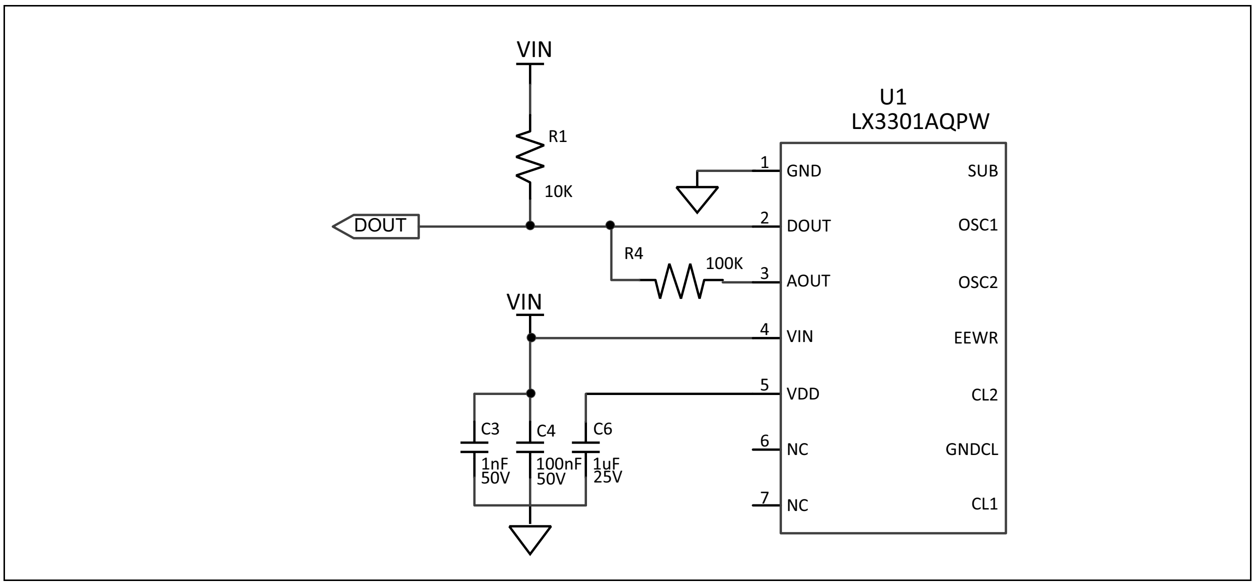

FIGURE 4-3: *Connecting A_{OUT} through 100k resistor (R4) from D_{OUT}.*

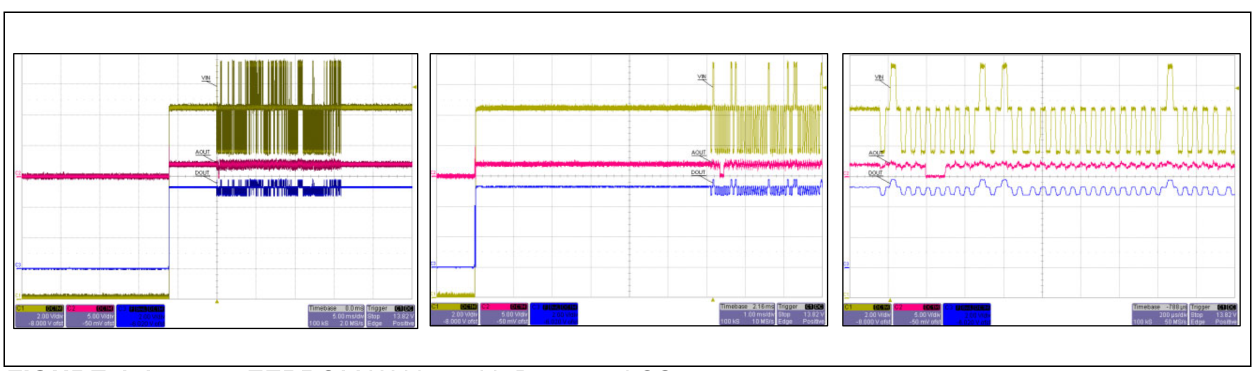

FIGURE 4-4: *EEPROM Writing with D_{OUT} and CS = `00`.*

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4.6.4 READING FROM EEPROM TO A_{OUT} AND D_{OUT}

To enter the EEPROM Read-Out mode from A_{OUT}, the user must enter the EEMODE and send the 12-bit command (`10100XX00101`) as shown in Example 4-3.

EXAMPLE 4-3:

Command					Addr	Addr	Command					WORD0			WORD1			...	WORD15			Checksum		
B0	B1	B2	B3	B4			B4	B3	B2	B1	B0	B0	...	B15	B0	...	B15	...	B0	...	B15	B0	...	B19
1	0	1	0	0	0/1	0/1	0	0	1	0	1	0/1	...	0/1	0/1	...	0/1	...	0/1	...	0/1	0/1	...	0/1

Once these 12-bit command have been sent, the outputs are reactivated and the A_{OUT} and D_{OUT} pins will have transitioned to logic high. To serial out the data, a clock pulse must be sent to V_{IN}. After each clock, the next bit is sent to the output, starting with bit 0 of WORD0 to bit 15 of WORD15. After bit 15 of WORD15 has been read, it will send the 20-bit checksum of WORD0 to WORD15 of EEPROM. An extra clock at the end will output logic low. Figure 4-5 shows examples of EEPROM Reading using address = A_{OUT} and CS = `11`.

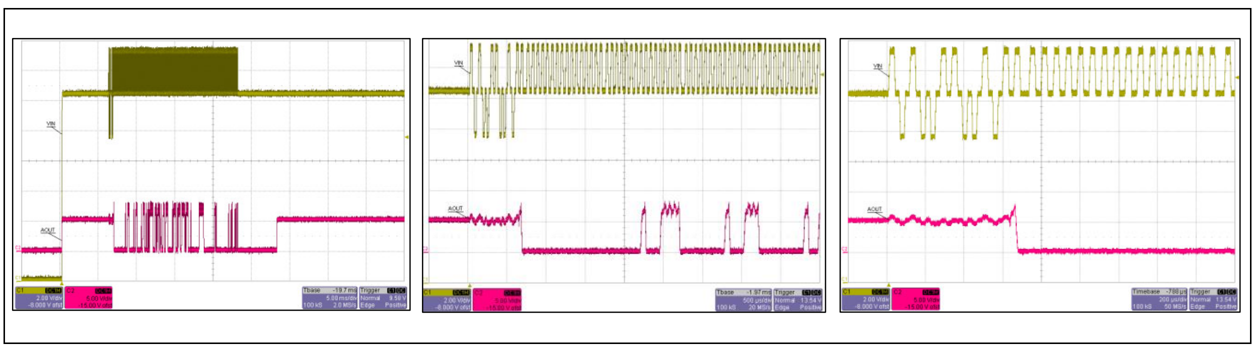

FIGURE 4-5: *EEPROM Reading using Address A_{OUT} and CS = `11`.*

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4.6.5 ADC READ MODE

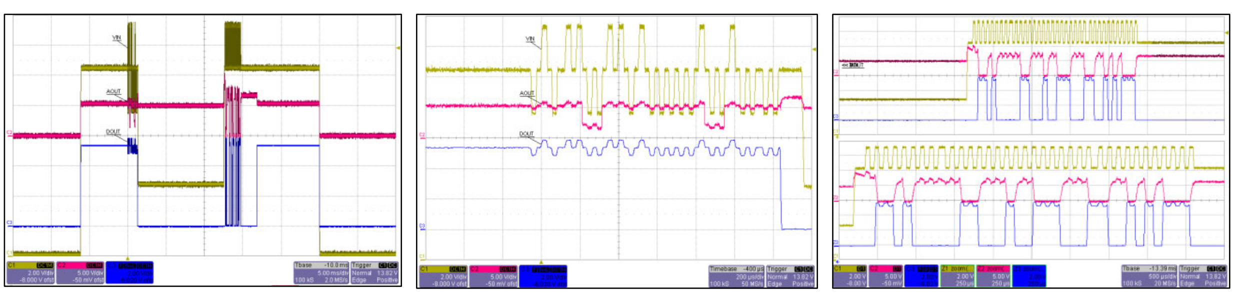
The ADC Read mode can be used for the input calibration. When the device enters this mode, then it can read out the value of the 3 ADCs (ADC1, ADC2 and ADC10). To enter this mode, the user must enter the EEMODE and send the Unlock command and then the 12-bit command as shown in Example 4-4 in order to have ADC values sent to the A_{OUT} and D_{OUT}. Then V_{IN} has to be lowered to the operating voltage. The device waits 21 refresh cycles and then it reads the ADCs. To read out the values, the V_{IN} has to be set to 13V and logic high will appear on the D_{OUT}. Then 36 clocks (ADC1 (13clocks) + ADC2 (13clocks) + ADC10 (10 clocks)) to read back data on A_{OUT} and D_{OUT}. An extra clock is needed to exit this mode. During this test mode, the refresh rate, the IOSC bits and the Filter selection are not changed.

EXAMPLE 4-4:

Unlock Command — **ADC Read Command**

Command					**Addr**	**Addr**	**Command**					**Command**					**Addr**	**Addr**	**Command**				
B0	B1	B2	B3	B4			B4	B3	B2	B1	B0	B0	B1	B2	B3	B4			B4	B3	B2	B1	B0
0	1	0	1	1	0	0	1	1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0

Note that if selecting A_{OUT} pin read out, the user must release the pin (which is used for addressing) as soon as $A_{OUT}$is de-tristate. Also note that the output of the digital will go straight to the A_{OUT} output buffer. This buffer will be working with its input stage in saturation mode and with a gain of 2.5. The consequence is that the logic high will clamp around 6.5V. The end user should therefore set this to logic high. The maximum threshold is around 5V. Figure 4-6 shows examples of ADC read operation.



Complete ADC cycle — Unlock Command — 36-bit ADCs Data

FIGURE 4-6: *ADC Read Operation.*

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4.7 PWM Controller

A 16-bit digital PWM controller is implemented on the chip. It can generate a pulse-width modulated signal of varying period and duty cycle. The PWM module has a 2-bit pre-scalar to divide the MCU clock signal. The PWM frequency is selected by REFRESH on the configuration EEPROM. The PWM mode can be set by OUTSEL. When the D_{OUT} PWM is selected, the pull-up resistor between D_{OUT} and V_{IN} or V_{DD} is needed (10 kΩ recommended). PWM frequency is trimmed at factory.

4.8 A_{OUT}

A_{OUT} has three functions that can be programmed to provide an analog output (amplified from the DAC output), a TD, or a PWM output. PWM will be a push-pull operation. It is also used as an address pin for EEMODE. For analog output, a 12-bit DAC is implemented on the chip. The internal DAC supply voltage is V_{DD}. The A_{OUT} is amplified from the DAC output and its supply voltage is from V_{IN}. Therefore, the A_{OUT} output range is limited by the V_{IN} voltage. The boot-up time (the time between the first valid A_{OUT} of the sensor from V_{IN} reaches the V_{IN} UVLO high threshold) is 4 ms (typical), with REFRESH = 2 kHz.

4.9 Protection

Versatile system diagnostic and protection functions are incorporated in the LX3301A to provide reliable protection of the device and the system. Key Fault conditions and output status are shown in Table 4-4.

4.10 Reverse Power and Ground Off Protection

The LX3301A implements the reverse power protection feature when V_{IN} and GND connections are reversed. When the power connection is reversed, the internal circuits are disconnected from the supply and the outputs are pulled to ground. The LX3301A implements the ground off protection feature when the ground is disconnected.

4.11 High-Voltage LDO

A high-voltage, low-temperature drift, low-dropout, precision voltage regulator is implemented on the chip. The regulator provides the internal power to the chip and also provides power for the external components, such as pull-up resistors. Decoupling caps are required to ensure high-performance analog measurements where the recommended value is 1 µF. V_{DD} is pre-trimmed at factory.

TABLE 4-4: FAULT CONDITIONS AND OUTPUT STATUS

Fault Condition	Output Status	Remarks
V_{IN} undervoltage	Tri-state	UVLO
V_{DD} undervoltage	Forced low	UVLO
V_{DD} unstable or oscillating	Forced low	V_{DD} noise or improper decoupling
CL1, 2 disconnected	Forced low	
CL1, 2 signal overvoltage	Forced low	Reacquire input values at next refresh cycle
CL1, 2 signal too low	Forced low	Reacquire input values at next refresh cycle
OSC1 connection fail	Forced low	
OSC1 overvoltage	Forced low	
OSC1 undervoltage	Forced low	
ROM or RAM test failure at start-up	Forced low	Restart by µP
EEPROM reading error or RAM writing failure	Forced low	Restart by µP
Periodic ROM checksum failure	Forced low	Restart by µP
Software does not follow the intended execution flow	Forced low	Restart by µP
CPU test vector failure	Forced low	Restart by µP

NOTES:

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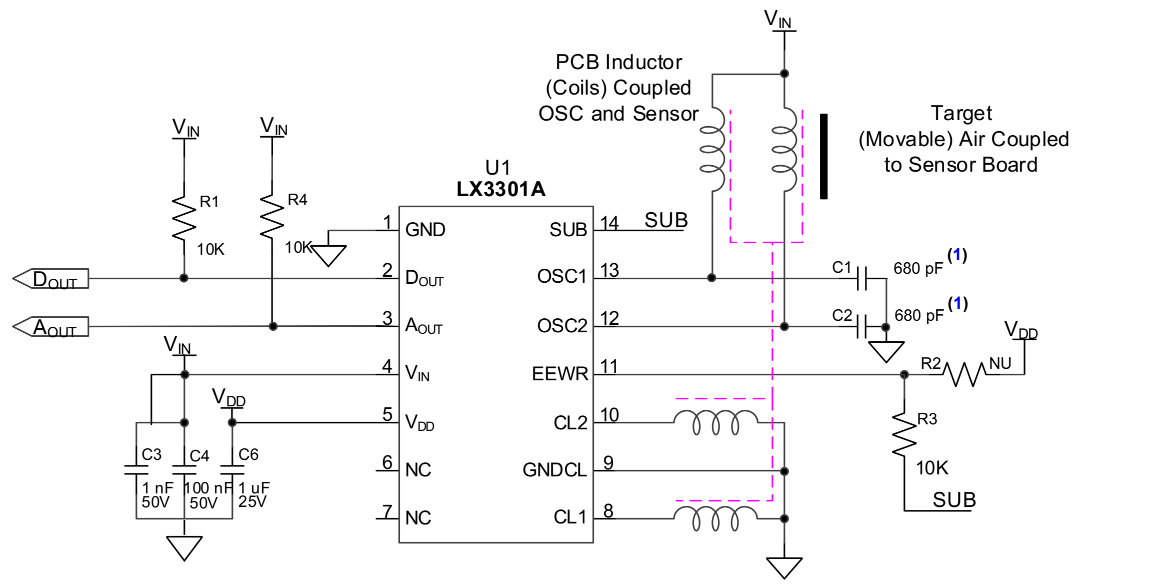
5.0 REFERENCE SCHEMATIC

The LX3301A 14-pin reference schematic is shown in Figure 5-1.



Note 1: Cap value is for reference only. The user must select it to set the desired oscillation frequency. Low-ESR, C0G, or NP0 type, 50V rated, should be used.

FIGURE 5-1: *LX3301A 14-Pin Reference Schematic.*

NOTES:

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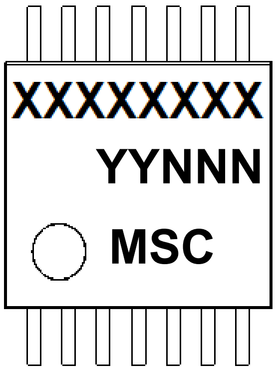
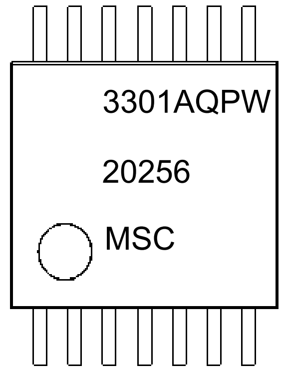
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

14-Lead TSSOP



Example



Legend:	XX...X	Device-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	NNN	Alphanumeric traceability code
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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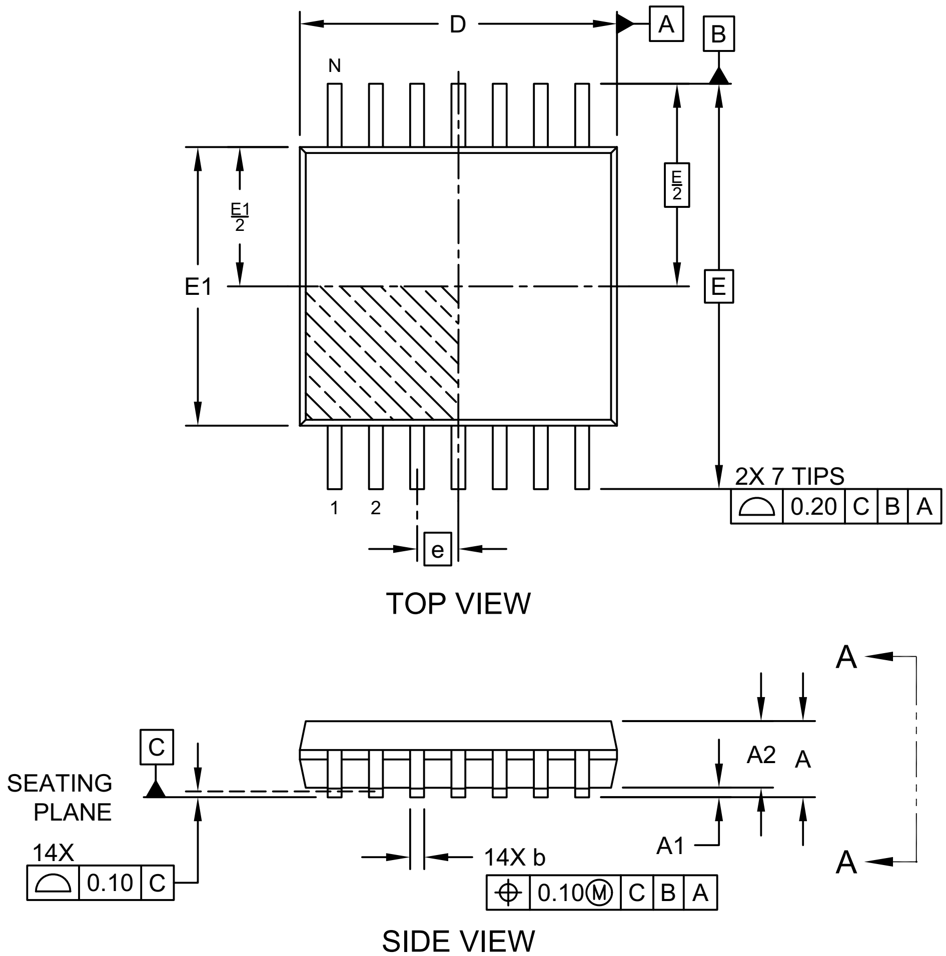
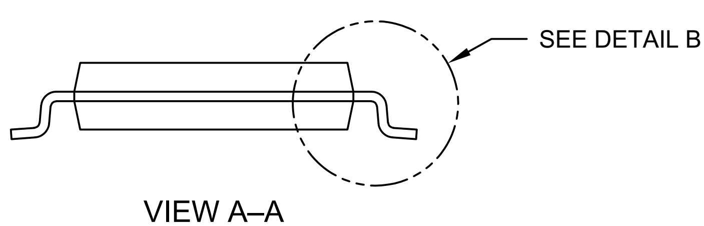
14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-087 Rev E Sheet 1 of 2

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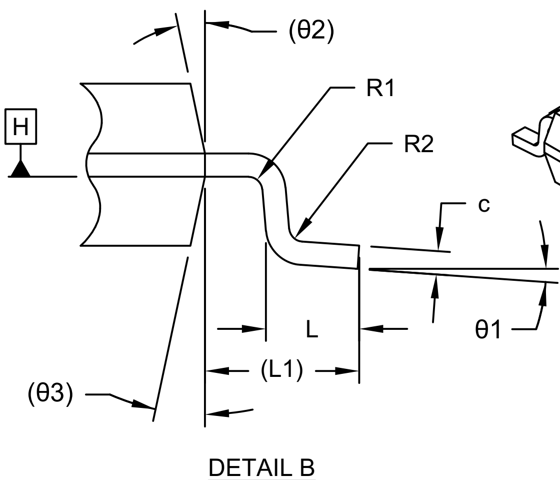
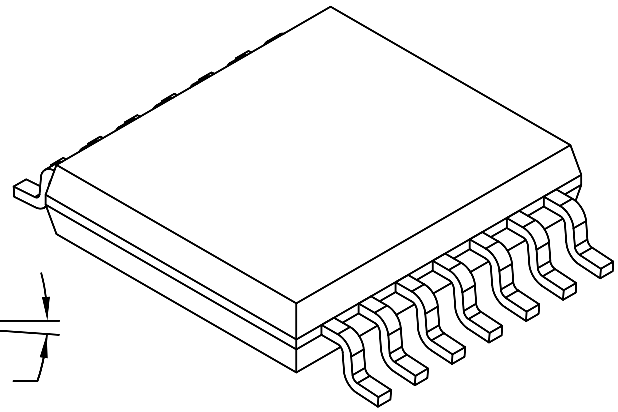
14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





		Units	MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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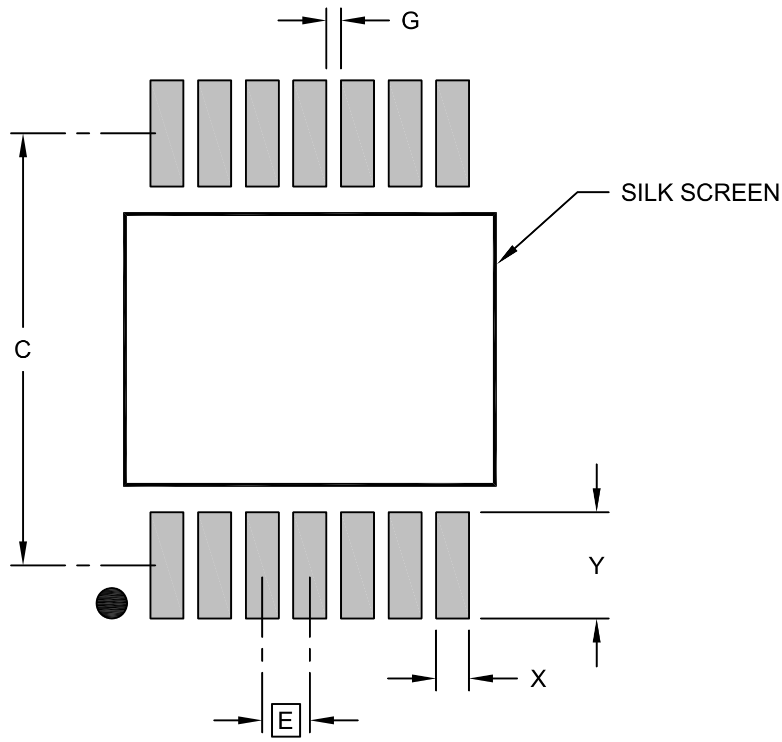
14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (Xnn)	X			0.45
Contact Pad Length (Xnn)	Y			1.45
Contact Pad to Contact Pad (Xnn)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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APPENDIX A: REVISION HISTORY

Revision C (July 2022)

The following is the list of modifications:

- Updated Recommended Operating Range.

Revision B (March 2021)

The following is the list of modifications:

- Updated Example 3-1.

Revision A (July 2020)

- Initial release of this document.
- This document replaces *"LX3301A Data Sheet – Inductive Sensor Interface IC with Embedded MCU"* (Microsemi, 1.5/12.19).

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	XX[(1)]
Device		Tape and Reel Option

Device: LX3301AQPW: Inductive Sensor Interface IC with Embedded MCU

Tape and Reel:
Blank = Standard Packaging (Tube)
TR = Tape and Reel

Examples:

a) LX3301AQPW: -40°C to +125°C Ambient Temperature, RoHS2 Compliant, Pb-free, 14-Lead TSSOP Package

b) LX3301AQPW-TR: -40°C to +125°C Ambient Temperature, RoHS2 Compliant, Pb-free, 14-Lead TSSOP Package, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with Microchip for package availability with the Tape and Reel option.

NOTES:

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