
**32-Bit Flash Microcontroller with MIPS32[®] microAptiv[™] UC Core
with Low Power and Low Pin Count**

Operating Conditions

- 2.0V to 3.6V, -40°C to +125°C, DC to 25 MHz
- 2.0V to 3.6V, -40°C to +85°C, DC to 25 MHz

Low-Power Modes

- Low-Power modes:
 - Idle: CPU off, peripherals run from system clock
 - Sleep: CPU and peripherals off:
 - Fast wake-up Sleep with retention
 - Low-power Sleep with retention
- 0.5 μ A Sleep Current for Regulator Retention mode and 5 μ A for Regulator Standby mode
- On-Chip 1.8V Voltage Regulator (VREG)
- On-Chip Ultra Low-Power Retention Regulator

High-Performance 32-Bit RISC CPU

- microAptiv[™] UC 32-Bit Core with 5-Stage Pipeline
- microMIPS[™] Instruction Set for 35% Smaller Code and 98% Performance compared to MIPS32 Instructions
- DC-25 MHz Operating Frequency
- 3.17 CoreMark[®]/MHz (79 CoreMark) Performance
- 1.53 DMIPS/MHz (37 DMIPS) (Dhrystone 2.1) Performance
- 16-Bit/32-Bit Wide Instructions with 32-Bit Wide Data Path
- Two Sets of 32 Core Register Files (32-bit) to Reduce Interrupt Latency
- Single-Cycle 32x16 Multiply and Two-Cycle 32x32 Multiply
- Hardware Divide Unit
- 64-Bit, Zero Wait State Flash with ECC to Maximize Endurance/Retention

Microcontroller Features

- Low Pin Count Packages, Ranging from 20 to 36 Pins, including UQFN as Small as 4x4 mm
- Up to 64K Flash Memory:
 - 20,000 erase/write cycle endurance
 - 20 years minimum data retention
 - Self-programmable under software control
- Up to 8K Data Memory
- Pin-Compatible with Most PIC24 MCU/dsPIC[®] DSC Devices
- Multiple Interrupt Vectors with Individually Programmable Priority
- Fail-Safe Clock Monitor mode
- Configurable Watchdog Timer with On-Chip, Low-Power RC Oscillator
- Programmable Code Protection
- Selectable Oscillator Options including:
 - High-precision, 8 MHz internal Fast RC (FRC) oscillator
 - High-speed crystal/resonator oscillator or external clock
 - 2x/3x/4x/6x/12x/24x PLL, which can be clocked from the FRC or primary oscillator

Peripheral Features

- Atomic Set, Clear and Invert Operation on Select Peripheral Registers
- High-Current Sink/Source 11 mA/16 mA on All Ports
- Independent, Low-Power 32 kHz Timer Oscillator
- Two 4-Wire SPI modules (up to 25 MHz non-PPS, 20 MHz PPS):
 - 16-byte FIFO
 - I²S mode
- Two UARTs:
 - RS-232, RS-485 and LIN/J2602 support
 - IrDA[®] with on-chip hardware encoder and decoder
- External Edge and Level Change Interrupt on All Ports
- CRC module
- Hardware Real-Time Clock and Calendar (RTCC)
- Up to 20 Peripheral Pin Select (PPS) Remappable Pins
- Seven Total 16-Bit Timers:
 - Timer1: Dedicated 16-bit timer/counter
 - Two additional 16-bit timers in each MCCP and SCCP module
- Capture/Compare/PWM/Timer modules:
 - Two 16-bit timers or one 32-bit timer in each module
 - PWM resolution down to 21 ns
 - One Multiple Output (MCCP) module:
 - Flexible configuration as PWM, input capture, output compare or timers
 - Six PWM outputs
 - Programmable dead time
 - Auto-shutdown
 - Two Single Output (SCCP) modules:
 - Flexible configuration as PWM, input capture, output compare or timers
 - Single PWM output
- Reference Clock Output (REFO)
- Two Configurable Logic Cells (CLC) with Internal Connections to Select Peripherals and PPS

Debug Features

- Two Programming and Debugging Interfaces:
 - 2-wire ICSP[™] interface with non-intrusive access and real-time data exchange with application
 - 4-wire MIPS[®] standard Enhanced JTAG interface
- IEEE Standard 1149.2 Compatible (JTAG) Boundary Scan

PIC32MM0064GPL036 FAMILY

Analog Features

- Two Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit DAC with Output Pin
- Up to 14-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
 - 12-bit, up to 222k samples/second conversion rate
 - 10-bit, up to 250k samples/second conversion rate
 - Sleep mode operation
 - Band gap reference input feature
 - Windowed threshold compare feature
 - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0064GPL036 FAMILY DEVICES

| Device | Pins | Program Memory (Kbytes) | | General Purpose I/O/PPS | 16-Bit Timers Maximum | PWM Outputs Maximum | Remappable Peripherals | | | | | 10/12-Bit ADC (Channels) | Comparators | CRC | RTCC | JTAG | Packages | |
|-------------------|-------|-------------------------|----------------------|-------------------------|-----------------------|---------------------|--------------------------------|---------------|---------------------|---------------------|-----|--------------------------|-------------|-----|------|------|----------|--------------------------------------|
| | | Program Memory (Kbytes) | Data Memory (Kbytes) | | | | UART ⁽¹⁾ /LIN/J2602 | 16-Bit Timers | MCCP ⁽³⁾ | SCCP ⁽⁴⁾ | CLC | | | | | | | SPI ⁽²⁾ /I ² S |
| PIC32MM0016GPL020 | 20 | 16 | 4 | 16/16 | 7 | 8 | 2 | 1 | 1 | 2 | 2 | 2 | 11 | 2 | Yes | Yes | Yes | SSOP/QFN |
| PIC32MM0032GPL020 | 20 | 32 | 8 | 16/16 | 7 | 8 | 2 | 1 | 1 | 2 | 2 | 2 | 11 | 2 | Yes | Yes | Yes | SSOP/QFN |
| PIC32MM0064GPL020 | 20 | 64 | 8 | 16/16 | 7 | 8 | 2 | 1 | 1 | 2 | 2 | 2 | 11 | 2 | Yes | Yes | Yes | SSOP/QFN |
| PIC32MM0016GPL028 | 28 | 16 | 4 | 22/19 | 7 | 8 | 2 | 1 | 1 | 2 | 2 | 2 | 12 | 2 | Yes | Yes | Yes | SSOP/SOIC/QFN/UQFN |
| PIC32MM0032GPL028 | 28 | 32 | 8 | 22/19 | 7 | 8 | 2 | 1 | 1 | 2 | 2 | 2 | 12 | 2 | Yes | Yes | Yes | SSOP/ SOIC/QFN/UQFN |
| PIC32MM0064GPL028 | 28 | 64 | 8 | 22/19 | 7 | 8 | 2 | 1 | 1 | 2 | 2 | 2 | 12 | 2 | Yes | Yes | Yes | SPDIP/SSOP/SOIC/QFN/UQFN |
| PIC32MM0016GPL036 | 36/40 | 16 | 4 | 29/20 | 7 | 8 | 2 | 1 | 1 | 2 | 2 | 2 | 14 | 2 | Yes | Yes | Yes | VQFN/UQFN |
| PIC32MM0032GPL036 | 36/40 | 32 | 8 | 29/20 | 7 | 8 | 2 | 1 | 1 | 2 | 2 | 2 | 14 | 2 | Yes | Yes | Yes | VQFN/UQFN |
| PIC32MM0064GPL036 | 36/40 | 64 | 8 | 29/20 | 7 | 8 | 2 | 1 | 1 | 2 | 2 | 2 | 14 | 2 | Yes | Yes | Yes | VQFN/UQFN |

Note 1: UART1 has assigned pins. UART2 is remappable.

2: SPI1 has assigned pins. SPI2 is remappable.

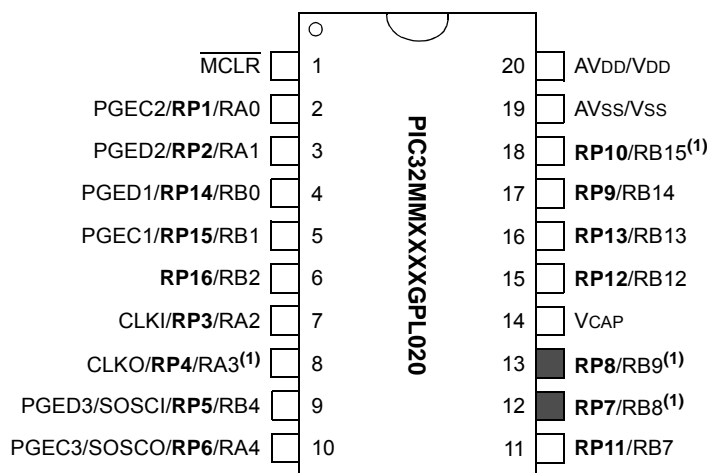
3: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

4: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

PIC32MM0064GPL036 FAMILY

Pin Diagrams

20-Pin SSOP



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to [Section 26.0 “Electrical Characteristics”](#) for details.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 20-PIN SSOP DEVICES

| Pin | Function | Pin | Function |
|-----|--|-----|--|
| 1 | MCLR | 11 | RP11/RB7 |
| 2 | PGEC2/VREF+/AN0/RP1/OCM1E/INT3/RA0 | 12 | TCK/RP7/U1CTS/SCK1/OCM1A/RB8 ⁽¹⁾ |
| 3 | PGED2/VREF-/AN1/RP2/OCM1F/RA1 | 13 | TMS/REFCLKI/RP8/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9 ⁽¹⁾ |
| 4 | PGED1/AN2/C1IND/C2INB/RP14/RB0 | 14 | VCAP |
| 5 | PGEC1/AN3/C1INC/C2INA/RP15/RB1 | 15 | TDO/AN7/LVDIN/RP12/RB12 |
| 6 | AN4/RP16/RB2 | 16 | TDI/AN8/RP13/RB13 |
| 7 | OSC1/CLKI/AN5/C1INB/RP3/OCM1C/RA2 | 17 | CDAC1/AN9/RP9/RTCC/U1TX/SDI1/C1OUT/INT1/RB14 |
| 8 | OSC2/CLKO/AN6/C1INA/RP4/OCM1D/RA3 ⁽¹⁾ | 18 | AN10/REFCLKO/RP10/U1RX/SS1/FSYNC1/INT0/RB15 ⁽¹⁾ |
| 9 | PGED3/SOSCI/RP5/RB4 | 19 | AVss/Vss |
| 10 | PGEC3/SOSCO/SCLKI/RP6/PWRLCLK/RA4 | 20 | AVDD/VDD |

Note 1: Pin has an increased current drive strength.

PIC32MM0064GPL036 FAMILY

Pin Diagrams (Continued)

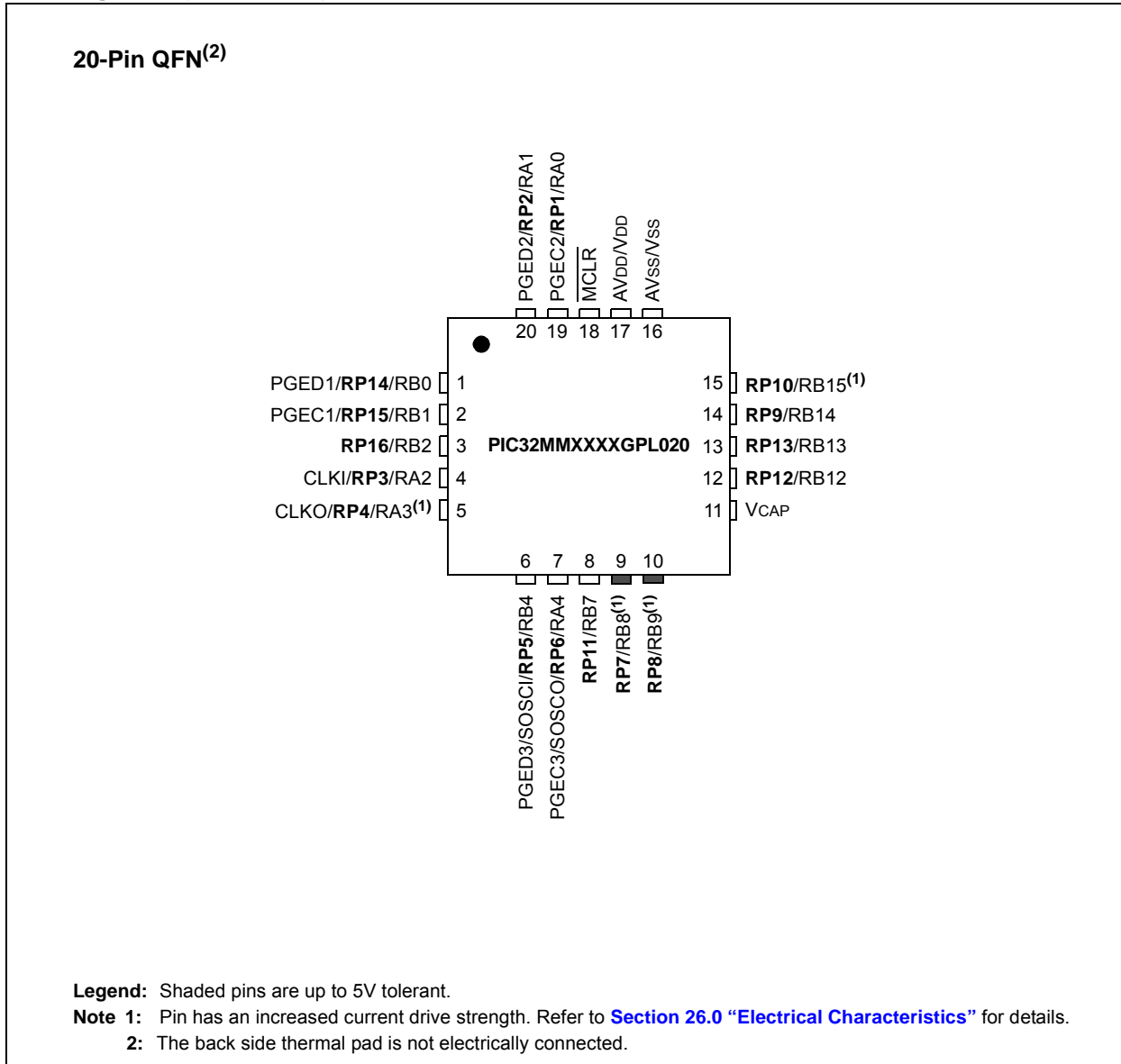


TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 20-PIN QFN DEVICES

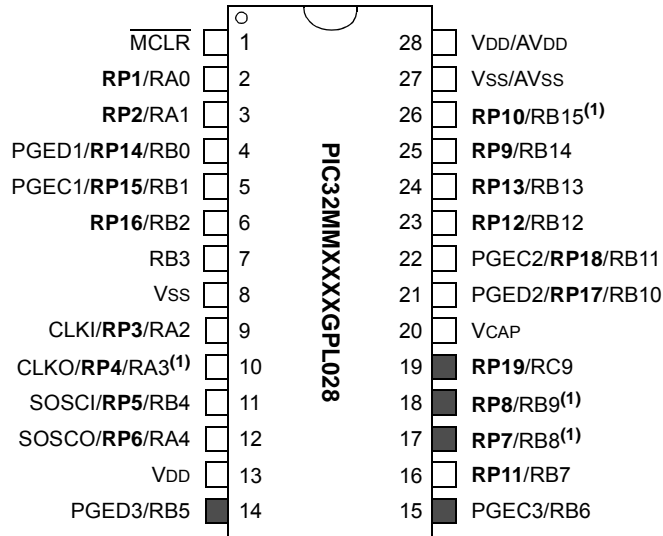
| Pin | Function | Pin | Function |
|-----|---|-----|---|
| 1 | PGED1/AN2/C1IND/C2INB/RP14/RB0 | 11 | VCAP |
| 2 | PGEC1/AN3/C1INC/C2INA/RP15/RB1 | 12 | TDO/AN7/LVDIN/RP12/RB12 |
| 3 | AN4/RP16/RB2 | 13 | TDI/AN8/RP13/RB13 |
| 4 | OSC1/CLKI/AN5/C1INB/RP3/OCM1C/RA2 | 14 | CDAC1/AN9/RP9/RTCC/U1TX/SDI1/C1OUT/IINT1/RB14 |
| 5 | OSC2/CLKO/AN6/C1INA/RP4/OCM1D/RA3 ⁽¹⁾ | 15 | AN10/REFCLKO/RP10/U1RX/SS1/FSYNC1/IINT0/RB15 ⁽¹⁾ |
| 6 | PGED3/SOSCI/RP5/RB4 | 16 | AVss/Vss |
| 7 | PGEC3/SOSCO/SCLKI/RP6/PWRLCLK/RA4 | 17 | AVDD/VDD |
| 8 | RP11/RB7 | 18 | MCLR |
| 9 | TCK/RP7/U1CTS/SCK1/OCM1A/RB8 ⁽¹⁾ | 19 | PGEC2/REF+/AN0/RP1/OCM1E/IINT3/RA0 |
| 10 | TMS/REFCLKI/RP8/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/IINT2/RB9 ⁽¹⁾ | 20 | PGED2/REF-/AN1/RP2/OCM1F/RA1 |

Note 1: Pin has an increased current drive strength.

PIC32MM0064GPL036 FAMILY

Pin Diagrams (Continued)

28-Pin SPDIP⁽²⁾/SSOP/SOIC



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to [Section 26.0 "Electrical Characteristics"](#) for details.

2: Only PIC32MM0064GPL028 comes in a 28-pin SPDIP package.

TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN SPDIP/SSOP/SOIC DEVICES

| Pin | Function | Pin | Function |
|-----|--|-----|--|
| 1 | MCLR | 15 | PGEC3/RB6 |
| 2 | VREF+/AN0/RP1/OCM1E/INT3/RA0 | 16 | RP11/RB7 |
| 3 | VREF-/AN1/RP2/OCM1F/RA1 | 17 | TCK/RP7/U1CTS/SCK1/OCM1A/RB8 ⁽¹⁾ |
| 4 | PGED1/AN2/C1IND/C2INB/RP14/RB0 | 18 | TMS/REFCLKI/RP8/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9 ⁽¹⁾ |
| 5 | PGEC1/AN3/C1INC/C2INA/RP15/RB1 | 19 | RP19/RC9 |
| 6 | AN4/C1INB/RP16/RB2 | 20 | VCAP |
| 7 | AN11/C1INA/RB3 | 21 | PGED2/TDO/RP17/RB10 |
| 8 | Vss | 22 | PGEC2/TDI/RP18/RB11 |
| 9 | OSC1/CLKI/AN5/RP3/OCM1C/RA2 | 23 | AN7/LVDIN/RP12/RB12 |
| 10 | OSC2/CLKO/AN6/RP4/OCM1D/RA3 ⁽¹⁾ | 24 | AN8/RP13/RB13 |
| 11 | SOSCI/RP5/RB4 | 25 | CDAC1/AN9/RP9/RTCC/U1TX/SDI1/C1OUT/INT1/RB14 |
| 12 | SOSCO/SCLKI/RP6/PWRLCLK/RA4 | 26 | AN10/REFCLKO/RP10/U1RX/SS1/FSYNC1/INT0/RB15 ⁽¹⁾ |
| 13 | VDD | 27 | Vss/AVss |
| 14 | PGED3/RB5 | 28 | VDD/AVDD |

Note 1: Pin has an increased current drive strength.

PIC32MM0064GPL036 FAMILY

Pin Diagrams (Continued)

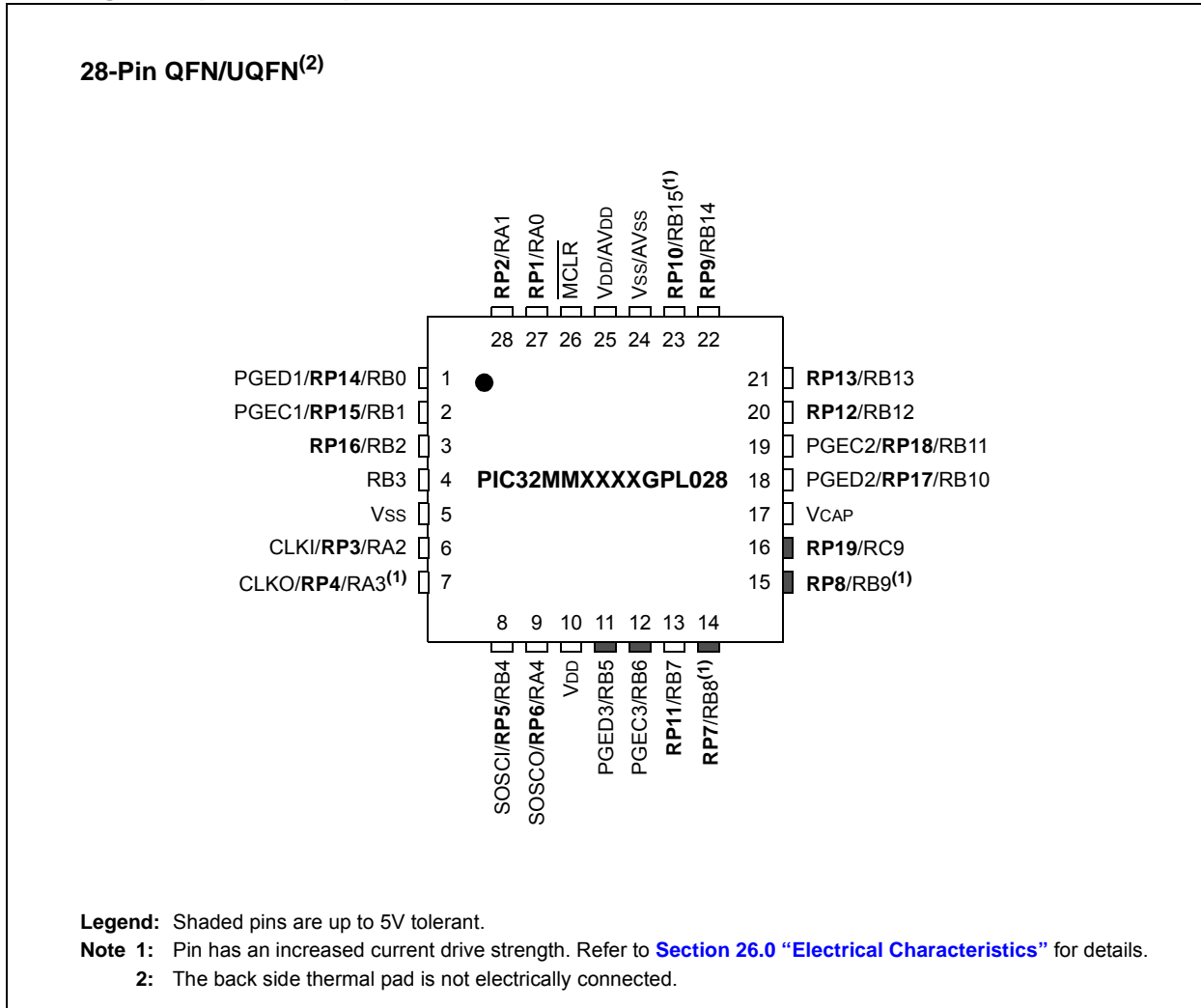


TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN QFN/UQFN DEVICES

| Pin | Function | Pin | Function |
|-----|--|-----|---|
| 1 | PGED1/AN2/C1IND/C2INB/ RP14 /RB0 | 15 | TMS/REFCLKI/ RP8 /T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9 ⁽¹⁾ |
| 2 | PGEC1/AN3/C1INC/C2INA/ RP15 /RB1 | 16 | RP19 /RC9 |
| 3 | AN4/C1INB/ RP16 /RB2 | 17 | VCAP |
| 4 | AN11/C1INA/RB3 | 18 | PGED2/TDO/ RP17 /RB10 |
| 5 | Vss | 19 | PGEC2/TDI/ RP18 /RB11 |
| 6 | OSC1/CLKI/AN5/ RP3 /OCM1C/RA2 | 20 | AN7/LVDIN/ RP12 /RB12 |
| 7 | OSC2/CLKO/AN6/ RP4 /OCM1D/RA3 ⁽¹⁾ | 21 | AN8/ RP13 /RB13 |
| 8 | SOSCI/ RP5 /RB4 | 22 | CDAC1/AN9/ RP9 /RTCC/U1TX/SDI1/C1OUT/INT1/RB14 |
| 9 | SOSCO/SCLKI/ RP6 /PWRLCLK/RA4 | 23 | AN10/REFCLKO/ RP10 /U1RX/ SS1 /FSYNC1/INT0/RB15 ⁽¹⁾ |
| 10 | VDD | 24 | Vss/AVss |
| 11 | PGED3/RB5 | 25 | VDD/AVDD |
| 12 | PGEC3/RB6 | 26 | MCLR |
| 13 | RP11 /RB7 | 27 | VREF+/AN0/ RP1 /OCM1E/INT3/RA0 |
| 14 | TCK/ RP7 /U1CTS/SCK1/OCM1A/RB8 ⁽¹⁾ | 28 | VREF-/AN1/ RP2 /OCM1F/RA1 |

Note 1: Pin has an increased current drive strength.

PIC32MM0064GPL036 FAMILY

Pin Diagrams (Continued)

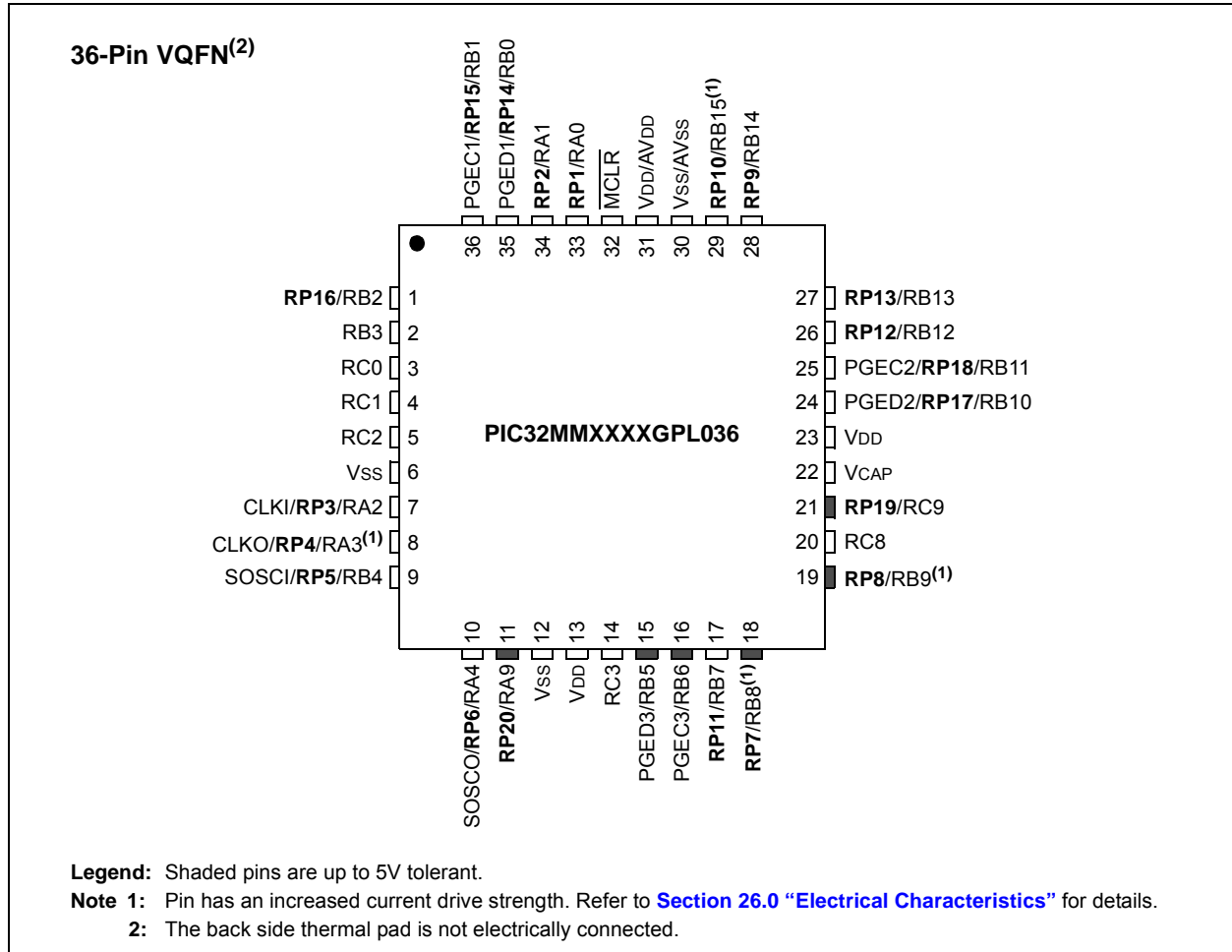


TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN VQFN DEVICES

| Pin | Function | Pin | Function |
|-----|---|-----|--|
| 1 | AN4/C1INB/RP16/RB2 | 19 | TMS/REFCLKI/RP8/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9 ⁽¹⁾ |
| 2 | AN11/C1INA/RB3 | 20 | RC8 |
| 3 | AN12/RC0 | 21 | RP19/RC9 |
| 4 | AN13/RC1 | 22 | VCAP |
| 5 | RC2 | 23 | VDD |
| 6 | Vss | 24 | PGED2/TDO/RP17/RB10 |
| 7 | OSC1/CLKI/AN5/RP3/OCM1C/RA2 | 25 | PGEC2/TDI/RP18/RB11 |
| 8 | OSC2/CLKO/AN6/RP4/OCM1D/RA3 ⁽¹⁾ | 26 | AN7/LVDIN/RP12/RB12 |
| 9 | SOSCI/RP5/RB4 | 27 | AN8/RP13/RB13 |
| 10 | SOSCO/SCLKI/RP6/PWRCLK/RA4 | 28 | CDAC1/AN9/RP9/RTCC/U1TX/SDI1/C1OUT/INT1/RB14 |
| 11 | RP20/RA9 | 29 | AN10/REFCLKO/RP10/U1RX/SS1/FSYNC1/INT0/RB15 ⁽¹⁾ |
| 12 | Vss | 30 | Vss/AVss |
| 13 | VDD | 31 | VDD/AVDD |
| 14 | RC3 | 32 | MCLR |
| 15 | PGED3/RB5 | 33 | VREF+/AN0/RP1/OCM1E/INT3/RA0 |
| 16 | PGEC3/RB6 | 34 | VREF-/AN1/RP2/OCM1F/RA1 |
| 17 | RP11/RB7 | 35 | PGED1/AN2/C1IND/C2INB/RP14/RB0 |
| 18 | TCK/RP7/U1CTS/SCK1/OCM1A/RB8 ⁽¹⁾ | 36 | PGEC1/AN3/C1INC/C2INA/RP15/RB1 |

Note 1: Pin has an increased current drive strength.

PIC32MM0064GPL036 FAMILY

Pin Diagrams (Continued)

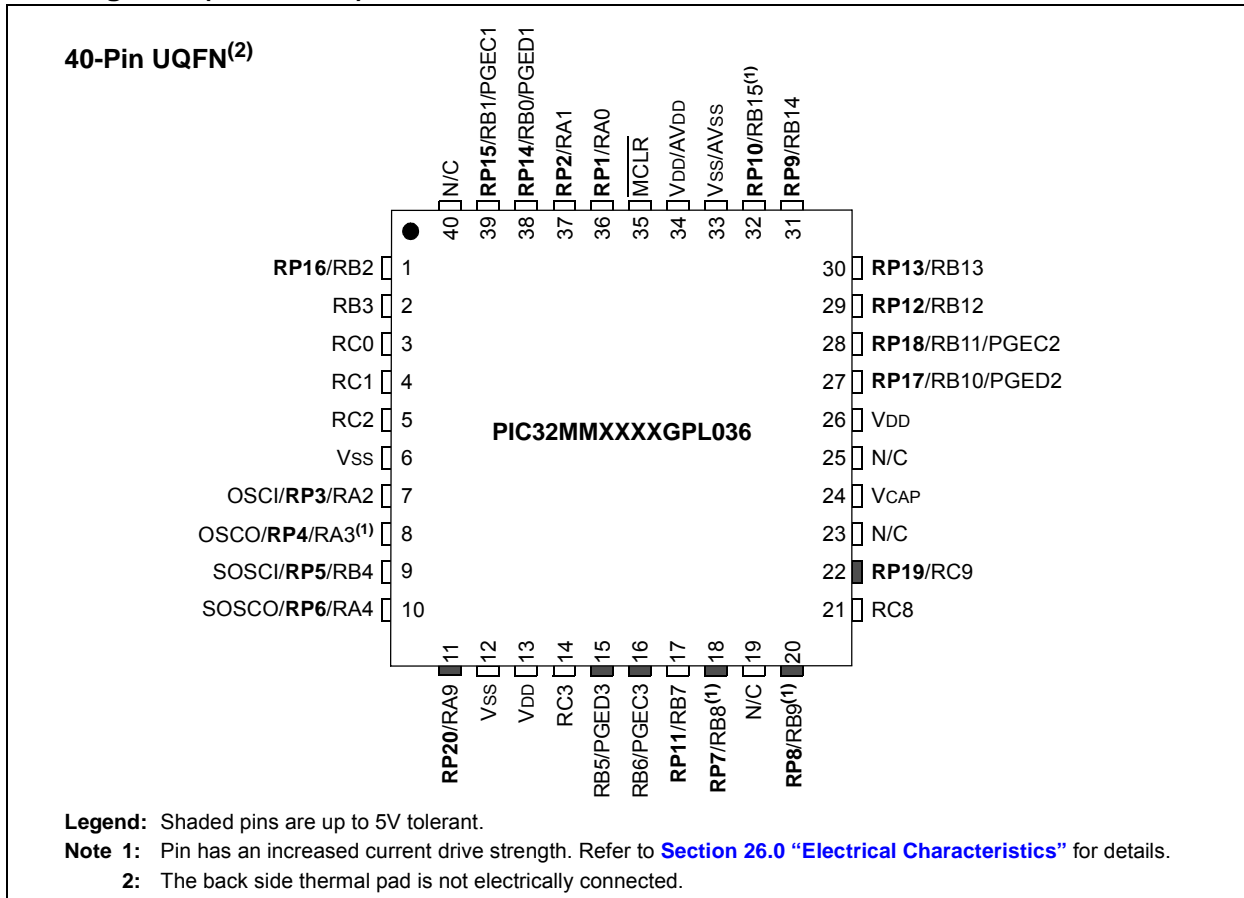


TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 40-PIN UQFN DEVICES

| Pin | Function | Pin | Function |
|-----|---|-----|---|
| 1 | AN4/C1INB/ RP16 /RB2 | 21 | RC8 |
| 2 | AN11/C1INA/RB3 | 22 | RP19 /RC9 |
| 3 | AN12/RC0 | 23 | N/C |
| 4 | AN13/RC1 | 24 | VCAP |
| 5 | RC2 | 25 | N/C |
| 6 | Vss | 26 | VDD |
| 7 | OSC1/CLKI/AN5/ RP3 /OCM1C/RA2 | 27 | PGED2/TDO/ RP17 /RB10 |
| 8 | OSC2/CLKO/AN6/ RP4 /OCM1D/RA3 ⁽¹⁾ | 28 | PGEC2/TDI/ RP18 /RB11 |
| 9 | SOSCI/ RP5 /RB4 | 29 | AN7/LVDIN/ RP12 /RB12 |
| 10 | SOSCO/SCLKI/ RP6 /PWRLCLK/RA4 | 30 | AN8/ RP13 /RB13 |
| 11 | RP20 /RA9 | 31 | CDAC1/AN9/ RP9 /RTCC/U1TX/SDI1/C1OUT/INT1/RB14 |
| 12 | Vss | 32 | AN10/REFCLKO/ RP10 /U1RX/SS1/FSYNC1/INT0/RB15 ⁽¹⁾ |
| 13 | VDD | 33 | Vss/AVss |
| 14 | RC3 | 34 | VDD/AVDD |
| 15 | PGED3/RB5 | 35 | MCLR |
| 16 | PGEC3/RB6 | 36 | VREF+/AN0/ RP1 /OCM1E/INT3/RA0 |
| 17 | RP11 /RB7 | 37 | VREF-/AN1/ RP2 /OCM1F/RA1 |
| 18 | TCK/ RP7 /U1CTS/SCK1/OCM1A/RB8 ⁽¹⁾ | 38 | PGED1/AN2/C1IND/C2INB/ RP14 /RB0 |
| 19 | N/C | 39 | PGEC1/AN3/C1INC/C2INA/ RP15 /RB1 |
| 20 | TMS/REFCLKI/ RP8 /T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9 ⁽¹⁾ | 40 | N/C |

Note 1: Pin has an increased current drive strength.

PIC32MM0064GPL036 FAMILY

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PIC32MM0064GPL036 FAMILY

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Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

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Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 5. "Flash Programming"** (DS60001121)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupts"** (DS60001108)
- **Section 10. "Power-Saving Modes"** (DS60001130)
- **Section 14. "Timers"** (DS60001105)
- **Section 19. "Comparator"** (DS60001110)
- **Section 21. "UART"** (DS60001107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 25. "12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect"** (DS60001359)
- **Section 28. "RTCC with Timestamp"** (DS60001362)
- **Section 30. "Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS60001381)
- **Section 33. "Programming and Diagnostics"** (DS61129)
- **Section 36. "Configurable Logic Cell"** (DS60001363)
- **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327)
- **Section 50. "CPU for Devices with MIPS32[®] microAptiv[™] and M-Class Cores"** (DS60001192)
- **Section 59. "Oscillators with DCO"** (DS60001329)
- **Section 60. "32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS60001336)
- **Section 62. "Dual Watchdog Timer"** (DS60001365)

PIC32MM0064GPL036 FAMILY

NOTES:

PIC32MM0064GPL036 FAMILY

1.0 DEVICE OVERVIEW

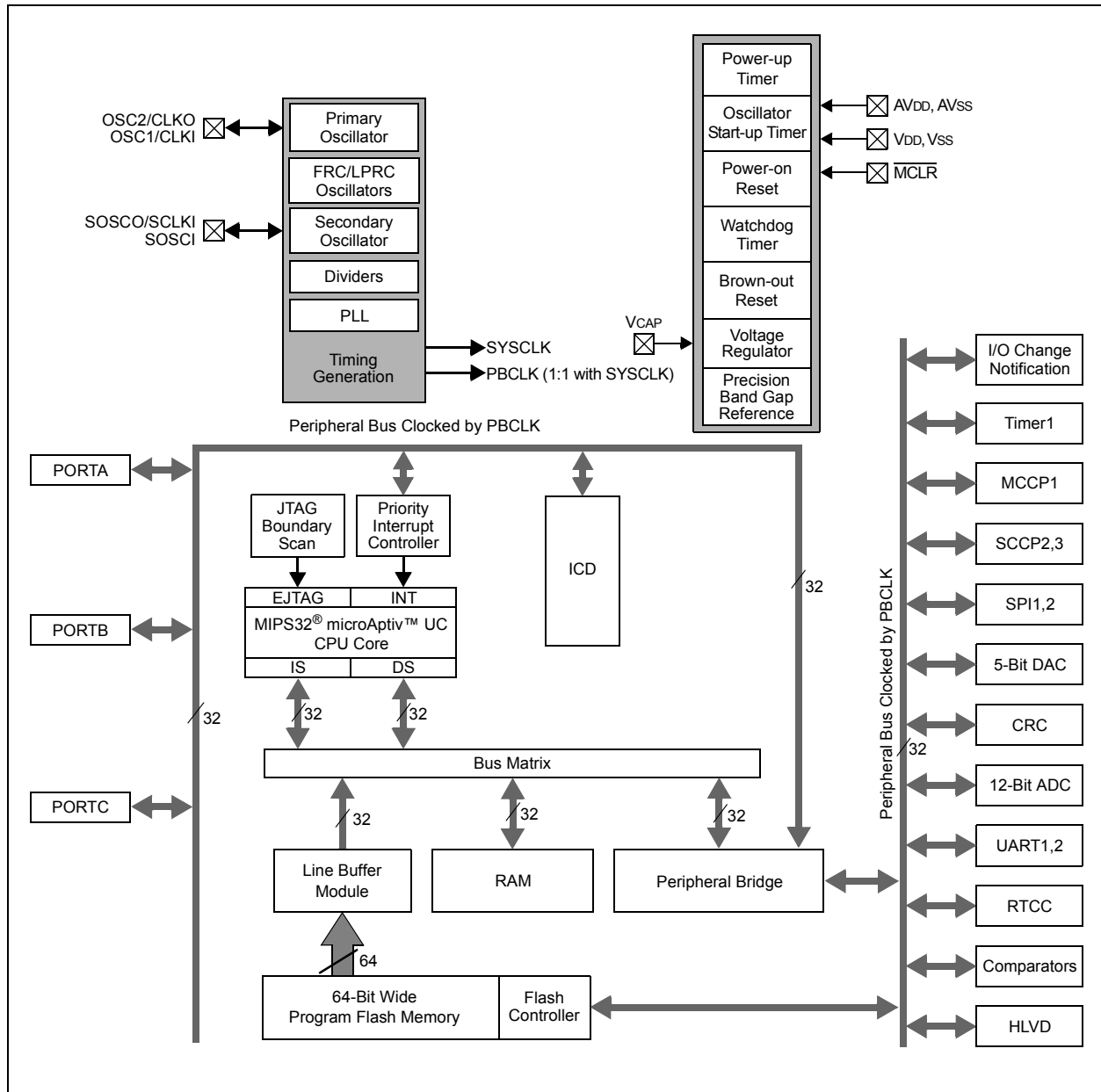
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0064GPL036 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0064GPL036 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0064GPL036 FAMILY BLOCK DIAGRAM



PIC32MM0064GPL036 FAMILY

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION

| Pin Name | Pin Number | | | | | | Pin Type | Buffer Type | Description |
|----------|------------|-------------|------------------|-------------------------|-------------|-------------|----------|-------------|--|
| | 20-Pin QFN | 20-Pin SSOP | 28-Pin QFN/ UQFN | 28-Pin SPDIP/ SSOP/SOIC | 36-Pin VQFN | 40-Pin UQFN | | | |
| AN0 | 19 | 2 | 27 | 2 | 33 | 36 | I | ANA | Analog-to-Digital Converter input channels |
| AN1 | 20 | 3 | 28 | 3 | 34 | 37 | I | ANA | |
| AN2 | 1 | 4 | 1 | 4 | 35 | 38 | I | ANA | |
| AN3 | 2 | 5 | 2 | 5 | 36 | 39 | I | ANA | |
| AN4 | 3 | 6 | 3 | 6 | 1 | 1 | I | ANA | |
| AN5 | 4 | 7 | 6 | 9 | 7 | 7 | I | ANA | |
| AN6 | 5 | 8 | 7 | 10 | 8 | 8 | I | ANA | |
| AN7 | 12 | 15 | 20 | 23 | 26 | 29 | I | ANA | |
| AN8 | 13 | 16 | 21 | 24 | 27 | 30 | I | ANA | |
| AN9 | 14 | 17 | 22 | 25 | 28 | 31 | I | ANA | |
| AN10 | 15 | 18 | 23 | 26 | 29 | 32 | I | ANA | |
| AN11 | — | — | 4 | 7 | 2 | 2 | I | ANA | |
| AN12 | — | — | — | — | 3 | 3 | I | ANA | |
| AN13 | — | — | — | — | 4 | 4 | I | ANA | |
| AVDD | 17 | 20 | 25 | 28 | 31 | 34 | P | — | Analog modules power supply ⁽¹⁾ |
| AVSS | 16 | 19 | 24 | 27 | 30 | 33 | P | — | Analog modules ground ⁽²⁾ |
| C1INA | 5 | 8 | 4 | 7 | 2 | 2 | I | ANA | Comparator 1 Input A |
| C1INB | 4 | 7 | 3 | 6 | 1 | 1 | I | ANA | Comparator 1 Input B |
| C1INC | 2 | 5 | 2 | 5 | 36 | 39 | I | ANA | Comparator 1 Input C |
| C1IND | 1 | 4 | 1 | 4 | 35 | 38 | I | ANA | Comparator 1 Input D |
| C1OUT | 14 | 17 | 22 | 25 | 28 | 31 | O | DIG | Comparator 1 output |
| C2INA | 2 | 5 | 2 | 5 | 36 | 39 | I | ANA | Comparator 2 Input A |
| C2INB | 1 | 4 | 1 | 4 | 35 | 38 | I | ANA | Comparator 2 Input B |
| C2OUT | 10 | 13 | 15 | 18 | 19 | 20 | O | DIG | Comparator 2 output |
| CLKI | 4 | 7 | 6 | 9 | 7 | 7 | I | ST | External Clock input (EC mode) |
| CLKO | 5 | 8 | 7 | 10 | 8 | 8 | O | DIG | System clock output |
| CDAC1 | 14 | 17 | 22 | 25 | 28 | 31 | O | ANA | Digital-to-Analog Converter output |
| FSYNC1 | 15 | 18 | 23 | 26 | 29 | 32 | I/O | ST/DIG | SPI1 frame signal input or output |
| INT0 | 15 | 18 | 23 | 26 | 29 | 32 | I | ST | External Interrupt 0 |
| INT1 | 14 | 17 | 22 | 25 | 28 | 31 | I | ST | External Interrupt 1 |
| INT2 | 10 | 13 | 15 | 18 | 19 | 20 | I | ST | External Interrupt 2 |
| INT3 | 19 | 2 | 27 | 2 | 33 | 36 | I | ST | External Interrupt 3 |
| LVDIN | 12 | 15 | 20 | 23 | 26 | 29 | I | ANA | High/Low-Voltage Detect input |
| MCLR | 18 | 1 | 26 | 1 | 32 | 35 | I | ST | Master Clear (device Reset) |
| OCM1A | 9 | 12 | 14 | 17 | 18 | 18 | O | DIG | MCCP1 Output A |
| OCM1B | 10 | 13 | 15 | 18 | 19 | 20 | O | DIG | MCCP1 Output B |
| OCM1C | 4 | 7 | 6 | 9 | 7 | 7 | O | DIG | MCCP1 Output C |
| OCM1D | 5 | 8 | 7 | 10 | 8 | 8 | O | DIG | MCCP1 Output D |
| OCM1E | 19 | 2 | 27 | 2 | 33 | 36 | O | DIG | MCCP1 Output E |
| OCM1F | 20 | 3 | 28 | 3 | 34 | 37 | O | DIG | MCCP1 Output F |
| OSC1 | 4 | 7 | 6 | 9 | 7 | 7 | — | — | Primary Oscillator crystal |
| OSC2 | 5 | 8 | 7 | 10 | 8 | 8 | — | — | Primary Oscillator crystal |

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

Note 1: VDD and AVDD are internally connected.

2: Vss and AVss are internally connected.

PIC32MM0064GPL036 FAMILY

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

| Pin Name | Pin Number | | | | | | Pin Type | Buffer Type | Description |
|----------|------------|-------------|-----------------|------------------------|-------------|-------------|----------|-------------|--------------------------------------|
| | 20-Pin QFN | 20-Pin SSOP | 28-Pin QFN/UQFN | 28-Pin SPDIP/SSOP/SOIC | 36-Pin VQFN | 40-Pin UQFN | | | |
| PGEC1 | 2 | 5 | 2 | 5 | 36 | 39 | I | ST | ICSP™ Port 1 programming clock input |
| PGEC2 | 19 | 2 | 19 | 22 | 25 | 28 | I | ST | ICSP Port 2 programming clock input |
| PGEC3 | 7 | 10 | 12 | 15 | 16 | 16 | I | ST | ICSP Port 3 programming clock input |
| PGED1 | 1 | 4 | 1 | 4 | 35 | 38 | I/O | ST/DIG | ICSP Port 1 programming data |
| PGED2 | 20 | 3 | 18 | 21 | 24 | 27 | I/O | ST/DIG | ICSP Port 2 programming data |
| PGED3 | 6 | 9 | 11 | 14 | 15 | 15 | I/O | ST/DIG | ICSP Port 3 programming data |
| PWRLCLK | 7 | 10 | 9 | 12 | 10 | 10 | I | ST | Real-Time Clock 50/60 Hz clock input |
| RA0 | 19 | 2 | 27 | 2 | 33 | 36 | I/O | ST/DIG | PORTA digital I/O |
| RA1 | 20 | 3 | 28 | 3 | 34 | 37 | I/O | ST/DIG | PORTA digital I/O |
| RA2 | 4 | 7 | 6 | 9 | 7 | 7 | I/O | ST/DIG | PORTA digital I/O |
| RA3 | 5 | 8 | 7 | 10 | 8 | 8 | I/O | ST/DIG | PORTA digital I/O |
| RA4 | 7 | 10 | 9 | 12 | 10 | 10 | I/O | ST/DIG | PORTA digital I/O |
| RA9 | — | — | — | — | 11 | 11 | I/O | ST/DIG | PORTA digital I/O |
| RB0 | 1 | 4 | 1 | 4 | 35 | 38 | I/O | ST/DIG | PORTB digital I/O |
| RB1 | 2 | 5 | 2 | 5 | 36 | 39 | I/O | ST/DIG | PORTB digital I/O |
| RB2 | 3 | 6 | 3 | 6 | 1 | 1 | I/O | ST/DIG | PORTB digital I/O |
| RB3 | — | — | 4 | 7 | 2 | 2 | I/O | ST/DIG | PORTB digital I/O |
| RB4 | 6 | 9 | 8 | 11 | 9 | 9 | I/O | ST/DIG | PORTB digital I/O |
| RB5 | — | — | 11 | 14 | 15 | 15 | I/O | ST/DIG | PORTB digital I/O |
| RB6 | — | — | 12 | 15 | 16 | 16 | I/O | ST/DIG | PORTB digital I/O |
| RB7 | 8 | 11 | 13 | 16 | 17 | 17 | I/O | ST/DIG | PORTB digital I/O |
| RB8 | 9 | 12 | 14 | 17 | 18 | 18 | I/O | ST/DIG | PORTB digital I/O |
| RB9 | 10 | 13 | 15 | 18 | 19 | 20 | I/O | ST/DIG | PORTB digital I/O |
| RB10 | — | — | 18 | 21 | 24 | 27 | I/O | ST/DIG | PORTB digital I/O |
| RB11 | — | — | 19 | 22 | 25 | 28 | I/O | ST/DIG | PORTB digital I/O |
| RB12 | 12 | 15 | 20 | 23 | 26 | 29 | I/O | ST/DIG | PORTB digital I/O |
| RB13 | 13 | 16 | 21 | 24 | 27 | 30 | I/O | ST/DIG | PORTB digital I/O |
| RB14 | 14 | 17 | 22 | 25 | 28 | 31 | I/O | ST/DIG | PORTB digital I/O |
| RB15 | 15 | 18 | 23 | 26 | 29 | 32 | I/O | ST/DIG | PORTB digital I/O |
| RC0 | — | — | — | — | 3 | 3 | I/O | ST/DIG | PORTC digital I/O |
| RC1 | — | — | — | — | 4 | 4 | I/O | ST/DIG | PORTC digital I/O |
| RC2 | — | — | — | — | 5 | 5 | I/O | ST/DIG | PORTC digital I/O |
| RC3 | — | — | — | — | 14 | 14 | I/O | ST/DIG | PORTC digital I/O |
| RC8 | — | — | — | — | 20 | 21 | I/O | ST/DIG | PORTC digital I/O |
| RC9 | — | — | 16 | 19 | 21 | 22 | I/O | ST/DIG | PORTC digital I/O |
| REFCLKI | 10 | 13 | 15 | 18 | 19 | 20 | I | ST | Reference clock input |
| REFCLKO | 15 | 18 | 23 | 26 | 29 | 32 | O | DIG | Reference clock output |

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

Note 1: VDD and AVDD are internally connected.

2: VSS and AVSS are internally connected.

PIC32MM0064GPL036 FAMILY

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

| Pin Name | Pin Number | | | | | | Pin Type | Buffer Type | Description |
|----------|------------|-------------|------------------|-------------------------|-------------|-------------|----------|-------------|---|
| | 20-Pin QFN | 20-Pin SSOP | 28-Pin QFN/ UQFN | 28-Pin SPDIP/ SSOP/SOIC | 36-Pin VQFN | 40-Pin UQFN | | | |
| RP1 | 19 | 2 | 27 | 2 | 33 | 36 | I/O | ST/DIG | Remappable peripherals (input or output) |
| RP2 | 20 | 3 | 28 | 3 | 34 | 37 | I/O | ST/DIG | |
| RP3 | 4 | 7 | 6 | 9 | 7 | 7 | I/O | ST/DIG | |
| RP4 | 5 | 8 | 7 | 10 | 8 | 8 | I/O | ST/DIG | |
| RP5 | 6 | 9 | 8 | 11 | 9 | 9 | I/O | ST/DIG | |
| RP6 | 7 | 10 | 9 | 12 | 10 | 10 | I/O | ST/DIG | |
| RP7 | 9 | 12 | 14 | 17 | 18 | 18 | I/O | ST/DIG | |
| RP8 | 10 | 13 | 15 | 18 | 19 | 20 | I/O | ST/DIG | |
| RP9 | 14 | 17 | 22 | 25 | 28 | 31 | I/O | ST/DIG | |
| RP10 | 15 | 18 | 23 | 26 | 29 | 32 | I/O | ST/DIG | |
| RP11 | 8 | 11 | 13 | 16 | 17 | 17 | I/O | ST/DIG | |
| RP12 | 12 | 15 | 20 | 23 | 26 | 29 | I/O | ST/DIG | |
| RP13 | 13 | 16 | 21 | 24 | 27 | 30 | I/O | ST/DIG | |
| RP14 | 1 | 4 | 1 | 4 | 35 | 38 | I/O | ST/DIG | |
| RP15 | 2 | 5 | 2 | 5 | 36 | 39 | I/O | ST/DIG | |
| RP16 | 3 | 6 | 3 | 6 | 1 | 1 | I/O | ST/DIG | |
| RP17 | — | — | 18 | 21 | 24 | 27 | I/O | ST/DIG | |
| RP18 | — | — | 19 | 22 | 25 | 28 | I/O | ST/DIG | |
| RP19 | — | — | 16 | 19 | 21 | 22 | I/O | ST/DIG | |
| RP20 | — | — | — | — | 11 | 11 | I/O | ST/DIG | |
| RTCC | 14 | 17 | 22 | 25 | 28 | 31 | O | DIG | Real-Time Clock alarm/seconds output |
| SCK1 | 9 | 12 | 14 | 17 | 18 | 18 | I/O | ST/DIG | SPI1 clock (input or output) |
| SCLKI | 7 | 10 | 9 | 12 | 10 | 10 | I | ST | Secondary Oscillator external clock input |
| SDI1 | 14 | 17 | 22 | 25 | 28 | 31 | I | ST | SPI1 data input |
| SDO1 | 10 | 13 | 15 | 18 | 19 | 20 | O | DIG | SPI1 data output |
| SOSCI | 6 | 9 | 8 | 11 | 9 | 9 | — | — | Secondary Oscillator crystal |
| SOSCO | 7 | 10 | 9 | 12 | 10 | 10 | — | — | Secondary Oscillator crystal |
| SS1 | 15 | 18 | 23 | 26 | 29 | 32 | I | ST | SPI1 slave select input |
| T1CK | 10 | 13 | 15 | 18 | 19 | 20 | I | ST | Timer1 external clock input |
| T1G | 10 | 13 | 15 | 18 | 19 | 20 | I | ST | Timer1 clock gate input |
| TCK | 9 | 12 | 14 | 17 | 18 | 18 | I | ST | JTAG clock input |
| TDI | 13 | 16 | 19 | 22 | 25 | 28 | I | ST | JTAG data input |
| TDO | 12 | 15 | 18 | 21 | 24 | 27 | O | DIG | JTAG data output |
| TMS | 10 | 13 | 15 | 18 | 19 | 20 | I | ST | JTAG mode select input |
| U1BCLK | 10 | 13 | 15 | 18 | 19 | 20 | O | DIG | UART1 IrDA® 16x baud clock output |
| U1CTS | 9 | 12 | 14 | 17 | 18 | 18 | I | ST | UART1 transmission control input |
| U1RTS | 10 | 13 | 15 | 18 | 19 | 20 | O | DIG | UART1 reception control output |
| U1RX | 15 | 18 | 23 | 26 | 29 | 32 | I | ST | UART1 receive data input |
| U1TX | 14 | 17 | 22 | 25 | 28 | 31 | O | DIG | UART1 transmit data output |

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

Note 1: VDD and AVDD are internally connected.

2: VSS and AVSS are internally connected.

PIC32MM0064GPL036 FAMILY

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

| Pin Name | Pin Number | | | | | | Pin Type | Buffer Type | Description |
|----------|------------|-------------|-----------------|------------------------|-------------|-------------|----------|-------------|--|
| | 20-Pin QFN | 20-Pin SSOP | 28-Pin QFN/UQFN | 28-Pin SPDIP/SSOP/SOIC | 36-Pin VQFN | 40-Pin UQFN | | | |
| VCAP | 11 | 14 | 17 | 20 | 22 | 24 | P | — | Core voltage regulator filter capacitor connection |
| VDD | 17 | 20 | 10,25 | 13,28 | 13,23,31 | 13,26,34 | P | — | Digital modules power supply ⁽¹⁾ |
| VREF- | 20 | 3 | 28 | 3 | 34 | 37 | I | ANA | ADC negative reference |
| VREF+ | 19 | 2 | 27 | 2 | 33 | 36 | I | ANA | ADC and DAC positive reference |
| VSS | 16 | 19 | 5,24 | 8,27 | 6,12,30 | 6,12,33 | P | — | Digital modules ground ⁽²⁾ |

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output
Note 1: VDD and AVDD are internally connected.
2: VSS and AVSS are internally connected.

PIC32MM0064GPL036 FAMILY

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

2.1 Basic Connection Requirements

Getting started with the PIC32MM0064GPL036 family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see [Section 2.2 “Decoupling Capacitors”](#))
- All AVDD and AVSS pins, even if the ADC module is not used (see [Section 2.2 “Decoupling Capacitors”](#))
- MCLR pin (see [Section 2.3 “Master Clear \(MCLR\) Pin”](#))
- VCAP pin (see [Section 2.4 “Capacitor on Internal Voltage Regulator \(VCAP\)”](#))
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see [Section 2.6 “ICSP Pins”](#))
- OSC1 and OSC2 pins, when external oscillator source is used (see [Section 2.8 “External Oscillator Pins”](#))

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source. The back side thermal pad, if present, is not electrically connected.

2.2 Decoupling Capacitors

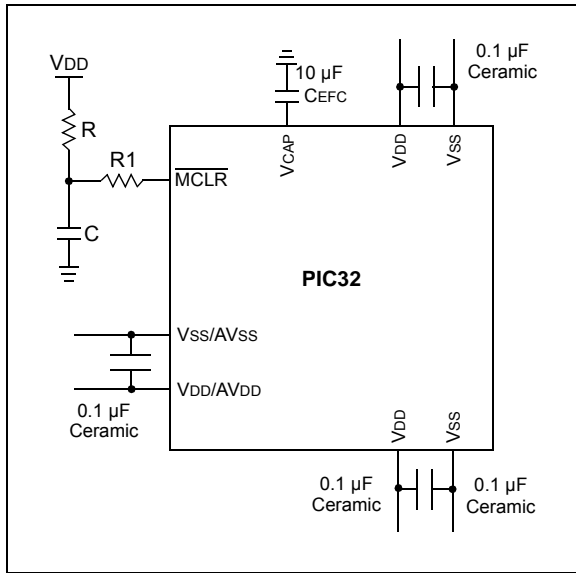
The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS, is required. See [Figure 2-1](#).

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 μF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances, as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

PIC32MM0064GPL036 FAMILY

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

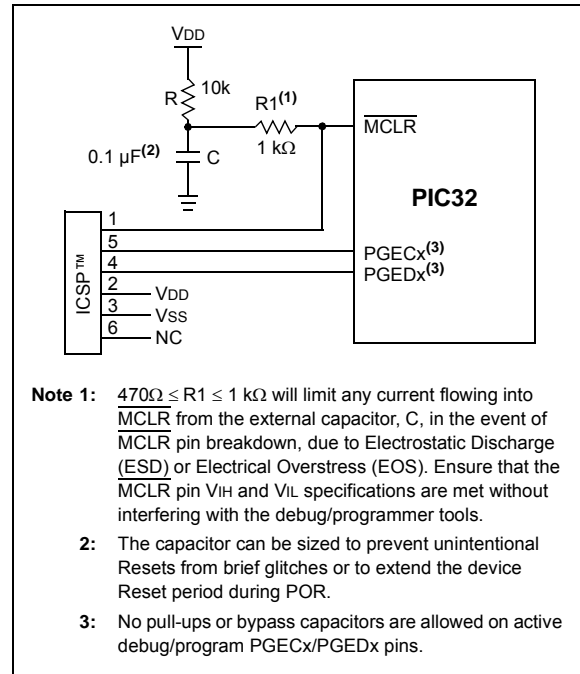
- Device Reset
- Device Programming and Debugging

Pulling the MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS^(1,2,3)



2.4 Capacitor on Internal Voltage Regulator (VCAP)

A low-ESR (<1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. The recommended value of the CEFC capacitor is 10 µF. On the printed circuit board, it should be placed as close to the VCAP pin as possible. If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to this capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF.

PIC32MM0064GPL036 FAMILY

2.5 Voltage Regulator Pin (VCAP)

A low-ESR ($< 5\Omega$) capacitor is required on the VCAP pin to stabilize the output voltage of the on-chip voltage regulator. The VCAP pin must not be connected to VDD and must use a capacitor of $10\ \mu\text{F}$ connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to Section 26.0 “Electrical Characteristics” for additional information.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP

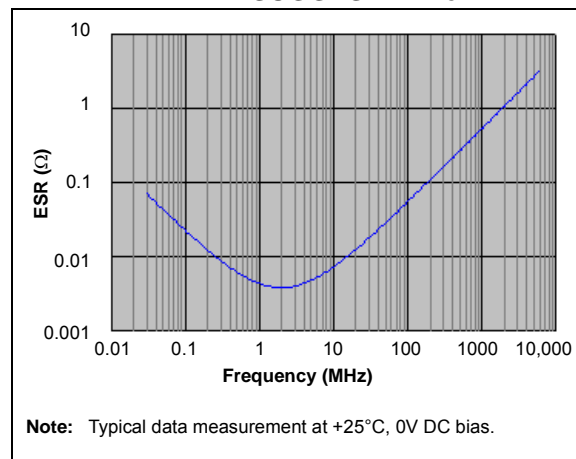


TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

| Make | Part # | Nominal Capacitance | Base Tolerance | Rated Voltage | Temp. Range |
|-----------|--------------------|---------------------|----------------|---------------|---------------|
| TDK | C3216X7R1C106K | $10\ \mu\text{F}$ | $\pm 10\%$ | 16V | -55 to +125°C |
| TDK | C3216X5R1C106K | $10\ \mu\text{F}$ | $\pm 10\%$ | 16V | -55 to +85°C |
| Panasonic | ECJ-3YX1C106K | $10\ \mu\text{F}$ | $\pm 10\%$ | 16V | -55 to +125°C |
| Panasonic | ECJ-4YB1C106K | $10\ \mu\text{F}$ | $\pm 10\%$ | 16V | -55 to +85°C |
| Murata | GRM319R61C106KE15D | $10\ \mu\text{F}$ | $\pm 10\%$ | 16V | -55 to +85°C |

PIC32MM0064GPL036 FAMILY

2.6 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Input Voltage High (VIH) and Input Voltage Low (VIL) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™ In-Circuit Emulator.

For more information on MPLAB ICD 3 and REAL ICE connection requirements, refer to the following documents that are available from the Microchip web site.

- “Using MPLAB® ICD 3 In-Circuit Debugger” (poster) (DS51765)
- “Development Tools Design Advisory” (DS51764)
- “MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide” (DS51616)
- “Using MPLAB® REAL ICE™ In-Circuit Emulator” (poster) (DS51749)

2.7 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector, and the JTAG pins on the device, as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

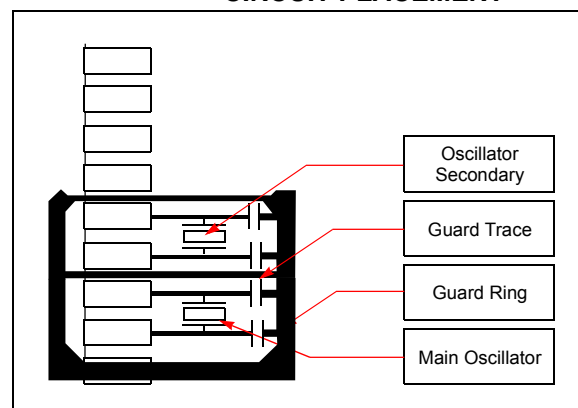
Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin Input Voltage High (VIH) and Input Voltage Low (VIL) requirements.

2.8 External Oscillator Pins

The PIC32MM0064GPL036 family has options for two external oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to [Section 8.0 “Oscillator Configuration”](#) for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in [Figure 2-4](#).

FIGURE 2-4: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.9 Unused I/Os

To minimize power consumption, unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic low or logic high state.

Alternatively, inputs can be reserved by ensuring the pin is always configured as an input and externally connecting the pin to Vss or VDD. A current-limiting resistor may be used to create this connection if there is any risk of inadvertently configuring the pin as an output with the logic output state opposite of the chosen power rail.

3.0 CPU

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. “CPU for Devices with MIPS32[®] microAptiv[™] and M-Class Cores”** (DS60001192) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). MIPS32[®] microAptiv[™] UC microprocessor core resources are available at: www.imgtec.com. The information in this data sheet supersedes the information in the FRM.

The MIPS32[®] microAptiv[™] UC microprocessor core is the heart of the PIC32MM0064GPL036 family devices. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of the instruction execution to the proper destinations.

3.1 Features

The PIC32MM0064GPL036 family processor core key features include:

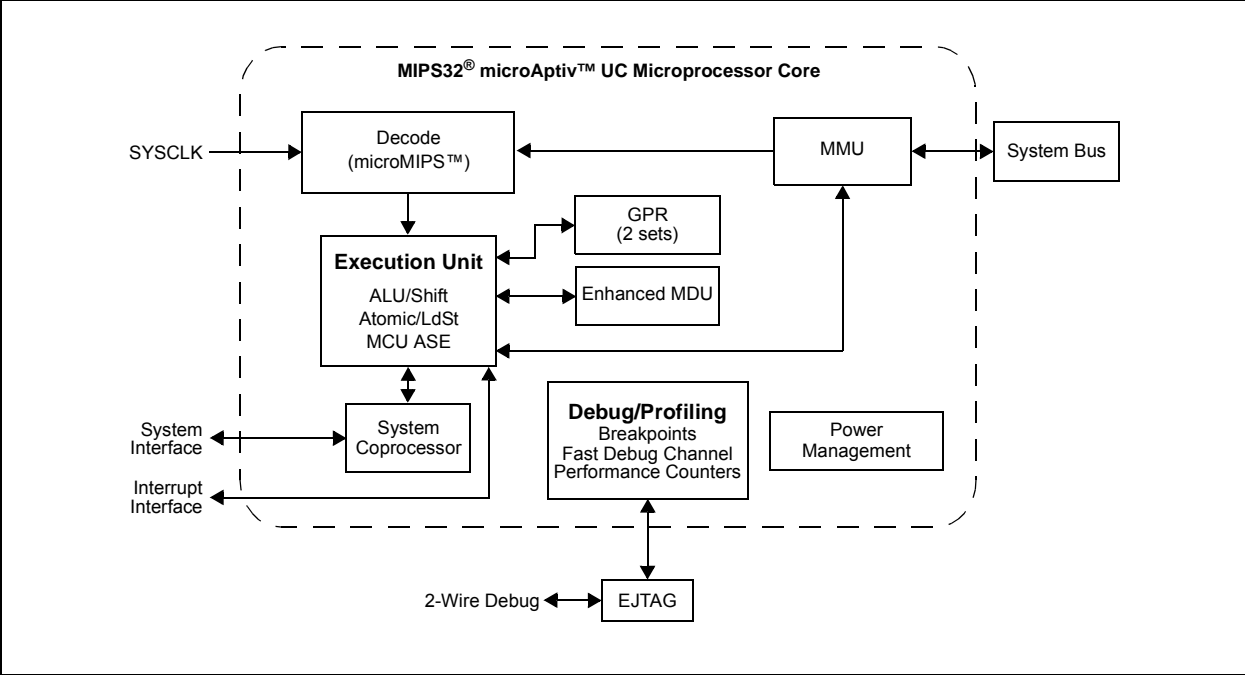
- 5-Stage Pipeline
- 32-Bit Address and Data Paths
- MIPS32 Enhanced Architecture:
 - Multiply-add and multiply-subtract instructions
 - Targeted multiply instruction
 - Zero and one detect instructions
 - WAIT instruction
 - Conditional move instructions
 - Vectored interrupts
 - Atomic interrupt enable/disable
 - One GPR shadow set to minimize latency of interrupts
 - Bit field manipulation instructions
- microMIPS[™] Instruction Set:
 - microMIPS allows improving the code size density over MIPS32, while maintaining MIPS32 performance.
 - microMIPS supports all MIPS32 instructions (except for branch-likely instructions) with new optimized 32-bit encoding. Frequent MIPS32 instructions are available as 16-bit instructions.
 - Added seventeen new and thirty-five MIPS32[®] corresponding commonly used instructions in 16-bit opcode format.
 - Stack Pointer implicit in instruction.
 - MIPS32 assembly and ABI compatible.

- Memory Management Unit with Simple Fixed Mapping Translation (FMT) Mechanism
- Multiply/Divide Unit (MDU):
 - Configurable using high-performance multiplier array.
 - Maximum issue rate of one 32x16 multiply per clock.
 - Maximum issue rate of one 32x32 multiply every other clock.
 - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension dependent).
- Power Control:
 - No minimum frequency: 0 MHz.
 - Power-Down mode (triggered by WAIT instruction).
- EJTAG Debug/Profiling:
 - CPU control with start, stop and single stepping.
 - Software breakpoints via the SDBBP instruction.
 - Optional simple hardware breakpoints on virtual addresses, 4 instruction and 2 data breakpoints.
 - PC and/or load/store address sampling for profiling.
 - Performance counters.
 - Supports Fast Debug Channel (FDC).

A block diagram of the PIC32MM0064GPL036 family processor core is shown in [Figure 3-1](#).

PIC32MM0064GPL036 FAMILY

FIGURE 3-1: PIC32MM0064GPL036 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



PIC32MM0064GPL036 FAMILY

3.2 Architecture Overview

The MIPS32[®] microAptiv™ UC microprocessor core in the PIC32MM0064GPL036 family devices contains several logic blocks, working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Memory Management Unit (MMU)
- Power Management
- microMIPS Instructions Decoder
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous Multiply/Divide Unit (MDU). The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid Stalls when executing instruction streams where data producing instructions are followed closely by consumers for their results
- Leading zero/one detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The microAptiv UC core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows the long-running MDU operations to be partially masked by system Stalls and/or other Integer Unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, Result/Accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the rs operand. The second number ('16' of 32x16) represents the rt operand. The microAptiv UC core only checks the value of the rt operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back, 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU. Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (rs) operand. If rs is 8 bits wide, 23 iterations are skipped. For a 16-bit wide rs, 15 iterations are skipped, and for a 24-bit wide rs, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline Stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be re-issued), and latency (number of cycles until a result is available) for the microAptiv UC core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

| Opcode | Operand Size (mul <i>rt</i>) (div <i>rs</i>) | Latency | Repeat Rate |
|------------------------------------|--|---------|-------------|
| MULT/MULTU, MADD/MADDU, MSUB/MSUBU | 16 bits | 1 | 1 |
| | 32 bits | 2 | 2 |
| MUL (GPR destination) | 16 bits | 2 | 1 |
| | 32 bits | 3 | 2 |
| DIV/DIVU | 8 bits | 12 | 11 |
| | 16 bits | 19 | 18 |
| | 24 bits | 26 | 25 |
| | 32 bits | 33 | 32 |

PIC32MM0064GPL036 FAMILY

The MIPS® architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS architecture also defines a Multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. These configuration options and other system information is available by accessing the CP0 registers listed in [Table 3-2](#).

PIC32MM0064GPL036 FAMILY

TABLE 3-2: COPROCESSOR 0 REGISTERS

| Register Number | Register Name | Function |
|-----------------|--|---|
| 0-3 | Reserved | Reserved in the microAptiv™ UC. |
| 4 | UserLocal | User information that can be written by privileged software and read via RDHWR, Register 29. |
| 5-6 | Reserved | Reserved in the microAptiv UC. |
| 7 | HWREna | Enables access via the RDHWR instruction to selected hardware registers in Non-Privileged mode. |
| 8 | BadVAddr ⁽¹⁾ | Reports the address for the most recent address related exception. |
| 9 | Count ⁽¹⁾ | Processor cycle count. |
| 10 | Reserved | Reserved in the microAptiv UC. |
| 11 | Compare ⁽¹⁾ | Timer interrupt control. |
| 12 | Status/ IntCtl/ SRSCtl/ SRSMAP1/ View_IPL/ SRSMAP2 | Processor status and control; interrupt control and shadow set control. |
| 13 | Cause ⁽¹⁾ / View_RIPL | Cause of last exception. |
| 14 | EPC ⁽¹⁾ | Program Counter at last exception. |
| 15 | PRId/ EBase/ CDMMBase | Processor identification and revision; exception base address; Common Device Memory Map Base register. |
| 16 | CONFIG/ CONFIG1/ CONFIG2/ CONFIG3/ CONFIG7 | Configuration registers. |
| 7-22 | Reserved | Reserved in the microAptiv UC. |
| 23 | Debug/ Debug2/ TraceControl/ TraceControl2/ UserTraceData1/ TraceBPC ⁽²⁾ | EJTAG Debug register. EJTAG Debug Register 2. EJTAG Trace Control register. EJTAG Trace Control Register 2. EJTAG User Trace Data 1 register. EJTAG Trace Breakpoint register. |
| 24 | DEPC ⁽²⁾ / UserTraceData2 | Program Counter at last debug exception. EJTAG User Trace Data 2 register. |
| 25 | PerfCtl0/ PerfCnt0/ PerfCtl1/ PerfCnt1 | Performance Counter 0 control. Performance Counter 0. Performance Counter 1 control. Performance Counter 1. |
| 26 | ErrCtl | Software parity check enable. |
| 27 | CacheErr | Records information about SRAM parity errors. |
| 28-29 | Reserved | Reserved in the PIC32 core. |
| 30 | ErrorEPC ⁽¹⁾ | Program Counter at last error. |
| 31 | DeSAVE ⁽²⁾ | Debug Handler Scratchpad register. |

Note 1: Registers used in exception processing.

2: Registers used in debug.

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3.3 Power Management

The processor core offers a number of power management features, including low-power design, active power management and Power-Down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during Idle periods.

The mechanism for invoking Power-Down mode is implemented through execution of the `WAIT` instruction. The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MM family makes extensive use of local gated clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The microAptiv UC core has an Enhanced JTAG (EJTAG) interface for use in the software debug. In addition to the standard mode of operation, the microAptiv UC core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (`DERET`) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the microAptiv UC core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification specify which registers are selected and how they are used.

3.5 MIPS32® microAptiv™ UC Core Configuration

[Register 3-1](#) through [Register 3-4](#) show the default configuration of the microAptiv UC core, which is included on PIC32MM0064GPL036 family devices.

PIC32MM0064GPL036 FAMILY

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | r-1 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | r-0 |
| | — | K23<2:0> | | | KU<2:0> | | | — |
| 23:16 | r-0 | R-0 | R-1 | R-0 | r-0 | r-0 | r-0 | R-1 |
| | — | UDI | SB | MDU | — | — | — | DS |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-1 | R-0 | R-1 |
| | BE | AT<1:0> | | AR<2:0> | | | MT<2:1> | |
| 7:0 | R-1 | r-0 | r-0 | r-0 | r-0 | R/W-0 | R/W-1 | R/W-0 |
| | MT<0> | — | — | — | — | K0<2:0> | | |

| | |
|-------------------|------------------------------------|
| Legend: | r = Reserved bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the CONFIG1 register

bit 30-28 **K23<2:0>:** Cacheability of the kseg2 and kseg3 Segments bits
010 = Cache is not implemented

bit 27-25 **KU<2:0>:** Cacheability of the kuseg and useg Segments bits
010 = Cache is not implemented

bit 24-23 **Reserved:** Must be written as zeros; returns zeros on reads

bit 22 **UDI:** User-Defined bit
0 = CorExtend user-defined instructions are not implemented

bit 21 **SB:** SimpleBE bit
1 = Only simple byte enables are allowed on the internal bus interface

bit 20 **MDU:** Multiply/Divide Unit bit
0 = Fast, high-performance MDU

bit 19-17 **Reserved:** Must be written as zeros; returns zeros on reads

bit 16 **DS:** Dual SRAM Interface bit
1 = Dual instruction/data SRAM interface

bit 15 **BE:** Endian Mode bit
0 = Little-endian

bit 14-13 **AT<1:0>:** Architecture Type bits
00 = MIPS32®

bit 12-10 **AR<2:0>:** Architecture Revision Level bits
001 = MIPS32 Release 2

bit 9-7 **MT<2:0>:** MMU Type bits
011 = Fixed mapping

bit 6-3 **Reserved:** Must be written as zeros; returns zeros on reads

bit 2-0 **K0<2:0>:** kseg0 Coherency Algorithm bits
010 = Cache is not implemented

PIC32MM0064GPL036 FAMILY

REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | r-1 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | R-1 | R-0 | R-0 | R-1 | R-0 |
| | — | — | — | PC | WR | CA | EP | FP |

| | | |
|-------------------|------------------|------------------------------------|
| Legend: | r = Reserved bit | U = Unimplemented bit, read as '0' |
| R = Readable bit | W = Writable bit | '0' = Bit is cleared |
| -n = Value at POR | '1' = Bit is set | x = Bit is unknown |

bit 31 **Reserved:** This bit is hardwired to a '1' to indicate the presence of the CONFIG2 register

bit 30-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit
1 = The processor core contains performance counters

bit 3 **WR:** Watch Register Presence bit
0 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e[®] are present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating-Point Unit bit
0 = Floating-Point Unit is not implemented

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REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|-----------------|------------------|----------------|----------------|------------------|----------------|---------------|-----------------|
| 31:24 | r-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — |
| 23:16 | U-0 — | R-0 IPLW<1:0> | R-1 — | R-0 — | R-0 MMAR<2:0> | R-0 — | R-1 MCU | R-1 ISAONEXC |
| 15:8 | R-0 ISA<1:0> | R-1 — | R-1 ULRI | R-1 RXI | U-0 — | U-0 — | U-0 — | R-0 ITL |
| 7:0 | U-0 — | R-1 VEIC | R-1 VINT | R-0 SP | R-1 CDMM | U-0 — | U-0 — | R-0 TL |

| | | |
|-------------------|----------------------|------------------------------------|
| Legend: | r = Reserved bit | U = Unimplemented bit, read as '0' |
| R = Readable bit | W = Writable bit | '1' = Bit is set |
| -n = Value at POR | '0' = Bit is cleared | x = Bit is unknown |

- bit 31 **Reserved:** This bit is hardwired as '0'
- bit 30-23 **Unimplemented:** Read as '0'
- bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8 bits in width
- bit 20-18 **MMAR<2:0>:** microMIPS™ Architecture Revision Level bits
000 = Release 1
- bit 17 **MCU:** MIPS® MCU ASE Implemented bit
1 = MCU ASE is implemented
- bit 16 **ISAONEXC:** ISA on Exception bit
1 = microMIPS is used on entrance to an exception vector
- bit 15-14 **ISA<1:0>:** Instruction Set Availability bits
01 = Only microMIPS is implemented
- bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented
- bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented
- bit 11-9 **Unimplemented:** Read as '0'
- bit 8 **ITL:** Indicates that iFlowtrace™ Hardware is Present bit
0 = The iFlowtrace hardware is not implemented in the core
- bit 7 **Unimplemented:** Read as '0'
- bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented.
- bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented
- bit 4 **SP:** Small Page bit
0 = 4-Kbyte page size
- bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented

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REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-1 |
| | — | — | — | — | — | — | — | NF |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

4.0 MEMORY ORGANIZATION

PIC32MM microcontrollers provide 4 Gbytes of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The data memory can be made executable, allowing the CPU to execute code from data memory.

Key features include:

- 32-Bit Native Data Width
- Separate Boot Flash Memory (BFM) for Protected Code
- Robust Bus Exception Handling to Intercept Runaway Code
- Simple Memory Mapping with Fixed Mapping Translation (FMT) Unit

The PIC32MM0064GPL036 family devices implement two address spaces: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions. Physical addresses are used by peripherals, such as Flash controllers, that access memory independently of the CPU.

The virtual address space is divided into two segments of 512 Mbytes each, labeled kseg0 and kseg1. The Program Flash Memory (PFM) and Data RAM Memory (DRM) are accessible from either kseg0 or kseg1, while the Boot Flash Memory (BFM) and peripheral SFRs are accessible only from kseg1.

The Fixed Mapping Translation (FMT) unit translates the memory segments into corresponding physical address regions. Figure 4-1 through Figure 4-3 illustrate the fixed mapping scheme, implemented by the PIC32MM0064GPL036 family core, between the virtual and physical address space.

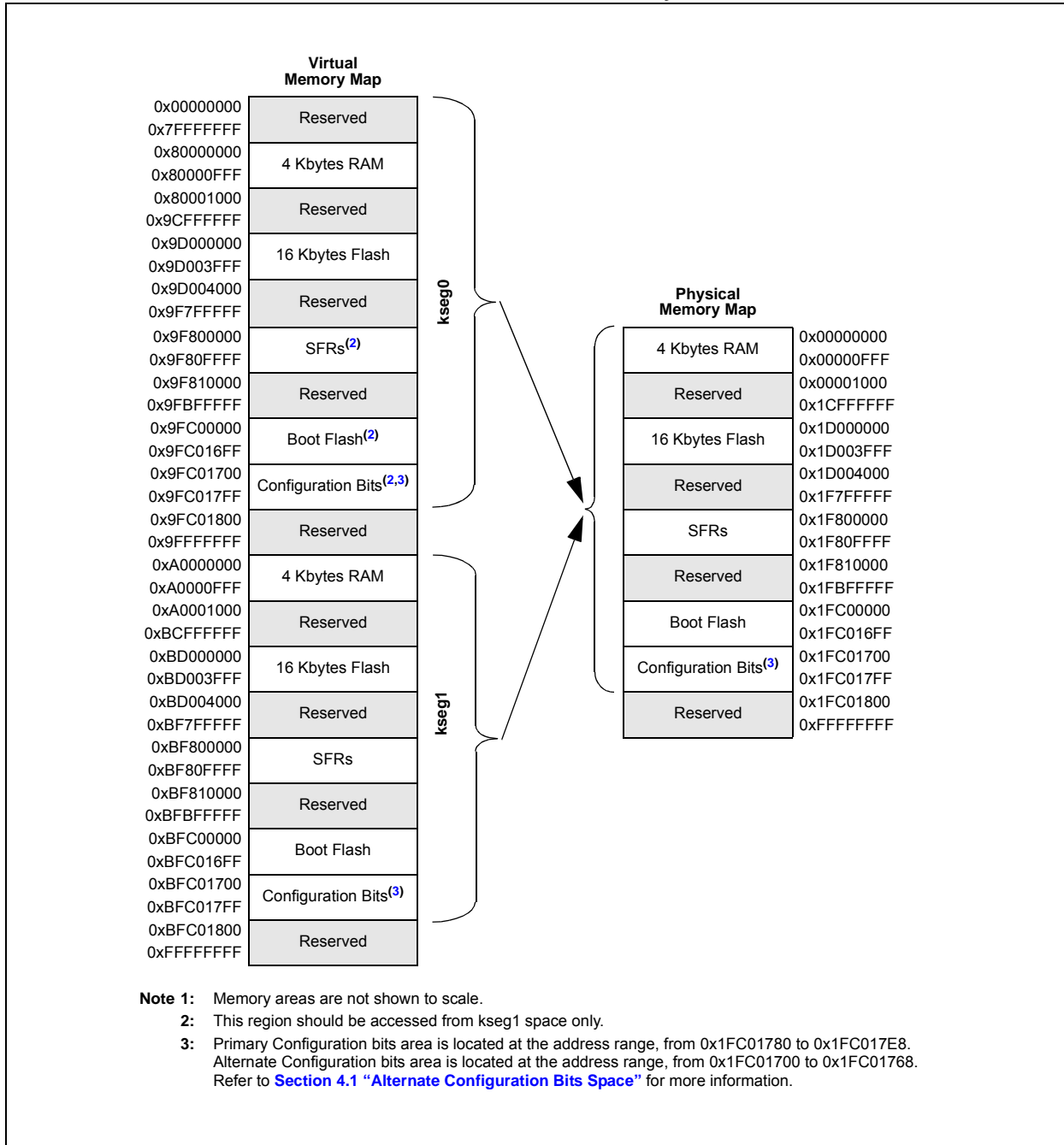
The mapping of the memory segments depends on the CPU error level, set by the ERL bit in the CPU STATUS Register (SR). Error level is set (ERL = 1) by the CPU on a Reset, Soft Reset or NMI. In this mode, the CPU can access memory by the physical address. This mode is provided for compatibility with other MIPS® processor cores that use a TLB-based MMU. The C start-up code clears the ERL bit to zero, so that when application software starts up, it sees the proper virtual to physical memory mapping.

4.1 Alternate Configuration Bits Space

Every Configuration Word has an associated Alternate Word (designated by the letter A as the first letter in the name of the word). During device start-up, Primary Words are read, and if uncorrectable ECC errors are found, the BCFGERR (RCON<27>) flag is set and Alternate Words are used. If uncorrectable ECC errors are found in Primary and Alternate Words, the BCFGFAIL (RCON<26>) flag is set, and the default configuration is used. The Primary Configuration bits area is located at the address range, from 0x1FC01780 to 0x1FC017E8. The Alternate Configuration bits area is located at the address range, from 0x1FC01700 to 0x1FC01768.

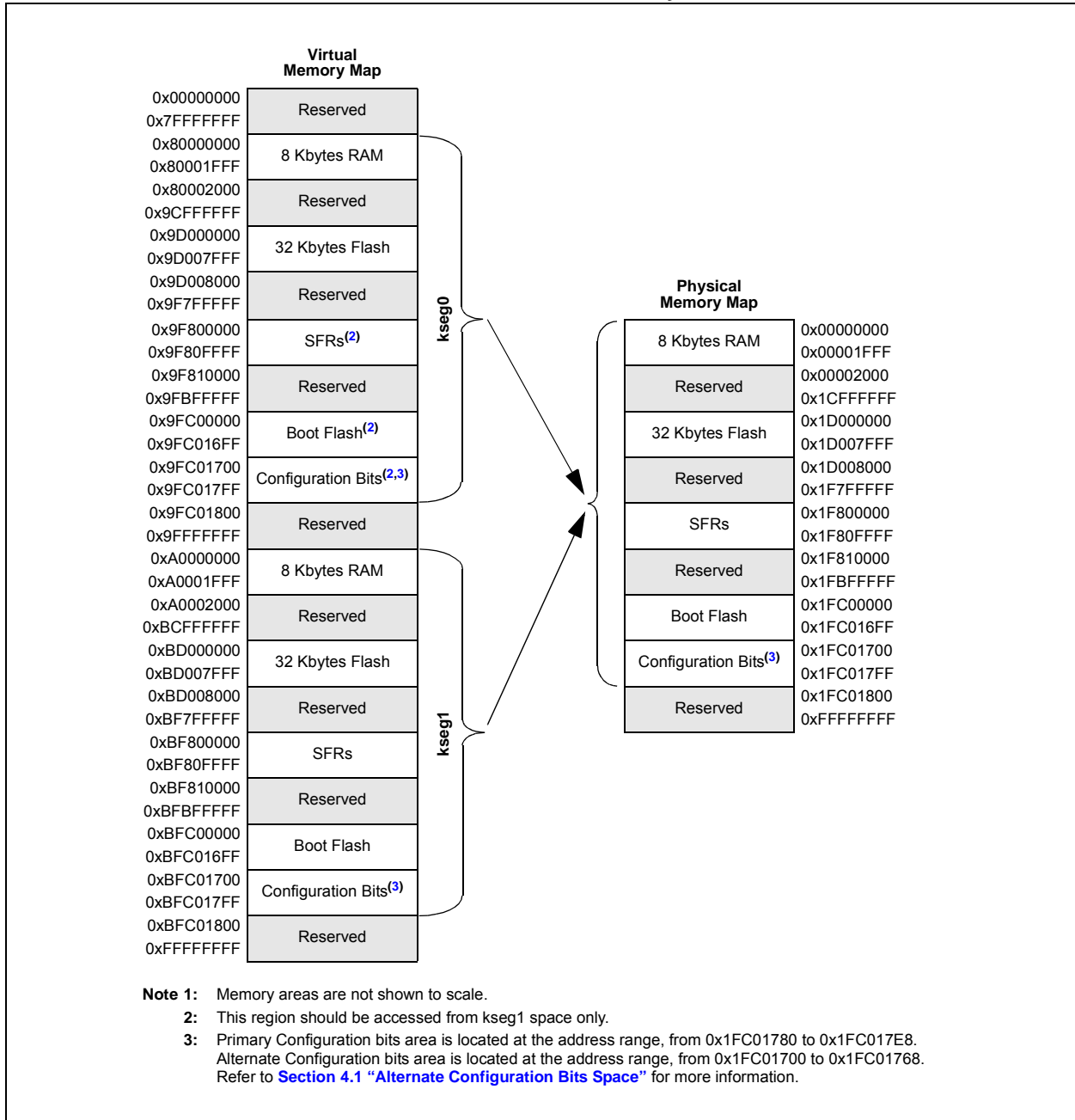
PIC32MM0064GPL036 FAMILY

FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 16 Kbytes OF PROGRAM MEMORY⁽¹⁾



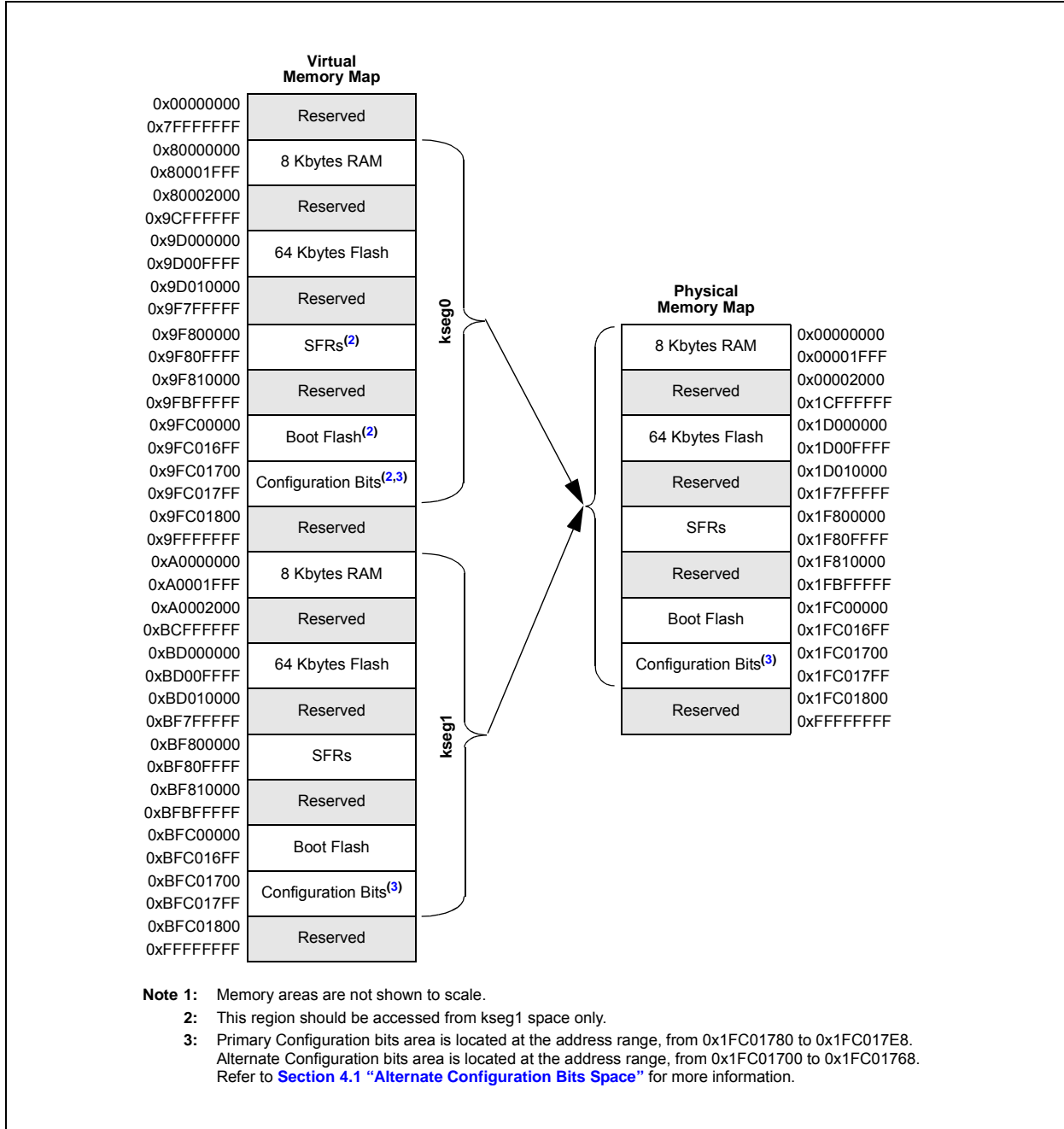
PIC32MM0064GPL036 FAMILY

FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 32 Kbytes OF PROGRAM MEMORY⁽¹⁾



PIC32MM0064GPL036 FAMILY

FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 64 Kbytes OF PROGRAM MEMORY⁽¹⁾



5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. “Flash Programming”** (DS60001121) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

PIC32MM0064GPL036 family devices contain an internal Flash program memory for executing user code. The Program and Boot Flash Memory can be write-protected. The erase page size is 512 32-bit words. The program row size is 64 32-bit words. The memory can be programmed by rows or by two 32-bit words.

The devices implement an Error Correcting Code (ECC). The memory control block contains a logic to write and read ECC bits to and from the Flash memory. The Flash is programmed at the same time as the corresponding ECC bits. The ECC provides improved resistance to Flash errors. The ECC single-bit error will be transparently corrected. The ECC double-bit error results in a bus error exception.

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is described in **Section 5. “Flash Programming”** in the *“PIC32 Family Reference Manual”*. EJTAG programming is performed using the JTAG port of the device. ICSP programming requires fewer connections than for EJTAG programming. The EJTAG and ICSP methods are described in the *“PIC32 Flash Programming Specification”* (DS60001145), which is available for download from the Microchip web site.

5.1 Flash Controller Registers Write Protection

The NVMPWP and NVMBWP registers, and the WR bit in the NVMCON register are protected (locked) from an accidental write. A special unlock sequence is required to modify the content of these registers or bits.

To unlock, the following steps should be done:

1. Disable interrupts prior to the unlock sequence.
2. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the NVMKEY register in two back-to-back Assembly or ‘C’ instructions.
3. Write the new value to the required bits.
4. Re-enable interrupts.

5.2 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|-----------------------------|------------------------|-----------|------------------|-------|-------|--------|-------|----------|------|------|------------|------|------|------|------------|------|------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | |
| 2380 | NVMCON ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | WR | WREN | WRERR | LVDERR | — | — | — | — | — | — | — | — | NVMOP<3:0> | | | 0000 |
| 2390 | NVMKEY | 31:16 | NVMKEY<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 23A0 | NVMADDR ⁽¹⁾ | 31:16 | NVMADDR<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 23B0 | NVMDATA0 | 31:16 | NVMDATA0<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 23C0 | NVMDATA1 | 31:16 | NVMDATA1<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 23D0 | NVMSRCADDR | 31:16 | NVMSRCADDR<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 23E0 | NVMPWP ⁽¹⁾ | 31:16 | PWPUNLOCK | — | — | — | — | — | — | — | PWP<23:16> | | | | | | | 8000 |
| | | 15:0 | PWP<15:0> | | | | | | | | | | | | | | | 0000 |
| 23F0 | NVMBWP ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BWPUNLOCK | — | — | — | — | BWP<2:0> | | | — | — | — | — | — | — | — | 8700 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 5-1: NVMCON: NVM PROGRAMMING CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|---------------------|---------------------|------------------------|-------------------------|---------------------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0, HC | R/W-0 | R-0, HS, HC | R-0, HS, HC | r-0 | U-0 | U-0 | U-0 |
| | WR ^(1,4) | WREN ⁽¹⁾ | WRERR ^(1,2) | LVDERR ^(1,2) | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | NVMOP<3:0> ⁽³⁾ | | | |

| | | |
|-------------------|----------------------------|--|
| Legend: | HS = Hardware Settable bit | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared r = Reserved bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit^(1,4)

This bit cannot be cleared and can be set only when WREN = 1, and the unlock sequence has been performed.

1 = Initiates a Flash operation

0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit⁽¹⁾

1 = Enables writes to the WR bit and disables writes to the NVMOP<3:0> bits

0 = Disables writes to the WR bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit^(1,2)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.

1 = Program or erase sequence did not complete successfully

0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit^(1,2)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.

1 = Low voltage is detected (possible data corruption if WRERR is set)

0 = Voltage level is acceptable for programming

bit 11 **Reserved:** Maintain as '0'

bit 10-4 **Unimplemented:** Read as '0'

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

2: These bits are cleared by setting NVMOP<3:0> = 0000 and initiating a Flash operation (i.e., WR).

3: NVMOP<3:0> bits are write-protected if the WREN bit is set.

4: Writes to the WR bit require an unlock sequence. Refer to [Section 5.1 "Flash Controller Registers Write Protection"](#) for details.

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REGISTER 5-1: NVMCON: NVM PROGRAMMING CONTROL REGISTER (CONTINUED)

bit 3-0 **NVMOP<3:0>**: NVM Operation bits⁽³⁾

These bits are only writable when WREN = 0.

1111 = Reserved

•
•
•

1000 = Reserved

0111 = Program Erase Operation: Erases all of Program Flash Memory (all pages must be unprotected in the NVMPWP register, Boot Flash Memory is not erased)

0110 = Reserved

0101 = Reserved

0100 = Page Erase Operation: Erases page selected by NVMADDR (erases Boot or Program Flash Memory, page must be unprotected in the NVMBWP or NVMPWP register)

0011 = Row Program Operation: Programs row selected by NVMADDR (programs Boot or Program Flash Memory, page must be unprotected in the NVMBWP or NVMPWP register)

0010 = Double-Word Program Operation: Programs two words to the address selected by NVMADDR (programs Boot or Program Flash Memory, page must be unprotected in the NVMBWP or NVMPWP register)

0001 = Reserved

0000 = No operation, clears WRERR and LVDERR bits

- Note 1:** These bits are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.
- Note 2:** These bits are cleared by setting NVMOP<3:0> = 0000 and initiating a Flash operation (i.e., WR).
- Note 3:** NVMOP<3:0> bits are write-protected if the WREN bit is set.
- Note 4:** Writes to the WR bit require an unlock sequence. Refer to [Section 5.1 “Flash Controller Registers Write Protection”](#) for details.

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REGISTER 5-2: NVMKEY: NVM PROGRAMMING UNLOCK REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| NVMKEY<31:24> | | | | | | | | |
| 23:16 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| NVMKEY<23:16> | | | | | | | | |
| 15:8 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| NVMKEY<15:8> | | | | | | | | |
| 7:0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| NVMKEY<7:0> | | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **NVMKEY<31:0>**: NVM Unlock Register bits
 These bits are write-only and read as '0' on any read.

REGISTER 5-3: NVMADDR: NVM FLASH ADDRESS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMADDR<31:24> | | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMADDR<23:16> | | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMADDR<15:8> | | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMADDR<7:0> | | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **NVMADDR<31:0>**: NVM Flash Address bits

| NVMOP<3:0> Selection | Flash Address Bits (NVMADDR<31:0>) |
|----------------------|---|
| Page Erase | Address identifies the page to erase (NVMADDR<10:0> are ignored). |
| Row Program | Address identifies the row to program (NVMADDR<7:0> are ignored). |
| Double-Word Program | Address identifies the double-word (64-bit) to program (NVMADDR<1:0> bits are ignored). |

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REGISTER 5-4: NVMDATAx: NVM FLASH DATA x REGISTER (x = 0-1)

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMDATAx<31:24> | | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMDATAx<23:16> | | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMDATAx<15:8> | | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMDATAx<7:0> | | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **NVMDATAx<31:0>**: NVM Flash Data x bits

Double-Word Program: Writes NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the least significant instruction word.

REGISTER 5-5: NVMSRCADDR: NVM SOURCE DATA ADDRESS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-------------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMSRCADDR<31:24> | | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMSRCADDR<23:16> | | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMSRCADDR<15:8> | | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMSRCADDR<7:0> | | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>**: NVM Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

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REGISTER 5-6: NVMPWP: NVM PROGRAM FLASH WRITE-PROTECT REGISTER⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|---------------------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-1 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | PWPUNLOCK | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PWP<23:16> ⁽²⁾ | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PWP<15:8> ⁽²⁾ | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PWP<7:0> ⁽²⁾ | | | | | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31 **PWPUNLOCK:** Program Flash Memory Page Write-Protect Unlock bit

1 = Register is not locked and can be modified
0 = Register is locked and cannot be modified

This bit is only clearable and cannot be set except by any Reset.

bit 30-24 **Unimplemented:** Read as '0'

bit 23-0 **PWP<23:0>:** Flash Program Write-Protect (Page) Address bits⁽²⁾

Physical memory below address, 0x1DXXXXXX, is write-protected, where 'XXXXXX' is specified by PWP<23:0>. When the PWP<23:0> bits have a value of '0', write protection is disabled for the entire Program Flash Memory. If the specified address falls within the page, the entire page and all pages below the current page will be protected.

Note 1: Writes to this register require an NVMKEY unlock sequence. Refer to [Section 5.1 “Flash Controller Registers Write Protection”](#) for details.

2: These bits can be modified only when the unlock bit (PWPUNLOCK) is set.

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REGISTER 5-7: NVMBWP: NVM BOOT FLASH (PAGE) WRITE-PROTECT REGISTER⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|---------------------|---------------------|---------------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-1 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 |
| | BWPULOCK | — | — | — | — | BWP2 ⁽²⁾ | BWP1 ⁽²⁾ | BWP0 ⁽²⁾ |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BWPULOCK:** Boot Alias Write-Protect Unlock bit
 1 = BWPx bits are not locked and can be modified
 0 = BWPx bits are locked and cannot be modified
 This bit is only clearable and cannot be set except by any Reset.

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **BWP2:** Boot Alias Page 2 Write-Protect bit⁽²⁾
 1 = Write protection for physical address, 0x1FC01000 through 0x1FC017FF, is enabled
 0 = Write protection for physical address, 0x1FC01000 through 0x1FC017FF, is disabled

bit 9 **BWP1:** Boot Alias Page 1 Write-Protect bit⁽²⁾
 1 = Write protection for physical address, 0x1FC00800 through 0x1FC00FFF, is enabled
 0 = Write protection for physical address, 0x1FC00800 through 0x1FC00FFF, is disabled

bit 8 **BWP0:** Boot Alias Page 0 Write-Protect bit⁽²⁾
 1 = Write protection for physical address, 0x1FC00000 through 0x1FC007FF, is enabled
 0 = Write protection for physical address, 0x1FC00000 through 0x1FC007FF, is disabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an NVMKEY unlock sequence. Refer to [Section 5.1 “Flash Controller Registers Write Protection”](#) for details.

2: These bits can be modified only when the associated unlock bit (BWPULOCK) is set.

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6.0 RESETS

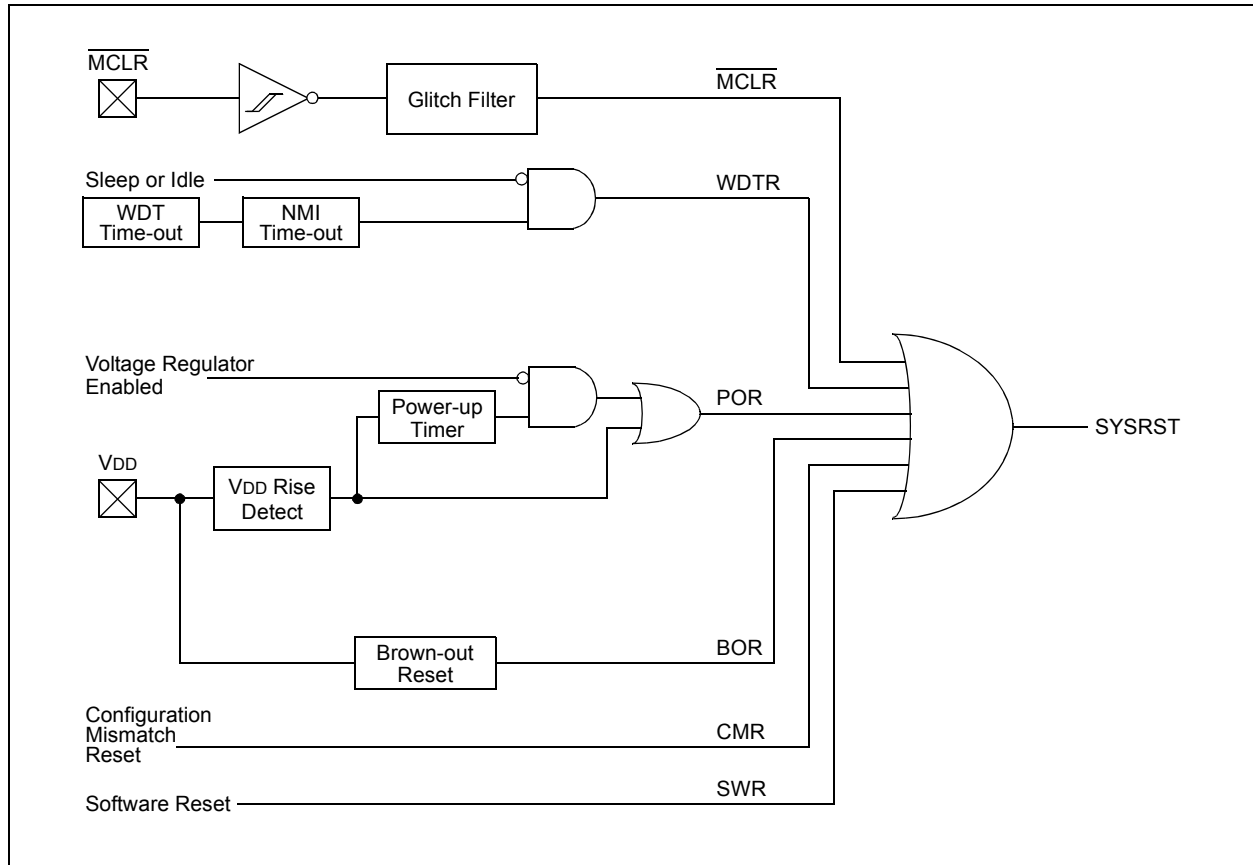
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Resets”** (DS60001118) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset Pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in [Figure 6-1](#).

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|--------------|---------|-------|-------|---------|----------|------|------|-------|------|------|------|------|-------|------|-------|------------|-------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | | |
| 1240 | RCON | 31:16 | PORIO | PORCORE | — | — | BCFGERR | BCFGFAIL | — | — | — | — | — | — | — | — | — | — | C000 | |
| | | 15:0 | — | — | — | — | — | — | — | CMR | — | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR | POR | 0003 |
| 1250 | RSWRST | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SWRST |
| 1260 | RNMICON | 31:16 | — | — | — | — | — | — | — | WDTR | SWNMI | — | — | — | — | GNMI | — | CF | WDTS | 0000 |
| | | 15:0 | NMICNT<15:0> | | | | | | | | | | | | | | | | 0000 | |
| 1270 | PWRCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SBORN | RETN | VREGS |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|---------------------|---------------|---------------|
| 31:24 | R/W-1, HS | R/W-1, HS | U-0 | U-0 | R/W-0, HS | R/W-0, HS | U-0 | U-0 |
| | PORIO | PORCORE | — | — | BCFGERR | BCFGFAIL | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HS | U-0 |
| | — | — | — | — | — | — | CMR | — |
| 7:0 | R/W-0, HS | R/W-0, HS | U-0 | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-1, HS | R/W-1, HS |
| | EXTR | SWR | — | WDTO | SLEEP | IDLE ⁽²⁾ | BOR | POR |

| | |
|-------------------|------------------------------------|
| Legend: | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | U = Unimplemented bit, read as '0' |
| | '1' = Bit is set |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

- bit 31 **PORIO:** VDD POR Flag bit
Set by hardware at detection of a VDD POR event.
1 = A Power-on Reset has occurred due to VDD voltage
0 = A Power-on Reset has not occurred due to VDD voltage
- bit 30 **PORCORE:** Core Voltage POR Flag bit
Set by hardware at detection of a core POR event.
1 = A Power-on Reset has occurred due to core voltage
0 = A Power-on Reset has not occurred due to core voltage
- bit 29-28 **Unimplemented:** Read as '0'
- bit 27 **BCFGERR:** Primary Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary Configuration registers
0 = No error occurred during a read of the Primary Configuration registers
- bit 26 **BCFGFAIL:** Primary/Secondary Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary and Alternate Configuration registers
0 = No error occurred during a read of the Primary and Alternate Configuration registers
- bit 25-10 **Unimplemented:** Read as '0'
- bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred
- bit 8 **Unimplemented:** Read as '0'
- bit 7 **EXTR:** External Reset (MCLR) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred
- bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset was not executed
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

- Note 1:** User software must clear bits in this register to view the next detection.
Note 2: The IDLE bit will also be set when the device wakes from Sleep mode.

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REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

- bit 3 **SLEEP:** Wake from Sleep Flag bit
 1 = Device was in Sleep mode
 0 = Device was not in Sleep mode
- bit 2 **IDLE:** Wake from Idle Flag bit⁽²⁾
 1 = Device was in Idle mode
 0 = Device was not in Idle mode
- bit 1 **BOR:** Brown-out Reset Flag bit
 1 = Brown-out Reset has occurred
 0 = Brown-out Reset has not occurred
- bit 0 **POR:** Power-on Reset Flag bit
 1 = Power-on Reset has occurred
 0 = Power-on Reset has not occurred

- Note 1:** User software must clear bits in this register to view the next detection.
Note 2: The IDLE bit will also be set when the device wakes from Sleep mode.

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|------------------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | W-0, HC |
| | — | — | — | — | — | — | — | SWRST ^(1,2) |

| | |
|-------------------|--|
| Legend: | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set '0' = Bit is cleared x = Bit is unknown |

- bit 31-1 **Unimplemented:** Read as '0'
- bit 0 **SWRST:** Software Reset Trigger bit^(1,2)
 1 = Enables Software Reset event
 0 = No effect

- Note 1:** The system unlock sequence must be performed before the SWRST bit can be written. Refer to [Section 23.4 “System Registers Write Protection”](#) for details.
Note 2: Once this bit is set, any read of the RSWRST register will cause a Reset to occur.

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REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0/HS |
| | — | — | — | — | — | — | — | WDTR |
| 23:16 | R/W-0/HS | U-0 | U-0 | U-0 | R/W-0/HS | U-0 | R/W-0/HS | R/W-0/HS |
| | SWNMI | — | — | — | GNMI | — | CF | WDTS |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NMI CNT <15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NMI CNT <7:0> | | | | | | | |

| | |
|-------------------|--|
| Legend: | HS = Hardware Settable bits |
| R = Readable bit | W = Writable bit U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set '0' = Bit is cleared x = Bit is unknown |

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **WDTR:** Watchdog Timer Time-out in Run Mode Flag bit

1 = A Run mode WDT time-out has occurred and caused an NMI

0 = WDT time-out has not occurred

Setting this bit will cause a WDT NMI event and NMI CNT <15:0> will begin counting.

bit 23 **SWNMI:** Software NMI Trigger bit

1 = An NMI has been generated

0 = An NMI was not generated

bit 22-20 **Unimplemented:** Read as '0'

bit 19 **GNMI:** Software General NMI Trigger bit

1 = A general NMI has been generated

0 = A general NMI was not generated

bit 18 **Unimplemented:** Read as '0'

bit 17 **CF:** Clock Fail Detect bit

1 = FSCM has detected clock failure and caused an NMI

0 = FSCM has not detected clock failure

Setting this bit will cause a CF NMI event, but will not cause a clock switch to the FRC.

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit

1 = WDT time-out has occurred during Sleep mode and caused a wake-up from Sleep

0 = WDT time-out has not occurred during Sleep mode

Setting this bit will cause a WDT NMI.

bit 15-0 **NMI CNT <15:0>:** NMI Reset Counter Value bits

These bits specify the reload value used by the NMI Reset counter.

FFFFh-0001h = Number of SYSCLK cycles before a device Reset occurs⁽²⁾

0000h = No delay between NMI assertion and device Reset event

Note 1: Writes to this register require an unlock sequence. Refer to [Section 23.4 “System Registers Write Protection”](#) for details.

2: If a Watchdog Timer NMI event (when not in Sleep mode) is cleared before this counter reaches '0', no device Reset is asserted. This NMI Reset counter is only applicable to the Watchdog Timer NMI event.

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REGISTER 6-4: PWRCON: POWER CONTROL REGISTER⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|-----------------------|----------------------|----------------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | SBOREN ⁽³⁾ | RETEN ⁽²⁾ | VREGS ⁽²⁾ |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **SBOREN:** BOR During Sleep Control bit⁽³⁾

1 = BOR is turned on
0 = BOR is turned off

bit 1 **RETEN:** Output Level of the Regulator During Sleep Selection bit⁽²⁾

1 = Writing a '1' to this bit will cause the main regulator to be put in a low-power state during Sleep mode
0 = Writing a '0' to this bit will have no effect

bit 0 **VREGS:** Voltage Regulator Standby Enable bit⁽²⁾

1 = Voltage regulator will remain active during Sleep mode
0 = Voltage regulator will go to Standby mode during Sleep mode

Note 1: Writes to this register require an unlock sequence. Refer to [Section 23.4 “System Registers Write Protection”](#) for details.

2: Refer to [Section 22.4 “On-Chip Voltage Regulator Low-Power Modes”](#) for details.

3: This bit is enabled only when the BOREN<1:0> Configuration bits (FPOR<1:0>) are set to '01'.

7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. “Interrupts”** (DS60001108) and **Section 50. “CPU for Devices with MIPS32® microAptiv™ and M-Class Cores”** (DS60001192) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM

PIC32MM0064GPL036 family devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

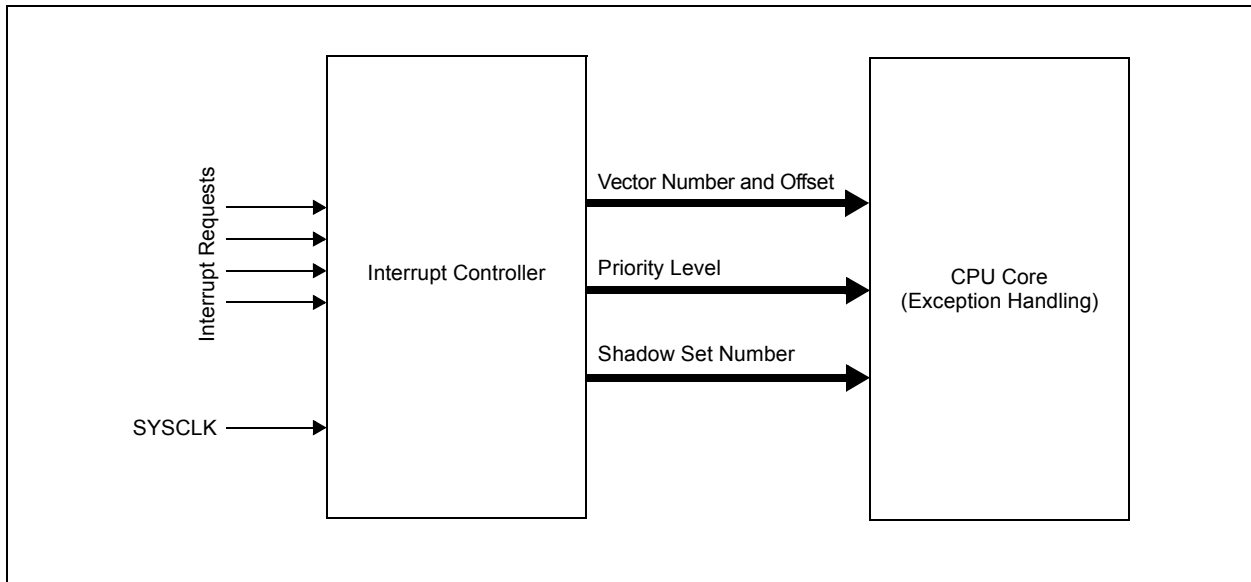
The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 “CPU Exceptions”**.

The PIC32MM0064GPL036 family device interrupt module includes the following features:

- Single Vector or Multivector mode Operation
- Five External Interrupts with Edge Polarity Control
- Interrupt Proximity Timer
- Module Freeze in Debug mode
- Seven User-Selectable Priority Levels for each Vector
- Four User-Selectable Subpriority Levels within each Priority
- One Shadow Register Set that can be used for any Priority Level, Eliminating Software Context Switching and Reducing Interrupt Latency
- Software can Generate any Interrupt
- User-Configurable Interrupt Vectors’ Offset and Vector Table Location

Figure 7-1 shows the block diagram for the interrupt controller and CPU exceptions.

FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM



7.1 CPU Exceptions

CPU Coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. [Table 7-1](#) lists the exception types in order of priority.

TABLE 7-1: MIPS32® microActiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES

| Exception Type (In Order of Priority) | Description | Branches to | Status Bits Set | Debug Bits Set | EXCCODE | XC32 Function Name |
|---|--|--|--------------------|-------------------|-------------|-------------------------------|
| Highest Priority | | | | | | |
| Reset | Assertion of MCLR. | 0xBFC0_0000 | BEV, ERL | — | — | _on_reset |
| Soft Reset | Execution of a RESET instruction. | 0xBFC0_0000 | BEV, SR, ERL | — | — | _on_reset |
| DSS | EJTAG debug single step. | 0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR) | — | DSS | — | — |
| DINT | EJTAG debug interrupt. Caused by setting the EhtagBrk bit in the ECR register. | 0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR) | — | DINT | — | — |
| NMI | Non-maskable interrupt. | 0xBFC0_0000 | BEV, NMI, ERL | — | — | _nmi_handler |
| Interrupt | Assertion of unmasked hardware or software interrupt signal. | See Table 7-2 | IPL<2:0> | — | Int (0x00) | See Table 7-2 |
| DIB | EJTAG debug hardware instruction break matched. | 0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR) | — | DIB | — | — |
| AdEL | Load address alignment error. | EBASE + 0x180 | EXL | — | ADEL (0x04) | _general_exception_handler |
| IBE | Instruction fetch bus error. | EBASE + 0x180 | EXL | — | IBE (0x06) | _general_exception_handler |
| DBp | EJTAG breakpoint (execution of SDBBP instruction). | 0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR) | DBp | — | — | — |
| Sys | Execution of SYSCALL instruction. | EBASE + 0x180 | EXL | — | Sys (0x08) | _general_exception_handler |
| Bp | Execution of BREAK instruction. | EBASE + 0x180 | EXL | — | Bp (0x09) | _general_exception_handler |

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

| Exception Type (In Order of Priority) | Description | Branches to | Status Bits Set | Debug Bits Set | EXCCODE | XC32 Function Name |
|---|---|--|--------------------|---|-------------|----------------------------|
| CpU | Execution of a coprocessor instruction for a coprocessor that is not enabled. | EBASE + 0x180 | CU, EXL | — | CpU (0x0B) | _general_exception_handler |
| RI | Execution of a reserved instruction. | EBASE + 0x180 | EXL | — | RI (0x0A) | _general_exception_handler |
| Ov | Execution of an arithmetic instruction that overflowed. | EBASE + 0x180 | EXL | — | Ov (0x0C) | _general_exception_handler |
| Tr | Execution of a trap (when trap condition is true). | EBASE + 0x180 | EXL | — | Tr (0x0D) | _general_exception_handler |
| DDBL | EJTAG data address break (address only) or EJTAG data value break on load (address and value). | 0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR) | — | DDBL for a load instruction or DDBS for a store instruction | — | — |
| DDBS | EJTAG data address break (address only) or EJTAG data value break on store (address and value). | 0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR) | — | DDBL for a load instruction or DDBS for a store instruction | — | — |
| AdES | Store address alignment error. | EBASE + 0x180 | EXL | — | ADES (0x05) | _general_exception_handler |
| DBE | Load or store bus error. | EBASE + 0x180 | EXL | — | DBE (0x07) | _general_exception_handler |
| CBrk | EJTAG complex breakpoint. | 0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR) | — | DIBImpr, DDBLImpr and/or DDBSImpr | — | — |
| Lowest Priority | | | | | | |

7.2 Interrupts

The PIC32MM0064GPL036 family uses fixed offset for vector spacing. For details, refer to **Section 8. “Interrupts”** (DS60001108) in the “PIC32 Family Reference Manual”. [Table 7-2](#) provides the interrupt related vectors and bits information.

TABLE 7-2: INTERRUPTS

| Interrupt Source | MPLAB® XC32 Vector Name | Vector Number | Interrupt Related Bits Location | | | | Persistent Interrupt |
|---------------------------|--------------------------------------|---------------|---------------------------------|----------|-------------|-------------|----------------------|
| | | | Flag | Enable | Priority | Subpriority | |
| Core Timer | <code>_CORE_TIMER_VECTOR</code> | 0 | IFS0<0> | IEC0<0> | IPC0<4:2> | IPC0<1:0> | No |
| Core Software 0 | <code>_CORE_SOFTWARE_0_VECTOR</code> | 1 | IFS0<1> | IEC0<1> | IPC0<12:10> | IPC0<9:8> | No |
| Core Software 1 | <code>_CORE_SOFTWARE_1_VECTOR</code> | 2 | IFS0<2> | IEC0<2> | IPC0<20:18> | IPC0<17:16> | No |
| External 0 | <code>_EXTERNAL_0_VECTOR</code> | 3 | IFS0<3> | IEC0<3> | IPC0<28:26> | IPC0<25:24> | No |
| External 1 | <code>_EXTERNAL_1_VECTOR</code> | 4 | IFS0<4> | IEC0<4> | IPC1<4:2> | IPC1<1:0> | No |
| External 2 | <code>_EXTERNAL_2_VECTOR</code> | 5 | IFS0<5> | IEC0<5> | IPC1<12:10> | IPC1<9:8> | No |
| External 3 | <code>_EXTERNAL_3_VECTOR</code> | 6 | IFS0<6> | IEC0<6> | IPC1<20:18> | IPC1<17:16> | No |
| External 4 | <code>_EXTERNAL_4_VECTOR</code> | 7 | IFS0<7> | IEC0<7> | IPC1<28:26> | IPC1<25:24> | No |
| PORTA Change Notification | <code>_CHANGE_NOTICE_A_VECTOR</code> | 8 | IFS0<8> | IEC0<8> | IPC2<4:2> | IPC2<1:0> | No |
| PORTB Change Notification | <code>_CHANGE_NOTICE_B_VECTOR</code> | 9 | IFS0<9> | IEC0<9> | IPC2<12:10> | IPC2<9:8> | No |
| PORTC Change Notification | <code>_CHANGE_NOTICE_C_VECTOR</code> | 10 | IFS0<10> | IEC0<10> | IPC2<20:18> | IPC2<17:16> | No |
| Timer1 | <code>_TIMER_1_VECTOR</code> | 11 | IFS0<11> | IEC0<11> | IPC2<28:26> | IPC2<25:24> | No |
| Comparator 1 | <code>_COMPARATOR_1_VECTOR</code> | 12 | IFS0<12> | IEC0<12> | IPC3<4:2> | IPC3<1:0> | No |
| Comparator 2 | <code>_COMPARATOR_2_VECTOR</code> | 13 | IFS0<13> | IEC0<13> | IPC3<12:10> | IPC3<9:8> | No |
| Real-Time Clock Alarm | <code>_RTCC_VECTOR</code> | 14 | IFS0<14> | IEC0<14> | IPC3<20:18> | IPC3<17:16> | No |
| ADC Conversion | <code>_ADC_VECTOR</code> | 15 | IFS0<15> | IEC0<15> | IPC3<28:26> | IPC3<25:24> | No |
| CRC | <code>_CRC_VECTOR</code> | 16 | IFS0<16> | IEC0<16> | IPC4<4:2> | IPC4<1:0> | Yes |
| High/Low-Voltage Detect | <code>_HLVD_VECTOR</code> | 17 | IFS0<17> | IEC0<17> | IPC4<12:10> | IPC4<9:8> | Yes |
| Logic Cell 1 | <code>_CLC1_VECTOR</code> | 18 | IFS0<18> | IEC0<18> | IPC4<20:18> | IPC4<17:16> | No |
| Logic Cell 2 | <code>_CLC2_VECTOR</code> | 19 | IFS0<19> | IEC0<19> | IPC4<28:26> | IPC4<25:24> | No |
| SPI1 Error | <code>_SPI1_ERR_VECTOR</code> | 20 | IFS0<20> | IEC0<20> | IPC5<4:2> | IPC5<1:0> | Yes |
| SPI1 Transmission | <code>_SPI1_TX_VECTOR</code> | 21 | IFS0<21> | IEC0<21> | IPC5<12:10> | IPC5<9:8> | Yes |
| SPI1 Reception | <code>_SPI1_RX_VECTOR</code> | 22 | IFS0<22> | IEC0<22> | IPC5<20:18> | IPC5<17:16> | Yes |

TABLE 7-2: INTERRUPTS (CONTINUED)

| Interrupt Source | MPLAB® XC32 Vector Name | Vector Number | Interrupt Related Bits Location | | | | Persistent Interrupt |
|--------------------------------------|-----------------------------|---------------|---------------------------------|----------|--------------|--------------|----------------------|
| | | | Flag | Enable | Priority | Subpriority | |
| UART1 Reception | _UART1_RX_VECTOR | 23 | IFS0<23> | IEC0<23> | IPC5<28:26> | IPC5<25:24> | Yes |
| UART1 Transmission | _UART1_TX_VECTOR | 24 | IFS0<24> | IEC0<24> | IPC6<4:2> | IPC6<1:0> | Yes |
| UART1 Error | _UART1_ERR_VECTOR | 25 | IFS0<25> | IEC0<25> | IPC6<12:10> | IPC6<9:8> | Yes |
| CCP1 Input Capture or Output Compare | _CCP1_VECTOR | 29 | IFS0<29> | IEC0<29> | IPC7<12:10> | IPC7<9:8> | No |
| CCP1 Timer | _CCT1_VECTOR | 30 | IFS0<30> | IEC0<30> | IPC7<20:18> | IPC7<17:16> | No |
| CCP2 Input Capture or Output Compare | _CCP2_VECTOR | 31 | IFS0<31> | IEC0<31> | IPC7<28:26> | IPC7<25:24> | No |
| CCP2 Timer | _CCT2_VECTOR | 32 | IFS1<0> | IEC1<0> | IPC8<4:2> | IPC8<1:0> | No |
| CCP3 Input Capture or Output Compare | _CCP3_VECTOR | 33 | IFS1<1> | IEC1<1> | IPC8<12:10> | IPC8<9:8> | No |
| CCP3 Timer | _CCT3_VECTOR | 34 | IFS1<2> | IEC1<2> | IPC8<20:18> | IPC8<17:16> | No |
| RESERVED | — | 35 | — | — | — | — | — |
| RESERVED | — | 36 | — | — | — | — | — |
| SPI2 Error | _SPI2_ERR_VECTOR | 37 | IFS1<5> | IEC1<5> | IPC9<12:10> | IPC9<9:8> | Yes |
| SPI2 Transmission | _SPI2_TX_VECTOR | 38 | IFS1<6> | IEC1<6> | IPC9<20:18> | IPC9<17:16> | Yes |
| SPI2 Reception | _SPI2_RX_VECTOR | 39 | IFS1<7> | IEC1<7> | IPC9<28:26> | IPC9<25:24> | Yes |
| UART2 Reception | _UART2_RX_VECTOR | 40 | IFS1<8> | IEC1<8> | IPC10<4:2> | IPC10<1:0> | Yes |
| UART2 Transmission | _UART2_TX_VECTOR | 41 | IFS1<9> | IEC1<9> | IPC10<12:10> | IPC10<9:8> | Yes |
| UART2 Error | _UART2_ERR_VECTOR | 42 | IFS1<10> | IEC1<10> | IPC10<20:18> | IPC10<17:16> | Yes |
| NVM Program or Erase Complete | _NVM_VECTOR | 46 | IFS1<14> | IEC1<14> | IPC11<20:18> | IPC11<17:16> | Yes |
| Core Performance Counter | _PERFORMANCE_COUNTER_VECTOR | 47 | IFS1<15> | IEC1<15> | IPC11<28:26> | IPC11<25:24> | No |

TABLE 7-3: INTERRUPT REGISTER MAP

| Virtual Address (BF80 #) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | All Resets | | |
|-----------------------------|---------------------------------|-----------|-------------|--------|--------|---------------|-------------|----------------------|---------------|--------|-------------|----------|----------|---------------------------|-------------|---------------------------|------------|--------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | | 17/1 | 16/0 |
| F000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | VS<6:0> | | | | 0000 | |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| F010 | PRISS | 31:16 | PRI7SS<3:0> | | | | PRI6SS<3:0> | | | | PRI5SS<3:0> | | | | PRI4SS<3:0> | | | | 0000 |
| | | 15:0 | PRI3SS<3:0> | | | | PRI2SS<3:0> | | | | PRI1SS<3:0> | | | | — | — | — | SS0 | 0000 |
| F020 | INTSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | SIRQ<7:0> | | | | | | | 0000 | |
| F030 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | IPTMR<31:0> | | | | | | | | | | | | | | 0000 | | |
| F040 | IFS0 | 31:16 | CCP2IF | CCT1IF | CCP1IF | — | — | — | U1EIF | U1TXIF | U1RXIF | SPI1RXIF | SPI1TXIF | SPI1EIF | CLC2IF | CLC1IF | LVDIF | CRCIF | 0000 |
| | | 15:0 | AD1IF | RTCCIF | CMP2IF | CMP1IF | T1IF | CNCIF ⁽²⁾ | CNBIF | CNAIF | INT4IF | INT3IF | INT2IF | INT1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| F050 | IFS1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |
| | | 15:0 | CPCIF | NVMIF | — | — | — | U2EIF | U2TXIF | U2RXIF | SPI2RXIF | SPI2TXIF | SPI2EIF | — | — | CCT3IF | CCP3IF | CCT2IF | 0000 |
| F0C0 | IEC0 | 31:16 | CCP2IE | CCT1IE | CCP1IE | — | — | — | U1EIE | U1TXIE | U1RXIE | SPI1RXIE | SPI1TXIE | SPI1EIE | CLC2IE | CLC1IE | LVDIE | CRCIE | 0000 |
| | | 15:0 | AD1IE | RTCCIE | CMP2IE | CMP1IE | T1IE | CNCIE ⁽²⁾ | CNBIE | CNAIE | INT4IE | INT3IE | INT2IE | INT1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| F0D0 | IEC1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |
| | | 15:0 | CPCIE | NVMIE | — | — | — | U2EIE | U2TXIE | U2RXIE | SPI2RXIE | SPI2TXIE | SPI2EIE | — | — | CCT3IE | CCP3IE | CCT2IE | 0000 |
| F140 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | | — | — | CS1IP<2:0> | | CS1IS<1:0> | | 0000 | |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | | — | — | CTIP<2:0> | | CTIS<1:0> | | 0000 | |
| F150 | IPC1 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | | — | — | INT3IP<2:0> | | INT3IS<1:0> | | 0000 | |
| | | 15:0 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | | — | — | INT1IP<2:0> | | INT1IS<1:0> | | 0000 | |
| F160 | IPC2 | 31:16 | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | | — | — | CNCIP<2:0> ⁽²⁾ | | CNCIS<1:0> ⁽²⁾ | | 0000 | |
| | | 15:0 | — | — | — | CNBIP<2:0> | | | CNBIS<1:0> | | | — | — | CNAIP<2:0> | | CNAIS<1:0> | | 0000 | |
| F170 | IPC3 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | | — | — | RTCCIP<2:0> | | RTCCIS<1:0> | | 0000 | |
| | | 15:0 | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | | — | — | CMP1IP<2:0> | | CMP1IS<1:0> | | 0000 | |
| F180 | IPC4 | 31:16 | — | — | — | CLC2IP<2:0> | | | CLC2IS<1:0> | | | — | — | CLC1IP<2:0> | | CLC1IS<1:0> | | 0000 | |
| | | 15:0 | — | — | — | LVDIP<2:0> | | | LVDIS<1:0> | | | — | — | CRCIP<2:0> | | CRCIS<1:0> | | 0000 | |
| F190 | IPC5 | 31:16 | — | — | — | U1RXIP<2:0> | | | U1RXIS<1:0> | | | — | — | SPI1RXIP<2:0> | | SPI1RXIS<1:0> | | 0000 | |
| | | 15:0 | — | — | — | SPI1TXIP<2:0> | | | SPI1TXIS<1:0> | | | — | — | SPI1EIP<2:0> | | SPI1EIS<1:0> | | 0000 | |
| F1A0 | IPC6 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |
| | | 15:0 | — | — | — | U1EIP<2:0> | | | U1EIS<1:0> | | | — | — | U1TXIP<2:0> | | U1TXIS<1:0> | | 0000 | |
| F1B0 | IPC7 | 31:16 | — | — | — | CCP2IP<2:0> | | | CCP2IS<1:0> | | | — | — | CCT1IP<2:0> | | CCT1IS<1:0> | | 0000 | |
| | | 15:0 | — | — | — | CCP1IP<2:0> | | | CCP1IS<1:0> | | | — | — | — | — | — | — | — | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

Note 2: These bits are not available on 20-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

| Virtual Address (BF80 #) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|---------------|-------|-------|---------------|------|------|------|------------|---------------|------------|---------------|------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | | 17/1 |
| F1C0 | IPC8 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | CCT3IP<2:0> | | CCT3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CCP3IP<2:0> | | | CCP3IS<1:0> | | — | — | — | CCT2IP<2:0> | | CCT2IS<1:0> | | 0000 |
| F1D0 | IPC9 | 31:16 | — | — | — | SPI2RXIP<2:0> | | | SPI2RXIS<1:0> | | — | — | — | SPI2TXIP<2:0> | | SPI2TXIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | SPI2EIP<2:0> | | | SPI2EIS<1:0> | | — | — | — | — | — | — | — | — |
| F1E0 | IPC10 | 31:16 | — | — | — | — | — | — | — | — | — | — | U2EIP<2:0> | | U2EIS<1:0> | | 0000 | |
| | | 15:0 | — | — | — | U2TXIP<2:0> | | | U2TXIS<1:0> | | — | — | — | U2RXIP<2:0> | | U2RXIS<1:0> | | 0000 |
| F1F0 | IPC11 | 31:16 | — | — | — | CPCIP<2:0> | | | CPCIS<1:0> | | — | — | — | NVMIP<2:0> | | NVMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: These bits are not available on 20-pin devices.

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REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | VS<6:0> | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MVEC | — | TPC<2:0> | | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22-16 **VS<6:0>:** Vector Spacing bits

Spacing Between Vectors:

0000000 = 0 Bytes
 0000001 = 8 Bytes
 0000010 = 16 Bytes
 0000100 = 32 Bytes
 0001000 = 64 Bytes
 0010000 = 128 Bytes
 0100000 = 256 Bytes
 1000000 = 512 Bytes

All other values are reserved. The operation of this device is undefined if a reserved value is written to this field. If MVEC = 0, this field is ignored.

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multivector Configuration bit

1 = Interrupt controller configured for Multivectored mode
 0 = Interrupt controller configured for Single Vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits

111 = Interrupts of Group Priority 7 or lower start the interrupt proximity timer
 110 = Interrupts of Group Priority 6 or lower start the interrupt proximity timer
 101 = Interrupts of Group Priority 5 or lower start the interrupt proximity timer
 100 = Interrupts of Group Priority 4 or lower start the interrupt proximity timer
 011 = Interrupts of Group Priority 3 or lower start the interrupt proximity timer
 010 = Interrupts of Group Priority 2 or lower start the interrupt proximity timer
 001 = Interrupts of Group Priority 1 start the interrupt proximity timer
 000 = Disables interrupt proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit

1 = Rising edge
 0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit

1 = Rising edge
 0 = Falling edge

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REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 2 **INT2EP**: External Interrupt 2 Edge Polarity Control bit
 1 = Rising edge
 0 = Falling edge
- bit 1 **INT1EP**: External Interrupt 1 Edge Polarity Control bit
 1 = Rising edge
 0 = Falling edge
- bit 0 **INT0EP**: External Interrupt 0 Edge Polarity Control bit
 1 = Rising edge
 0 = Falling edge

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------------------|----------------|----------------|----------------|----------------------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PRI7SS<3:0> ⁽¹⁾ | | | | PRI6SS<3:0> ⁽¹⁾ | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PRI5SS<3:0> ⁽¹⁾ | | | | PRI4SS<3:0> ⁽¹⁾ | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PRI3SS<3:0> ⁽¹⁾ | | | | PRI2SS<3:0> ⁽¹⁾ | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
| | PRI1SS<3:0> ⁽¹⁾ | | | | — | — | — | SS0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-28 **PRI7SS<3:0>**: Interrupt with Priority Level 7 Shadow Set bits⁽¹⁾

11111 = Reserved

•
•
•

0010 = Reserved

0001 = Interrupt with a priority level of 7 uses Shadow Set 1

0000 = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>**: Interrupt with Priority Level 6 Shadow Set bits⁽¹⁾

1111 = Reserved

•
•
•

0010 = Reserved

0001 = Interrupt with a priority level of 6 uses Shadow Set 1

0000 = Interrupt with a priority level of 6 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

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REGISTER 7-2: PRIS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 23-20 **PRI5SS<3:0>**: Interrupt with Priority Level 5 Shadow Set bits⁽¹⁾

1111 = Reserved

•

•

0010 = Reserved

0001 = Interrupt with a priority level of 5 uses Shadow Set 1

0000 = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>**: Interrupt with Priority Level 4 Shadow Set bits⁽¹⁾

1111 = Reserved

•

•

0010 = Reserved

0001 = Interrupt with a priority level of 4 uses Shadow Set 1

0000 = Interrupt with a priority level of 4 uses Shadow Set 0

bit 15-12 **PRI3SS<3:0>**: Interrupt with Priority Level 3 Shadow Set bits⁽¹⁾

1111 = Reserved

•

•

0010 = Reserved

0001 = Interrupt with a priority level of 3 uses Shadow Set 1

0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>**: Interrupt with Priority Level 2 Shadow Set bits⁽¹⁾

1111 = Reserved

•

•

0010 = Reserved

0001 = Interrupt with a priority level of 2 uses Shadow Set 1

0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>**: Interrupt with Priority Level 1 Shadow Set bits⁽¹⁾

1111 = Reserved

•

•

0010 = Reserved

0001 = Interrupt with a priority level of 1 uses Shadow Set 1

0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented**: Read as '0'

bit 0 **SS0**: Single Vector Shadow Register Set bit

1 = Single vector is presented with a shadow set

0 = Single vector is not presented with a shadow set

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

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REGISTER 7-3: INTSTAT: INTERRUPT STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|---------------------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | — | — | — | — | — | SRIPL<2:0> ⁽¹⁾ | | |
| 7:0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | SIRQ<7:0> | | | | | | | |

| | | |
|-------------------|----------------------------|--|
| Legend: | HS = Hardware Settable bit | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level for Single Vector Mode bits⁽¹⁾

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-0 **SIRQ<7:0>:** Last Interrupt Request Serviced Status bits

11111111-00000000 = The last interrupt request number serviced by the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-4: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IPTMR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IPTMR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IPTMR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IPTMR<7:0> | | | | | | | |

| | | |
|-------------------|------------------|--|
| Legend: | W = Writable bit | U = Unimplemented bit, read as '0' |
| R = Readable bit | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |
| -n = Value at POR | | |

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits

Used by the interrupt proximity timer as a reload value when the interrupt proximity timer is triggered by an interrupt event.

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REGISTER 7-5: IFSx: INTERRUPT FLAG STATUS REGISTER x⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS<7:0> | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **IFS<31:0>**: Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

Note 1: This register represents a generic definition of the IFSx register. Refer to [Table 7-3](#) for the exact bit definitions.

REGISTER 7-6: IECx: INTERRUPT ENABLE CONTROL REGISTER x⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC<7:0> | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **IEC<31-0>**: Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: This register represents a generic definition of the IECx register. Refer to [Table 7-3](#) for the exact bit definitions.

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REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP3<2:0> | | | IS3<1:0> | |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP2<2:0> | | | IS2<1:0> | |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP1<2:0> | | | IS1<1:0> | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP0<2:0> | | | IS0<1:0> | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note 1: This register represents a generic definition of the IPCx register. Refer to [Table 7-3](#) for the exact bit definitions.

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REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x⁽¹⁾ (CONTINUED)

bit 12-10 **IP1<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 9-8 **IS1<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 7-5 **Unimplemented**: Read as '0'

bit 4-2 **IP0<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 1-0 **IS0<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

Note 1: This register represents a generic definition of the IPCx register. Refer to [Table 7-3](#) for the exact bit definitions.

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 59. “Oscillators with DCO”** (DS60001329) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The PIC32MM0064GPL036 family oscillator system has the following modules and features:

- On-Chip PLL with User-Selectable Multiplier and Output Divider to Boost Operating Frequency on Select Internal and External Oscillator Sources
- Primary High-Frequency Crystal Oscillator
- Secondary Low-Frequency and Low-Power Crystal Oscillator
- On-Chip Fast RC (FRC) Oscillator with User-Selectable Output Divider
- Software-Controllable Switching between Various Clock Sources
- Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Flexible Reference Clock Output (REFO)

A block diagram of the oscillator system is provided in [Figure 8-1](#). A block diagram of the REFO clock is provided in [Figure 8-2](#).

8.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MM0064GPL036 family oscillator system includes a Fail-Safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the FRC oscillator and triggers a Non-Maskable Interrupt (NMI). When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode, both the SYSCLK and the FSCM halt, which prevents FSCM detection.

8.2 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOS, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC32 devices have a safeguard lock built into the switching process.

Note: The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMOD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

8.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in FOSC must be programmed to '0'. (Refer to [Section 23.1 “Configuration Bits”](#) for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled; this is the default setting.

The NOSC<2:0> control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC<2:0> bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSC<2:0> Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

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8.2.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC<2:0> bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register.
3. Write the appropriate value to the NOSC<2:0> bits (OSCCON<10:8>) for the new oscillator source.
4. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the SPLLRDY (CLKSTAT<7>) and CF (OSCCON<3>) bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (SPLLRDY = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC<2:0> bits values are transferred to the COSC<2:0> bits.
6. The old clock source is turned off if it is not being used by a peripheral, or enabled by device configuration or a control register.

Note 1: The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

- 2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

A recommended code sequence for a clock switch includes the following:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for OSCCON by writing 0xAA996655 and 0x556699AA to the SYSKEY register.
3. Write the new oscillator source to the NOSC<2:0> bits.
4. Set the OSWEN bit.
5. Relock the OSCCON register.
6. Continue to execute code that is not clock-sensitive (optional).

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in [Example 8-1](#).

EXAMPLE 8-1: BASIC CODE SEQUENCE FOR CLOCK SWITCHING

```
SYSKEY = 0x00000000; // force lock
SYSKEY = 0xAA996655; // unlock
SYSKEY = 0x556699AA;

OSCCONbits.NOSC = 3; // select the new
                    // clock source

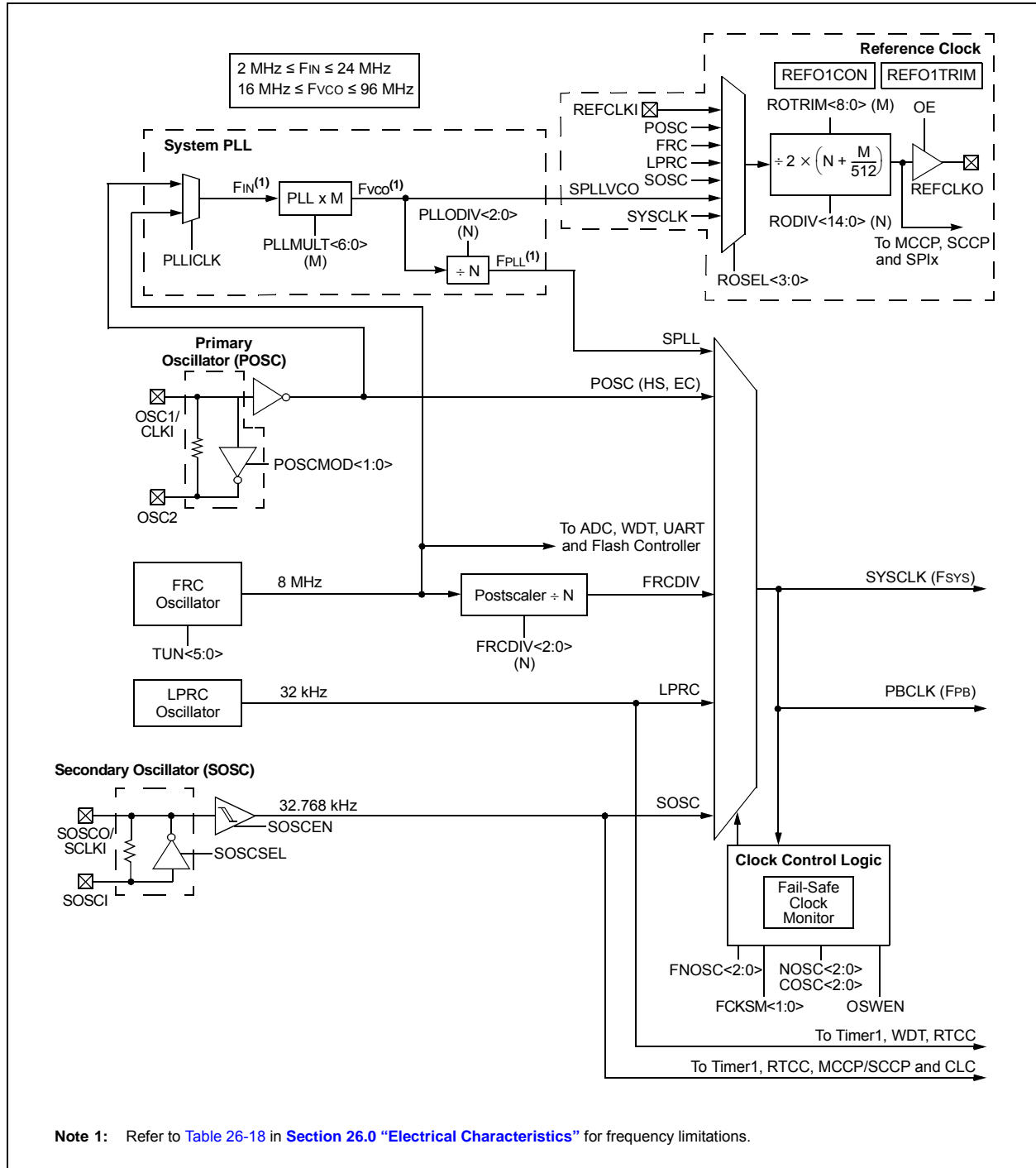
OSCCONSET = 1; // set the OSWEN bit

SYSKEY = 0x00000000; // force lock

while (OSCCONbits.OSWEN); // optional wait for
                          // switch operation
```

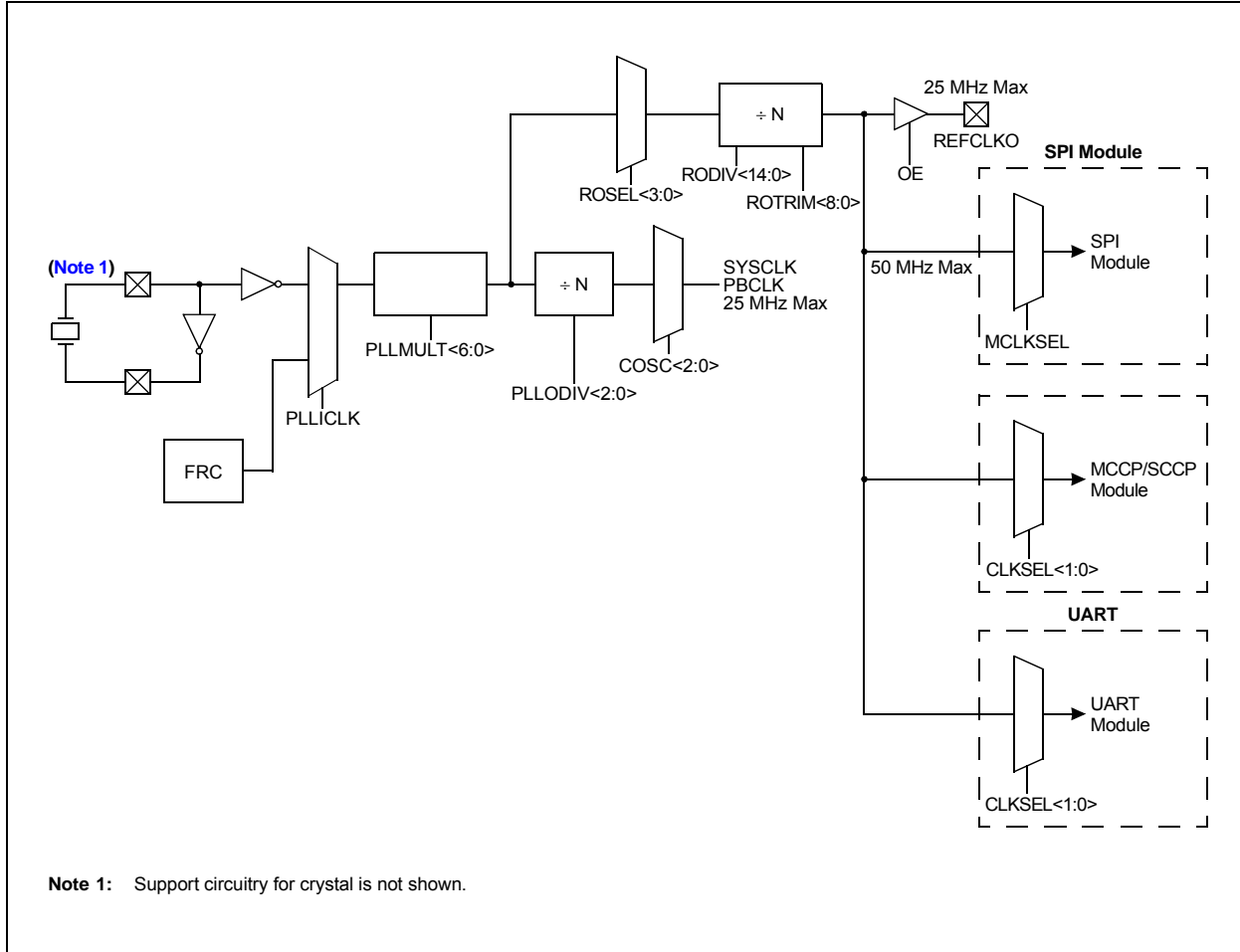
PIC32MM0064GPL036 FAMILY

FIGURE 8-1: PIC32MM0064GPL036 FAMILY OSCILLATOR DIAGRAM



PIC32MM0064GPL036 FAMILY

FIGURE 8-2: REFERENCE OSCILLATOR CLOCK DIAGRAM



8.3 Oscillator Control Registers

TABLE 8-1: OSCILLATOR CONFIGURATION REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽²⁾ | Bit Range | Bits | | | | | | | | | | | | | | | All Resets ⁽¹⁾ | |
|-----------------------------|---------------------------------|-----------|-------------|-------------|-------|-------|-------|--------------|---------|---------|---------|--------------|----------|---------|------------|---------|----------|---------------------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | | 16/0 |
| 2000 | OSCCON | 31:16 | — | — | — | — | — | FRCDIV<2:0> | | | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | COSC<2:0> | | | — | NOSC<2:0> | | CLKLOCK | — | — | SLPEN | CF | — | SOSCEN | OSWEN | xx0x | |
| 2020 | SPLLCON | 31:16 | — | — | — | — | — | PLLODIV<2:0> | | | — | PLLMULT<6:0> | | | | | | 0001 | |
| | | 15:0 | — | — | — | — | — | — | — | — | PLLICK | — | — | — | — | — | — | — | 0000 |
| 20A0 | REFO1CON | 31:16 | — | RODIV<14:0> | | | | | | | | | | | | | | 0000 | |
| | | 15:0 | ON | — | SIDL | OE | RSLP | — | DIVSWEN | ACTIVE | — | — | — | — | ROSEL<3:0> | | | 0000 | |
| 20B0 | REFO1TRIM | 31:16 | ROTRIM<8:0> | | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 20F0 | CLKSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | SPLLRDY | — | LPRCRDY | SOSCRDY | — | POSCRDY | SPDIVRDY | FRCRDY | 0000 |
| 2200 | OSCTUN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | 0000 | |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the FOSCSEL Configuration bits and the type of Reset.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|--------------------------|----------------|----------------|----------------|--------------------------|-----------------------|----------------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | FRCDIV<2:0> | | |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R-y, HS, HC | R-y, HS, HC | R-y, HS, HC | U-0 | R/W-y | R/W-y | R/W-y |
| | — | COSC<2:0> ⁽³⁾ | | | — | NOSC<2:0> ⁽³⁾ | | |
| 7:0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0, HS | U-0 | R/W-y | R/W-y, HC |
| | CLKLOCK | — | — | SLPEN | CF | — | SOSCEN ⁽⁴⁾ | OSWEN ⁽²⁾ |

Legend:

| | | |
|-----------------------------|----------------------------|--|
| HC = Hardware Clearable bit | HS = Hardware Settable bit | y = Value set from Configuration bits on Reset |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits

111 = FRC divided by 256
 110 = FRC divided by 64
 101 = FRC divided by 32
 100 = FRC divided by 16
 011 = FRC divided by 8
 010 = FRC divided by 4
 001 = FRC divided by 2
 000 = FRC divided by 1 (default setting)

bit 23-15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits⁽³⁾

111 and 110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by the FRCDIV<2:0> bits (FRCDIV))
 101 = Internal Low-Power RC (LPRC) Oscillator
 100 = Secondary Oscillator (SOSC)
 011 = Reserved
 010 = Primary Oscillator (POSC) (XT, HS or EC)
 001 = System PLL (SPLL)
 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

bit 11 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to [Section 23.4 “System Registers Write Protection”](#) for details.

2: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) Configuration bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.

3: The Reset value for these bits matches the setting of the FNOSC<2:0> (FOSCSEL<2:0>) Configuration bits.

4: The Reset value for this bit matches the setting of the SOSCEN (FOSCSEL<6>) Configuration bit.

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REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾ (CONTINUED)

- bit 10-8 **NOSC<2:0>**: New Oscillator Selection bits⁽³⁾
111 and 110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV))
101 = Internal Low-Power RC (LPRC) Oscillator
100 = Secondary Oscillator (SOSC)
011 = Reserved
010 = Primary Oscillator (POSC) (XT, HS or EC)
001 = System PLL (SPLL)
000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)
On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (FOSCSEL<2:0>).
- bit 7 **CLKLOCK**: Clock Selection Lock Enable bit
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified
- bit 6-5 **Unimplemented**: Read as '0'
- bit 4 **SLPEN**: Sleep Mode Enable bit
1 = Device will enter Sleep mode when a WAIT instruction is executed
0 = Device will enter Idle mode when a WAIT instruction is executed
- bit 3 **CF**: Clock Fail Detect bit
1 = FSCM has detected a clock failure
0 = No clock failure has been detected
- bit 2 **Unimplemented**: Read as '0'
- bit 1 **SOSCEN**: Secondary Oscillator (SOSC) Enable bit⁽⁴⁾
1 = Enables Secondary Oscillator
0 = Disables Secondary Oscillator
- bit 0 **OSWEN**: Oscillator Switch Enable bit⁽²⁾
1 = Initiates an oscillator switch to a selection specified by the NOSC<2:0> bits
0 = Oscillator switch is complete

- Note 1:** Writes to this register require an unlock sequence. Refer to [Section 23.4 “System Registers Write Protection”](#) for details.
- 2:** The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) Configuration bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.
- 3:** The Reset value for these bits matches the setting of the FNOSC<2:0> (FOSCSEL<2:0>) Configuration bits.
- 4:** The Reset value for this bit matches the setting of the SOSCEN (FOSCSEL<6>) Configuration bit.

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REGISTER 8-2: SPLLCON: SYSTEM PLL CONTROL REGISTER⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | PLLODIV<2:0> | | |
| 23:16 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
| | — | PLLMULT<6:0> | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-y | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | PLLICK | — | — | — | — | — | — | — |

| | |
|-------------------|--|
| Legend: | y = Values set from Configuration bits on Reset |
| R = Readable bit | W = Writable bit U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set '0' = Bit is cleared x = Bit is unknown |

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits

111 = PLL divide-by-256
 110 = PLL divide-by-64
 101 = PLL divide-by-32
 100 = PLL divide-by-16
 011 = PLL divide-by-8
 010 = PLL divide-by-4
 001 = PLL divide-by-2
 000 = PLL divide-by-1 (default setting)

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier bits

111111-0000111 = Reserved
 0000110 = 24x
 0000101 = 12x
 0000100 = 8x
 0000011 = 6x
 0000010 = 4x
 0000001 = 3x (default setting)
 0000000 = 2x

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **PLLICK:** System PLL Input Clock Source bit

1 = FRC is selected as the input to the system PLL (not divided)
 0 = POSC is selected as the input to the system PLL

The POR default value is specified by the PLLSRC Configuration bit in the FOSCSEL register. Refer to [Register 23-9](#) in [Section 23.0 "Special Features"](#) for more information.

bit 6-0 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to [Section 23.4 "System Registers Write Protection"](#) for details. All bits in this register must be modified only if the PLL is not used.

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REGISTER 8-3: REFO1CON: REFERENCE OSCILLATOR CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|-------------------|----------------|----------------|-------------------|---------------------------|----------------|---------------|-----------------------|
| 31:24 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | RODIV<14:8> | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RODIV<7:0> | | | | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0, HC | R-0, HS, HC |
| | ON ⁽¹⁾ | — | SIDL | OE ⁽⁴⁾ | RSLP ^(2,4) | — | DIVSWEN | ACTIVE ⁽¹⁾ |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | ROSEL<3:0> ⁽³⁾ | | | |

| | | |
|-------------------|-----------------------------|--|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits

The value selects the reference clock divider bits (see [Figure 8-1](#) for details). A value of '0' selects no divider.

bit 15 **ON:** Reference Oscillator Output Enable bit⁽¹⁾

1 = Reference oscillator module is enabled
0 = Reference oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit⁽⁴⁾

1 = Reference clock is driven out on the REFCLKO pin
0 = Reference clock is not driven out on the REFCLKO pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit^(2,4)

1 = Reference oscillator module output continues to run in Sleep
0 = Reference oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit

1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit⁽¹⁾

1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.

2: This bit is ignored when the ROSEL<3:0> bits = 0000.

3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

4: Operation with output enabled in Retention Sleep mode is not recommended.

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REGISTER 8-3: REFO1CON: REFERENCE OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 3-0 **ROSEL<3:0>**: Reference Clock Source Select bits⁽³⁾

1111 = Reserved

•

•

1010 = Reserved

1001 = REFCLKI pin

1000 = Reserved

0111 = System PLL output (not divided)

0110 = Reserved

0101 = Secondary Oscillator (SOSC)

0100 = Low-Power RC Oscillator (LPRC)

0011 = Fast RC Oscillator (FRC)

0010 = Primary Oscillator (POSC)

0001 = Instruction/System Clock (SYSCLK)

0000 = Instruction/System Clock (SYSCLK)

- Note 1:** Do not write to this register when the ON bit is not equal to the ACTIVE bit.
- 2:** This bit is ignored when the ROSEL<3:0> bits = 0000.
- 3:** The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
- 4:** Operation with output enabled in Retention Sleep mode is not recommended.

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REGISTER 8-4: REFO1TRIM: REFERENCE OSCILLATOR TRIM REGISTER^(1,2,3)

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ROTRIM<8:1> | | | | | | | | |
| 23:16 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ROTRIM<0> | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-23 **ROTRIM<8:0>**: Reference Oscillator Trim bits

111111111 = 511/512 divisor added to the RODIVx value

111111110 = 510/512 divisor added to the RODIVx value

•

•

•

100000000 = 256/512 divisor added to the RODIVx value

•

•

•

000000010 = 2/512 divisor added to the RODIVx value

000000001 = 1/512 divisor added to the RODIVx value

000000000 = 0 divisor added to the RODIVx value

bit 22-0 **Unimplemented**: Read as '0'

Note 1: While the ON bit (REFO1CON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

2: Do not write to this register when the ON bit (REFO1CON<15>) is not equal to the ACTIVE bit (REFO1CON<8>).

3: Specified values in this register do not take effect if RODIV<14:0> (REFO1CON<30:16>) = 0.

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REGISTER 8-5: CLKSTAT: CLOCK STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0, HS, HC | U-0 | R-0, HS, HC | R-0, HS, HC | U-0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | SPLLRDY | — | LPRCRDY | SOSCRDY | — | POSCRDY | SPDIVRDY | FRCDY |

| | | |
|-------------------|----------------------------|--|
| Legend: | HS = Hardware Settable bit | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **SPLLRDY:** PLL Lock bit

1 = PLL is locked and ready
0 = PLL is not locked

bit 6 **Unimplemented:** Read as '0'

bit 5 **LPRCRDY:** LPRC Oscillator Ready bit

1 = LPRC oscillator is stable and ready
0 = LPRC oscillator is not stable

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready bit

1 = SOSC is stable and ready
0 = SOSC is not stable

bit 3 **Unimplemented:** Read as '0'

bit 2 **POSCRDY:** Primary Oscillator (POSC) Ready bit

1 = POSC is stable and ready
0 = POSC is not stable

bit 1 **SPDIVRDY:** System PLL (with postscaler, SPLLDIV) Clock Ready Status bit

1 = SPLLDIV is stable and ready
0 = SPLLDIV is not stable

bit 0 **FRCDY:** Fast RC (FRC) Oscillator Ready bit

1 = FRC oscillator is stable and ready
0 = FRC oscillator is not stable

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REGISTER 8-6: OSCTUN: FRC TUNING REGISTER⁽¹⁾

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|-------------------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | TUN<5:0> ⁽²⁾ | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits⁽²⁾

100000 = Center frequency – 1.5%

100001

•

•

•

111111

000000 = Center frequency; oscillator runs at 8 MHz

000001

•

•

•

011110

011111 = Center frequency + 1.5%

Note 1: Writes to this register require an unlock sequence. Refer to [Section 23.4 “System Registers Write Protection”](#) for details.

2: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized nor tested.

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NOTES:

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9.0 I/O PORTS

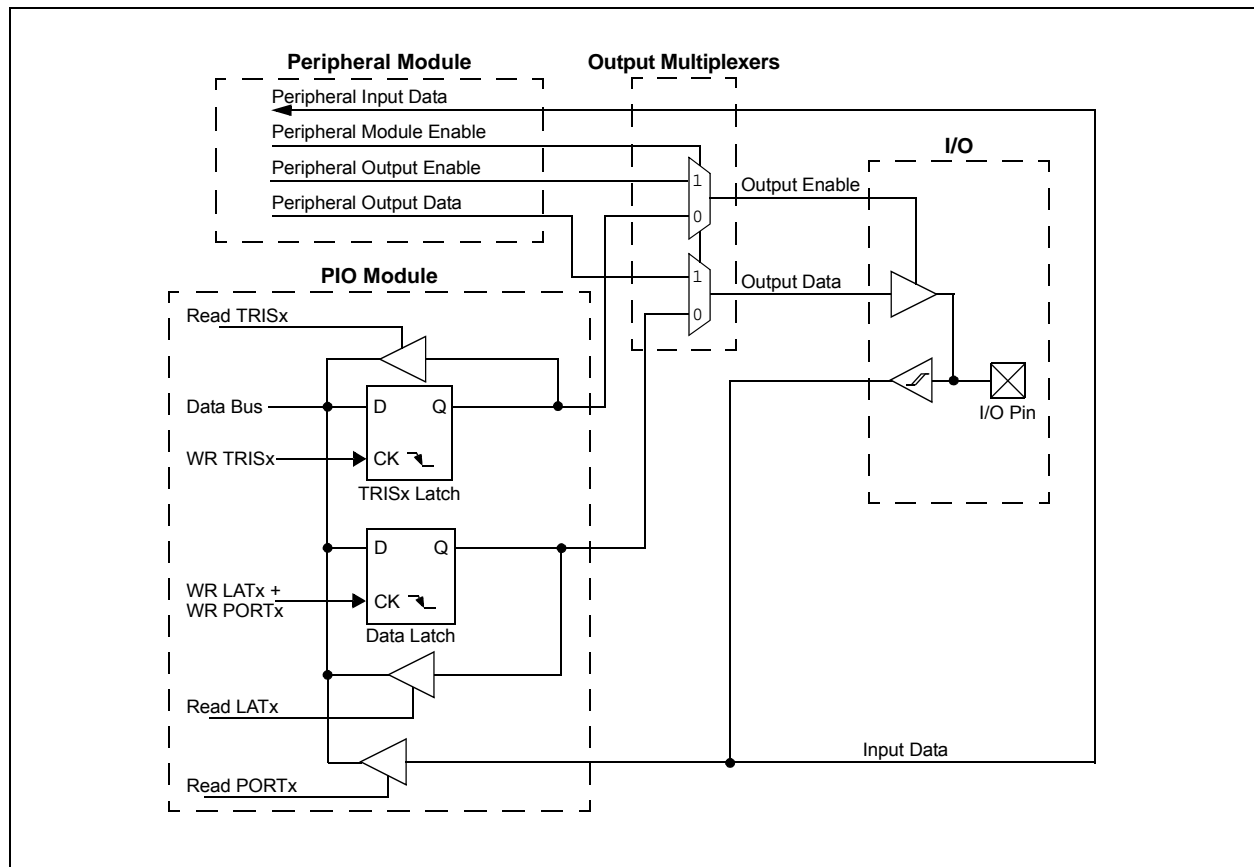
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. “I/O Ports”** (DS60001120) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

Many of the device pins are shared among the peripherals and the Parallel I/O (PIO) ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity. Some pins in the devices are 5V tolerant pins. Some of the key features of the I/O ports are:

- Individual Output Pin Open-Drain Enable/Disable
- Individual Input Pin Weak Pull-up and Pull-Down
- Monitor Selective Inputs and Generate Interrupt when Change-in-Pin State is Detected
- Operation during Sleep and Idle modes
- Fast Bit Manipulation using the CLR, SET and INV registers

Figure 9-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 9-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



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9.1 CLR, SET and INV Registers

Every I/O module register has a corresponding CLR (Clear), SET (Set) and INV (Invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the effects of a write operation to a SET, CLR or INV register, the base register must be read.

9.2 Parallel I/O (PIO) Ports

All port pins have 14 registers directly associated with their operation as digital I/Os. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. The LATx register controls the pin level when it is configured as an output. Reads from the PORTx register read the port pins, while writes to the port pins write the latch, LATx. The I/O state reflected in the PORTx register is synchronized with the system clock and delayed by 3 system clock cycles.

9.3 Open-Drain Configuration

In addition to the PORTx, LATx and TRISx registers for data control, the port pins can also be individually configured for either digital or open-drain outputs. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V), on any desired 5V tolerant pins, by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

9.4 Configuring Analog and Digital Port Pins

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications. The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as timers, UARTs, etc., the corresponding ANSELx bit must be cleared. The ANSELx register has a default value of 0xFFFF. Therefore, all pins that share analog functions are analog (not digital) by default. If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is used by an analog peripheral, such as the ADC or comparator module.

9.5 I/O Port Write/Read Timing

Three instructions cycles are required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP.

9.6 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows the PIC32MM devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State. Five control registers are associated with the Change Notification (CN) functionality of each I/O port. To enable the Change Notification feature for the port, the ON bit (CNCONx<15>) must be set.

The CNEN0x and CNEN1x registers contain the CN interrupt enable control bits for each of the input pins. The setting of these bits enables a CN interrupt for the corresponding pins. Also, these bits, in combination with the CNSTYLE bit (CNCONx<11>), define a type of transition when the interrupt is generated. Possible CN event options are listed in [Table 9-1](#).

TABLE 9-1: CHANGE NOTIFICATION EVENT OPTIONS

| CNSTYLE Bit (CNCONx<11>) | CNEN1x Bit | CNEN0x Bit | Change Notification Event Description |
|--------------------------|-----------------|------------|---|
| 0 | Does not matter | 0 | Disabled |
| 0 | Does not matter | 1 | Detects a mismatch between the last read state and the current state of the pin |
| 1 | 0 | 0 | Disabled |
| 1 | 0 | 1 | Detects a positive transition only (from '0' to '1') |
| 1 | 1 | 0 | Detects a negative transition only (from '1' to '0') |
| 1 | 1 | 1 | Detects both positive and negative transitions |

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit. In addition to the CNSTATx register, the CNFx register is implemented for each port. This register contains flags for Change Notification events. These flags are set if the valid transition edge, selected in the CNEN0x and CNEN1x registers, is detected. CNFx stores the occurrence of the event. CNFx bits must be cleared in software to get the next Change Notification interrupt. The CN interrupt is generated only for the I/Os configured as inputs (corresponding TRISx bits must be set).

9.7 Pin Pull-up and Pull-Down

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source, or sink source, connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

9.8 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features, while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

9.8.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation, "RPn", in their full pin designation, where "RP" designates a Remappable Peripheral and "n" is the remappable port number.

9.8.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (MCCP, SCCP) and others.

In comparison, some digital only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/Os and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

9.8.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

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9.8.4 INPUT MAPPING

The RPINRx registers are used to assign the peripheral input to the required remappable pin, RPn (refer to the peripheral inputs and the corresponding RPINRx registers listed in Table 9-2). Each RPINRx register contains sets of 5-bit fields. Programming these bits with the remappable pin number will connect the peripheral to this RPn pin. Example 9-1 and Figure 9-2 illustrate the remappable pin selection for the U2RX input.

EXAMPLE 9-1: UART2 RX INPUT ASSIGNMENT TO RP9/RB14 PIN

```
RPINR9bits.U2RXR = 9; // connect UART2 RX
                    // input to RP9 pin
```

FIGURE 9-2: REMAPPABLE INPUT EXAMPLE FOR U2RX

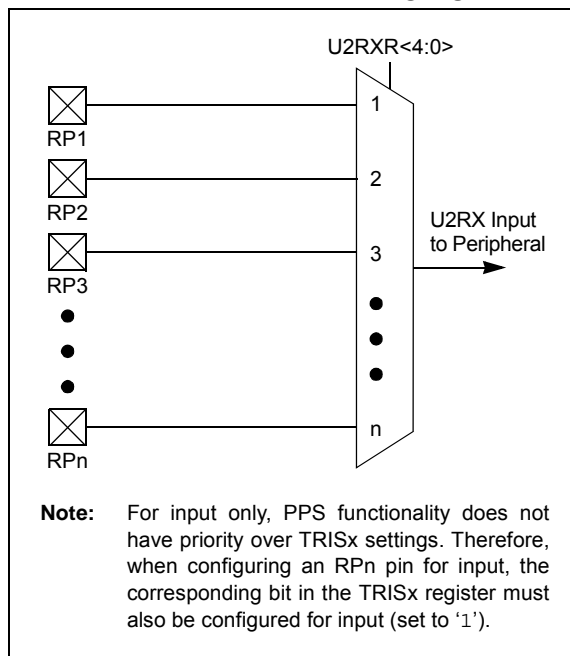


TABLE 9-2: INPUT PIN SELECTION

| Input Name | Function Name | Register | Function Bits |
|-------------------------|--------------------|----------|---------------|
| External Interrupt 4 | INT4 | RPINR1 | INT4R<4:0> |
| MCCP1 Input Capture | ICM1 | RPINR2 | ICM1R<4:0> |
| SCCP2 Input Capture | ICM2 | RPINR2 | ICM2R<4:0> |
| SCCP3 Input Capture | ICM3 | RPINR3 | ICM3R<4:0> |
| Output Compare Fault A | OCFA | RPINR5 | OCFAR<4:0> |
| Output Compare Fault B | OCFB | RPINR5 | OCFBR<4:0> |
| CCP Clock Input A | TCKIA | RPINR6 | TCKIAR<4:0> |
| CCP Clock Input B | TCKIB | RPINR6 | TCKIBR<4:0> |
| UART2 Receive | U2RX | RPINR9 | U2RXR<4:0> |
| UART2 Clear-to-Send | $\overline{U2CTS}$ | RPINR9 | U2CTSR<4:0> |
| SPI2 Data Input | SDI2 | RPINR11 | SDI2R<4:0> |
| SPI2 Clock Input | SCK2IN | RPINR11 | SCK2INR<4:0> |
| SPI2 Slave Select Input | SS2IN | RPINR11 | SS2INR<4:0> |
| CLC Input A | CLCINA | RPINR12 | CLCINAR<4:0> |
| CLC Input B | CLCINB | RPINR12 | CLCINBR<4:0> |

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9.8.5 OUTPUT MAPPING

The RPORx registers are used to assign the peripheral output to the required remappable pin, RPn. Each RPORx register contains 4-bit fields corresponding to the remappable pins. A special value is defined for each peripheral output. This value should be written to the remappable pin bit field in the RPORx register to connect the peripheral output to the RPn pin. All possible (implemented) values for the peripheral's outputs are listed in [Table 9-3](#).

[Example 9-2](#) and [Figure 9-3](#) illustrate the peripheral's output selection for the remappable pin.

EXAMPLE 9-2: UART2 TX OUTPUT ASSIGNMENT TO RP13/RB13 PIN

```
RPOR4bits.RP13R = 1;    // connect UART2 TX (= 1)
                        // to RP13 pin
```

FIGURE 9-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RP1

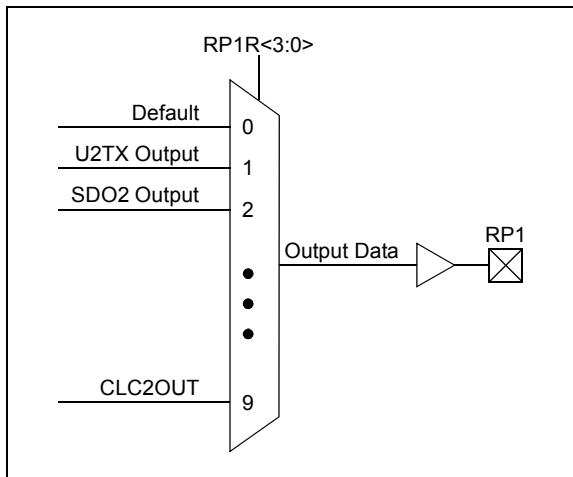


TABLE 9-3: OUTPUT PIN SELECTION

| Output Function Number | Function | Output Name |
|------------------------|----------------------|--------------------------|
| 0 | None (not connected) | — |
| 1 | U2TX | UART2 Transmit |
| 2 | $\overline{U2RTS}$ | UART2 Request-to-Send |
| 3 | SDO2 | SPI2 Data Output |
| 4 | SCK2OUT | SPI2 Clock Output |
| 5 | SS2OUT | SPI2 Slave Select Output |
| 6 | OCM2 | SCCP2 Output Compare |
| 7 | OCM3 | SCCP3 Output Compare |
| 8 | CLC1OUT | CLC1 Output |
| 9 | CLC2OUT | CLC2 Output |

9.8.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MM0064GPL036 family devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

9.8.6.1 Control Register Lock

Under normal operation, the RPORx and RPINRx registers can be written, but they can also be locked to prevent accidental writes. This feature is controlled by the IOLOCK bit in the RPCON register. If the IOLOCK bit is set, then the contents of the RPORx and RPINRx registers cannot be changed.

To modify the IOLOCK bit, an unlock sequence must be executed. Refer to [Section 23.4 “System Registers Write Protection”](#) for details.

9.9 I/O Ports Control Registers

TABLE 9-4: PORTA REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽³⁾ | Bit Range | Bits | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|-------|---------|---------------------------|------|------|------|------|------|------|--------------|------|---------------|-------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | | 17/1 |
| 2600 | ANSELA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | ANSA<3:0> | | | 000F |
| 2610 | TRISA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | TRISA9 ^(1,2) | — | — | — | — | — | — | TRISA<4:0> | | | 021F |
| 2620 | PORTA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | RA9 ^(1,2) | — | — | — | — | — | — | RA<4:0> | | | xxxxx |
| 2630 | LATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | LATA9 ^(1,2) | — | — | — | — | — | — | LATA<4:0> | | | 0000 |
| 2640 | ODCA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | ODCA9 ^(1,2) | — | — | — | — | — | — | ODCA<4:0> | | | 0000 |
| 2650 | CNPUA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | CNPUA9 ^(1,2) | — | — | — | — | — | — | CNPUA<4:0> | | | 0000 |
| 2660 | CNPDA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | CNPDA9 ^(1,2) | — | — | — | — | — | — | CNPDA<4:0> | | | 0000 |
| 2670 | CNCONA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | CNSTYLE | — | — | — | — | — | — | — | — | — | — | 0000 |
| 2680 | CNEN0A | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | CNIEA9 ^(1,2) | — | — | — | — | — | — | CNIEA<4:0> | | | 0000 |
| 2690 | CNSTATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | CNSTATA9 ^(1,2) | — | — | — | — | — | — | CNSTATA<4:0> | | | 0000 |
| 26A0 | CNEN1A | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | CNIE1A9 ^(1,2) | — | — | — | — | — | — | CNIE1A<4:0> | | | 0000 |
| 26B0 | CNFA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | CNFA9 ^(1,2) | — | — | — | — | — | — | CNFA<4:0> | | | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits are not implemented in 20-pin devices.

2: These bits are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

TABLE 9-5: PORTB REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽²⁾ | Bit Range | Bits | | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|------------------------------|-------|-------|-------|---------|-------|------|------|------|------|------|------|--------------------------|------|------|---------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | | 16/0 |
| 2700 | ANSELB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ANSB<15:12> | | | | | | — | — | — | — | — | — | ANSB<3:0> ⁽¹⁾ | | | F00F | |
| 2710 | TRISB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISB<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | FFFF | |
| 2720 | PORTB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RB<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | 0000 | |
| 2730 | LATB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATB<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | 0000 | |
| 2740 | ODCB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCB<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | 0000 | |
| 2750 | CNPUB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUB<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | 0000 | |
| 2760 | CNPDB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDB<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | 0000 | |
| 2770 | CNCONB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | CNSTYLE | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 2780 | CNEN0B | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEB<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | 0000 | |
| 2790 | CNSTATB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNSTATB<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | 0000 | |
| 27A0 | CNEN1B | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIE1B<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | 0000 | |
| 27B0 | CNFB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNFB<15:0> ⁽¹⁾ | | | | | | | | | | | | | | | 0000 | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits<11:10,6:5,3> are not implemented in 20-pin devices.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

TABLE 9-6: PORTC REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽³⁾ | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|-----------------------------|---------------------------------|-----------|-------------------|-------|-------|-------|------------------------|-------|-------------------------------|------|------|------|------|------|------|------|-------------------------------|----------------------------|---------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2800 | ANSEL_C | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ANSC<1:0> ^(1,2) | 0003 |
| 2810 | TRISC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | TRISC<9:8> ^(1,2) | — | — | — | — | — | — | — | TRISC<3:0> ^(1,2) | — | 030F |
| 2820 | PORTC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | RC<9:8> ^(1,2) | — | — | — | — | — | — | — | RC<3:0> ^(1,2) | — | 0000 |
| 2830 | LATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | LATC<9:8> ^(1,2) | — | — | — | — | — | — | — | LATC<3:0> ^(1,2) | — | 0000 |
| 2840 | ODCC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ODCC<9:8> ^(1,2) | — | — | — | — | — | — | — | ODCC<3:0> ^(1,2) | — | 0000 |
| 2850 | CNPUC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPUC<9:8> ^(1,2) | — | — | — | — | — | — | — | CNPUC<3:0> ^(1,2) | — | 0000 |
| 2860 | CNPDC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPDC<9:8> ^(1,2) | — | — | — | — | — | — | — | CNPDC<3:0> ^(1,2) | — | 0000 |
| 2870 | CNCONC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON ⁽¹⁾ | — | — | — | CNSTYLE ⁽¹⁾ | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 2880 | CNEN0C | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNIE0C<9:8> ^(1,2) | — | — | — | — | — | — | — | CNIE0C<3:0> ^(1,2) | — | 0000 |
| 2890 | CNSTATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNSTATC<9:8> ^(1,2) | — | — | — | — | — | — | — | CNSTATC<3:0> ^(1,2) | — | 0000 |
| 28A0 | CNEN1C | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNIE1C<9:8> ^(1,2) | — | — | — | — | — | — | — | CNIE1C<3:0> ^(1,2) | — | 0000 |
| 28B0 | CNFC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNFC<9:8> ^(1,2) | — | — | — | — | — | — | — | CNFC<3:0> ^(1,2) | — | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits<15,11,9:8,3:0> are not implemented in 20-pin devices.

2: Bits<8,3:0> are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

TABLE 9-7: PERIPHERAL PIN SELECT REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets | | |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|-------|--------|-------|------|------|------|------|------|------|------|------|------|------|--------------|--------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | | | |
| 2480 | RPCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | | |
| | | 15:0 | — | — | — | — | IOLOCK | — | — | — | — | — | — | — | — | — | — | — | 0000 | | |
| 24A0 | RPINR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | | |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | INT4R<4:0> | 0000 | |
| 24B0 | RPINR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ICM2R<4:0> | ICM1R<4:0> | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 24C0 | RPINR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ICM3R<4:0> | — | 0000 |
| 24E0 | RPINR5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | OCFBR<4:0> | OCFAR<4:0> | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 24F0 | RPINR6 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TCKIBR<4:0> | TCKIAR<4:0> | 0000 |
| 2520 | RPINR9 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | U2CTSR<4:0> | U2RXR<4:0> | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 2540 | RPINR11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS2INR<4:0> | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SCK2INR<4:0> | SDI2R<4:0> | 0000 |
| 2550 | RPINR12 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CLCINBR<4:0> | CLCINAR<4:0> | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 2590 | RPOR0 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP4R<3:0> | RP3R<3:0> | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP2R<3:0> | RP1R<3:0> | 0000 |
| 25A0 | RPOR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP8R<3:0> | RP7R<3:0> | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP6R<3:0> | RP5R<3:0> | 0000 |
| 25B0 | RPOR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP12R<3:0> | RP11R<3:0> | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP10R<3:0> | RP9R<3:0> | 0000 |
| 25C0 | RPOR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP16R<3:0> | RP15R<3:0> | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP14R<3:0> | RP13R<3:0> | 0000 |
| 25D0 | RPOR4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP20R<3:0> | RP19R<3:0> | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RP18R<3:0> | RP17R<3:0> | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

PIC32MM0064GPL036 FAMILY

REGISTER 9-1: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER (x = A-C)

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 |
| | ON | — | — | — | CNSTYLE | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notification (CN) Control On bit

1 = CN is enabled

0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CNSTYLE:** Change Notification Style Selection bit

1 = Edge style (detects edge transitions, CNFx bits are used for a Change Notice event)

0 = Mismatch style (detects change from last PORTx read, CNSTATx bits are used for a Change Notification event)

bit 10-0 **Unimplemented:** Read as '0'

PIC32MM0064GPL036 FAMILY

10.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. “Timers”** (DS60001105) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

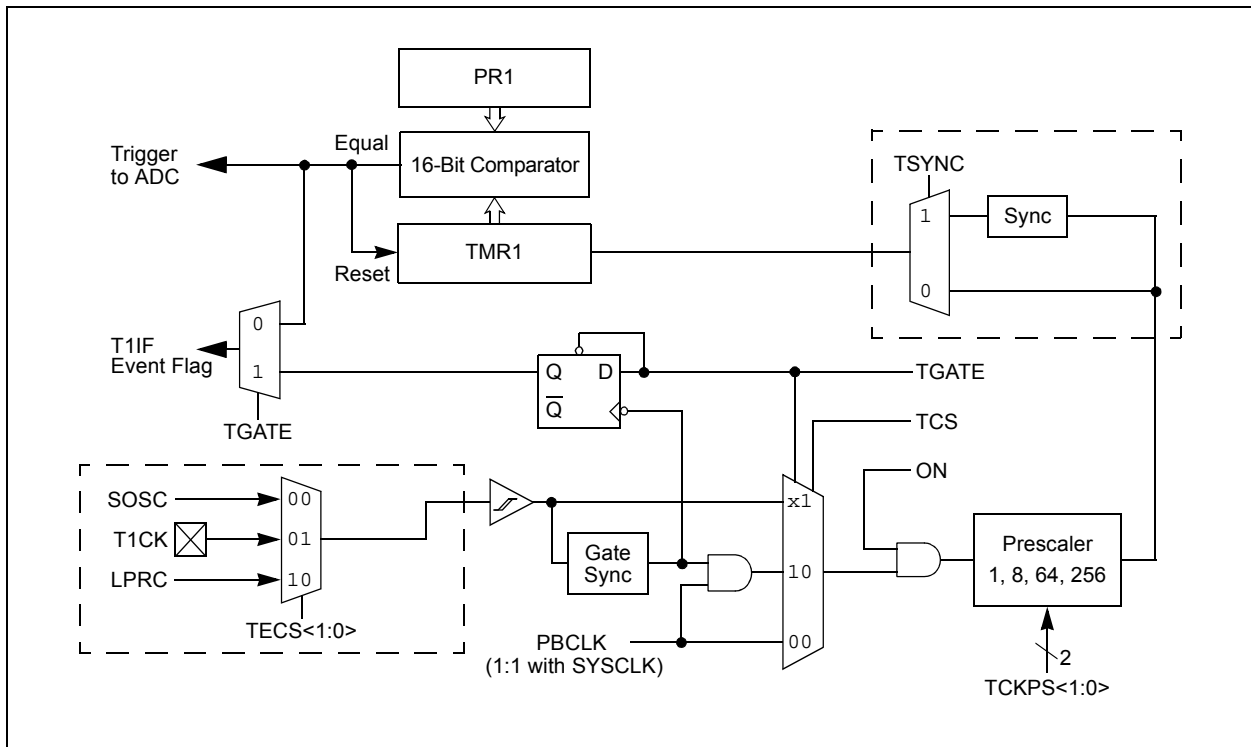
PIC32MM0064GPL036 family devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can be clocked from different sources, such as the Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK), Secondary Oscillator (SOSC), T1CK pin or LPRC oscillator.

The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

The timer has a selectable clock prescaler and can operate in Sleep and Idle modes.

FIGURE 10-1: TIMER1 BLOCK DIAGRAM



10.1 Timer1 Control Register

TABLE 10-1: TIMER1 REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|------------|-------|-------|-------|-------|-------|-----------|-------|------|------------|------|-------|------|------|------|------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | | 16/0 |
| 8000 | T1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | TWDIS | TWIP | — | TECS<1:0> | TGATE | — | TCKPS<1:0> | — | TSYNC | TCS | — | — | — | 0000 |
| 8010 | TMR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR1<15:0> | | | | | | | | | | | | | | | 0000 | |
| 8020 | PR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR1<15:0> | | | | | | | | | | | | | | | FFFF | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

PIC32MM0064GPL036 FAMILY

REGISTER 10-1: T1CON: TIMER1 CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|---------------------|----------------|----------------|----------------|--------------------|---------------|
| 31:24 | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — |
| 23:16 | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — |
| 15:8 | R/W-0 ON | U-0 — | R/W-0 SIDL | R/W-0 TWDIS | R-0 TWIP | U-0 — | R/W-0 TECS<1:0> | R/W-0 — |
| 7:0 | R/W-0 TGATE | U-0 — | R/W-0 TCKPS<1:0> | R/W-0 — | U-0 — | R/W-0 TSYNC | R/W-0 TCS | U-0 — |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-16 **Unimplemented:** Read as '0'
- bit 15 **ON:** Timer1 On bit
 1 = Timer1 is enabled
 0 = Timer1 is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SIDL:** Timer1 Stop in Idle Mode bit
 1 = Discontinues operation when device enters Idle mode
 0 = Continues operation even in Idle mode
- bit 12 **TWDIS:** Asynchronous Timer1 Write Disable bit
 1 = Writes to TMR1 are ignored until pending write operation completes
 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer mode functionality)
- bit 11 **TWIP:** Asynchronous Timer1 Write in Progress bit
In Asynchronous Timer1 mode:
 1 = Asynchronous write to TMR1 register is in progress
 0 = Asynchronous write to TMR1 register is complete
In Synchronous Timer1 mode:
 This bit is read as '0'.
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
 11 = Reserved
 10 = External clock comes from the LPRC
 01 = External clock comes from the T1CK Pin
 00 = External clock comes from the Secondary Oscillator (SOSC)
- bit 7 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
 This bit is ignored.
When TCS = 0:
 1 = Gated time accumulation is enabled
 0 = Gated time accumulation is disabled
- bit 6 **Unimplemented:** Read as '0'
- bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
 11 = 1:256 prescale value
 10 = 1:64 prescale value
 01 = 1:8 prescale value
 00 = 1:1 prescale value

PIC32MM0064GPL036 FAMILY

REGISTER 10-1: T1CON: TIMER1 CONTROL REGISTER (CONTINUED)

- bit 3 **Unimplemented:** Read as '0'
- bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Selection bit
 When TCS = 1:
 1 = External clock input is synchronized
 0 = External clock input is not synchronized
 When TCS = 0:
 This bit is ignored.
- bit 1 **TCS:** Timer1 Clock Source Select bit
 1 = External clock is defined by the TECS<1:0> bits
 0 = Internal peripheral clock
- bit 0 **Unimplemented:** Read as '0'

PIC32MM0064GPL036 FAMILY

11.0 WATCHDOG TIMER (WDT)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 62. “Dual Watchdog Timer”** (DS60001365) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

When enabled, the Watchdog Timer (WDT) can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are:

- Configuration or Software Controlled
- User-Configurable Time-out Period
- Different Time-out Periods for Run and Sleep/Idle modes
- Operates from LPRC Oscillator in Sleep/Idle modes
- Different Clock Sources for Run mode
- Can Wake the Device from Sleep or Idle

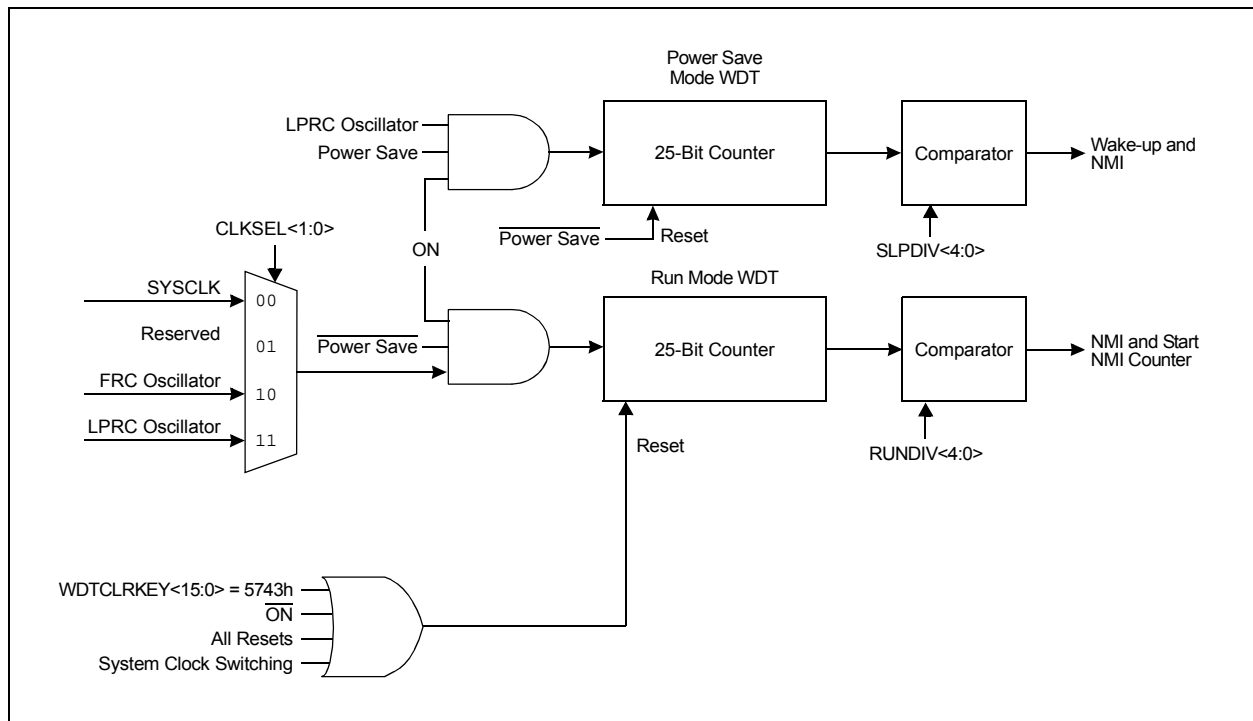
The Watchdog Timer can be cleared by writing the 16-bit value, 0x5743, to the upper half of the WDTCON register.

EXAMPLE 11-1: CODE SEQUENCE TO CLEAR THE WDT

```
unsigned short *pWdtClr; // 16-bit variable
// create a pointer to the upper half of WDTCON
pWdtClr = (unsigned short*)&WDTCON + 1;

main()
{
    ...user code
    *pWdtClr = 0x5743; // clear the WDT
}
```

FIGURE 11-1: WATCHDOG TIMER BLOCK DIAGRAM



11.1 Watchdog Timer Control Registers

TABLE 11-1: WATCHDOG TIMER REGISTER MAP

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|-----------------------------|-----------------------|-----------|-----------------|-------|-------|-------------|-------|-------|-------------|------|------|-------------|------|------|----------|-------|------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | |
| 3E80 | WDTCON ⁽¹⁾ | 31:16 | WDTCLRKEY<15:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | ON | — | — | RUNDIV<4:0> | | | CLKSEL<1:0> | | | SLPDIV<4:0> | | | WDTWINEN | xxxxx | | |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

PIC32MM0064GPL036 FAMILY

REGISTER 11-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------------------------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| WDTCLRKEY<15:8> | | | | | | | | |
| 23:16 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| WDTCLRKEY<7:0> | | | | | | | | |
| 15:8 | R/W-0 | U-0 | U-0 | R-y | R-y | R-y | R-y | R-y |
| ON ⁽¹⁾ — — RUNDIV<4:0> | | | | | | | | |
| 7:0 | R-y | R-y | R-y | R-y | R-y | R-y | R-y | R/W-y |
| CLKSEL<1:0> | | | SLPDIV<4:0> | | | | | WDTWINEN |

| | |
|-------------------|--|
| Legend: | y = Values set from Configuration bits on Reset |
| R = Readable bit | W = Writable bit U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set '0' = Bit is cleared x = Bit is unknown |

bit 31-16 **WDTCLRKEY<15:0>**: Watchdog Timer Clear Key bits

To clear the Watchdog Timer to prevent a time-out, software must write the value, 0x5743, to this location using a single 16-bit write.

bit 15 **ON**: Watchdog Timer Enable bit⁽¹⁾

1 = The WDT is enabled
0 = The WDT is disabled

bit 14-13 **Unimplemented**: Read as '0'

bit 12-8 **RUNDIV<4:0>**: Shadow Copy of Watchdog Timer Postscaler Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RWDTPS<4:0> Configuration bits in FWDT.

bit 7-6 **CLKSEL<1:0>**: Shadow Copy of Watchdog Timer Clock Selection Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RCLKSEL<1:0> Configuration bits in FWDT.

bit 5-1 **SLPDIV<4:0>**: Shadow Copy of Watchdog Timer Postscaler Value for Sleep/Idle Mode from Configuration bits
On Reset, these bits are set to the values of the SWDTPS<4:0> Configuration bits in FWDT.

bit 0 **WDTWINEN**: Watchdog Timer Window Enable bit

On Reset, this bit is set to the inverse of the value of the inverse of the WINDIS Configuration bit in FWDT.
1 = Windowed mode is enabled
0 = Windowed mode is disabled

Note 1: This bit only has control when FWDTEN (FWDT<15>) = 0.

PIC32MM0064GPL036 FAMILY

NOTES:

12.0 CAPTURE/COMPARE/PWM/TIMER MODULES (MCCP AND SCCP)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 30. “Capture/Compare/PWM/Timer (MCCP and SCCP)”** (DS60001381) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

12.1 Introduction

PIC32MM0064GPL036 family devices include three Capture/Compare/PWM/Timer (CCP) modules. These modules are similar to the multipurpose timer modules found on many other 32-bit microcontrollers. They also provide the functionality of the comparable input capture, output compare and general purpose timer peripherals found in all earlier PIC32 devices.

CCP modules can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

There are two different forms of the module, distinguished by the number of PWM outputs that the module can generate. Single Capture/Compare/PWM/Timer (SCCPs) output modules provide only one PWM output. Multiple Capture/Compare/PWM/Timer (MCCPs) output modules can provide up to six outputs and an extended range of output control features, depending on the pin count of the particular device.

All modules (SCCP and MCCP) include these features:

- User-Selectable Clock Inputs, including System Clock and External Clock Input Pins
- Input Clock Prescaler for Time Base
- Output Postscaler for module Interrupt Events or Triggers
- Synchronization Output Signal for Coordinating other MCCP/SCCP modules with User-Configurable Alternate and Auxiliary Source Options

- Fully Asynchronous Operation in All Modes and in Low-Power Operation
- Special Output Trigger for ADC Conversions
- 16-Bit and 32-Bit General Purpose Timer modes with Optional Gated Operation for Simple Time Measurements
- Capture modes:
 - Backward compatible with previous input capture peripherals of the PIC32 family
 - 16-bit or 32-bit capture of time base on external event
 - Up to four-level deep FIFO capture buffer
 - Capture source input multiplexer
 - Gated capture operation to reduce noise-induced false captures
- Output Compare/PWM modes:
 - Backward compatible with previous output compare peripherals of the PIC32 family
 - Single Edge and Dual Edge Compare modes
 - External Input mode

MCCP modules also include these extended PWM features:

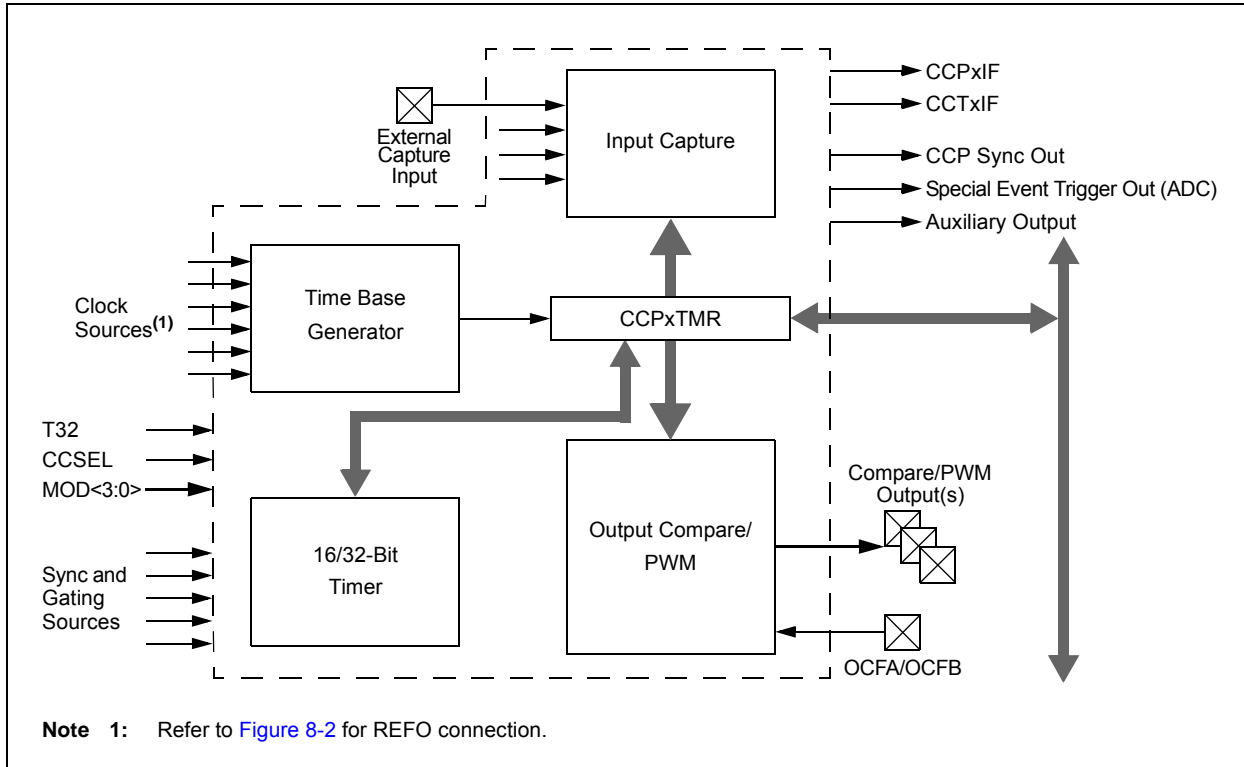
- Single Output Steerable mode
- Brush DC Motor (Forward and Reverse) modes
- Half-Bridge with Dead-Time Delay mode
- Push-Pull PWM mode
- Output Scan mode
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity
- Center-Aligned Compare mode
- Variable Frequency Pulse mode

The SCCP and MCCP modules can be operated in only one of the three major modes (Capture, Compare or Timer) at any time. The other modes are not available unless the module is reconfigured.

A conceptual block diagram for the module is shown in [Figure 12-1](#). All three modes use the time base generator and the common Timer register pair (CCPxTMR). Other shared hardware components, such as comparators and buffer registers, are activated and used as a particular mode requires.

PIC32MM0064GPL036 FAMILY

FIGURE 12-1: MCCP/SCCP CONCEPTUAL BLOCK DIAGRAM



12.2 Registers

Each MCCP/SCCP module has up to seven control and status registers:

- CCPxCON1 ([Register 12-1](#)) controls many of the features common to all modes, including input clock selection, time base prescaling, timer synchronization, Trigger mode operations and postscaler selection for all modes. The module is also enabled and the operational mode is selected from this register.
- CCPxCON2 ([Register 12-2](#)) controls auto-shutdown and restart operation, primarily for PWM operations, and also configures other input capture and output compare features, and configures auxiliary output operation.
- CCPxCON3 ([Register 12-3](#)) controls multiple output PWM dead time, controls the output of the output compare and PWM modes, and configures the PWM Output mode for the MCCP modules.
- CCPxSTAT ([Register 12-4](#)) contains read-only status bits showing the state of module operations.

Each module also includes eight buffer/counter registers that serve as Timer Value registers or data holding buffers:

- CCPxTMR is the 32-Bit Timer/Counter register
- CCPxPR is the 32-Bit Timer Period register
- CCPxR is the 32-bit primary data buffer for output compare operations
- CCPxBUF(H/L) registers are the 32-bit buffer register pair, which are used in input capture FIFO operations

TABLE 12-1: MCCP/SCCP REGISTER MAP

| Virtual Address (BF80 :#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | All Resets | | |
|------------------------------|---------------------------------|--------------|-----------------|------------|-------|--------|----------|-------------|-------|--------|------------|---------|-----------|-------------|-------------|----------|-------------|---------------|------|-------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | | 16/0 | |
| 0100 | CCP1CON1 | 31:16 | OPSSRC | RTRGEN | — | — | OPS<3:0> | | | TRIGEN | ONESHOT | ALTSYNC | SYNC<4:0> | | | | | 0000 | | |
| | | 15:0 | ON | — | SIDL | CCPSLP | TMRSYNC | CLKSEL<2:0> | | | TMRPS<1:0> | | T32 | CCSEL | MOD<3:0> | | | 0000 | | |
| 0110 | CCP1CON2 | 31:16 | OENSYNC | — | OCFEN | OCEEN | OCDEN | OCCEN | OCBEN | OCAEN | ICGSM<1:0> | | — | AUXOUT<1:0> | | ICS<2:0> | | 0100 | | |
| | | 15:0 | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG<7:0> | | | | | | | 0000 | | |
| 0120 | CCP1CON3 | 31:16 | OETRIG | OSCNT<2:0> | | | — | OUTM<2:0> | | | — | — | POLACE | POLBDF | PSSACE<1:0> | | PSSBDF<1:0> | | 0000 | |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | DT<5:0> | | | | | | 0000 | |
| 0130 | CCP1STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | PRLWIP | TMRHWIP | TMRLWIP | RBWIP | RAWIP | 0000 | |
| | | 15:0 | — | — | — | — | — | — | — | ICGARM | — | — | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE |
| 0140 | CCP1TMR | 31:16 | CCP1 TMRH<15:0> | | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | CCP1 TMRL<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0150 | CCP1PR | 31:16 | CCP1 PRH<15:0> | | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | CCP1 PRL<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0160 | CCP1RA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPA<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0170 | CCP1RB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPB<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0180 | CCP1BUF | 31:16 | CCP1 BUFH<15:0> | | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | CCP1 BUFL<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0200 | CCP2CON1 | 31:16 | OPSSRC | RTRGEN | — | — | OPS<3:0> | | | TRIGEN | ONESHOT | ALTSYNC | SYNC<4:0> | | | | | 0000 | | |
| | | 15:0 | ON | — | SIDL | CCPSLP | TMRSYNC | CLKSEL<2:0> | | | TMRPS<1:0> | | T32 | CCSEL | MOD<3:0> | | | 0000 | | |
| 0210 | CCP2CON2 | 31:16 | OENSYNC | — | — | — | — | — | — | OCAEN | ICGSM<1:0> | | — | AUXOUT<1:0> | | ICS<2:0> | | 0100 | | |
| | | 15:0 | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG<7:0> | | | | | | | 0000 | | |
| 0220 | CCP2CON3 | 31:16 | OETRIG | — | — | — | — | — | — | — | — | — | POLACE | — | PSSACE<1:0> | | — | — | 0000 | |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 0230 | CCP2STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | PRLWIP | TMRHWIP | TMRLWIP | RBWIP | RAWIP | 0000 | |
| | | 15:0 | — | — | — | — | — | — | — | ICGARM | — | — | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE |
| 0240 | CCP2TMR | 31:16 | CCP2 TMRH<15:0> | | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | CCP2 TMRL<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0250 | CCP2PR | 31:16 | CCP2 PRH<15:0> | | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | CCP2 PRL<15:0> | | | | | | | | | | | | | | | 0000 | | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

TABLE 12-1: MCCP/SCCP REGISTER MAP (CONTINUED)

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | All Resets | | |
|-----------------------------|---------------------------------|-----------|-----------------|------------|-------|--------|----------|-------------|--------|------------|------------|---------|---------|-------------|-------------|----------|---------|---------------|-------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | | 16/0 | |
| 0260 | CCP2RA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |
| | | 15:0 | CMPA<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0270 | CCP2RB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |
| | | 15:0 | CMPB<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0280 | CCP2BUF | 31:16 | CCP2 BUFH<15:0> | | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | CCP2 BUFL<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0300 | CCP3CON1 | 31:16 | OPSSRC | RTRGEN | — | — | OPS<3:0> | | | | TRIGEN | ONESHOT | ALTSYNC | SYNC<4:0> | | | | 0000 | | |
| | | 15:0 | ON | — | SIDL | CCPSLP | TMRSYNC | CLKSEL<2:0> | | TMRPS<1:0> | | T32 | CCSEL | MOD<3:0> | | | 0000 | | | |
| 0310 | CCP3CON2 | 31:16 | OENSYNC | — | — | — | — | — | — | OCAEN | ICGSM<1:0> | | — | AUXOUT<1:0> | | ICS<2:0> | | 0100 | | |
| | | 15:0 | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG<7:0> | | | | | | | 0000 | | |
| 0320 | CCP3CON3 | 31:16 | OETRIG | OSCNT<2:0> | | | — | — | — | — | — | — | POLACE | — | PSSACE<1:0> | | — | — | 0000 | |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |
| 0330 | CCP3STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | PRLWIP | TMRHWIP | TMRLWIP | RBWIP | RAWIP | 0000 |
| | | 15:0 | — | — | — | — | — | — | ICGARM | — | — | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE | 0000 |
| 0340 | CCP3TMR | 31:16 | CCP3 TMRH<15:0> | | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | CCP3 TMRL<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0350 | CCP3PR | 31:16 | CCP3 PRH<15:0> | | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | CCP3 PRL<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0360 | CCP3RA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |
| | | 15:0 | CMPA<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0370 | CCP3RB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |
| | | 15:0 | CMPB<15:0> | | | | | | | | | | | | | | | 0000 | | |
| 0380 | CCP3BUF | 31:16 | CCP3 BUFH<15:0> | | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | CCP3 BUFL<15:0> | | | | | | | | | | | | | | | 0000 | | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

PIC32MM0064GPL036 FAMILY

REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|-----------------------|-----------------------|----------------|----------------|-------------------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | OPSSRC ⁽¹⁾ | RTRGEN ⁽²⁾ | — | — | OPS<3:0> ⁽³⁾ | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TRIGEN | ONESHOT | ALTSYNC | SYNC<4:0> | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON ⁽⁴⁾ | — | SIDL | CCPSLP | TMRSYNC | CLKSEL<2:0> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TMRPS<1:0> | | T32 | CCSEL | MOD<3:0> | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **OPSSRC:** Output Postscaler Source Select bit⁽¹⁾
 1 = Output postscaler scales the Special Event Trigger output events
 0 = Output postscaler scales the timer interrupt events
- bit 30 **RTRGEN:** Retrigger Enable bit⁽²⁾
 1 = Time base can be retrIGGERED when CCPTRIG = 1
 0 = Time base may not be retrIGGERED when CCPTRIG = 1
- bit 29-28 **Unimplemented:** Read as '0'
- bit 27-24 **OPS<3:0>:** CCPx Interrupt Output Postscale Select bits⁽³⁾
 1111 = Interrupt every 16th time base period match
 1110 = Interrupt every 15th time base period match
 ...
 0100 = Interrupt every 5th time base period match
 0011 = Interrupt every 4th time base period match or 4th input capture event
 0010 = Interrupt every 3rd time base period match or 3rd input capture event
 0001 = Interrupt every 2nd time base period match or 2nd input capture event
 0000 = Interrupt after each time base period match or input capture event
- bit 23 **TRIGEN:** CCPx Triggered Enable bit
 1 = Triggered operation of the timer is enabled
 0 = Triggered operation of the timer is disabled
- bit 22 **ONESHOT:** One-Shot Mode Enable bit
 1 = One-Shot Triggered mode is enabled; trigger duration is set by OSCNT<2:0>
 0 = One-Shot Triggered mode is disabled
- bit 21 **ALTSYNC:** CCPx Clock Select bit
 1 = An alternate signal is used as the module synchronization output signal
 0 = The module synchronization output signal is the Time Base Reset/rollover event

- Note 1:** This control bit has no function in Input Capture modes.
Note 2: This control bit has no function when TRIGEN = 0.
Note 3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.
Note 4: Refer to [Figure 8-2](#) for REFO connection.
Note 5: Not available on SCCP modules.

PIC32MM0064GPL036 FAMILY

REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

bit 20-16 **SYNC<4:0>**: CCPx Synchronization Source Select bits

11111 = Timer is in the Free-Running mode and rolls over at FFFFh (Timer Period register is ignored)

11110 = Reserved

...

11100 = Reserved

11011 = Time base is synchronized to the start of ADC conversion

11010 = Reserved

11001 = Time base is synchronized to Comparator 2

11000 = Time base is synchronized to Comparator 1

10111 = Reserved

...

10010 = Reserved

10001 = Time base is synchronized to CLC2

10000 = Time base is synchronized to CLC1

01111 = Reserved

01110 = Reserved

01101 = Time base is synchronized to the INT4 pin (remappable)

01100 = Time base is synchronized to the INT3 pin

01011 = Time base is synchronized to the INT2 pin

01010 = Time base is synchronized to the INT1 pin

01001 = Time base is synchronized to the INT0 pin

01000 = Reserved

...

00101 = Reserved

00100 = Time base is synchronized to SCCP3

00011 = Time base is synchronized to SCCP2

00010 = Time base is synchronized to MCCP1

00001 = Time base is synchronized to this MCCP/SCCP

00000 = No external synchronization; timer rolls over at FFFFh or matches with the Timer Period register

bit 15 **ON**: CCPx Module Enable bit⁽¹⁾

1 = Module is enabled with the operating mode specified by the MOD<3:0> bits

0 = Module is disabled

bit 14 **Unimplemented**: Read as '0'

bit 13 **SIDL**: CCPx Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12 **CCPSLP**: CCPx Sleep Mode Enable bit

1 = Module continues to operate in Sleep modes

0 = Module does not operate in Sleep modes

bit 11 **TMRSYNC**: Time Base Clock Synchronization bit

1 = Module time base clock is synchronized to internal system clocks; timing restrictions apply

0 = Module time base clock is not synchronized to internal system clocks

Note 1: This control bit has no function in Input Capture modes.

2: This control bit has no function when TRIGEN = 0.

3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

4: Refer to [Figure 8-2](#) for REFO connection.

5: Not available on SCCP modules.

PIC32MM0064GPL036 FAMILY

REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

- bit 10-8 **CLKSEL<2:0>**: CCPx Time Base Clock Select bits
111 = TCKIA pin (remappable)
110 = TCKIB pin (remappable)
101 = Reserved
100 = Reserved
011 = CLC1 output for M CCP1 and SCCP2/CLC2 output for SCCP3
010 = Secondary Oscillator (SOSC) clock
001 = REFCLKO output clock⁽⁴⁾
000 = System clock (FSYS)
- bit 7-6 **TMRPS<1:0>**: CCPx Time Base Prescale Select bits
11 = 1:64 prescaler
10 = 1:16 prescaler
01 = 1:4 prescaler
00 = 1:1 prescaler
- bit 5 **T32**: 32-Bit Time Base Select bit
1 = 32-bit time base for timer, single edge output compare or input capture function
0 = 16-bit time base for timer, single edge output compare or input capture function
- bit 4 **CCSEL**: Capture/Compare Mode Select bit
1 = Input Capture mode
0 = Output Compare/PWM or Timer mode (exact function is selected by the MOD<3:0> bits)
- bit 3-0 **MOD<3:0>**: CCPx Mode Select bits
CCSEL = 1 (Input Capture modes):
1xxx = Reserved
011x = Reserved
0101 = Capture every 16th rising edge
0100 = Capture every 4th rising edge
0011 = Capture every rising and falling edge
0010 = Capture every falling edge
0001 = Capture every rising edge
0000 = Capture every rising and falling edge (Edge Detect mode)
CCSEL = 0 (Output Compare modes):
1111 = External Input mode: Pulse generator is disabled, source is selected by ICS<2:0>
1110 = Reserved
110x = Reserved
10xx = Reserved
0111 = Variable Frequency Pulse mode⁽⁵⁾
0110 = Center-Aligned PWM mode, buffered⁽⁵⁾
0101 = Dual Edge PWM mode, buffered
0100 = Dual Edge Compare mode
0011 = 16-Bit/32-Bit Single Edge mode: Toggles output on compare match
0010 = 16-Bit/32-Bit Single Edge mode: Drives output low on compare match
0001 = 16-Bit/32-Bit Single Edge mode: Drives output high on compare match
0000 = 16-Bit/32-Bit Timer mode: Output functions are disabled

- Note 1:** This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.
4: Refer to [Figure 8-2](#) for REFO connection.
5: Not available on SCCP modules.

PIC32MM0064GPL036 FAMILY

REGISTER 12-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------------|----------------------|----------------------|----------------------|----------------------|---------------|
| 31:24 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
| | OENSYNC | — | OCFEN ⁽¹⁾ | OCEEN ⁽¹⁾ | OCDEN ⁽¹⁾ | OCCEN ⁽¹⁾ | OCBEN ⁽¹⁾ | OCAEN |
| 23:16 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ICGSM<1:0> | | — | AUXOUT<1:0> | | ICS<2:0> | | |
| 15:8 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | PWMRSEN | ASDGM | — | SSDG | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ASDG<7:0> | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **OENSYNC:** Output Enable Synchronization bit
 1 = Update by output enable bits occurs on the next Time Base Reset or rollover
 0 = Update by output enable bits occurs immediately
- bit 30 **Unimplemented:** Read as '0'
- bit 29-24 **OC<F:A>EN:** Output Enable/Steering Control bits⁽¹⁾
 1 = OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
 0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin
- bit 23-22 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits
 11 = Reserved
 10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
 01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
 00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events
- bit 21 **Unimplemented:** Read as '0'
- bit 20-19 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits
 11 = Input capture or output compare event; no signal in Timer mode
 10 = Signal output depends on module operating mode
 01 = Time base rollover event (all modes)
 00 = Disabled
- bit 18-16 **ICS<2:0>:** Input Capture Source Select bits
 111 = Reserved
 110 = Reserved
 101 = CLC2 output
 100 = CLC1 output
 011 = Reserved
 010 = Comparator 2 output
 001 = Comparator 1 output
 000 = ICMx pin (remappable)
- bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
 1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
 0 = ASEVT must be cleared in software to resume PWM activity on output pins

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.

PIC32MM0064GPL036 FAMILY

REGISTER 12-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER (CONTINUED)

- bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
1 = Waits until the next Time Base Reset or rollover for shutdown to occur
0 = Shutdown event occurs immediately
- bit 13 **Unimplemented:** Read as '0'
- bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting the ASDGM bit still applies)
0 = Normal module operation
- bit 11-8 **Unimplemented:** Read as '0'
- bit 7-0 **ASDG<7:0>:** CCPx Auto-Shutdown/Gating Source Enable bits
1xxx xxxx = Auto-shutdown is controlled by the OCFB pin (remappable)
x1xx xxxx = Auto-shutdown is controlled by the OCFA pin (remappable)
xx1x xxxx = Auto-shutdown is controlled by CLC1 for MCCP1/SCCP2 and by CLC2 for SCCP3
xxx1 xxxx = Auto-shutdown is controlled by the SCCP2 output for MCCP1 and by MCCP1 for SCCP2/SCCP3
xxxx 1xxx = Auto-shutdown is controlled by the SCCP3 output for MCCP1/SCCP2 and by SCCP2 for SCCP3
xxxx x1xx = Reserved
xxxx xx1x = Auto-shutdown is controlled by Comparator 2
xxxx xxx1 = Auto-shutdown is controlled by Comparator 1

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.

PIC32MM0064GPL036 FAMILY

REGISTER 12-3: CCPxCON3: CAPTURE/COMPARE/PWMx CONTROL 3 REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|-------------------|-------------------|------------------------|-----------------------|-------------------|--------------------------|----------------------------|------------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | OETRIG | OSCNT<2:0> | | | — | OUTM<2:0> ⁽¹⁾ | | |
| 23:16 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | POLACE | POLBDF ⁽¹⁾ | PSSACE<1:0> | | PSSBDF<1:0> ⁽¹⁾ | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | DT<5:0> ⁽¹⁾ | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **OETRIG:** PWM Dead-Time Select bit
 1 = For Triggered mode (TRIGEN = 1), the module does not drive enabled output pins until triggered
 0 = Normal output pin operation
- bit 30-28 **OSCNT<2:0>:** One-Shot Event Count bits
 Extends the duration of a one-shot trigger event by an additional n clock cycles (n+1 total cycles).
 111 = 7 timer count periods (8 cycles total)
 110 = 6 timer count periods (7 cycles total)
 101 = 5 timer count periods (6 cycles total)
 100 = 4 timer count periods (5 cycles total)
 011 = 3 timer count periods (4 cycles total)
 010 = 2 timer count periods (3 cycles total)
 001 = 1 timer count period (2 cycles total)
 000 = Does not extend the one-shot trigger event (the event takes 1 timer count period)
- bit 27 **Unimplemented:** Read as '0'
- bit 26-24 **OUTM<2:0>:** PWMx Output Mode Control bits⁽¹⁾
 111 = Reserved
 110 = Output Scan mode
 101 = Brush DC Output mode, forward
 100 = Brush DC Output mode, reverse
 011 = Reserved
 010 = Half-Bridge Output mode
 001 = Push-Pull Output mode
 000 = Steerable Single Output mode
- bit 23-22 **Unimplemented:** Read as '0'
- bit 21 **POLACE:** CCPx Output Pins, OCxA, OCxC and OCxE, Polarity Control bit
 1 = Output pin polarity is active-low
 0 = Output pin polarity is active-high
- bit 20 **POLBDF:** CCPx Output Pins, OCxB, OCxD and OCxF, Polarity Control bit⁽¹⁾
 1 = Output pin polarity is active-low
 0 = Output pin polarity is active-high
- bit 19-18 **PSSACE<1:0>:** PWMx Output Pins, OCxA, OCxC and OCxE, Shutdown State Control bits
 11 = Pins are driven active when a shutdown event occurs
 10 = Pins are driven inactive when a shutdown event occurs
 0x = Pins are in a high-impedance state when a shutdown event occurs

Note 1: These bits are implemented in MCCP modules only.

PIC32MM0064GPL036 FAMILY

REGISTER 12-3: CCPxCON3: CAPTURE/COMPARE/PWMx CONTROL 3 REGISTER (CONTINUED)

bit 17-16 **PSSBDF<1:0>**: PWMx Output Pins, OCxB, OCxD and OCxF, Shutdown State Control bits⁽¹⁾

11 = Pins are driven active when a shutdown event occurs

10 = Pins are driven inactive when a shutdown event occurs

0x = Pins are in a high-impedance state when a shutdown event occurs

bit 15-6 **Unimplemented**: Read as '0'

bit 5-0 **DT<5:0>**: PWM Dead-Time Select bits⁽¹⁾

111111 = Inserts 63 dead-time delay periods between complementary output signals

111110 = Inserts 62 dead-time delay periods between complementary output signals

...

000010 = Inserts 2 dead-time delay periods between complementary output signals

000001 = Inserts 1 dead-time delay period between complementary output signals

000000 = Dead-time logic is disabled

Note 1: These bits are implemented in MCCP modules only.

PIC32MM0064GPL036 FAMILY

REGISTER 12-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|-------------------|-------------------|-------------------|-------------------|-------------------|-----------------------|------------------|------------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | PRLWIP | TMRHWIP | TMRLWIP | RBWIP | RAWIP |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R/C-0 | U-0 | U-0 |
| | — | — | — | — | — | ICGARM ⁽¹⁾ | — | — |
| 7:0 | R-0 | W1-0 | W1-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE |

| | |
|-------------------|------------------------------------|
| Legend: | C = Clearable bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

- bit 31-21 **Unimplemented:** Read as '0'
- bit 20 **PRLWIP:** CCPxPRL Write in Progress Status bit
 - 1 = An update to the CCPxPRL register with the buffered contents is in progress
 - 0 = An update to the CCPxPRL register is not in progress
- bit 19 **TMRHWIP:** CCPxTMRH Write in Progress Status bit
 - 1 = An update to the CCPxTMRH register with the buffered contents is in progress
 - 0 = An update to the CCPxTMRH register is not in progress
- bit 18 **TMRLWIP:** CCPxTMRL Write in Progress Status bit
 - 1 = An update to the CCPxTMRL register with the buffered contents is in progress
 - 0 = An update to the CCPxTMRL register is not in progress
- bit 17 **RBWIP:** CCPxRB Write in Progress Status bit
 - 1 = An update to the CCPxRB register with the buffered contents is in progress
 - 0 = An update to the CCPxRB register is not in progress
- bit 16 **RAWIP:** CCPxRA Write in Progress Status bit
 - 1 = An update to the CCPxRA register with the buffered contents is in progress
 - 0 = An update to the CCPxRA register is not in progress
- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **ICGARM:** Input Capture Gate Arm bit⁽¹⁾

A write of '1' to this location will arm the input capture gating logic for a one-shot gate event when ICGSM<1:0> = 01 or 10. The bit location reads as '0'.
- bit 9-8 **Unimplemented:** Read as '0'
- bit 7 **CCPTRIG:** CCPx Trigger Status bit
 - 1 = Timer has been triggered and is running (set by hardware or writing to TRSET)
 - 0 = Timer has not been triggered and is held in Reset (cleared by writing to TRCLR)
- bit 6 **TRSET:** CCPx Trigger Set Request bit

Write '1' to this location to trigger the timer when TRIGEN = 1 (location always reads '0').
- bit 5 **TRCLR:** CCPx Trigger Clear Request bit

Write '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads '0').
- bit 4 **ASEVT:** CCPx Auto-Shutdown Event Status/Control bit
 - 1 = A shutdown event is in progress; CCPx outputs are in the shutdown state
 - 0 = CCPx outputs operate normally

Note 1: This is not a physical bit location and will always read as '0'. A write of '1' will initiate the hardware event.

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REGISTER 12-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER (CONTINUED)

- bit 3 **SCEVT**: Single Edge Compare Event Status bit
1 = A single edge compare event has occurred
0 = A single edge compare event has not occurred
- bit 2 **ICDIS**: Input Capture Disable bit
1 = Event on input capture pin does not generate a capture event
0 = Event on input capture pin will generate a capture event
- bit 1 **ICOV**: Input Capture Buffer Overflow Status bit
1 = The input capture FIFO buffer has overflowed
0 = The input capture FIFO buffer has not overflowed
- bit 0 **ICBNE**: Input Capture Buffer Status bit
1 = The input capture buffer has data available
0 = The input capture buffer is empty

Note 1: This is not a physical bit location and will always read as '0'. A write of '1' will initiate the hardware event.

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NOTES:

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13.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I²S)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. “Serial Peripheral Interface (SPI)”** (DS61106) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The SPI/I²S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well

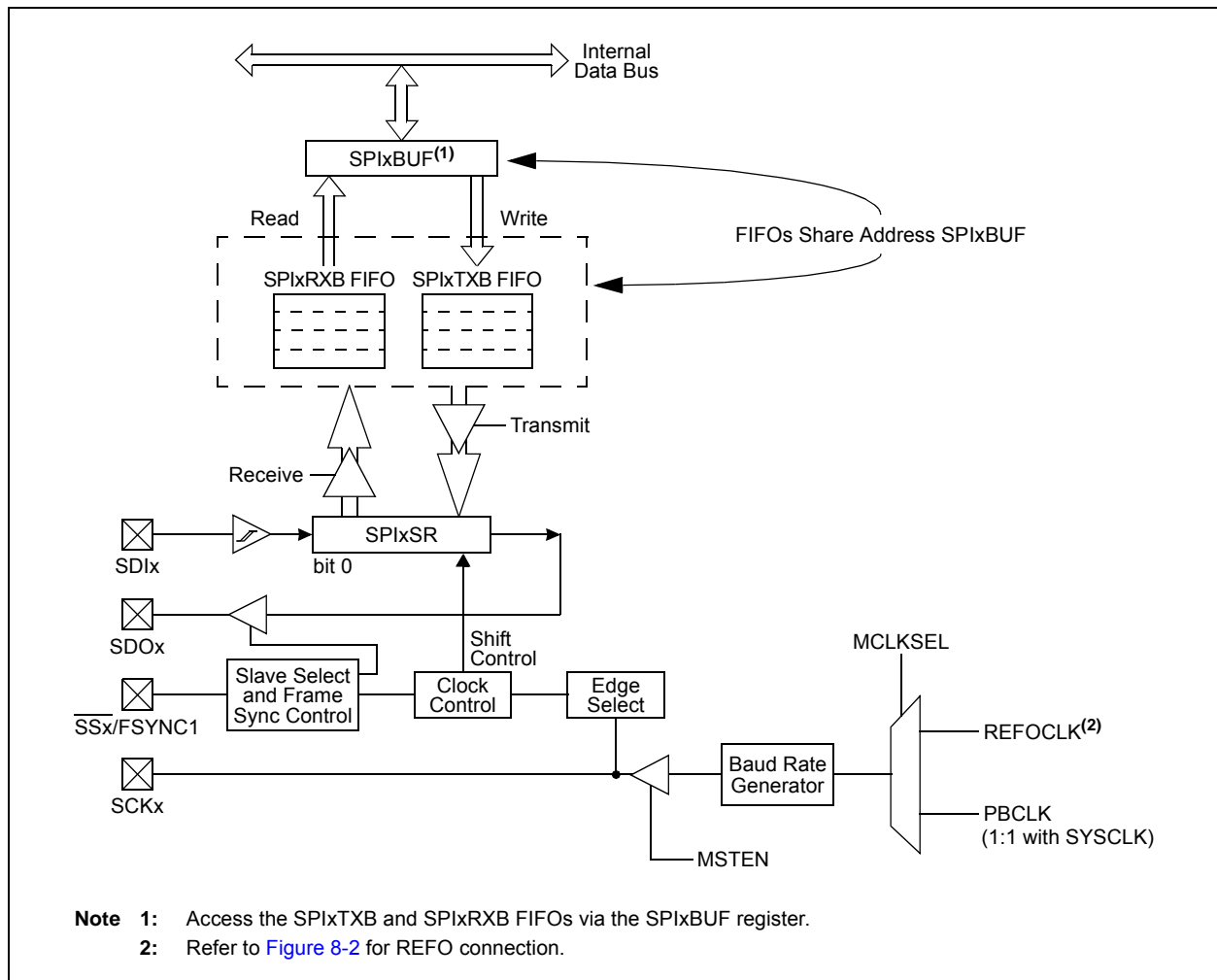
as digital audio devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters (ADC), etc.

The SPI/I²S module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes Support
- Four Different Clock Formats
- Enhanced Framed SPI Protocol Support
- User-Configurable 8-Bit, 16-Bit and 32-Bit Data Width
- Separate SPI FIFO Buffers for Receive and Transmit:
 - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable Interrupt Event on Every 8-Bit, 16-Bit and 32-Bit Data Transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
 - I²S protocol

FIGURE 13-1: SPI/I²S MODULE BLOCK DIAGRAM



13.1 SPI Control Registers

TABLE 13-1: SPI1 AND SPI2 REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | All Resets | | |
|-----------------------------|---------------------------------|-----------|------------|---------|--------|---------------|----------|-------------|--------|--------|---------|--------|---------------|--------|--------------|--------------|-------------|--------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | | 17/1 | 16/0 |
| 8080 | SPI1CON | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSEN | FRMSYPW | FRMCNT<2:0> | | | MCLKSEL | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | DISSDI | STXISEL<1:0> | SRXISEL<1:0> | — | — | 0000 |
| 8090 | SPI1STAT | 31:16 | — | — | — | RXBUFELM<4:0> | | | | — | — | — | TXBUFELM<4:0> | | | | 0000 | | |
| | | 15:0 | — | — | — | FRMERR | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 0008 |
| 80A0 | SPI1BUF | 31:16 | DATA<31:0> | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | DATA<31:0> | | | | | | | | | | | | | | 0000 | | |
| 80B0 | SPI1BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | BRG<12:0> | | | | | | | | | | | 0000 | | |
| 80C0 | SPI1CON2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SPIGNEXT | — | — | FRMERRREN | SPIROVEN | SPITUREN | IGNROV | IGNTUR | AUDEN | — | — | — | AUDMONO | — | AUDMOD<1:0> | — | — |
| 8100 | SPI2CON | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSEN | FRMSYPW | FRMCNT<2:0> | | | MCLKSEL | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | DISSDI | STXISEL<1:0> | SRXISEL<1:0> | — | — | 0000 |
| 8110 | SPI2STAT | 31:16 | — | — | — | RXBUFELM<4:0> | | | | — | — | — | TXBUFELM<4:0> | | | | 0000 | | |
| | | 15:0 | — | — | — | FRMERR | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 0008 |
| 8120 | SPI2BUF | 31:16 | DATA<31:0> | | | | | | | | | | | | | | 0000 | | |
| | | 15:0 | DATA<31:0> | | | | | | | | | | | | | | 0000 | | |
| 8130 | SPI2BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | BRG<12:0> | | | | | | | | | | | 0000 | | |
| 8140 | SPI2CON2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SPIGNEXT | — | — | FRMERRREN | SPIROVEN | SPITUREN | IGNROV | IGNTUR | AUDEN | — | — | — | AUDMONO | — | AUDMOD<1:0> | — | — |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table, except SPIxBUF, have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|------------------------|--------------------|----------------|-----------------------|----------------|----------------|---------------|-----------------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMEN | FRMSYNC | FRMPOL | MSEN | FRMSYPW | FRMCNT<2:0> | | |
| 23:16 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | MCLKSEL ⁽¹⁾ | — | — | — | — | — | SPIFE | ENHBUF ⁽¹⁾ |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON | — | SIDL | DISSDO ⁽⁴⁾ | MODE32 | MODE16 | SMP | CKE ⁽²⁾ |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SSEN | CKP ⁽³⁾ | MSTEN | DISSDI ⁽⁴⁾ | STXISEL<1:0> | | SRXISEL<1:0> | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **FRMEN:** Framed SPI Support bit

- 1 = Framed SPI support is enabled (\overline{SSx} pin is used as the FSYNC1 input/output)
- 0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on \overline{SSx} Pin bit (Framed SPI mode only)

- 1 = Frame sync pulse input (Slave mode)
- 0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)

- 1 = Frame pulse is active-high
- 0 = Frame pulse is active-low

bit 28 **MSEN:** Master Mode Slave Select Enable bit

- 1 = Slave select SPI support is enabled; the \overline{SSx} pin is automatically driven during transmission in Master mode, polarity is determined by the FRMPOL bit
- 0 = Slave select SPI support is disabled

bit 27 **FRMSYPW:** Frame Sync Pulse-Width bit

- 1 = Frame sync pulse is one character wide
- 0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits

Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.

- 111 = Reserved
- 110 = Reserved
- 101 = Generates a frame sync pulse on every 32 data characters
- 100 = Generates a frame sync pulse on every 16 data characters
- 011 = Generates a frame sync pulse on every 8 data characters
- 010 = Generates a frame sync pulse on every 4 data characters
- 001 = Generates a frame sync pulse on every 2 data characters
- 000 = Generates a frame sync pulse on every data character

Note 1: These bits can only be written when the ON bit = 0. Refer to [Section 26.0 “Electrical Characteristics”](#) for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see [Section 9.8 “Peripheral Pin Select \(PPS\)”](#) for more information).

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REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

- bit 23 **MCLKSEL**: Master Clock Enable bit⁽¹⁾
1 = REFCLKO is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator (1:1 with SYSCLK)
- bit 22-18 **Unimplemented**: Read as '0'
- bit 17 **SPIFE**: SPIx Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock
- bit 16 **ENHBUF**: Enhanced Buffer Enable bit⁽¹⁾
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled
- bit 15 **ON**: SPIx Module On bit
1 = SPIx module is enabled
0 = SPIx module is disabled
- bit 14 **Unimplemented**: Read as '0'
- bit 13 **SIDL**: SPIx Stop in Idle Mode bit
1 = Discontinues operation when CPU enters Idle mode
0 = Continues operation in Idle mode
- bit 12 **DISSDO**: Disable SDOx Pin bit⁽⁴⁾
1 = SDOx pin is not used by the module; the pin is controlled by the associated PORTx register
0 = SDOx pin is controlled by the module
- bit 11-10 **MODE<32,16>**: 32/16/8-Bit Communication Select bits
- When AUDEN = 1:
- | MODE32 | MODE16 | Communication |
|--------|--------|---|
| 1 | 1 | 24-bit data, 32-bit FIFO, 32-bit channel/64-bit frame |
| 1 | 0 | 32-bit data, 32-bit FIFO, 32-bit channel/64-bit frame |
| 0 | 1 | 16-bit data, 16-bit FIFO, 32-bit channel/64-bit frame |
| 0 | 0 | 16-bit data, 16-bit FIFO, 16-bit channel/32-bit frame |
- When AUDEN = 0:
- | MODE32 | MODE16 | Communication |
|--------|--------|---------------|
| 1 | x | 32-bit |
| 0 | 1 | 16-bit |
| 0 | 0 | 8-bit |
- bit 9 **SMP**: SPIx Data Input Sample Phase bit
- Master mode (MSTEN = 1):
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
- Slave mode (MSTEN = 0):
SMP value is ignored when SPIx is used in Slave mode. The module always uses SMP = 0.
- bit 8 **CKE**: SPIx Clock Edge Select bit⁽²⁾
1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)
- Note 1:** These bits can only be written when the ON bit = 0. Refer to [Section 26.0 “Electrical Characteristics”](#) for maximum clock frequency requirements.
- Note 2:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- Note 3:** When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.
- Note 4:** These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see [Section 9.8 “Peripheral Pin Select \(PPS\)”](#) for more information).

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REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

- bit 7 **SSEN**: Slave Select Enable (Slave mode) bit
1 = \overline{SSx} pin is used for Slave mode
0 = \overline{SSx} pin is not used for Slave mode, pin is controlled by port function
- bit 6 **CKP**: Clock Polarity Select bit⁽³⁾
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level
- bit 5 **MSTEN**: Master Mode Enable bit
1 = Master mode
0 = Slave mode
- bit 4 **DISSDI**: Disable SDIx bit⁽⁴⁾
1 = SDIx pin is not used by the SPIx module (pin is controlled by port function)
0 = SDIx pin is controlled by the SPIx module
- bit 3-2 **STXISEL<1:0>**: SPIx Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPIxSR and transmit operations are complete
- bit 1-0 **SRXISEL<1:0>**: SPIx Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

- Note 1:** These bits can only be written when the ON bit = 0. Refer to [Section 26.0 “Electrical Characteristics”](#) for maximum clock frequency requirements.
- 2:** This bit is not used in the Framed SPI mode. The user should program this bit to ‘0’ for the Framed SPI mode (FRMEN = 1).
- 3:** When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to ‘1’, regardless of the actual value of the CKP bit.
- 4:** These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see [Section 9.8 “Peripheral Pin Select \(PPS\)”](#) for more information).

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REGISTER 13-2: SPIxCON2: SPIx CONTROL REGISTER 2

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------------|----------------|----------------|----------------|--------------------------|----------------|------------------------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SPISGNEXT | — | — | FRMERREN | SPIROVEN | SPITUREN | IGNROV | IGNTUR |
| 7:0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | AUDEN ⁽¹⁾ | — | — | — | AUDMONO ^(1,2) | — | AUDMOD<1:0> ^(1,2) | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** SPIx Sign-Extend Read Data from the RX FIFO bit
 1 = Data from RX FIFO is sign-extended
 0 = Data from RX FIFO is not sign-extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
 1 = Frame error overflow generates error events
 0 = Frame error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
 1 = Receive Overflow (ROV) generates error events
 0 = Receive Overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
 1 = Transmit Underrun (TUR) generates error events
 0 = Transmit Underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow (ROV) bit (for audio data transmissions)
 1 = A ROV is not a critical error; during ROV, data in the FIFO is not overwritten by receive data
 0 = A ROV is a critical error which stops SPIx operation

bit 8 **IGNTUR:** Ignore Transmit Underrun (TUR) bit (for audio data transmissions)
 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
 0 = A TUR is a critical error which stops SPIx operation

bit 7 **AUDEN:** Enable Audio Codec Support bit⁽¹⁾
 1 = Audio protocol is enabled
 0 = Audio protocol is disabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit^(1,2)
 1 = Audio data is mono (each data word is transmitted on both left and right channels)
 0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bits^(1,2)
 11 = PCM/DSP mode
 10 = Right Justified mode
 01 = Left Justified mode
 00 = I²S mode

Note 1: These bits can only be written when the ON bit = 0.
Note 2: These bits are only valid for AUDEN = 1.

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REGISTER 13-3: SPIxSTAT: SPIx STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | RXBUFELM<4:0> | | | | |
| 23:16 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | TXBUFELM<4:0> | | | | |
| 15:8 | U-0 | U-0 | U-0 | R/C-0, HS | R-0 | U-0 | U-0 | R-0 |
| | — | — | — | FRMERR | SPIBUSY | — | — | SPITUR |
| 7:0 | R-0 | R/W-0 | R-0 | U-0 | R-1 | U-0 | R-0 | R-0 |
| | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF |

| | | |
|-------------------|-------------------|--|
| Legend: | C = Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 31-29 **Unimplemented:** Read as '0'
- bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 23-21 **Unimplemented:** Read as '0'
- bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **FRMERR:** SPIx Frame Error status bit
 - 1 = Frame error is detected
 - 0 = No frame error is detected
 - This bit is only valid when FRMEN = 1.
- bit 11 **SPIBUSY:** SPIx Activity Status bit
 - 1 = SPIx peripheral is currently busy with some transactions
 - 0 = SPIx peripheral is currently Idle
- bit 10-9 **Unimplemented:** Read as '0'
- bit 8 **SPITUR:** SPIx Transmit Underrun (TUR) bit
 - 1 = Transmit buffer has encountered an underrun condition
 - 0 = Transmit buffer has no underrun condition
 - This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.
- bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
 - 1 = When the SPIx Shift register is empty
 - 0 = When the SPIx Shift register is not empty
- bit 6 **SPIROV:** SPIx Receive Overflow (ROV) Flag bit
 - 1 = New data is completely received and discarded; the user software has not read the previous data in the SPIxBUF register
 - 0 = No overflow has occurred
 - This bit is set in hardware; it can only be cleared (= 0) in software.
- bit 5 **SPIRBE:** SPIx RX FIFO Empty bit (valid only when ENHBUF = 1)
 - 1 = RX FIFO is empty (CPU Read Pointer (CRPTR) = SPI Write Pointer (SWPTR))
 - 0 = RX FIFO is not empty (CRPTR ≠ SWPTR)
- bit 4 **Unimplemented:** Read as '0'

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REGISTER 13-3: SPIxSTAT: SPIx STATUS REGISTER (CONTINUED)

- bit 3 **SPITBE:** SPIx Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB, is empty
0 = Transmit buffer, SPIxTXB, is not empty
Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit buffer is not full
Standard Buffer mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.
Enhanced Buffer mode:
Set when the CPU Write Pointer (CWPTR) + 1 = SPI Read Pointer (SRPTR); cleared otherwise.
- bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB, is full
0 = Receive buffer, SPIxRXB, is not full
Standard Buffer mode:
Automatically set in hardware when the SPIx module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise.

14.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. “UART”** (DS60001107) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

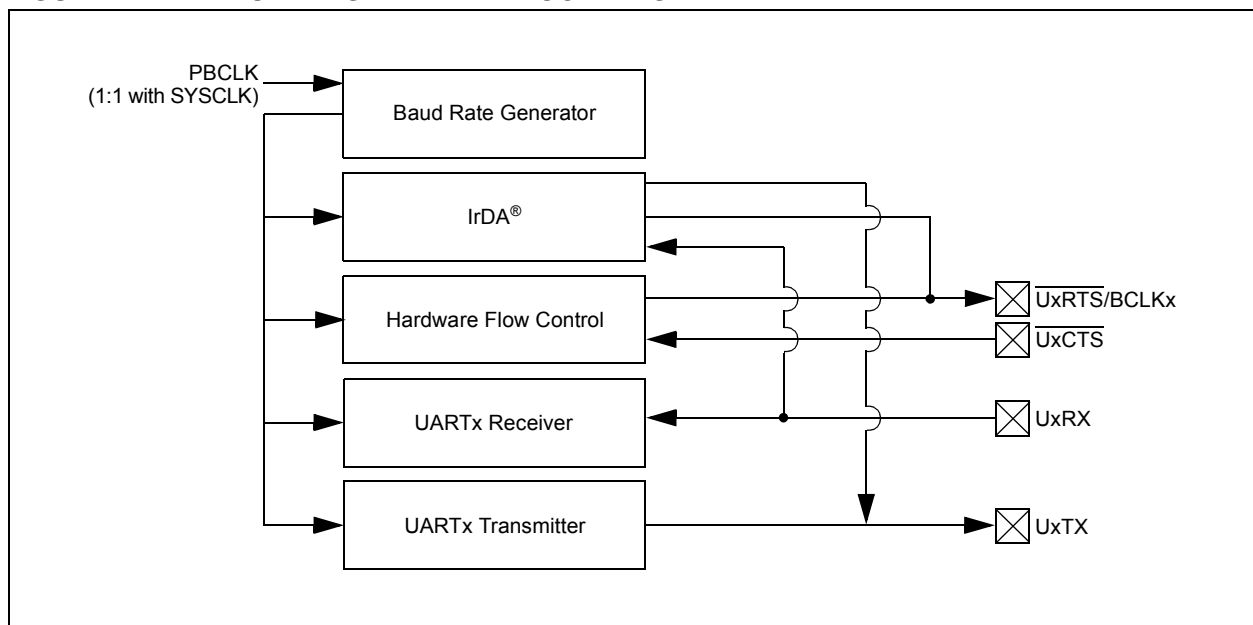
The UART module is one of the serial I/O modules available in the PIC32MM0064GPL036 family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN/J2602 and IrDA®. The module also supports the hardware flow control option with the \overline{UxCTS} and \overline{UxRTS} pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8-Bit or 9-Bit Data Transmission
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop Bits
- Hardware Auto-Baud Feature
- Hardware Flow Control Option
- Fully Integrated Baud Rate Generator (BRG) with 16-Bit Prescaler
- Baud Rates Ranging from 47.7 bps to 6.26 Mbps at 25 MHz
- 8-Level Deep First-In-First-Out (FIFO) Transmit Data Buffer
- 8-Level Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for Interrupt Only on Address Detect (9th bit = 1)
- Separate Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- LIN/J2602 Protocol Support
- IrDA Encoder and Decoder with 16x Baud Clock Output for External IrDA Encoder/Decoder Support
- Supports Separate UART Baud Clock Input
- Ability to Continue to Run when a Receive Overflow (ROV) Condition Exists
- Ability to Run and Receive Data during Sleep mode

Figure 14-1 illustrates a simplified block diagram of the UART module.

FIGURE 14-1: UARTx SIMPLIFIED BLOCK DIAGRAM



14.1 UART Control Registers

TABLE 14-1: UART1 AND UART2 REGISTER MAP

| Virtual Address (BF80.#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets | | |
|-----------------------------|-----------------------|-----------|-------------------------------|-------|--------|-------|--------|-------|-------|----------|------|-------------------------|--------|-------|------|------|-------------|------------|-------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | | 16/0 | |
| 0600 | U1MODE ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | SLPEN | ACTIVE | — | — | — | CLKSEL<1:0> | OVFDIS | 0000 | |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | — | UEN<1:0> | WAKE | LPBACK | ABAUD | RXINV | BRGH | — | — | PDSEL<1:0> | STSEL | 0000 |
| 0610 | U1STA ⁽¹⁾ | 31:16 | UART1 MASK<7:0> | | | | | | | | | UART1 ADDR<7:0> | | | | | | | 0000 | |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | — | — | — | — | — | — | — | — | — | — |
| 0620 | U1TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | TX8 | UART1 Transmit Register | | | | | | | 0000 | |
| 0630 | U1RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 0640 | U1BRG ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | 0000 | | |
| 0680 | U2MODE ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | SLPEN | ACTIVE | — | — | — | CLKSEL<1:0> | OVFDIS | 0000 | |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | — | UEN<1:0> | WAKE | LPBACK | ABAUD | RXINV | BRGH | — | — | PDSEL<1:0> | STSEL | 0000 |
| 0690 | U2STA ⁽¹⁾ | 31:16 | UART2 MASK<7:0> | | | | | | | | | UART2 ADDR<7:0> | | | | | | | 0000 | |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | — | — | — | — | — | — | — | — | — | — |
| 06A0 | U2TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | TX8 | UART2 Transmit Register | | | | | | | 0000 | |
| 06B0 | U2RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 06C0 | U2BRG ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | 0000 | | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

PIC32MM0064GPL036 FAMILY

REGISTER 14-1: UxMODE: UARTx MODE REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|-------------------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | SLPEN | ACTIVE | — | — | — | CLKSEL<1:0> | | OVDIS |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> ⁽²⁾ | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **SLPEN:** Run During Sleep Enable bit
 1 = UARTx clock runs during Sleep
 0 = UARTx clock is turned off during Sleep

bit 22 **ACTIVE:** UARTx Running Status bit
 1 = UARTx is active (UxMODE register shouldn't be updated)
 0 = UARTx is not active (UxMODE register can be updated)

bit 21-19 **Unimplemented:** Read as '0'

bit 18-17 **CLKSEL<1:0>:** UARTx Clock Selection bits⁽¹⁾
 11 = The UARTx clock is the Reference Clock Output (REFCLKO)
 10 = The UARTx clock is the FRC oscillator clock
 01 = The UARTx clock is the SYSCLK
 00 = The UARTx clock is the PBCLK (1:1 with SYSCLK)

bit 16 **OVDIS:** Run During Overflow Condition Mode bit
 1 = When an Overflow Error (OERR) condition is detected, the Shift register continues to run to remain synchronized
 0 = When an Overflow Error (OERR) condition is detected, the Shift register stops accepting new data (Legacy mode)

bit 15 **ON:** UARTx Enable bit
 1 = UARTx is enabled; UARTx pins are controlled by UARTx, as defined by the UEN<1:0> and UTXEN control bits
 0 = UARTx is disabled; all UARTx pins are controlled by the corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** UARTx Stop in Idle Mode bit
 1 = Discontinues operation when device enters Idle mode
 0 = Continues operation in Idle mode

bit 12 **IREN:** IrDA[®] Encoder and Decoder Enable bit
 1 = IrDA is enabled
 0 = IrDA is disabled

Note 1: Refer to [Figure 8-2](#) for REFO connection.

2: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see [Section 9.8 "Peripheral Pin Select \(PPS\)"](#) for more information).

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REGISTER 14-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UARTx Enable bits⁽²⁾
11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS/UxBCLK}}$ pins are controlled by corresponding bits in the PORTx register
- bit 7 **WAKE:** Enable Wake-up on Start Bit Detect During Sleep Mode bit
1 = Wake-up is enabled
0 = Wake-up is disabled
- bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Loopback mode is enabled
0 = Loopback mode is disabled
- bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement is disabled or has completed
- bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'
- bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock is enabled
0 = Standard Speed mode – 16x baud clock is enabled
- bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity
- bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

- Note 1:** Refer to [Figure 8-2](#) for REFO connection.
- 2:** These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see [Section 9.8 “Peripheral Pin Select \(PPS\)”](#) for more information).

PIC32MM0064GPL036 FAMILY

REGISTER 14-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MASK<7:0> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADDR<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-1 |
| | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/W-0 | R-0 |
| | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **MASK<7:0>**: UARTx Address Match Mask bits

Used to mask the ADDR<7:0> bits.

For MASK<x>:

1 = ADDR<x> is used to detect the address match

0 = ADDR<x> is not used to detect the address match

bit 23-16 **ADDR<7:0>**: UARTx Automatic Address Mask bits

When the ADDEN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>**: UARTx TX Interrupt Mode Selection bits

11 = Reserved, do not use

10 = Interrupt is generated and asserted while the transmit buffer is empty

01 = Interrupt is generated and asserted when all characters have been transmitted

00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV**: UARTx Transmit Polarity Inversion bit

If IrDA mode is Disabled (i.e., IREN (UxMODE<12>) is '0'):

1 = UxTX Idle state is '0'

0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):

1 = IrDA[®] encoded UxTX Idle state is '1'

0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN**: UARTx Receiver Enable bit

1 = UARTx receiver is enabled, UxRX pin is controlled by UARTx (if ON = 1)

0 = UARTx receiver is disabled, UxRX pin is ignored by the UARTx module

bit 11 **UTXBRK**: UARTx Transmit Break bit

1 = Sends Break on next transmission; Start bit, followed by twelve '0' bits, followed by Stop bit, cleared by hardware upon completion

0 = Break transmission is disabled or has completed

bit 10 **UTXEN**: UARTx Transmit Enable bit

1 = UARTx transmitter is enabled, UxTX pin is controlled by UARTx (if ON = 1)

0 = UARTx transmitter is disabled, any pending transmission is aborted and the buffer is reset

bit 9 **UTXBF**: UARTx Transmit Buffer Full Status bit (read-only)

1 = Transmit buffer is full

0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT**: Transmit Shift Register (TSR) is Empty bit (read-only)

1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)

0 = Transmit Shift Register is not empty, a transmission is in progress or queued in the transmit buffer

PIC32MM0064GPL036 FAMILY

REGISTER 14-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 7-6 **URXISEL<1:0>**: UARTx Receive Interrupt Mode Selection bits
- 11 = Reserved
 - 10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
 - 01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
 - 00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)
- bit 5 **ADDEN**: Address Character Detect bit (bit 8 of received data = 1)
- 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this control bit has no effect
 - 0 = Address Detect mode is disabled
- bit 4 **RIDLE**: Receiver Idle bit (read-only)
- 1 = Receiver is Idle
 - 0 = Data is being received
- bit 3 **PERR**: Parity Error Status bit (read-only)
- 1 = Parity error has been detected for the current character
 - 0 = Parity error has not been detected
- bit 2 **FERR**: Framing Error Status bit (read-only)
- 1 = Framing error has been detected for the current character
 - 0 = Framing error has not been detected
- bit 1 **OERR**: Receive Buffer Overrun Error Status bit
- This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to the empty state.
- 1 = Receive buffer has overflowed
 - 0 = Receive buffer has not overflowed
- bit 0 **URXDA**: UARTx Receive Buffer Data Available bit (read-only)
- 1 = Receive buffer has data, at least one more character can be read
 - 0 = Receive buffer is empty

15.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

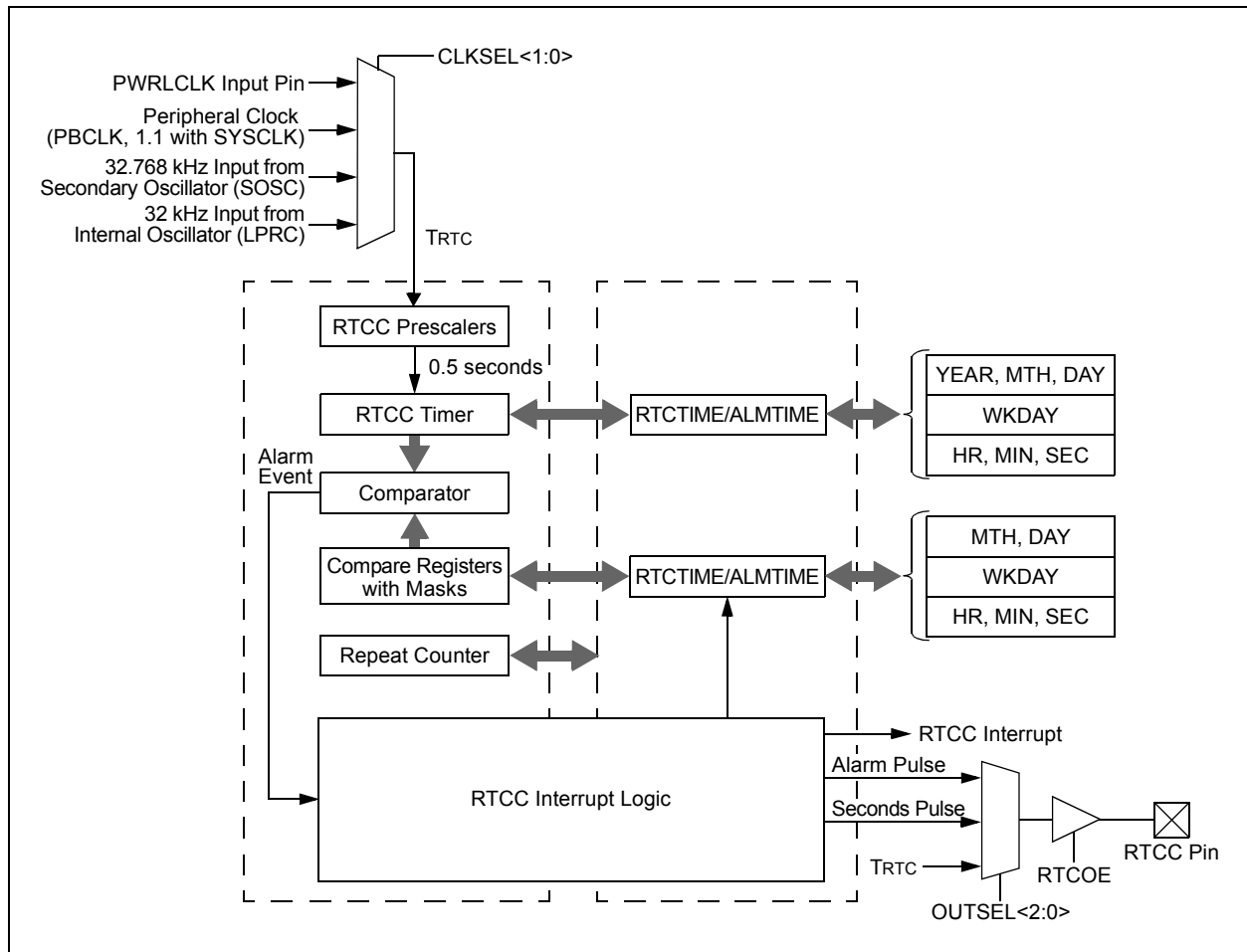
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 28. “RTCC with Timestamp”** (DS60001362) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

Key features of the RTCC module are:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (military time)
- Visibility of One-Half Second Period
- Provides Calendar: Weekday, Date, Month and Year
- Alarm Intervals are Configurable for Half of a second, One Second, 10 Seconds, One Minute, 10 Minutes, One Hour, One Day, One Week, One Month and One Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat: Chime
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Smaller Firmware Overhead
- Optimized for Long-Term Battery Operation
- Fractional Second Synchronization
- User Calibration of the Clock Crystal Frequency with Auto-Adjust
- Uses External 32.768 kHz Crystal, 32 kHz Internal Oscillator, PWRLCLK Input Pin or Peripheral Clock
- Alarm Pulse, Seconds Clock or Internal Clock Output on RTCC Pin

FIGURE 15-1: RTCC BLOCK DIAGRAM



15.1 RTCC Control Registers

TABLE 15-1: RTCC REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|-------------|------------|-------------|-------|-------------|-------|------|------|-------------|-------------|--------|-------------|-----------|------|------------|-------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | | 17/1 |
| 0000 | RTCCON1 | 31:16 | ALRMEN | CHIME | — | — | AMASK<3:0> | | | | ALMRPT<7:0> | | | | | | 0000 | |
| | | 15:0 | ON | — | — | — | WRLOCK | — | — | — | RTCOE | OUTSEL<2:0> | | | — | — | — | 0000 |
| 0010 | RTCCON2 | 31:16 | DIV<15:0> | | | | | | | | | | | | | | 0000 | |
| | | 15:0 | FDIV<4:0> | | | | — | — | — | — | — | — | — | — | — | — | — | CLKSEL<1:0> |
| 0030 | RTCSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | ALMEVT | — | — | SYNC | ALMSYNC | HALFSEC |
| 0040 | RTCTIME | 31:16 | — | HRTEN<2:0> | | | HRONE<3:0> | | | — | MINTEN<2:0> | | | MINONE<3:0> | | | xxxx | |
| | | 15:0 | SECTEN<3:0> | | | | SECONE<3:0> | | | — | — | — | — | — | — | — | — | xx00 |
| 0050 | RTCDATE | 31:16 | YRTEN<3:0> | | | | YRONE<3:0> | | | — | — | — | MHTEN | MTHONE<3:0> | | | 0000 | |
| | | 15:0 | — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | — | — | — | — | — | WDAY<2:0> | | 0000 | |
| 0060 | ALMTIME | 31:16 | — | HRTEN<2:0> | | | HRONE<3:0> | | | — | MINTEN<2:0> | | | MINONE<3:0> | | | xxxx | |
| | | 15:0 | SECTEN<3:0> | | | | SECONE<3:0> | | | — | — | — | — | — | — | — | — | xx00 |
| 0070 | ALMDATE | 31:16 | — | — | — | — | — | — | — | — | — | — | MHTEN | MTHONE<3:0> | | | 0000 | |
| | | 15:0 | — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | — | — | — | — | — | WDAY<2:0> | | 0000 | |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 15-1: RTCCON1: RTCC CONTROL 1 REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------------------|----------------|----------------|----------------|-----------------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ALRMEN | CHIME | — | — | AMASK<3:0> | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ALMRPT<7:0> ⁽¹⁾ | | | | | | | |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 |
| | ON | — | — | — | WRLOCK ⁽²⁾ | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | RTCOE | OUTSEL<2:0> | | | — | — | — | — |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **ALRMEN:** Alarm Enable bit

1 = Alarm is enabled
0 = Alarm is disabled

bit 30 **CHIME:** Chime Enable bit

1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from '00' to 'FF'
0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach '00'

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **AMASK<3:0>:** Alarm Mask Configuration bits

11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half second

bit 23-16 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits⁽¹⁾

11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
...
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

bit 15 **ON:** RTCC Enable bit

1 = RTCC is enabled and counts from selected clock source
0 = RTCC is disabled

bit 14-12 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

2: To clear this bit, an unlock sequence is required. Refer to [Section 23.4 "System Registers Write Protection"](#) for details.

PIC32MM0064GPL036 FAMILY

REGISTER 15-1: RTCCON1: RTCC CONTROL 1 REGISTER (CONTINUED)

- bit 11 **WRLOCK:** RTCC Registers Write Lock bit⁽²⁾
1 = Registers associated with accurate timekeeping are locked
0 = Registers associated with accurate timekeeping may be written to by user
- bit 10-8 **Unimplemented:** Read as '0'
- bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output is enabled; signal selected by OUTSEL<2:0> is presented on the RTCC pin
0 = RTCC clock output is disabled
- bit 6-4 **OUTSEL<2:0>:** RTCC Signal Output Selection bits
111 = Reserved
...
011 = Reserved
010 = RTCC input clock source (user-defined divided output based on the combination of the RTCCON2 bits, DIV<15:0> and PS<1:0>)
001 = Seconds clock
000 = Alarm event
- bit 3-0 **Unimplemented:** Read as '0'

- Note 1:** The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.
- 2:** To clear this bit, an unlock sequence is required. Refer to [Section 23.4 "System Registers Write Protection"](#) for details.

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REGISTER 15-2: RTCCON2: RTCC CONTROL 2 REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DIV<15:8> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DIV<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | FDIV<4:0> | | | | | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | CLKSEL<1:0> | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **DIV<15:0>**: Clock Divide bits

Sets the period of the clock divider counter; value should cause a nominal 1/2 second underflow.

bit 15-11 **FDIV<4:0>**: Fractional Clock Divide bits

11111 = Clock period increases by 31 RTCC input clock cycles every 16 seconds

11101 = Clock period increases by 30 RTCC input clock cycles every 16 seconds

...

00010 = Clock period increases by 2 RTCC input clock cycles every 16 seconds

00001 = Clock period increases by 1 RTCC input clock cycle every 16 seconds

00000 = No fractional clock division

bit 10-2 **Unimplemented**: Read as '0'

bit 1-0 **CLKSEL<1:0>**: Clock Select bits

11 = Peripheral clock (FCY)

10 = PWRLCLK input pin

01 = LPRC

00 = SOSOC

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REGISTER 15-3: RTCSTAT: RTCC STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R-0, HS, HC | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | — | — | ALMEVT | — | — | SYNC | ALMSYNC | HALFSEC |

| | | |
|-------------------|-----------------------------|--|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
 1 = An alarm event has occurred
 0 = An alarm event has not occurred

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **SYNC:** Synchronization Status bit
 1 = Time registers may change during software read
 0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization status bit
 1 = Alarm registers (ALMTIME and ALMDATE) and RTCCON1 should not be modified; the ALRMEN and ALMRPT<7:0> bits may change during software read
 0 = Alarm registers and Alarm Control registers may be modified safely

bit 0 **HALFSEC:** Half Second Status bit
 1 = Second half of 1-second period
 0 = First half of 1-second period

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REGISTER 15-4: RTCTIME/ALMTIME: RTCC/ALARM TIME REGISTERS

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | HRTEN<2:0> | | | HRONE<3:0> | | | |
| 23:16 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | MINTEN<2:0> | | | MINONE<3:0> | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | SECTEN<3:0> | | | SECONE<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **Unimplemented:** Read as '0'
- bit 30-28 **HRTEN<2:0>**: Binary Coded Decimal Value of Hours 10-Digit bits
Contains a value from 0 to 2.
- bit 27-24 **HRONE<3:0>**: Binary Coded Decimal Value of Hours 1-Digit bits
Contains a value from 0 to 9.
- bit 23 **Unimplemented:** Read as '0'
- bit 22-20 **MINTEN<2:0>**: Binary Coded Decimal Value of Minutes 10-Digit bits
Contains a value from 0 to 5.
- bit 19-16 **MINONE<3:0>**: Binary Coded Decimal Value of Minutes 1-Digit bits
Contains a value from 0 to 9.
- bit 15-12 **SECTEN<3:0>**: Binary Coded Decimal Value of Seconds 10-Digit bits
Contains a value from 0 to 5.
- bit 11-8 **SECONE<3:0>**: Binary Coded Decimal Value of Seconds 1-Digit bits
Contains a value from 0 to 9.
- bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 15-5: RTCDATE: RTCC DATE REGISTERS

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | YRTEN<3:0> | | | | YRONE<3:0> | | | |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MHTTEN | MTHONE<3:0> | | | |
| 15:8 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | WDAY<2:0> | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31-28 **YRTEN<3:0>**: Binary Coded Decimal Value of Years 10-Digit bits
- bit 27-24 **YRONE<3:0>**: Binary Coded Decimal Value of Years 1-Digit bits
- bit 23-21 **Unimplemented**: Read as '0'
- bit 20 **MHTTEN**: Binary Coded Decimal Value of Months 10-Digit bit
Contains a value from 0 to 1.
- bit 19-16 **MTHONE<3:0>**: Binary Coded Decimal Value of Months 1-Digit bits
Contains a value from 0 to 9.
- bit 15-14 **Unimplemented**: Read as '0'
- bit 13-12 **DAYTEN<1:0>**: Binary Coded Decimal Value of Days 10-Digit bits
Contains a value from 0 to 3.
- bit 11-8 **DAYONE<3:0>**: Binary Coded Decimal Value of Days 1-Digit bits
Contains a value from 0 to 9.
- bit 7-3 **Unimplemented**: Read as '0'
- bit 2-0 **WDAY<2:0>**: Binary Coded Decimal Value of Weekdays Digit bits
Contains a value from 0 to 6.

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REGISTER 15-6: ALMDATE: ALARM DATE REGISTERS

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MHTTEN | MTHONE<3:0> | | | |
| 15:8 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | WDAY<2:0> | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MHTTEN:** Binary Coded Decimal Value of Months 10-Digit bit

Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months 1-Digit bits

Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days 10-Digit bits

Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days 1-Digit bits

Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays Digit bits

Contains a value from 0 to 6.

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NOTES:

16.0 12-BIT ANALOG-TO-DIGITAL CONVERTER WITH THRESHOLD DETECT

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 25. “12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect”** (DS60001359) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold Amplifier (SHA)
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed-Length Configurable Conversion Result Buffer
- Eight Options for Result Alignment and Encoding
- Configurable Interrupt Generation
- Operation during CPU Sleep and Idle modes

Figure 16-1 illustrates a block diagram of the 12-bit ADC. The 12-bit ADC has 14 external analog inputs, AN0 through AN13, and 3 internal analog inputs connected to VDD, VSS and band gap. In addition, there are two analog input pins for external voltage reference connections.

16.1 Introduction

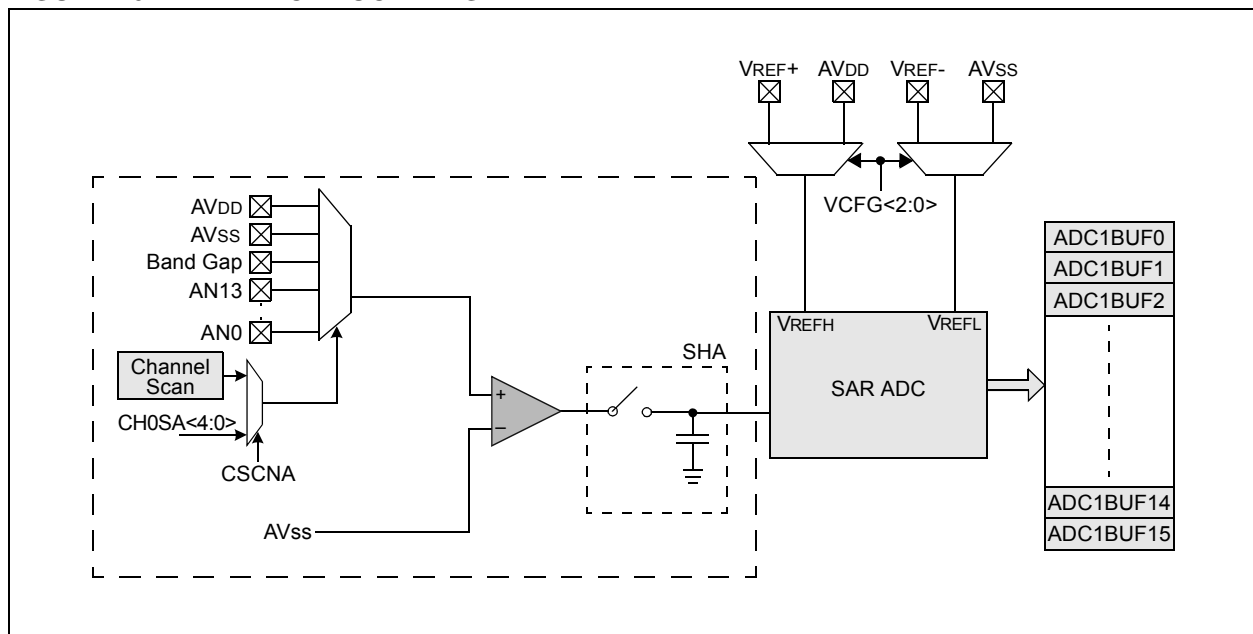
The 12-bit ADC Converter with Threshold Detect includes the following features:

- Successive Approximation Register (SAR) Conversion
- User-Selectable Resolution of 10 or 12 Bits
- Conversion Speeds of up to 222 ksps for 12-bit mode and 250 ksps for 10-bit mode
- Up to 17 Analog Inputs (internal and external)

The analog inputs are connected through a multiplexer to the SHA. Unipolar differential conversions are possible on all inputs (see Figure 16-1).

The Automatic Input Scan mode sequentially converts multiple analog inputs. A special control register specifies which inputs will be included in the scanning sequence. The 12-bit ADC is connected to a 16-word result buffer. The 12-bit result is converted to one of eight output formats in either 32-bit or 16-bit word widths.

FIGURE 16-1: ADC BLOCK DIAGRAM



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16.2 Control Registers

The ADC module has the following Special Function Registers (SFRs):

- [AD1CON1: ADC Control Register 1](#)
- [AD1CON2: ADC Control Register 2](#)
- [AD1CON3: ADC Control Register 3](#)
- [AD1CON5: ADC Control Register 5](#)

The AD1CON1, AD1CON2, AD1CON3 and AD1CON5 registers control the operation of the ADC module.

- [AD1CHS: ADC Input Select Register](#)

The AD1CHS register selects the input pins to be connected to the SHA.

- [AD1CSS: ADC Input Scan Select Register](#)

The AD1CSS register selects inputs to be sequentially scanned.

- [AD1CHIT: ADC Compare Hit Register](#)

The AD1CHIT register indicates the channels meeting specified comparison requirements.

[Table 16-1](#) provides a summary of all ADC module related registers, including their addresses and formats. Corresponding registers appear after the summary, followed by a detailed description of each register. All unimplemented registers and/or bits within a register read as zero.

TABLE 16-1: ADC REGISTER MAP

| Virtual Address (BF80_#) | Register Name(s) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|-----------------------------|---------------------|-----------|-----------------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | |
| 0700 | ADC1BUF0 | 31:16 | ADC1BUF0<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 0710 | ADC1BUF1 | 31:16 | ADC1BUF1<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 0720 | ADC1BUF2 | 31:16 | ADC1BUF2<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 0730 | ADC1BUF3 | 31:16 | ADC1BUF3<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 0740 | ADC1BUF4 | 31:16 | ADC1BUF4<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 0750 | ADC1BUF5 | 31:16 | ADC1BUF5<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 0760 | ADC1BUF6 | 31:16 | ADC1BUF6<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 0770 | ADC1BUF7 | 31:16 | ADC1BUF7<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 0780 | ADC1BUF8 | 31:16 | ADC1BUF8<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 0790 | ADC1BUF9 | 31:16 | ADC1BUF9<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 07A0 | ADC1BUF10 | 31:16 | ADC1BUF10<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 07B0 | ADC1BUF11 | 31:16 | ADC1BUF11<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 07C0 | ADC1BUF12 | 31:16 | ADC1BUF12<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |
| 07D0 | ADC1BUF13 | 31:16 | ADC1BUF13<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The CSS<13:11> and CHH<13:11> bits are not implemented in 20-pin devices.

2: The CSS<13:12> and CHH<13:12> bits are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

TABLE 16-1: ADC REGISTER MAP (CONTINUED)

| Virtual Address (BF80_#) | Register Name ⁽³⁾ | Bit Range | Bits | | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|-----------------|--------|----------------------------|-----------|-------|-----------|------------|-----------|------------|-----------|------------|------|---------|------|---------|------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | | 16/0 |
| 07E0 | ADC1BUF14 | 31:16 | ADC1BUF14<31:0> | | | | | | | | | | | | | | | 0000 | |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 | |
| 07F0 | ADC1BUF15 | 31:16 | ADC1BUF15<31:0> | | | | | | | | | | | | | | | 0000 | |
| | | 15:0 | | | | | | | | | | | | | | | | 0000 | |
| 0800 | AD1CON1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | FORM<2:0> | | SSRC<3:0> | | | MODE12 | ASAM | SAMP | DONE | — | 0000 | |
| 0810 | AD1CON2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | VCFG<2:0> | | OFFCAL | BUFREGEN | CSCNA | — | — | BUFS | — | SMPI<3:0> | | | — | — | — | — | 0000 |
| 0820 | AD1CON3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ADRC | EXTSAM | — | SAMC<4:0> | | | | ADCS<7:0> | | | | | | | — | 0000 | |
| 0840 | AD1CHS | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CH0NA<2:0> | | CH0SA<4:0> | | | | | | — |
| 0850 | AD1CSS | 31:16 | CSS<30:28> | | | | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CSS<13:0> ^(1,2) | | | | | | | | | | | — | 0000 | | |
| 0870 | AD1CON5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ASEN | LPEN | — | BGREQ | — | — | ASINT<1:0> | | — | — | — | — | WM<1:0> | | CM<1:0> | | — |
| 0880 | AD1CHIT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CHH<13:0> ^(1,2) | | | | | | | | | | | — | 0000 | | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The CSS<13:11> and CHH<13:11> bits are not implemented in 20-pin devices.

2: The CSS<13:12> and CHH<13:12> bits are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 16-1: AD1CON1: ADC CONTROL REGISTER 1

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------------|---------------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON | — | SIDL | — | — | FORM<2:0> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0, HSC | R/W-0, HSC |
| | SSRC<3:0> | | | | MODE12 | ASAM | SAMP ^(1,3) | DONE ⁽²⁾ |

| | |
|-------------------|---------------------------------------|
| Legend: | HSC = Hardware Settable/Clearable bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ADC Operating Mode bit

1 = ADC module is operating
0 = ADC is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** ADC Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits

For 12-Bit Operation (MODE12 bit = 1):

111 = Signed Fractional 32-bit (DOUT = sddd dddd dddd 0000 0000 0000 0000)
110 = Fractional 32-bit (DOUT = dddd dddd dddd 0000 0000 0000 0000)
101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sddd dddd dddd)
100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 dddd dddd dddd)
011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dddd 0000)
010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dddd 0000)
001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sddd dddd dddd)
000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 dddd dddd dddd)

For 10-Bit Operation (MODE12 bit = 0):

111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000)
101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

- Note 1:** The SAMP bit is cleared and cannot be written if the ADC is disabled (ON bit = 0).
Note 2: The DONE bit is not persistent in Automatic modes; it is cleared by hardware at the beginning of the next sample.
Note 3: In Manual Sample/Manual Convert mode, the sample time must be greater than 3 TAD.
Note 4: This mode is not available as a trigger when in Threshold Detect mode (ASEN = 1).

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REGISTER 16-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

- bit 7-4 **SSRC<3:0>**: Conversion Trigger Source Select bits
- 1111-1101 = Reserved
 - 1100 = CLC2 module event ends sampling and starts conversion
 - 1011 = CLC1 module event ends sampling and starts conversion
 - 1010 = SCCP3 module event ends sampling and starts conversion
 - 1001 = SCCP2 module event ends sampling and starts conversion
 - 1000 = M CCP1 module event ends sampling and starts conversion
 - 0111 = Internal counter ends sampling and starts conversion (auto-convert)
 - 0110 = Timer1 period match ends sampling and starts conversion (can trigger during Sleep mode)
 - 0101 = Timer1 period match ends sampling and starts conversion (will not trigger during Sleep mode)
 - 0100-0010 = Reserved
 - 0001 = Active transition on INT0 pin ends sampling and starts conversion
 - 0000 = Clearing the SAMP bit ends sampling and starts conversion⁽⁴⁾
- bit 3 **MODE12**: 12-Bit Operation Mode bit
- 1 = 12-bit ADC operation
 - 0 = 10-bit ADC operation
- bit 2 **ASAM**: ADC Sample Auto-Start bit
- 1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
 - 0 = Sampling begins when SAMP bit is set
- bit 1 **SAMP**: ADC Sample Enable bit^(1,3)
- 1 = The ADC Sample-and-Hold Amplifier (SHA) is sampling
 - 0 = The ADC Sample-and-Hold Amplifier is holding
- bit 0 **DONE**: ADC Conversion Status bit⁽²⁾
- 1 = Analog-to-Digital conversion is done
 - 0 = Analog-to-Digital conversion is not done or has not started
- Clearing this bit will not affect any operation in progress.

- Note 1:** The SAMP bit is cleared and cannot be written if the ADC is disabled (ON bit = 0).
- Note 2:** The DONE bit is not persistent in Automatic modes; it is cleared by hardware at the beginning of the next sample.
- Note 3:** In Manual Sample/Manual Convert mode, the sample time must be greater than 3 TAD.
- Note 4:** This mode is not available as a trigger when in Threshold Detect mode (ASEN = 1).

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REGISTER 16-3: AD1CON3: ADC CONTROL REGISTER 3

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADRC | EXTSAM | — | SAMC<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADCS<7:0> | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source (TSRC) bit
 1 = Clock derived from Fast RC (FRC) oscillator
 0 = Clock derived from Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK)

bit 14 **EXTSAM:** Extended Sampling Time bit
 1 = ADC is still sampling after SAMP bit = 0
 0 = ADC stops sampling when SAMP bit = 0

bit 13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
 11111 = 31 TAD
 •
 •
 •
 00001 = 1 TAD
 00000 = 0 TAD (not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits
 11111111 = $2 \cdot \text{TSRC} \cdot \text{ADCS}<7:0> = 510 \cdot \text{TSRC} = \text{TAD}$
 •
 •
 •
 00000001 = $2 \cdot \text{TSRC} \cdot \text{ADCS}<7:0> = 2 \cdot \text{TSRC} = \text{TAD}$
 00000000 = $1 \cdot \text{TSRC} = \text{TAD}$
 Where TSRC is a period of clock selected by the ADRC bit (AD1CON3<15>).

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REGISTER 16-4: AD1CON5: ADC CONTROL REGISTER 5

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|---------------------|----------------|----------------|----------------|----------------|----------------|---------------------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | ASEN ⁽¹⁾ | LPEN | — | BGREQ | — | — | ASINT<1:0> ⁽²⁾ | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | WM<1:0> | | CM<1:0> | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ASEN:** Auto-Scan Enable bit⁽¹⁾

1 = Auto-scan is enabled
0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit

1 = Low power is enabled after scan
0 = Full power is enabled after scan

bit 13 **Unimplemented:** Read as '0'

bit 12 **BGREQ:** Band Gap Request bit

1 = Band gap is enabled when the ADC is enabled and active
0 = Band gap is not enabled by the ADC

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits⁽²⁾

11 = Interrupt after Threshold Detect sequence has completed and a valid compare has occurred
10 = Interrupt after valid compare has occurred
01 = Interrupt after Threshold Detect sequence has completed
00 = No interrupt

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **WM<1:0>:** Write Mode bits

11 = Reserved
10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CM<1:0> and ASINT<1:0> bits)
01 = Convert and save (conversion results saved to ADC1BUFx registers when a match occurs, as defined by the CM<1:0> bits)
00 = Threshold (Comparison) mode is disabled, legacy operation (conversion data saved to ADC1BUFx registers)

Note 1: When auto-scan is enabled (ASEN (AD1CON5<15>) = 1), the CSCNA (AD1CON2<10>) and SMPI<3:0> (AD1CON2<5:2>) bits are ignored.

2: The ASINT<1:0> bits setting only takes effect when ASEN (AD1CON5<15>) = 1. Interrupt generation is governed by the SMPI<3:0> bits field.

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REGISTER 16-4: AD1CON5: ADC CONTROL REGISTER 5 (CONTINUED)

bit 1-0 **CM<1:0>**: Compare Mode bits

- 11 = Outside Window mode (valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair)
- 10 = Inside Window mode (valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair)
- 01 = Greater Than mode (valid match occurs if the result is greater than the value in the corresponding buffer register)
- 00 = Less Than mode (valid match occurs if the result is less than the value in the corresponding buffer register)

Note 1: When auto-scan is enabled (ASEN (AD1CON5<15>) = 1), the CSCNA (AD1CON2<10>) and SMPI<3:0> (AD1CON2<5:2>) bits are ignored.

2: The ASINT<1:0> bits setting only takes effect when ASEN (AD1CON5<15>) = 1. Interrupt generation is governed by the SMPI<3:0> bits field.

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REGISTER 16-5: AD1CHS: ADC INPUT SELECT REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|---------------------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CH0NA<2:0> | | | | CH0SA<4:0> ⁽¹⁾ | | | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-5 **CH0NA<2:0>:** Negative Input Select bits

111-001 = Reserved
000 = Negative input is AVss

bit 4-0 **CH0SA<4:0>:** Positive Input Select bits⁽¹⁾

11111 = Reserved
11110 = Positive input is AVDD
11101 = Positive input is AVSS
11100 = Positive input is Band Gap Reference (VBG)
11011-01110 = Reserved
01101 = Positive input is AN13^(2,3)
01100 = Positive input is AN12^(2,3)
01011 = Positive input is AN11⁽²⁾
01010 = Positive input is AN10
01001 = Positive input is AN9
01000 = Positive input is AN8
00111 = Positive input is AN7
00110 = Positive input is AN6
00101 = Positive input is AN5
00100 = Positive input is AN4
00011 = Positive input is AN3
00010 = Positive input is AN2
00001 = Positive input is AN1
00000 = Positive input is AN0

Note 1: The CH0SA<4:0> positive input selection is only used when CSCNA (AD1CON2<10>) = 0 and ASEN (AD1CON5<15>) = 0. The AD1CSS bits specify the positive inputs when CSCNA = 1 or ASEN = 1.

2: This option is not implemented in the 20-pin devices.

3: This option is not implemented in the 28-pin devices.

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REGISTER 16-6: AD1CSS: ADC INPUT SCAN SELECT REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | CSS<30:28> | | | | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSS<13:8> ^(1,2) | | | | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSS<7:0> | | | | | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 31 **Unimplemented:** Read as '0'
- bit 30-28 **CSS<30:28>**: ADC Input Pin Scan Selection bits
 1 = Selects ANx for the input scan
 0 = Skips ANx for the input scan
- bit 27-14 **Unimplemented:** Read as '0'
- bit 13-0 **CSS<13:0>**: ADC Input Pin Scan Selection bits^(1,2)
 1 = Selects ANx for the input scan
 0 = Skips ANx for the input scan

- Note 1:** The CSS<13:11> bits are not implemented in 20-pin devices.
Note 2: The CSS<13:12> bits are not implemented in 28-pin devices.

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REGISTER 16-7: AD1CHIT: ADC COMPARE HIT REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|-------------------|-------------------|----------------------------|-------------------|-------------------|-------------------|------------------|------------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | CHH<13:8> ^(1,2) | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHH<7:0> | | | | | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-14 **Unimplemented:** Read as '0'

bit 13-0 **CHH<13:0>:** ADC Compare Hit bits^(1,2)

If CM<1:0> = 11:

1 = ADC Result Buffer x has been written with data or a match has occurred

0 = ADC Result Buffer x has not been written with data

For All Other Values of CM<1:0>:

1 = A match has occurred on ADC Result Channel n

0 = No match has occurred on ADC Result Channel n

Note 1: The CHH<13:11> bits are not implemented in 20-pin devices.

Note 2: The CHH<13:12> bits are not implemented in 28-pin devices.

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NOTES:

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17.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 60. “32-Bit Programmable Cyclic Redundancy Check”** (DS60001336) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

Figure 17-1 displays a simplified block diagram of the CRC generator.

FIGURE 17-1: CRC BLOCK DIAGRAM

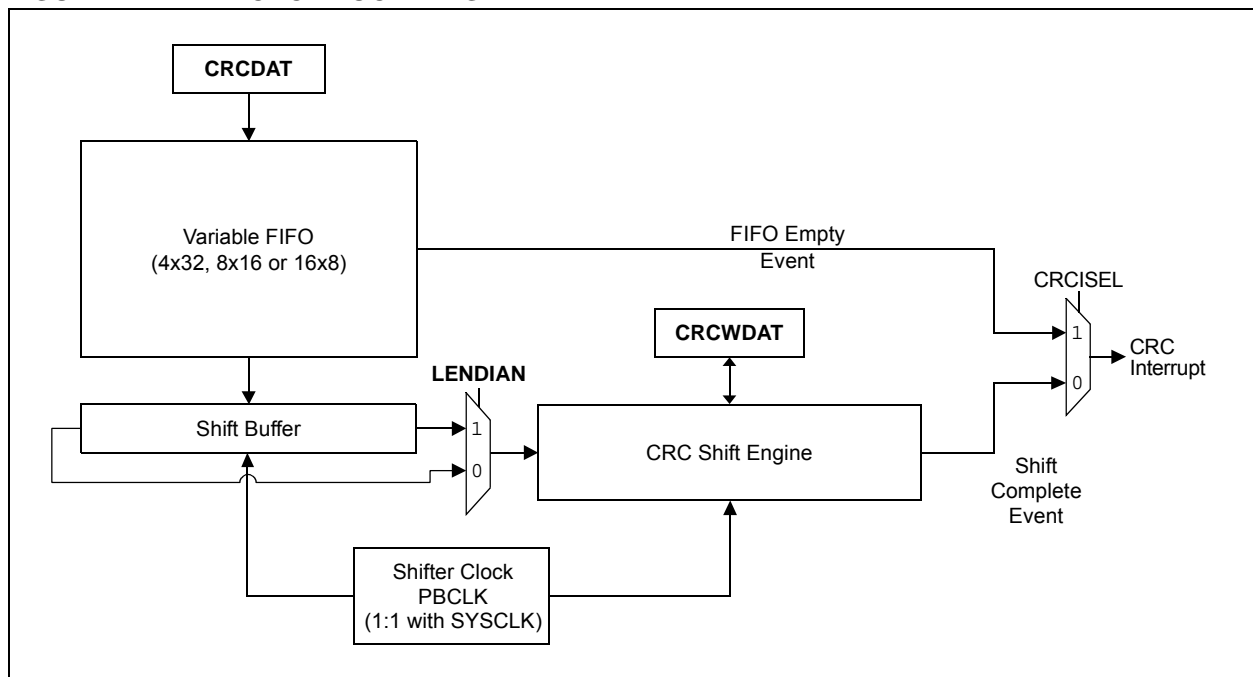


TABLE 17-1: CRC REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | All Resets |
|-----------------------------|---------------------------------|-----------|---------------|-------|-------|-------------|-------|-------|------|--------|--------|---------|-----------|---------|------|------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | |
| 0A00 | CRCCON | 31:16 | — | — | — | DWIDTH<4:0> | | | | — | — | — | PLEN<4:0> | | | | 0000 |
| | | 15:0 | ON | — | SIDL | VWORD<4:0> | | | | CRCFUL | CRCMPT | CRCISEL | CRCGO | LENDIAN | MOD | — | — |
| 0A10 | CRCXOR | 31:16 | X<31:16> | | | | | | | | | | | | | | 0000 |
| | | 15:0 | X<15:1> | | | | | | | | | | | | | — | 0000 |
| 0A20 | CRCDAT | 31:16 | CRCDAT<31:0> | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | 0000 |
| 0A30 | CRCWDAT | 31:16 | CRCWDAT<31:0> | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 17-1: CRCCON: CRC CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | DWIDTH<4:0> | | | | |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | PLEN<4:0> | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | ON | — | SIDL | VWORD<4:0> | | | | |
| 7:0 | R-0, HS, HC | R-1, HS, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | CRCFUL | CRCMPT | CRCISEL | CRCGO | LENDIAN | MOD | — | — |

| | | |
|-------------------|-----------------------------|------------------------------------|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **DWIDTH<4:0>:** Data Word Width Configuration bits
Configures the width of the data word (Data Word Width – 1).

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **PLEN<4:0>:** Polynomial Length Configuration bits
Configures the length of the polynomial (Polynomial Length – 1).

bit 15 **ON:** CRC Enable bit
1 = Enables module
0 = Disables module

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** CRC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **VWORD<4:0>:** Counter Value bits
Indicates the number of valid words in the FIFO. Has a maximum value of 16 when DWIDTH<4:0> ≤ 8 (data words, 8-bit wide or less). Has a maximum value of 8 when DWIDTH<4:0> ≤ 15 (data words from 9 to 16-bit wide). Has a maximum value of 4 when DWIDTH<4:0> ≤ 31 (data words from 17 to 32-bit wide).

bit 7 **CRCFUL:** CRC FIFO Full bit
1 = FIFO is full
0 = FIFO is not full

bit 6 **CRCMPT:** CRC FIFO Empty bit
1 = FIFO is empty
0 = FIFO is not empty

bit 5 **CRCISEL:** CRC Interrupt Selection bit
1 = Interrupt on FIFO is empty; final word of data is still shifted through CRC
0 = Interrupt on shift is complete (FIFO is empty and no data is shifted from the shift buffer)

bit 4 **CRCGO:** Start CRC bit
1 = Starts CRC serial shifter; clearing the bit aborts shifting
0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
1 = Data word is shifted into the CRC, starting with the LSb (little-endian); reflected input data
0 = Data word is shifted into the CRC, starting with the MSb (big-endian); non-reflected input data

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REGISTER 17-1: CRCCON: CRC CONTROL REGISTER (CONTINUED)

- bit 2 **MOD:** CRC Calculation Mode bit
 1 = Alternate mode
 0 = Legacy mode
- bit 1-0 **Unimplemented:** Read as '0'

REGISTER 17-2: CRCXOR: CRC XOR REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | X<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | X<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | X<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| | X<7:1> | | | | | | | — |

Legend:

| | | |
|-------------------|------------------|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 31-1 **X<31:1>:** XOR of Polynomial Term X^n Enable bits
- bit 0 **Unimplemented:** Read as '0'

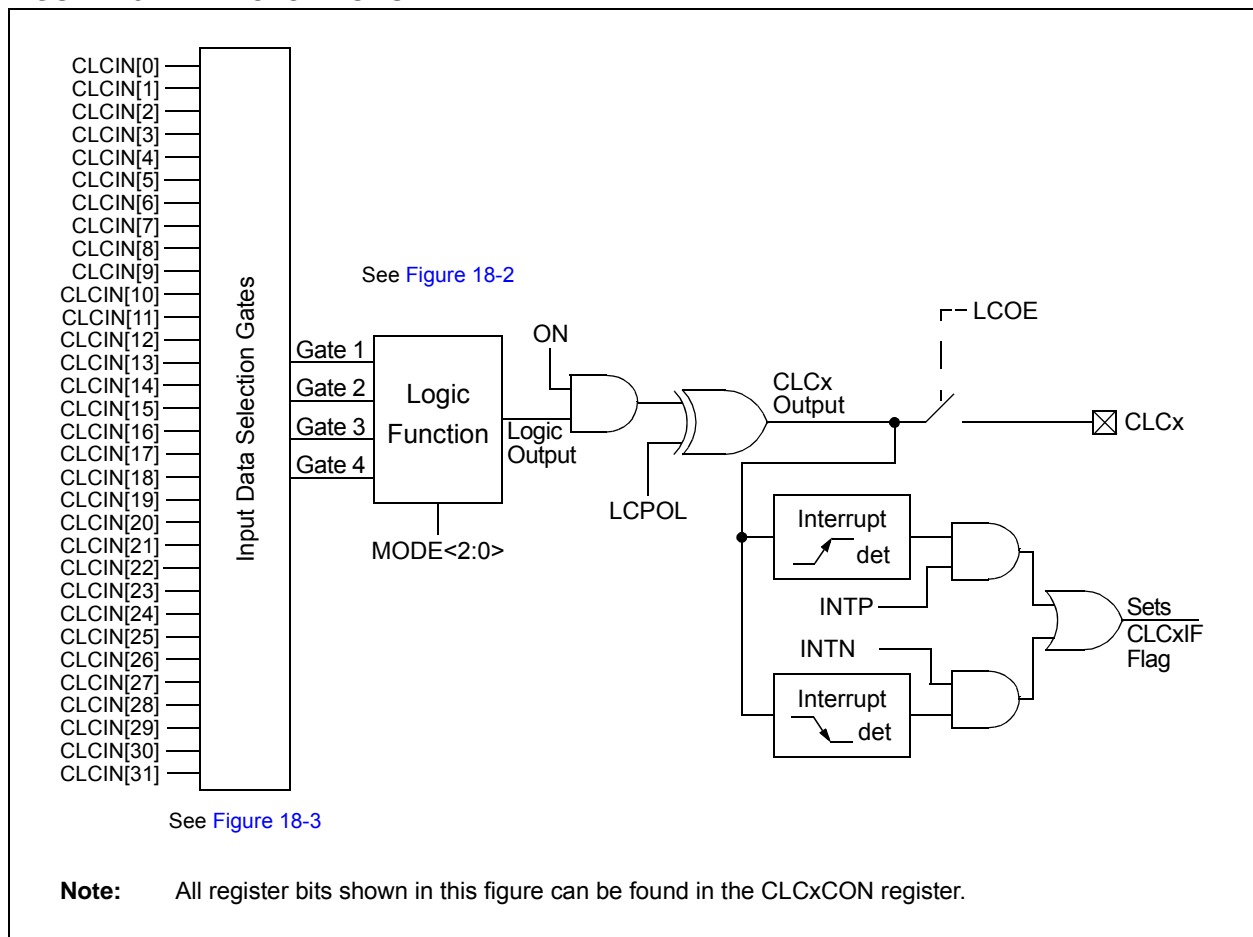
18.0 CONFIGURABLE LOGIC CELL (CLC)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 36. “Configurable Logic Cell”** (DS60001363) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution, and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 18-1 shows an overview of the module. Figure 18-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 18-1: CLCx MODULE



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FIGURE 18-2: CLCx LOGIC FUNCTION COMBINATORIAL OPTIONS

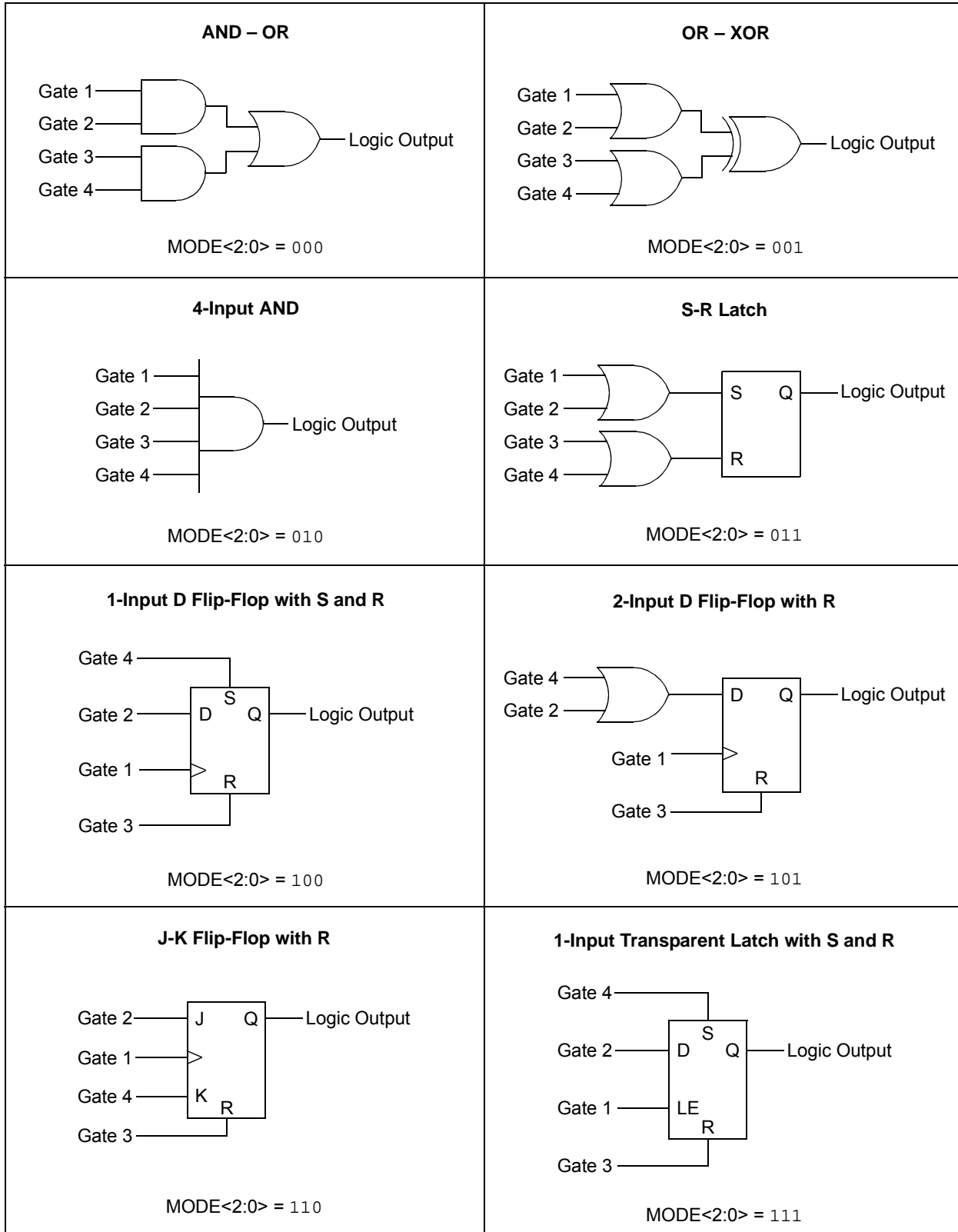
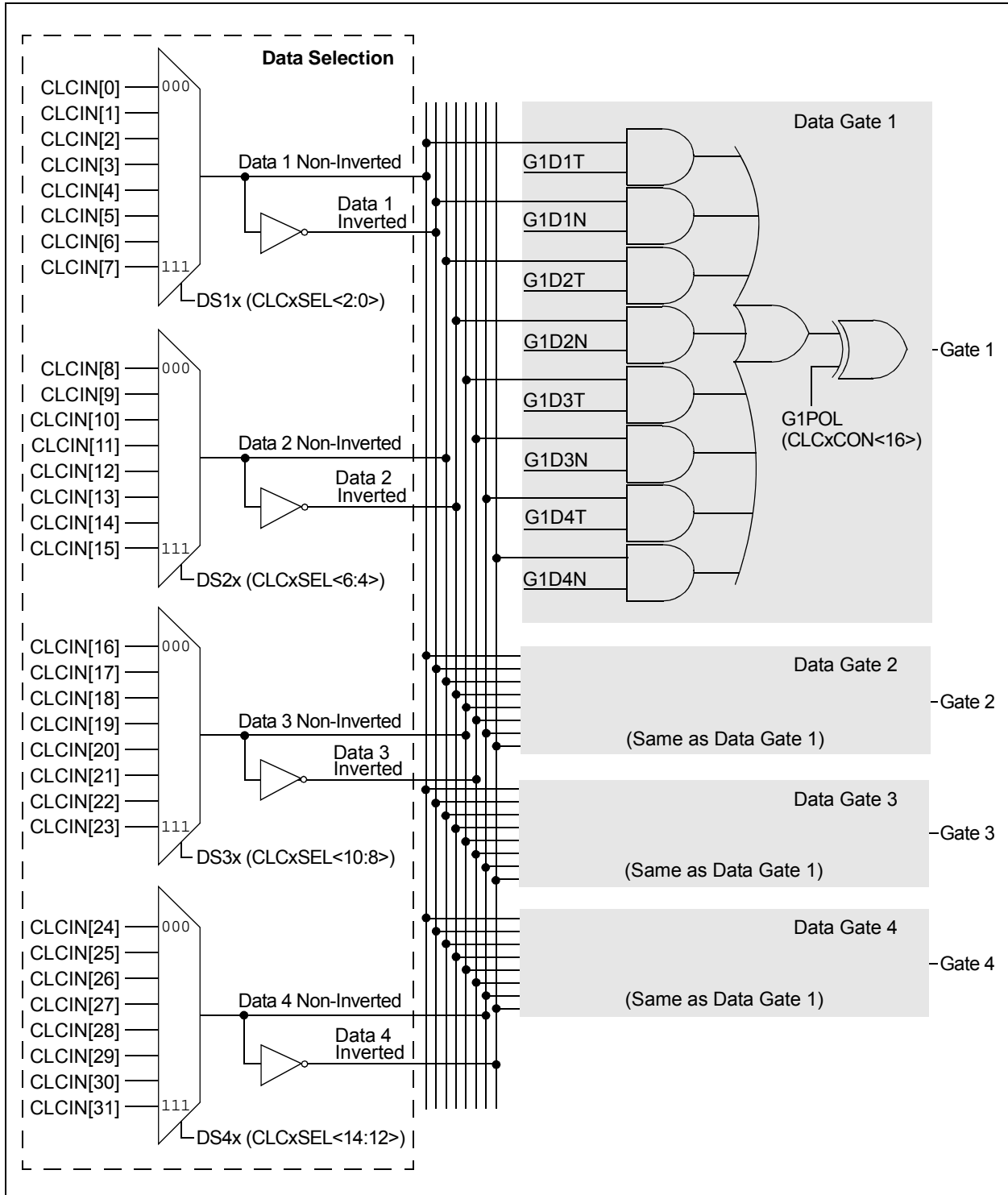


FIGURE 18-3: CLCx INPUT SOURCE SELECTION DIAGRAM



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18.1 Control Registers

The CLCx module is controlled by the following registers:

- CLCxCON
- CLCxSEL
- CLCxGLS

The CLCx Control register (CLCxCON) is used to enable the module and interrupts, control the output enable bit, select output polarity and select the logic function. The CLCx Control registers also allow the user to control the logic polarity of not only the cell output, but also some intermediate variables.

The CLCx Input MUX Select register (CLCxSEL) allows the user to select up to 4 data input sources using the 4 data input selection multiplexers. Each multiplexer has a list of 8 data sources available.

The CLCx Gate Logic Input Select register (CLCxGLS) allows the user to select which outputs from each of the selection MUXes are used as inputs to the input gates of the logic cell. Each data source MUX outputs both a true and a negated version of its output. All of these 8 signals are enabled, ORed together by the logic cell input gates.

TABLE 18-1: CLC1 AND CLC2 REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|-------|----------|-------|-------|-------|-------|----------|-------|-------|-------|-------|----------|-------|-------|-----------|-------|------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | | |
| 0A80 | CLC1CON | 32:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | G4POL | G3POL | G2POL | G1POL | 0000 |
| | | 15:0 | ON | — | — | — | — | INTP | INTN | — | — | LCOE | LCOUT | LCPOL | — | — | MODE<2:0> | | | 0000 |
| 0A90 | CLC1SEL | 32:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | DS4<2:0> | | | | — | DS3<2:0> | | | | — | DS2<2:0> | | | | — | DS1<2:0> | |
| 0AA0 | CLC1GLS | 32:16 | G4D4T | G4D4N | G4D3T | G4D3N | G4D2T | G4D2N | G4D1T | G4D1N | G3D4T | G3D4N | G3D3T | G3D3N | G3D2T | G3D2N | G3D1T | G3D1N | 0000 | |
| | | 15:0 | G2D4T | G2D4N | G2D3T | G2D3N | G2D2T | G2D2N | G2D1T | G2D1N | G1D4T | G1D4N | G1D3T | G1D3N | G1D2T | G1D2N | G1D1T | G1D1N | 0000 | |
| 0B00 | CLC2CON | 32:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | G4POL | G3POL | G2POL | G1POL | 0000 |
| | | 15:0 | ON | — | — | — | — | INTP | INTN | — | — | LCOE | LCOUT | LCPOL | — | — | MODE<2:0> | | | 0000 |
| 0B10 | CLC2SEL | 32:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | DS4<2:0> | | | | — | DS3<2:0> | | | | — | DS2<2:0> | | | | — | DS1<2:0> | |
| 0B20 | CLC2GLS | 32:16 | G4D4T | G4D4N | G4D3T | G4D3N | G4D2T | G4D2N | G4D1T | G4D1N | G3D4T | G3D4N | G3D3T | G3D3N | G3D2T | G3D2N | G3D1T | G3D1N | 0000 | |
| | | 15:0 | G2D4T | G2D4N | G2D3T | G2D3N | G2D2T | G2D2N | G2D1T | G2D1N | G1D4T | G1D4N | G1D3T | G1D3N | G1D2T | G1D2N | G1D1T | G1D1N | 0000 | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 18-1: CLCxCON: CLCx CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|---------------------|---------------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | G4POL | G3POL | G2POL | G1POL |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | ON | — | — | — | INTP ⁽¹⁾ | INTN ⁽¹⁾ | — | — |
| 7:0 | R/W-0 | R-0, HS, HC | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | LCOE | LCOUT | LCPOL | — | — | MODE<2:0> | | |

| | | |
|-------------------|-----------------------------|--|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-20 **Unimplemented:** Read as '0'

bit 19 **G4POL:** Gate 4 Polarity Control bit

1 = The output of Channel 4 logic is inverted when applied to the logic cell
0 = The output of Channel 4 logic is not inverted

bit 18 **G3POL:** Gate 3 Polarity Control bit

1 = The output of Channel 3 logic is inverted when applied to the logic cell
0 = The output of Channel 3 logic is not inverted

bit 17 **G2POL:** Gate 2 Polarity Control bit

1 = The output of Channel 2 logic is inverted when applied to the logic cell
0 = The output of Channel 2 logic is not inverted

bit 16 **G1POL:** Gate 1 Polarity Control bit

1 = The output of Channel 1 logic is inverted when applied to the logic cell
0 = The output of Channel 1 logic is not inverted

bit 15 **ON:** CLCx Enable bit

1 = CLCx is enabled and mixing input signals
0 = CLCx is disabled and has logic zero outputs

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **INTP:** CLCx Positive Edge Interrupt Enable bit⁽¹⁾

1 = Interrupt will be generated when a rising edge occurs on LCOUT
0 = Interrupt will not be generated

bit 10 **INTN:** CLCx Negative Edge Interrupt Enable bit⁽¹⁾

1 = Interrupt will be generated when a falling edge occurs on LCOUT
0 = Interrupt will not be generated

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **LCOE:** CLCx Port Enable bit

1 = CLCx port pin output is enabled
0 = CLCx port pin output is disabled

bit 6 **LCOUT:** CLCx Data Output Status bit

1 = CLCx output high
0 = CLCx output low

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

REGISTER 18-1: CLCxCON: CLCx CONTROL REGISTER (CONTINUED)

- bit 5 **LCPOL**: CLCx Output Polarity Control bit
 1 = The output of the module is inverted
 0 = The output of the module is not inverted
- bit 4-3 **Unimplemented**: Read as '0'
- bit 2-0 **MODE<2:0>**: CLCx Mode bits
 111 = Cell is a 1-input transparent latch with S and R
 110 = Cell is a JK flip-flop with R
 101 = Cell is a 2-input D flip-flop with R
 100 = Cell is a 1-input D flip-flop with S and R
 011 = Cell is an SR latch
 010 = Cell is a 4-input AND
 001 = Cell is an OR-XOR
 000 = Cell is a AND-OR

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

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REGISTER 18-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | DS4<2:0> | | | — | DS3<2:0> | | |
| 7:0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | DS2<2:0> | | | — | DS1<2:0> | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14-12 **DS4<2:0>**: Data Selection MUX 4 Signal Selection bits

For CLC1:

111 = SCCP3 compare match event

110 = MCCP1 compare match event

101 = RTCC event

100 = Reserved

011 = SPI1 SDI input

010 = SCCP3 OCM3 output

001 = CLC2 output

000 = CLCINB I/O pin

For CLC2:

111 = SCCP3 compare match event

110 = MCCP1 compare match event

101 = RTCC event

100 = Reserved

011 = SPI2 SDI input

010 = SCCP3 OCM3 output

001 = CLC1 output

000 = CLCINB I/O pin

bit 11 **Unimplemented:** Read as '0'

REGISTER 18-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 10-8 **DS3<2:0>**: Data Selection MUX 3 Signal Selection bits

For CLC1:

111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART1 RX input
011 = SPI1 SDO output
010 = Comparator 2 output
001 = CLC1 output
000 = CLCINA I/O pin

For CLC2:

111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART2 RX input
011 = SPI2 SDO output
010 = Comparator 2 output
001 = CLC2 output
000 = CLCINA I/O pin

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **DS2<2:0>**: Data Selection MUX 2 Signal Selection bits

For CLC1:

111 = Reserved
110 = M CCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion (EOC) event
011 = UART1 TX output
010 = Comparator 1 output
001 = CLC2 output
000 = CLCINB I/O pin

For CLC2:

111 = Reserved
110 = M CCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion event
011 = UART2 TX output
010 = Comparator 1 output
001 = CLC1 output
000 = CLCINB I/O pin

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DS1<2:0>**: Data Selection MUX 1 Signal Selection bits

111 = M CCP1 OCM1C output
110 = M CCP1 OCM1B output
101 = M CCP1 OCM1A output
100 = REFCLKO output
011 = LPRC clock source
010 = SOSC clock source
001 = System clock (FSYS)
000 = CLCINA I/O pin

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REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | G4D4T | G4D4N | G4D3T | G4D3N | G4D2T | G4D2N | G4D1T | G4D1N |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | G3D4T | G3D4N | G3D3T | G3D3N | G3D2T | G3D2N | G3D1T | G3D1N |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | G2D4T | G2D4N | G2D3T | G2D3N | G2D2T | G2D2N | G2D1T | G2D1N |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | G1D4T | G1D4N | G1D3T | G1D3N | G1D2T | G1D2N | G1D1T | G1D1N |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **G4D4T:** Gate 4 Data Source 4 True Enable bit
 1 = The Data Source 4 signal is enabled for Gate 4
 0 = The Data Source 4 signal is disabled for Gate 4
- bit 30 **G4D4N:** Gate 4 Data Source 4 Negated Enable bit
 1 = The Data Source 4 inverted signal is enabled for Gate 4
 0 = The Data Source 4 inverted signal is disabled for Gate 4
- bit 29 **G4D3T:** Gate 4 Data Source 3 True Enable bit
 1 = The Data Source 3 signal is enabled for Gate 4
 0 = The Data Source 3 signal is disabled for Gate 4
- bit 28 **G4D3N:** Gate 4 Data Source 3 Negated Enable bit
 1 = The Data Source 3 inverted signal is enabled for Gate 4
 0 = The Data Source 3 inverted signal is disabled for Gate 4
- bit 27 **G4D2T:** Gate 4 Data Source 2 True Enable bit
 1 = The Data Source 2 signal is enabled for Gate 4
 0 = The Data Source 2 signal is disabled for Gate 4
- bit 26 **G4D2N:** Gate 4 Data Source 2 Negated Enable bit
 1 = The Data Source 2 inverted signal is enabled for Gate 4
 0 = The Data Source 2 inverted signal is disabled for Gate 4
- bit 25 **G4D1T:** Gate 4 Data Source 1 True Enable bit
 1 = The Data Source 1 signal is enabled for Gate 4
 0 = The Data Source 1 signal is disabled for Gate 4
- bit 24 **G4D1N:** Gate 4 Data Source 1 Negated Enable bit
 1 = The Data Source 1 inverted signal is enabled for Gate 4
 0 = The Data Source 1 inverted signal is disabled for Gate 4
- bit 23 **G3D4T:** Gate 3 Data Source 4 True Enable bit
 1 = The Data Source 4 signal is enabled for Gate 3
 0 = The Data Source 4 signal is disabled for Gate 3
- bit 22 **G3D4N:** Gate 3 Data Source 4 Negated Enable bit
 1 = The Data Source 4 inverted signal is enabled for Gate 3
 0 = The Data Source 4 inverted signal is disabled for Gate 3
- bit 21 **G3D3T:** Gate 3 Data Source 3 True Enable bit
 1 = The Data Source 3 signal is enabled for Gate 3
 0 = The Data Source 3 signal is disabled for Gate 3

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REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

- bit 20 **G3D3N:** Gate 3 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 3
0 = The Data Source 3 inverted signal is disabled for Gate 3
- bit 19 **G3D2T:** Gate 3 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 3
0 = The Data Source 2 signal is disabled for Gate 3
- bit 18 **G3D2N:** Gate 3 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 3
0 = The Data Source 2 inverted signal is disabled for Gate 3
- bit 17 **G3D1T:** Gate 3 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 3
0 = The Data Source 1 signal is disabled for Gate 3
- bit 16 **G3D1N:** Gate 3 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 3
0 = The Data Source 1 inverted signal is disabled for Gate 3
- bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 2
0 = The Data Source 4 signal is disabled for Gate 2
- bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2
- bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 2
0 = The Data Source 3 signal is disabled for Gate 2
- bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2
- bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 2
0 = The Data Source 2 signal is disabled for Gate 2
- bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2
- bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 2
0 = The Data Source 1 signal is disabled for Gate 2
- bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 2
0 = The Data Source 1 inverted signal is disabled for Gate 2
- bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 1
0 = The Data Source 4 signal is disabled for Gate 1
- bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1
- bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 1
0 = The Data Source 3 signal is disabled for Gate 1

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REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

- bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
 1 = The Data Source 3 inverted signal is enabled for Gate 1
 0 = The Data Source 3 inverted signal is disabled for Gate 1
- bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
 1 = The Data Source 2 signal is enabled for Gate 1
 0 = The Data Source 2 signal is disabled for Gate 1
- bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
 1 = The Data Source 2 inverted signal is enabled for Gate 1
 0 = The Data Source 2 inverted signal is disabled for Gate 1
- bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
 1 = The Data Source 1 signal is enabled for Gate 1
 0 = The Data Source 1 signal is disabled for Gate 1
- bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
 1 = The Data Source 1 inverted signal is enabled for Gate 1
 0 = The Data Source 1 inverted signal is disabled for Gate 1

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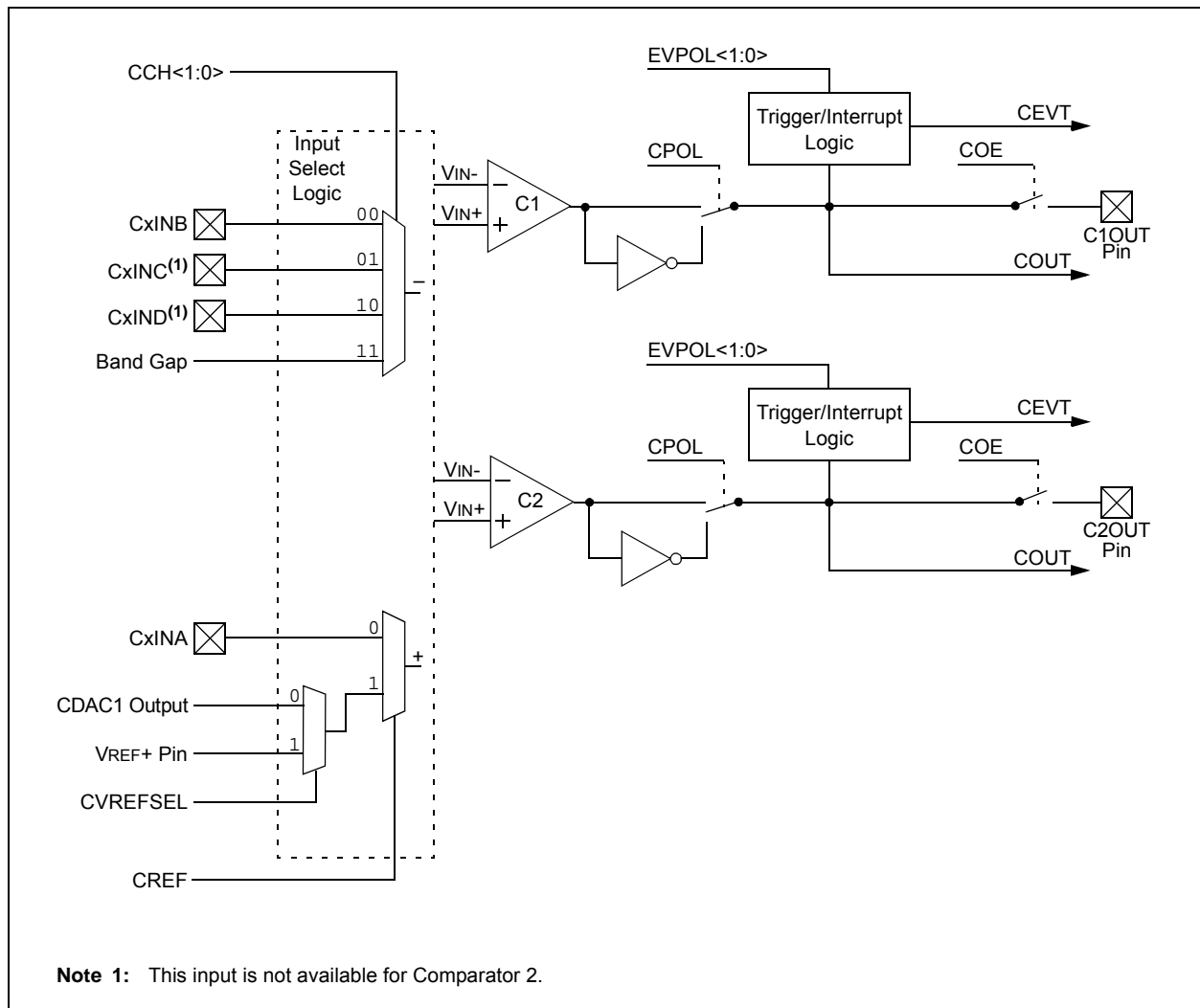
19.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS600011110) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The comparator module provides two dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and VREF+). The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals ‘1’, the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in **Figure 19-1**. Each comparator has its own control register, CMxCON (**Register 19-2**), for enabling and configuring its operation. The output and event status of two comparators is provided in the CMSTAT register (**Register 19-1**).

FIGURE 19-1: DUAL COMPARATOR MODULE BLOCK DIAGRAM



19.1 Comparator Control Registers

TABLE 19-1: COMPARATOR 1 AND 2 REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|-------|-------|-------|------|----------|------------|------|------|------|------|------|----------|------------|-------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | | 16/0 |
| 0900 | CMSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | C2EVT | C1EVT | 0000 |
| | | 15:0 | — | — | SIDL | — | — | — | — | CVREFSEL | — | — | — | — | — | — | — | C2OUT | C1OUT |
| 0910 | CM1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | 0000 |
| 0930 | CM2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 19-1: CMSTAT: COMPARATOR MODULE STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC |
| | — | — | — | — | — | — | C2EVT | C1EVT |
| 15:8 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | — | — | SIDL | — | — | — | — | CVREFSEL |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC |
| | — | — | — | — | — | — | C2OUT | C1OUT |

| | | |
|-------------------|-----------------------------|------------------------------------|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 31-18 **Unimplemented:** Read as '0'

bit 17 **C2EVT:** Comparator 2 Event Status bit (read-only)
Shows the current event status of Comparator 2 (CM2CON<9>).

bit 16 **C1EVT:** Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON<9>).

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all enabled comparators in Idle mode

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **CVREFSEL:** Comparator Reference Voltage Select Enable bit
1 = External voltage reference from the VREF+ pin is selected
0 = Voltage from CDAC1 is selected

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **C2OUT:** Comparator 2 Output Status bit (read-only)
Shows the current output of Comparator 2 (CM2CON<8>).

bit 0 **C1OUT:** Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON<8>).

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REGISTER 19-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 AND 2)

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC |
| | ON | COE | CPOL | — | — | — | CEVT | COUT |
| 7:0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | |

| | | |
|-------------------|-----------------------------|--|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Enable bit

1 = Comparator is enabled

0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit

1 = Comparator output is present on the CxOUT pin

0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit

1 = Comparator output is inverted

0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit

1 = Comparator event that is defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared

0 = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit

When CPOL = 0:

1 = $V_{IN+} > V_{IN-}$

0 = $V_{IN+} < V_{IN-}$

When CPOL = 1:

1 = $V_{IN+} < V_{IN-}$

0 = $V_{IN+} > V_{IN-}$

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REGISTER 19-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 AND 2) (CONTINUED)

bit 7-6 **EVPOL<1:0>**: Trigger/Event/Interrupt Polarity Select bits

11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/event/interrupt is generated on transition of the comparator output:

If CPOL = 0 (non-inverted polarity):

High-to-low transition only.

If CPOL = 1 (inverted polarity):

Low-to-high transition only.

01 = Trigger/event/interrupt is generated on transition of the comparator output:

If CPOL = 0 (non-inverted polarity):

Low-to-high transition only.

If CPOL = 1 (inverted polarity):

High-to-low transition only.

00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented**: Read as '0'

bit 4 **CREF**: Comparator Reference Select bit (non-inverting input)

1 = Non-inverting input connects to the internal reference defined by the CVREFSEL bit in the CMSTAT register

0 = Non-inverting input connects to the CxINA pin

bit 3-2 **Unimplemented**: Read as '0'

bit 1-0 **CCH<1:0>**: Comparator Channel Select bits

11 = Inverting input of the comparator connects to the band gap reference voltage

10 = Inverting input of the comparator connects to the CxIND pin

01 = Inverting input of the comparator connects to the CxINC pin

00 = Inverting input of the comparator connects to the CxINB pin

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NOTES:

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20.0 CONTROL DIGITAL-TO-ANALOG CONVERTER (CDAC)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 45. “Control Digital-to-Analog Converter (CDAC)”** (DS60001327) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

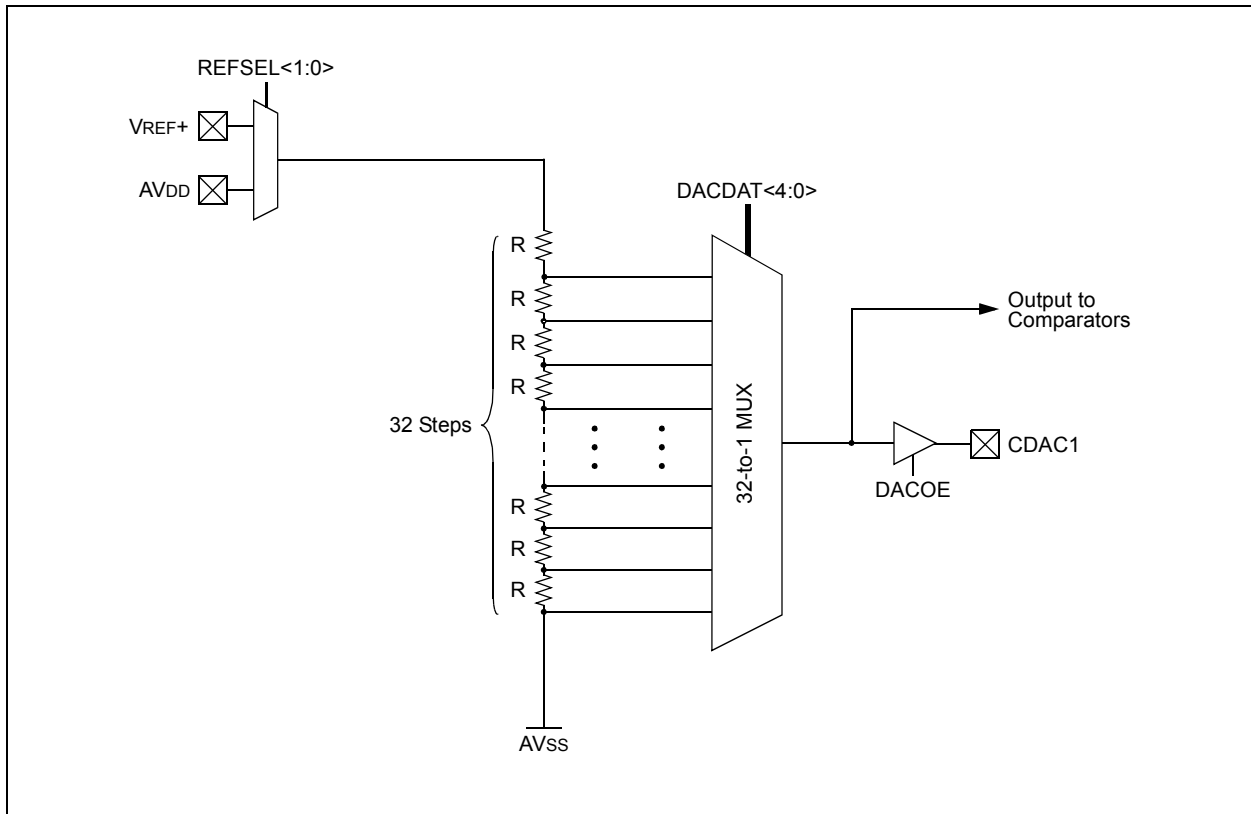
The Control Digital-to-Analog Converter (CDAC) generates analog voltage corresponding to the digital input.

The CDAC has the following features:

- 32 Output Levels are Available
- Internally Connected to Comparators to Conserve Device Pins
- Output can be Connected to a Pin

A block diagram of the CDAC module is illustrated in [Figure 20-1](#).

FIGURE 20-1: CDAC BLOCK DIAGRAM



20.1 CDAC Control Registers

TABLE 20-1: CDAC REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|-------|-------|-------|------|-------|------|------|------|-------------|------|------|-------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | | 17/1 |
| 0980 | DAC1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | DACDAT<4:0> | | | | 0000 |
| | | 15:0 | ON | — | — | — | — | — | — | DACOE | — | — | — | — | — | — | REFSEL<1:0> | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 20-1: DAC1CON: CDAC CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | DACDAT<4:0> | | | | |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | ON | — | — | — | — | — | — | DACOE |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | REFSEL<1:0> | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **DACDAT<4:0>:** CDAC Voltage Reference Selection bits

11111 = (DACDAT<4:0> * VREF+/32) or (DACDAT<4:0> * AVDD/32) volts depending on the REFSEL<1:0> bits

•
•
•

00000 = 0.0 volts

bit 15 **ON:** Voltage Reference Enable bit

1 = Voltage reference is enabled

0 = Voltage reference is disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **DACOE:** CDAC Voltage Reference Output Enable bit

1 = Voltage level is output on the CDAC1 pin

0 = Voltage level is disconnected from the CDAC1 pin

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **REFSEL<1:0>:** CDAC Voltage Reference Source Select bits

11 = Reference voltage is AVDD

10 = No reference is selected – output is AVss

01 = Reference voltage is the VREF+ input pin voltage

00 = No reference is selected – output is AVss

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NOTES:

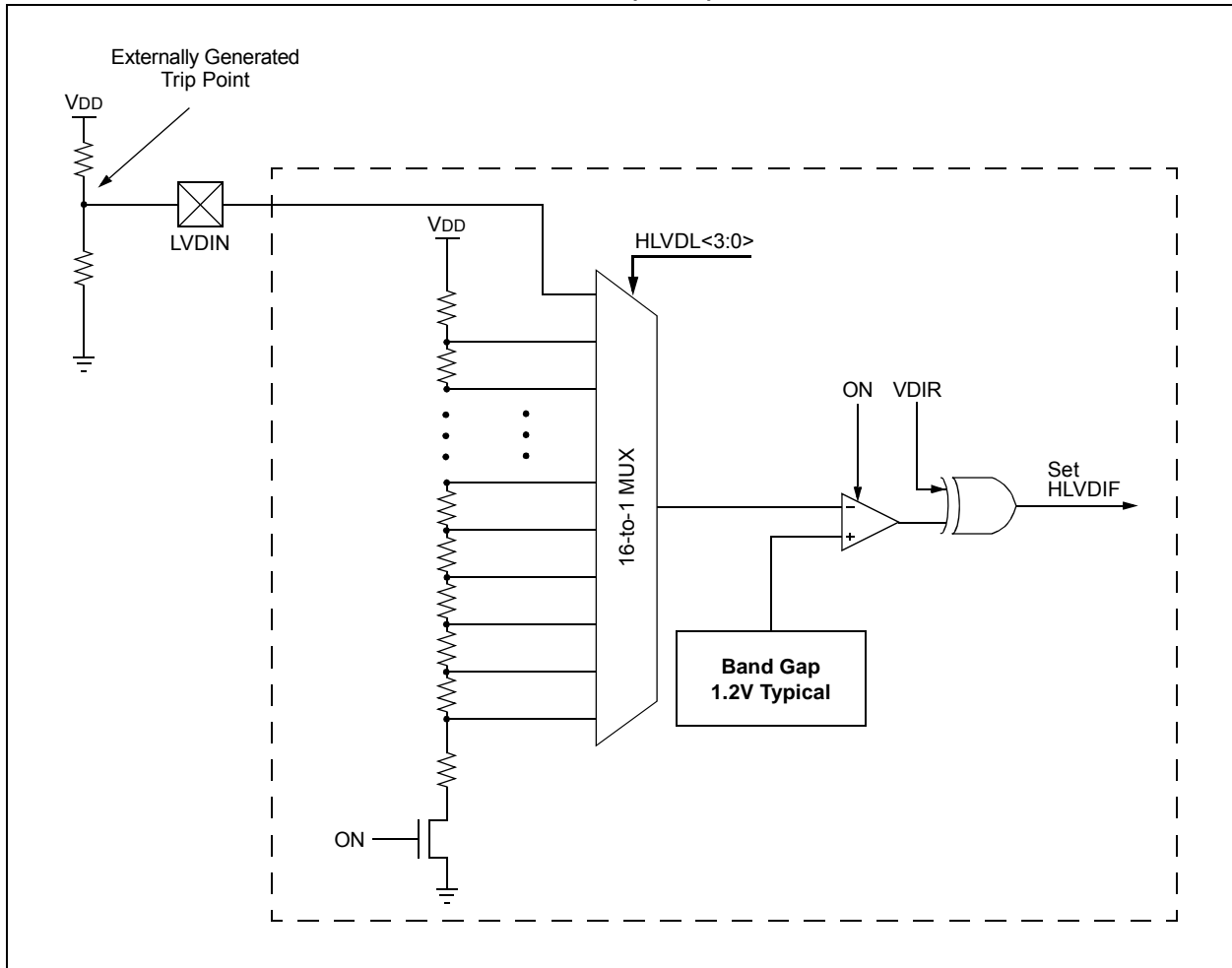
21.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see [Register 21-1](#)) completely controls the operation of the HLVD module. This allows the circuitry to be “turned off” by the user under software control, which minimizes the current consumption for the device.

FIGURE 21-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



21.1 High/Low-Voltage Detect Registers

TABLE 21-1: HIGH/LOW-VOLTAGE DETECT REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|-------|-------|-------|-------|-------|------|------|------|------|------------|------|------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | | 17/1 |
| 2310 | HLVDCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | VDIR | BGVST | IRVST | HLEVT | — | — | — | — | HLVDL<3:0> | | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 21-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | ON | — | SIDL | — | VDIR | BGVST | IRVST | HLEVT |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | HLVDL<3:0> | | | |

| | | |
|-------------------|-----------------------------|--|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** HLVD Power Enable bit

- 1 = HLVD is enabled
- 0 = HLVD is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** HLVD Stop in Idle Mode bit

- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **VDIR:** Voltage Change Direction Select bit

- 1 = Event occurs when voltage equals or exceeds the trip point (HLVDL<3:0>)
- 0 = Event occurs when voltage equals or falls below the trip point (HLVDL<3:0>)

bit 10 **BGVST:** Band Gap Voltage Stable Flag bit

- 1 = Indicates that the band gap voltage is stable
- 0 = Indicates that the band gap voltage is unstable

bit 9 **IRVST:** Internal Reference Voltage Stable Flag bit

- 1 = Internal reference voltage is stable; the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
- 0 = Internal reference voltage is unstable; the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

bit 8 **HLEVT:** High/Low-Voltage Detection Event Status bit

- 1 = Indicates HLVD event is active
- 0 = Indicates HLVD event is not active

bit 7-4 **Unimplemented:** Read as '0'

Note 1: The voltage is typical. It is for design guidance only and not tested. Refer to [Table 26-13](#) in [Section 26.0](#) “[Electrical Characteristics](#)” for minimum and maximum values.

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REGISTER 21-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER (CONTINUED)

bit 3-0 **HLVDL<3:0>**: High/Low-Voltage Detection Limit bits

1111 = External analog input is used (input comes from the LVDIN pin and is compared with 1.2V band gap)

1110 = VDD trip point is 2.11V⁽¹⁾

1101 = VDD trip point is 2.21V⁽¹⁾

1100 = VDD trip point is 2.30V⁽¹⁾

1011 = VDD trip point is 2.40V⁽¹⁾

1010 = VDD trip point is 2.52V⁽¹⁾

1001 = VDD trip point is 2.63V⁽¹⁾

1000 = VDD trip point is 2.82V⁽¹⁾

0111 = VDD trip point is 2.92V⁽¹⁾

0110 = VDD trip point is 3.13V⁽¹⁾

0101 = VDD trip point is 3.44V⁽¹⁾

0100-0000 = Reserved; do not use

Note 1: The voltage is typical. It is for design guidance only and not tested. Refer to [Table 26-13](#) in [Section 26.0](#) “[Electrical Characteristics](#)” for minimum and maximum values.

22.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. “Power-Saving Modes”** (DS60001130) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This section describes power-saving features for the PIC32MM0064GPL036 family devices. These devices offer various methods and modes that allow the application to balance power consumption with device performance. In all of the methods and modes described in this section, power saving is controlled by software. The peripherals and CPU can be halted or disabled to reduce power consumption.

22.1 Sleep Mode

In Sleep mode, the CPU and most peripherals are halted, and the associated clocks are disabled. Some peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep. The device enters Sleep mode when the SLPEN bit (OSCCON<4>) is set and a WAIT instruction is executed.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit remains operative during Sleep mode.
- If WDT is enabled, the Run mode counter is not cleared upon entry to Sleep and the Sleep mode counter is reset upon entering Sleep.
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC and Timer1).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The on-chip regulator enters Standby mode if the VREGS bit (PWRCON<0>) is set.
- A separate special low-power, low-voltage/retention regulator is activated if the RETVR Configuration bit (FPOR<2>) is programmed to zero and the RETEN bit (PWRCON<1>) is set.

The processor will exit, or “wake-up”, from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out.

If the interrupt priority is lower than, or equal to, the current priority, the CPU will remain halted, but the Peripheral Bus Clock (PBCLK) will start running and the device will enter into Idle mode. To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 “System Registers Write Protection”** for details.

22.2 Idle Mode

In Idle mode, the CPU is halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a WAIT instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than, or equal to, the current priority of the CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any form of device Reset.
- On a WDT time-out interrupt.

To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 “System Registers Write Protection”** for details.

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22.3 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not take effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default).

To prevent accidental configuration changes under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK bit in PMDCON register (PMDCON<11>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes. To set or clear PMDLOCK, an unlock sequence must be executed. Refer to [Section 23.4 “System Registers Write Protection”](#) for details.

[Table 22-1](#) lists the module disable bits and locations for all modules.

TABLE 22-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

| Peripheral | PMDx Bit Name | Register Name and Bit Location |
|---|---------------|--------------------------------|
| Analog-to-Digital Converter (ADC) | ADCMD | PMD1<0> |
| Voltage Reference (VR) | VREFMD | PMD1<12> |
| High/Low-Voltage Detect (HLVD) | HLVDM | PMD1<20> |
| Comparator 1 (CMP1) | CMP1MD | PMD2<0> |
| Comparator 2 (CMP2) | CMP2MD | PMD2<1> |
| Configurable Logic Cell 1 (CLC1) | CLC1MD | PMD2<24> |
| Configurable Logic Cell 2 (CLC2) | CLC2MD | PMD2<25> |
| Multiple Outputs Capture/Compare/PWM/Timer1 (MCCP1) | CCP1MD | PMD3<8> |
| Single Output Capture/Compare/PWM/Timer2 (SCCP2) | CCP2MD | PMD3<9> |
| Single Output Capture/Compare/PWM/Timer3 (SCCP3) | CCP3MD | PMD3<10> |
| Timer1 (TMR1) | T1MD | PMD4<0> |
| Universal Asynchronous Receiver Transmitter 1 (UART1) | U1MD | PMD5<0> |
| Universal Asynchronous Receiver Transmitter 2 (UART2) | U2MD | PMD5<1> |
| Serial Peripheral Interface 1 (SPI1) | SPI1MD | PMD5<8> |
| Serial Peripheral Interface 2 (SPI2) | SPI2MD | PMD5<9> |
| Real-Time Clock and Calendar (RTCC) | RTCCMD | PMD6<0> |
| Reference Clock Output (REFCLKO) | REFOMD | PMD6<8> |
| Programmable Cyclic Redundancy Check (CRC) | CRCMD | PMD7<3> |

22.4 On-Chip Voltage Regulator Low-Power Modes

The main on-chip regulator always consumes an incremental amount of current over IDD/IPD, including when the device is in Sleep mode, even though the core digital logic does not require power. To provide additional savings in applications where power resources are critical, the regulator can be made to enter Standby mode

and/or Retention mode. Standby mode is controlled by the VREGS bit (PWRCON<0>), and Retention mode is controlled by the RETEN (PWRCON<1>) and RETVR (FPOR<2>) bits. The available Regulator Low-Power modes are listed in Table 22-2. For more information about the wake-up time and the current consumption for different modes, refer to the electrical specifications listed in Table 26-6 and Table 26-22.

TABLE 22-2: VOLTAGE REGULATOR LOW-POWER MODES

| Mode | VREGS Bit (PWRCON<0>) | RETEN Bit (PWRCON<1>) | RETVR Bit (FPOR<2>) | Wake-up Time (Table 26-22) | Current (Table 26-6) |
|-----------------------|-----------------------|-----------------------|---------------------|----------------------------|----------------------|
| Normal | 1 | 0 | 1 | Fastest | Highest |
| Standby Only | 0 | 0 | 1 | Medium | Medium |
| Retention Only | 1 | 1 | 0 | Medium | Medium |
| Standby and Retention | 0 | 1 | 0 | Slowest | Lowest |

22.4.1 REGULATOR STANDBY MODE

Whenever the device goes into Sleep mode, the regulator can be made to enter Standby mode. This feature is controlled by the VREGS bit (PWRCON<0>). Clearing the VREGS bit enables Standby mode. If Standby mode is used, the voltage regulator needs some time to switch to normal operation mode and generate output. During this time, the code execution is disabled. The delay is applied every time the device resumes operation after Standby mode.

and the RTCC, while all other core digital logic is powered down. The low-voltage/retention regulator is available only when Sleep mode is invoked. It is controlled by the RETVR Configuration bit (FPOR<2>) and in firmware by the RETEN bit (PWRCON<1>). RETVR must be programmed to zero (= 0) and the RETEN bit must be set (= 1) for the retention regulator to be enabled.

22.4.2 REGULATOR RETENTION MODE

When in Sleep mode, the device can use a separate low-power, low-voltage/retention regulator to power critical circuits. This regulator, which operates at 1V nominal, maintains power to data RAM, WDT, Timer1

22.5 Low-Power Brown-out Reset

The PIC32MM0064GPL036 family devices have a second low-power Brown-out Reset circuit with a reduced precision of the trip point. This low-power BOR circuit can be activated when the main BOR is disabled. The circuit is enabled by programming the LPBOREN Configuration bit (FPOR<3>) to '1'.

TABLE 22-3: PERIPHERAL MODULE DISABLE REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|--------|---------|-------|--------|--------|--------|------|------|--------|------|-------|--------|--------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2C00 | PMDCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | PMDLOCK | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 2C10 | PMD1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | HLVDMD | — | — | — | — | FFEF |
| | | 15:0 | — | — | — | VREFMD | — | — | — | — | — | — | — | — | — | — | — | ADCMD | EFFE |
| 2C20 | PMD2 | 31:16 | — | — | — | — | — | — | CLC2MD | CLC1MD | — | — | — | — | — | — | — | — | FCFF |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CMP2MD | CMP1MD | FFFC |
| 2C30 | PMD3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FFFF |
| | | 15:0 | — | — | — | — | — | — | CCP3MD | CCP2MD | CCP1MD | — | — | — | — | — | — | — | F8FF |
| 2C40 | PMD4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FFFF |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | T1MD | FFFE |
| 2C50 | PMD5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | r | r | FFFC |
| | | 15:0 | — | — | — | — | — | — | SPI2MD | SPI1MD | — | — | — | — | — | — | — | U2MD | U1MD |
| 2C60 | PMD6 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FFFF |
| | | 15:0 | — | — | — | — | — | — | — | REFOMD | — | — | — | — | — | — | — | — | RTCCMD |
| 2C70 | PMD7 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FFFF |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | CRCMD | — | — | FFF7 |

Legend: — = unimplemented, read as '1'; r = reserved bit, maintain as '1'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

PIC32MM0064GPL036 FAMILY

23.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 33. “Programming and Diagnostics”** (DS61129) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

23.1 Configuration Bits

PIC32MM0064GPL036 family devices contain a Boot Flash Memory (BFM) with an associated configuration space. All Configuration Words are listed in [Table 23-3](#) and [Table 23-4](#); [Register 23-1](#) through [Register 23-6](#) describe the configuration options.

23.2 Code Execution from RAM

PIC32MM0064GPL036 family devices allow executing the code from RAM. The starting boundary of this special RAM space can be adjusted using the EXECADDR<7:0> bits in the CFGCON register with a 1-Kbyte step. Writing a non-zero value to these bits will move the boundary, effectively reducing the total amount of program memory space in RAM. Refer to [Table 23-5](#) and [Register 23-7](#) for more information.

23.3 Device ID

The Device ID identifies the device used. The ID can be read from the DEVID register. The Device IDs for PIC32MM0064GPL036 family devices are listed in [Table 23-1](#). Also refer to [Table 23-5](#) and [Register 23-8](#) for more information.

TABLE 23-1: DEVICE IDs FOR PIC32MM0064GPL036 FAMILY DEVICES

| Device | DEVID |
|-------------------|------------|
| PIC32MM0016GPL020 | 0x06B04053 |
| PIC32MM0032GPL020 | 0x06B0C053 |
| PIC32MM0064GPL020 | 0x06B14053 |
| PIC32MM0016GPL028 | 0x06B02053 |
| PIC32MM0032GPL028 | 0x06B0A053 |
| PIC32MM0064GPL028 | 0x06B12053 |
| PIC32MM0016GPL036 | 0x06B06053 |
| PIC32MM0032GPL036 | 0x06B0E053 |
| PIC32MM0064GPL036 | 0x06B16053 |

23.4 System Registers Write Protection

The critical registers in the PIC32MM0064GPL036 family devices are protected (locked) from an accidental write. If the registers are locked, a special unlock sequence is required to modify the content of these registers.

To unlock the registers, the following steps should be done:

1. Disable interrupts prior to the system unlock sequence.
2. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the SYSKEY register, in two back-to-back assembly or 'C' instructions.
3. Write the new value to the required register.
4. Write a non-key value (such as 0x00000000) to the SYSKEY register to perform a lock.
5. Re-enable interrupts.

The registers that require this unlocking sequence are listed in [Table 23-2](#).

TABLE 23-2: SYSTEM LOCKED REGISTERS

| Register Name | Register Description | Peripheral |
|---------------|-------------------------------------|------------|
| OSCCON | Oscillator Control | Oscillator |
| SPLLCON | System PLL Control | Oscillator |
| OSCTUN | FRC Tuning | Oscillator |
| PMDCON | Peripheral Module Disable Control | PMD |
| RSWRST | Software Reset | Reset |
| RPCON | Peripheral Pin Select Configuration | I/O Ports |
| RNMICON | Non-Maskable Interrupt Control | Reset |
| PWRCON | Power Control | Reset |
| RTCCON1 | RTCC Control 1 | RTCC |

The SYSKEY register read value indicates the status. A value of '0' indicates the system registers are locked. A value of '1' indicates the system registers are unlocked. For more information about the SYSKEY register, refer to [Table 23-5](#) and [Register 23-9](#).

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23.5 Band Gap Voltage Reference

PIC32MM0064GPL036 family devices have a precision voltage reference band gap circuit used by many modules. The analog buffers are implemented between the band gap circuit and these modules. The buffers are automatically enabled by the hardware if some part of the device needs the band gap reference. The stabilization time is required when the buffer is switched on. The software can enable these buffers in advance to allow the band gap voltage to stabilize before the module uses it. The ANCFG register contains bits to enable the band gap buffers for the comparators (VBGCMP bit) and ADC (VBGADC bit). Refer to [Table 23-6](#) and [Register 23-10](#) for more information.

23.6 Programming and Diagnostics

PIC32MM0064GPL036 family devices provide a complete range of programming and diagnostic features:

- Simplified Field Programmability using Two-Wire In-Circuit Serial Programming™ (ICSP™) Interfaces
- Debugging using ICSP
- Programming and Debugging Capabilities using the EJTAG Extension of JTAG
- JTAG Boundary Scan Testing for Device and Board Diagnostics

23.7 Unique Device Identifier (UDID)

PIC32MM0064GPL036 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. The UDID cannot be erased by a bulk erase command or any other user accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 32-bit program words. When taken together, these fields form a unique 160-bit identifier.

The UDID is stored in five read-only locations, located from 0xBF41840 to 0xBF41854 in the device configuration space. [Table 23-7](#) lists the addresses of the Identifier Words.

23.8 Reserved Registers

PIC32MM0064GPL036 family devices have 3 reserved registers, located at 0xBF800400, 0xBF800480 and 0xBF802280. The application code must not modify these reserved locations. [Table 23-8](#) lists the addresses of these reserved registers.

23.9 Configuration Words and System Registers

TABLE 23-3: CONFIGURATION WORDS SUMMARY

| Virtual Address (BFC0_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | |
|-----------------------------|------------------|-----------|--------------|--------------|-------|-------------|-------|----------|--------------|--------|----------------|--------|------|-------------|----------|------------|--------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 |
| 17C0 | RESERVED | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 17C4 | FDEVOPT | 31:16 | USERID<15:0> | | | | | | | | | | | | | | | |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | SOSCHP | r-1 | r-1 |
| 17C8 | FICD | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | ICS<1:0> | | JTAGEN | r-1 |
| 17CC | FPOR | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | LPBOREN | RETVR | BOREN<1:0> |
| 17D0 | FWDT | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | FWDTEN | RCLKSEL<1:0> | | RWDTPS<4:0> | | | | WINDIS | FWDTWINSZ<1:0> | | | SWDTPS<4:0> | | | | |
| 17D4 | FOSCSSEL | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | FCKSM<1:0> | | r-1 | SOSCSSEL | r-1 | OSCIOfNC | POSCMOD<1:0> | | IESO | SOSCEN | r-1 | PLLSRC | r-1 | FNOSC<2:0> | | |
| 17D8 | FSEC | 31:16 | CP | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 17DC | RESERVED | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 17E0 | RESERVED | 31:16 | r-0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 17E4 | RESERVED | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

TABLE 23-4: ALTERNATE CONFIGURATION WORDS SUMMARY

| Virtual Address (BFC0_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | |
|-----------------------------|------------------|-----------|--------------|--------------|-------|-------|-------------|-------|----------|--------------|--------|----------------|--------|-------------|---------|--------|------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 |
| 1740 | RESERVED | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 1744 | AFDEVOPT | 31:16 | USERID<15:0> | | | | | | | | | | | | | | | |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | SOSCHP | r-1 | r-1 |
| 1748 | AFICD | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | ICS<1:0> | | JTAGEN | r-1 | r-1 |
| 174C | AFPOR | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | LPBOREN | RETVR | BOREN<1:0> | |
| 1750 | AFWDT | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | FWDTEN | RCLKSEL<1:0> | | | RWDTPS<4:0> | | | | WINDIS | FWDTWINSZ<1:0> | | SWDTPS<4:0> | | | | |
| 1754 | AFOSCSEL | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | FCKSM<1:0> | | | r-1 | SOSCSEL | r-1 | OSCIOFNC | POSCMOD<1:0> | | IESO | SOSCEN | r-1 | PLLSRC | r-1 | FNOSC<2:0> | |
| 1758 | AFSEC | 31:16 | CP | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 175C | RESERVED | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 1760 | RESERVED | 31:16 | r-0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 1764 | RESERVED | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

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REGISTER 23-1: FDEVOPT/AFDEVOPT: DEVICE OPTIONS CONFIGURATION REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | USERID<15:8> | | | | | | | |
| 23:16 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | USERID<7:0> | | | | | | | |
| 15:8 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 7:0 | r-1 | r-1 | r-1 | r-1 | R/P | r-1 | r-1 | r-1 |
| | — | — | — | — | SOSCHP | — | — | — |

| | | |
|-------------------|------------------|--|
| Legend: | r = Reserved bit | P = Programmable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-16 **USERID<15:0>**: User ID bits (2 bytes which can be programmed to any value)

bit 15-4 **Reserved**: Program as '1'

bit 3 **SOSCHP**: Secondary Oscillator (SOSC) High-Power Enable bit

1 = SOSC operates in Normal Power mode

0 = SOSC operates in High-Power mode

bit 2-0 **Reserved**: Program as '1'

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REGISTER 23-2: FICD/AFICD: ICD/DEBUG CONFIGURATION REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 15:8 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 7:0 | r-1 | r-1 | r-1 | R/P | R/P | R/P | r-1 | r-1 |
| | — | — | — | ICS<1:0> | | JTAGEN | — | — |

| | | |
|-------------------|------------------|------------------------------------|
| Legend: | r = Reserved bit | P = Programmable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 31-5 **Reserved:** Program as '1'
- bit 4-3 **ICS<1:0>:** ICE/ICD Communication Channel Selection bits
 - 11 = Communicates on PGEC1/PGED1
 - 10 = Communicates on PGEC2/PGED2
 - 01 = Communicates on PGEC3/PGED3
 - 00 = Not connected
- bit 2 **JTAGEN:** JTAG Enable bit
 - 1 = JTAG is enabled
 - 0 = JTAG is disabled
- bit 1-0 **Reserved:** Program as '1'

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REGISTER 23-3: FPOR/AFPOR: POWER-UP SETTINGS CONFIGURATION REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 15:8 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 7:0 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P | R/P |
| | — | — | — | — | LPBOREN | RETVR | BOREN<1:0> | |

| | | |
|-------------------|------------------|------------------------------------|
| Legend: | r = Reserved bit | P = Programmable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 31-4 **Reserved:** Program as '1'

bit 3 **LPBOREN:** Low-Power BOR Enable bit

1 = Low-Power BOR is enabled when the main BOR is disabled

0 = Low-Power BOR is disabled

bit 2 **RETVR:** Retention Voltage Regulator Enable bit

1 = Retention regulator is disabled

0 = Retention regulator is enabled and controlled by the RETEN bit during Sleep

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits

11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled

10 = Brown-out Reset is enabled only while device is active and is disabled in Sleep; SBOREN bit is disabled

01 = Brown-out Reset is controlled with the SBOREN bit setting

00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

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REGISTER 23-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | FWDTEN | RCLKSEL<1:0> | | RWDTPS<4:0> | | | | |
| 7:0 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | WINDIS | FWDTWINSZ<1:0> | | SWDTPS<4:0> | | | | |

| | | |
|-------------------|------------------|--|
| Legend: | r = Reserved bit | P = Programmable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-16 **Reserved:** Program as '1'

bit 15 **FWDTEN:** Watchdog Timer Enable bit

1 = WDT is enabled
0 = WDT is disabled

bit 14-13 **RCLKSEL<1:0>:** Run Mode Watchdog Timer Clock Source Selection bits

11 = Clock source is the LPRC oscillator (same as for Sleep mode)
10 = Clock source is the FRC oscillator
01 = Reserved
00 = Clock source is the system clock

bit 12-8 **RWDTPS<4:0>:** Run Mode Watchdog Timer Postscale Select bits

From 10100 to 11111 = 1:1048576.

10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

bit 7 **WINDIS:** Windowed Watchdog Timer Disable bit

1 = Windowed mode is disabled
0 = Windowed mode is enabled

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REGISTER 23-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER (CONTINUED)

bit 6-5 **FWDTWINSZ<1:0>**: Watchdog Timer Window Size bits

- 11 = Watchdog Timer window size is 25%
- 10 = Watchdog Timer window size is 37.5%
- 01 = Watchdog Timer window size is 50%
- 00 = Watchdog Timer window size is 75%

bit 4-0 **SWDTPS<4:0>**: Sleep Mode Watchdog Timer Postscale Select bits

From 10100 to 11111 = 1:1048576.

- 10011 = 1:524288
- 10010 = 1:262144
- 10001 = 1:131072
- 10000 = 1:65536
- 01111 = 1:32768
- 01110 = 1:16384
- 01101 = 1:8192
- 01100 = 1:4096
- 01011 = 1:2048
- 01010 = 1:1024
- 01001 = 1:512
- 01000 = 1:256
- 00111 = 1:128
- 00110 = 1:64
- 00101 = 1:32
- 00100 = 1:16
- 00011 = 1:8
- 00010 = 1:4
- 00001 = 1:2
- 00000 = 1:1

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REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — |
| 23:16 | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — |
| 15:8 | R/P | R/P | r-1 | R/P | r-1 | R/P | R/P | R/P |
| | FCKSM<1:0> | | — | SOSCSEL | — | OSCIOFNC | POSCMOD<1:0> | |
| 7:0 | R/P | R/P | r-1 | R/P | r-1 | R/P | R/P | R/P |
| | IESO | SOSCEN | — | PLLSRC | — | FNOSC<2:0> | | |

| | | |
|-------------------|------------------|--|
| Legend: | r = Reserved bit | P = Programmable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-16 **Reserved:** Program as '1'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Enable bits

- 11 = Clock switching is enabled; Fail-Safe Clock Monitor is enabled
- 10 = Clock switching is disabled; Fail-Safe Clock Monitor is enabled
- 01 = Clock switching is enabled; Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is disabled; Fail-Safe Clock Monitor is disabled

bit 13 **Reserved:** Program as '1'

bit 12 **SOSCSEL:** Secondary Oscillator (SOSC) External Clock Enable bit

- 1 = Crystal is used (RA4 and RB4 pins are controlled by SOSC)
- 0 = External clock is connected to the SOSCO pin (RA4 and RB4 pins are controlled by I/O PORTx registers)

bit 11 **Reserved:** Program as '1'

bit 10 **OSCIOFNC:** System Clock on CLKO Pin Enable bit

- 1 = OSC2/CLKO pin operates as normal I/O
- 0 = System clock is connected to the OSC2/CLKO pin

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator (POSC) Mode Selection bits

- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock (EC) mode is selected

bit 7 **IESO:** Two-Speed Start-up Enable bit

- 1 = Two-Speed Start-up is enabled
- 0 = Two-Speed Start-up is disabled

bit 6 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit

- 1 = Secondary Oscillator is enabled
- 0 = Secondary Oscillator is disabled

bit 5 **Reserved:** Program as '1'

bit 4 **PLLSRC:** System PLL Input Clock Selection bit

- 1 = FRC oscillator is selected as the PLL reference input on a device Reset
- 0 = Primary Oscillator (POSC) is selected as the PLL reference input on a device Reset

bit 3 **Reserved:** Program as '1'

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REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER (CONTINUED)

bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits
 110 and 111 = Reserved (selects Fast RC (FRC) Oscillator with Divide-by-N)
 101 = Low-Power RC Oscillator (LPRC)
 100 = Secondary Oscillator (SOSC)
 011 = Reserved
 010 = Primary Oscillator (XT, HS, EC)
 001 = Primary or FRC Oscillator with PLL
 000 = Fast RC (FRC) Oscillator with Divide-by-N

REGISTER 23-6: FSEC/AFSEC: CODE-PROTECT CONFIGURATION REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/P | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | CP | — | — | — | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 15:8 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 7:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |

| | | |
|-------------------|------------------|--|
| Legend: | r = Reserved bit | P = Programmable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31 **CP**: Code Protection Enable bit
 1 = Code protection is disabled
 0 = Code protection is enabled

bit 30-0 **Reserved**: Program as '1'

TABLE 23-5: RAM CONFIGURATION, DEVICE ID AND SYSTEM LOCK REGISTERS MAP

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets ⁽¹⁾ |
|--------------------------|---------------|-----------|--------------|-------|-------|-------|-------|-----------|------|------|---------------|------|------|------|--------|------|------|---------------------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | |
| 3B00 | CFGCON | 31:16 | — | — | — | — | — | — | — | — | EXECADDR<7:0> | | | | | | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | JTAGEN | — | — | — |
| 3B20 | DEVID | 31:16 | VER<3:0> | | | | | ID<27:16> | | | | | | | | | | xxxxx |
| | | 15:0 | ID<15:0> | | | | | | | | | | | | | | | xxxxx |
| 3B30 | SYSKEY | 31:16 | SYSKEY<31:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | SYSKEY<31:0> | | | | | | | | | | | | | | | 0001 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

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REGISTER 23-7: CFGCON: CONFIGURATION CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | r-0 | U-0 | r-0 | r-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EXECADDR<7:0> | | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-y | U-0 | r-1 | r-1 |
| | — | — | — | — | JTAGEN | — | — | — |

| | | |
|-------------------|------------------|--|
| Legend: | r = Reserved bit | y = Value set from Configuration bits on Reset |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **Reserved:** Must be written as '0'

bit 26 **Unimplemented:** Read as '0'

bit 25-24 **Reserved:** Must be written as '0'

bit 23-16 **EXECADDR<7:0>:** RAM Program Space Start Address bits

11111111 = RAM program space starts at the 255-Kbyte boundary (from 0xA003FC00)

•
•
•

00000010 = RAM program space starts at the 2-Kbyte boundary (from 0xA0000800)

00000001 = RAM program space starts at the 1-Kbyte boundary (from 0xA0000400)

00000000 = All data RAM is allocated to program space (from 0xA0000000)

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Enable bit

1 = JTAG port is enabled

0 = JTAG port is disabled

The Reset value of this bit is the value of the JTAGEN (FICD<2>) Configuration bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Must be written as '1'

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REGISTER 23-8: DEVID: DEVICE ID REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|--------------------------|----------------|----------------|----------------|--------------------------|----------------|---------------|---------------|
| 31:24 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | VER<3:0> ⁽¹⁾ | | | | ID<27:24> ⁽¹⁾ | | | |
| 23:16 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | ID<23:16> ⁽¹⁾ | | | | | | | |
| 15:8 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | ID<15:8> ⁽¹⁾ | | | | | | | |
| 7:0 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | ID<7:0> ⁽¹⁾ | | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **VER<3:0>**: Revision Identifier bits⁽¹⁾

bit 27-0 **DEVID<27:0>**: Device ID bits⁽¹⁾

Note 1: Reset values are dependent on the device variant.

REGISTER 23-9: SYSKEY: SYSTEM UNLOCK REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | SYSKEY<31:24> | | | | | | | |
| 23:16 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | SYSKEY<23:16> | | | | | | | |
| 15:8 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | SYSKEY<15:8> | | | | | | | |
| 7:0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | SYSKEY<7:0> | | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **SYSKEY<31:0>**: Unlock and Lock Key bits

TABLE 23-6: BAND GAP REGISTER MAP

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets | |
|-----------------------------|----------------------|-----------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|--------|------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | | 16/0 |
| 2300 | ANCFG ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VBGADC | VBGCMP | — |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 23-10: ANCFG: BAND GAP CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HS, HC | R/W-0, HS, HC | U-0 |
| | — | — | — | — | — | VBGADC | VBGCMP | — |

| | | |
|-------------------|-----------------------------|--|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 31-3 **Unimplemented:** Read as '0'
- bit 2 **VBGADC:** ADC Band Gap Enable bit
 - 1 = ADC band gap is enabled
 - 0 = ADC band gap is disabled
- bit 1 **VBGCMP:** Comparator Band Gap Enable bit
 - 1 = Comparator band gap is enabled
 - 0 = Comparator band gap is disabled
- bit 0 **Unimplemented:** Read as '0'

TABLE 23-7: UNIQUE DEVICE IDENTIFIER (UDID) REGISTER MAP

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | All Resets |
|--------------------------|---------------|-----------|-------------------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | |
| 1840 | UDID1 | 31:16 | UDID Word 1<31:0> | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | xxxx |
| 1844 | UDID2 | 31:16 | UDID Word 2<31:0> | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | xxxx |
| 1848 | UDID3 | 31:16 | UDID Word 3<31:0> | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | xxxx |
| 184C | UDID4 | 31:16 | UDID Word 4<31:0> | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | xxxx |
| 1850 | UDID5 | 31:16 | UDID Word 5<31:0> | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | xxxx |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 23-8: RESERVED REGISTERS MAP

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | All Resets |
|--------------------------|---------------|-----------|---------------------------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | |
| 0400 | RESERVED1 | 31:16 | Reserved Register 1<31:0> | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | 0000 |
| 0480 | RESERVED2 | 31:16 | Reserved Register 2<31:0> | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | 0000 |
| 2280 | RESERVED3 | 31:16 | Reserved Register 3<31:0> | | | | | | | | | | | | | | 0C00 |
| | | 15:0 | | | | | | | | | | | | | | | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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NOTES:

24.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers (MCU) and dsPIC[®] digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB[®] X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/
MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for
Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE[™] In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICKit[™] 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
Evaluation Kits and Starter Kits
- Third-party development tools

24.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows[®], Linux and Mac OS[®] X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

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24.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

24.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

24.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

24.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

24.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

24.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

24.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

24.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

24.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

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24.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

24.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

25.0 INSTRUCTION SET

The PIC32MM0064GPL036 family instruction set complies with the MIPS® Release 3 instruction set architecture. Only microMIPS32™ instructions are supported. The PIC32MM0064GPL036 family does not have the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to the “MIPS® Architecture for Programmers Volume II-B: The microMIPS32™ Instruction Set” at www.imgtec.com for more information.

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NOTES:

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26.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MM0064GPL036 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MM0064GPL036 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings^(†)

| | |
|--|-----------------------|
| Ambient temperature under bias | -40°C to +125°C |
| Storage temperature | -65°C to +150°C |
| Voltage on VDD with respect to VSS | -0.3V to +4.0V |
| Voltage on any general purpose digital or analog pin (not 5.5V tolerant) with respect to VSS | -0.3V to (VDD + 0.3V) |
| Voltage on any general purpose digital or analog pin (5.5V tolerant) with respect to VSS: | |
| When VDD = 0V: | -0.3V to +4.0V |
| When VDD ≥ 2.0V: | -0.3V to +6.0V |
| Voltage on AVDD with respect to VSS | VDD |
| Voltage on AVSS with respect to VSS | VSS |
| Maximum current out of VSS pin | 100 mA |
| Maximum current into VDD pin ⁽¹⁾ | 300 mA |
| Maximum output current sunk by I/O pin | 11 mA |
| Maximum output current sourced by I/O pin | 16 mA |
| Maximum output current sunk by I/O pin with increased current drive strength (RA3, RB8, RB9 and RB15) | 17 mA |
| Maximum output current sourced by I/O pin with increased current drive strength (RA3, RB8, RB9 and RB15) | 24 mA |
| Maximum current sunk by all ports | 300 mA |
| Maximum current sourced by all ports ⁽¹⁾ | 300 mA |

Note 1: Maximum allowable current is a function of device maximum power dissipation (see [Table 26-1](#)).

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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26.1 DC Characteristics

FIGURE 26-1: PIC32MM0064GPL036 FAMILY VOLTAGE-FREQUENCY GRAPH

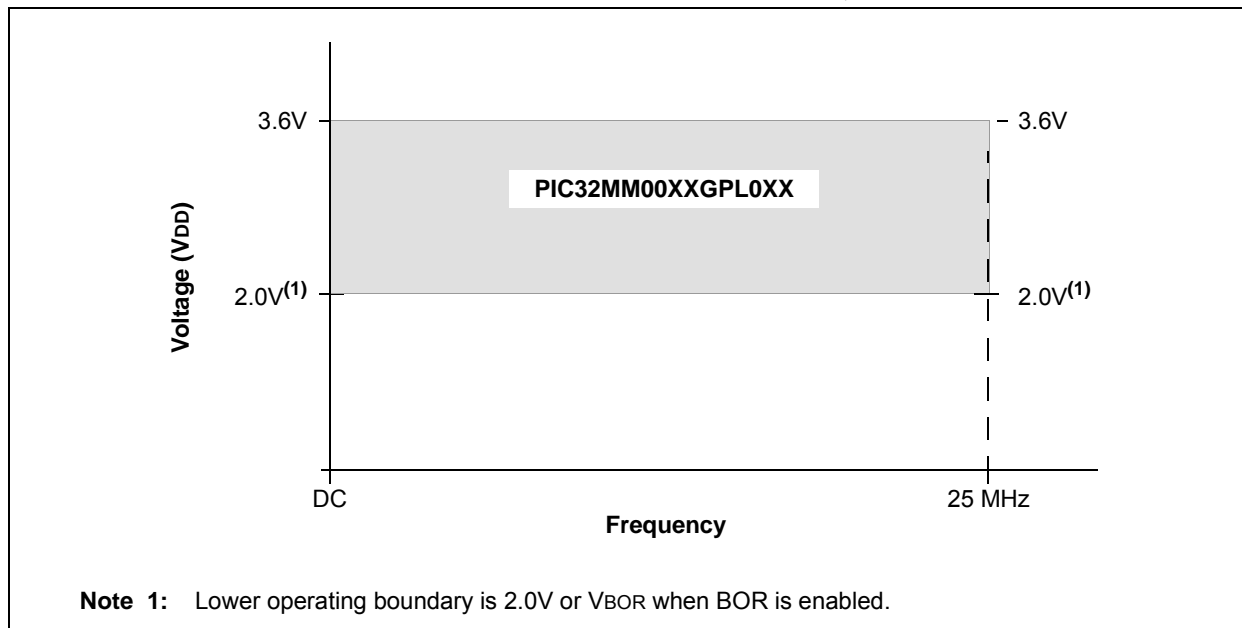


TABLE 26-1: THERMAL OPERATING CONDITIONS

| Rating | Symbol | Min | Typ | Max | Unit |
|--|-------------------|-------------------------------------|-----|------|-------------------|
| PIC32MM00XXGPL0XX: Operating Junction Temperature Range | TJ | -40 | — | +100 | °C ⁽¹⁾ |
| | TJ | -40 | — | +140 | °C ⁽²⁾ |
| PIC32MM00XXGPL0XX: Operating Ambient Temperature Range | TA | -40 | — | +85 | °C ⁽¹⁾ |
| | TA | -40 | — | +125 | °C ⁽²⁾ |
| Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$ | PD | P _{INT} + P _{I/O} | | | W |
| Maximum Allowed Power Dissipation | PD _{MAX} | $(T_J - T_A) / \theta_{JA}$ | | | W |

Note 1: 85°C rated parts.

Note 2: 125°C rated parts.

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TABLE 26-2: PACKAGE THERMAL RESISTANCE⁽¹⁾

| Package | Symbol | Typ | Unit |
|--------------|---------------|------|------|
| 20-Pin SSOP | θ_{JA} | 87.3 | °C/W |
| 20-Pin QFN | θ_{JA} | 43.0 | °C/W |
| 28-Pin SPDIP | θ_{JA} | 60.0 | °C/W |
| 28-Pin SSOP | θ_{JA} | 71.0 | °C/W |
| 28-Pin SOIC | θ_{JA} | 69.7 | °C/W |
| 28-Pin UQFN | θ_{JA} | 27.5 | °C/W |
| 28-Pin QFN | θ_{JA} | 20.0 | °C/W |
| 36-Pin VQFN | θ_{JA} | 31.1 | °C/W |
| 40-Pin UQFN | θ_{JA} | 41.0 | °C/W |

Note 1: Junction to ambient thermal resistance; Theta-JA (θ_{JA}) numbers are achieved by package simulations.

TABLE 26-3: OPERATING VOLTAGE SPECIFICATIONS

| Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +125°C (unless otherwise stated) | | | | | | |
|--|---------------------|---|------|------|-------|-------------------------------------|
| Param No. | Symbol | Characteristic | Min | Max | Units | Conditions |
| DC10 | VDD | Supply Voltage | 2.0 | 3.6 | V | BOR disabled |
| | | | VBOR | 3.6 | V | BOR enabled |
| DC16 | VPOR ⁽¹⁾ | VDD Start Voltage to Ensure Internal Power-on Reset Signal | VSS | — | V | |
| DC17A | SVDD ⁽¹⁾ | VDD Rise Rate to Ensure Internal Power-on Reset Signal | 0.05 | — | V/ms | 0-3.3V in 66 ms, 0-2.0V in 40 ms |
| DC17B | VBOR | Brown-out Reset Voltage on VDD Transition, High-to-Low | 1.94 | 2.22 | V | |

Note 1: If the VPOR or SVDD parameters are not met, or the application experiences slow power-down VDD ramp rates, it is recommended to enable and use BOR.

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TABLE 26-4: OPERATING CURRENT (IDD)⁽²⁾

| Operating Conditions: -40°C < TA < +85°C (unless otherwise stated) | | | | | |
|--|------------------------|------|-------|------|-----------------------|
| Parameter No. | Typical ⁽¹⁾ | Max | Units | VDD | Conditions |
| DC19 | 0.45 | 0.65 | mA | 2.0V | FSYS = 1 MHz |
| | 0.45 | 0.65 | mA | 3.3V | |
| DC23 | 2.5 | 3.5 | mA | 2.0V | FSYS = 8 MHz |
| | 2.5 | 3.5 | mA | 3.3V | |
| DC24 | 7.0 | 9.2 | mA | 2.0V | FSYS = 25 MHz |
| | 7.0 | 9.2 | mA | 3.3V | |
| DC25A | 0.26 | 0.35 | mA | 2.0V | FSYS = 32 kHz |
| | 0.26 | 0.35 | mA | 3.3V | |
| DS25B | 0.70 | 0.90 | mA | 3.3V | FSYS = 32 kHz, +125°C |

Note 1: Data in the “Typical” column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IDD current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 010 and POSCMOD<1:0> (FOSCSEL<9:8>) = 00)
- OSC1 pin is driven with external square wave with levels from 0.3V to VDD – 0.3V
- OSC2 is configured as an I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins (except OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- NOP instructions are executed

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TABLE 26-5: IDLE CURRENT (I_{IDLE})⁽²⁾

| Operating Conditions: -40°C < T _A < +85°C (unless otherwise stated) | | | | | |
|--|------------------------|------|-------|-----------------|-----------------------------------|
| Parameter No. | Typical ⁽¹⁾ | Max | Units | V _{DD} | Conditions |
| DC40A | 0.26 | 0.46 | mA | 2.0V | F _{SYS} = 1 MHz |
| | 0.26 | 0.46 | mA | 3.3V | |
| DC41A | 0.85 | 1.5 | mA | 2.0V | F _{SYS} = 8 MHz |
| | 0.85 | 1.5 | mA | 3.3V | |
| DC42A | 2.3 | 3.7 | mA | 2.0V | F _{SYS} = 25 MHz |
| | 2.3 | 3.7 | mA | 3.3V | |
| DC44A | 0.18 | 0.34 | mA | 2.0V | F _{SYS} = 32 kHz |
| | 0.18 | 0.34 | mA | 3.3V | |
| DC40B | 0.6 | 1 | mA | 2.0V | F _{SYS} = 1 MHz, +125°C |
| | 0.6 | 1 | mA | 3.3V | |
| DC41B | 1.4 | 2.1 | mA | 2.0V | F _{SYS} = 8 MHz, +125°C |
| | 1.4 | 2.1 | mA | 3.3V | |
| DC42B | 2.9 | 4.3 | mA | 2.0V | F _{SYS} = 25 MHz, +125°C |
| | 2.9 | 4.3 | mA | 3.3V | |
| DC44B | 0.4 | 0.64 | mA | 2.0V | F _{SYS} = 32 kHz, +125°C |
| | 0.4 | 0.64 | mA | 3.3V | |

Note 1: Data in the “Typical” column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{IDLE} current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 010 and POSCMOD<1:0> (FOSCSEL<9:8>) = 00)
- OSC1 pin is driven with external square wave with levels from 0.3V to V_{DD} – 0.3V
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins (excepting OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

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TABLE 26-6: POWER-DOWN CURRENT (IPD)⁽²⁾

| Parameter No. | Typical ⁽¹⁾ | Max | Units | Operating Temperature | VDD | Conditions |
|---------------|------------------------|------|--------|-----------------------|------|--|
| DC60 | 134 | 198 | μA | -40°C | 2.0V | Sleep with active main voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) = 0) |
| | 136 | 208 | μA | +25°C | | |
| | 141 | 217 | μA | +85°C | | |
| | 350 | 640 | μA | +125°C | | |
| | 139 | 209 | μA | -40°C | 3.3V | |
| | 141 | 217 | μA | +25°C | | |
| | 143 | 231 | μA | +85°C | | |
| | 400 | 650 | μA | +125°C | | |
| DC61 | 4.3 | 11.7 | μA | -40°C | 2.0V | Sleep with main voltage regulator in Standby mode (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 0) |
| | 5.1 | 15.6 | μA | +25°C | | |
| | 35 | 55 | μA | +85°C | | |
| | 40 | 90 | μA | +125°C | | |
| | 6.1 | 16.8 | μA | -40°C | 3.3V | |
| | 6.9 | 20.1 | μA | +25°C | | |
| | 12.7 | 36.0 | μA | +85°C | | |
| | 60 | 100 | μA | +125°C | | |
| DC62 | 2.3 | — | μA | -40°C | 2.0V | Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0) |
| | 2.7 | — | μA | +25°C | | |
| | 5.2 | — | μA | +85°C | | |
| | 2.3 | — | μA | -40°C | 3.3V | |
| | 2.7 | — | μA | +25°C | | |
| | 5.4 | — | μA | +85°C | | |
| 10.1 | — | μA | +125°C | | | |
| DC63 | 0.28 | — | μA | -40°C | 2.0V | Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0) |
| | 0.44 | — | μA | +25°C | | |
| | 2.52 | — | μA | +85°C | | |
| | 0.29 | — | μA | -40°C | 3.3V | |
| | 0.44 | — | μA | +25°C | | |
| | 2.62 | — | μA | +85°C | | |
| | 10.1 | — | μA | +125°C | | |

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IPD is measured with:

- Oscillator is configured in FRC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 000)
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

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TABLE 26-7: INCREMENTAL PERIPHERAL Δ CURRENT⁽²⁾

| Operating Conditions: 2.0V < V _{DD} < 3.6V, -40°C < T _A < +85°C (unless otherwise stated) | | | |
|---|--------------------|---------|------------------------------------|
| Parameter No. | Typ ⁽¹⁾ | Units | Conditions |
| Brown-out Reset Incremental Current (ΔBOR) | | | |
| DC71A | 2.7 | μ A | |
| DC71B | 3.4 | μ A | +125°C |
| Watchdog Timer Incremental Current (ΔWDT) | | | |
| DC72A | 80 | nA | with LPRC |
| DC72B | 140 | nA | +125°C with LPRC |
| High/Low-Voltage Detect Incremental Current (ΔHLVD) | | | |
| DC73 | 2.1 | μ A | |
| Real-Time Clock and Calendar Incremental Current (ΔRTCC) | | | |
| DC74A | 1.0 | μ A | with SOSC |
| DC74B | 2.0 | μ A | +125°C with SOSC |
| DC75A | 0.4 | μ A | with LPRC |
| DC75B | 0.65 | μ A | +125°C with LPRC |
| ADC Incremental Current (ΔADC) | | | |
| DC76A | 450 | μ A | 12-bit, 100 ksps, with FRC |
| DC76B | 590 | μ A | +125°C, 12-bit, 100 ksps, with FRC |
| FRC Oscillator Incremental Current (ΔFRC) | | | |
| DC78A | 305 | μ A | |
| DC78B | 350 | μ A | +125°C |
| PLL Incremental Current (ΔPLL) | | | |
| DC79A | 1230 | μ A | Fvco = 24 MHz |
| DC79B | 1550 | μ A | Fvco = 24MHz +125°C |
| DC80A | 1550 | μ A | Fvco = 48 MHz |
| DC80B | 1850 | μ A | Fvco = 48MHz +125°C |
| Digital-to-Analog Converter Incremental Current, CDAC (ΔDAC) | | | |
| DC81A | 27.5 | μ A | |
| DC81B | 40.0 | μ A | +125°C |
| Low-Power BOR Incremental Current (ΔLPBOR) | | | |
| DC82A | 200 | nA | |
| DC82B | 420 | nA | +125°C |
| Comparator Incremental Current (ΔCMP) | | | |
| DC83A | 24.0 | μ A | |
| DC83B | 38.0 | μ A | +125°C |

Note 1: Data in the "Typ" column is for design guidance only and is not tested.

2: The Δ current is an additional current consumed when the module is enabled. This current should be added to the base IPD current.

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TABLE 26-8: I/O PIN INPUT SPECIFICATIONS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | | |
|---|-----------------|--|---------------------|--------------------|---------------------|-------|---|
| Param No. | Symbol | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| DI10 DI15 DI16 DI17 | V _{IL} | Input Low Voltage⁽²⁾ | | | | | |
| | | I/O Pins with ST Buffer | V _{SS} | — | 0.2 V _{DD} | V | |
| | | \overline{MCLR} | V _{SS} | — | 0.2 V _{DD} | V | |
| | | OSC1/CLKI (XT mode) | V _{SS} | — | 0.2 V _{DD} | V | |
| DI17 | | OSC1/CLKI (HS mode) | V _{SS} | — | 0.2 V _{DD} | V | |
| DI20 DI25 DI26 DI27 | V _{IH} | Input High Voltage⁽²⁾ | | | | | |
| | | I/O Pins with ST Buffer: without 5V Tolerance | 0.8 V _{DD} | — | V _{DD} | V | |
| | | with 5V Tolerance | 0.8 V _{DD} | — | 5.5 | V | |
| | | \overline{MCLR} | 0.8 V _{DD} | — | V _{DD} | V | |
| | | OSCI/CLKI (XT mode) | 0.7 V _{DD} | — | V _{DD} | V | |
| DI27 | | OSC1/CLKI (HS mode) | 0.7 V _{DD} | — | V _{DD} | V | |
| DI30 | ICNPU | CNPUx Pull-up Current | — | 350 | — | μA | V _{PIN} = 0V, V _{DD} = 3.3V |
| DI30A | ICNPD | CNPDx Pull-Down Current | — | 300 | — | μA | V _{PIN} = 3.3V, V _{DD} = 3.3V |
| DI50 DI51 DI55 DI56 | I _{IL} | Input Leakage Current | | | | | |
| | | I/O Pins – 5V Tolerant | — | 0.1 | 1.0 | μA | V _{PIN} = 3.3V, V _{DD} = 3.3V, pin at high-impedance |
| | | I/O Pins – Not 5V Tolerant | — | 0.1 | 1.0 | μA | V _{PIN} = 3.3V, V _{DD} = 3.3V, pin at high-impedance |
| | | \overline{MCLR} | — | 0.1 | 1.0 | μA | V _{PIN} = 3.3V, V _{DD} = 3.3V |
| DI56 | | OSC1/CLKI | — | 0.1 | 1.0 | μA | V _{PIN} = 3.3V, V _{DD} = 3.3V |

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Refer to [Table 1-1](#) for I/O pin buffer types.

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TABLE 26-9: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | |
|---|------------------|--|--------------------|-----------------------|-------|---|
| Param. No. | Symbol | Characteristics | Min. | Max. | Units | Conditions |
| DI60a | I _{ICL} | Input Low Injection Current | 0 | -5 ^(1,4) | mA | This parameter applies to all pins, except V _{DD} , V _{SS} , MCLR and V _{CAP} . |
| DI60b | I _{ICH} | Input High Injection Current | 0 | +5 ^(2,3,4) | mA | This parameter applies to all pins, except V _{DD} , V _{SS} , MCLR, V _{CAP} and all 5V tolerant pins. |
| | | | 0 | +0 ^(2,3,4) | mA | 5V tolerant pins. |
| DI60c | ΣI_{ICT} | Total Input Injection Current (sum of all I/O and control pins) | -20 ⁽⁵⁾ | +20 ⁽⁵⁾ | mA | Absolute instantaneous sum of all \pm input injection currents from all I/O pins, ($ I_{ICL} + I_{ICH} $) $\leq \Sigma I_{ICT}$ |

- Note 1:** V_{IL} Source < (V_{SS} – 0.3). Characterized but not tested.
- Note 2:** V_{IH} Source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- Note 3:** Digital 5V tolerant pins do not have an internal high-side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- Note 4:** Injection currents can affect the ADC results.
- Note 5:** Any number and/or combination of I/O pins, not excluded under I_{ICL} or I_{ICH} conditions, are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit.

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TABLE 26-10: I/O PIN OUTPUT SPECIFICATIONS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | |
|---|--------|----------------------------------|------|------|-------|---------------------------|
| Param No. | Symbol | Characteristic | Min | Max | Units | Conditions |
| DO10 DO16 | VOL | Output Low Voltage | | | | |
| | | I/O Ports | — | 0.36 | V | IOL = 6.0 mA, VDD = 3.6V |
| | | | — | 0.21 | V | IOL = 3.0 mA, VDD = 2V |
| | | RA3, RB8, RB9 and RB15 I/O Ports | — | 0.16 | V | IOL = 6.0 mA, VDD = 3.6V |
| | | | — | 0.12 | V | IOL = 3.0 mA, VDD = 2V |
| DO20 DO26 | VOH | Output High Voltage | | | | |
| | | I/O Ports | 3.25 | — | V | IOH = -6.0 mA, VDD = 3.6V |
| | | | 1.4 | — | V | IOH = -3.0 mA, VDD = 2V |
| | | RA3, RB8, RB9 and RB15 I/O Ports | 3.3 | — | V | IOH = -6.0 mA, VDD = 3.6V |
| | | | 1.55 | — | V | IOH = -3.0 mA, VDD = 2V |

TABLE 26-11: PROGRAM FLASH MEMORY SPECIFICATIONS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | | |
|---|--------|--|-------|--------------------|------|-------|---|
| Param No. | Symbol | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| D130 | EP | Cell Endurance | 10000 | 20000 | — | E/W | |
| D131 | VICSP | VDD for In-Circuit Serial Programming™ (ICSP™) | VBOR | — | 3.6 | V | |
| D132 | VRTSP | VDD for Run-Time Self-Programming (RTSP) | 2.0 | — | 3.6 | V | |
| D133 | TIW | Self-Timed Double-Word Write Cycle Time | 19.7 | 21.0 | 22.3 | μs | 8 bytes, data is not all '1's |
| | | Self-Timed Row Write Cycle Time | 1.3 | 1.4 | 1.5 | ms | 256 bytes, data is not all '1's, SYSCLK > 2 MHz |
| D133 | TIE | Self-Timed Page Erase Time | 15.0 | 16.0 | 17.0 | ms | 2048 bytes |
| D134 | TRETD | Characteristic Retention | 20 | — | — | Year | If no other specifications are violated |
| D136 | TCE | Self-Timed Chip Erase Time | 16.0 | 17.0 | 18.0 | ms | |

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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TABLE 26-12: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | | |
|---|--------|--------------------------------------|-------|--------------------|-------|---------|---|
| Param No. | Symbol | Characteristics | Min | Typ ⁽¹⁾ | Max | Units | Comments |
| DVR10 | VBG | Band Gap Reference Voltage | 1.163 | 1.2 | 1.237 | V | |
| DVR20 | VRGOUT | Regulator Output Voltage | — | 1.8 | — | V | $V_{DD} > 1.9V$ |
| DVR21 | CEFC | External Filter Capacitor Value | 4.7 | 10 | — | μF | Series Resistance $< 3\Omega$ recommended; $< 5\Omega$ required |
| DVR30 | VLVR | Low-Voltage Regulator Output Voltage | 0.9 | — | 1.2 | V | RETEN = 1, RETVR (FPOR<2>) = 0 |

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 26-13: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | | |
|---|----------------------|--------------------------------------|-------------------|------|--------------------|------|-------|
| Param No. | Symbol | Characteristic | | Min | Typ ⁽²⁾ | Max | Units |
| DC18 | VHLVD ⁽¹⁾ | HLVD Voltage on VDD Transition | HLVDL<3:0> = 0110 | 2.95 | — | 3.45 | V |
| | | | HLVDL<3:0> = 0111 | 2.75 | — | 3.13 | V |
| | | | HLVDL<3:0> = 1000 | 2.65 | — | 3.01 | V |
| | | | HLVDL<3:0> = 1001 | 2.45 | — | 2.83 | V |
| | | | HLVDL<3:0> = 1010 | 2.35 | — | 2.72 | V |
| | | | HLVDL<3:0> = 1011 | 2.25 | — | 2.57 | V |
| | | | HLVDL<3:0> = 1100 | 2.15 | — | 2.46 | V |
| | | | HLVDL<3:0> = 1101 | 2.08 | — | 2.35 | V |
| | | | HLVDL<3:0> = 1110 | 2.00 | — | 2.24 | V |
| DC101 | VTHL | HLVD Voltage on LVDIN Pin Transition | HLVDL<3:0> = 1111 | — | 1.2 | — | V |

Note 1: Trip points for values of HLVD<3:0>, from ‘0000’ to ‘0101’, are not implemented.

2: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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TABLE 26-14: COMPARATOR SPECIFICATIONS

| Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +125°C (unless otherwise stated) | | | | | | |
|--|----------------------|---------------------------|-----|--------------------|-----|------------------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽²⁾ | Max | Units |
| D300 | VIOFF | Input Offset Voltage | -60 | 12 | 60 | mV |
| D301 | VICM | Input Common-Mode Voltage | 0 | — | VDD | V ⁽¹⁾ |
| D307 | TRESP ⁽¹⁾ | Response Time | — | 150 | — | ns |

Note 1: Measured with one input at VDD/2 and the other transitioning from VSS to VDD.

Note 2: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 26-15: VOLTAGE REFERENCE (CDAC) SPECIFICATIONS

| Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +125°C (unless otherwise stated) | | | | | | |
|--|--------|------------------------------|-----|--------------------|-----|-------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽²⁾ | Max | Units |
| VRD310 | TSET | Settling Time ⁽¹⁾ | — | — | 10 | μs |
| VRD311 | VRA | Accuracy | -1 | — | 1 | LSb |
| VRD312 | VRUR | Unit Resistor Value (R) | — | 4.5 | — | kΩ |

Note 1: Measures the interval while VRDAT<4:0> transitions from '11111' to '00000'.

Note 2: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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26.2 AC Characteristics and Timing Parameters

FIGURE 26-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

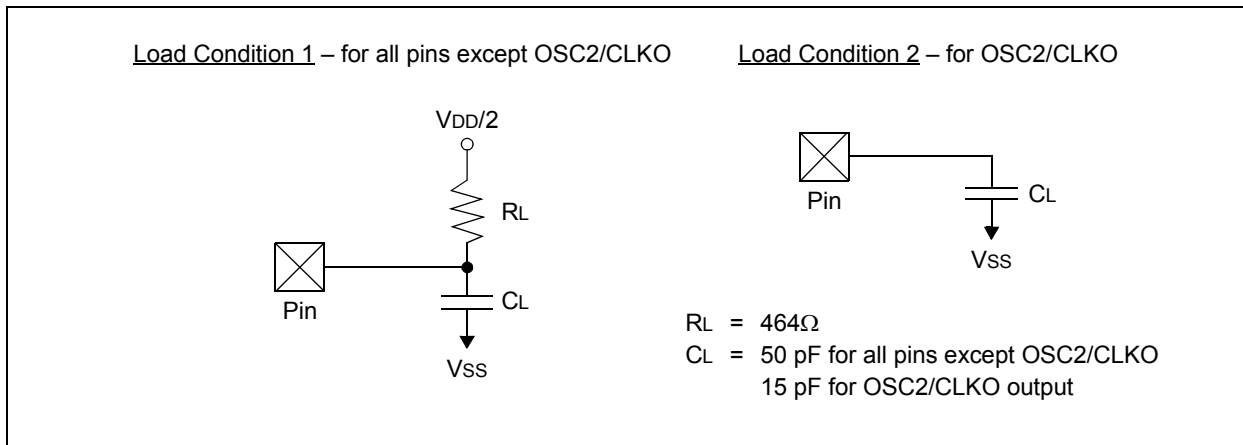


TABLE 26-16: CAPACITIVE LOADING CONDITIONS ON OUTPUT PINS

| Param No. | Symbol | Characteristic | Min | Max | Units | Conditions |
|-----------|--------|-----------------------|-----|-----|-------|---|
| DO50 | Cosco | OSC2/CLKO Pin | — | 15 | pF | In XT and HS modes when external clock is used to drive OSC1/CLKI |
| DO56 | Cio | All I/O Pins and OSC2 | — | 50 | pF | EC mode |

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FIGURE 26-3: EXTERNAL CLOCK TIMING

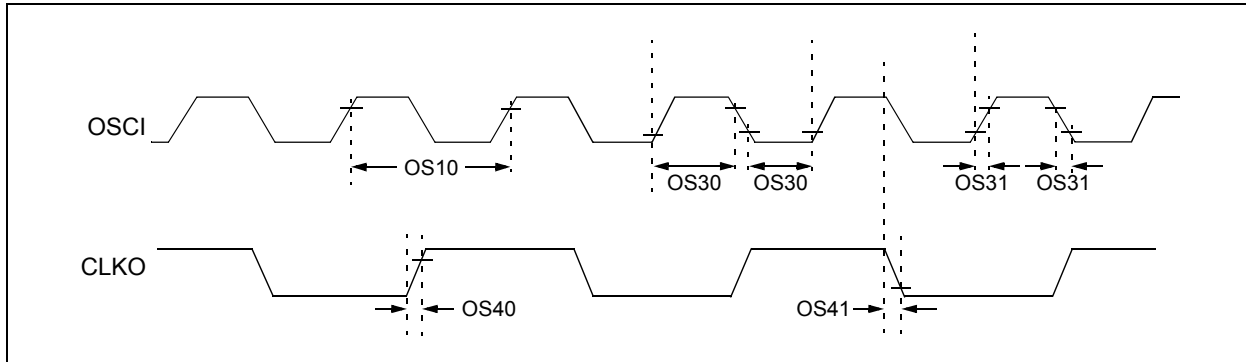


TABLE 26-17: EXTERNAL CLOCK TIMING REQUIREMENTS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | | |
|---|---------------|---|-----------------------|--------------------|-----------------------|----------------------|----------------------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| OS10 | Fosc | External CLKI Frequency | DC | — | 25 | MHz | EC |
| | | | 2 | — | 12.5 | MHz | ECPLL ⁽²⁾ |
| | | Oscillator Frequency | 3.5 | — | 10 | MHz | XT |
| | | | 3.5 | — | 10 | MHz | XTPLL ⁽²⁾ |
| | | | 10 | — | 25 | MHz | HS |
| | | 10 | — | 25 | MHz | HSPLL ⁽²⁾ | |
| | | 31 | — | 50 | kHz | SOSC | |
| OS30 | TosL, TosH | External Clock in (OSC1) High or Low Time | $0.45 \times T_{osc}$ | — | $0.55 \times T_{osc}$ | ns | EC |
| OS31 | TosR, TosF | External Clock in (OSC1) Rise or Fall Time | — | — | 20 | ns | EC |
| OS40 | TckR | CLKO Rise Time ⁽³⁾ | — | 15 | 20 | ns | |
| OS41 | TckF | CLKO Fall Time ⁽³⁾ | — | 15 | 20 | ns | |

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: PLL dividers and postscalers must be configured so that the system clock frequency does not exceed the maximum operating frequency.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

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TABLE 26-18: PLL CLOCK TIMING SPECIFICATIONS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | |
|---|--------|---|-------|------|---------|
| Param No. | Symbol | Characteristic | Min | Max | Units |
| OS50 | FPLLI | PLL Input Frequency Range ⁽¹⁾ | 2 | 24 | MHz |
| OS54 | FPLLO | PLL Output Frequency Range ⁽¹⁾ | 16 | 96 | MHz |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | — | 24 | μs |
| OS53 | DCLK | CLKO Stability (Jitter) | -0.12 | 0.12 | % |

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 26-19: INTERNAL OSCILLATOR ACCURACY⁽¹⁾

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | |
|---|---|-----|--------------------|-----|-------|
| Param No. | Characteristic | Min | Typ ⁽²⁾ | Max | Units |
| F20A | FRC Accuracy @ 8 MHz | -5 | — | 5 | % |
| F20B | FRC Accuracy @ 8 MHz ⁽³⁾ | -3 | — | 3 | % |
| F21A | LPRC @ 32 kHz ⁽³⁾ | -20 | — | 20 | % |
| F21B | LPRC @ 32 kHz | -30 | — | 30 | % |
| F22 | FRC Tune Step-Size (in OSCTUN register) | — | 0.05 | — | %/Bit |

Note 1: To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.

2: Data in the “Typ” column is 3.3V unless otherwise stated. Parameters are for design guidance only and are not tested.

3: $-40^{\circ}C$ to $+85^{\circ}C$.

TABLE 26-20: INTERNAL OSCILLATOR START-UP TIME

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | |
|---|--------|---------------------------------------|-----|---------|
| Param No. | Symbol | Characteristic | Max | Units |
| FR0 | TFRC | FRC Oscillator Start-up Time | 2 | μs |
| FR1 | TLPRC | Low-Power RC Oscillator Start-up Time | 70 | μs |

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FIGURE 26-4: CLKO AND I/O TIMING CHARACTERISTICS

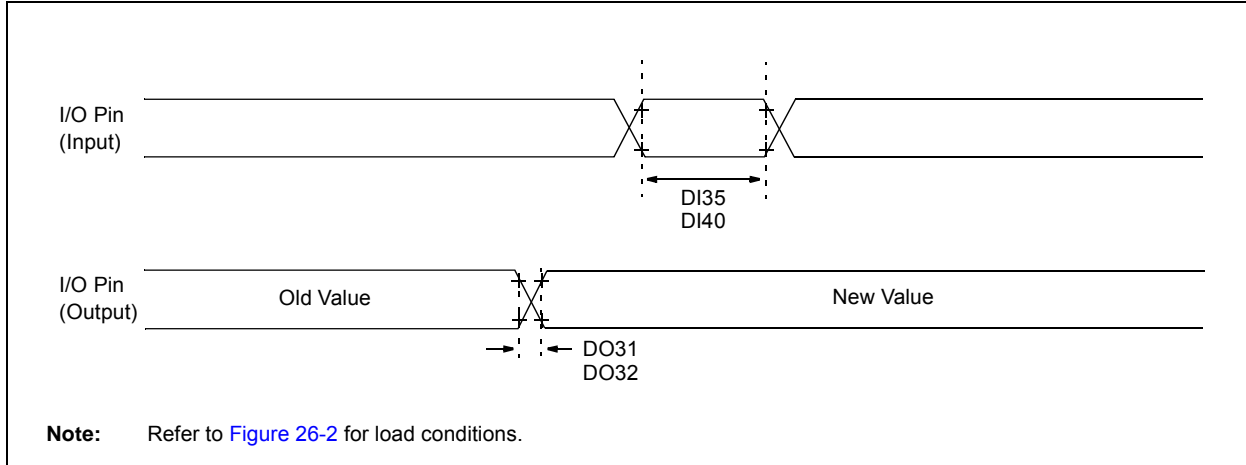


TABLE 26-21: CLKO AND I/O TIMING REQUIREMENTS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | |
|---|--------|---------------------------------|-----|--------------------|-----|-------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽¹⁾ | Max | Units |
| DO31 | TioR | Port Output Rise Time | — | 10 | 25 | ns |
| DO32 | TioF | Port Output Fall Time | — | 10 | 25 | ns |
| DI35 | TINP | INTx Input Pin High or Low Time | 10 | — | — | ns |
| DI40 | TRBP | CNx Input Pin High or Low Time | 10 | — | — | ns |

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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TABLE 26-22: RESET, BROWN-OUT RESET AND SLEEP MODES TIMING SPECIFICATIONS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | | |
|---|-------------------------|---|-----|--------------------|-----|---------|--|
| Param No. | Symbol | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| SY10 | TMCL | MCLR Pulse Width (Low) | 2 | — | — | μs | |
| SY13 | TIOZ | I/O High-Impedance from MCLR Low | — | 1 | — | μs | |
| SY25 | TBOR | Brown-out Reset Pulse Width | 1 | — | — | μs | $V_{DD} \leq V_{BOR}$ |
| SY45 | TRST | Reset State Time | — | 25 | — | μs | |
| SY71 | TWAKE ⁽²⁾ | Wake-up Time with Main Voltage Regulator | — | 22 | — | μs | Sleep wake-up with VREGS = 0, RETEN = 0, RETVR = 1 |
| | | | — | 3.8 | — | μs | Sleep wake-up with VREGS = 1, RETEN = 0, RETVR = 1 |
| SY72 | TWAKELVR ⁽²⁾ | Wake-up Time with Retention Low-Voltage Regulator | — | 163 | — | μs | Sleep wake-up with VREGS = 0, RETEN = 1, RETVR = 0 |
| | | | — | 23 | — | μs | Sleep wake-up with VREGS = 1, RETEN = 1, RETVR = 0 |

Note 1: Data in the “Typ.” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The parameters are measured with the external clock source (EC). To get the full wake-up time, the oscillator start-up time must be added.

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FIGURE 26-5: TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS

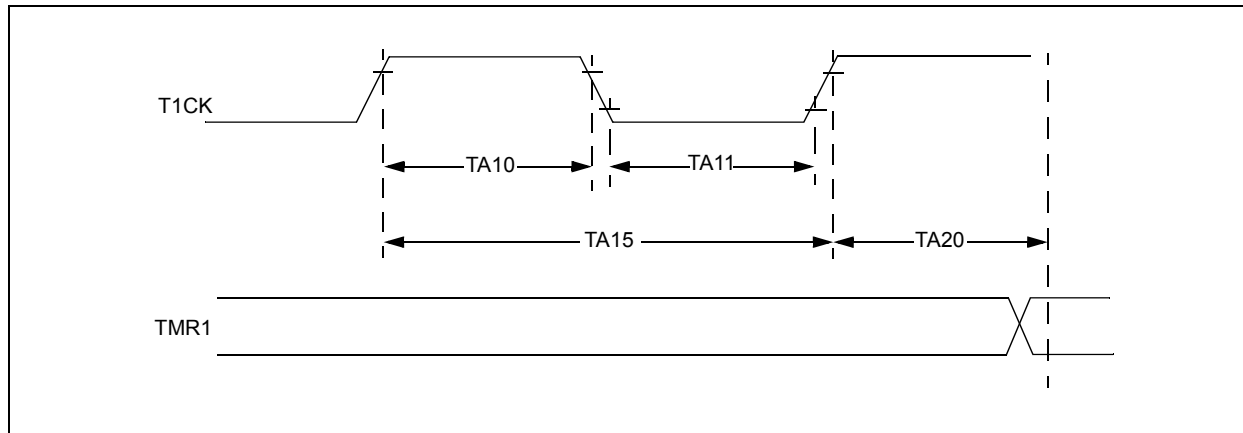


TABLE 26-23: MCCP/SCCP TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | | |
|---|-----------|--|--------------|-----|-----|--------|-------------------------------|
| Param. No. | Symbol | Characteristics ⁽¹⁾ | | Min | Max | Units | Conditions |
| TA10 | TCKH | T1CK High Time | Synchronous | 1 | — | TPBCLK | Must also meet Parameter TA15 |
| | | | Asynchronous | 10 | — | ns | |
| TA11 | TCKL | T1CK Low Time | Synchronous | 1 | — | TPBCLK | Must also meet Parameter TA15 |
| | | | Asynchronous | 10 | — | ns | |
| TA15 | TCKP | T1CK Input Period | Synchronous | 2 | — | TPBCLK | |
| | | | Asynchronous | 20 | — | ns | |
| TA20 | TCKEXTMRL | Delay from External T1CK Clock Edge to Timer Increment | | — | 3 | TPBCLK | Synchronous mode |

Note 1: These parameters are characterized but not tested in manufacturing.

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FIGURE 26-6: MCCP/SCCP TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

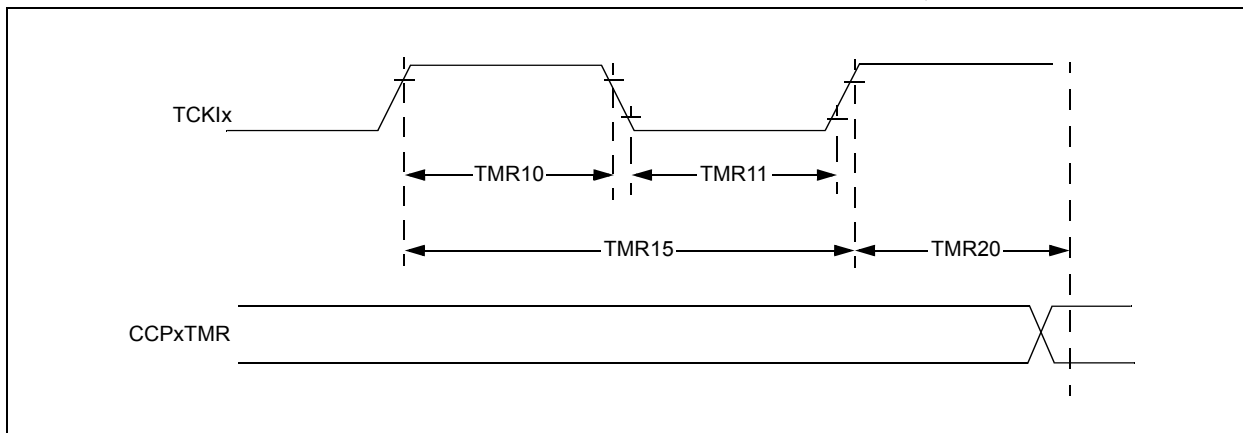


TABLE 26-24: MCCP/SCCP TIMING REQUIREMENTS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | | |
|---|-----------|---|--------------|-----|--------|------------|--------------------------------|
| Param. No. | Symbol | Characteristics ⁽¹⁾ | Min | Max | Units | Conditions | |
| TMR10 | TCKH | TCKIx High Time | Synchronous | 1 | — | TPBCLK | Must also meet Parameter TMR15 |
| | | | Asynchronous | 10 | — | ns | |
| TMR11 | TCKL | TCKIx Low Time | Synchronous | 1 | — | TPBCLK | Must also meet Parameter TMR15 |
| | | | Asynchronous | 10 | — | ns | |
| TMR15 | TCKP | TCKIx Input Period | Synchronous | 2 | — | TPBCLK | |
| | | | Asynchronous | 20 | — | ns | |
| TMR20 | TCKEXTMRL | Delay from External TCKIx Clock Edge to Timer Increment | — | 1 | TPBCLK | | |

Note 1: These parameters are characterized but not tested in manufacturing.

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FIGURE 26-7: MCCP AND SCCP INPUT CAPTURE x MODE TIMING CHARACTERISTICS

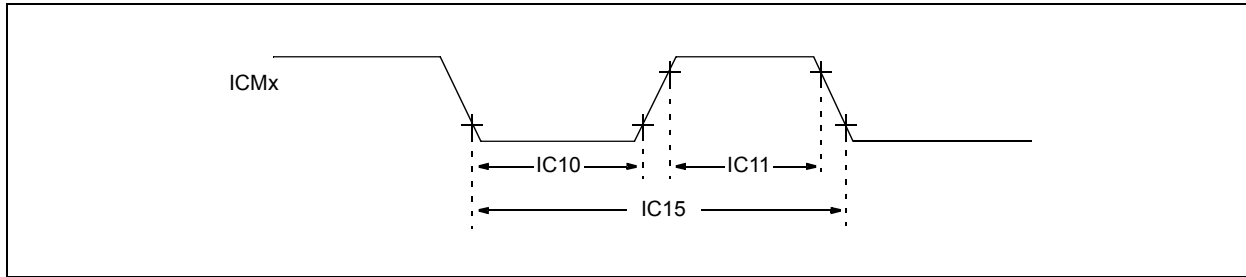


TABLE 26-25: MCCP AND SCCP INPUT CAPTURE x MODE TIMING REQUIREMENTS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | |
|---|--------|--------------------------------|-----|-----|-------|-------------------------------|
| Param. No. | Symbol | Characteristics ⁽¹⁾ | Min | Max | Units | Conditions |
| IC10 | TICL | ICMx Input Low Time | 25 | — | ns | Must also meet Parameter IC15 |
| IC11 | TICH | ICMx Input High Time | 25 | — | ns | Must also meet Parameter IC15 |
| IC15 | TICP | ICMx Input Period | 50 | — | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 26-8: MCCP AND SCCP OUTPUT COMPARE x MODE TIMING CHARACTERISTICS

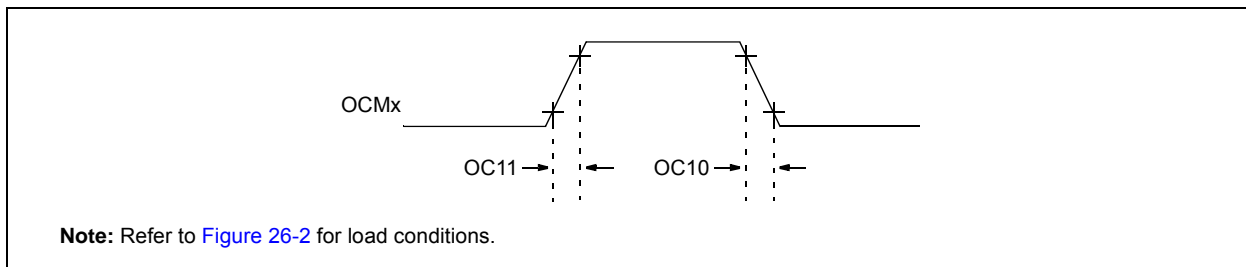


TABLE 26-26: MCCP AND SCCP OUTPUT COMPARE x MODE TIMING REQUIREMENTS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | |
|---|--------|--------------------------------|-----|-----|-----|-------|
| Param. No. | Symbol | Characteristics ⁽¹⁾ | Min | Typ | Max | Units |
| OC10 | TOCF | OCMx Output Fall Time | — | 10 | 25 | ns |
| OC11 | TOCR | OCMx Output Rise Time | — | 10 | 25 | ns |

Note 1: These parameters are characterized but not tested in manufacturing.

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FIGURE 26-9: MCCP AND SCCP PWM_x MODE TIMING CHARACTERISTICS

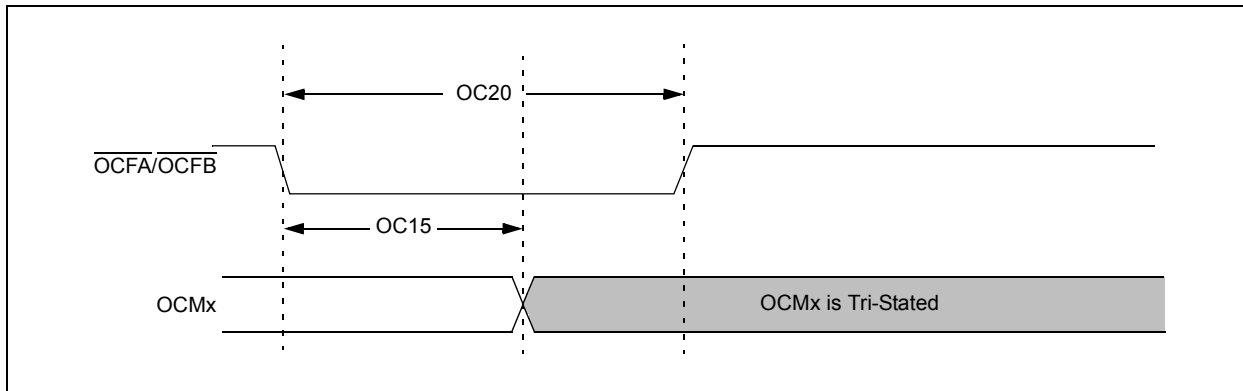


TABLE 26-27: MCCP AND SCCP PWM MODE TIMING REQUIREMENTS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | |
|---|--------|--------------------------------|-----|-----|-------|
| Param No. | Symbol | Characteristics ⁽¹⁾ | Min | Max | Units |
| OC15 | TFD | Fault Input to PWM I/O Change | — | 30 | ns |
| OC20 | TFLT | Fault Input Pulse Width | 10 | — | ns |

Note 1: These parameters are characterized but not tested in manufacturing.

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FIGURE 26-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS

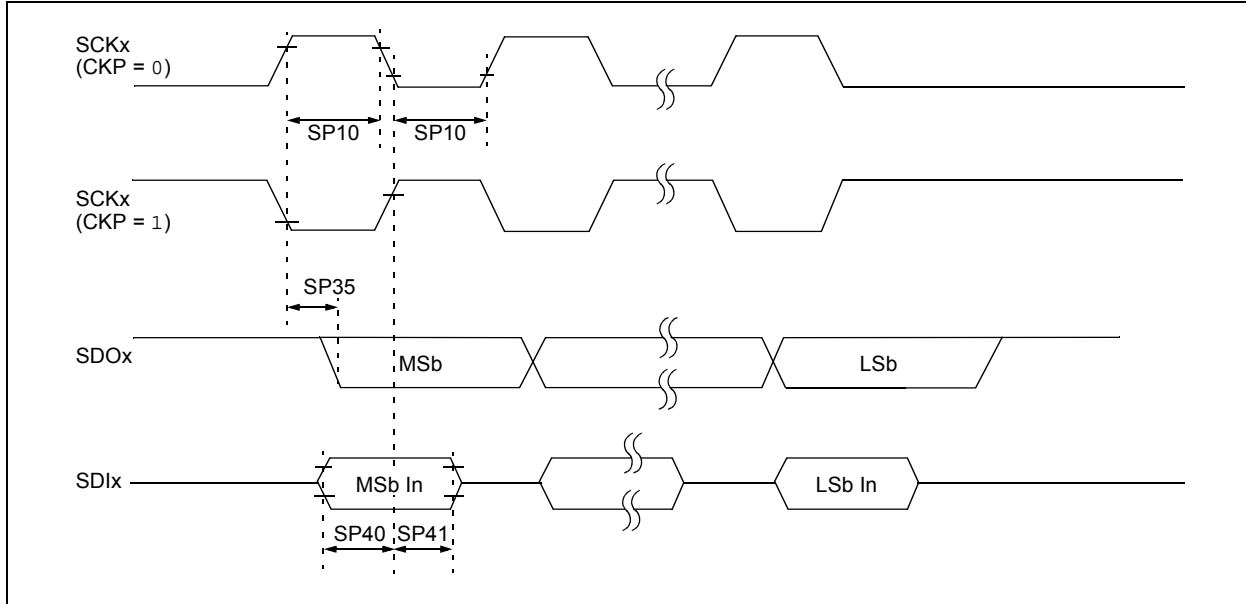
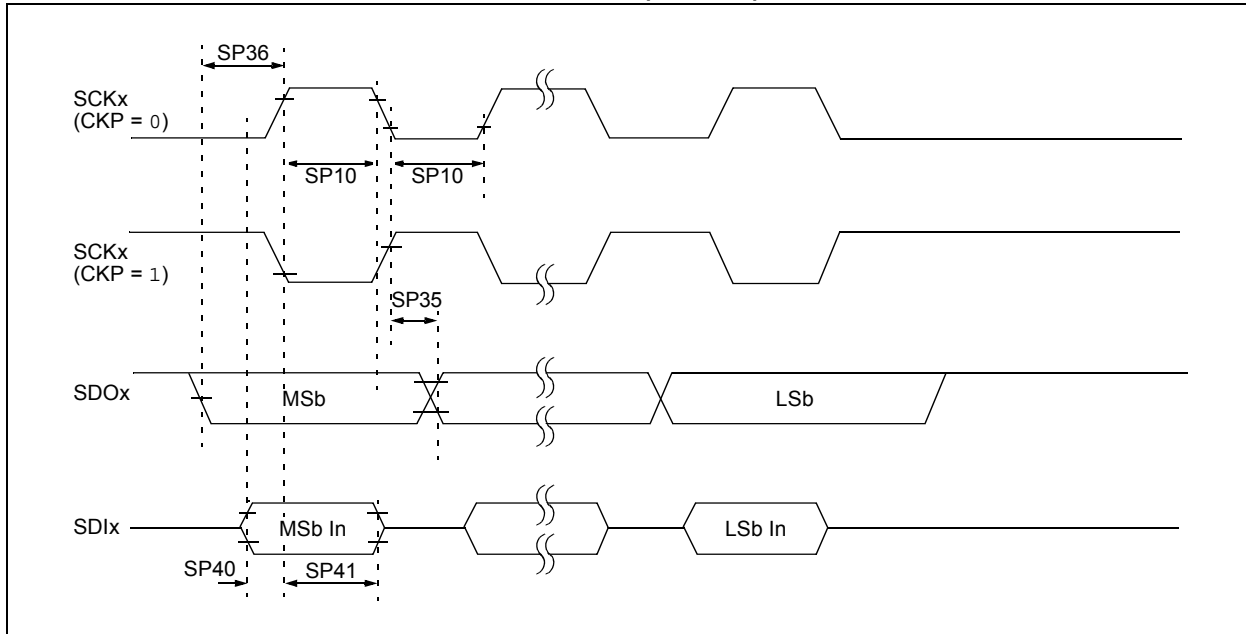


FIGURE 26-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



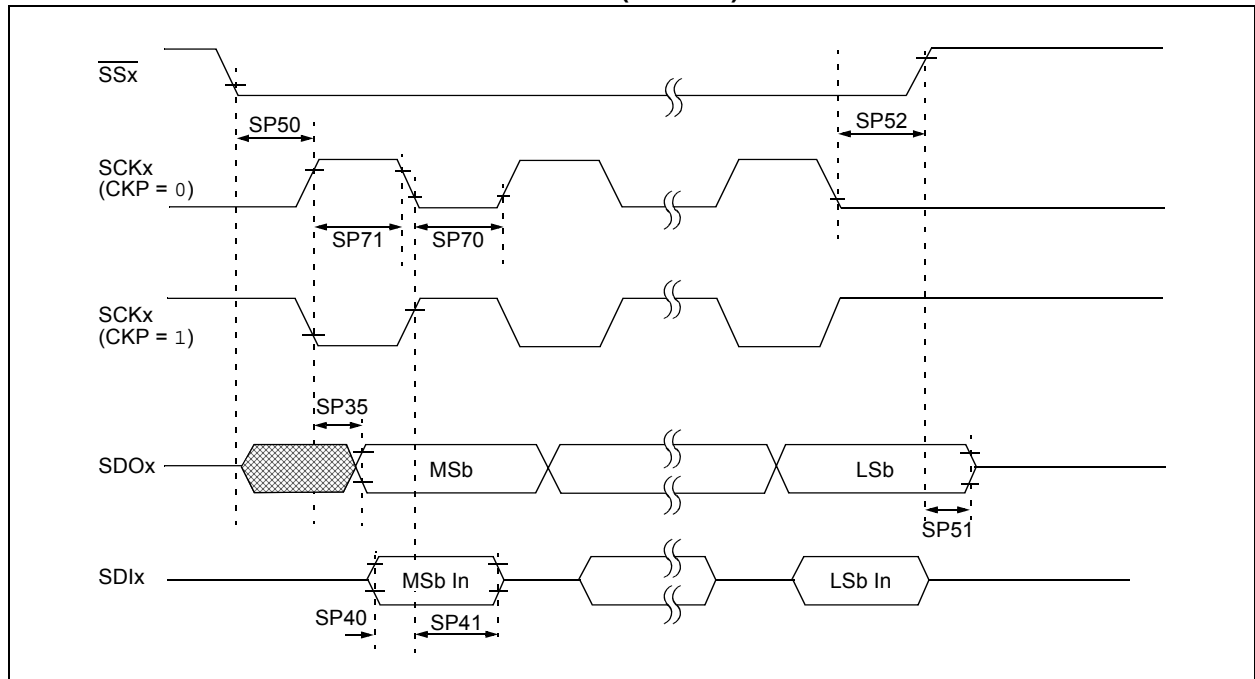
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TABLE 26-28: SPIx MODULE MASTER MODE TIMING REQUIREMENTS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | |
|---|--------------------|--|-----|-----|-------|
| Param. No. | Symbol | Characteristics ⁽¹⁾ | Min | Max | Units |
| SP10 | TsCL, TscH | SCKx Output Low or High Time | 10 | — | ns |
| SP35 | Tsch2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 7 | ns |
| SP36 | TdoV2sc, TdoV2scl | SDOx Data Output Setup to First SCKx Edge | 7 | — | ns |
| SP40 | TdIV2sch, TdIV2scl | Setup Time of SDIx Data Input to SCKx Edge | 7 | — | ns |
| SP41 | Tsch2dIL, TscL2dIL | Hold Time of SDIx Data Input to SCKx Edge | 7 | — | ns |

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 26-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



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FIGURE 26-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

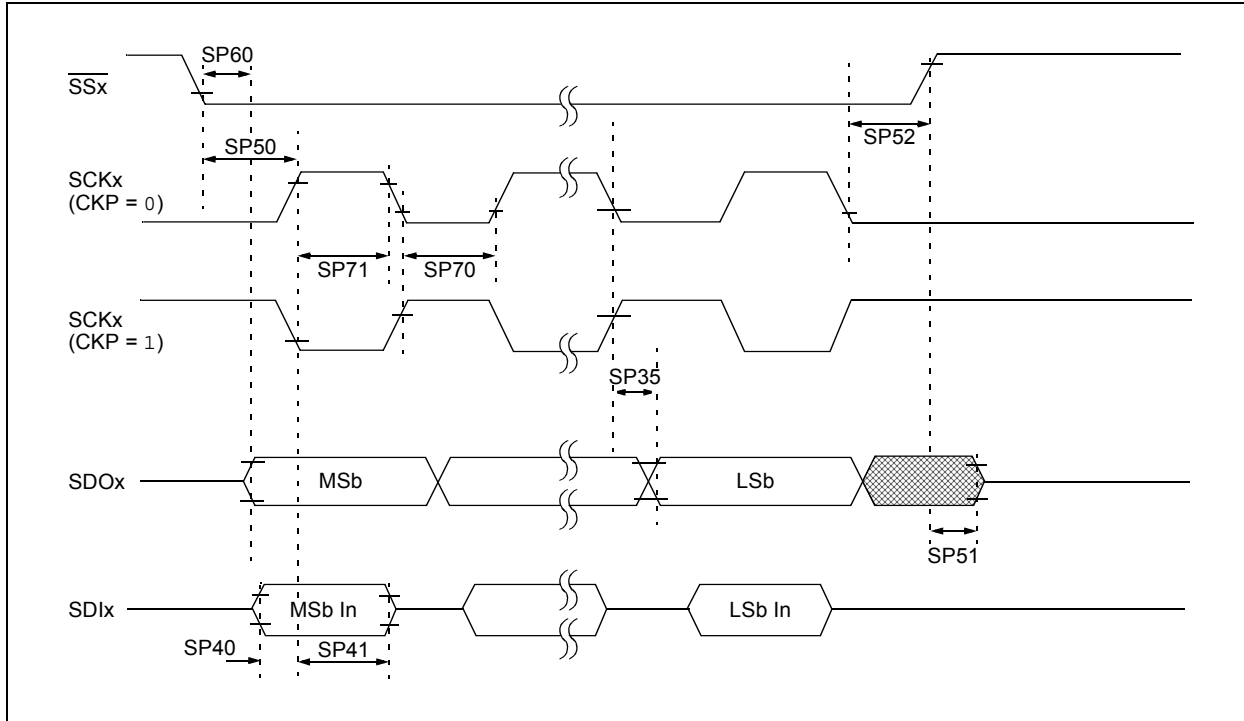


TABLE 26-29: SPIx MODULE SLAVE MODE TIMING REQUIREMENTS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | |
|---|-----------------------|---|-----|------|-------|
| Param.No. | Symbol | Characteristics ⁽¹⁾ | Min | Max | Units |
| SP70 | TscL | SCKx Input Low Time | 10 | — | ns |
| SP71 | Tsch | SCKx Input High Time | 10 | — | ns |
| SP35 | Tsch2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 10 | ns |
| SP40 | TdIV2sch, TdIV2scL | Setup Time of SDIx Data Input to SCKx Edge | 0 | — | ns |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 7 | — | ns |
| SP50 | Tssl2sch, Tssl2scL | $\overline{SSx} \downarrow$ to SCKx \downarrow or SCKx \uparrow Input | 40 | — | ns |
| SP51 | Tssh2doZ | $\overline{SSx} \uparrow$ to SDOx Output High-Impedance | 2.5 | 12 | ns |
| SP52 | Tsch2ssH TscL2ssH | $\overline{SSx} \uparrow$ after SCKx Edge | 10 | — | ns |
| SP60 | Tssl2doV | SDOx Data Output Valid after \overline{SSx} Edge | — | 12.5 | ns |

Note 1: These parameters are characterized but not tested in manufacturing.

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TABLE 26-30: ADC MODULE INPUTS SPECIFICATIONS

| Operating Conditions: $2.2V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | |
|---|-----------------------|--|-------------------|-------------------|-------|
| Param No. | Symbol | Characteristic | Min | Max | Units |
| Reference Inputs | | | | | |
| AD01 | AVDD | Module VDD Supply | VDD | VDD | V |
| AD02 | AVSS | Module Vss Supply | VSS | VSS | V |
| Analog Inputs | | | | | |
| AD10 | V _{INH-VINL} | Full-Scale Input Span | V _{REFL} | V _{REFH} | V |
| AD11 | V _{IN} | Absolute Input Voltage | VSS – 0.3 | VDD + 0.3 | V |
| AD12 | V _{INL} | Absolute V _{INL} Input Voltage | VSS – 0.3 | VDD + 0.3 | V |
| AD17 | R _{IN} | Recommended Impedance of Analog Voltage Source | — | 1.2K | Ω |

TABLE 26-31: ADC ACCURACY AND CONVERSION TIMING REQUIREMENTS FOR 12-BIT MODE⁽¹⁾

| Operating Conditions: $V_{DD} = AV_{DD} = V_{REFH} \geq 2.9V$, $AV_{SS} = V_{REFL} = 0V$, $-40^{\circ}C < T_A < +125^{\circ}C$ | | | | | | |
|--|-------------------|---|-----|--------------------|-------------|-----------------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽²⁾ | Max | Units |
| ADC Accuracy | | | | | | |
| AD20B | Nr | Resolution | — | 12 | — | bits |
| AD21B | INL | Integral Nonlinearity | — | ±2.5 | ±3.5 | LSb |
| AD22B | DNL | Differential Nonlinearity | — | ±0.75 | +1.75/-0.95 | LSb |
| AD23B | GERR | Gain Error | — | ±2 | ±3 | LSb |
| AD24B | E _{OFF} | Offset Error | — | ±1 | ±2 | LSb |
| Clock Parameters | | | | | | |
| AD50B | T _{AD} | ADC Clock Period | 250 | — | — | ns |
| AD50B ⁽³⁾ | T _{AD} | ADC Clock Period | 300 | — | — | ns |
| AD56B ⁽³⁾ | FCNV | FCNV Throughput Rate | — | — | 185 | ksps |
| AD56B | FCNV | Throughput Rate | — | — | 222 | ksps |
| Conversion Rate | | | | | | |
| AD55B | t _{CONV} | Conversion Time | — | 16 | — | T _{AD} |
| AD61B | t _{PSS} | Sample Start Delay from Setting Sample bit (SAMP) | 2 | — | 3 | T _{AD} |

- Note 1:** Measurements are taken with the external V_{REF+} and V_{REF-} used as the ADC voltage reference.
- Note 2:** Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- Note 3:** $2.2V < (V_{DD} = AV_{DD} = V_{REFH}) < 2.9V$, $AV_{SS} = V_{REFL} = 0V$, $-40^{\circ}C < T_A < +125^{\circ}C$

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TABLE 26-32: ADC ACCURACY AND CONVERSION TIMING REQUIREMENTS FOR 10-BIT MODE⁽¹⁾

| Operating Conditions: $V_{DD} = AV_{DD} = V_{REFH} \geq 2.9V$, $AV_{SS} = V_{REFL} = 0V$, $-40^{\circ}C < T_A < +125^{\circ}C$ | | | | | | |
|--|-------------------|---|-----|--------------------|---------------|-----------------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽²⁾ | Max | Units |
| ADC Accuracy | | | | | | |
| AD20A | Nr | Resolution | — | 10 | — | bits |
| AD21A | INL | Integral Nonlinearity | — | ± 2.5 | ± 3.5 | LSb |
| AD22A | DNL | Differential Nonlinearity | — | ± 0.75 | $+1.75/-0.95$ | LSb |
| AD23A | GERR | Gain Error | — | ± 2 | ± 3 | LSb |
| AD24A | E _{OFF} | Offset Error | — | ± 1 | ± 2 | LSb |
| Clock Parameters | | | | | | |
| AD50A | T _{AD} | ADC Clock Period | 250 | — | — | ns |
| AD50A ⁽³⁾ | T _{AD} | ADC Clock Period | 300 | — | — | ns |
| AD61A | t _{PSS} | Sample Start Delay from Setting Sample bit (SAMP) | 2 | — | 3 | T _{AD} |
| Conversion Rate | | | | | | |
| AD55A | t _{CONV} | Conversion Time | — | 14 | — | T _{AD} |
| AD56A | F _{CONV} | Throughput Rate | — | — | 250 | ksps |
| AD56A ⁽³⁾ | F _{CONV} | Throughput Rate | — | — | 187 | ksps |

Note 1: Measurements are taken with the external VREF+ and VREF- used as the ADC voltage reference.

2: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: $2.2V < (V_{DD} = AV_{DD} = V_{REFH}) < 2.9V$, $AV_{SS} = V_{REFL} = 0V$, $-40^{\circ}C < T_A < +125^{\circ}C$

PIC32MM0064GPL036 FAMILY

FIGURE 26-14: EJTAG TIMING CHARACTERISTICS

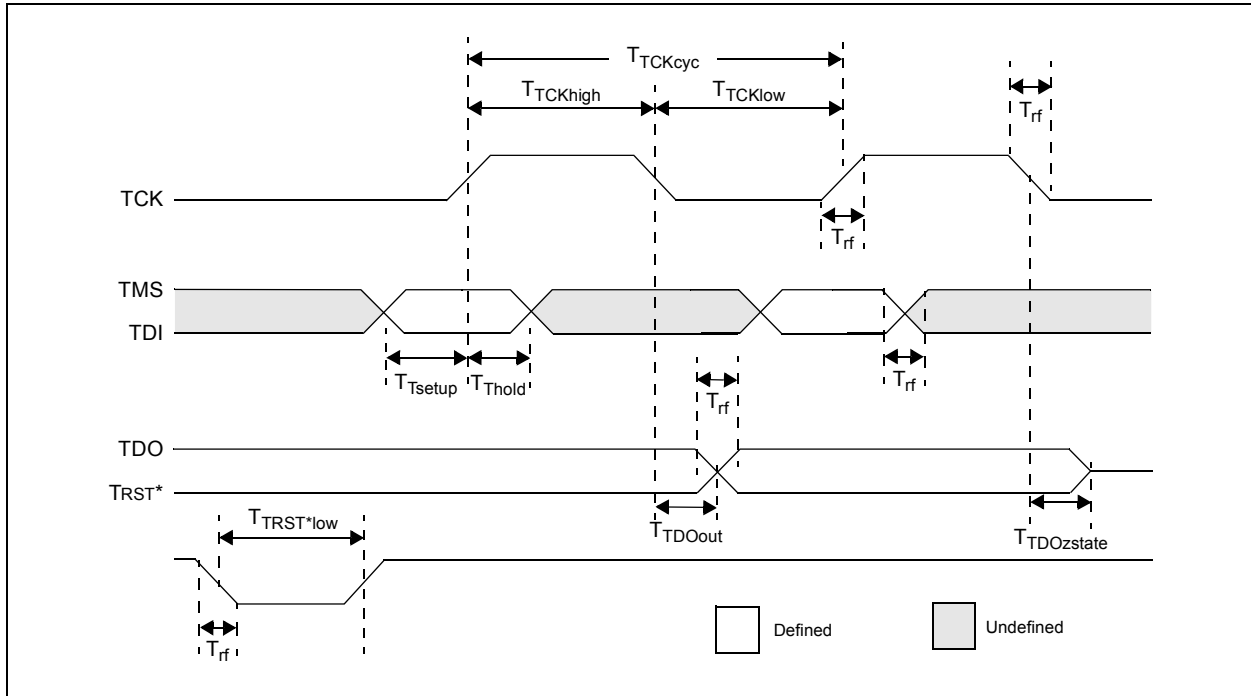


TABLE 26-33: EJTAG TIMING REQUIREMENTS

| Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (unless otherwise stated) | | | | | | |
|---|------------|--|-----|-----|-------|------------|
| Param. No. | Symbol | Description ⁽¹⁾ | Min | Max | Units | Conditions |
| EJ1 | TTCKCYC | TCK Cycle Time | 25 | — | ns | |
| EJ2 | TTCKHIGH | TCK High Time | 10 | — | ns | |
| EJ3 | TTCKLOW | TCK Low Time | 10 | — | ns | |
| EJ4 | TTSETUP | TAP Signals Setup Time before Rising TCK | 5 | — | ns | |
| EJ5 | TTHOLD | TAP Signals Hold Time after Rising TCK | 3 | — | ns | |
| EJ6 | TTDOOUT | TDO Output Delay Time from Falling TCK | — | 5 | ns | |
| EJ7 | TTDOZSTATE | TDO 3-State Delay Time from Falling TCK | — | 5 | ns | |
| EJ8 | TTRSTLOW | TRST Low Time | 25 | — | ns | |
| EJ9 | TRF | TAP Signals Rise/Fall Time, All Input and Output | — | — | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

PIC32MM0064GPL036 FAMILY

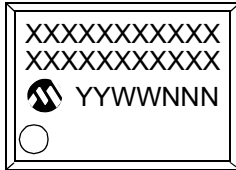
NOTES:

PIC32MM0064GPL036 FAMILY

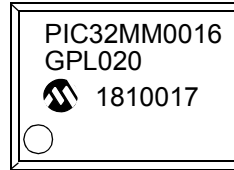
27.0 PACKAGING INFORMATION

27.1 Package Marking Information

20-Lead SSOP



Example



20-Lead QFN



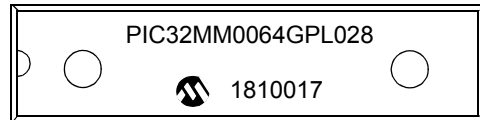
Example



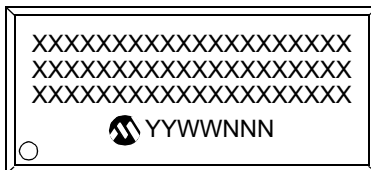
28-Lead SPDIP



Example



28-Lead SOIC (7.5 mm)



Example



| | | |
|----------------|---|--|
| Legend: | XX...X | Customer-specific information |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | * | All packages are Pb-free |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. | |

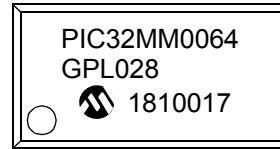
PIC32MM0064GPL036 FAMILY

27.1 Package Marking Information (Continued)

28-Lead SSOP



Example



28-Lead QFN



Example



28-Lead UQFN



Example



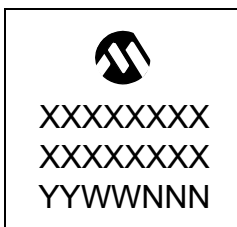
36-Lead VQFN



Example



40-Lead UQFN



Example



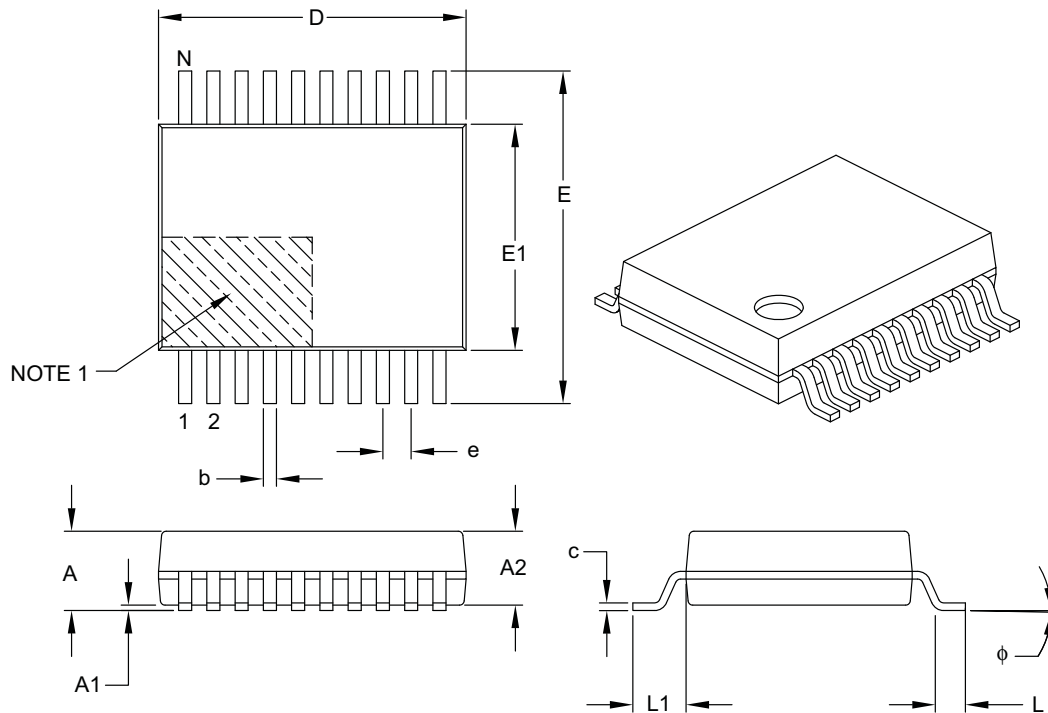
PIC32MM0064GPL036 FAMILY

27.2 Package Details

The following sections give the technical details of the packages.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | MILLIMETERS | | |
|--------------------------|--------|-------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 20 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 6.90 | 7.20 | 7.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | 1.25 REF | | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | ϕ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

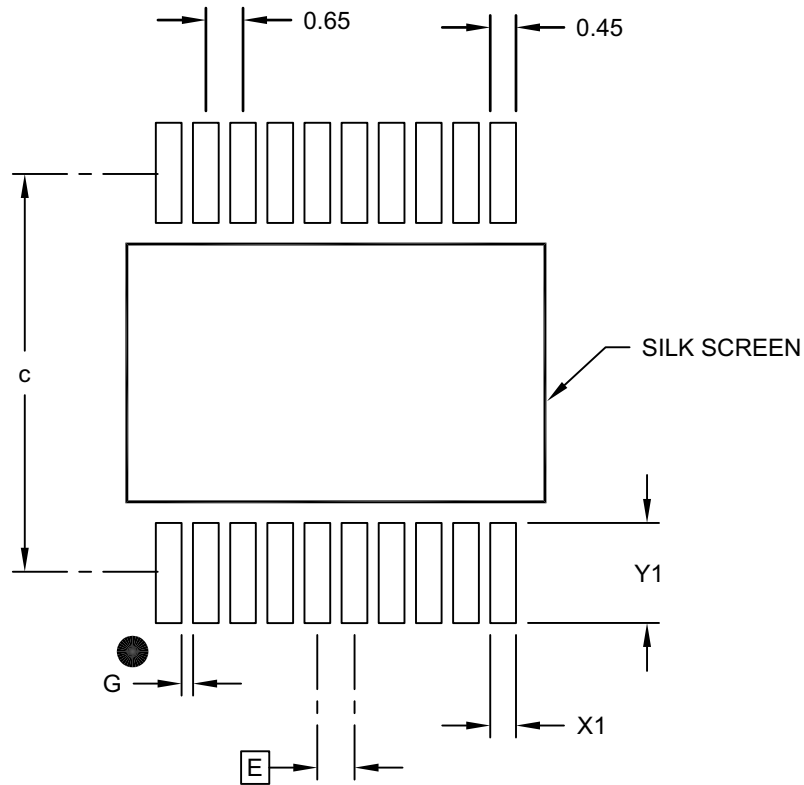
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

PIC32MM0064GPL036 FAMILY

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 7.20 | |
| Contact Pad Width (X20) | X1 | | | 0.45 |
| Contact Pad Length (X20) | Y1 | | | 1.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

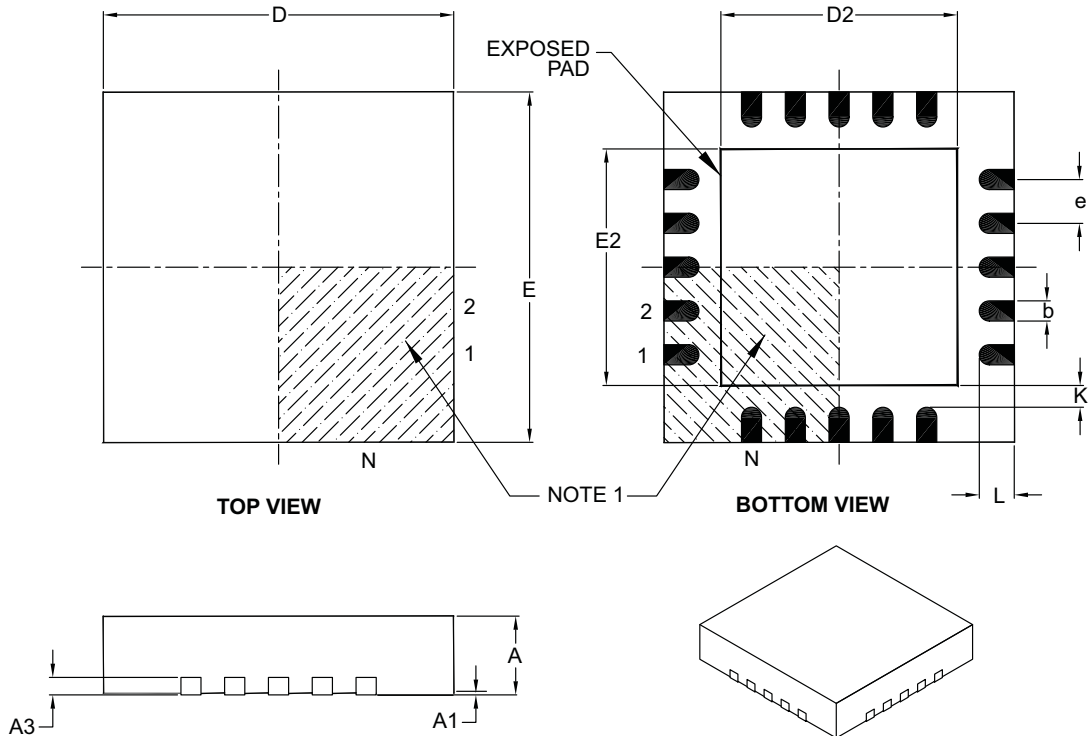
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072B

PIC32MM0064GPL036 FAMILY

20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 20 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Width | E | 4.00 BSC | | |
| Exposed Pad Width | E2 | 2.60 | 2.70 | 2.80 |
| Overall Length | D | 4.00 BSC | | |
| Exposed Pad Length | D2 | 2.60 | 2.70 | 2.80 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

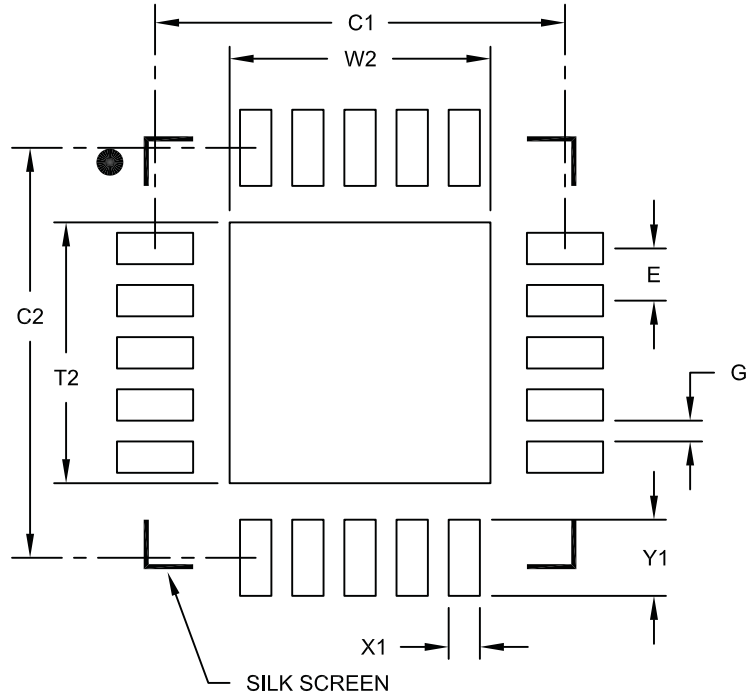
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

PIC32MM0064GPL036 FAMILY

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | W2 | | | 2.50 |
| Optional Center Pad Length | T2 | | | 2.50 |
| Contact Pad Spacing | C1 | | 3.93 | |
| Contact Pad Spacing | C2 | | 3.93 | |
| Contact Pad Width | X1 | | | 0.30 |
| Contact Pad Length | Y1 | | | 0.73 |
| Distance Between Pads | G | 0.20 | | |

Notes:

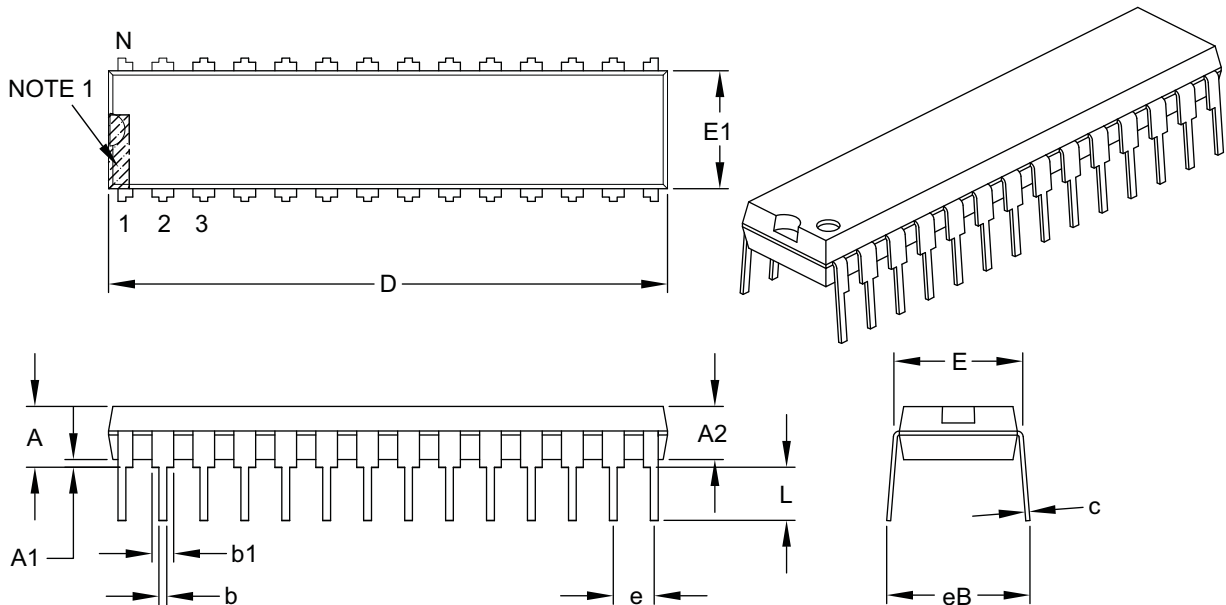
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A

PIC32MM0064GPL036 FAMILY

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | INCHES | | |
|----------------------------|-------|----------|-------|-------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .200 |
| Molded Package Thickness | A2 | .120 | .135 | .150 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .335 |
| Molded Package Width | E1 | .240 | .285 | .295 |
| Overall Length | D | 1.345 | 1.365 | 1.400 |
| Tip to Seating Plane | L | .110 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .050 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

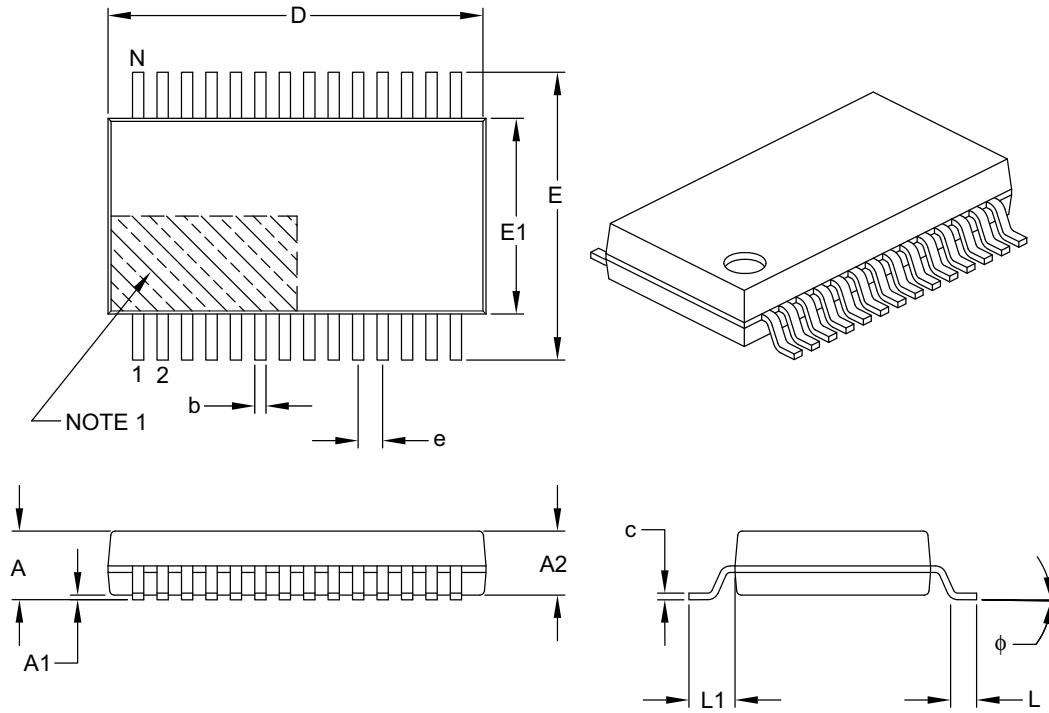
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

PIC32MM0064GPL036 FAMILY

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|-------|-------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 9.90 | 10.20 | 10.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | 1.25 REF | | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | ϕ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

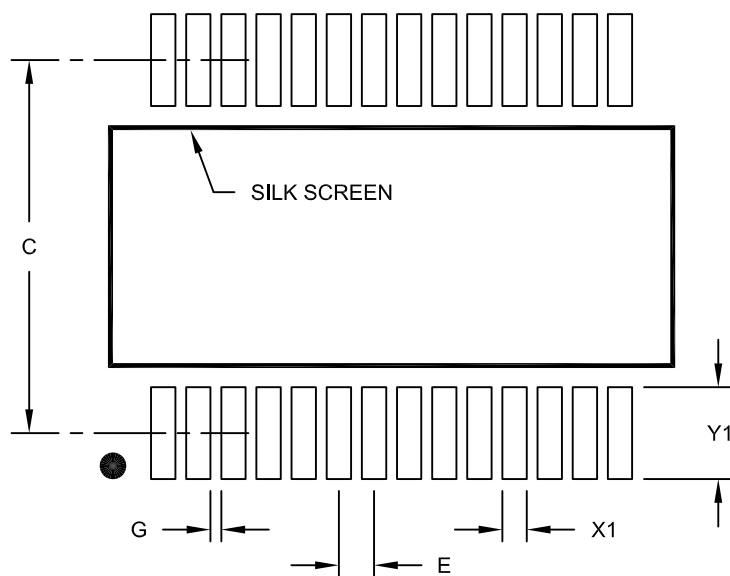
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

PIC32MM0064GPL036 FAMILY

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | 7.20 | | |
| Contact Pad Width (X28) | X1 | | | 0.45 |
| Contact Pad Length (X28) | Y1 | | | 1.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

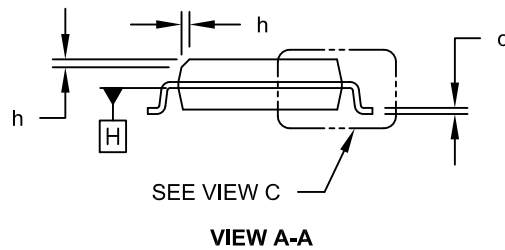
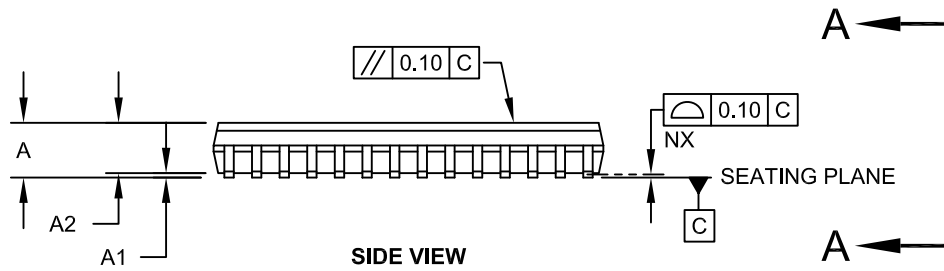
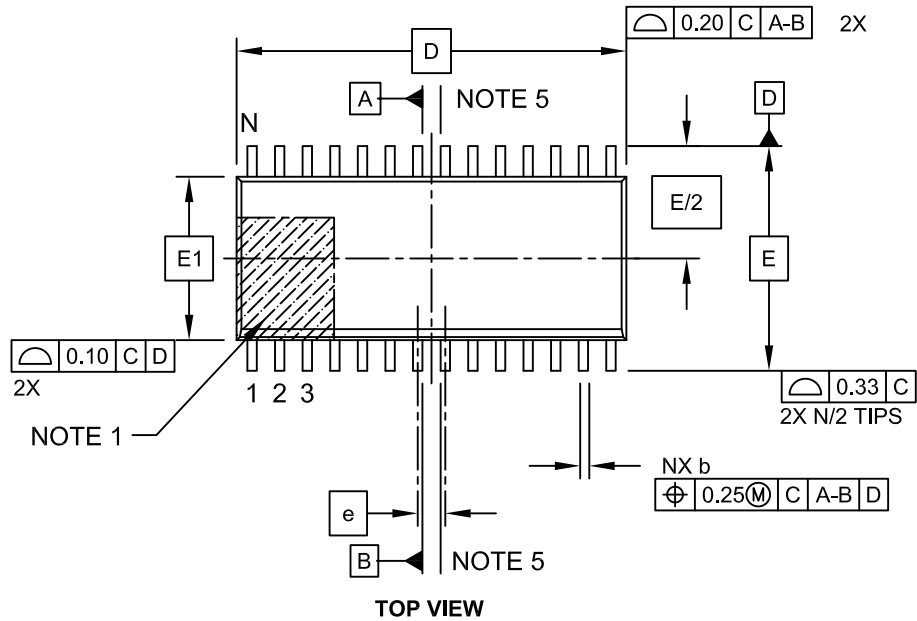
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

PIC32MM0064GPL036 FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

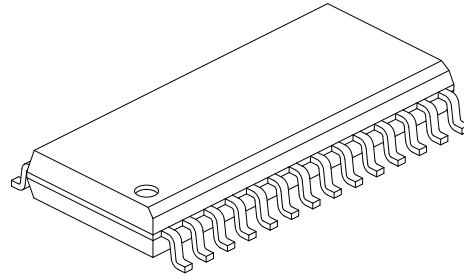
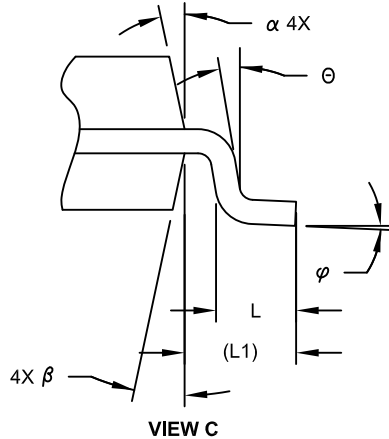


Microchip Technology Drawing C04-052C Sheet 1 of 2

PIC32MM0064GPL036 FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | MILLIMETERS | | |
|--------------------------|----|-------|-------------|-----|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | | |
| Pitch | e | | 1.27 BSC | | |
| Overall Height | A | - | - | - | 2.65 |
| Molded Package Thickness | A2 | 2.05 | - | - | - |
| Standoff § | A1 | 0.10 | - | - | 0.30 |
| Overall Width | E | | 10.30 BSC | | |
| Molded Package Width | E1 | | 7.50 BSC | | |
| Overall Length | D | | 17.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | - | 0.75 |
| Foot Length | L | 0.40 | - | - | 1.27 |
| Footprint | L1 | | 1.40 REF | | |
| Lead Angle | θ | 0° | - | - | - |
| Foot Angle | φ | 0° | - | - | 8° |
| Lead Thickness | c | 0.18 | - | - | 0.33 |
| Lead Width | b | 0.31 | - | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | - | 15° |

Notes:

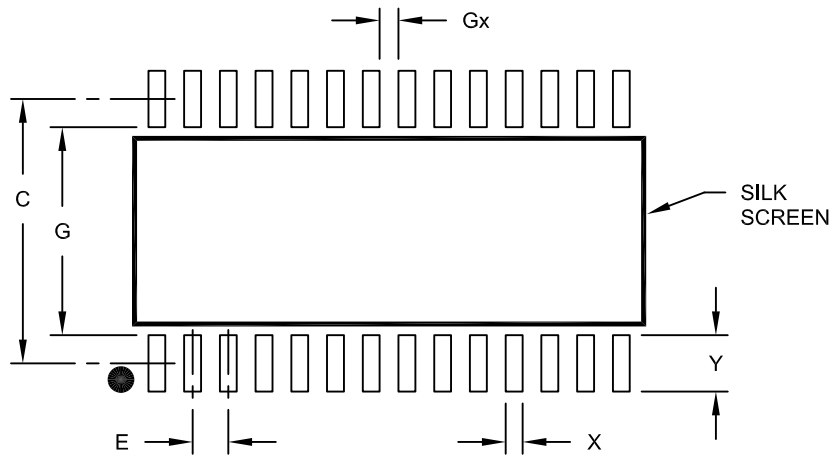
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

PIC32MM0064GPL036 FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| | | Units | MILLIMETERS | | |
|--------------------------|----|------------------|-------------|------|------|
| | | Dimension Limits | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | | |
| Contact Pad Spacing | C | | | 9.40 | |
| Contact Pad Width (X28) | X | | | | 0.60 |
| Contact Pad Length (X28) | Y | | | | 2.00 |
| Distance Between Pads | Gx | | 0.67 | | |
| Distance Between Pads | G | | 7.40 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

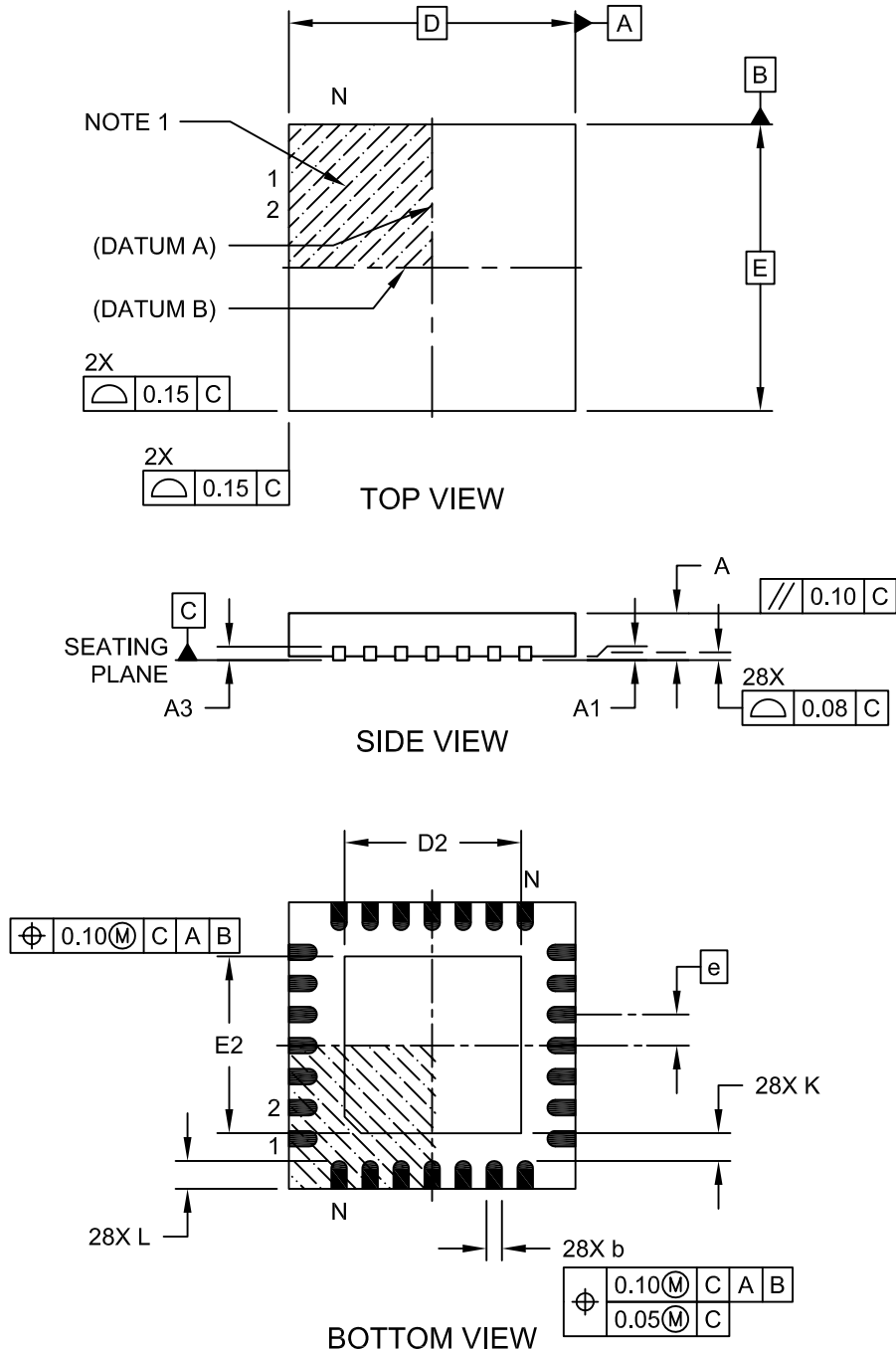
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

PIC32MM0064GPL036 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

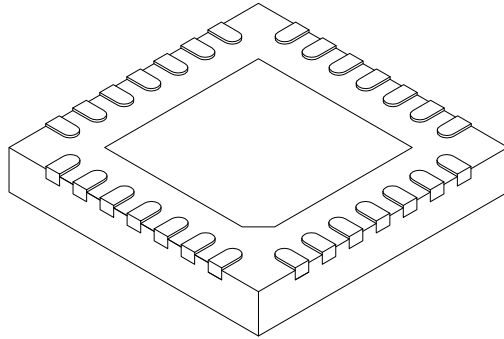


Microchip Technology Drawing C04-105C Sheet 1 of 2

PIC32MM0064GPL036 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension | Units Limits | MILLIMETERS | | |
|-------------------------|-----------------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.20 REF | | |
| Overall Width | E | 6.00 BSC | | |
| Exposed Pad Width | E2 | 3.65 | 3.70 | 4.20 |
| Overall Length | D | 6.00 BSC | | |
| Exposed Pad Length | D2 | 3.65 | 3.70 | 4.20 |
| Terminal Width | b | 0.23 | 0.30 | 0.35 |
| Terminal Length | L | 0.50 | 0.55 | 0.70 |
| Terminal-to-Exposed Pad | K | 0.20 | - | - |

Notes:

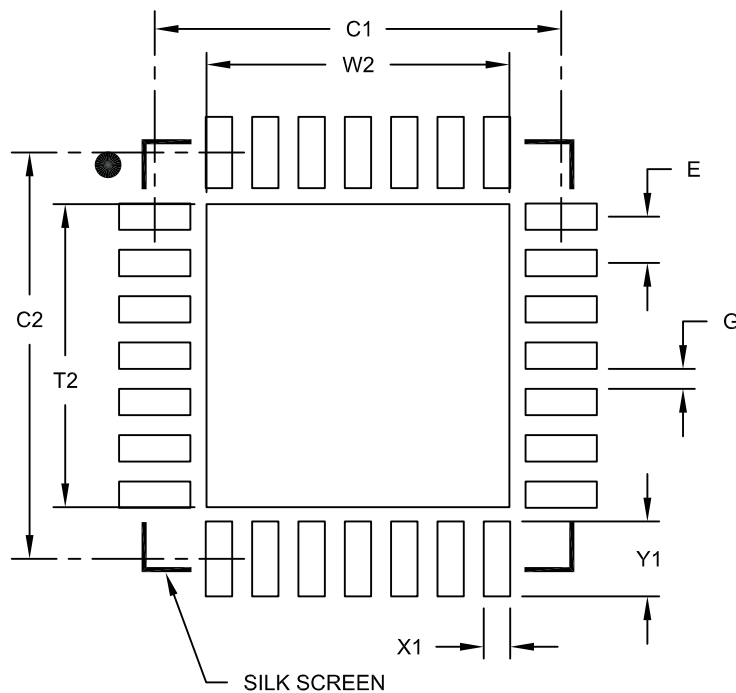
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105C Sheet 2 of 2

PIC32MM0064GPL036 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W2 | | | 4.25 |
| Optional Center Pad Length | T2 | | | 4.25 |
| Contact Pad Spacing | C1 | | 5.70 | |
| Contact Pad Spacing | C2 | | 5.70 | |
| Contact Pad Width (X28) | X1 | | | 0.37 |
| Contact Pad Length (X28) | Y1 | | | 1.00 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

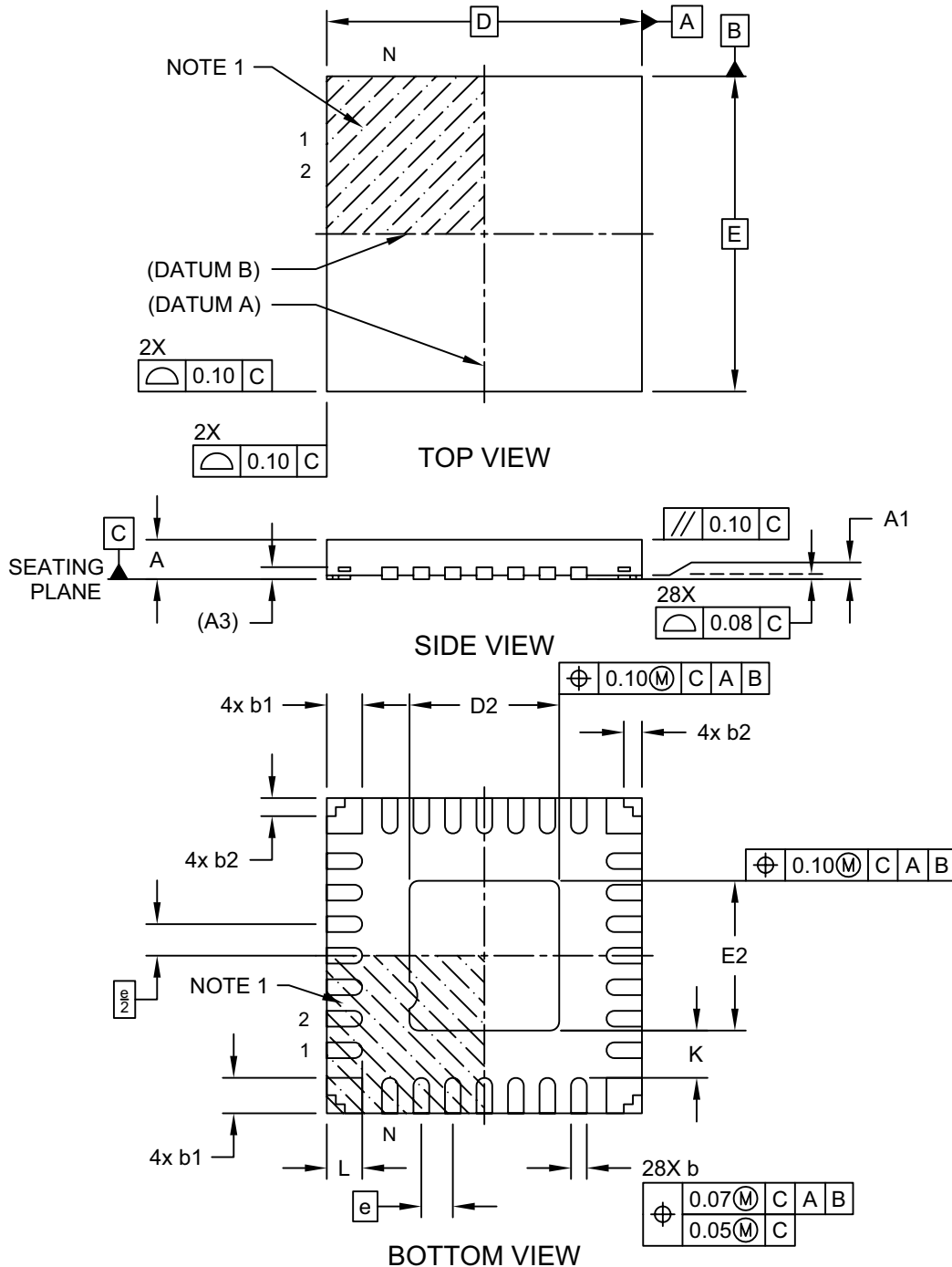
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

PIC32MM0064GPL036 FAMILY

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

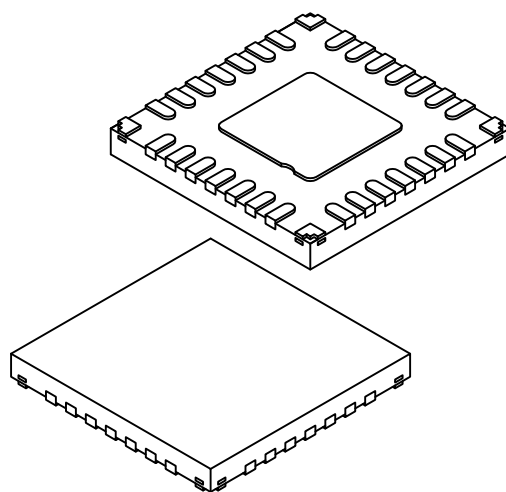


Microchip Technology Drawing C04-333-M6 Rev B Sheet 1 of 2

PIC32MM0064GPL036 FAMILY

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | MILLIMETERS | | |
|-----------------------------|----|-------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 0.40 BSC | | |
| Overall Height | A | - | - | 0.60 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.152 REF | | |
| Overall Width | E | 4.00 BSC | | |
| Exposed Pad Width | E2 | 1.80 | 1.90 | 2.00 |
| Overall Length | D | 4.00 BSC | | |
| Exposed Pad Length | D2 | 1.80 | 1.90 | 2.00 |
| Terminal Width | b | 0.15 | 0.20 | 0.25 |
| Corner Anchor Pad | b1 | 0.40 | 0.45 | 0.50 |
| Corner Pad, Metal Free Zone | b2 | 0.18 | 0.23 | 0.28 |
| Terminal Length | L | 0.30 | 0.45 | 0.50 |
| Terminal-to-Exposed-Pad | K | - | 0.60 | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

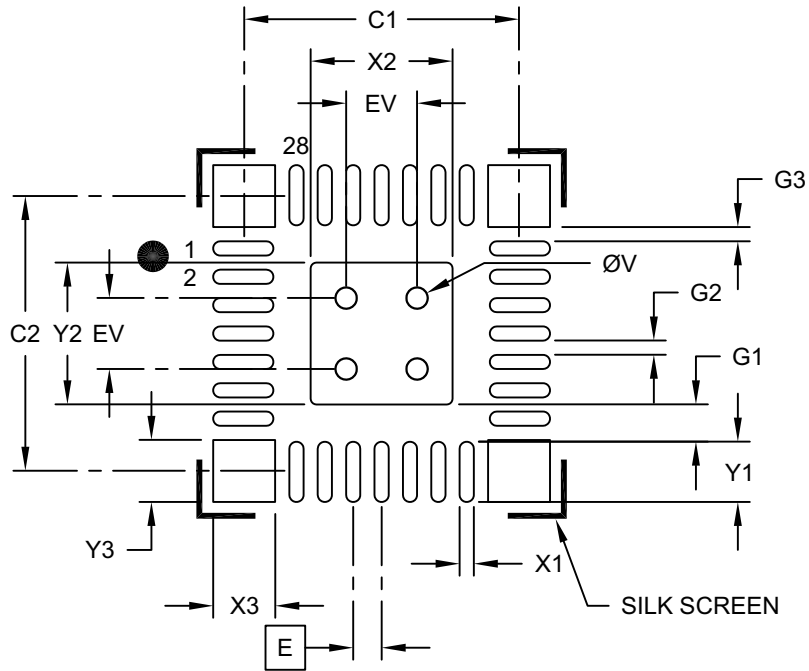
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-333-M6 Rev A Sheet 2 of 2

PIC32MM0064GPL036 FAMILY

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|---------------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.40 BSC | | |
| Center Pad Width | X2 | | | 2.00 |
| Center Pad Length | Y2 | | | 2.00 |
| Contact Pad Spacing | C1 | | 3.90 | |
| Contact Pad Spacing | C2 | | 3.90 | |
| Contact Pad Width (X28) | X1 | | | 0.20 |
| Contact Pad Length (X28) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (X28) | G1 | | 0.52 | |
| Contact Pad to Pad (X24) | G2 | 0.20 | | |
| Contact Pad to Corner Pad (X8) | G3 | 0.20 | | |
| Corner Anchor Width (X4) | X3 | | | 0.78 |
| Corner Anchor Length (X4) | Y3 | | | 0.78 |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

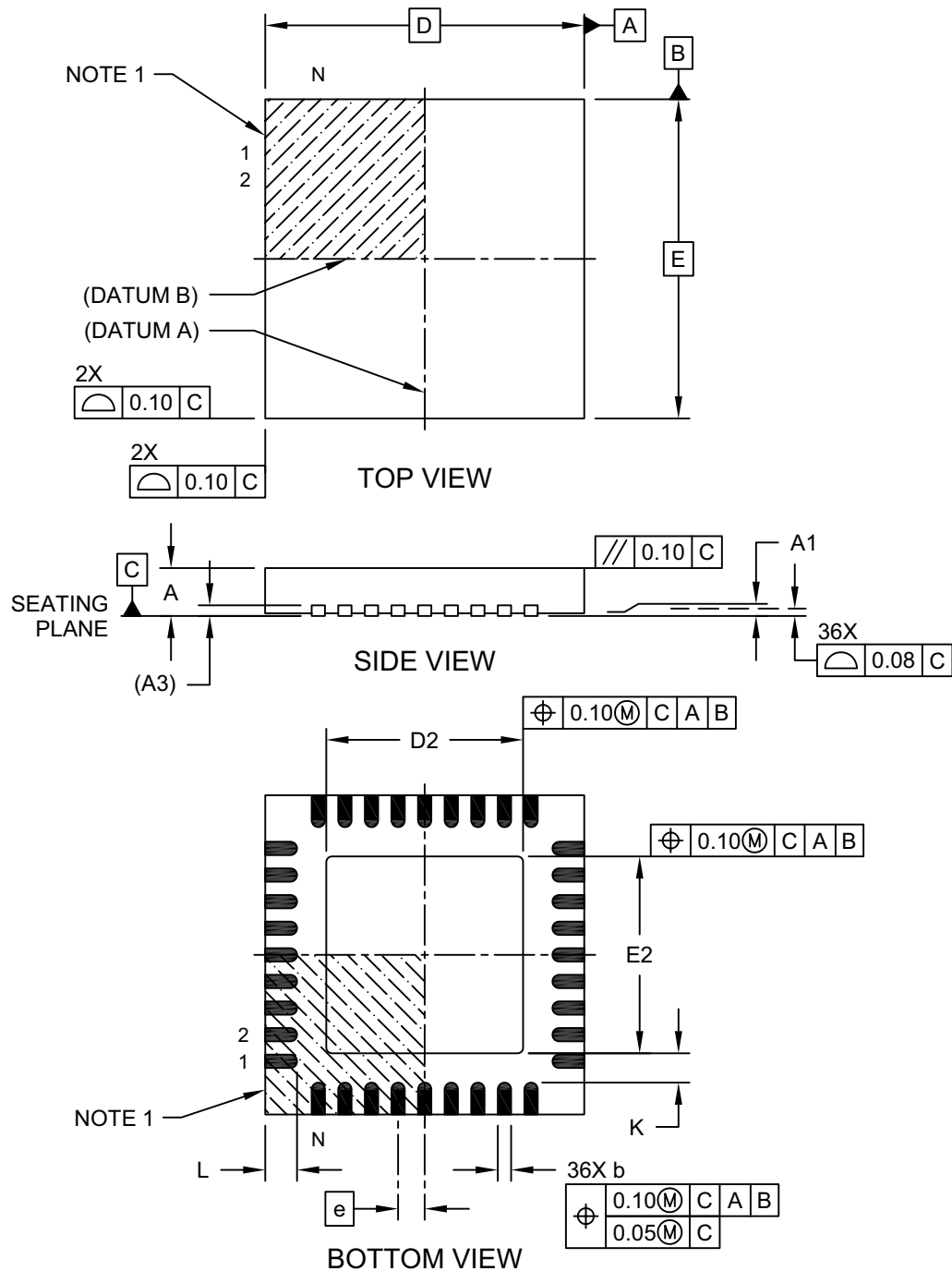
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2333-M6 Rev B

PIC32MM0064GPL036 FAMILY

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

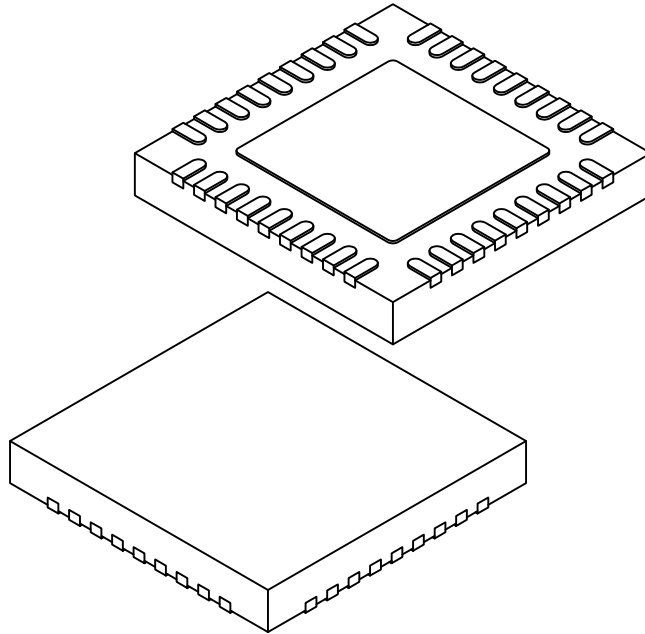


Microchip Technology Drawing C04-272B-M2 Sheet 1 of 2

PIC32MM0064GPL036 FAMILY

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Terminals | N | 36 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.20 REF | | |
| Overall Width | E | 6.00 BSC | | |
| Exposed Pad Width | E2 | 3.60 | 3.70 | 3.80 |
| Overall Length | D | 6.00 BSC | | |
| Exposed Pad Length | D2 | 3.60 | 3.70 | 3.80 |
| Terminal Width | b | 0.18 | 0.25 | 0.30 |
| Terminal Length | L | 0.50 | 0.60 | 0.75 |
| Terminal-to-Exposed-Pad | K | 0.45 | 0.55 | - |

Notes:

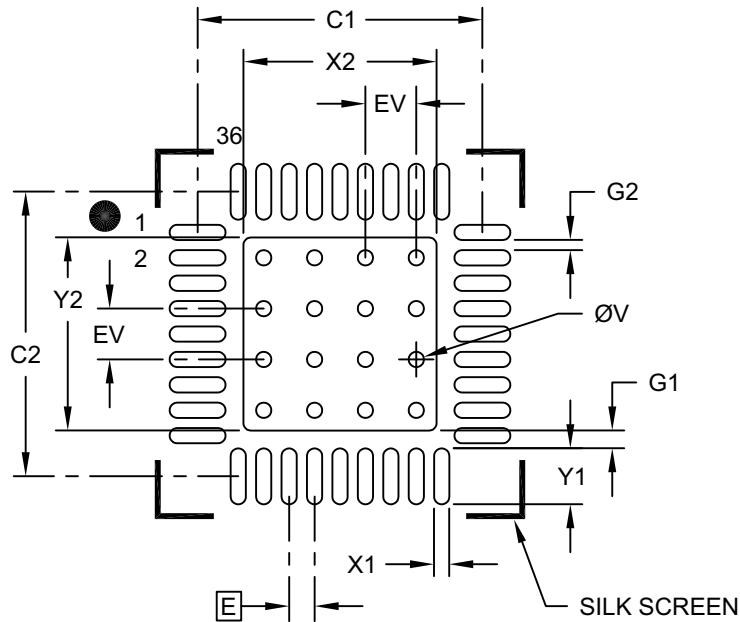
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-272B-M2 Sheet 2 of 2

PIC32MM0064GPL036 FAMILY

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x0.9 mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | X2 | | | 3.80 |
| Optional Center Pad Length | Y2 | | | 3.80 |
| Contact Pad Spacing | C1 | | 5.60 | |
| Contact Pad Spacing | C2 | | 5.60 | |
| Contact Pad Width (X36) | X1 | | | 0.30 |
| Contact Pad Length (X36) | Y1 | | | 1.10 |
| Contact Pad to Center Pad (X36) | G1 | 0.35 | | |
| Space Between Contact Pads (X32) | G2 | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

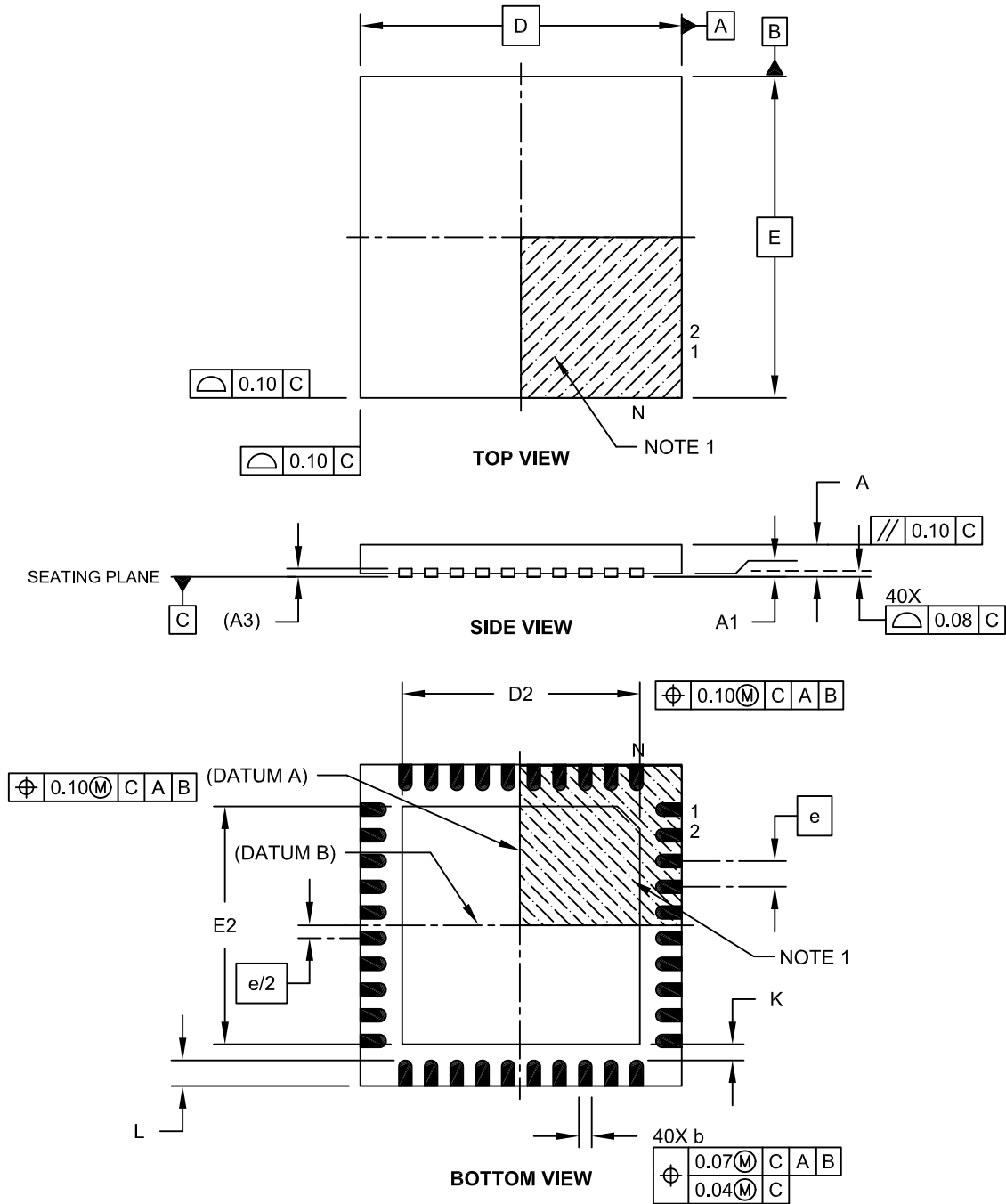
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2272B-M2

PIC32MM0064GPL036 FAMILY

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

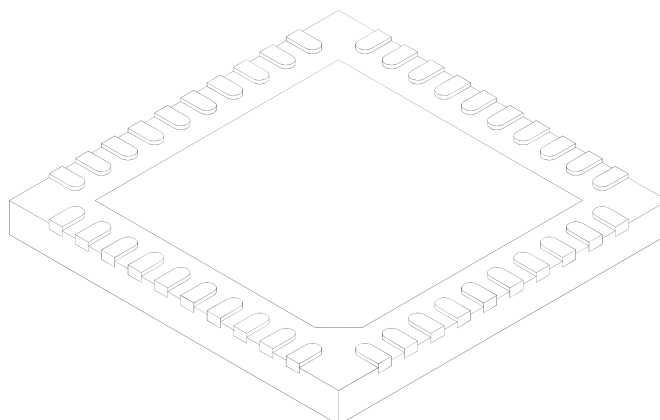


Microchip Technology Drawing C04-156A Sheet 1 of 2

PIC32MM0064GPL036 FAMILY

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 40 | | |
| Pitch | e | 0.40 BSC | | |
| Overall Height | A | 0.45 | 0.50 | 0.55 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.127 REF | | |
| Overall Width | E | 5.00 BSC | | |
| Exposed Pad Width | E2 | 3.60 | 3.70 | 3.80 |
| Overall Length | D | 5.00 BSC | | |
| Exposed Pad Length | D2 | 3.60 | 3.70 | 3.80 |
| Contact Width | b | 0.15 | 0.20 | 0.25 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

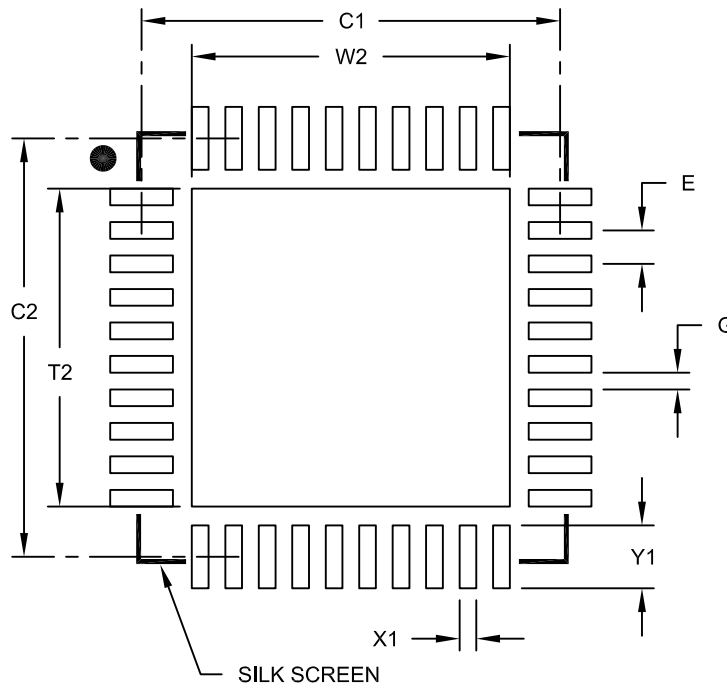
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-156A Sheet 2 of 2

PIC32MM0064GPL036 FAMILY

40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.40 BSC | | |
| Optional Center Pad Width | W2 | | | 3.80 |
| Optional Center Pad Length | T2 | | | 3.80 |
| Contact Pad Spacing | C1 | | 5.00 | |
| Contact Pad Spacing | C2 | | 5.00 | |
| Contact Pad Width (X40) | X1 | | | 0.20 |
| Contact Pad Length (X40) | Y1 | | | 0.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2156B

APPENDIX A: REVISION HISTORY

Revision A (February 2015)

This is the initial version of the document.

Revision B (May 2016)

This revision incorporates the following updates:

- Registers:
 - Updates Register 5-1, Register 5-3, Register 5-6, Register 5-7, Register 6-3, Register 6-4, Register 7-2, Register 8-2, Register 8-3, Register 8-5, Register 8-6, Register 11-1, Register 13-1, Register 14-1, Register 15-1, Register 15-5, Register 15-6, Register 16-1, Register 16-2, Register 16-3, Register 16-5, Register 18-2, Register 19-1, Register 19-2 and Register 23-7
- Tables:
 - Updates Table 1-1, Table 5-1, Table 6-1, Table 7-2, Table 7-3, Table 9-3, Table 9-7, Table 15-1, Table 16-1, Table 19-1, Table 22-1, Table 23-4, Table 23-5, Table 26-2, Table 26-3, Table 26-4 and Table 26-6 through Table 26-33
 - Adds Table 23-8
- Figures:
 - Updates Figure 1-1, Figure 3-1, Figure 8-1, Figure 10-1, Figure 14-1, Figure 13-1, Figure 14-1, Figure 14-1, Figure 15-1, Figure 17-1, Figure 18-1, Figure 18-3, Figure 26-1, Figure 26-3, Figure 26-4, Figure 26-9, Figure 26-10, Figure 26-11 and Figure 26-12
- Updates pin function descriptions in **Section 1.0 “Device Overview”**
- Updates text in **Section 9.6 “Input Change Notification (ICN)”**, **Section 9.8.4 “Input Mapping”**, **Section 23.7 “Unique Device Identifier (UDID)”**, **Section 22.5 “Low-Power Brown-out Reset”** and **Section 27.0 “Packaging Information”**
- Adds **Section 5.1 “Flash Controller Registers Write Protection”**, **Section 8.0 “Oscillator Configuration”**, **Section 23.4 “System Registers Write Protection”**, reference to **Section 22.1 “Sleep Mode”**, **Section 22.2 “Idle Mode”** and **Section 23.8 “Reserved Registers”**
- Updates the Absolute Maximum Ratings in **Section 26.0 “Electrical Characteristics”**

This revision also includes minor typographical and formatting changes throughout the data sheet text.

Revision C (April 2018)

This revision incorporates the following updates:

Adds +125°C specifications.

- Sections:
 - Updates **“Operating Conditions”**, **“Peripheral Features”** and **“Analog Features”** on the first two pages.
 - Updates **Section 2.5 “Voltage Regulator Pin (V_{CAP})”**, **Section 9.5 “I/O Port Write/Read Timing”**, **Section 12.1 “Introduction”** and **Section 26.0 “Electrical Characteristics”**.
 - Adds **Section 9.2 “Parallel I/O (PIO) Ports”**.
- Tables:
 - Updates Table 8-1, Table 26-1, Table 26-3, Table 26-4, Table 26-5, Table 26-6, Table 26-7, Table 26-8, Table 26-9, Table 26-10, Table 26-11, Table 26-12, Table 26-13, Table 26-14, Table 26-15, Table 26-17, Table 26-18, Table 26-19, Table 26-20, Table 26-21, Table 26-22, Table 26-23, Table 26-24, Table 26-25, Table 26-26, Table 26-27, Table 26-28, Table 26-29, Table 26-30, Table 26-31, Table 26-32 and Table 26-33.
- Registers:
 - Updates Register 5-7, Register 6-3, Register 8-1, Register 8-3, Register 11-1, Register 12-1, Register 15-1 and Register 16-1.
 - Adds Register 8-2.
- Figures:
 - Updates Figure 8-2.
- Examples:
 - Adds Example 11-1.
 - Updates Example 8-1.

PIC32MM0064GPL036 FAMILY

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PIC32MM0064GPL036 FAMILY

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PIC32MM0064GPL036 FAMILY

NOTES:

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Technical support is available through the web site at: <http://microchip.com/support>

PIC32MM0064GPL036 FAMILY

NOTES:

PIC32MM0064GPL036 FAMILY

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| | PIC32 | MM | XXXX | GP | L | XXX | T - XXX |
|------------------------------------|-------|----|------|-------|-------|-------|---------|
| Microchip Brand | _____ | | | | | | |
| Architecture | _____ | | | | | | _____ |
| Flash Memory Size | _____ | | | _____ | _____ | _____ | _____ |
| Family | _____ | | | | _____ | _____ | _____ |
| Key Feature Set | _____ | | | | | _____ | _____ |
| Pin Count | _____ | | | | | | _____ |
| Tape and Reel Flag (if applicable) | _____ | | | | | | |
| Pattern | _____ | | | | | | |

| | |
|-------------------|--|
| Architecture | MM = MIPS32 [®] microAptiv™ UC CPU Core |
| Flash Memory Size | 0016 = 16 Kbytes 0032 = 32 Kbytes 0064 = 64 Kbytes |
| Family | GP = General Purpose Family |
| Key Feature | L = Up to 25 MHz operating frequency with basic peripheral set of 2 UART and 2 SPI modules |
| Pin Count | 020 = 20-pin 028 = 28-pin 036 = 36/40-pin |
| Pattern | Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample |

Example:
 PIC32MM0064GPL036-I/M2:
 PIC32 General Purpose Device with MIPS32[®] microAptiv™ UC Core, 64-Kbyte Program Memory, 36-Pin Package.

PIC32MM0064GPL036 FAMILY

NOTES:

Note the following details of the code protection feature on Microchip devices:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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