CEC173x

Real Time Platform Root of Trust Controllers

Operating Conditions

- Operating Voltage: 3.3 V
- Interface Voltages: 3.3 V and optional 1.8 V SPI
- Operating Temperature Range: -40 °C to 85 °C

Low Power Modes

- Chip is designed to always operate in Lowest Power state during Normal Operation
- Supports 2 Chip-level Sleep Modes: Light Sleep and Heavy Sleep
  - Low Standby Current in Sleep Modes

ARM® Cortex-M4F Embedded Processor

- Programmable clock frequency up to 96 MHz
- Floating point processor
- Single 4GByte Addressing Space
- Nested Vectored Interrupt Controller (NVIC)
  - Maskable Interrupt Controller
  - Maskable hardware wake up events
  - 8 Levels of priority, individually assignable by vector
- EC Interrupt Aggregator expands number of Interrupt sources supported or reduces number of vectors needed
- Complete ARM® Standard debug support
  - JTAG-Based DAP port, comprised of SWJ-DP and AHB-AP debugger access functions
- MPU Feature (Memory Protection Unit)

Memory Components

- SRAM 384 KB Total
  - Code: 320 KB; Data: 64 KB
  - Two independent partitions allow for execution with no wait states
- 8Kbit One Time Programmable (OTP) Memory
  - In circuit programmable without additional BOM components
- ROM
  - Contains Boot ROM
  - Contains Real Time APIs for built-in functions
- In-package SPI Serial Flash
  - 2MBytes for 64-pin Single SPI Channel
  - 4MBytes for 84-pin Dual SPI Channel

Clocks

- 96 MHz Internal PLL
- Internal 32 kHz silicon oscillator clock source

Package Options

- 84-pin WFBGA, dual SPI channel monitors
- 64-pin VFBGA, single SPI channel monitor

Security Features

- Boot ROM Secure Boot Loader
  - CNSA Compliant (SHA-384/ECC384)
  - Meets NIST 800-193 PFR Guidelines
  - Supports 2 Code Images in internal SPI Flash (Primary and Fall-back image)
  - Authenticates SPI Flash image before loading
  - Support AES-256 Encrypted SPI Flash images
- SPI Boot Flash Monitoring and Intervention
  - Dual Channel: BMC and CPU (in 84-pin)
  - Allows 50 MHz operation of SPI Flash
  - Real Time load module verification and execution path matching during Host boot
  - Prevents unauthorized Read/Write/Erase during Host runtime
  - Isolates Host from Flash devices using internal QSPI Analog switches
  - Each SPI Monitor block has its own 64KB Match patterns for comparison with SPI Channel data
  - Performs Hash calculation on 8KB match region
- Hardware Accelerators:
  - Multi purpose AES Crypto Engine:
    - Support for 128-bit - 256-bit key length
  - Cryptographic Hash Engine
    - SHA-2: SHA-256, SHA-384, SHA-512
  - Public Key Crypto Engine
    - Hardware support for RSA and Elliptic Curve asymmetric public key algorithms
    - RSA keys length of 1024 to 4096 bits
    - ECC Prime Field keys up to 521 bits
    - ECC Binary Field keys up to 571 bits
    - Microcoded support for standard public key algorithms
      - ECDSA
      - KC-ECDSA
      - Ed25519
- Hardware Physically Unclonable Function (PUF)
  - Supports up to ECC384/P-384 key size

- OTP for storing Keys and IDs
  - Lockable on 32 Byte boundaries to prevent read access or write access
- Deterministic Random Number Generator
  - Includes True Random Number Generator, conditioning and health tests
    - Compliant with NIST SP800-90B test suites
  - 1K-bit FIFO
- JTAG Disabled by default
- Tamper Protection Countermeasures
  - Temperature
  - Voltage
  - Side channel power
- TCG DICE Compliant
  - DICE in immutable code (ROM)
  - Generates DICE CDI

System Host Interface

- Two Serial Peripheral Interface (SPI) Host Controllers
  - Dual and Quad I/O Support
  - Flexible Clock Rates
  - Support for 1.8V and 3.3V Target Devices
  - SPI Burst Capable
  - SPI Controller Operates with Internal DMA Controller with CRC Generation
- Two QSPI Analog Switches
- Two SPI Peripheral Target Modules
  - Single / Quad Wire and Mode 0 / Mode 3 transfers
  - Standalone 8,16, 32 bit or up to 8 DWord block read/write memory accesses
  - Memory Access Window of 256 – 64K bytes
  - Interrupt pin to SPI Host
  - Wake capable

Peripheral Features

- Internal DMA Controller
  - Hardware or Firmware Flow Control
  - Firmware Initiated Memory-to-Memory transfers
  - Hardware CRC-32 Generator on Channel 0
  - 10 Hardware DMA Channels Support the 14 internal SMBus Host/Target Controllers and internal SPI Controllers
- I2C/SMBus Controllers
  - Five I2C/SMBus controllers
  - Six Configurable I2C ports
    - Full Crossbar switch allows any port to be connected to any controller
  - Supports Promiscuous mode of operation
  - Fully Operational on Standby Power
  - Multi-Host Capable
  - Supports Clock Stretching
  - Programmable Bus Speeds
  - 1 MHz Capable
  - Supports DMA Network Layer
- General Purpose I/O Pins
  - Inputs
    - Asynchronous rising and falling edge wakeup detection Interrupt High or Low Level
  - Outputs:
    - Push Pull or Open Drain output
    - Programmable power well emulation
  - Pull up or pull down resistor control
    - Automatically disabling pull-up resistors when output driven low
    - Automatically disabling pull-down resistors when output driven high
  - Programmable drive strength
  - Two separate1.8V/3.3V configurable IO regions
  - Group or individual control of GPIO data
  - Glitch protection and Under-Voltage Protection on all GPIO pins
- Universal Asynchronous Receiver Transmitter (UART)
  - One 2-pin High Speed NS16C550A Compatible UART with Send/Receive 16-Byte FIFOs
  - Programmable Main Power or Standby Power Functionality
  - Standard Baud Rates to 115.2 Kbps, Custom Baud Rates to 1.5 Mbps
- One Programmable Pulse Width Modulator (PWM) output
  - Multiple Clock Rates
  - 16-Bit ON & 16-Bit OFF Counters
- Breathing LED Interface
  - Two Blinking/Breathing LEDs
  - Programmable Blink Rates
  - Piecewise Linear Breathing LED Output Controller
    - Provides for programmable rise and fall waveforms
  - Operational in EC Sleep States

Timers

- Capture and Compare timer
  - 32-bit Free-running timer
  - Nine 32-bit Capture Registers
  - Compare and Overflow Interrupts
- Programmable Timer Interface
  - Two 16-bit Auto-reloading Timer Instances
    - 16 bit Pre-Scale divider

  - Halt and Reload control
  - Auto Reload
- Two 32-bit Auto-reloading Timer Instances
  - 16 bit Pre-Scale divider
  - Halt and Reload control
  - Auto Reload
- Three Operating Modes per Instance: Timer (Reload or Free-Running) or One-shot.
  - Event Mode is not supported

- 32-bit RTOS Timer
  - Runs Off 32kHz Clock Source
  - Continues Counting in all the Chip Sleep States regardless of Processor Sleep State
  - Counter is Halted when Embedded Controller is Halted (e.g., JTAG debugger active, break point)
  - Generates wake-capable interrupt event
- Watch Dog Timer (WDT)
  - Watchdog reset IRQ vector
- Hibernation Timer Interface
  - Two 32.768 KHz Driven Timers
  - Programmable Wake-up from 0.5ms to 128 Minutes

Debug Features

- 2-pin Serial Wire Debug (SWD) interface
  - SWD I/F debugger and programmer
- 4-Pin JTAG interface for Boundary Scan
- Trace FIFO Debug Port (TFDP)

Terms and Abbreviations

The following terms are used in this document:

- Boot ROM - The boot ROM is the name given to the immutable bootloader code stored in ROM. The boot ROM is the first code executed any time the embedded processor is reset (for example, Power-on-Reset, WDT Event, and so on). The CEC173x boot ROM is a secure bootloader that may be used as a root of trust in a system.
- EC - Embedded Controller. CEC173x is an embedded controller.
- EC_FW-EC Firmware. The EC_FW is a mutable code stored in external Flash memory and loaded into the EC's SRAM memory by a bootloader. This code is executed when the bootloader jumps into this code.
- FMC - First Mutable Code. The FMC is the EC firmware loaded by the boot ROM.
- POR - Power-on-Reset
- RESET_SYS - Used to reset the processor and all VTR powered logic as defined in the CEC173x Data Sheet. May be triggered by a VTR POR and non-POR reset events.
- SMB/I^2C Initiator - An initiator issues commands, generates the clocks, and terminates the transfer.
- SMB/I^2C Target - A target device responds to its own address and receives commands.

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1.0 GENERAL DESCRIPTION

The CEC173x Trust Shield Family is the Real Time Platform Root of Trust Controller for Servers, Telecommunications, Networking, Industrials, and Embedded Computing. The CEC173x is a highly-configurable, mixed-signal, advanced I/O controller. It contains a 32-bit 96 MHz ARM® Cortex-M4 processor core with closely-coupled memory for optimal code execution and data access. The immutable Boot ROM, embedded in the design, is used to store the power on/boot sequence and APIs available during run time. When VTR_REG power is applied to the device, the secure boot loader API is used to download the firmware image from internal Flash storage. Programming capability for this Flash is provided by various means, thereby allowing system designers to customize the device's behavior while maintaining the integrity of the image by cryptographic signatures.

The CEC173x device is directly powered by a Suspend supply plane (VTR_REG and VTR_ANALOG) and uses two independent runtime power wells (VTR1 and VTR2) as power for mediating accesses between two independent Host processors and their SPI Flash boot devices. The two banks of I/O pins powered by VTR1 and VTR2 operate at either 3.3V or 1.8V, as dictated by the Host and the type of Flash devices selected.

The CEC173x's SPI Flash Monitor blocks, one instance per Host, maintain Host firmware integrity both during Host Boot and Host Runtime.

At Host Boot, it calculates and verifies signatures of the loaded code blocks in real time, while also verifying that the Host's firmware at this time is executing the correct opcodes from Flash.

At Host Runtime, it verifies that only legal Flash accesses are performed, using regional access permission settings, and that no illegal or questionable opcodes (such as Chip Erase) are attempted. Upon seeing an attempted violation of SPI integrity or access rules, it will intervene in real time, in such a way as to cancel a Read, Write, Program or Erase before it can be performed. The Intervention technique works with even the most economical 8-pin standard NOR Flash devices.

The CEC173x also contains, separately, a core Crypto hardware accelerator engine supporting SHA-384,128-bit and 256-bit AES encryption, ECDSA and EC_KCDSA signing algorithms, RSA and Elliptic asymmetric public key algorithms, and a Deterministic Random Number Generator (DRNG). Runtime APIs are provided in the ROM for customer application code to use the cryptographic hardware.

PUF ID generation resources and algorithms are included, as well as lockable OTP storage for keys and IDs. Fused Life Cycle security gives access to these resources only when appropriate for development, test or production phases.

The CEC173x is designed to be incorporated into low power designs. During normal operation, the hardware always operates in the lowest power state for a given configuration. The chip power management logic offers two low power states: light sleep and heavy sleep. When the chip is sleeping, it has many wake events that can be configured to return the device to normal operation, for example any GPIO pin.

The CEC173x offers a software development system interface that includes a Trace FIFO Debug port, serial debug port (UART) and a 2-pin Serial Wire Debug (SWD) interface. Also included is a full 4-wire JTAG interface for Boundary Scan testing (disabled for production).

The immutable secure bootloader implemented in the CEC173x ROM (Boot ROM) loads and authenticates the embedded controller firmware (EC_FW) from the internal SPI Flash. The validated EC_FW along with the Boot ROM code supports many additional security features of the device, including Key Revocation, Code Rollback Protection and Transfer of Ownership. In addition, the Boot ROM implements Life Cycle Management and the EC_FW implements SPDM for Attestation. The SPDM implementation in EC_FW supports commands that return certificates and measurement information for attestation. A platform RoT in the system will act as a Requester to verify the authenticity of the CEC173x.

Both the Boot ROM and the EC_FW support more than one public key for image authentication and key revocation. A public key may be revoked, i.e., taken out of service, if the private key becomes compromised.

The Boot ROM and the EC_FW also support Rollback Protection, which prevents certain firmware images from being permitted to run in a system. This feature is used if an older image version may compromise the system security.

The Boot ROM and Soteria-G3 support Transfer of Ownership of the platform.

The Life Cycle of the CEC173x is managed by the Boot ROM using OTP bits to keep track of the life cycle mode of the device.

TABLE 1-1: CEC173X FEATURE LIST

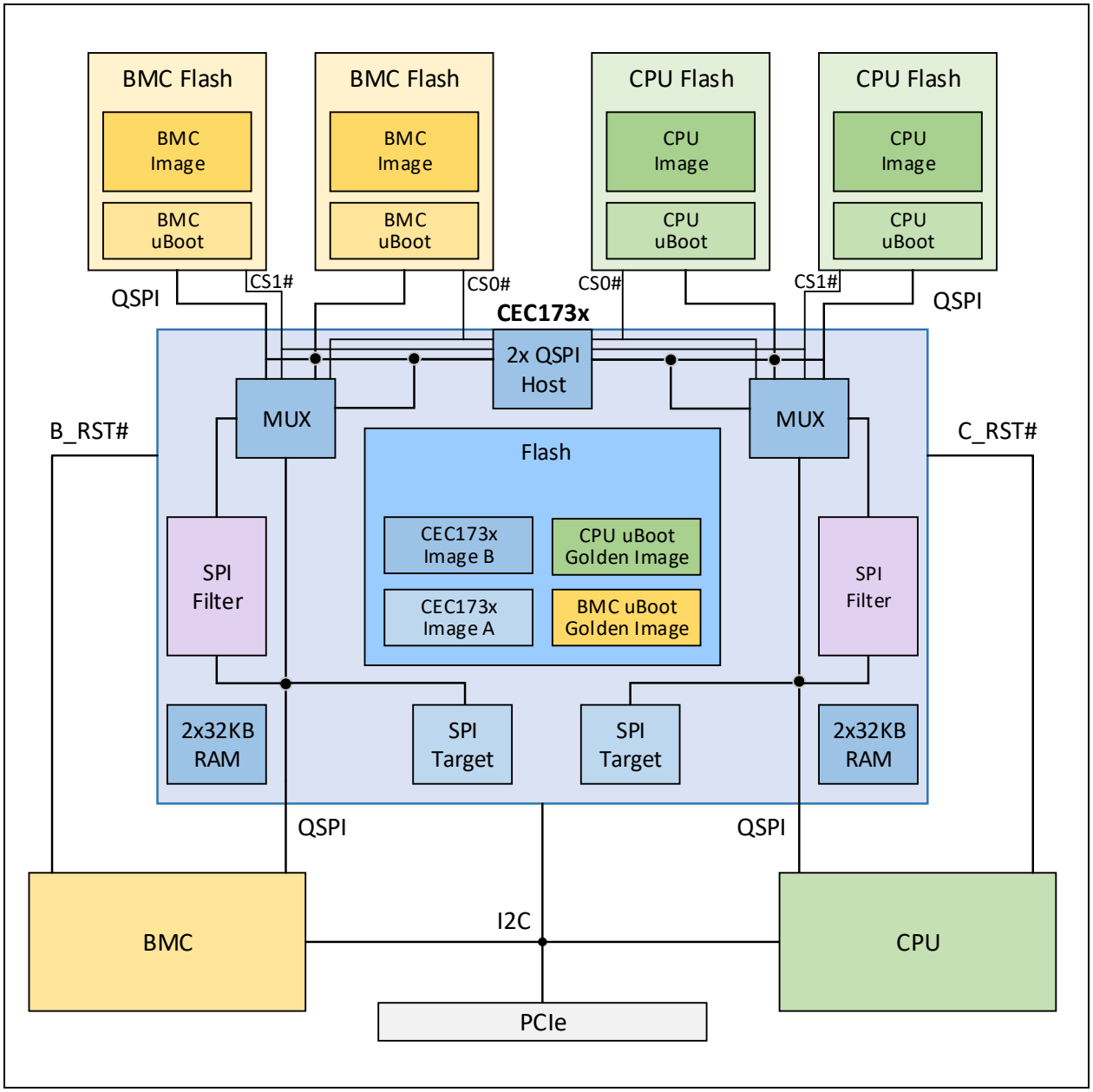
Feature	64-Pin CEC1734-S0-I/2HW CEC1736-S0-I/2HW	84-Pin CEC1734-S0-I/2ZW CEC1736-S0-I/2ZW
Package	**2HW (1 SPI Monitor)**	**2ZW (2 SPI Monitor)**
Device ID - CEC1734 MainID_SubID_RevID Device ID - CEC1736 MainID_SubID_RevID	0024_32_xx h 0024_21_xx h	0024_52_xx h 0024_41_xx h
JTAG ID	02252445h	02252445h
Total General Purpose SRAM	384KB	384KB
General Purpose SRAM Code/Data (Primary Use)	320KB / 64KB	320KB / 64KB
PUF for key generation, capable of locking 1KB of SRAM individually	2 x 1KB	2 x 1KB
Dedicated SRAM for Matching (SPI-Flash Monitoring)	1 x 64KB	2 x 64KB
Integrated SPI Flash Device	2MByte	4MByte
Integrated EMC Hardware Monitor (for Tampers)	Yes	Yes
SPI-Flash Monitor with Active Intervention	Single	Dual
Secure Boot - Authentication and Decryption	Yes	Yes
Trace FIFO Debug Port	1	1
Internal DMA Channels	10	10
16-bit/32-bit Basic Timer	2	2
Capture Timer	1	1
ICT Channels (Input Capture/Compare Timer)	9	9
Compare Timer	1	1
Watchdog Timer (WDT)	1	1
Hibernation Timer	2	2
RTOS Timer	1	1
SMB/I2C Host Controllers - up to 1 MHz	5	5
SMB/I2C Ports	6	6
Blinking/Breathing LED	2	2
PWM	1	2
GPIO functionality multiplexed on pins	52	71
Quad Mode SPI Host Controller (QMSPI)	1	2
Either QMSPI Host selectable to drive Internal Flash	1	1
SPI Target Controllers, one per SPI Host	2	2
SPI Flash Analog MUX / Isolation	1	2
UART	1, 2-pin	1, 2-pin
JTAG	4pin / 2pin	4pin / 2pin
Boundary Scan	Yes	Yes
AES Hardware Support	Yes	Yes
• AES-GCM	Yes	Yes
SHA-2 Hashing Support, Core Crypto SHA256, SHA384, SHA512	1	1
SHA-2 Hashing Support, SPI Monitors SHA256, SHA384	1	2
Public Key Cryptography Support	Yes	Yes
Deterministic Random Number Generator	Yes	Yes
• Includes TRNG, health tests and conditioning	Yes	Yes
Generate Public/Private key pairs	Yes	Yes
PUF Support in Boot ROM	Yes	Yes

TABLE 1-1: CEC173X FEATURE LIST (CONTINUED)

Feature	64-Pin CEC1734-S0-I/2HW CEC1736-S0-I/2HW	84-Pin CEC1734-S0-I/2ZW CEC1736-S0-I/2ZW
Package	**2HW (1 SPI Monitor)**	**2ZW (2 SPI Monitor)**
OTP	8k bits	8k bits
• In circuit OTP programming	Yes	Yes
• Fused device life cycle stages, from Google OpenTitan spec	Yes	Yes
Tamper Protection Countermeasures	Yes	Yes
• Temperature	Yes, CEC1736	Yes, CEC1736
• Voltage	Yes, CEC1736	Yes, CEC1736
• Side Channel Power	Yes	Yes
TCG DICE Compliant	Yes	Yes
• DICE in immutable code	Yes	Yes
• Generate DICE UDS	Yes	Yes
Key Revocation	Yes	Yes
Code Rollback Protection	Yes	Yes
Transfer of Ownership	Yes	Yes
Life Cycle Management	Yes	Yes
SPDM support for Attestation	Yes	Yes

1.1 BLOCK DIAGRAM

FIGURE 1-1: SYSTEM BLOCK DIAGRAM - SERVER APPLICATION



2.0 PIN CONFIGURATION

2.1 Description

The Pin Configuration chapter includes Pin List, Pin Multiplexing and Package Information.

2.2 Terminology and Symbols for Pins/Buffers

2.2.1 BUFFER TERMINOLOGY

Term	Definition
#	The '#' sign at the end of a signal name indicates an active-low signal
n	The lowercase 'n' preceding a signal name indicates an active-low signal
PWR	Power
PIO	Programmable as Input, Output, Open Drain Output, Bi-directional or Bi-directional with Open Drain Output. **Note:** GPIO pin drive strength is determined by the Pin Control Register Defaults field in the Pin Control Register 2. • PIO (12mA): Configurable drive strength from 2ma to 12ma **Note:** PIO (12mA) GPIO pins are indicated in the tables in Section 2.4.11, "Pin Multiplexing" as PIO with 12mA in the "Drive strength" column. • PIO (24mA): Configurable drive strength from 4ma to 24ma. **Note:** PIO (24mA) GPIO pins are indicated in the tables in Section 2.4.11, "Pin Multiplexing" as PIO with 24mA in the "Drive strength" column.
I	Input Buffer.
O	Output Buffer. Strength is taken from the PIO entry on the same pin.
Q-SW	Connected via a Q Switch isolator to another pin. See Section 2.4.13, "Q-Switch Pins"
VTR1	Input/Output pins that operate at the SPI0 bus voltage level (SPI Channel 0), which may be at 3.3V or 1.8V nominal.
VTR2	Input/Output pins that operate at the SPI1 bus voltage level (SPI Channel 1), which may be at 3.3V or 1.8V nominal. These pins are not available in the smaller, single-channel packages.
VTR_REG	These pins operate at the core 3.3V nominal voltage level (VTR_REG).

2.2.2 PIN NAMING CONVENTIONS

- Pin Name is composed of the multiplexed options separated by '/'. E.g., GPIOxxxx/SignalA/SignalB.
- The first signal shown in a pin name is the default signal. E.g., GPIOxxxx/SignalA/SignalB means the GPIO is the default signal.
- Square brackets '[ ]' are used to indicate there is a Strap Option on a pin, used by the Boot ROM. This is always shown as the last signal on the Pin Name.
- Function names suffixed with a numeric value indicate the Instance Number. E.g., PWM0, PWM1, etc. indicates that PWM0 is the PWM output for PWM Instance 0, PWM1 is the PWM output for PWM Instance 1, etc. The instance number may be omitted if there in only one instance of the IP block implemented.
- Function names starting with "JTAG_" are selected by the JTAG_RST# pin, which will override other programmed settings.

2.3 Pin List

Note 1: The GPIO253 pin is reserved for TST_CLK_OUT. A pull-down resistor is required on this pin; recommend 10k ohm.

- This pin is configured by default to GPIO input (disabled), interrupt disabled state after a RESET_SYS event. It is then reconfigured by chip-level setup in the Boot ROM to enable the pull-down on this pin.

2: It is recommended to enable the internal pull up resistor on GPIOs that have an external pullup to ensure minimum voltage at the pad pin during power up. This is done using the PU/PD (PU_PD) bits in the Pin Control Registers.

TABLE 2-1: CEC1734 PINOUT

CEC1734-S0-I/2HW	CEC1734 Signal Name
E2	GPIO000/SPI0_KILL/SPI0_RESET#
F9	GPIO002/QSPI0_CS1#/SPIMON_QSPI0_CS1#
J2	GPIO003/I2C00_SDA(FATAL_ERROR#)
G2	GPIO004/I2C00_SCL
J3	GPIO012(EXTRST#)
K7	GPIO013/SP1_ALT_IO3
F2	GPIO015/ICT10[BSTRAP]
D10	GPIO016/QSPI0_IO3/QSPI0_IO3_CLAMP
G9	GPIO020/QSPI0_IN_CS0#
D9	GPIO021/QSPI0_IN_CS1#
A7	GPIO022/QSPI0_IN_IO1
A8	GPIO023/QSPI0_IN_IO0
A4	GPIO026/SP0_AP_INTR[I2C_ADDR0]
K2	GPIO027/ALT_TFDP_CLK
D1	GPIO030/I2C10_SDA
G1	GPIO031/SP1_ALT_IO0
F1	GPIO034/SP1_AP_INTR[I2C_ADDR1]
C2	GPIO046/SP1_ALT_CS#
K3	GPIO047/SP1_ALT_IO1
H2	GPIO050/ICT0
J5	GPIO053/PWM0
E9	GPIO055/QSPI0_CS0#/SPIMON_QS-PI0_CS0#(QSPI0_PWRGD)
B9	GPIO056/QSPI0_CLK/QSPI0_CLK_CLAMP
J4	GPIO057/VCC_PWRGD
H1	GPIO063/SP1_ALT_CLK
K5	GPIO104/UART0_TX/TFDP_CLK
J6	GPIO105/UART0_RX/TFDP_DATA
K6	GPIO106/AP0_RESET#(AP0_RESET#)
E1	GPIO107/I2C10_SCL/ALT_VIOL_0
K8	GPIO112/ALT_VIOL_1/ALT_TFDP_DATA
J7	GPIO127/SP1_ALT_IO2
J1	GPIO130/32KHZ_IN
D2	GPIO132/I2C06_SDA
C1	GPIO140/I2C06_SCL

TABLE 2-1: CEC1734 PINOUT

CEC1734-S0-I/2HW	CEC1734 Signal Name
A2	GPIO143/I2C04_SDA
A3	GPIO144/I2C04_SCL(REMOTE_ACCESS)
B4	GPIO145/I2C09_SDA/JTAG_TDI
B2	GPIO146/I2C09_SCL/ITM/JTAG_TDO(SWV)
B1	GPIO147/I2C15_SDA/JTAG_CLK (SWDCLK)
B3	GPIO150/I2C15_SCL/JTAG_TMS (SWDIO)
J10	GPIO156/LED0
G10	GPIO157/LED1
J8	GPIO170[JTAG_STRAP]
J9	GPIO201/32KHZ_OUT[CR_FLASH]
C9	GPIO202/QSPI0_IN_IO2
E10	GPIO203/QSPI0_IN_IO3
B10	GPIO204/QSPI0_IN_CLK
A6	GPIO223/QSPI0_IO0/QSPI0_IO0_CLAMP
A9	GPIO224/QSPI0_IO1/QSPI0_IO1_CLAMP
B7	GPIO227/QSPI0_IO2/QSPI0_IO2_CLAMP
C10	GPIO250/SPI0PER_CS#
B6	GPIO253/TST_CLK_OUT
H9	JTAG_RST#
H10	nRESET_IN
G4	VSS_ANALOG
K9	VTR_PLL
D7	VSS
G7	VTR_REG
B8	VTR1
D4	VTR_ANALOG
K4	VR_CAP
A5	VSS
F10	VSS
B5	VSS

TABLE 2-2: CEC1734 PINOUT

CEC1734-S0-I/2ZW	CEC1734 Signal Name
A4	GPIO000/SPI0_KILL/SPI0_RESET#
J2	GPIO002/QSPI0_CS1#/SPIMON_QSPI0_CS1#
C6	GPIO003/I2C00_SDA(FATAL_ERROR#)
C1	GPIO004/I2C00_SCL
D6	GPIO012(EXTRST#)
F2	GPIO013/SP1_ALT_IO3
B3	GPIO015/ICT10[BSTRAP]
K4	GPIO016/QSPI0_IO3/QSPI0_IO3_CLAMP
K1	GPIO020/QSPI0_IN_CS0#
J3	GPIO021/QSPI0_IN_CS1#

TABLE 2-2: CEC1734 PINOUT

CEC1734-S0-I/2ZW	CEC1734 Signal Name
J7	GPIO022/QSPI0_IN_IO1
E9	GPIO023/QSPI0_IN_IO0
F7	GPIO024/SPI1PER_CS#
A10	GPIO026/SP0_AP_INTR[I2C_ADDR0]
D5	GPIO027/TFDP_CLK_ALT
B6	GPIO030/I2C10_SDA
A3	GPIO031/SP1_ALT_IO0
K10	GPIO032/QSPI1_IN_IO1
B4	GPIO033
A5	GPIO034/SP1_AP_INTR[I2C_ADDR1]
H9	GPIO045/QSPI1_IN_CS1#
A7	GPIO046/SP1_ALT_CS#
C2	GPIO047/SP1_ALT_IO1
B2	GPIO050/ICT0
E1	GPIO053/PWM0
K2	GPIO055/QSPI0_CS0#/SPIMON_QS-PI0_CS0#(QSPI0_PWRGD)
K7	GPIO056/QSPI0_CLK/QSPI0_CLK_CLAMP
D4	GPIO057/VCC_PWRGD
A1	GPIO063/SP1_ALT_CLK
D10	GPIO070/QSPI1_IN_IO0
J9	GPIO071/QSPI1_IN_CS0#
E4	GPIO104/UART0_TX/TFDP_CLK
E2	GPIO105/UART0_RX/TFDP_DATA
E3	GPIO106/AP0_RESET#(AP0_RESET#)
A6	GPIO107/I2C10_SCL/ALT_VIOL_0
F4	GPIO112/ALT_VIOL_1/TFDP_DATA_ALT
A2	GPIO113/ICT9
H10	GPIO120/QSPI1_CS1#/SPIMON_QSPI1_CS1#
F9	GPIO121/QSPI1_IO0/QSPI1_IO0_CLAMP
K9	GPIO122/QSPI1_IO1/QSPI1_IO1_CLAMP
F10	GPIO123/QSPI1_IO2/QSPI1_IO2_CLAMP
J8	GPIO124/QSPI1_CS0#/SPIMON_QS-PI1_CS0#(QSPI1_PWRGD)
J10	GPIO125/QSPI1_CLK/QSPI1_CLK_CLAMP
G10	GPIO126/QSPI1_IO3/QSPI1_IO3_CLAMP
F3	GPIO127/SP1_ALT_IO2
B1	GPIO130/32KHZ_IN
D2	GPIO131/AP1_RESET# (AP1_RESET#)
C9	GPIO132/I2C06_SDA
B7	GPIO140/I2C06_SCL
A9	GPIO143/I2C04_SDA
B9	GPIO144/I2C04_SCL(REMOTE_ACCESS)
B10	GPIO145/I2C09_SDA/JTAG_TDI
C10	GPIO146/I2C09_SCL/ITM/JTAG_TDO(SWV)

TABLE 2-2: CEC1734 PINOUT

CEC1734-S0-I/2ZW	CEC1734 Signal Name
B8	GPIO147/I2C15_SDA/JTAG_CLK (SWDCLK)
A8	GPIO150/I2C15_SCL/JTAG_TMS (SWDIO)
H2	GPIO156/LED0
H1	GPIO157/LED1
B5	GPIO163/SPI1_KILL/SPI1_RESET#
E10	GPIO165/QSPI1_IN_IO2
G5	GPIO170[JTAG_STRAP]
G9	GPIO171/QSPI1_IN_IO3
K8	GPIO200/QSPI1_IN_CLK
G2	GPIO201/32KHZ_OUT[CR_FLASH]
K5	GPIO202/QSPI0_IN_IO2
K3	GPIO203/QSPI0_IN_IO3
K6	GPIO204/QSPI0_IN_CLK
F8	GPIO223/QSPI0_IO0/QSPI0_IO0_CLAMP
J6	GPIO224/QSPI0_IO1/QSPI0_IO1_CLAMP
J4	GPIO227/QSPI0_IO2/QSPI0_IO2_CLAMP
J5	GPIO250/SPI0PER_CS#
E8	GPIO253/TST_CLK_OUT
G1	JTAG_RST#
G4	nRESET_IN
G6	VSS_ANALOG
F1	VTR_PLL
D9	VSS
D7	VTR_REG
H5	VTR1
C5	VTR_ANALOG
D1	VR_CAP
E7	VSS
H6	VTR2
J1	VSS
G7	VSS

TABLE 2-3: CEC1736 PINOUT

CEC1736-S0-I/2HW	CEC1736 Signal Name
E2	GPIO000/SPI0_KILL/SPI0_RESET#
F9	GPIO002/QSPI0_CS1#/SPIMON_QSPI0_CS1#
J2	GPIO003/I2C00_SDA(FATAL_ERROR#)
G2	GPIO004/I2C00_SCL
J3	GPIO012(EXTRST#)
K7	GPIO013/SP1_ALT_IO3
F2	GPIO015/ICT10[BSTRAP]
D10	GPIO016/QSPI0_IO3/QSPI0_IO3_CLAMP
G9	GPIO020/QSPI0_IN_CS0#

TABLE 2-3: CEC1736 PINOUT

CEC1736-S0-I/2HW	CEC1736 Signal Name
D9	GPIO021/QSPI0_IN_CS1#
A7	GPIO022/QSPI0_IN_IO1
A8	GPIO023/QSPI0_IN_IO0
A4	GPIO026/SP0_AP_INTR[I2C_ADDR0]
K2	GPIO027/ALT_TFDP_CLK
D1	GPIO030/I2C10_SDA
G1	GPIO031/SP1_ALT_IO0
F1	GPIO034/SP1_AP_INTR[I2C_ADDR1]
C2	GPIO046/SP1_ALT_CS#
K3	GPIO047/SP1_ALT_IO1
H2	GPIO050/ICT0
J5	GPIO053/PWM0
E9	GPIO055/QSPI0_CS0#/SPIMON_QS-PI0_CS0#(QSPI0_PWRGD)
B9	GPIO056/QSPI0_CLK/QSPI0_CLK_CLAMP
J4	GPIO057/VCC_PWRGD
H1	GPIO063/SP1_ALT_CLK
K5	GPIO104/UART0_TX/TFDP_CLK
J6	GPIO105/UART0_RX/TFDP_DATA
K6	GPIO106/AP0_RESET#(AP0_RESET#)
E1	GPIO107/I2C10_SCL/ALT_VIOL_0
K8	GPIO112/ALT_VIOL_1/ALT_TFDP_DATA
J7	GPIO127/SP1_ALT_IO2
J1	GPIO130/32KHZ_IN
D2	GPIO132/I2C06_SDA
C1	GPIO140/I2C06_SCL
A2	GPIO143/I2C04_SDA
A3	GPIO144/I2C04_SCL(REMOTE_ACCESS)
B4	GPIO145/I2C09_SDA/JTAG_TDI
B2	GPIO146/I2C09_SCL/ITM/JTAG_TDO(SWV)
B1	GPIO147/I2C15_SDA/JTAG_CLK (SWDCLK)
B3	GPIO150/I2C15_SCL/JTAG_TMS (SWDIO)
J10	GPIO156/LED0
G10	GPIO157/LED1
J8	GPIO170[JTAG_STRAP]
J9	GPIO201/32KHZ_OUT[CR_FLASH]
C9	GPIO202/QSPI0_IN_IO2
E10	GPIO203/QSPI0_IN_IO3
B10	GPIO204/QSPI0_IN_CLK
A6	GPIO223/QSPI0_IO0/QSPI0_IO0_CLAMP
A9	GPIO224/QSPI0_IO1/QSPI0_IO1_CLAMP
B7	GPIO227/QSPI0_IO2/QSPI0_IO2_CLAMP
C10	GPIO250/SPI0PER_CS#
B6	GPIO253/TST_CLK_OUT
H9	JTAG_RST#

TABLE 2-3: CEC1736 PINOUT

CEC1736-S0-I/2HW	CEC1736 Signal Name
H10	nRESET_IN
G4	VSS_ANALOG
K9	VTR_PLL
D7	VSS
G7	VTR_REG
B8	VTR1
D4	VTR_ANALOG
K4	VR_CAP
A5	VSS
F10	VSS
B5	VSS

TABLE 2-4: CEC1736 PINOUT

CEC1736-S0-I/2ZW	CEC1736 Signal Name
A4	GPIO000/SPI0_KILL/SPI0_RESET#
J2	GPIO002/QSPI0_CS1#/SPIMON_QSPI0_CS1#
C6	GPIO003/I2C00_SDA(FATAL_ERROR#)
C1	GPIO004/I2C00_SCL
D6	GPIO012(EXTRST#)
F2	GPIO013/SP1_ALT_IO3
B3	GPIO015/ICT10[BSTRAP]
K4	GPIO016/QSPI0_IO3/QSPI0_IO3_CLAMP
K1	GPIO020/QSPI0_IN_CS0#
J3	GPIO021/QSPI0_IN_CS1#
J7	GPIO022/QSPI0_IN_IO1
E9	GPIO023/QSPI0_IN_IO0
F7	GPIO024/SPI1PER_CS#
A10	GPIO026/SP0_AP_INTR[I2C_ADDR0]
D5	GPIO027/TFDP_CLK_ALT
B6	GPIO030/I2C10_SDA
A3	GPIO031/SP1_ALT_IO0
K10	GPIO032/QSPI1_IN_IO1
B4	GPIO033
A5	GPIO034/SP1_AP_INTR[I2C_ADDR1]
H9	GPIO045/QSPI1_IN_CS1#
A7	GPIO046/SP1_ALT_CS#
C2	GPIO047/SP1_ALT_IO1
B2	GPIO050/ICT0
E1	GPIO053/PWM0
K2	GPIO055/QSPI0_CS0#/SPIMON_QSPI0_CS0#(QSPI0_PWRGD)
K7	GPIO056/QSPI0_CLK/QSPI0_CLK_CLAMP

TABLE 2-4: CEC1736 PINOUT

CEC1736-S0-I/2ZW	CEC1736 Signal Name
D4	GPIO057/VCC_PWRGD
A1	GPIO063/SP1_ALT_CLK
D10	GPIO070/QSPI1_IN_IO0
J9	GPIO071/QSPI1_IN_CS0#
E4	GPIO104/UART0_TX/TFDP_CLK
E2	GPIO105/UART0_RX/TFDP_DATA
E3	GPIO106/AP0_RESET#(AP0_RESET#)
A6	GPIO107/I2C10_SCL/ALT_VIOL_0
F4	GPIO112/ALT_VIOL_1/TFDP_DATA_ALT
A2	GPIO113/ICT9
H10	GPIO120/QSPI1_CS1#/SPIMON_QSPI1_CS1#
F9	GPIO121/QSPI1_IO0/QSPI1_IO0_CLAMP
K9	GPIO122/QSPI1_IO1/QSPI1_IO1_CLAMP
F10	GPIO123/QSPI1_IO2/QSPI1_IO2_CLAMP
J8	GPIO124/QSPI1_CS0#/SPIMON_QSPI1_CS0#(QSPI1_PWRGD)
J10	GPIO125/QSPI1_CLK/QSPI1_CLK_CLAMP
G10	GPIO126/QSPI1_IO3/QSPI1_IO3_CLAMP
F3	GPIO127/SP1_ALT_IO2
B1	GPIO130/32KHZ_IN
D2	GPIO131/AP1_RESET# (AP1_RESET#)
C9	GPIO132/I2C06_SDA
B7	GPIO140/I2C06_SCL
A9	GPIO143/I2C04_SDA
B9	GPIO144/I2C04_SCL(REMOTE_ACCESS)
B10	GPIO145/I2C09_SDA/JTAG_TDI
C10	GPIO146/I2C09_SCL/ITM/JTAG_TDO(SWV)
B8	GPIO147/I2C15_SDA/JTAG_CLK (SWDCLK)
A8	GPIO150/I2C15_SCL/JTAG_TMS (SWDIO)
H2	GPIO156/LED0
H1	GPIO157/LED1
B5	GPIO163/SPI1_KILL/SPI1_RESET#
E10	GPIO165/QSPI1_IN_IO2
G5	GPIO170[JTAG_STRAP]
G9	GPIO171/QSPI1_IN_IO3
K8	GPIO200/QSPI1_IN_CLK
G2	GPIO201/32KHZ_OUT[CR_FLASH]
K5	GPIO202/QSPI0_IN_IO2
K3	GPIO203/QSPI0_IN_IO3
K6	GPIO204/QSPI0_IN_CLK
F8	GPIO223/QSPI0_IO0/QSPI0_IO0_CLAMP
J6	GPIO224/QSPI0_IO1/QSPI0_IO1_CLAMP
J4	GPIO227/QSPI0_IO2/QSPI0_IO2_CLAMP
J5	GPIO250/SPI0PER_CS#
E8	GPIO253/TST_CLK_OUT

TABLE 2-4: CEC1736 PINOUT

CEC1736-S0-I/2ZW	CEC1736 Signal Name
G1	JTAG_RST#
G4	nRESET_IN
G6	VSS_ANALOG
F1	VTR_PLL
D9	VSS
D7	VTR_REG
H5	VTR1
C5	VTR_ANALOG
D1	VR_CAP
E7	VSS
H6	VTR2
J1	VSS
G7	VSS

2.4 Pin Multiplexing

2.4.1 DEFAULT STATE

The default state for all pins is floating. The default state for all pins that contain a GPIO function is to select that GPIO function, while floating with input/output/interrupt disabled. The only non-GPIO signal pins have strictly input functionality.

Pins that are connected to each other via internal analog Q-switches are isolated from each other by default.

2.4.2 POWER RAIL

The Power Rail column defines the power pin that provides I/O power for the signal pin.

2.4.3 BUFFER TYPES

The Buffer Type column defines the type of Buffer associated with each signal. See Section "Buffer Terminology," on page 9.

2.4.4 ANTI-GLITCH PROTECTION

All signal pins are Anti-Glitch protected, as described here. During power-up of a pin's power domain (VTR_REG, VTR1 or VTR2), this feature holds the output drivers in their floating condition, while also connecting the pins internally to ground via weak pull-down resistors (60K typ: 40K min / 80K max), until the pin's internal power voltage is within the operating range.

Once the pin's internal power voltage is above the minimum threshold, the internal pull-down resistor will be disabled and each pin will be truly floating, in the GPIO input/output/interrupt-disabled state.

If there is an external pull-up resistor on the GPIO pin, this feature will present an additional DC load from the internal pull-down resistor during the power-up transition, resulting in reduced voltage on the signal at this time. System designers should choose the external pull-up resistor value to ensure a guaranteed minimum high voltage at the pin during power up.

For pins that need to be initially low, an external pull-down resistor will still be needed to ensure this level between the time the power well has powered up and pin function initialization has been performed, since the internal pull-down will no longer be engaged.

Note:	The power rail must rise monotonically in order for this behavior to be guaranteed.

2.4.5 OVER-VOLTAGE PROTECTION

If a pin is powered by 1.8V +/- 5% (operational), it can tolerate up to 1.8V +10% (i.e., +1.98V max). If the pad is powered by 3.3V +/- 5% (operational) it can tolerate up to 3.3V +10% (i.e., +3.63V max).

2.4.6 UNDER-VOLTAGE PROTECTION

All pins are under-voltage protected.

Pins that are identified as having Under-voltage PROTECTION may be configured so they will not sink excess current if powered by 3.3V and externally pulled up to 1.8V. The following configuration requirements must be met.

- If the pad is an output only pad type and it is configured as either open drain or the output is disabled.
- If the pin is a GPIO pin with a PIO pad type then it must be configured as open drain output with the input disabled. The input is disabled by setting the GPIO Power Gating Signals (PGS) bits to 11b.

2.4.7 BACKDRIVE PROTECTION

Backdrive protection is not provided for external voltages that are above the power well of the pin by an amount outside the specified margin. If a pin is not powered, it must not be externally driven.

2.4.8 EMULATED POWER WELL

Power wells are not emulated. Each pin has a designated well by which it is powered.

2.4.9 GATED STATE

This column defines the internal value of an input signal when either its power well is inactive or it is not selected by the GPIO alternate function MUX. A value of “No Gate” means that the internal signal always follows the pin even when the power well is off.

Note:	Gated state is only meaningful to the operation of input signals. A gated state on an output pin defines the internal behavior of the GPIO MUX and does not imply pin behavior.

2.4.10 NOTES

The below notes are for all tables in this chapter.

2.4.11 PIN MULTIPLEXING

The GPIO Mux Control bits located in the Pin Control Registers are used to support up to three alternate functions on any GPIO pin. The following tables define all the GPIO Multiplexing Options implemented for each of the products.

TABLE 2-5: CEC1734_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO000	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SPI0_KILL	O			NA	NA			
2	SPI0_RESET#	PIO			NA	High			
Default :0	GPIO002	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CS1#	O			NA	NA			Q-SW
2	SPIMON_QSPI0_CS1#	O			NA	NA			Q-SW
Default :0	GPIO003	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C00_SDA	PIO			NA	High			
2	Reserved								

TABLE 2-5: CEC1734_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO004	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C00_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO012	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO013	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO3	PIO			NA	High			
2	Reserved								
Default :0	GPIO015	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	ICT10	I			NA	Low			
Default :0	GPIO016	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO3	PIO			NA	High			Q-SW
2	QSPI0_IO3_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO020	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CS0#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO021	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CS1#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO022	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO1	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO023	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO0	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO026	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP0_AP_INTR	O			NA	NA			
2	Reserved								
Default :0	GPIO027	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								

TABLE 2-5: CEC1734_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO030	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C10_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO031	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO0	PIO			NA	High			
2	Reserved								
Default :0	GPIO034	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_AP_INTR	O			NA	NA			
2	Reserved								
Default :0	GPIO046	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_CS#	I			NA	High			
2	Reserved								
Default :0	GPIO047	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO1	PIO			NA	High			
2	Reserved								
Default :0	GPIO050	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ICT0	I			NA	Low			
2	Reserved								
Default :0	GPIO053	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	PWM0	O			NA	NA			
2	Reserved								
Default :0	GPIO055	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CS0#	O			NA	NA			Q-SW
2	SPIMON_QSPI0_CS0#	O			NA	NA			Q-SW
Default :0	GPIO056	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CLK	O			NA	NA			Q-SW
2	QSPI0_CLK_CLAMP	O			NA	NA			Q-SW
Default :0	GPIO057	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	VCC_PWRGD	I			NA	High			
2	Reserved								
Default :0	GPIO063	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_CLK	I			NA	Low			
2	Reserved								

TABLE 2-5: CEC1734_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO104	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	UART0_TX	O			NA	NA			
2	TFDP_CLK	O			NA	NA			
Default :0	GPIO105	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	UART0_RX	I			NA	Low			
2	TFDP_DATA	O			NA	NA			
Default :0	GPIO106	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	AP0_RESET#	O			NA	NA			
2	Reserved								
Default :0	GPIO107	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C10_SCL	PIO			NA	High			
2	ALT_VIOL_0	O			NA	NA			
Default :0	GPIO112	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ALT_VIOL_1	O			NA	NA			
2	Reserved								
Default :0	GPIO127	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO2	PIO			NA	High			
2	Reserved								
Default :0	GPIO130	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	32KHZ_IN	I			NA	Low			
2	Reserved								
Default :0	GPIO132	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C06_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO140	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C06_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO143	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C04_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO144	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C04_SCL	PIO			NA	High			
2	Reserved								

TABLE 2-5: CEC1734_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO145	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C09_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO146	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C09_SCL	PIO			NA	High			
2	ITM	O			NA	NA			
Default :0	GPIO147	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C15_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO150	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C15_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO156	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	LED0	O			NA	NA			
2	Reserved								
Default :0	GPIO157	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	LED1	O			NA	NA			
2	Reserved								
Default :0	GPIO170	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO201	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	32KHZ_OUT	O			NA	NA			
2	Reserved								
Default :0	GPIO202	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO2	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO203	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO3	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO204	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CLK	I			NA	Low			Q-SW
2	Reserved								

TABLE 2-5: CEC1734_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO223	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO0	PIO			NA	High			Q-SW
2	QSPI0_IO0_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO224	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO1	PIO			NA	High			Q-SW
2	QSPI0_IO1_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO227	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO2	PIO			NA	High			Q-SW
2	QSPI0_IO2_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO250	PIO	12mA	VTR1	NA	No Gate	No	No	
1	SPI0PER_CS#	I			NA	High			
2	Reserved								
Default :0	GPIO253	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	TST_CLK_OUT	O			NA	NA			
2	Reserved								
NA	JTAG_RST#	I	NA	VTR_REG	NA	NA	No	No	
1	Reserved								
2	Reserved								
NA	nRESET_IN	I	NA	VTR_REG	NA	NA	No	No	
1	Reserved								
2	Reserved								

TABLE 2-6: CEC1734_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO000	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SPI0_KILL	O			NA	NA			
2	SPI0_RESET#	PIO			NA	High			
Default :0	GPIO002	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CS1#	O			NA	NA			Q-SW
2	SPIMON_QSPI0_CS1#	O			NA	NA			Q-SW

TABLE 2-6: CEC1734_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO003	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C00_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO004	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C00_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO012	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO013	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO3	PIO			NA	High			
2	Reserved								
Default :0	GPIO015	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	ICT10	I			NA	Low			
Default :0	GPIO016	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO3	PIO			NA	High			Q-SW
2	QSPI0_IO3_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO020	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CS0#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO021	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CS1#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO022	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO1	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO023	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO0	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO024	PIO	12mA	VTR2	NA	No Gate	No	No	
1	SPI1PER_CS#	I			NA	High			
2	Reserved								

TABLE 2-6: CEC1734_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO026	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP0_AP_INTR	O			NA	NA			
2	Reserved								
Default :0	GPIO027	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	TFDP_CLK_ALT	O			NA	NA			
2	Reserved								
Default :0	GPIO030	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C10_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO031	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO0	PIO			NA	High			
2	Reserved								
Default :0	GPIO032	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_IO1	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO033	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO034	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_AP_INTR	O			NA	NA			
2	Reserved								
Default :0	GPIO045	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_CS1#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO046	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_CS#	I			NA	High			
2	Reserved								
Default :0	GPIO047	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO1	PIO			NA	High			
2	Reserved								
Default :0	GPIO050	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ICT0	I			NA	Low			
2	Reserved								

TABLE 2-6: CEC1734_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO053	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	PWM0	O			NA	NA			
2	Reserved								
Default :0	GPIO055	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CS0#	O			NA	NA			Q-SW
2	SPIMON_QSPI0_CS0#	O			NA	NA			Q-SW
Default :0	GPIO056	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CLK	O			NA	NA			Q-SW
2	QSPI0_CLK_CLAMP	O			NA	NA			Q-SW
Default :0	GPIO057	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	VCC_PWRGD	I			NA	High			
2	Reserved								
Default :0	GPIO063	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_CLK	I			NA	Low			
2	Reserved								
Default :0	GPIO070	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_IO0	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO071	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_CS0#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO104	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	UART0_TX	O			NA	NA			
2	TFDP_CLK	O			NA	NA			
Default :0	GPIO105	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	UART0_RX	I			NA	Low			
2	TFDP_DATA	O			NA	NA			
Default :0	GPIO106	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	AP0_RESET#	O			NA	NA			
2	Reserved								
Default :0	GPIO107	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C10_SCL	PIO			NA	High			
2	ALT_VIOL_0	O			NA	NA			

TABLE 2-6: CEC1734_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO112	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ALT_VIOL_1	O			NA	NA			
2	TFDP_DATA_ALT	O			NA	NA			
Default :0	GPIO113	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ICT9	I			NA	Low			
2	Reserved								
Default :0	GPIO120	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_CS1#	O			NA	NA			Q-SW
2	SPIMON_QSPI1_CS1#	O			NA	NA			Q-SW
Default :0	GPIO121	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IO0	PIO			NA	High			Q-SW
2	QSPI1_IO0_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO122	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IO1	PIO			NA	High			Q-SW
2	QSPI1_IO1_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO123	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IO2	PIO			NA	High			Q-SW
2	QSPI1_IO2_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO124	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_CS0#	O			NA	NA			Q-SW
2	SPIMON_QSPI1_CS0#	O			NA	NA			Q-SW
Default :0	GPIO125	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_CLK	O			NA	NA			Q-SW
2	QSPI1_CLK_CLAMP	O			NA	NA			Q-SW
Default :0	GPIO126	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IO3	PIO			NA	High			Q-SW
2	QSPI1_IO3_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO127	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO2	PIO			NA	High			
2	Reserved								
Default :0	GPIO130	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	32KHZ_IN	I			NA	Low			

TABLE 2-6: CEC1734_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
2	Reserved								
Default :0	GPIO131	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	AP1_RESET#	O			NA	NA			
2	Reserved								
Default :0	GPIO132	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C06_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO140	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C06_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO143	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C04_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO144	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C04_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO145	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C09_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO146	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C09_SCL	PIO			NA	High			
2	ITM	O			NA	NA			
Default :0	GPIO147	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C15_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO150	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C15_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO156	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	LED0	O			NA	NA			
2	Reserved								
Default :0	GPIO157	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	LED1	O			NA	NA			
2	Reserved								

TABLE 2-6: CEC1734_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO163	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SPI1_KILL	O			NA	NA			
2	SPI1_RESET#	PIO			NA	High			
Default :0	GPIO165	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_IO2	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO170	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO171	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_IO3	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO200	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_CLK	I			NA	Low			Q-SW
2	Reserved								
Default :0	GPIO201	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	32KHZ_OUT	O			NA	NA			
2	Reserved								
Default :0	GPIO202	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO2	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO203	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO3	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO204	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CLK	I			NA	Low			Q-SW
2	Reserved								
Default :0	GPIO223	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO0	PIO			NA	High			Q-SW
2	QSPI0_IO0_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO224	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO1	PIO			NA	High			Q-SW
2	QSPI0_IO1_CLAMP	PIO			NA	High			Q-SW

TABLE 2-6: CEC1734_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO227	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO2	PIO			NA	High			Q-SW
2	QSPI0_IO2_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO250	PIO	12mA	VTR1	NA	No Gate	No	No	
1	SPI0PER_CS#	I			NA	High			
2	Reserved								
Default :0	GPIO253	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	TST_CLK_OUT	O			NA	NA			
2	Reserved								
NA	JTAG_RST#	I	NA	VTR_REG	NA	NA	No	No	
1	Reserved								
2	Reserved								
NA	nRESET_IN	I	NA	VTR_REG	NA	NA	No	No	
1	Reserved								
2	Reserved								

TABLE 2-7: CEC1736_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO000	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SPI0_KILL	O			NA	NA			
2	SPI0_RESET#	PIO			NA	High			
Default :0	GPIO002	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CS1#	O			NA	NA			Q-SW
2	SPIMON_QSPI0_CS1#	O			NA	NA			Q-SW
Default :0	GPIO003	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C00_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO004	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C00_SCL	PIO			NA	High			
2	Reserved								

TABLE 2-7: CEC1736_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO012	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO013	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO3	PIO			NA	High			
2	Reserved								
Default :0	GPIO015	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	ICT10	I			NA	Low			
Default :0	GPIO016	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO3	PIO			NA	High			Q-SW
2	QSPI0_IO3_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO020	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CS0#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO021	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CS1#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO022	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO1	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO023	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO0	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO026	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP0_AP_INTR	O			NA	NA			
2	Reserved								
Default :0	GPIO027	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO030	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C10_SDA	PIO			NA	High			
2	Reserved								

TABLE 2-7: CEC1736_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO031	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO0	PIO			NA	High			
2	Reserved								
Default :0	GPIO034	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_AP_INTR	O			NA	NA			
2	Reserved								
Default :0	GPIO046	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_CS#	I			NA	High			
2	Reserved								
Default :0	GPIO047	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO1	PIO			NA	High			
2	Reserved								
Default :0	GPIO050	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ICT0	I			NA	Low			
2	Reserved								
Default :0	GPIO053	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	PWM0	O			NA	NA			
2	Reserved								
Default :0	GPIO055	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CS0#	O			NA	NA			Q-SW
2	SPIMON_QSPI0_CS0#	O			NA	NA			Q-SW
Default :0	GPIO056	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CLK	O			NA	NA			Q-SW
2	QSPI0_CLK_CLAMP	O			NA	NA			Q-SW
Default :0	GPIO057	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	VCC_PWRGD	I			NA	High			
2	Reserved								
Default :0	GPIO063	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_CLK	I			NA	Low			
2	Reserved								
Default :0	GPIO104	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	UART0_TX	O			NA	NA			
2	TFDP_CLK	O			NA	NA			

TABLE 2-7: CEC1736_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO105	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	UART0_RX	I			NA	Low			
2	TFDP_DATA	O			NA	NA			
Default :0	GPIO106	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	AP0_RESET#	O			NA	NA			
2	Reserved								
Default :0	GPIO107	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C10_SCL	PIO			NA	High			
2	ALT_VIOL_0	O			NA	NA			
Default :0	GPIO112	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ALT_VIOL_1	O			NA	NA			
2	Reserved								
Default :0	GPIO127	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO2	PIO			NA	High			
2	Reserved								
Default :0	GPIO130	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	32KHZ_IN	I			NA	Low			
2	Reserved								
Default :0	GPIO132	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C06_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO140	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C06_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO143	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C04_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO144	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C04_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO145	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C09_SDA	PIO			NA	High			
2	Reserved								

TABLE 2-7: CEC1736_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO146	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C09_SCL	PIO			NA	High			
2	ITM	O			NA	NA			
Default :0	GPIO147	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C15_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO150	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C15_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO156	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	LED0	O			NA	NA			
2	Reserved								
Default :0	GPIO157	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	LED1	O			NA	NA			
2	Reserved								
Default :0	GPIO170	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO201	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	32KHZ_OUT	O			NA	NA			
2	Reserved								
Default :0	GPIO202	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO2	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO203	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO3	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO204	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CLK	I			NA	Low			Q-SW
2	Reserved								
Default :0	GPIO223	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO0	PIO			NA	High			Q-SW
2	QSPI0_IO0_CLAMP	PIO			NA	High			Q-SW

TABLE 2-7: CEC1736_2HW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO224	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO1	PIO			NA	High			Q-SW
2	QSPI0_IO1_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO227	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO2	PIO			NA	High			Q-SW
2	QSPI0_IO2_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO250	PIO	12mA	VTR1	NA	No Gate	No	No	
1	SPI0PER_CS#	I			NA	High			
2	Reserved								
Default :0	GPIO253	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	TST_CLK_OUT	O			NA	NA			
2	Reserved								
NA	JTAG_RST#	I	NA	VTR_REG	NA	NA	No	No	
1	Reserved								
2	Reserved								
NA	nRESET_IN	I	NA	VTR_REG	NA	NA	No	No	
1	Reserved								
2	Reserved								

TABLE 2-8: CEC1736_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO000	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SPI0_KILL	O			NA	NA			
2	SPI0_RESET#	PIO			NA	High			
Default :0	GPIO002	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CS1#	O			NA	NA			Q-SW
2	SPIMON_QSPI0_CS1#	O			NA	NA			Q-SW
Default :0	GPIO003	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C00_SDA	PIO			NA	High			
2	Reserved								

TABLE 2-8: CEC1736_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO004	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C00_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO012	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO013	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO3	PIO			NA	High			
2	Reserved								
Default :0	GPIO015	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	ICT10	I			NA	Low			
Default :0	GPIO016	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO3	PIO			NA	High			Q-SW
2	QSPI0_IO3_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO020	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CS0#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO021	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CS1#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO022	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO1	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO023	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO0	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO024	PIO	12mA	VTR2	NA	No Gate	No	No	
1	SPI1PER_CS#	I			NA	High			
2	Reserved								
Default :0	GPIO026	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP0_AP_INTR	O			NA	NA			
2	Reserved								

TABLE 2-8: CEC1736_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO027	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	TFDP_CLK_ALT	O			NA	NA			
2	Reserved								
Default :0	GPIO030	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C10_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO031	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO0	PIO			NA	High			
2	Reserved								
Default :0	GPIO032	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_IO1	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO033	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO034	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_AP_INTR	O			NA	NA			
2	Reserved								
Default :0	GPIO045	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_CS1#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO046	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_CS#	I			NA	High			
2	Reserved								
Default :0	GPIO047	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO1	PIO			NA	High			
2	Reserved								
Default :0	GPIO050	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ICT0	I			NA	Low			
2	Reserved								
Default :0	GPIO053	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	PWM0	O			NA	NA			
2	Reserved								

TABLE 2-8: CEC1736_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO055	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CS0#	O			NA	NA			Q-SW
2	SPIMON_QS-PI0_CS0#	O			NA	NA			Q-SW
Default :0	GPIO056	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_CLK	O			NA	NA			Q-SW
2	QSPI0_CLK_-CLAMP	O			NA	NA			Q-SW
Default :0	GPIO057	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	VCC_PWRGD	I			NA	High			
2	Reserved								
Default :0	GPIO063	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_CLK	I			NA	Low			
2	Reserved								
Default :0	GPIO070	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_IO0	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO071	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_CS0#	I			NA	High			Q-SW
2	Reserved								
Default :0	GPIO104	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	UART0_TX	O			NA	NA			
2	TFDP_CLK	O			NA	NA			
Default :0	GPIO105	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	UART0_RX	I			NA	Low			
2	TFDP_DATA	O			NA	NA			
Default :0	GPIO106	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	AP0_RESET#	O			NA	NA			
2	Reserved								
Default :0	GPIO107	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C10_SCL	PIO			NA	High			
2	ALT_VIOL_0	O			NA	NA			
Default :0	GPIO112	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ALT_VIOL_1	O			NA	NA			
2	TFDP_DATA_ALT	O			NA	NA			

TABLE 2-8: CEC1736_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO113	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	ICT9	I			NA	Low			
2	Reserved								
Default :0	GPIO120	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_CS1#	O			NA	NA			Q-SW
2	SPIMON_QSPI1_CS1#	O			NA	NA			Q-SW
Default :0	GPIO121	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IO0	PIO			NA	High			Q-SW
2	QSPI1_IO0_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO122	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IO1	PIO			NA	High			Q-SW
2	QSPI1_IO1_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO123	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IO2	PIO			NA	High			Q-SW
2	QSPI1_IO2_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO124	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_CS0#	O			NA	NA			Q-SW
2	SPIMON_QSPI1_CS0#	O			NA	NA			Q-SW
Default :0	GPIO125	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_CLK	O			NA	NA			Q-SW
2	QSPI1_CLK_CLAMP	O			NA	NA			Q-SW
Default :0	GPIO126	PIO	24mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IO3	PIO			NA	High			Q-SW
2	QSPI1_IO3_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO127	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SP1_ALT_IO2	PIO			NA	High			
2	Reserved								
Default :0	GPIO130	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	32KHZ_IN	I			NA	Low			
2	Reserved								
Default :0	GPIO131	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	AP1_RESET#	O			NA	NA			

TABLE 2-8: CEC1736_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
2	Reserved								
Default :0	GPIO132	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C06_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO140	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C06_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO143	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C04_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO144	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C04_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO145	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C09_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO146	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C09_SCL	PIO			NA	High			
2	ITM	O			NA	NA			
Default :0	GPIO147	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C15_SDA	PIO			NA	High			
2	Reserved								
Default :0	GPIO150	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	I2C15_SCL	PIO			NA	High			
2	Reserved								
Default :0	GPIO156	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	LED0	O			NA	NA			
2	Reserved								
Default :0	GPIO157	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	LED1	O			NA	NA			
2	Reserved								
Default :0	GPIO163	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	SPI1_KILL	O			NA	NA			
2	SPI1_RESET#	PIO			NA	High			

TABLE 2-8: CEC1736_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO165	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_IO2	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO170	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	Reserved								
2	Reserved								
Default :0	GPIO171	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_IO3	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO200	PIO	12mA	VTR2	NA	No Gate	No	No	
1	QSPI1_IN_CLK	I			NA	Low			Q-SW
2	Reserved								
Default :0	GPIO201	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	32KHZ_OUT	O			NA	NA			
2	Reserved								
Default :0	GPIO202	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO2	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO203	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_IO3	PIO			NA	High			Q-SW
2	Reserved								
Default :0	GPIO204	PIO	12mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IN_CLK	I			NA	Low			Q-SW
2	Reserved								
Default :0	GPIO223	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO0	PIO			NA	High			Q-SW
2	QSPI0_IO0_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO224	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO1	PIO			NA	High			Q-SW
2	QSPI0_IO1_CLAMP	PIO			NA	High			Q-SW
Default :0	GPIO227	PIO	24mA	VTR1	NA	No Gate	No	No	
1	QSPI0_IO2	PIO			NA	High			Q-SW
2	QSPI0_IO2_CLAMP	PIO			NA	High			Q-SW

TABLE 2-8: CEC1736_2ZW

Mux value	Signal Name	Buffer type	Drive Strength	PAD Power Well	Emulated Power Well	Gated State	OVP	BDP	Notes
Default :0	GPIO250	PIO	12mA	VTR1	NA	No Gate	No	No	
1	SPI0PER_CS#	I			NA	High			
2	Reserved								
Default :0	GPIO253	PIO	12mA	VTR_REG	NA	No Gate	No	No	
1	TST_CLK_OUT	O			NA	NA			
2	Reserved								
NA	JTAG_RST#	I	NA	VTR_REG	NA	NA	No	No	
1	Reserved								
2	Reserved								
NA	nRESET_IN	I	NA	VTR_REG	NA	NA	No	No	
1	Reserved								
2	Reserved								

GPIO Documentation Conventions

The GPIO registers and bits are allocated for the full GPIO complement. Therefore, even GPIOs that are not implemented in the package will appear in the GPIO register lists. Please refer to the pinout to determine which GPIOs are bonded out in the package. GPIOs that are not available in the package should not have their configuration register altered.

2.4.12 STRAPPING OPTIONS

TABLE 2-9: STRAP PINS

Pin	I/O Power	Function	Description
GPIO170	VTR_REG	JTAG_STRAP (Note 3)	1=Use the JTAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)
GPIO201/32KHZ_OUT	VTR_REG	CR_FLASH (Note 2)	Crisis Flash Recovery 1=Don't Boot from Crisis Recovery Flash Component 0=Boot from Crisis Recovery Flash Component **Note:** The CR_FLASH strap pin is an optional feature enabled in OTP. If this feature is enabled, the pin requires an external pull-up for normal operation. If the feature is disabled, no external pull required. **Note:** Crisis Flash Component is determined by OTP
GPIO015/ICT10	VTR_REG	BSTRAP (Note 1)	0=Boot Strap (Boot ROM I2C or UART Crisis port) 1=Normal operation **Note:** BSTRAP may be enabled in OTP for UART Crisis Recovery and/or I2C Crisis Recovery. If enabled in OTP, this pin requires an external pull-up for normal operation.
GPIO026/SP0_AP_INTR	VTR_REG	I2C_ADDR0	I2C Address Strap Option pin 0 **Note:** I2C_ADDR[1:0] pins are used to select 1 of 4 possible I2C Addressing Profiles

TABLE 2-9: STRAP PINS (CONTINUED)

Pin	I/O Power	Function	Description
GPIO034/SP1_AP_INTR	VTR_REG	I2C_ADDR1	I2C Address Strap Option pin 1 **Note:** I2C_ADDR[1:0] pins are used to select 1 of 4 possible I2C Addressing Profiles

Note 1: The BSTRAP is an optional feature that may be enabled for either UART Crisis Recovery or I2C Crisis Recovery. If UART and I2C Crisis Recovery modes are disabled (default), the pin is ignored by the boot ROM and does not require any external hardware. If UART or I2C Crisis Recovery modes are enabled in OTP as a strap option, the system designer must ensure this pin is always high following a RESET_EC event, otherwise the device could enter Crisis Recovery Mode in error. If the external logic is driving a low into the BSTRAP pin the Boot ROM will detect a low and enter Crisis Recovery mode.

2: If the CR_FLASH strap pin is low it configures the part to boot from the crisis flash component. During normal operation, the system designer must ensure this pin is always high following a RESET_EC event, otherwise the Boot ROM may enter crisis mode in error. If the external logic is driving a low into the strap pin the Boot ROM will detect a low and enter Crisis Recovery mode.

3: The JTAG_STRAP pin requires a pull-down resistor for normal operation; recommend a resistor value of 10k ohm or less.

2.4.13 Q-SWITCH PINS

The following pins are connected via Q-switches.

TABLE 2-10: Q-SWITCH CHIP SELECT PINS

QSPIx_IN Signal	QSPIx Signal
GPIO020/QSPI0_IN_CS0#	GPIO055/QSPI0_CS0#/SPIMON_QSPI0_CS0#
	GPIO002/QSPI0_CS1#/SPIMON_QSPI0_CS1#
GPIO071/QSPI1_IN_CS0#	GPIO124/QSPI1_CS0#/SPIMON_QSPI1_CS0#
	GPIO120/QSPI1_CS1#/SPIMON_QSPI1_CS1#
GPIO021/QSPI0_IN_CS1#	GPIO055/QSPI0_CS0#/SPIMON_QSPI0_CS0#
	GPIO002/QSPI0_CS1#/SPIMON_QSPI0_CS1#
GPIO045/QSPI1_IN_CS1#	GPIO124/QSPI1_CS0#/SPIMON_QSPI1_CS0#
	GPIO120/QSPI1_CS1#/SPIMON_QSPI1_CS1#

Note 1: The two connections shown per input are selectable, one at a time.

TABLE 2-11: Q-SWITCH CLOCK AND IO PINS

QSPIx_IN Signal	QSPIx Signal
GPIO204/QSPI0_IN_CLK	GPIO056/QSPI0_CLK/QSPI0_CLK_CLAMP
GPIO023/QSPI0_IN_IO0	GPIO223/QSPI0_IO0/QSPI0_IO0_CLAMP
GPIO022/QSPI0_IN_IO1	GPIO224/QSPI0_IO1/QSPI0_IO1_CLAMP
GPIO202/QSPI0_IN_IO2	GPIO227/QSPI0_IO2/QSPI0_IO2_CLAMP
GPIO203/QSPI0_IN_IO3	GPIO016/QSPI0_IO3/QSPI0_IO3_CLAMP
GPIO200/QSPI1_IN_CLK	GPIO125/QSPI1_CLK/QSPI1_CLK_CLAMP
GPIO070/QSPI1_IN_IO0	GPIO121/QSPI1_IO0/QSPI1_IO0_CLAMP
GPIO032/QSPI1_IN_IO1	GPIO122/QSPI1_IO1/QSPI1_IO1_CLAMP
GPIO165/QSPI1_IN_IO2	GPIO123/QSPI1_IO2/QSPI1_IO2_CLAMP
GPIO171/QSPI1_IN_IO3	GPIO126/QSPI1_IO3/QSPI1_IO3_CLAMP

2.5 Package Information

2.5.1 64 PIN VFBGA PACKAGE

FIGURE 2-1: 2HW Package Dimensions, Sheet 1

64-Ball Very Thin Fine-Pitch Ball Grid Array (2HW) - 5.5x5.5x0.92 mm Body [VFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

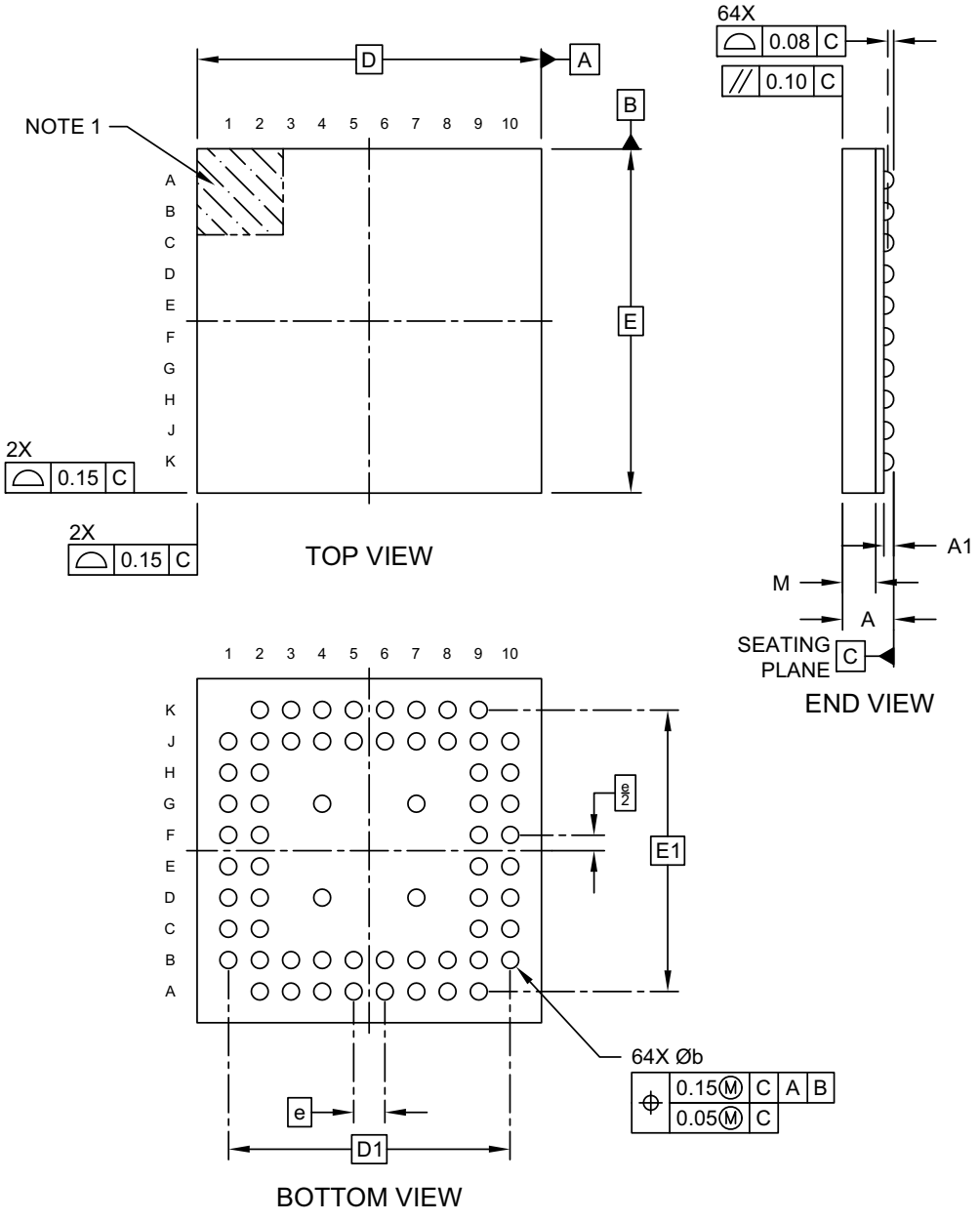
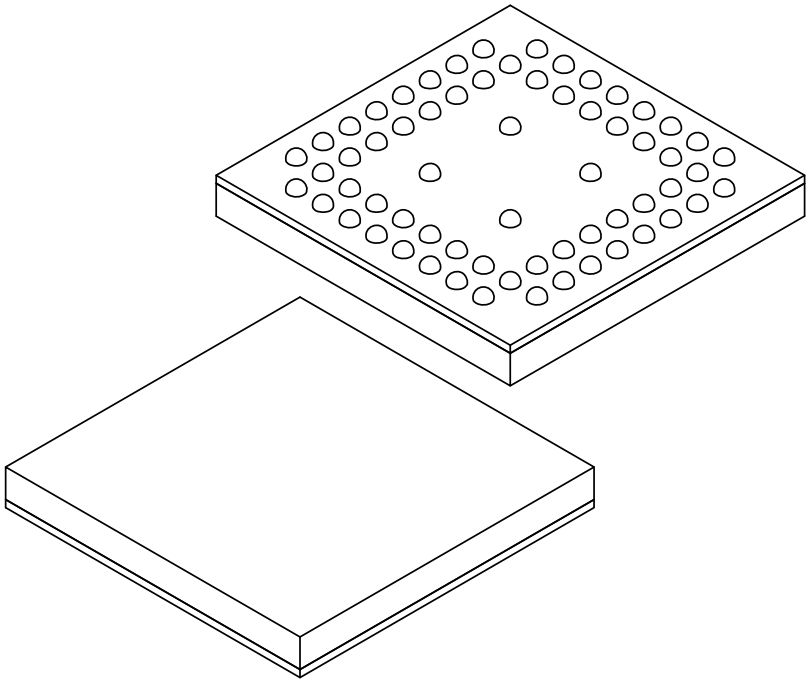


FIGURE 2-2: 2HW Package Dimensions, Sheet 2

64-Ball Very Thin Fine-Pitch Ball Grid Array (2HW) - 5.5x5.5x0.92 mm Body [VFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	0.92
Ball Height	A1	0.12	0.16	–
Mold Thickness	M	0.48	0.53	0.58
Overall Length	D		5.50 BSC	
Ball Array Length	D1		4.50 BSC	
Overall Width	E		5.50 BSC	
Ball Array Width	E1		4.50 BSC	
Ball Diameter	b	0.23	0.28	0.33

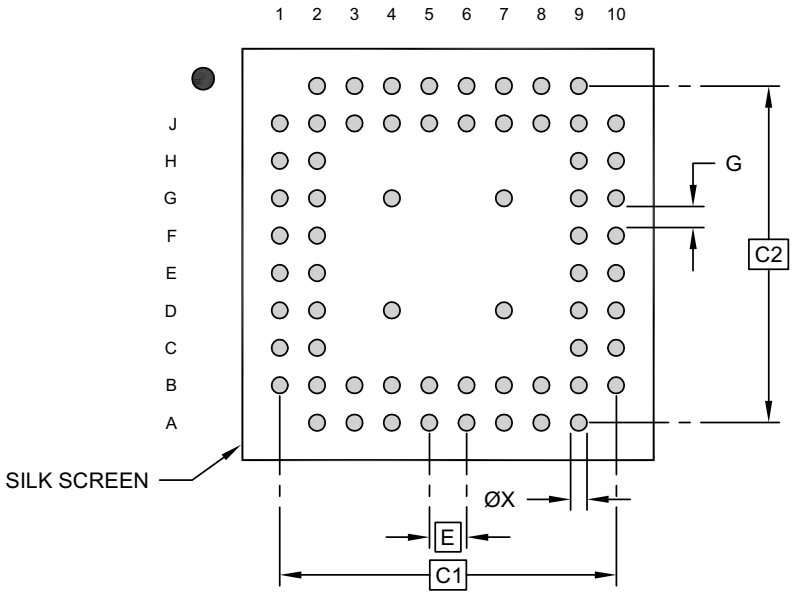
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

FIGURE 2-3: 2HW Package Dimensions, Sheet 3

64-Ball Very Thin Fine-Pitch Ball Grid Array (2HW) - 5.5x5.5x0.92 mm Body [VFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1	4.50 BSC		
Contact Pad Spacing	C2	4.50 BSC		
Contact Pad Diameter (X64)	X1			X.XX
Contact Pad to Contact Pad (Xnn)	G	0.28		

Notes:

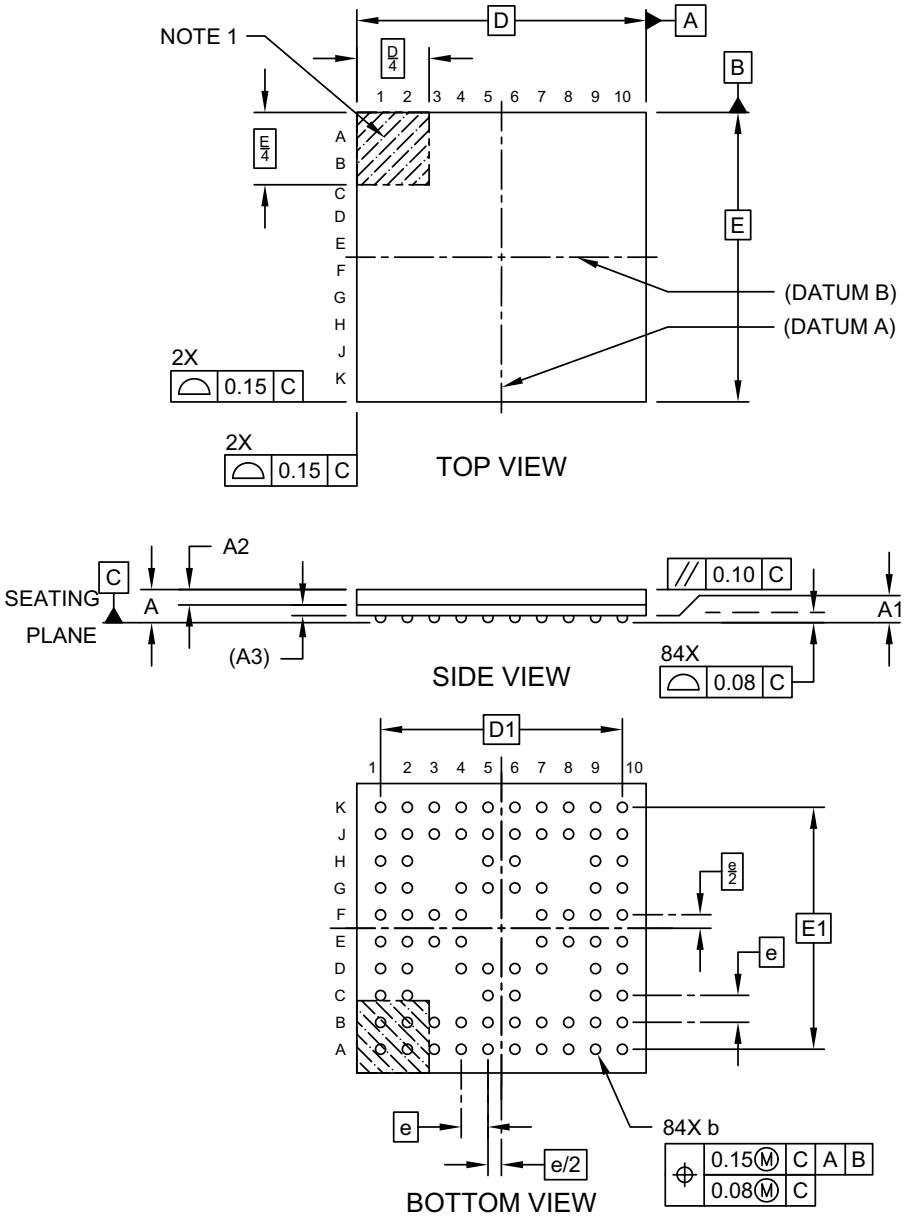
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2.5.2 84 PIN WFBGA PACKAGE

FIGURE 2-4: 2ZW Package Dimensions, Sheet 1

84-Ball Very, Very Thin fine Pitch Ball Grid Array (2ZW) - 7x7x0.8 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

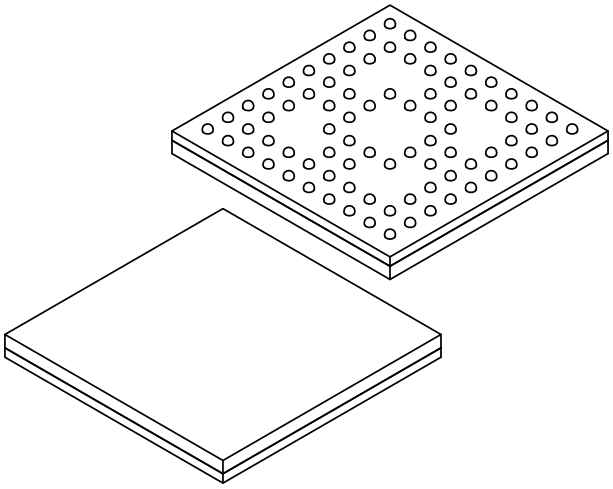


Microchip Technology Drawing C04-390-2ZW Rev C Sheet 1 of 2

FIGURE 2-5: 2ZW Package Dimensions, Sheet 2

84-Ball Very, Very Thin fine Pitch Ball Grid Array (2ZW) - 7x7x0.8 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		84	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	0.80
Standoff	A1	0.12	0.17	-
Mold Cap Thickness	A2	0.35	0.40	0.45
Substrate Thickness	A3		0.13 REF	
Overall Length	D		7.00 BSC	
Overall Termnal Spacing	D1		5.85 BSC	
Overall Width	E		7.00 BSC	
Overall Termnal Spacing	E1		5.85 BSC	
Ball Diameter	b	0.20	0.25	0.30

Notes:

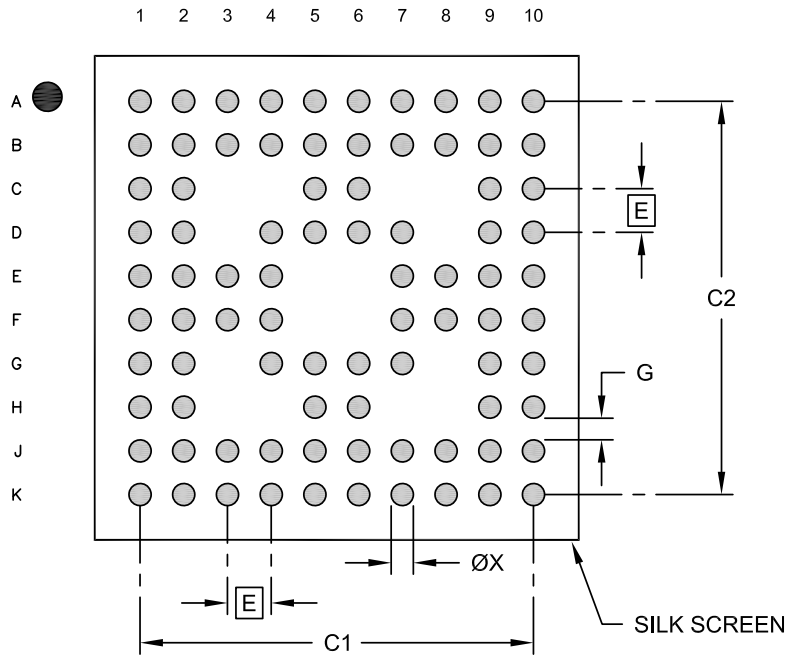
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-390-2ZW Rev C Sheet 2 of 2

FIGURE 2-6: 2ZW Package Dimensions, Sheet 3

84-Ball Very, Very Thin Fine Pitch Ball Grid Array (2ZW) - 7x7x0.8 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Overall Contact Pad Spacing	C1		5.85	
Overall Contact Pad Spacing	C2		5.85	
Contact Pad Width (X84)	X1			0.33
Contact Pad to Contact Pad	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2390-2WX Rev C

APPENDIX A: PRODUCT BRIEF REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00004571A (05-10-22)	Document release	

PRODUCT IDENTIFICATION SYSTEM

Not all of the possible combinations of Device, Temperature Range and Package may be offered for sale. To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.[1]	- XX	- X/XXX[2]	- [X][3]	- [XXX]
Device	Version/ Revision	Temp Range/ Package	Tape and Reel Option	Programmed Option

Device:	CEC1734		Cryptographic Embedded Controller
	CEC1736		Cryptographic Embedded Controller, Temperature and Voltage Countermeasures
Version/ Revision:	S#		S = Soteria Version # = Revision Version Number
Temperature Range	I/	=	-40°C to +85°C (Industrial)
Package:	2ZW		84 ball WFBGA, 7x7x0.8 mm body, 0.65 pitch, 4MB Flash, Dual SPI Monitor
	2HW		64 ball VFBGA, 5.5x5.5x0.92 mm body, 0.5 pitch, 2MB Flash, Single SPI Monitor
Tape and Reel Option:	Blank	=	Tray packaging
	TR	=	Tape and Reel[3]
Programmed Option:	Blank	=	Unprogrammed
	XXX	=	Programmed with “XXX” (application specific) code

Example:

a) CEC1736-S0-I/2ZW = CEC1736, Soteria Version, Revision Version 0, 84 ball WFBGA, 7mm x 7mm body, 4MB Flash, Dual SPI Monitor, Industrial grade, Tray packaging

b) CEC1736-S0-I/2HW-TR = CEC1736, Soteria Version, Revision Version 0, 64 ball VFBGA, 5.5mm x 5.5mm body, 2MB Flash, Single SPI Monitor, Industrial grade, Tape and Reel packaging

c) CEC1734-S0-I/2ZW-TR = CEC1734, Soteria Version, Revision Version 0, 84 ball WFBGA, 7mm x 7mm body, 4MB Flash, Dual SPI Monitor, Industrial grade, Tape and Reel packaging

d) CEC1734-S0-I/2HW = CEC1734, Soteria Version, Revision Version 0, 64 ball VFBGA, 5.5mm x 5.5mm body, 2MB Flash, Single SPI Monitor, Industrial grade, Tray packaging

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html

3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option

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