# ±2g Dual Axis Accelerometer with I2C Interface and 1mg Resolution

# MXC6245XU

## FEATURES

- High accuracy 2-axis accelerometer:
  - 2g Full Scale Range
  - 1 mg/LSB resolution
  - 0.3 mg/C offset drift over temperature
  - 0.5% Sensitivity matching
  - 12 Bit A/D Converter
  - No sensor resonance
- 400kHz I2C Interface (1.8V compatible)
- Small, 6-pin 3 x 3mm Ceramic LCC package
- Operates from 2.7V to 5.5V Supply
- High reliability Automotive Process and Package
- 50,000g shock survivability
- RoHS Compliant
- Operates from -40C to +85C

## APPLICATIONS

- Car Navigation System
- Projector Auto Keystone Correction
- DSC horizontal position detect
- Inclination sensing
- General purpose accelerometer

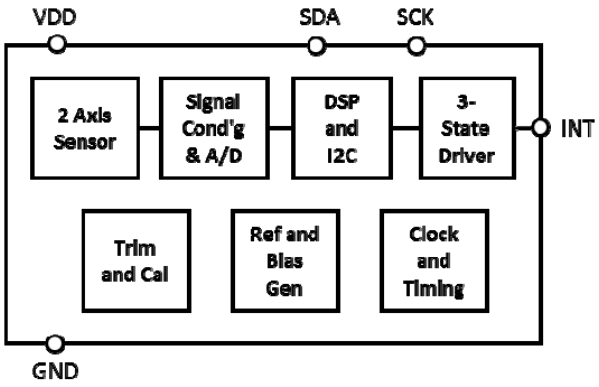


**FIGURE 1: FUNCTIONAL BLOCK DIAGRAM**

## DESCRIPTION

The MXC6245XU is a complete 2 axis accelerometer system with 1mg resolution, very low 0g offset drift, and excellent sensitivity matching. The internal status of the sensor can be read via the I2C interface.

The MXC6245XU uses MEMSIC's proprietary thermal accelerometer technology. Because the sensing element uses heated gas molecules instead of a mechanical beam structure, the device is extremely robust and reliable, with 50000g shock tolerance, no possibility of "stiction," virtually no mechanical resonance, and very high accuracy over temperature. This makes the device extremely well suited to harsh or high-vibration environments, where other sensors can exhibit false readings due to resonance or other errors.

The MXC6245XU has built in orientation detection. The device can be set to generate an interrupt if the orientation of the device changes with respect to gravity. See register $06 description for more detailed information.

The MXC6245XU runs from a single 2.7V to 5.5V supply over the industrial temperature range of -40 to 85C, and is packaged in a small 6-pin, 3 x 3 x 1 mm ceramic LCC package.



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## SENSOR CHARACTERISTICS:

(TA=25C, $V_{DD}$= 5V, unless otherwise specified. Typical values are specified at 25C)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Full Scale Range | | | ±2 | | g |
| Sensitivity | TA=25C | 975 | 1024 | 1075 | LSB/g |
| | Temperature Drift (-40 to +85C)[1] | | ±6 | ±8.5 | % |
| | X/Y Matching over Temperature (-40 to +85C)[1,4] | | ±0.3 | ±0.5 | % |
| Zero-g Bias | TA=25C | | ±10 | ±30 | mg |
| | Temperature Drift (-40 to +85C)[1] | | ±0.1 | ±0.3 | mg/C |
| Sensor Bandwidth | (Note 2) | | 11 | | Hz |
| Input Referred Noise | Total RMS Noise, ODR = 100Hz | | 1.5 | | mg RMS |
| Resonance | (Note 3) | Undetectable | | | Hz |

Note 1: Established statistically at the average value 3 standard deviations from 30 pieces x 3 lot characterization data
Note 2: The sensor has an inherent low pass filter characteristic, which is very effective in attenuating out of band vibration.
Note 3: The thermal accelerometer sensors use heated gas molecules, and have no measurable resonance
Note 4: Indicates how closely X and Y axis sensitivities change over temperature

## ELECTRICAL SPECIFICATIONS:

(TA=25C, $V_{DD}$= 5V, unless otherwise specified. Typical values are specified at 25C)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Voltage | | 2.7 | | 5.5 | V |
| Supply Current | Operating Mode | | 0.8 | 3 | mA |
| | Sleep Mode | | 0.5 | 1 | uA |
| Operating Temperature | | -40 | | 85 | °C |
| A/D Sample Frequency (Fs) | | | 100 | | kHz |
| Output Data Rate | | | 100 | | Hz |
| Wake Time | (After exiting Sleep mode) | | 300 | 500 | ms |
| Power On Time | (After Vdd Rising Edge) | | 300 | 500 | ms |
| Power On Reset Threshold | | 0.8 | 1.2 | 1.6 | V |
| VDD Rise Time | (Note 5) | | | 8 | ms |

Note 5: Maximum allowable power supply rise time from 0.25V to 2.5V (minimum). Slower VDD rise time may cause erroneous data retrieval from OTP memory at power-up

## DIGITAL PARAMETERS (Note 6)

(TA=25C, $V_{DD}$= 5V, unless otherwise specified. Typical values are specified at 25C)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Logic Input Low | SDA, SCK Inputs | | 0 | 0.3*VIO | V |
| Logic Input High | SDA, SCK Inputs | 0.7*VIO | VIO | | V |
| Logic Output Low | SDA, INT, Sinking 0.5 mA (Note 7) | | | 0.1*VIO | V |
| Logic Output High | INT, Sourcing 0.5 mA (Note 7) | 0.9*VIO | | 1.1*VIO | |

Note 6: VIO is automatically detected using a peak-hold circuit on the SCK pin. The SCK or SDA voltage should not remain in the LOW state for more than 10ms.
Note 7: The output driver is capable of sourcing and sinking much higher currents, but it is recommended to keep the load current below 0.5mA to avoid thermal gradients which may affect the zero-g offset.

## DIGITAL SWITCHING CHARACTERISTICS

(TA=25C, $V_{DD}$= 5V, unless otherwise specified. Typical values are specified at 25C)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operating Valid Time (Note 8) | $t_{OP}$ | 30 | | | ms |
| SCK Clock Frequency | $f_{SCK}$ | 0.1 | | 400 | kHz |
| Rise Time | $t_R$ | | | 0.3 | µs |
| Fall Time | $t_F$ | | | 0.3 | µs |
| SCK Low Time | $t_{LOW}$ | 1.3 | | | µs |
| SCK High Time | $t_{HIGH}$ | 0.6 | | | µs |
| SDA Setup Time | $t_{SU;D}$ | 0.1 | | | µs |
| SDA Hold Time | $t_{H;D}$ | 0 | | 0.9 | µs |
| Start Setup Time | $t_{SU;S}$ | 0.6 | | | µs |
| Start Hold Time | $t_{H;S}$ | 0.6 | | | µs |
| Stop Setup Time | $t_{SU;P}$ | 0.6 | | | µs |
| Bus Free Time | $t_{BF}$ | 1.3 | | | µs |

Note 8: This is the wait time after VDD applied to communicate successfully over I2C interface.

## ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ($V_{DD}$) ……..-0.5 to +7V

Storage Temperature …..……-40°C to +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

## PIN DESCRIPTION

| Pin | Name | Description | I/O |
|---|---|---|---|
| 1 | INT | Interrupt Output. This pin will be low under normal operation, and will transition to high to alert to an orientation change event. A high impedance state reflects a fault condition in the sensor. This pin can be left open if not used. | O |
| 2 | NC | Factory use, connect to ground | |
| 3 | VDD | Positive power supply. Connect to 2.7V to 5.5V. Bypass this to ground using a 0.1uF capacitor | P |
| 4 | SCK | I2C clock input | I |
| 5 | SDA | I2C data pin (input/output) | I/O |
| 6 | GND | Connect to power supply ground. | P |

## RESPONSE TO VIBRATION

The MXC6245XU is unique in its vibration characteristics, due both to its sensor structure, and its signal processing features.

The MXC6245XU uses MEMSIC's proprietary thermal MEMS acceleration sensor, which uses heated gas molecules in a sealed cavity. This technology offers two distinct benefits: (a) The sensor has no detectable resonance, and (b) The sensor has an inherent low-pass frequency response, which provides very effective filtering of unwanted vibration signals prior to the electronic signal path. Below is the typical frequency response.

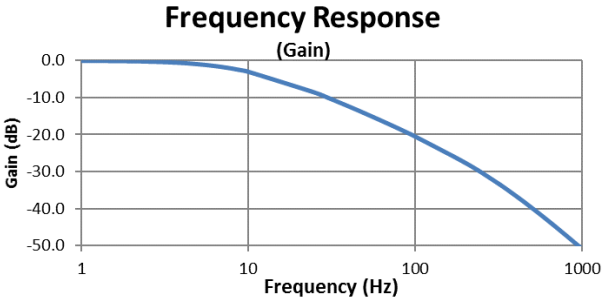



**FIGURE 2: MXC6245XU SENSOR FREQUENCY RESPONSE**

## I2C INTERFACE DESCRIPTION

The 7-bit I2C address for MXC6245XU is set as 0010101b.

A slave mode I2C interface, capable of operating in standard or fast mode, is implemented on the MXC6245XU. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bi-directional communication between master and slave devices. A master (typically a microprocessor) initiates all data transfers to and from the device, and generates the SCL clock that synchronizes the data transfer. The SDA pin on the MXC6245XU operates both as an input and an open drain output. Since the MXC6245XU only operates as a slave device, the SCL pin is always an input. There are external pull-up resistors on the I2C bus lines. Devices that drive the I2C bus lines do so through open-drain n-channel driver transistors, creating a wired NOR type arrangement.

Data on SDA is only allowed to change when SCL is low. A high to low transition on SDA when SCL is high is indicative of a START condition, whereas a low to high transition on SDA when SCL is high is indicative of a STOP condition. When the interface is not busy, both SCL and SDA are high. A data transmission is initiated by the master pulling SDA low while SCL is high, generating a START condition. The data transmission occurs serially in 8 bit bytes, with the MSB transmitted first. During each byte of transmitted data, the master will generate 9 clock pulses. The first 8 clock pulses are used to clock the data, the 9th clock pulse is for the acknowledge bit. After the 8 bits of data are clocked in, the transmitting device releases SDA, and the receiving device pulls it down so that it is stable low during the entire 9th clock pulse. By doing this, the receiving device "acknowledges" that it has received the transmitted byte. If the slave receiver does not generate an acknowledge, then the master device can generate a STOP condition and abort the transfer. If the master is the receiver in a data transfer, then it must signal the end of data to the slave by not generating an acknowledge on the last byte that was clocked out of the slave. The slave must release SDA to allow the master to generate a STOP or repeated START condition.

The master initiates a data transfer by generating a START condition. After a data transmission is complete, the master may terminate the data transfer by generating a STOP condition. The bus is considered to be free again a certain time after the STOP condition. Alternatively, the master can keep the bus busy by generating a repeated START condition instead of a STOP condition. This repeated START condition is functionally identical to a START condition that follows a STOP. Each device that sits on the I2C bus has a unique 7-bit address.

The first byte transmitted by the master following a START is used to address the slave device. The first 7 bits contain the address of the slave device, and the 8th bit is the R/W* bit (read = 1, write = 0; the asterisk indicates active low, and is used instead of a bar). If the transmitted address matches up to that of the MXC6245XU then the MXC6245XU will acknowledge receipt of the address, and prepare to receive or send data.

If the master is writing to the MXC6245XU then the next byte that the MXC6245XU receives, following the address byte, is loaded into the address counter internal to the MXC6245XU. The contents of the address counter indicate which register on the MXC6245XU is being accessed. If the master now wants to write data to the MXC6245XU it just continues to send 8-bit bytes. Each byte of data is latched into the register on the MXC6245XU that the address counter points to. The address counter is incremented after the transmission of each byte.

If the master wants to read data from the MXC6245XU it first needs to write the address of the register it wants to begin reading data from to the MXC6245XU address counter. It does this by generating a START, followed by the address byte containing the MXC6245XU address, with R/W* = 0. The next transmitted byte is then loaded into the MXC6245XU address counter. Then, the master repeats the START condition and re-transmits the MXC6245XU address, but this time with the R/W* bit set to 1. During the next transmission period, a byte of data from the MXC6245XU register that is addressed by the contents of the address counter will be transmitted from the MXC6245XU to the master. As in the case of the master writing to the MXC6245XU the contents of the address counter will be incremented after the transmission of each byte. The protocol for multiple byte reads and writes between a master and a slave device is depicted in FIGURE 3.

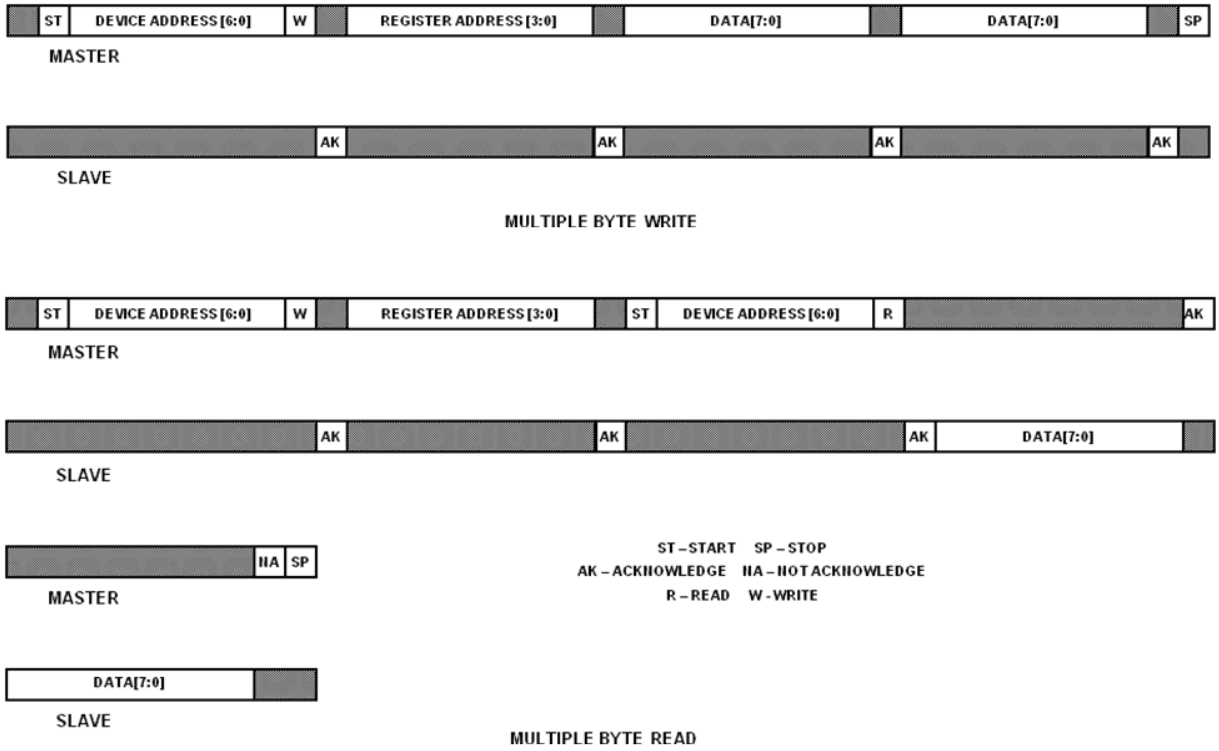



**FIGURE 3**

MXC6245XU I2C interface allows I2C interface voltage VIO to be lower than the supply voltage VDD. VIO can be as low as 1.62V. In order to achieve reliable operation, avoid the situation when both SCL and SDA pins are low for longer than 10ms. Please contact Memsic if you plan on using I2C interface voltage VIO greater than VDD.

## I2C REGISTER DEFINITION

The 7-bit I2C address for MXC6245XU is set as 0010101b.

The MXC6245XU has 10 user-accessible registers which are identified and summarized in the table below.

| Address | Name | Definition | Access |
|---|---|---|---|
| $00 | XOUT0 | Lower 8 bits of X acceleration output | read |
| $01 | XOUT1 | Higher bits of 12-bit X output | read |
| $02 | YOUT0 | Lower 8 bits of Y acceleration output | read |
| $03 | YOUT1 | Higher bits of 12-bit Y output | read |
| $06 | STATUS | Orientation and status | read |
| $07 | POWERDOWN | Low power sleep mode | write |
| $08 | Factory 8 | Factory use only | write |
| $0A | CLK_CONT | Control register | write |
| $10 | Who_Am_I | Allows electronic identification | read |

*User Register Summary*

Following is a more detailed description of the contents and function of each Register.

**Register $00**: XOUT0 – Lower 8 bits of x-axis acceleration output (read only)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| XOUT[7] | XOUT[6] | XOUT[5] | XOUT[4] | XOUT[3] | XOUT[2] | XOUT[1] | XOUT[0] |

**Register $01:** XOUT1 – Upper 4 bits of x-axis acceleration output (read only)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | XOUT[11] | XOUT[10] | XOUT[9] | XOUT[8] |

The number of bits in XOUT is fixed at 12 bits. Output is presented in 2's complement format. Bits 4 through 7 of register $01 are always zeroes.

**Register $02:** YOUT0 – Lower 8 bits of y-axis acceleration output (read only)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| YOUT[7] | YOUT[6] | YOUT[5] | YOUT[4] | YOUT[3] | YOUT[2] | YOUT[1] | YOUT[0] |

**Register $03:** YOUT1 – Upper 4 bits of y-axis acceleration output (read only)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | YOUT[11] | YOUT[10] | YOUT[9] | YOUT[8] |

The number of bits in YOUT is fixed at 12 bits. Output is presented in 2's complement format. Bits 4 through 7 of register $03 are always zeroes.

**Register $06:** STATUS –status register (read only)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| INT | CRC_OK | - | TILT | ORI[1] | ORI[0] | OR[1] | OR[0] |

OR[1:0] is a 2-bit indication of the device orientation, according to the following scheme: OR[1:0] = 00 – device is oriented in Region 1 (see FIGURE 4 below titled "Orientation Regions"); OR[1:0]=01 – device is in Region 2 (vertical in upright orientation); OR[1:0]=10 – device is in Region 3; OR[1:0]=11 – device is in Region 4 (vertical in inverted orientation). The bits OR[1:0] are indicative of "long-term" orientation when anti-dithering circuit is used.

The orientation is determined by measuring the quantities A*ax – B*ay, and A*ax + B*ay and comparing results to zero. The coefficients A and B are defined internally based on 45 degree threshold angle. In addition to these measurements, the orientation measurement must be validated by requiring that the larger in magnitude of ax, ay be greater than 3/8 g. When anti-dithering circuit is enabled in order for a new value of OR[1:0] to be written to the STATUS register, a valid measurement of the new orientation must be measured 16 consecutive times. This provides a low-pass filtering and hysteresis effect that keeps a display from flickering near orientation boundaries. If anti-dithering circuit is not enabled the OR[1:0] bits are the same as ORI[1:0].

TILT is an indication of whether there is enough acceleration signal strength to make a valid orientation measurement. If TILT = 0, the orientation measurement is valid, if TILT = 1, then the orientation measurement is invalid. TILT is updated every measurement cycle.

Accuracy of angle threshold detection is degraded above ±15 degrees of off axis tilt. At ±60 degrees of off axis tilt, orientation detection is disabled. See FIGURE 5 below. Refer to the section "USING MXC6245XU TO DETECT ORIENTATON" for a more detailed description.

ORI[1:0] is the instantaneous device orientation. It follows the same scheme as OR[1:0], except that it is updated every time a valid orientation measurement is made, not subject to the same anti-dithering filtering as OR[1:0].

CRC_OK is an indicator that OTP memory has loaded correctly and passed the CRC check. It transitions high approximately 10ms after power-up. If this bit stays low it is an indication of OTP memory failure. The part should not be trusted in such condition. It is recommended to read this bit 50ms after power-up to make sure it is high.

INT is low when OR[1:0] = 01, and is high otherwise. This serves as a rotate indicator when the part is mounted upright.

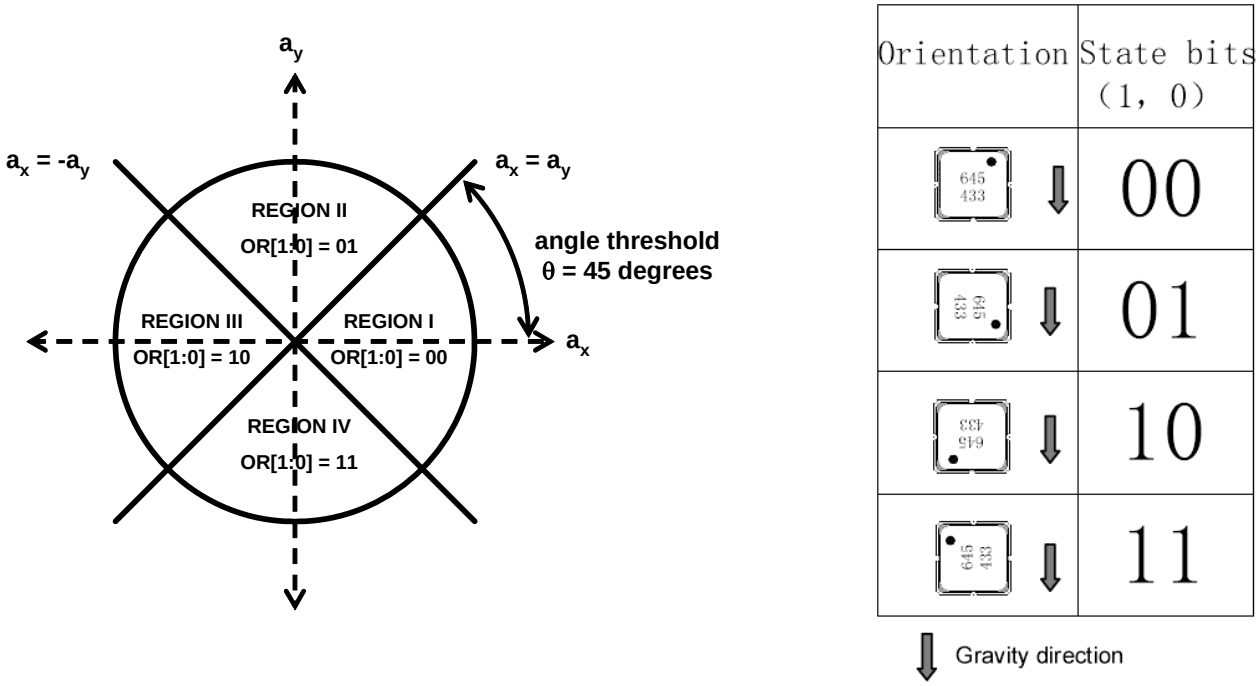



**FIGURE 4: Orientation Regions**

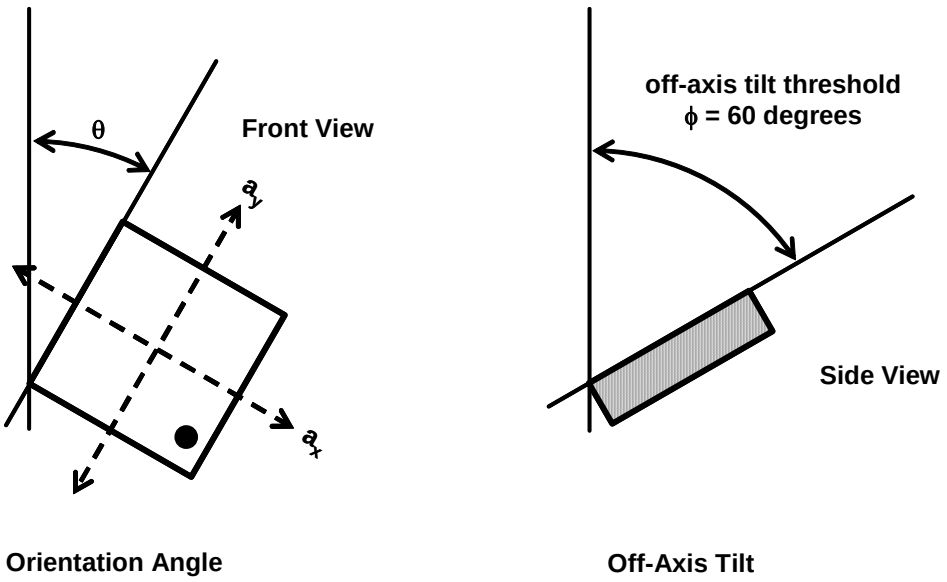



**FIGURE 5: Orientation Angle and Off Axis Tilt**

**Register $07:** POWERDOWN CONTROL (write only)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| PD | Dis_T_Comp | Self_Test | 0 | 0 | 1 | 1 | Dis_Or_INT |

PD = 1 powers down the MXC6245XU to a non-functional low power state with a maximum current drain of 1 uA.

Dis_T_Comp = 1 disables sensitivity temperature compensation. This is necessary to properly perform on-demand self-test. See Self-test section for details.

Self_Test = 1 enables on-demand self-test. When enabled, one of the four heaters in the sensor dissipates only a fraction of the power dissipated by the other 3 heaters thereby causing an offset shift.

Writing both PD = 1 and Self_Test = 1 will cause the Software Reset, similar to power-up. MXC6245XU will clear all registers and perform its startup routine, including OTP CRC check.

D4 – D1 should be written to 0011b after every power-up or Software Reset to ensure proper orientation detection.

Dis_Or_INT = 1 disables INT pin from changing its state when orientation changes. INT pin will not transition to high-z state if internal failure is detected

**Register $08:** FACTORY 8 - is a factory register. It should be written to 0x0F after every power-up or Software Reset.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Register $0A:** CLK_CONT – controls anti-dithering and orientation detection. This register need to be written to 0b xxx1 11xxb after every power down or reset event.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| x | x | x | 1 | 1 | 1 | OR_I2C | XY_Only |

XY_ONLY = 1 disables orientation detection and causes MXC6245XU to only measure X and Y acceleration values. ODR is 50 Hz when this bit = 0 and 100Hz when this bit =1.

ORC_I2C = 1 enables anti-dithering circuit. Filtered orientation indicator OR<1:0> will be updated after 16 identical consecutive readings of ORI<1:0>. Interrupt will also be updated based on slower OR<1:0> values. This is helpful to prevent screen flickering in a camera or cell phone.

**Register $10:** Who_Am_I – is a read-only register used to identify the MXC6245XU.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 1 | WAI[6] | WAI[5] | WAI[4] | WAI[3] | WAI[2] | WAI[1] | WAI[0] |

The value of WAI<6:0> is 0x10 and identifies the device as the MXC6245XU.

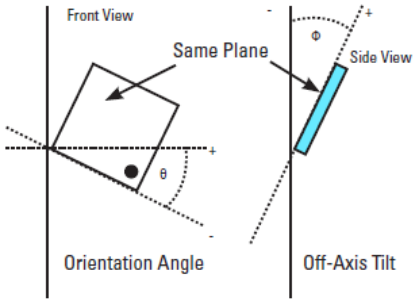
## USING MXC6245XU TO DETECT ORIENTATON

The MXC6245XU has built-in 45 degree angle thresholds which can be used to generate an interrupt or determine the orientation of the device.

To use this mode of operation, the MXC6245XU must be mounted as shown in the figure below, with the y-axis in vertical-upright location (for zero inclination).

The status of the angle threshold can be read either via the I2C bus (bit D7 in Register $06) or by the state of the INT output pin.

MOUNTING ORIENTATION
(Threshold Angle = Θ below)
(Off-Axis Tilt = Φ below)




Off-axis tilt is the angle of the x-y plane of the device from vertical (See figure above). As off-axis tilt increases from 0 to 90 degrees, the magnitude of the acceleration vector in the x-y plane decreases. If the acceleration signal is too small, an accurate determination of orientation cannot be made. Angle accuracy is degraded when off-axis tilt angle exceeds ±15 degrees. Orientation detection is disabled if off axis tilt exceeds approximately ±60 degrees.

## INTERNAL FAULT DETECTION

The MXC6245XU has an internal fault detection circuit features.

On power up (within 10ms of a valid supply voltage appearing on the VDD pin), the internal circuitry checks for the following condition:

- Valid non-volatile memory contents. On power up a CRC algorithm checks if any of the bits have changed from their factory programmed values. If this check is completed successfully the CRC_OK bit is set in the Status register. If this test fails, the output INT will go to a high impedance state until the power supply is removed, or the part is reset via the I2C interface. Note this CRC check cannot be disabled by the user.

It is recommended to check the status of the CRC_OK bit 50 ms after power on or SW reset to make sure it is set.

## SELF-TEST DETAILED DESCRIPTION-INITIATING ON-DEMAND SIGNAL PATH SELF-TEST

The basic principle of the on-demand self-test is to reduce power to one of the four internal heater elements, inducing a gross offset change, equivalent to approximately +2g on the X channel, and -2g on the Y channel. These offsets can be read via the X and Y I2C registers (see the section “I2C REGISTER DEFINITION” for a complete description). In this way the sensor and the signal processing electronics can be checked for functionality. In addition, these offsets may cause the INT output to change state.

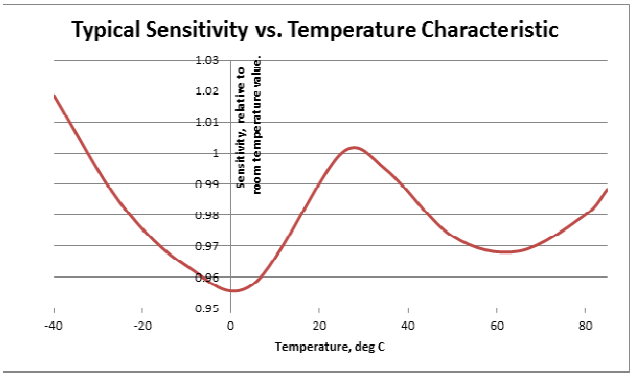
An on-demand self-test is executed by the following 6-step procedure:

- *Step 1:* Disable Temperature Compensation (Set the control register bit Dis_T_Comp=1). This step is necessary because the internal temperature compensation function interferes with the self test results.
- *Step 2:* Read the X and Y acceleration values (call them OUTX1 and OUTY1).
- *Step 3:* Enable Self-Test (Set the control bit ST=1), while leaving Temperature Compensation disabled (Dis_T_Comp=1)
- *Step 4:* Wait approximately 300 ms for the X and Y sensor channels to settle, then read the X and Y acceleration values (call them OUTX2 and OUTY2)
- *Step 5:* Subtract OUTX1 from OUTX2 and OUTY1 from OUTY2. These values are the X and Y self-test amplitudes. A dramatic shift (>100mg) in either the X or Y self-test amplitudes over time indicates a fault in the sensor or signal processing electronics
- *Step 6:* Return the device to normal operation (set Dis_T_Comp=0 and ST=0)

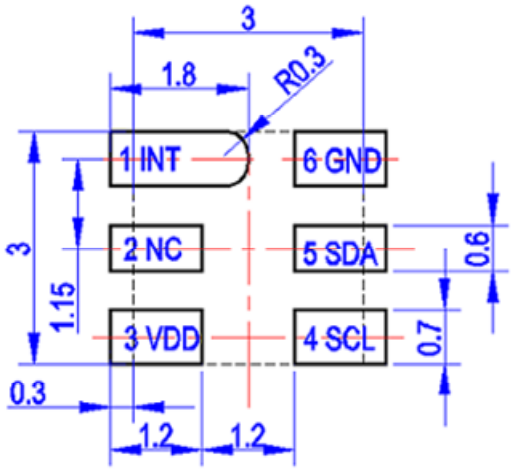
Using the above method, the presence of a real constant acceleration stimulus does not affect the ST amplitude, provided that (a) the acceleration plus self-test signal is not so large that the signal path is saturated, and (b) the external acceleration does not change dramatically over the self test period.

## SENSITIVITY TEMPERATURE COMPENSATION

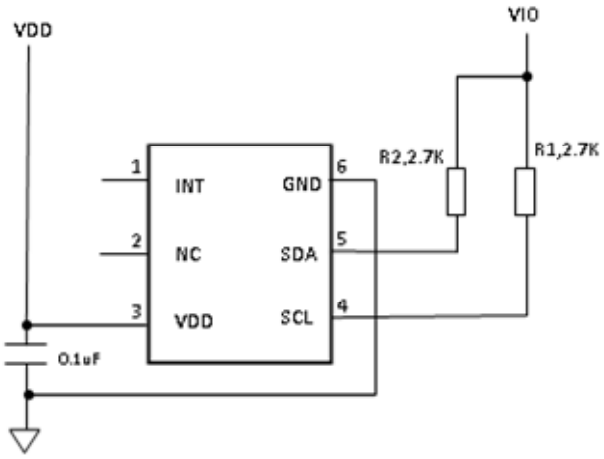
Thermal accelerometers exhibit significant change of sensitivity with temperature. The MXC6245XU includes internal temperature compensation circuitry. Sensitivity change versus temperature for a typical part with internal compensation is shown below.



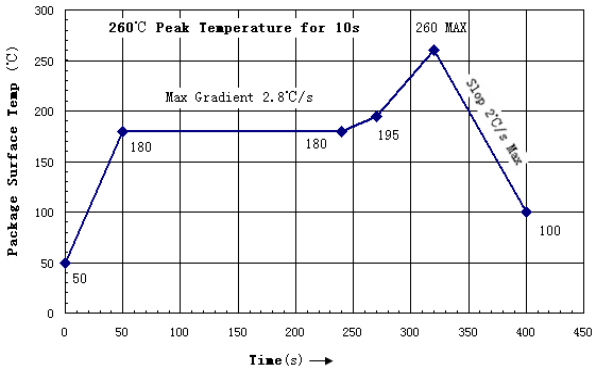

## LANDING PATTERN (Unit: mm)




## CIRCUIT SCHEMATIC




## REFLOW PROFILE




**Notes**:

- Reflow is limited to two cycles.
- If a second reflow cycle is implemented, it should be applied only after device has cooled down to 25℃ (room temperature)
- Figure 8 is the reflow profile for Pb free process
- The peak temperature on the sensor surface must be limited to under 260℃ for 10 seconds. Follow solder paste supplier's recommendations for the best SMT quality.
- When soldering manually or repairing via soldering iron for the accelerometer, the time must be limited to less than 10 seconds and the temperature must not exceed 275℃. If a heat gun is used, the time must be limited to less than 10seconds and the temperature must not exceed 270℃
- Avoid bending the PCB after sensor assembly

**MARKING ILLUSTRATION AND PACKAGE DRAWING:**