Specification

Model S110D

P/N SD-H90NH-1A8

- True VGA ToF camera module
- Wide FoV design

S110D image of the development version

Revision History

Date	Ref. Page	Description	Remark
21-05-06	-	Draft write	
21-05-25	9, 10, 22	Added Measurement Range, RK1109	
21-06-02	29	Changed Host board connector	

Contents

Contents

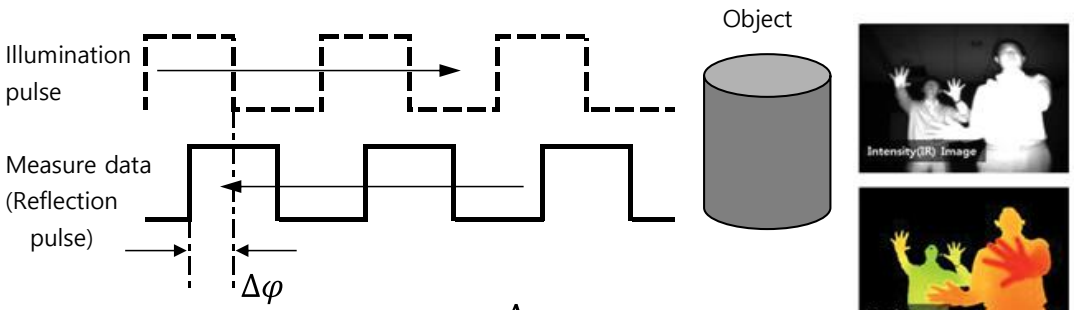
Figures

Tables

1. Introduction

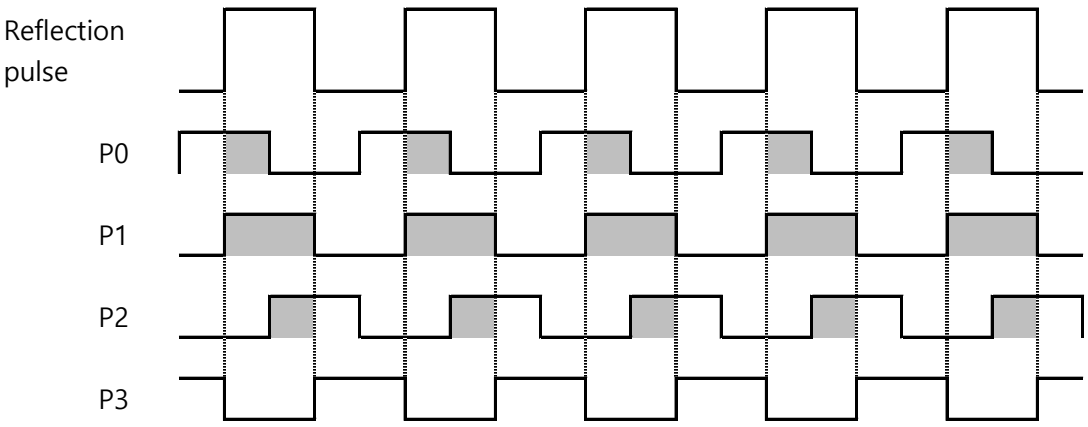
1.1. ToF 3D technology overview

3D time-of-flight (ToF) cameras illuminate an object or a scene with a modulated light source and observe the light reflected from the object. This is achieved via a laser diode illuminator and a receiver. The phase shift between the emitted light and reflected light is measured and translated to distance. This camera can measure an object's distance by pixel unit.



$$\text{distance to object [d]} = \frac{c}{2}\frac{\Delta\varphi}{2\pi f}$$

Fig 1. Principles of indirect Time of Flight



A0 is digital value measured at the P0 photogate $\varphi = tan^{-1}(\frac{A_1 - A_3}{A_0 - A_2})$

Fig 2. ToF demodulation using 4-phase sampling

1. Introduction

1.2. System block diagram

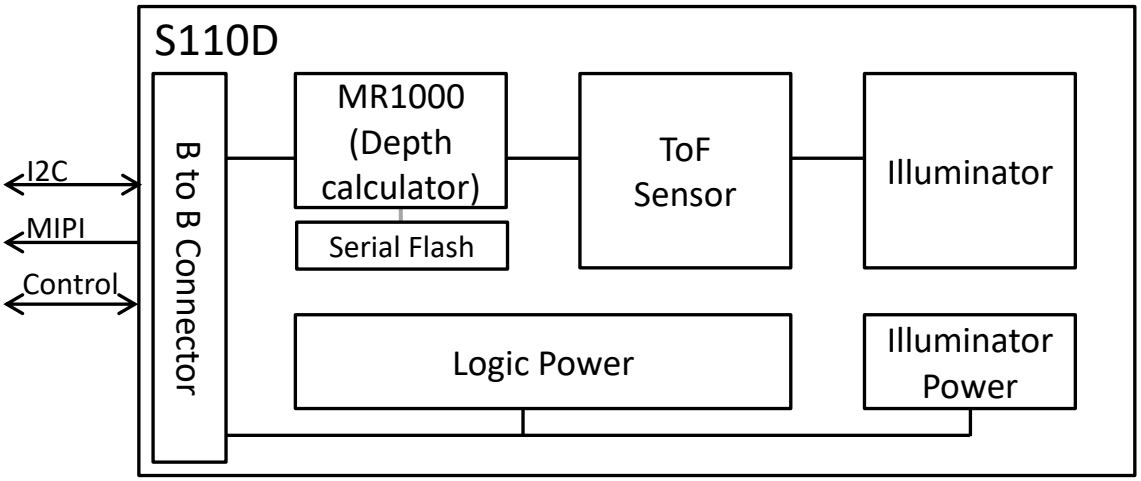


Fig 3. System block diagram

Parts	Summary
Illuminator	2W VCSEL(package with PD)
ToF sensor	VGA, 4 phase data out, global shutter
MR1000	Depth calculation
Serial Flash	MR1000 bootloader, calibration parameter
Power	Illuminator/Sensor/MR1000 Power
B to B Connector	Connector for host interface

Table 1. Main parts specification summary

2. General Specification

ToF Sensor		
Type of sensor	Samsung System LSI S5K33DXX	
Resolution	VGA (640x480), unit pixel size : 7.0 um	
Illumination		
Source	2W VCSEL	
Wavelength	940 nm	
Modulation frequency	80 MHz, 100 MHz	
Optics		
FOV (H x V)	90˚ x 68˚	
Measurement Range	F#1.25 Lens	0.2 ~ 3.0 m
	F#1.70 Lens	0.2 ~ 2.0 m
Accuracy		
0.2 ~ 0.5 m	<± 10 mm	※ Measurement condition - Target : flat screen of >70 % reflectivity - Target area : 7x7 central pixels - Number of data acquisition : 20 frames - Ambient illumination : normal indoor - Ambient temperature : 23 ~ 25℃
0.5 ~ 2.0 m	<± 1.0% by distance	
Interface		
Control interface	I2C 400 Kbps	
Data interface	MIPI CSI-2 2 lanes, 500 Mbps/lane	
Power		
Input	DC 5V 3A	
Power consumption	Average 1.5 W, peak 15 W (TBD)	
Temperature		
Operating Tem.	0 ~ 60℃	
Storage Tem.	-20 ~ 70℃	
Size		
Dimensions	63.0 x 15.0 x 22.0 ㎜³	
Weight	10g(TBD)	
USB 3.0 Bridge board (Option)		
Dimensions	50.0 x 23.0 x 8.6 ㎜³	
Interface	USB 3.0 C type	
Input power	DC 5V 5A (adaptor)	
Software (SDK for USB connecting user)		
Operation system	Windows 10, Ubuntu	
Output data	Raw 10 bits	

Table 2. Information of general specification

3. Component Specification

3.1. Main component

ToF sensor	VGA, 4:3 ratio, Active area 1/3.2"
	Electric global shutter
	ADC accuracy : 10bits
	Control I2C : max 1 MHz
Lens	F number : 1.7 & 1.25
	Focal Length : 4.13mm
	Horizontal Field of View : 90°
	Vertical Field of View : 68°
	Diagonal Field of View : 109°
Illuminator	Illuminator wavelength : 940 nm
	SIP configuration : VCSEL, diffuser, VCSEL driver IC, PD
	Laser compliance : Eyesafety class 1

Table 3. Main components description

3.2. MR1000 calculating depth

There are 2 lanes of each Rx/Tx of MIPI on-chip in MR1000.
It also contains depth engine, image correction, post image filter, cartesian coordinate conversion and memory for frame buffer as well as memory controller.

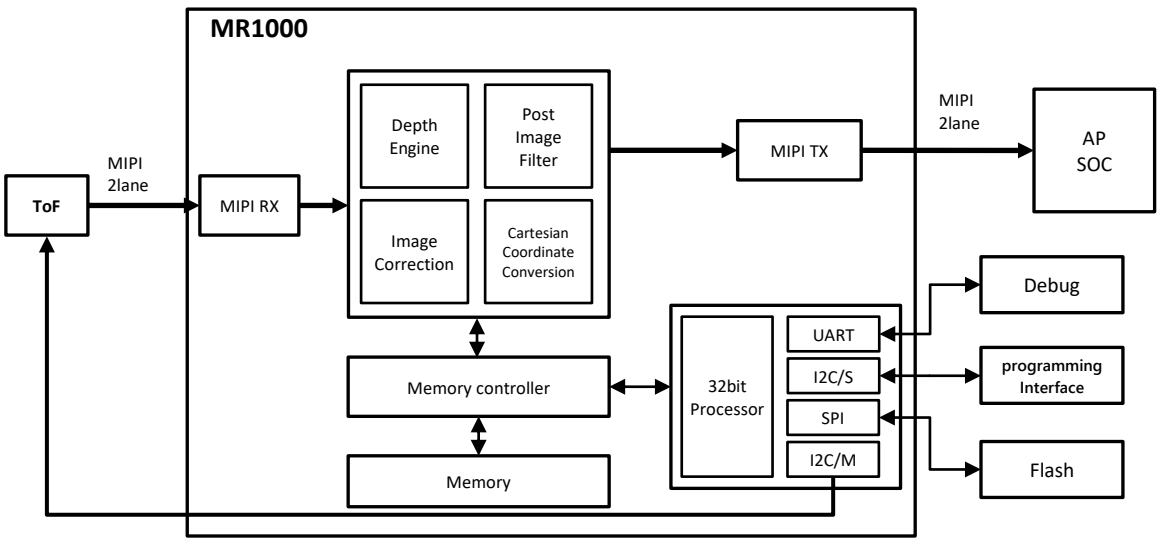


Fig 4. MR1000 block diagram

4. Functional Specification

4.1. MIPI CSI-2 output

- Support MIPI DPHY v1.1 and MIPI CSI-2 v1.1 RAW10
- 80Mbps to 500Mbps with 2-lane selectable

4.2. High speed depth calculation using MR1000

- Support resolution VGA
- Depth calculation in spherical coordinate
- Amplitude/Intensity data ouput
- Depth correction
- Temperature compensation
- Low motion blur(Single frequency mode)
- Noise/TNR/spatial filter selectable
- Cartesian coordinate conversion(Point cloud)

5. Operation

5.1. Initialization

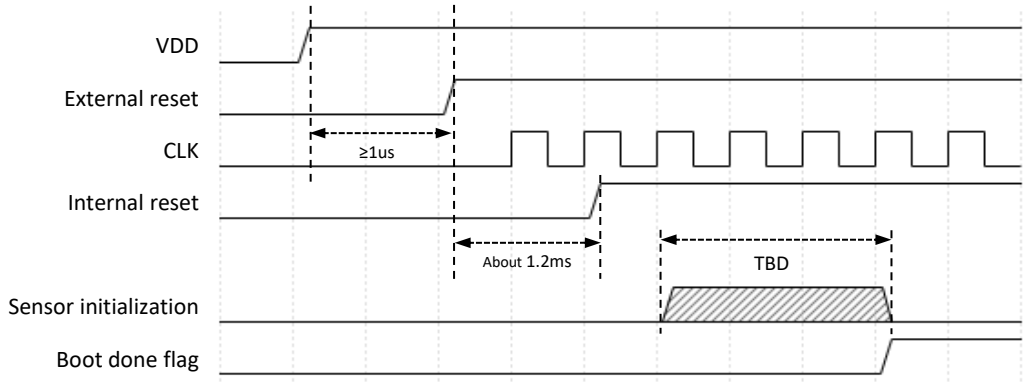


Fig 5. Power on sequence, sensor boot time

After power on, and when external reset is “High”, CLK comes in and internal reset will be "High" after 1200 us (CLK at 24 MHz standard). All processes will work when the internal reset is high.

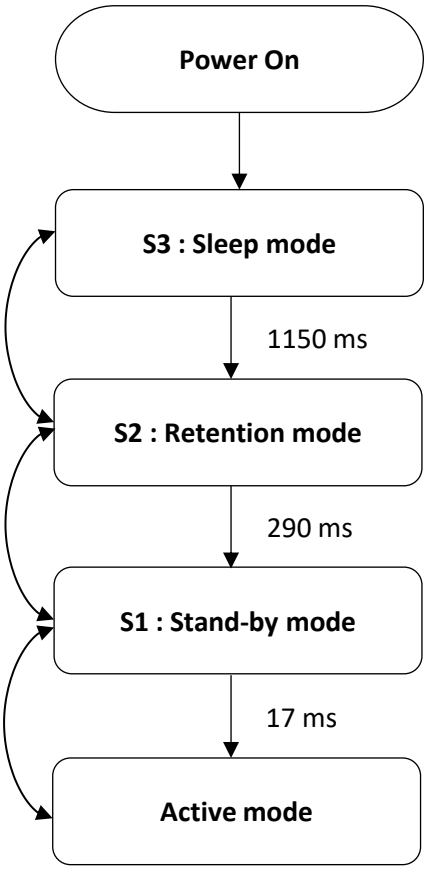
Booting is complete if the status of the boot done flag is '1'. Proceed with protocol work after checking boot done register status.

5.2. Operation(Boot) Mode

Mode	Description	Switching time	Power consumption
S3	Sleep mode : Minimum power consumption	off → S3 100 ms under	280 mW
S2	Retention mode : Minimum boot time	S3 → S2 1150 ms	340 mW
S1	Stand-by mode : Active ready	S2 → S1 290 ms	430 mW

Table 4. Operation mode description

5. Operation



Each mode can only be moved in sequential order

Fig 6. Boot mode diagram

6. I2C Control Protocol

6.1. Protocol description

Description	Start		Length		CMD		Address				Check sum		Data
Size(Byte)	2		2		2		4				2		0~63
Byte order	0	1	2	3	4	5	6	7	8	9	10	11	12-76
	L	H	L	H	L	H	L	H	L	H	L	H	L-H

Table 5. Protocol header

Action	Start	Length	CMD	Address	Check sum	Data
Register setting	0xB0A1	0x0002	0x0006	0x0000****	0x0000	0x****
Illumination	0xB0A1	0x0001	0x0007	0x00000000	0x0000	1:ON, 0:OFF
MIPI TX Mode	0xB0A1	0x0001	0x0009	0x00000000	0x0000	0 : 2560 1 : 1280 2 : 640
MIPI TX reset	0xB0A1	0x0001	0x000A	0x00000000	0x0000	1
Auto exposure	0xB0A1	0x0001	0x000C	0x00000000	0x0000	1:ON, 0:OFF
Sleep mode	0xB0A1	0x0001	0x000D	0x00000000	0x0000	0 : Active 1 : S1 2 : S2 3 : S3
Register reset (default)	0xB0A1	0x0001	0x000E	0x00000000	0x0000	1

Table 6. Protocol action

6. I2C Control Protocol

6.2. Example

Slave address 0xE0 (Write)
0xE1 (Read)

Ex1) Register write(address 0x1122, data 0x33445566)

Protocol name	Slave	Start		Length		CMD		Address				Check sum		Data
Byte order(Write)	-	0	1	2	3	4	5	6	7	8	9	10	11	12
Register write	0xE0	0xA1	0xB0	0x01	0x00	0x06	0x00	0x22	0x11	0x00	0x00	0x00	0x00	0x66554433
Illumination on	0xE0	0xA1	0xB0	0x01	0x00	0x07	0x00	0x00	0x00	0x00	0x00	0x00	0x00	1
MIPI TX mode 0	0xE0	0xA1	0xB0	0x01	0x00	0x09	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0
MIPI TX reset	0xE0	0xA1	0xB0	0x01	0x00	0x0A	0x00	0x00	0x00	0x00	0x00	0x00	0x00	1
Auto exposure on	0xE0	0xA1	0xB0	0x01	0x00	0x0C	0x00	0x00	0x00	0x00	0x00	0x00	0x00	1
Auto exposure off	0xE0	0xA1	0xB0	0x01	0x00	0x0C	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0
Sleep mode active	0xE0	0xA1	0xB0	0x01	0x00	0x0D	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0
Sleep mode S1	0xE0	0xA1	0xB0	0x01	0x00	0x0D	0x00	0x00	0x00	0x00	0x00	0x00	0x00	1

Table 7. Protocol write

Protocol name	Slave	Address				Slave	Return size	Description
Byte order(Write)	-	0	1	2	3	-	-	
Register read	0xE0	0xA1	0xB2	0x11	0x22	0xE1	4	read address(0x2211)
Product name	0xE0	0xA1	0xB3	0xF0	0xF2	0xE1	8	000S110D(ASCII)
Firmware version	0xE0	0xA1	0xB3	0xF1	0xF2	0xE1	5	year/month/day/major/minor
Serial number	0xE0	0xA1	0xB3	0xF2	0xF2	0xE1	6	
Boot done	0xE0	0xA1	0xB3	0xF1	0xF1	0xE1	1	0 : not boot, 1 : boot

Table 8. Protocol read

7. MIPI interface

7.1. MIPI TX specification

- MIPI D-PHY 1.17 Nov 2011 compliant
- Forward (Unidirectional) high-speed only (LPDT/ULPS not support)
- HS diff.swing 200mV, HS common level 200mV
- Raw 10 data type supported
- Resolution mode
  mode 0 : 2560x961
  mode 1 : 1280x961
  mode 2 : 640x961
- Frame rate : 30 fps
- MIPI CSI-2 2-lane (500Mbps/lane)
- First line : embedded frame head

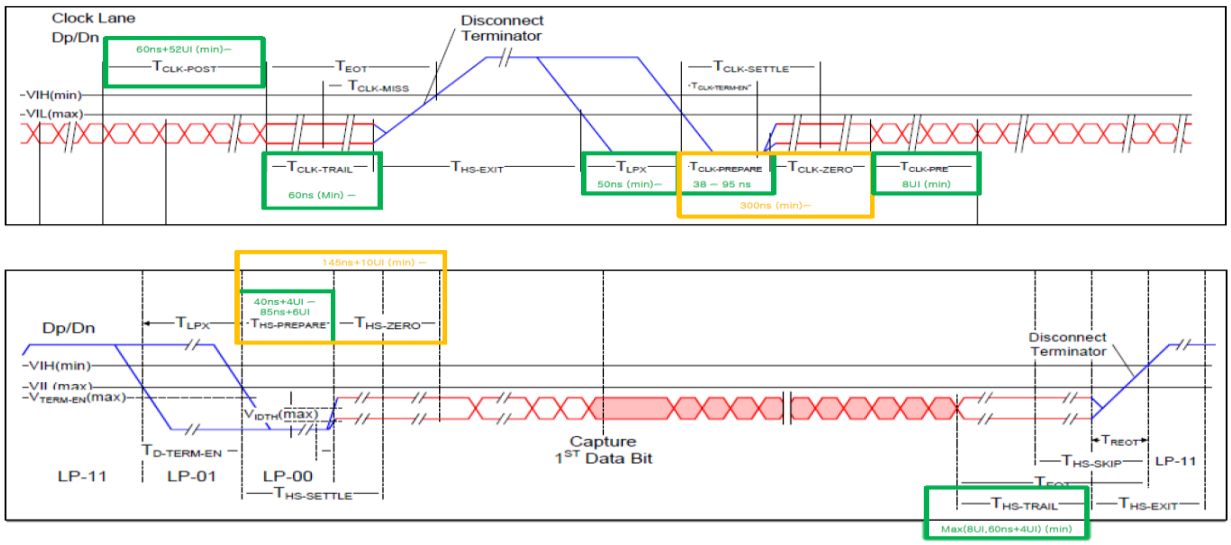


Fig 7. MIPI TX operation TX signal timing

8. Register Map

8.1. Register information

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default value	Access
0x0028	amp_max_limit																amp_min_limit																0xFFFF0000	R/W
0x0029	depth_max_limit																depth_min_limit																0xFFFF0000	R/W
0x002A	scat_threshold																Reserved																0x00000200	R/W
0x0030	depth_error_threshold																																0xFFFFFFFF	R/W
0x0031	Reserved																											*1	*2	*3	*4		0x0DAC000F	R/W
0x0033	Reserved																g_offset																0x80000000	R/W
0x0039																	flying pixel_threshold																0x0000FFFF	R/W
0x003A																											temporal_mblur						0x02000020	R/W
0x003B																							mci_thresh										0x00000000	R/W
0x003D	multi_freq_ctrl																																0xFF000C80	R/W
0x0042	*5																Reserved																0x00001D4C	R/W
0x0046	set_tx_mode				data_format_sel												vcycle_dly																hcycle_dly										0x10003032	R/W
0x0041																	firm_rev_no																Reserved											R
0x00AD																																BD		R
0x0127																																	mci_flag											R

*1 : filter3 *2 : remove flying pixel *3 : filter2 *4 : filter1 *5 : filter3_ctrl

Table 9. Register information

8. Register Map

8.2. Register description

8.2.1. Amplitude threshold control registers

Register Name	Address	Bit	Default	Description
amp_max_limit	0x0028	[31:16]	0xFFFF	More than the set value, depth = 0 if(amplitude > amp_max_limit) depth = 0 else depth = depth
amp_min_limit	0x0028	[15:0]	0x0000	Less than the set value, depth = 0 if(amplitude < amp_min_limit) depth = 0 else depth = depth

Table 10. Amplitude threshold register setting

8.2.2. Depth threshold control registers

Register Name	Address	Bit	Default	Description
depth_max_limit	0x0029	[31:16]	0xFFFF	More than the set value, depth = 0 if(depth > depth_max_limit) depth = 0 else depth = depth
depth_min_limit	0x0029	[15:0]	0x0000	Less than the set value, depth = 0 if(depth < depth_min_limit) depth = 0 else depth = depth

Table 11. Depth threshold register setting

8.2.3. Scattering threshold control registers

Register Name	Address	Bit	Default	Description
scat_threshold	0x002A	[31:16]	0xFFFF	scat amplitude = Internally calculated value if(scat amplitude < scat_threshold) depth = 0 else depth = depth
Reserved	0x002A	[15:0]	0x0200	Do not change

Table 12. Scattering threshold register setting

8.2.4. Depth error threshold control registers

Register Name	Address	Bit	Default	Description
depth_error_threshold	0x0030	[31:0]	0xFFFFFFFF	error coefficient = Internally calculated value if(error coefficient > depth_error_threshold) depth = 0 else depth = depth

Table 13. Depth error threshold register setting

8. Register Map

8.2.5. Image filter control registers

Register Name	Address	Bit	Default	Description
Reserved	0x0031	[31:16]	0x0DAC	Do not change
Reserved	0x0031	[0]	0x1	Do not change
Reserved	0x0042	[15:0]	0x1D4C	Do not change
filter 3	0x0031	[4]	0x0	noise filter 3 on/off 1 = on, 0 = off
filter3_ctrl	0x0042	[31]	0x0	noise filter 3 change 1 = gaussian filter, 0 = default filter
remove flying pixel	0x0031	[3]	0x1	remove flying pixel on/off 1 = on, 0 = off
flying pixel_threshold	0x0039	[15:0]	0xFFFF	flying pixel coefficient = Internally calculated value if(flying pixel coefficient > flying pixel_threshold) depth = 0 else depth = depth
filter 2	0x0031	[2]	0x1	noise filter 2 on/off 1 = on, 0 = off
filter 1	0x0031	[1]	0x1	noise filter 1 on/off 1 = on, 0 = off

Table 14. Image filter register setting

8.2.6. Depth offset control registers

Register Name	Address	Bit	Default	Description
Reserved	0x0033	[31:16]	0x8000	Do not change
g_offset	0x0030	[15:0]	0x0000	Global offset value, Adds or subtracts from the depth value according to the set value (scale : 1mm).

Table 15. Depth offset register setting

8. Register Map

8.2.7. Motion blur control registers

Register Name	Address	Bit	Default	Description
temporal_mblur	0x003A	[7:0]	0x20	Temporal motion blur weight The motion blur is reduced as smaller input value (Input value range : 0x00 ~ 0xFF) As the input value decreases, the deviation of depth increases.
multi_freq_ctrl	0x003D	[31:23]	0x30	Multi-frequency motion blur weight The motion blur is reduced as smaller input value (Input value range : 0x00 ~ 0xFE) When set to 0XFF, multi-Frequency motion blur is completely removed, but aliasing always occurs. As the input value decreases, aliasing for moving objects increases.
multi_freq_ctrl	0x003D	[22:16]	0x01	Do not change

Table 16. Motion blur register setting

8.2.8. Multi camera interference control registers

Register Name	Address	Bit	Default	Description
mci_thresh	0x003B	[12:0]	0x00	mci threshold value mci_flag is generated by comparing the difference value between a the previous frame and the current frame. The difference value is the average value of a specific area. if (|frame (N-1) - frame(N)| > mci thres value) mci_flag = '1' else mci_flag = '0'
mci_flag	0x0127	[3:0]	0x00	mci_flag consists of 4 bits, and each bit is the area information as follows. mci_flag[0] : area 1(left up side) mci_flag[1] : area 2(right up side) mci_flag[2] : area 3(left down side) mci_flag[3] : area 4(right down side)

Table 17. Multi camera interference reducing register setting

8. Register Map

8.2.9. Output data format control registers

Register Name	Address	Bit	Default	Description
set_tx_mode	0x0046	[31:28]	0x1	MIPI TX Resolution Selection 0x1 : XYZA 2560 * 961 0x2 : ZA 1280*961 0x4 : Z 640* 961
data_format_sel	0x0046	[0]	0x0	set_dist_sel[0] : Depth Output Selection 0x1 : R(Radial distance) 0x0 : Z(Point cloud)
		[1]	0x0	set_dist_sel[1] : Amplitute Output Selection 0x0 : Amplitute 0x1 : Intensity
		[3:2]	0x0	set_dist_sel[3:2] : MIPI TX Frame Selection 0x1 : 15 Fps 0x2 : 7.5 Fps default : 30 Fps
vcycle_dly	0x0046	[23:12]	0x000	vertical delay value Use it when setting the MIPI TX mode.
hcycle_dly	0x0046	[11:0]	0x000	horizontal delay value Use it when setting the MIPI TX mode.

Table 18. Output data format register setting

8.2.10. Information register

Register Name	Address	Bit	Default	Description
firm_rev_no	0x0041	[27:16]	0x21	firmware version information
BD	0x00AD	[0]	0x1	Boot status information 0x01 : idle, 0x01 : Boot done
sleep mode	TBD	TBD	TBD	sleep mode status information

Table 19. Module information register

9. Software(SDK)

9.1. Conditions of the example code (MIPI connection)

Environment

- Linux kernel version : 4.4.189
- V4L2 compatible
- Rockchip RK1109 compatible

Information

- file name : tof_lsi_mipi.c

9.2. CubeEye software development kit (USB3.0 connection)

libCubeEye is a cross-platform library for working with CubeEye camera (include S110D).

※ The SDK at a minimum includes :

- CubeEyeShell : This application can be used view, debug and set camera configurations and other controls.
- Code Examples : Examples to demostrate the use of SDK to include S110D snippets into applictions.
- Doc : Documents for use the SDK.

10. System Integration

10.1. System level block diagram

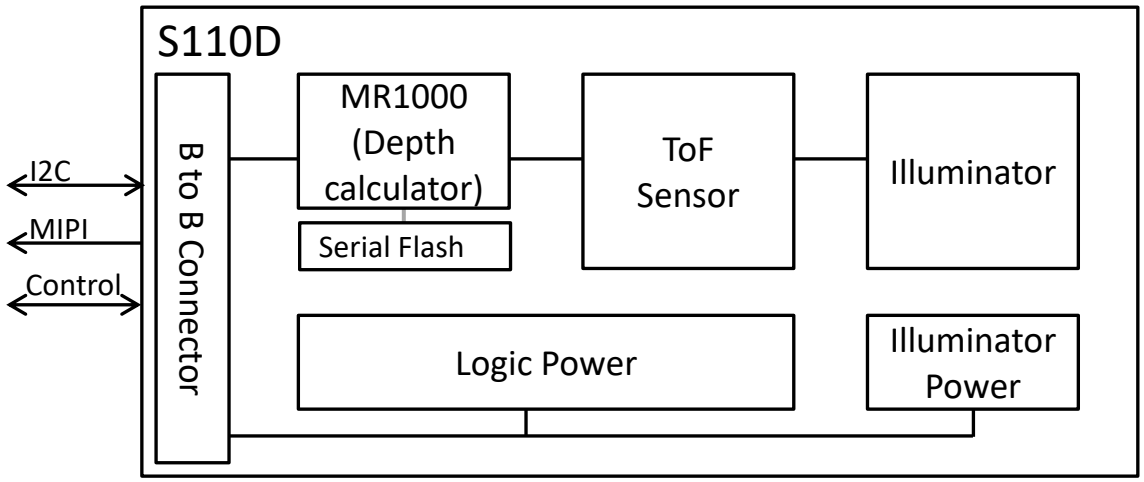


Fig 8. S110D system block diagram

10.2. System power

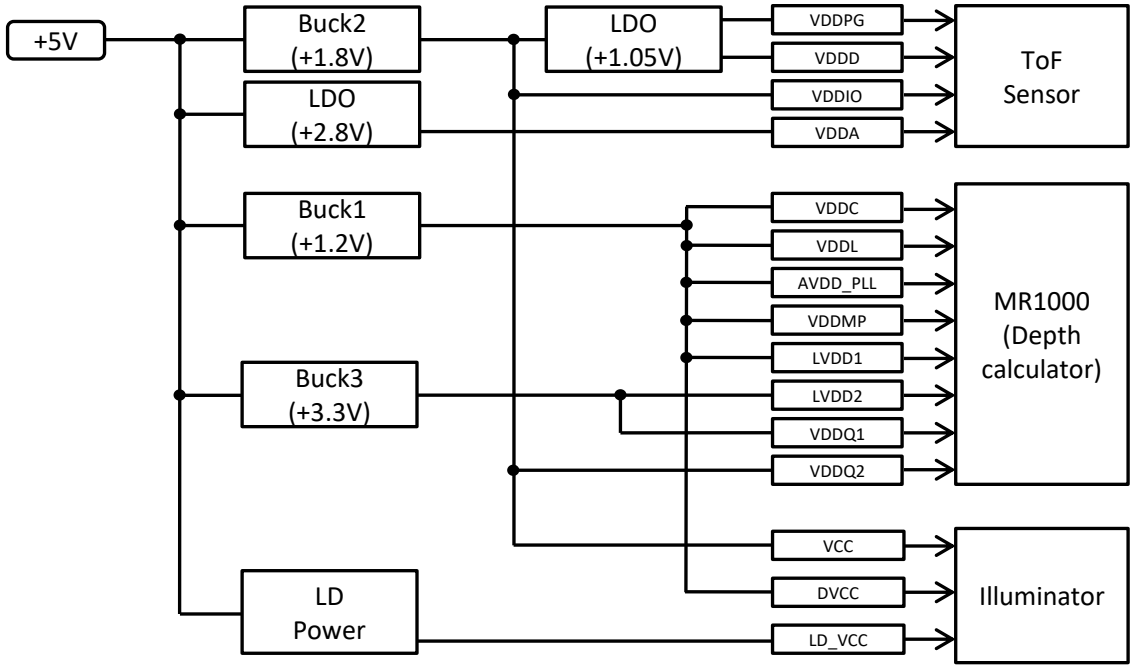


Fig 9. S110D system power

10. System Integration

10.3. B to B connector pin map(BBR50-04001-001)

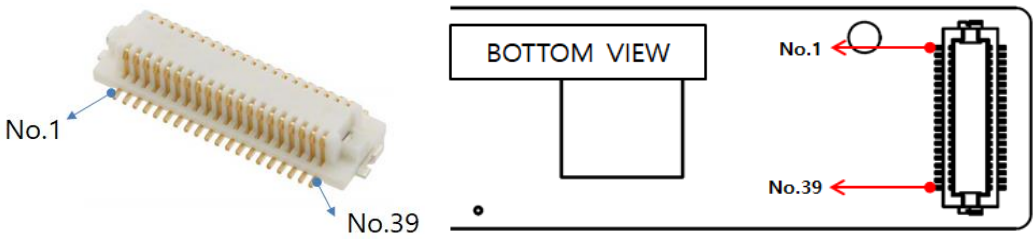


Fig 10. B to B connector No.1 position

Name	No.		Name
+5V	1	2	GND
+5V	3	4	GND
+5V	5	6	GND
+5V	7	8	GND
+5V	9	10	GND
+5V	11	12	GND
+5V	13	14	GND
GND	15	16	GND
LVDS_RX_P	17	18	LVDS_TX_P
LVDS_RX_N	19	20	LVDS_TX_N
GND	21	22	GND
MIPI_DATA0_P	23	24	Boot done
MIPI_DATA0_N	25	26	RESET
GND	27	28	LD Enable
MIPI_CLK_P	29	30	GPIO0
MIPI_CLK_N	31	32	GPIO1
GND	33	34	GPIO2
MIPI_DATA1_P	35	36	I2C_SDA
MIPI_DATA1_N	37	38	I2C_SCL
GND	39	40	Sync Input

Table 20. B to B connector pin map

10. System Integration

10.4. B to B connector pin information

Name	Description	Electrical Characteristics
+5V	ToF Module Power Input	5V/3A
MIPI_DATA0_N	MIPI data lane 0(negative)	MIPI
MIPI_DATA0_P	MIPI data lane 0(positive)	MIPI
MIPI_CLK_N	MIPI clock lane(negative)	MIPI
MIPI_CLK_P	MIPI clock lane(positive)	MIPI
MIPI_DATA1_N	MIPI data lane 1(negative)	MIPI
MIPI_DATA1_P	MIPI data lane 1(positive)	MIPI
LVDS_TX_P	Differential modulation clock output(positive)	LVDS
LVDS_TX_N	Differential modulation clock output(negative)	LVDS
LVDS_RX_P	Differential modulation clock input(negative)	LVDS
LVDS_RX_N	Differential modulation clock input(positive)	LVDS
Boot done	Booting Done : Active High	1.8V
RESET	Reset : Active Low	1.8V
LD ENABLE	Laser Diode(VCSEL) Enable : Active Low	1.8V
GPIO	General Purpose I/O	1.8V
I2C_SDA	I2C Serial Data(Slave)	1.8V
I2C_SCL	I2C Serial Clock(Slave)	1.8V
Sync Input	Second camera SYNC signal : Input	1.8V

Table 21. B to B connector pin information

11. Design Guidelines

11.1. LVDS line PCB design guide(Mandatory)

- Assign those two pair of pins as close as possible, to be connected in the shortest path on the host PCB.
- Line length should be the same.
- Design with an impedance of 100 ohm.

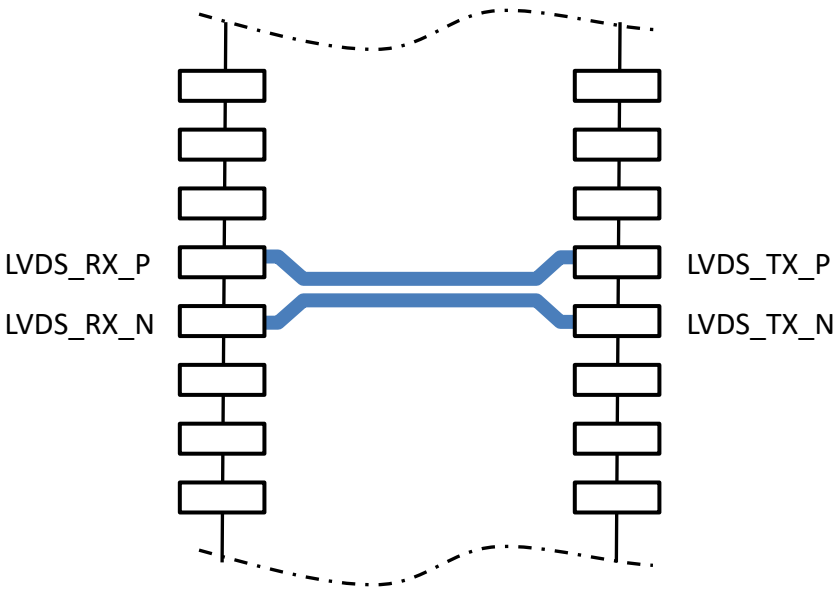


Fig 11. Host PCB LVDS line design guide

11.2. MIPI signals artwork guide

- Keep the length difference of the differential traces less than 1mm.
- Design with an impedance of 100 Ω

11.3. Notes on design

- Design the host PCB, the connector pin 1 position should not be changed
- The specified power must be supplied to the ToF camera module

12. Mechanical Drawings

12.1. Schematic

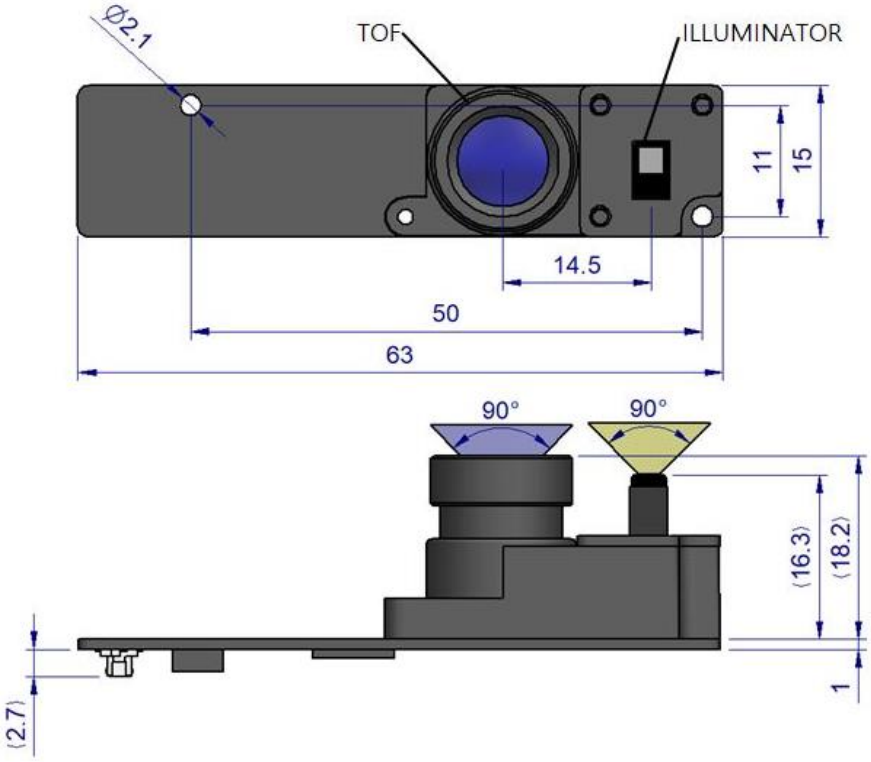


Fig 12. S110D dimension and schematic

12.2. Physical z=0 plane

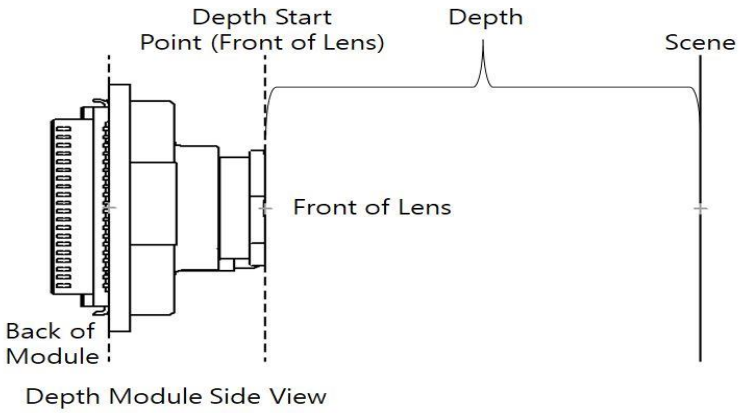
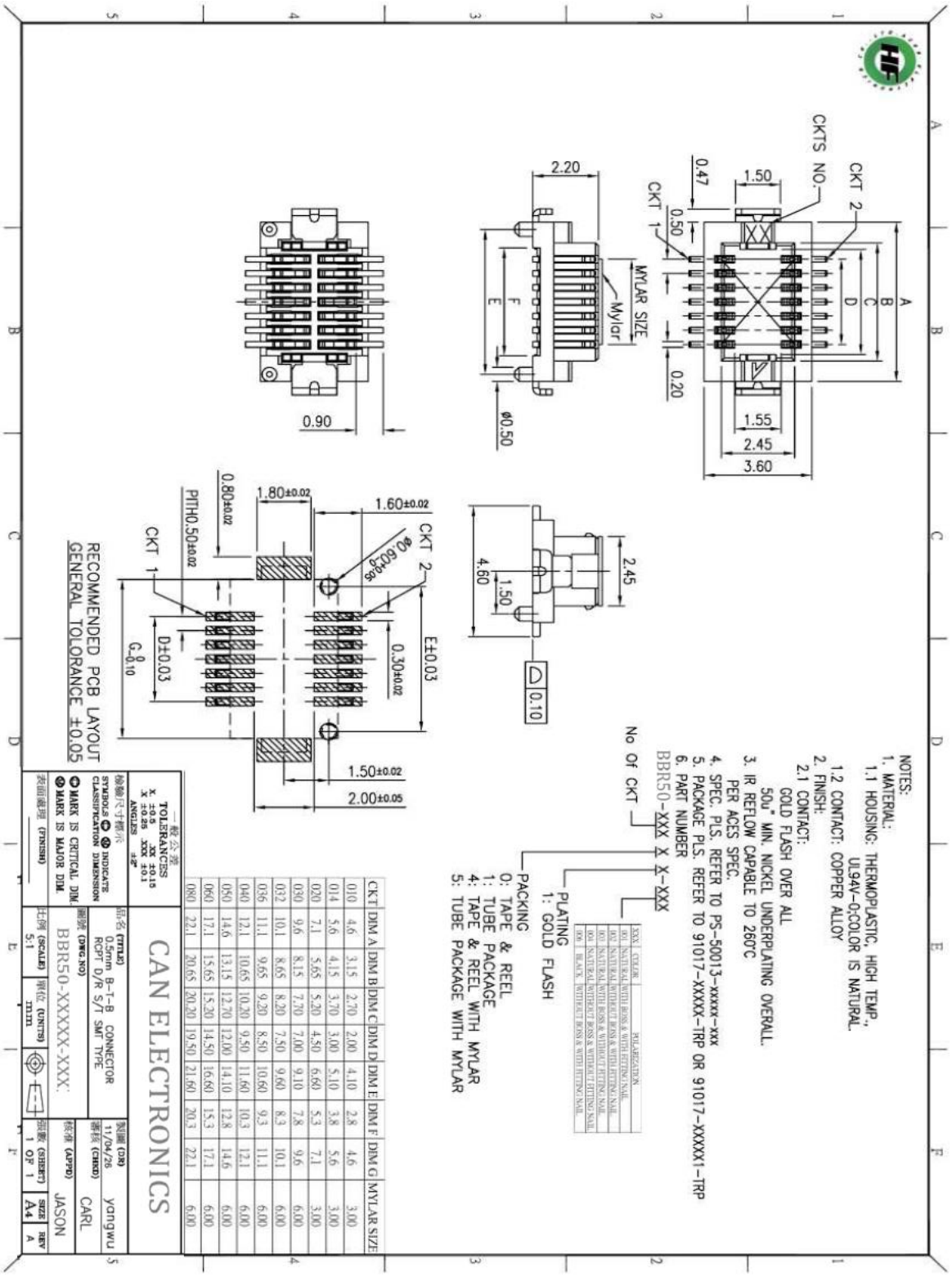


Fig 13. Physical z=0 plane

13. Connector Drawings

13.1. S110D B to B connector drawing (BBR50-04001-001)



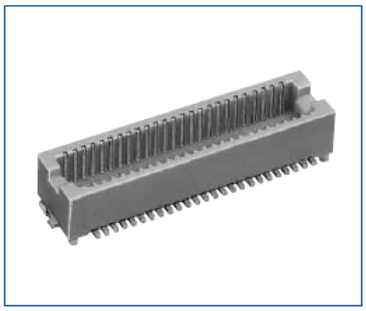
CKT	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	MYLAR SIZE
010	4.6	3.15	2.70	2.00	4.10	2.8	4.6	3.00
014	5.6	4.15	3.70	3.00	5.10	3.8	5.6	3.00
020	7.1	5.65	5.20	4.50	6.60	5.3	7.1	3.00
030	9.6	8.15	7.70	7.00	9.10	7.8	9.6	6.00
032	10.1	8.65	8.20	7.50	9.60	8.3	10.1	6.00
036	11.1	9.65	9.20	8.50	10.60	9.3	11.1	6.00
040	12.1	10.65	10.20	9.50	11.60	10.3	12.1	6.00
050	14.6	13.15	12.70	12.00	14.10	12.8	14.6	6.00
060	17.1	15.65	15.20	14.50	16.60	15.3	17.1	6.00
080	22.1	20.65	20.20	19.50	21.60	20.3	22.1	6.00

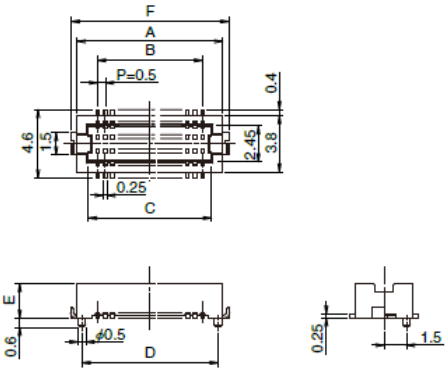
Fig 14. S110D connector

13. Connector Drawings

13.2. Host board connector drawing (DF12(5.0)-40DP-0.5V(86))

■Header With metal fitting





●Stacking Height : 3.5 to 5mm Product

Unit : mm

Part No.	HRS No.	No. of Contacts	A	B	C	D	E	F	Remarks	RoHS
DF12 (3.5)-20DP-0.5V (86)	537-0028-7 86	20	7.2	4.5	5.7	6.6	2.8	8.1	With metal fitting With boss	YES
DF12 (3.5)-30DP-0.5V (86)	537-0030-9 86	30	9.7	7.0	8.2	9.1		10.6		
DF12 (3.5)-36DP-0.5V (86)	537-0031-1 86	36	11.2	8.5	9.7	10.6		12.1		
DF12 (3.5)-40DP-0.5V (86)	537-0032-4 86	40	12.2	9.5	10.7	11.6		13.1		
DF12 (3.5)-50DP-0.5V (86)	537-0034-0 86	50	14.7	12.0	13.2	14.1		15.6		
DF12 (3.5)-60DP-0.5V (86)	537-0036-5 86	60	17.2	14.5	15.7	16.6		18.1		
DF12 (4.0)-20DP-0.5V (86)	537-0053-4 86	20	7.2	4.5	5.7	6.6	3.3	8.1		
DF12 (4.0)-30DP-0.5V (86)	537-0055-0 86	30	9.7	7.0	8.2	9.1		10.6		
DF12 (4.0)-32DP-0.5V (86)	537-0926-2 86	32	10.2	7.5	8.7	9.6		11.1		
DF12 (4.0)-36DP-0.5V (86)	537-0056-2 86	36	11.2	8.5	9.7	10.6		12.1		
DF12 (4.0)-40DP-0.5V (86)	537-0057-5 86	40	12.2	9.5	10.7	11.6		13.1		
DF12 (4.0)-50DP-0.5V (86)	537-0059-0 86	50	14.7	12.0	13.2	14.1		15.6		
DF12 (4.0)-60DP-0.5V (86)	537-0061-2 86	60	17.2	14.5	15.7	16.6		18.1		
DF12 (5.0)-20DP-0.5V (86)	537-0153-9 86	20	7.2	4.5	5.7	6.6	4.3	8.1		
DF12 (5.0)-30DP-0.5V (86)	537-0155-4 86	30	9.7	7.0	8.2	9.1		10.6		
DF12 (5.0)-36DP-0.5V (86)	537-0156-7 86	36	11.2	8.5	9.7	10.6		12.1		
DF12 (5.0)-40DP-0.5V (86)	537-0157-0 86	40	12.2	9.5	10.7	11.6		13.1		
DF12 (5.0)-50DP-0.5V (86)	537-0159-5 86	50	14.7	12.0	13.2	14.1		15.6		
DF12 (5.0)-60DP-0.5V (86)	537-0161-7 86	60	17.2	14.5	15.7	16.6		18.1		
DF12B (3.5)-20DP-0.5V (86)	537-0328-0 86	20	7.2	4.5	5.7	—	2.8	8.1	With metal fitting Without boss	
DF12B (3.5)-30DP-0.5V (86)	537-0330-2 86	30	9.7	7.0	8.2			10.6		
DF12B (3.5)-36DP-0.5V (86)	537-0331-5 86	36	11.2	8.5	9.7			12.1		
DF12B (3.5)-40DP-0.5V (86)	537-0332-8 86	40	12.2	9.5	10.7			13.1		
DF12B (3.5)-50DP-0.5V (86)	537-0334-3 86	50	14.7	12.0	13.2			15.6		
DF12B (3.5)-60DP-0.5V (86)	537-0336-9 86	60	17.2	14.5	15.7			18.1		
DF12B (4.0)-20DP-0.5V (86)	537-0353-8 86	20	7.2	4.5	5.7	—	3.3	8.1		
DF12B (4.0)-30DP-0.5V (86)	537-0355-3 86	30	9.7	7.0	8.2			10.6		
DF12B (4.0)-32DP-0.5V (86)	537-0927-5 86	32	10.2	7.5	8.7			11.1		
DF12B (4.0)-36DP-0.5V (86)	537-0356-6 86	36	11.2	8.5	9.7			12.1		
DF12B (4.0)-40DP-0.5V (86)	537-0357-9 86	40	12.2	9.5	10.7			13.1		
DF12B (4.0)-50DP-0.5V (86)	537-0359-4 86	50	14.7	12.0	13.2			15.6		
DF12B (4.0)-60DP-0.5V (86)	537-0361-6 86	60	17.2	14.5	15.7			18.1		
DF12B (5.0)-20DP-0.5V (86)	537-0378-9 86	20	7.2	4.5	5.7	—	4.3	8.1		
DF12B (5.0)-30DP-0.5V (86)	537-0380-0 86	30	9.7	7.0	8.2			10.6		
DF12B (5.0)-36DP-0.5V (86)	537-0381-3 86	36	11.2	8.5	9.7			12.1		
DF12B (5.0)-40DP-0.5V (86)	537-0382-6 86	40	12.2	9.5	10.7			13.1		
DF12B (5.0)-50DP-0.5V (86)	537-0384-1 86	50	14.7	12.0	13.2			15.6		
DF12B (5.0)-60DP-0.5V (86)	537-0386-7 86	60	17.2	14.5	15.7			18.1		

Note : Please order the embossed tape packaging product per reel. (1000 pcs./reel)

Fig 15. Host board Connector

14. Certification

14.1. Eye safety

Standard	Result
IEC 60825-1:2014 (Third Edition)	Class 1

Table 22. Eyesafety standard information

Appendix A : Data Format

A.1. Data format - Raw 10 bits (16 bits unsigned int)

The S110D has 3 output modes as shown in the table below.(Default : mode 0)
Each (Z/R) and (Amplitude/Intensity) is selectable and the default is Z, Amplitude.

mode	Resolution	Position(Z/R selectable)			IR(selectable)
		X	Y	Z / R	Amplitude / Intensity
mode 0	2560 x 961	O	O	O	O
mode 1	1280 x 961	-	-	O	O
mode 2	640 x 961	-	-	O	-

Table 23. Data mode

A.1.1. 1 pixel format

Each mode has a different pixel size. Attention is required in these situations.

mode 0 (64bits): 1pixel (16bits X, 16bits Y, 16bits Z, 16bits A)
mode 1 (32bits): 1pixel (16bits R, 16bits A)
mode 2 (16bits): 1pixel (16bits R)

A.1.2. 16 bits Data format

Complexly, it imports two 10-bit raw MIPI data to convert one 16-bit.
The 16-bit data generated becomes a component of the pixel.

2 MIPI Raw 10 bits to 16 bits data

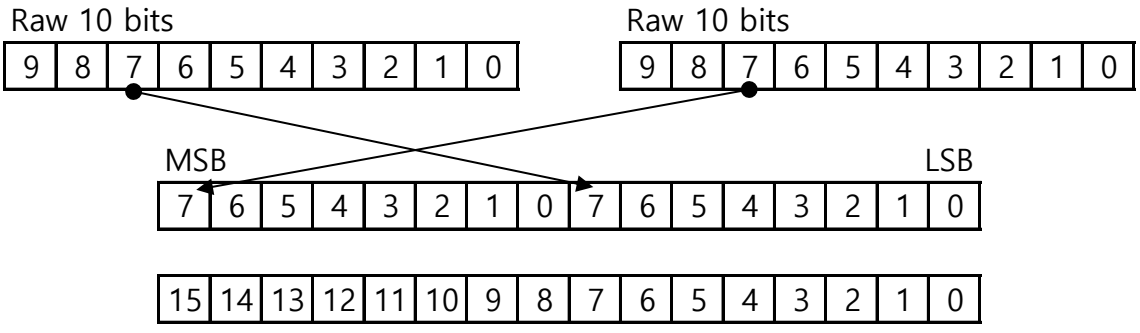


Fig 16. Data reconstruction

Appendix A : Data Format

A.2. Mode example

Expression rule

X - * _ #_$

X : data information

* : pixel x index

: pixel y index

$: L(LSB) H(MSB)

Em - #

Em : embedded data

: data index

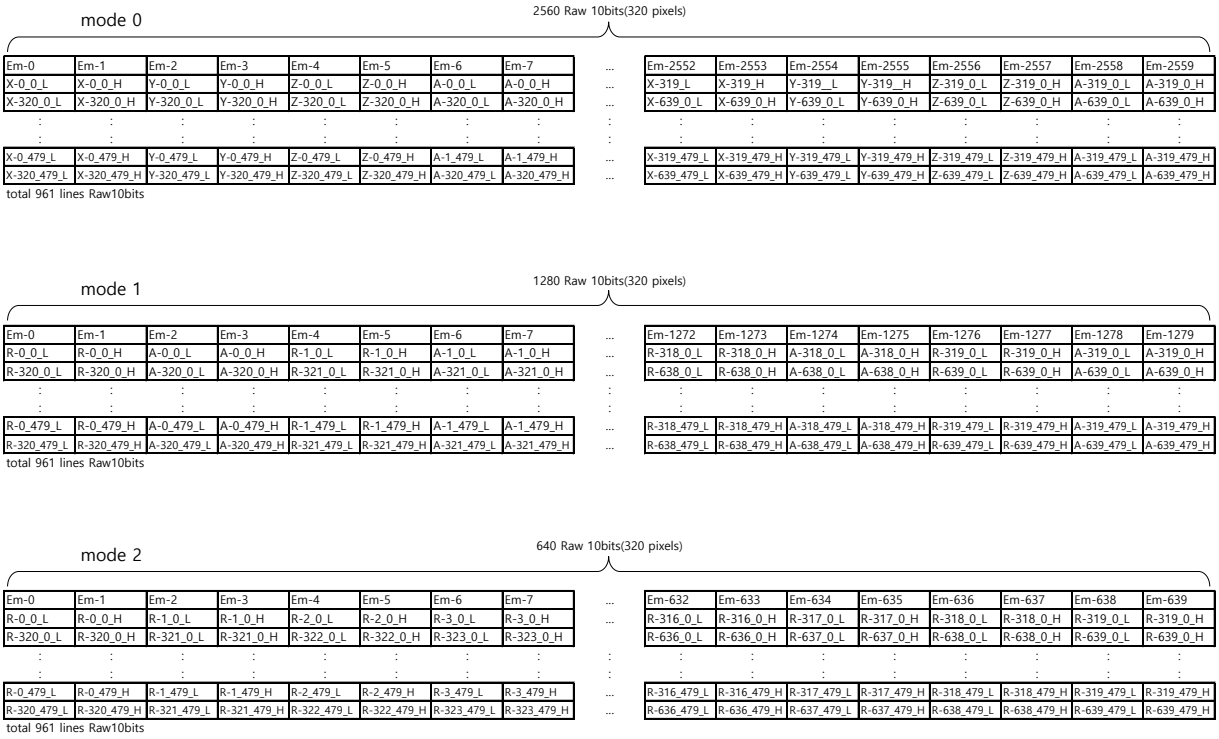


Fig 17. Output mode examples

Appendix A : Data Format

A.3. Embedded line data description

Data index	Bus_width	Name	Description
Em-0	8	rev_no[7:0]	MR1000 Revision number
Em-6	8	frame_count[7:0]	frame_count[7:0]
Em-7	8	frame_count[15:8]	frame_count[15:8]
Em-8	1	filter3_on[7]	filter3_on/off
	1	remove_flying_pixel_on[6]	remove_flying_pixel_on/off
	1	flter2_on[5]	flter2_on/off
	1	filter1_on[4]	filter1_on/off
Em-12	8	set_firm_rev_no[7:0]	firmware Revision number
Em-17	8	tof_temp[7:0]	ToF temperature = tof_temp[15:0] * 256
Em-18	8	tof_temp[15:8]	
Em-19	8	drv_temp[7:0]	drive IC temperature = drv_temp[15:0] * 256
Em-20	8	drv_temp[15:8]	
Em-21	8	amp_max_limit[7:0]	amp_max_limit
Em-22	8	amp_max_limit[15:8]	
Em-23	8	amp_min_limit[7:0]	amp_min_limit
Em-24	8	amp_min_limit[15:8]	
Em-25	8	depth_max_limit[7:0]	depth_max_limit
Em-26	8	depth_max_limit[15:8]	
Em-27	8	depth_min_limit[7:0]	depth_min_limit
Em-28	8	depth_min_limit[15:8]	
Em-29	8	mci_thresh[7:0]	mci_thresh
Em-30	8	mci_thresh[15:8]	
Em-35	4	mci_flag[3:0]	mci_flag
Em-38	8	scat_threshold[7:0]	scat_threshold
Em-39	8	scat_threshold[15:8]	
Em-40	8	flying pixel_threshold[7:0]	remove_flying_pixel_thresh
Em-41	8	flying pixel_threshold[15:8]	
Em-42	8	temporal_mblur[7:0]	temporal_mblur
Em-43	8	multi_freq_ctrl[7:0]	multi_freq_ctrl
Em-68	4	data_format_sel[3:0]	data_format_sel[3:0]
Em-73	8	g_offset[7:0]	global_offset
Em-74	8	g_offset[15:8]	

Table 24. Embedded line data description

Appendix B : USB3.0 bridge board(U300)

B.1. Block Diagram

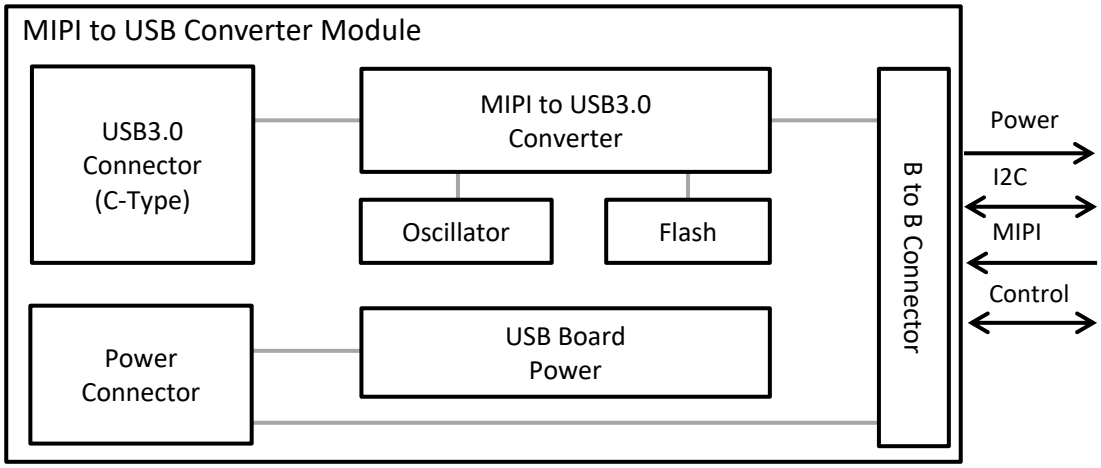
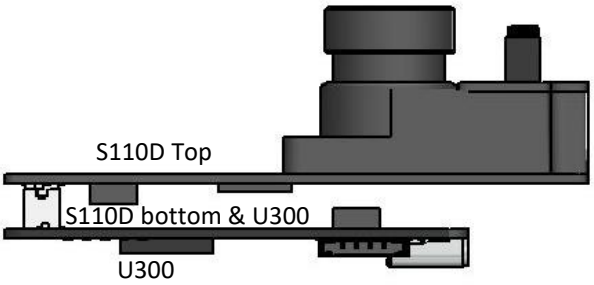


Fig 18. U300 block diagram

B.2. S110D on U300



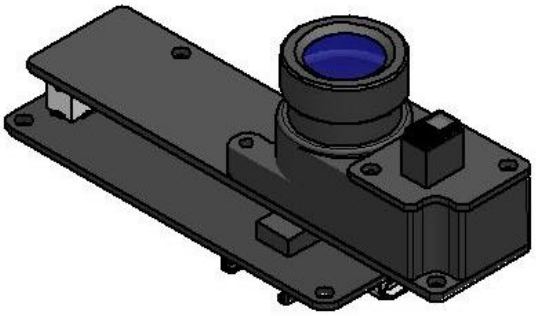


Fig 19. Combined S110D and U300

Appendix B : USB3.0 bridge board(U300)

B.3. U300 schematic

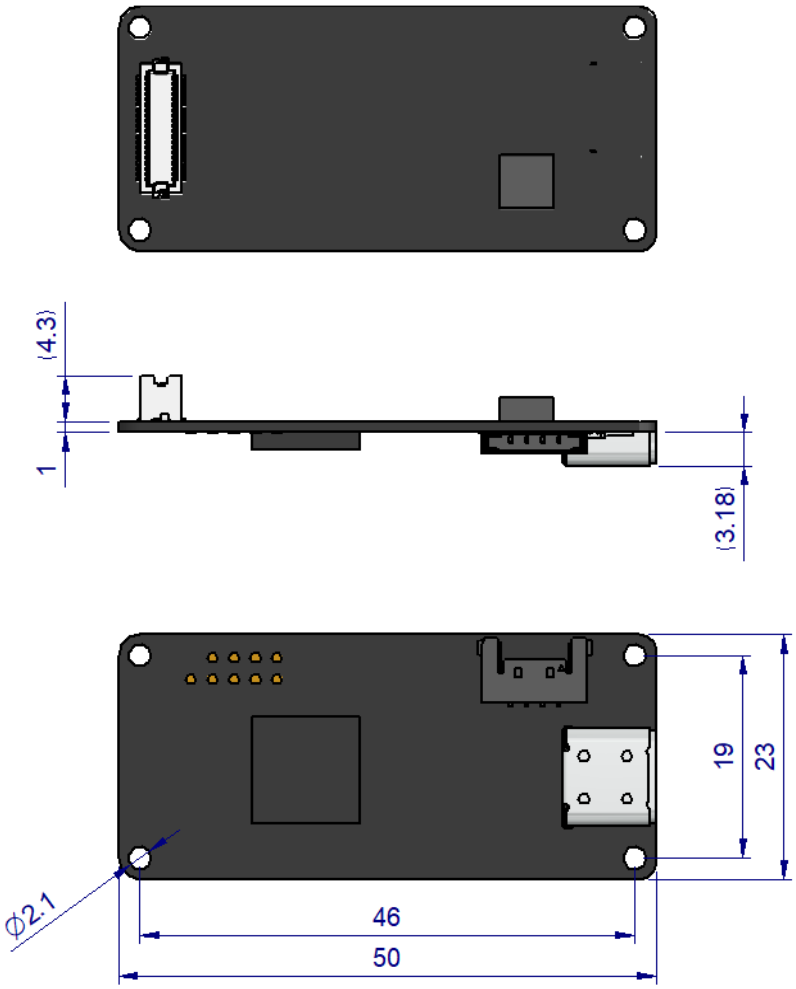


Fig 20. U300 dimension

Appendix B : USB3.0 bridge board(U300)

B.4. U300 connector pin map(BBP50-04001-001)

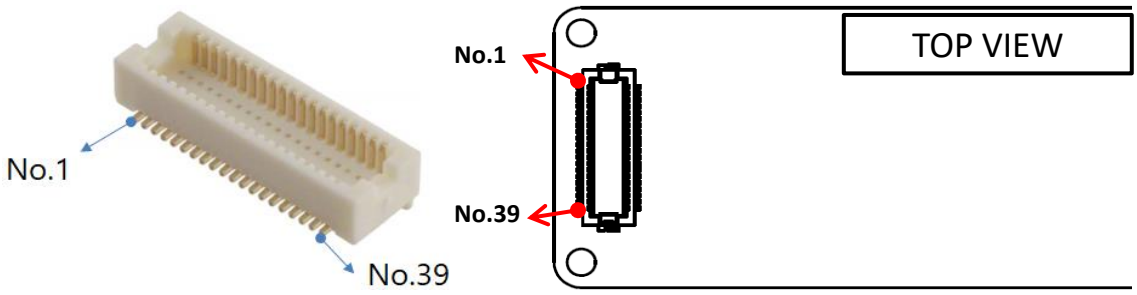


Fig 21. U300 B to B connector

Name	No.		Name
N.C	1	2	GND
I2C_SCL	3	4	MIPI_DATA1_N
I2C_SDA	5	6	MIPI_DATA1_P
GPIO2	7	8	GND
GPIO1	9	10	MIPI_CLK_N
GPIO0	11	12	MIPI_CLK_P
N.C	13	14	GND
RESET	15	16	MIPI_DATA0_N
Boot done	17	18	MIPI_DATA0_P
GND	19	20	GND
LVDS_RX_N	21	22	LVDS_TX_N
LVDS_RX_P	23	24	LVDS_TX_P
GND	25	26	GND
GND	27	28	+5V
GND	29	30	+5V
GND	31	32	+5V
GND	33	34	+5V
GND	35	36	+5V
GND	37	38	+5V
GND	39	40	+5V

Table 25. U300 B to B connector pin map

Appendix B : USB3.0 bridge board(U300)

B.5. U300 connector pin Information

Name	Description	Electrical Characteristics
+5V	ToF Module Power Input	5V/3A
MIPI_DATA0_N	MIPI data lane 0(negative)	MIPI
MIPI_DATA0_P	MIPI data lane 0(positive)	MIPI
MIPI_CLK_N	MIPI clock lane(negative)	MIPI
MIPI_CLK_P	MIPI clock lane(positive)	MIPI
MIPI_DATA1_N	MIPI data lane 1(negative)	MIPI
MIPI_DATA1_P	MIPI data lane 1(positive)	MIPI
LVDS_RX_P	Differential modulation clock input(positive)	LVDS
LVDS_RX_N	Differential modulation clock input(negative)	LVDS
LVDS_TX_P	Differential modulation clock output(negative)	LVDS
LVDS_TX_N	Differential modulation clock output(positive)	LVDS
Boot done	Booting Done : Active High	1.8V
RESET	Reset : Active Low	1.8V
GPIO	General Purpose I/O	1.8V
I2C_SDA	I2C Serial Data(Slave)	1.8V
I2C_SCL	I2C Serial Clock(Slave)	1.8V

Table 26. U300 pin information

Appendix B : USB3.0 bridge board(U300)

B.6. Accessories

- Adaptor
- Power Cable
- USB3.0 Cable(A to C-type)

Fig 22. U300 accessories

B.7. Cable connection

- Power Cable/USB Cable connection

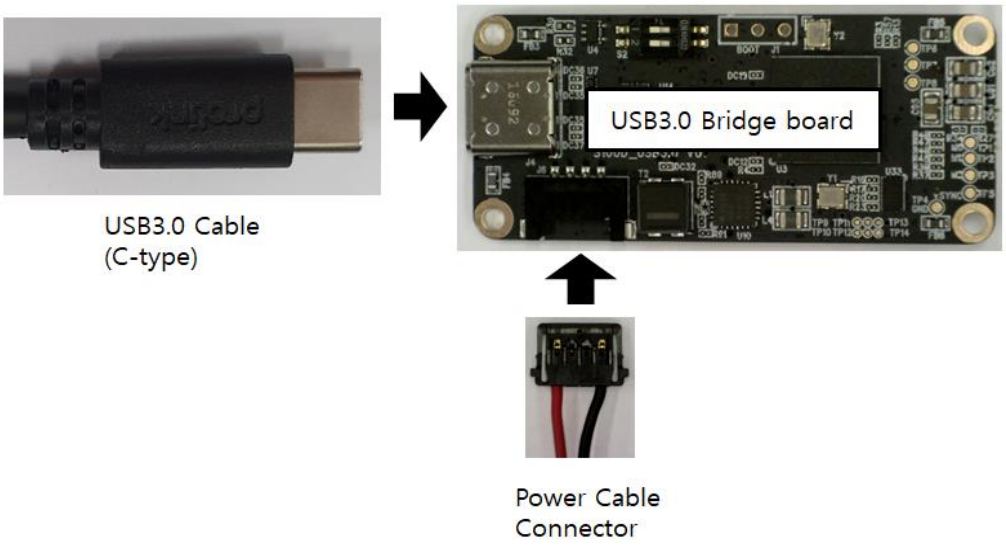


Fig 23. Cable connection

Appendix C : Part Number

Configuration of part number

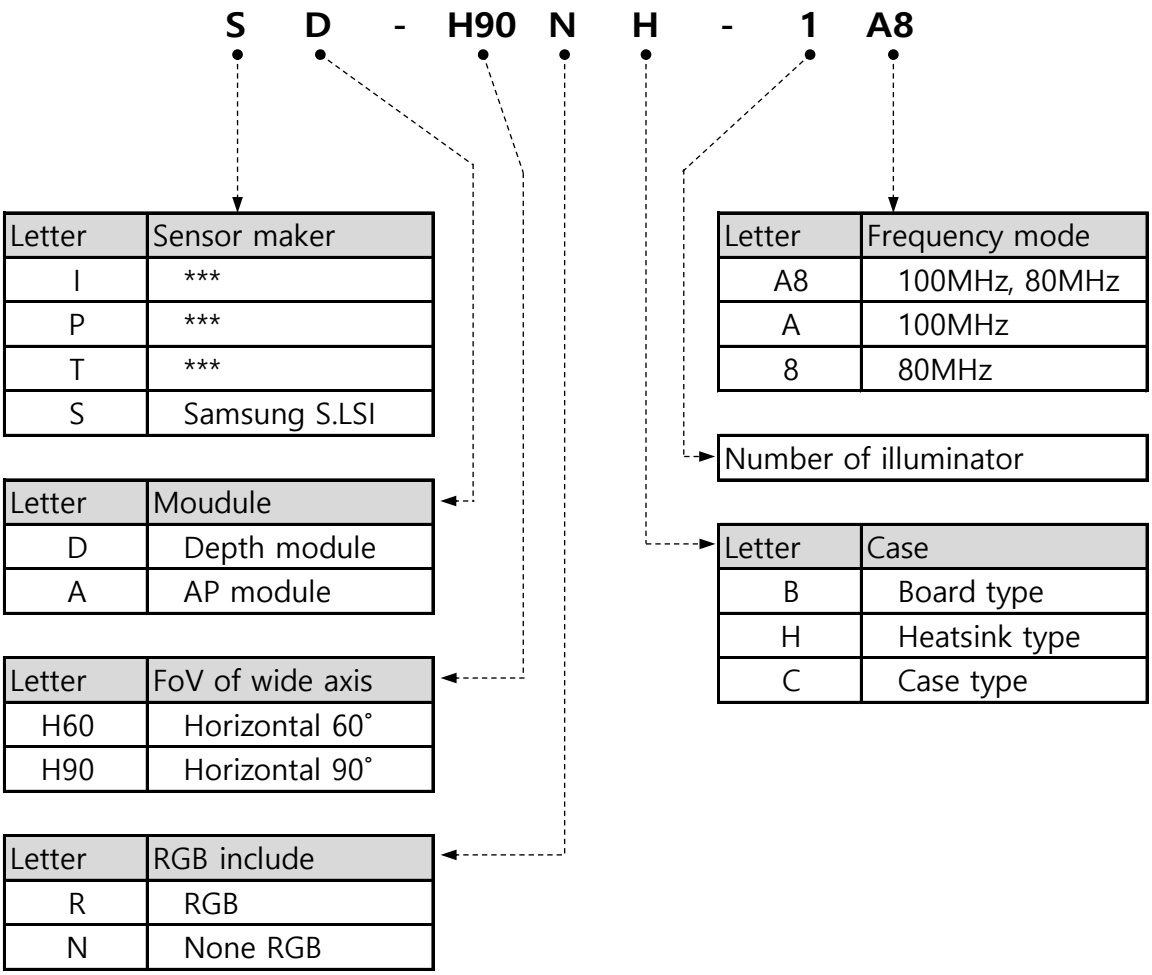


Fig 24. Decription of the part number configuration

Appendix D : Cover Glass Assy' Guide

When using the cover glass, it is recommended to place it as close to the lens as possible. And it is necessary to place a light barrier between RX and TX to minimize light spread.

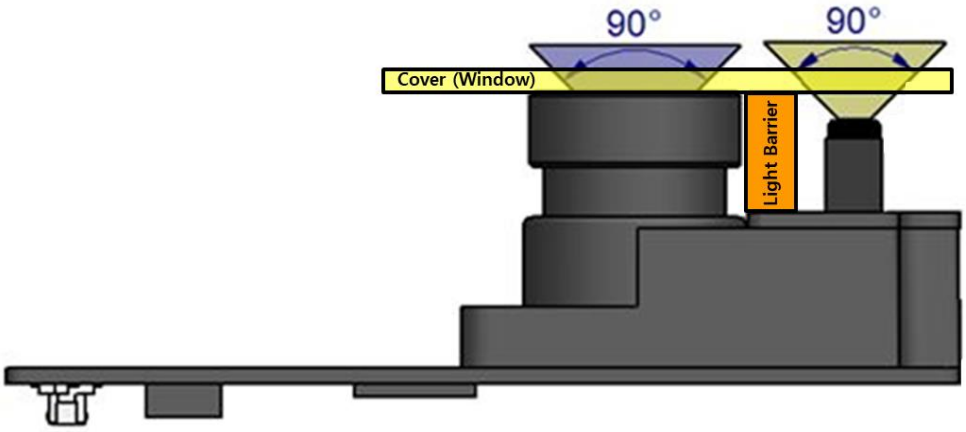


Fig 25. Example image of use of cover glass (type1)

If the cover glass is pierced by the Lens, a light barrier is not necessary

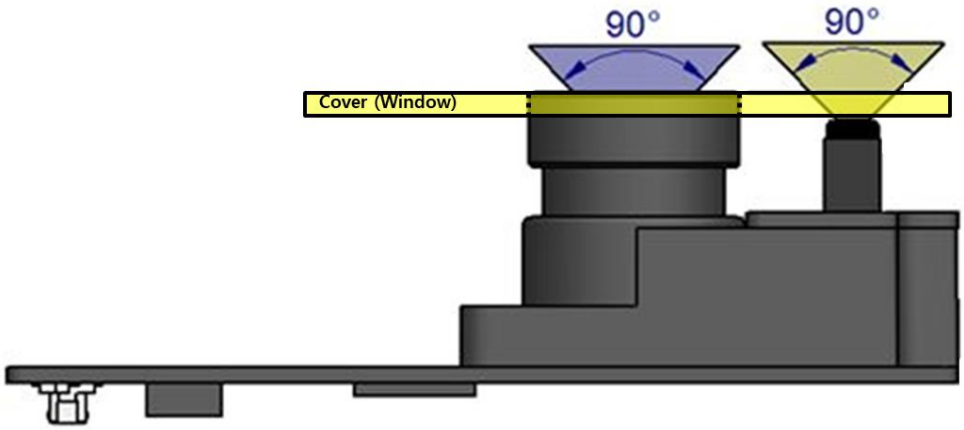


Fig 26. Example image of use of cover glass (type2)