

LI-OV13850-MIPI-AF SPECIFICATION

**Rev 1.1
Leopard Imaging Inc.**

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Version History

Version	Description	Release Date
1.0	First Release	3. Jan. 2015
1.1	Update OV13850 module to V1.1	10. Feb. 2016



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Key Information

Module Part#		LI-OV13850-MIPI-AF
Module Size		27.75 mm (L) x 8.50 mm (W) x 5.70 mm(H)
Sensor Type		OV13850
Array Size		4224 x 3136
Power Supply	core	1.14 ~ 1.26V (1.2V nominal)
	analog	2.6 ~ 3.0V (2.8V nominal)
	I/O	1.7 ~ 3.0 V (1.8V or 2.8V nominal)
Lens Size		1/3.06"
Focus(F.NO)		2.2
FOV (D)		70°
Focal Length		3.81 mm
Focusing Range		10cm to infinity
TV Distortion		< 1.5 %
Sensitivity		TBD
Pixel size		1.12 um x 1.12 um
IR Cutter		650 nm
Sensor Temperature Range	Operating	-30 ℃ to +85 ℃
	Stable Image	0 ℃ to +60 ℃
Output Formats		10-bit RAW RGB data
Support for image sizes		13.2MP(4224 x 3136); 10M(16:9 – 4224 x 2376); 4K2K(3840 x 2160); EIS 1080P(2112 x 1188); EIS 720P(1408 x 792); and more
Dynamic Range		TBD
Max S/N ratio		TBD
Power Requirement	Active	199 mW (13MP @ 30 fps, ISP OFF)
	Standby	300uW
	XSHUTDOWN	1 uW
Image area		4815 um x 3678.3 um
Dark Current		TBD
Die Dimensions		6210um x 5517um (COB), 6260 um x 5567um (RW)



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Pin Assignment

No.	Name	Pin type	Description
1	SDA	I/O	SCCB data
2	SCL	Input	SCCB input clock
3	DOVDD1.8V/2.8V	Power	Power for I/O circuit
4	MCP	Output	MIPI clock positive output
5	MCN	Output	MIPI clock negative output
6	GND	Ground	
7	MDP1	Output	MIPI data positive output
8	MDN1	Output	MIPI data negative output
9	GND	Ground	
10	MDP2	Output	MIPI data positive output
11	MDN2	Output	MIPI data negative output
12	GND	Ground	
13	MDP3	Output	MIPI data positive output
14	MDN3	Output	MIPI data negative output
15	GND	Ground	
16	MDP4	Output	MIPI data positive output
17	MDN4	Output	MIPI data negative output
18	DVDD1.2V	Power	Power for digital core
19	XCLK	Input	System input clock
20	PWDN	Input	Power down (active high with internal pull-down resistor)
21	RESET	Input	Reset (active low with internal pull-up resistor)
22	AVDD2.8	Power	Analog power
23	AF-VCC2.8V	Power	Power for analog circuit
24	AF-AGND	Ground	Ground for analog circuit



Electrical Characteristics

1. Absolute Maximum Ratings

parameter		absolute maximum rating ^a
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V _{DD-A}	4.5V
	V _{DD-D}	3V
	V _{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V _{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2. Functional temperature

parameter	range
operating temperature ^a	-30°C to +85°C junction temperature
stable image temperature ^b	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range



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3. DC Characteristics (-30 °C < T_J < 85 °C)

symbol	parameter	min	typ	max	unit
supply					
V _{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V _{DD-D}	supply voltage (digital core)	1.14	1.2	1.26	V
V _{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
I _{DD-A}	active (operating) current for 13Mpixel @ 30fps ^a		39	45	mA
I _{DD-D}			90	120	mA
I _{DD-IO}			1	10	mA
I _{DDS-SCCB}	standby current ^b		TBD		μA
I _{DDS-PWDN}			TBD		μA
I _{DDS-XSHUTDOWN}			TBD		μA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V, EVDD = 1.2V)					
V _{IL}	input voltage LOW			0.54	V
V _{IH}	input voltage HIGH	1.26			V
C _{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V _{OH}	output voltage HIGH	1.62			V
V _{OL}	output voltage LOW			0.18	V
serial interface inputs					
V _{IL} ^c	SIOC and SIOD	-0.5	0	0.54	V
V _{IH}	SIOC and SIOD	1.28	1.8	3.0	V

- a. active current is measured with ISP OFF
b. standby current is measured at room temperature
c. based on DOVDD = 1.8V

4. AC Characteristics

symbol	parameter	min	typ	max	unit
inputs					
f _{CLK}	input clock frequency	6	24	64	MHz
t _{CLK}	input clock period		41.67		ns
t _{CLK:DC}	clock duty cycle	45	50	55	%



5. Timing Characteristics

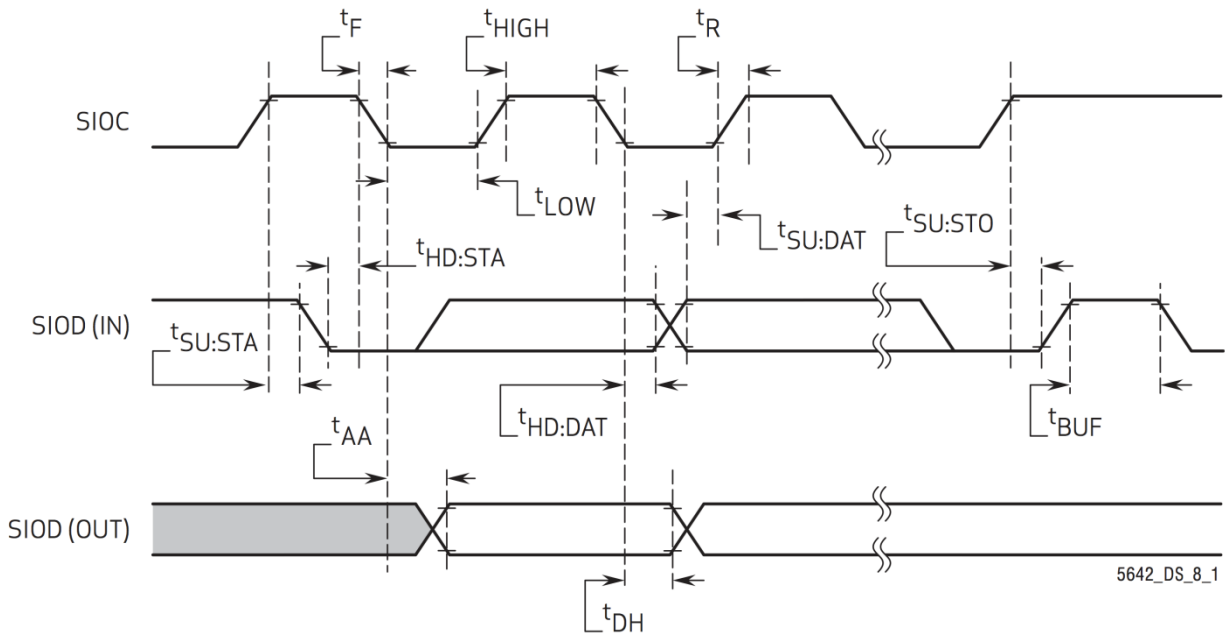
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{osc}	frequency (EXTCLK) ^a	6	24	64	MHz
t_r, t_f	clock input rise/fall time			(see footnote ^b)	ns
	clock input duty cycle	45	50	55	%

a. for input clock range 6~64MHz, the OV13850 can tolerate input clock period jitter up to 600ps peak-to-peak

b. for clock input rise/fall time, max is 27% of whole clock period

6. SCCB timing

a. SCCB interface timing



5642_DS_8_1

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b. SCCB interface timing Specification^{ab}

symbol	parameter	conditions	min	typ	max	unit
f _{SIOC}	SIOC clock frequency			400	400	kHz
t _{HIGH}	SIOC clock high period	V _{PADVDD} =1.8V	0.6			μs
t _{LOW}	SIOC clock low period	V _{PADVDD} =1.8V	1.3			μs
t _{BUF}	bus free time before new start cycle	V _{PADVDD} =1.8V	1.3			μs
t _{HD:STA}	start of transmission hold time	V _{PADVDD} =1.8V	0.6			μs
t _{SU:STA}	start of transmission setup time	V _{PADVDD} =1.8V	0.6			μs
t _{SU:STO}	stop of transmission setup time	V _{PADVDD} =1.8V	0.6			μs
t _{SU:DAT}	input data in setup time	V _{PADVDD} =1.8V	100			ns
t _{HD:DAT}	input data in hold time	V _{PADVDD} =1.8V	0			μs
t _{VD:DAT}	time for data signal from SIOC low to SIOD output	V _{PADVDD} =1.8V			0.9	μs
t _{VD:ACK}	time for ACK signal from SIOC low to SIOD output	V _{PADVDD} =1.8V			0.9	μs
t _{r SIOD}	SIOD clock rising time	V _{PADVDD} =1.8V, 30~70%	20		300	ns
t _{f SIOD}	SIOD clock falling time	V _{PADVDD} =1.8V, 30~70%	20×(VDD / 5.5V) = 6.55		300	ns

7. Format and frame rate

format	resolution	max frame rate	methodology	10-bit output MIPI data rate
13.2 megapixel	4224 x 3136	30 fps	full resolution	4-lane @ 1200 Mbps/lane
2112x1568	2112x1568	60 fps	2x2 binning	4-lane @ 640 Mbps/lane
EIS 1080p	2112x1188	60 fps	cropping + 2x2 binning	4-lane @ 640 Mbps/lane
EIS 720p	1408x792	60 fps	cropping + 2x2 binning	4-lane @ 640 Mbps/lane
720p	1280x720	120 fps	cropping + 2x2 binning	4-lane @ 640 Mbps/lane
10 megapixel (16:9)	4224x2376	30 fps	cropping	4-lane @ 1200 Mbps/lane



8. Power Up Sequence

case	XSHUTDOWN	PWDNB	power up sequence requirement
1	GPIO	DOVDD	Refer to figure 2-4 1. DOVDD rising must occur before DVDD rising 2. AVDD rising can occur before or after DOVDD rising 3. XSHUTDOWN rising must occur after AVDD, DOVDD and DVDD are stable
2	DOVDD	GPIO	Refer to figure 2-5 1. AVDD rising occurs before DOVDD rising 2. DOVDD rising occurs before DVDD 3. PWDNB rising occurs after DVDD rising

a. Power Up Sequence (case 1)

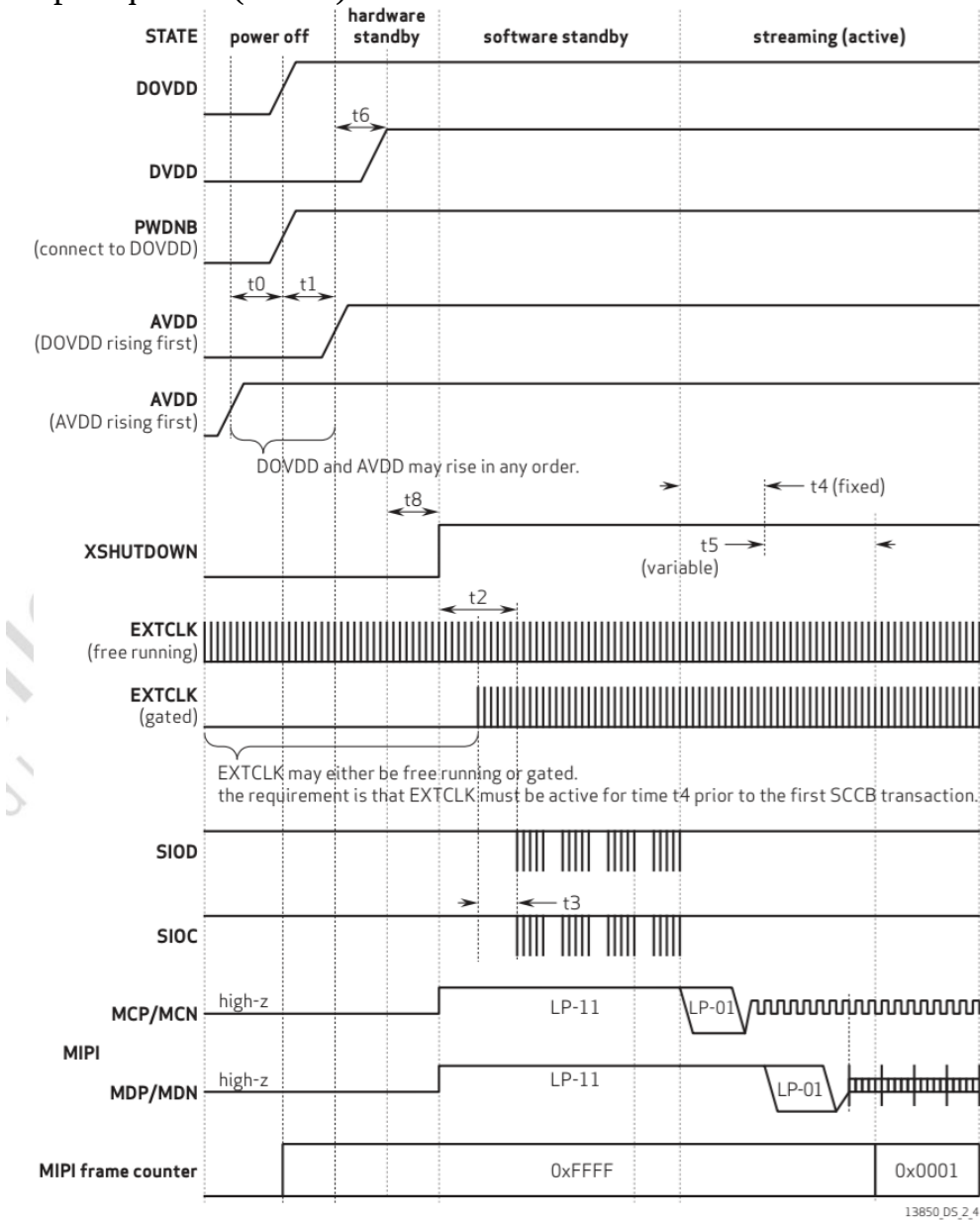


Figure 2-4

b. Power Up Sequence (case 2)

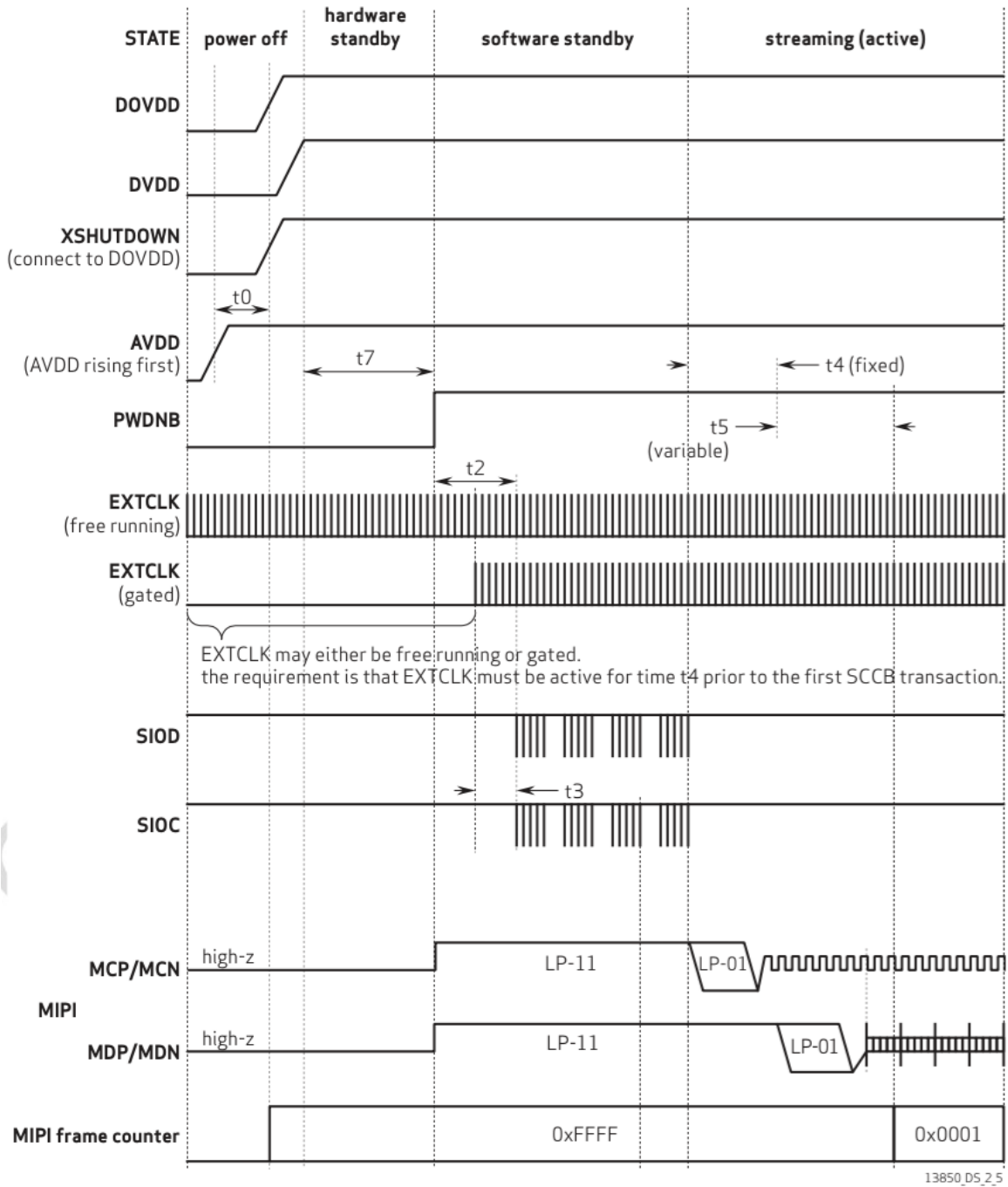


Figure 2-5



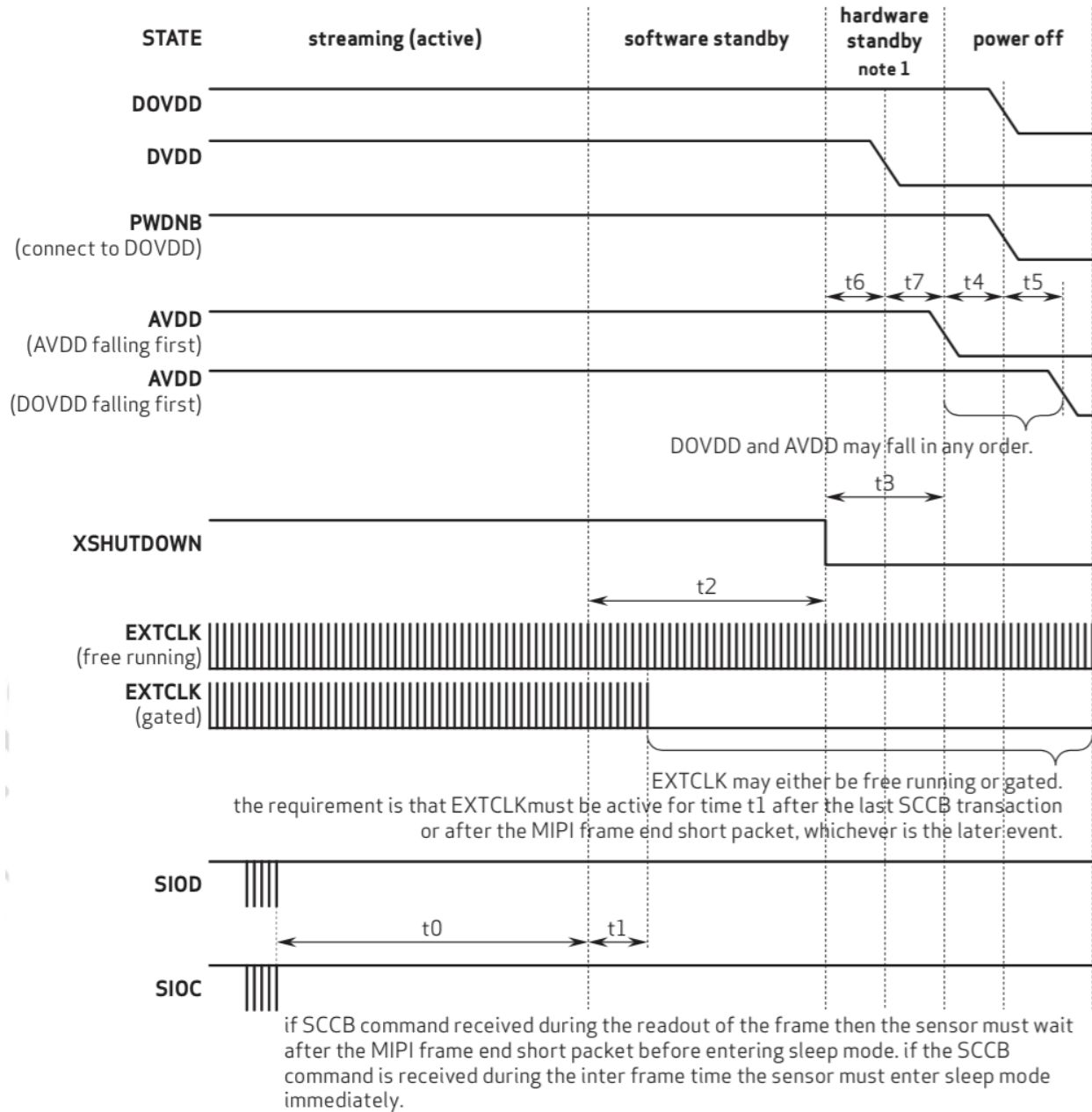
c. Power Up Sequence Timing Constraints

constraint	label	min	max	unit
AVDD rising – DOVDD rising	t0	0	∞	ns
DOVDD rising – AVDD rising	t1			ns
XSHUTDOWN rising – first CCI transaction	t2	8192		EXTCLK cycles
minimum number of EXTCLK cycles prior to the first CCI transaction	t3	8192		EXTCLK cycles
entering streaming mode – first frame start sequence (fixed part)	t4		10	ms
entering streaming mode – first frame start sequence (variable part)	t5	delay is the exposure time value		lines
AVDD or DOVDD, whichever is last – DVDD	t6	0.0	∞	ns
DVDD - PWDNB rising	t7	10	∞	ms
DVDD - XSHUTDOWN rising	t8	10	∞	ms

9. Power Down Sequence

case	XSHUTDOWN	PWDNB	power down sequence requirement
1	GPIO	DOVDD	Refer to figure 2-6 1. software standby recommended 2. pull XSHUTDOWN low for low power consumption 3. cut off DVDD, then it will be in hardware standby state for minimum power consumption 4. pull AVDD and DOVDD low in any order
2	DOVDD	GPIO	Refer to figure 2-7 1. software standby recommended 2. pull PWDNB low for low power consumption 3. cut off DVDD, then it will be in hardware standby mode for minimum power consumption 4. turn off DOVDD 5. turn off AVDD

a. Power Down Sequence (case 1)



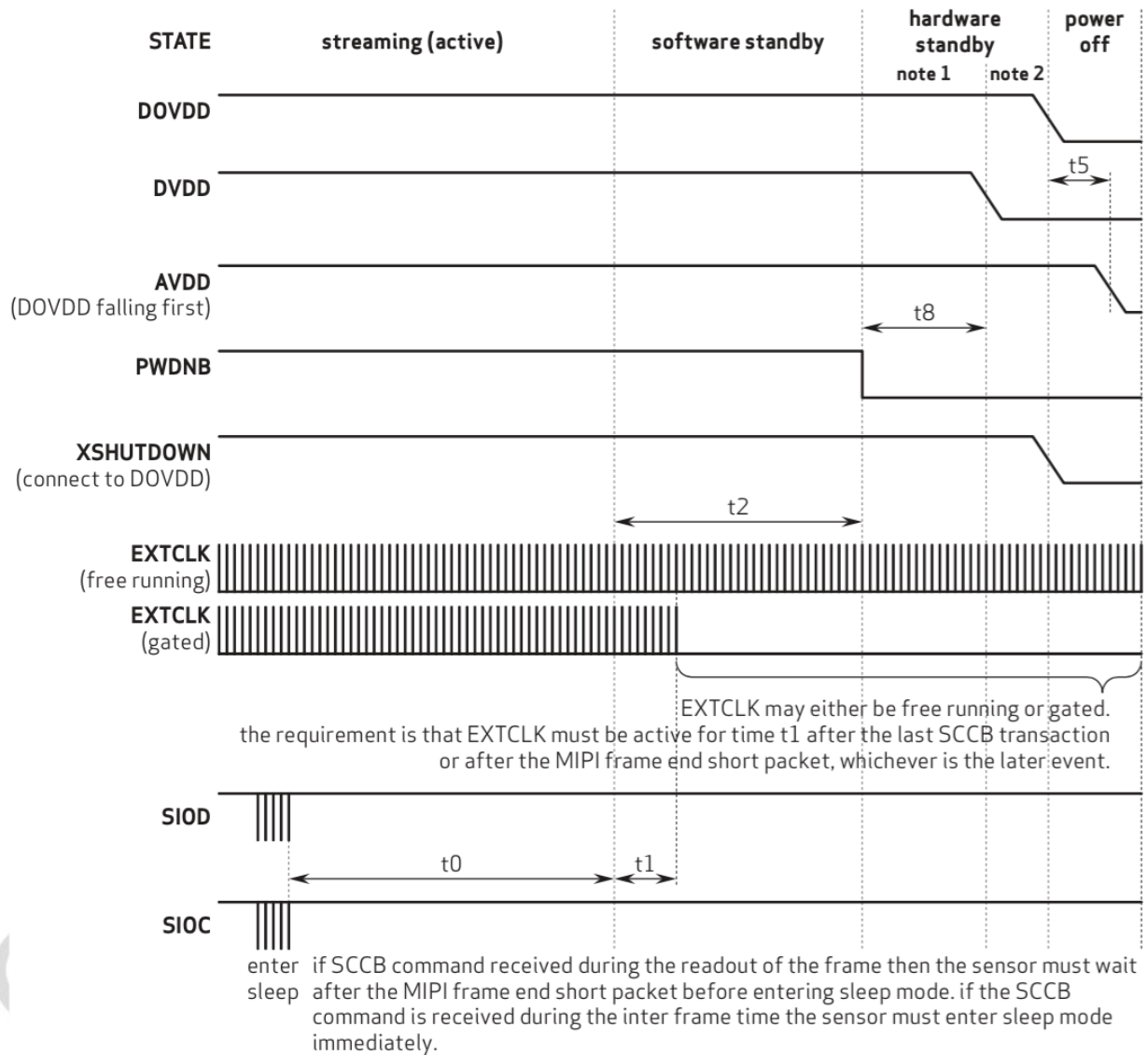
note 1 with minimum power consumption

13850_DS_2_6

Figure 2-6



b. Power Down Sequence (case 2)



note 1 with low power consumption

note 2 with minimum power consumption

13850_DS_2_7

Figure 2-7



c. Power Down Sequence Timing Constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of EXTCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		EXTCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		EXTCLK cycles
XSHUTDOWN falling – AVDD falling or DOVDD falling whichever is first	t3	0.0		ns
AVDD falling – DOVDD falling	t4	AVDD and DOVDD may fall in any order, the falling separation can vary from 0 ns to infinity		ns
DOVDD falling – AVDD falling	t5			ns
XSHUTDOWN falling – external DVDD falling	t6	0.0		ns
external DVDD falling – AVDD falling or DOVDD falling whichever is first	t7	0.0		ns
PWDNB falling – external DVDD falling	t8	0.0		ns

