XMC4400

Microcontroller Series
for Industrial Applications

XMC4000 Family

ARM® Cortex®-M4
32-bit processor core

Data Sheet

V1.3 2018-09

Microcontrollers

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Revision History: V1.3 2018-09

Previous Versions:
V1.2 2015-12
V1.1 2014-03
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Page	Subjects
46	Added RMS Noise parameter in VADC Parameters table.
12	Added a section listing the packages of the different markings.
14	Added BA marking variant.
37	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
38	Changed pull device definition to System Requirement (SR) to reflect that the specified currents are defined by the characteristics of the external load/driver.
38	Added information that $\overline{\text{PORST}}$ Pull-up is identical to the pull-up on standard I/O pins.
45	Updated C_{AINSW}, C_{AINTOT} and R_{AIN} parameters with improved values.
59	Added footnote on test configuration for LPAC measurement.
61	Corrected parameter name of of USB pull device (upstream port receiving) definition according to USB standard (referenced to DM instead of DP)
66	Relaxed RTC_XTAL V_{PPX} parameter value and changed it to a system requirement.
70	Added footnote on current consumption by enabling of f_{CCU}.
71	Added Flash endurance parameter for 64 Kbytes Physical Sector PS4 N_{EPS4} for devices with BA marking.
many	Added PG-TQFP-64-19 and PG-LQFP-100-25 package information.
97, **100**	Added tables describing the differences between PG-LQFP-100-11 to PG-LQFP-100-25 as well as PG-LQFP-64-19 to PG-TQFP-64-19 packages.
102	Updated to JEDEC standard J-STD-020D for the moisture sensitivity level and added solder temperature parameter according to the same standard.

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Table of Contents

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4500 series devices.

The document describes the characteristics of a superset of the XMC4500 series devices. For simplicity, the various device types are referred to by the collective term XMC4500 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

1 Summary of Features

The XMC4400 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

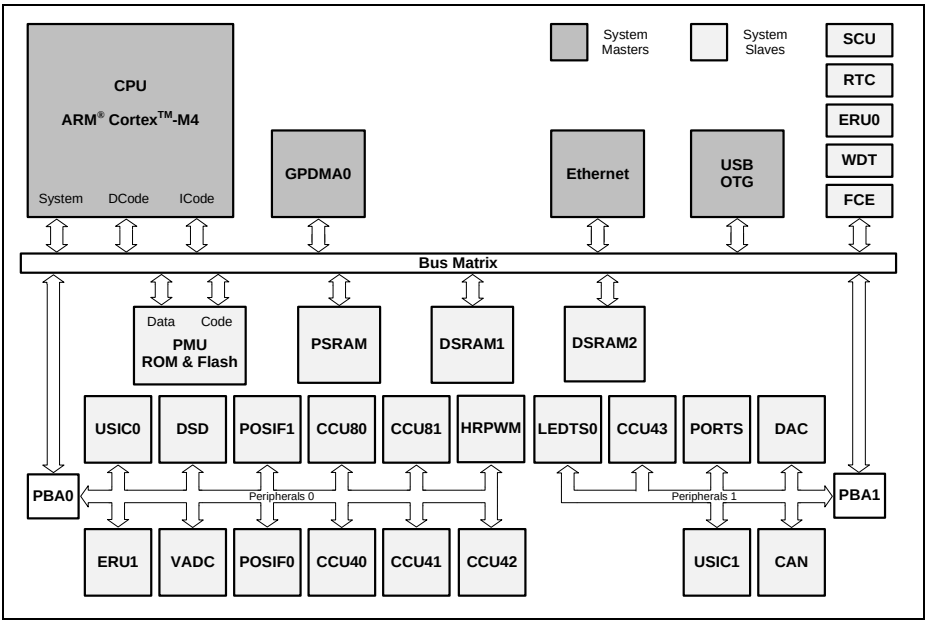

Figure 1 XMC4400 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- 16 KB on-chip high-speed program memory
- 32 KB on-chip high speed data memory
- 32 KB on-chip high-speed communication memory
- 512 KB on-chip Flash Memory with 4 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with two nodes, 64 message objects (MO), data rate up to 1MBit/s
- Four Universal Serial Interface Channels (USIC), providing four serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Four High Resoultion PWM (HRPWM) channels
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - E: LFBGA
  - F: LQFP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4400 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4400 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC4400** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC4400 **Device Types**

Derivative[1)]	**Package**	**Flash Kbytes**	**SRAM Kbytes**
XMC4400-F100x512	PG-LQFP-100	512	80
XMC4400-F64x512	PG-yQFP-64[2)]	512	80
XMC4400-F100x256	PG-LQFP-100	256	80
XMC4400-F64x256	PG-yQFP-64[2)]	256	80
XMC4402-F100x256	PG-LQFP-100	256	80
XMC4402-F64x256	PG-yQFP-64[2)]	256	80

1) x is a placeholder for the supported temperature range.

2) y is a placeholder for the QFP package variant, LQFP or TQFP depending on the stepping, see **Section 1.3**.

1.3 Package Variants

Different markings of the XMC4400 use different package variants. Details of those packages are given in the **Package Parameters** section of the Data Sheet.

Table 2 XMC4400 **Package Variants**

Package Variant	Marking	Package
XMC4400-F100	EES-AA, ES-AA, ES-AB, AB	PG-LQFP-100-11
XMC4400-F64		PG-LQFP-64-19
XMC4400-F100	BA	PG-LQFP-100-25
XMC4400-F64		PG-TQFP-64-19

1.4 Device Type Features

The following table lists the available features per device type.

Table 3 **Features of** XMC4400 **Device Types**

Derivative[1)]	LEDTS Intf.	ETH Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4400-F100x512	1	RMII	1	2 x 2	N0, N1 MO[0..63]
XMC4400-F64x512	1	RMII	1	2 x 2	N0, N1 MO[0..63]
XMC4400-F100x256	1	RMII	1	2 x 2	N0, N1 MO[0..63]
XMC4400-F64x256	1	RMII	1	2 x 2	N0, N1 MO[0..63]
XMC4402-F100x256	1	–	1	2 x 2	N0, N1 MO[0..63]
XMC4402-F64x256	1	–	1	2 x 2	N0, N1 MO[0..63]

1) x is a placeholder for the supported temperature range.

Table 4 Features of XMC4400 Device Types

Derivative[1)]	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.	HRPWM Intf.
XMC4400-F100x512	24	4	2	4 x 4	2 x 4	2	1
XMC4400-F64x512	14	4	2	4 x 4	2 x 4	2	1
XMC4400-F100x256	24	4	2	4 x 4	2 x 4	2	1
XMC4400-F64x256	14	4	2	4 x 4	2 x 4	2	1
XMC4402-F100x256	24	4	2	4 x 4	2 x 4	2	1
XMC4402-F64x256	14	4	2	4 x 4	2 x 4	2	1

1) x is a placeholder for the supported temperature range.

1.5 Definition of Feature Variants

The XMC4400 types are offered with several memory sizes and number of available VADC channels. **Table 5** describes the location of the available Flash memory, **Table 6** describes the location of the available SRAMs, **Table 7** the available VADC channels.

Table 5 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
256 Kbytes	$0800\ 0000_H$ – $0803\ FFFF_H$	$0C00\ 0000_H$ – $0C03\ FFFF_H$
512 Kbytes	$0800\ 0000_H$ – $0807\ FFFF_H$	$0C00\ 0000_H$ – $0C07\ FFFF_H$

Table 6 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
80 Kbytes	$1FFF\ C000_H$ – $1FFF\ FFFF_H$	$2000\ 0000_H$ – $2000\ 7FFF_H$	$2000\ 8000_H$ – $2000\ FFFF_H$

Table 7 ADC Channels[1)]

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3
PG-LQFP-64	CH0, CH3..CH7	CH0, CH1, CH3, CH6	CH0, CH1	CH2, CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.6 Identification Registers

The identification registers allow software to identify the marking.

Table 8 XMC4400 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	$0004\ 4001_H$	EES-AA, ES-AA
SCU_IDCHIP	$0004\ 4002_H$	ES-AB, AB
SCU_IDCHIP	$0004\ 4003_H$	BA
JTAG IDCODE	$101D\ C083_H$	EES-AA, ES-AA
JTAG IDCODE	$201D\ C083_H$	ES-AB, AB
JTAG IDCODE	$301D\ C083_H$	BA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

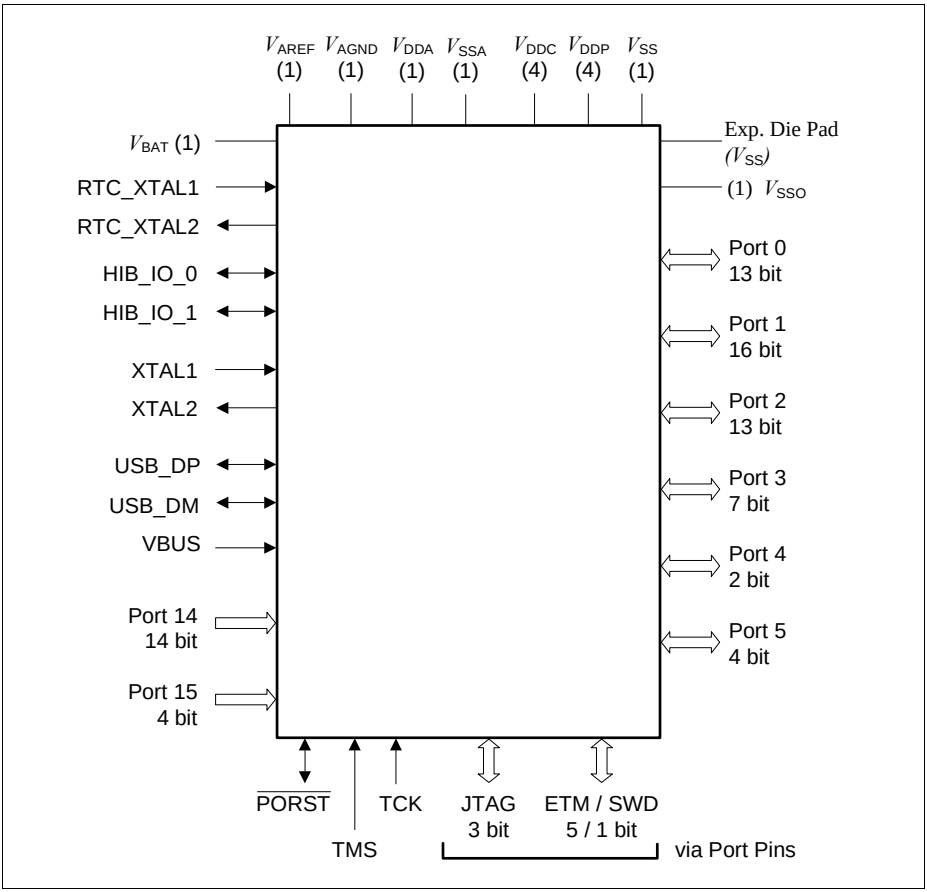

Figure 2 XMC4400 Logic Symbol PG-LQFP-100

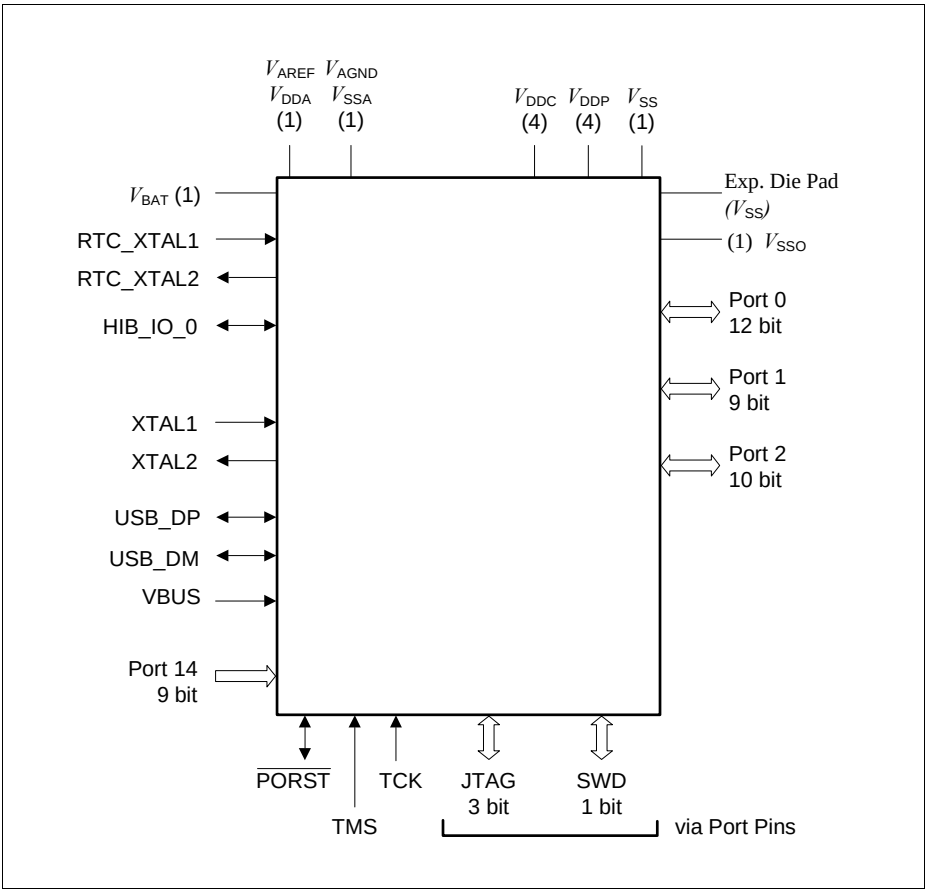

Figure 3 XMC4400 Logic Symbol PG-LQFP-64 and PG-TQFP-64

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

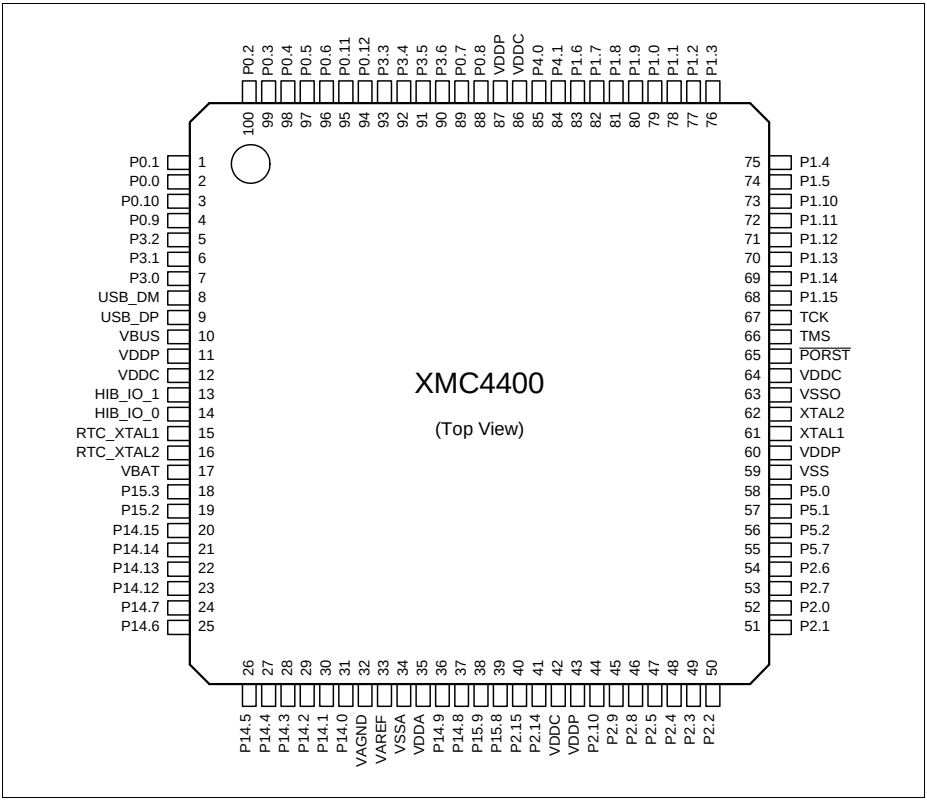

Figure 4 XMC4400 PG-LQFP-100 Pin Configuration (top view)

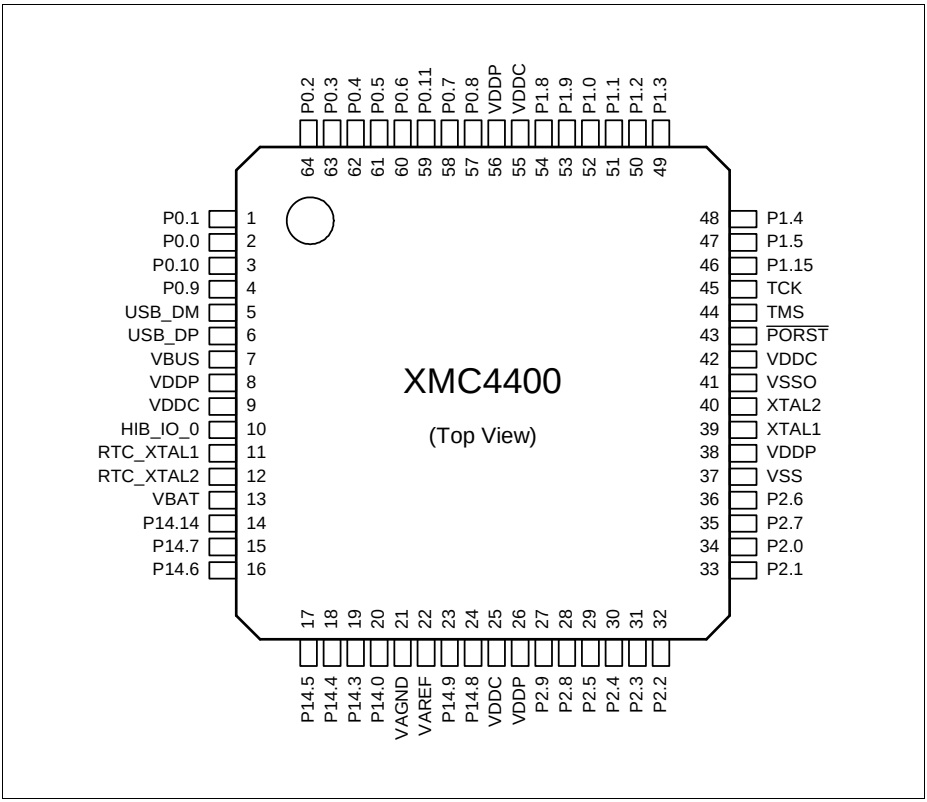

Figure 5 XMC4400 PG-LQFP-64 and PG-TQFP-64 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 9 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 10 Package Pin Mapping

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
P0.0	2	2	A1+	
P0.1	1	1	A1+	
P0.2	100	64	A2	
P0.3	99	63	A2	
P0.4	98	62	A2	
P0.5	97	61	A2	
P0.6	96	60	A2	
P0.7	89	58	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	88	57	A2	After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active.
P0.9	4	4	A2	
P0.10	3	3	A1+	

Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
P0.11	95	59	A1+	
P0.12	94	-	A1+	
P1.0	79	52	A1+	
P1.1	78	51	A1+	
P1.2	77	50	A2	
P1.3	76	49	A2	
P1.4	75	48	A1+	
P1.5	74	47	A1+	
P1.6	83	-	A2	
P1.7	82	-	A2	
P1.8	81	54	A2	
P1.9	80	53	A2	
P1.10	73	-	A1+	
P1.11	72	-	A1+	
P1.12	71	-	A2	
P1.13	70	-	A2	
P1.14	69	-	A2	
P1.15	68	46	A2	
P2.0	52	34	A2	
P2.1	51	33	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	50	32	A2	
P2.3	49	31	A2	
P2.4	48	30	A2	
P2.5	47	29	A2	
P2.6	54	36	A1+	
P2.7	53	35	A1+	
P2.8	46	28	A2	
P2.9	45	27	A2	
P2.10	44	-	A2	
P2.14	41	-	A2	
P2.15	40	-	A2	

Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
P3.0	7	-	A2	
P3.1	6	-	A2	
P3.2	5	-	A2	
P3.3	93	-	A1+	
P3.4	92	-	A1+	
P3.5	91	-	A2	
P3.6	90	-	A2	
P4.0	85	-	A2	
P4.1	84	-	A2	
P5.0	58	-	A1+	
P5.1	57	-	A1+	
P5.2	56	-	A1+	
P5.7	55	-	A1+	
P14.0	31	20	AN/DIG_IN	
P14.1	30	-	AN/DIG_IN	
P14.2	29	-	AN/DIG_IN	
P14.3	28	19	AN/DIG_IN	
P14.4	27	18	AN/DIG_IN	
P14.5	26	17	AN/DIG_IN	
P14.6	25	16	AN/DIG_IN	
P14.7	24	15	AN/DIG_IN	
P14.8	37	24	AN/DAC/DIG_IN	
P14.9	36	23	AN/DAC/DIG_IN	
P14.12	23	-	AN/DIG_IN	
P14.13	22	-	AN/DIG_IN	
P14.14	21	14	AN/DIG_IN	
P14.15	20	-	AN/DIG_IN	
P15.2	19	-	AN/DIG_IN	
P15.3	18	-	AN/DIG_IN	
P15.8	39	-	AN/DIG_IN	
P15.9	38	-	AN/DIG_IN	

Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
USB_DP	9	6	special	
USB_DM	8	5	special	
HIB_IO_0	14	10	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
HIB_IO_1	13	-	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active. As output the medium driver mode is active.
TCK	67	45	A1	Weak pull-down active.
TMS	66	44	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	65	43	special	Strong pull-down controlled by EVR. Weak pull-up active while strong pull-down is not active.
XTAL1	61	39	clock_IN	
XTAL2	62	40	clock_O	
RTC_XTAL1	15	11	clock_IN	
RTC_XTAL2	16	12	clock_O	
VBAT	17	13	Power	When VDDP is supplied VBAT has to be supplied as well.
VBUS	10	7	special	
VAREF	33	-	AN_Ref	
VAGND	32	-	AN_Ref	
VDDA	35	-	AN_Power	

Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
VDDA/VAREF	-	22	AN_Power/AN_Ref	Shared analog supply and reference voltage pin.
VSSA	34	-	AN_Power	
VSSA/VAGND	-	21	AN_Power/AN_Ref	Shared analog supply and reference ground pin.
VDDC	12	9	Power	
VDDC	42	25	Power	
VDDC	64	42	Power	
VDDC	86	55	Power	
VDDP	11	8	Power	
VDDP	43	26	Power	
VDDP	60	38	Power	
VDDP	87	56	Power	
VSS	59	37	Power	
VSSO	63	41	Power	
VSS	Exp. Pad	Exp. Pad	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.

2.2.2 Port I/O Functions

The following general scheme is used to describe each PORT pin:

Table 11 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

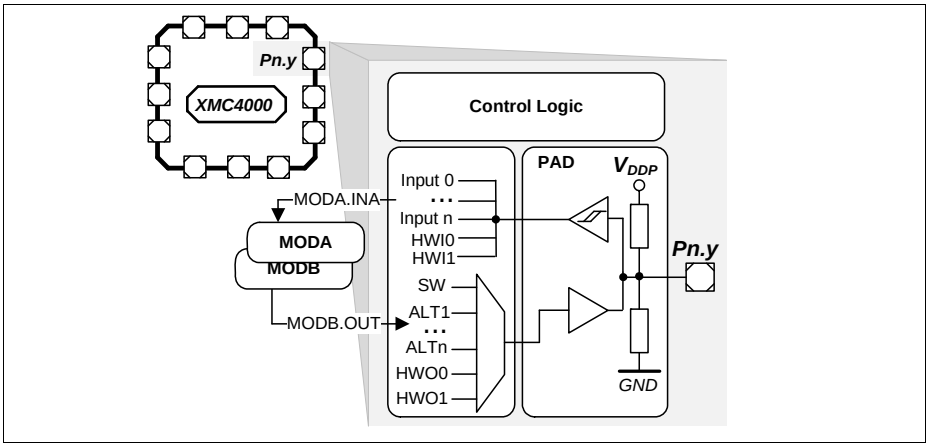

Figure 6 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

2.2.2.1 Port I/O Function Table

Table 12 Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P0.0		CAN. N0_TXD	CCU80. OUT21	LEDTS0. COL2			U1C1. DX0D	ETH0. CLK_RMIIB	ERU0. 0B0			HRPWM0. C1INB		ETH0. CLKRXB
P0.1	USB. DRIVEVBUS	U1C1. DOUT0	CCU80. OUT11	LEDTS0. COL3				ETH0. CRS_DVB	ERU0. 0A0			HRPWM0. C2INB		ETH0. RXDVB
P0.2		U1C1. SELO1	CCU80. OUT01	HRPWM0. HROUT01	U1C0. DOUT3	U1C0. HWIN3	ETH0. RXD0B		ERU0. 3B3					
P0.3			CCU80. OUT20	HRPWM0. HROUT20	U1C0. DOUT2	U1C0. HWIN2	ETH0. RXD1B			ERU1. 3B0				
P0.4	ETH0. TX_EN		CCU80. OUT10	HRPWM0. HROUT21	U1C0. DOUT1	U1C0. HWIN1		U1C0. DX0A	ERU0. 2B3					
P0.5	ETH0. TXD0	U1C0. DOUT0	CCU80. OUT00	HRPWM0. HROUT00	U1C0. DOUT0	U1C0. HWIN0		U1C0. DX0B		ERU1. 3A0				
P0.6	ETH0. TXD1	U1C0. SELO0	CCU80. OUT30	HRPWM0. HROUT30				U1C0. DX2A	ERU0. 3B2		CCU80. IN2B			
P0.7	WWDT. SERVICE_OUT	U0C0. SELO0		HRPWM0. HROUT11		DB. TDI	U0C0. DX2B	DSD. DIN1A	ERU0. 2B1		CCU80. IN0A	CCU80. IN1A	CCU80. IN2A	CCU80. IN3A
P0.8	SCU. EXTCLK	U0C0. SCLKOUT		HRPWM0. HROUT10		$\overline{\text{DB.}}$ $\overline{\text{TRST}}$	U0C0. DX1B	DSD. DIN0A	ERU0. 2A1		CCU80. IN1B			
P0.9	HRPWM0. HROUT31	U1C1. SELO0	CCU80. OUT12	LEDTS0. COL0	ETH0. MDO	ETH0. MDIA	U1C1. DX2A	USB. ID	ERU0. 1B0					
P0.10	ETH0. MDC	U1C1. SCLKOUT	CCU80. OUT02	LEDTS0. COL1			U1C1. DX1A		ERU0. 1A0					
P0.11		U1C0. SCLKOUT	CCU80. OUT31				ETH0. RXERB	U1C0. DX1A	ERU0. 3A2					
P0.12		U1C1. SELO0	CCU40. OUT3					U1C1. DX2B	ERU0. 2B2					
P1.0	DSD. CGPWMN	U0C0. SELO0	CCU40. OUT3	ERU1. PDOUT3			U0C0. DX2A		ERU0. 3B0		CCU40. IN3A	HRPWM0. C0INA		
P1.1	DSD. CGPWMP	U0C0. SCLKOUT	CCU40. OUT2	ERU1. PDOUT2			U0C0. DX1A	POSIF0. IN2A	ERU0. 3A0		CCU40. IN2A	HRPWM0. C1INA		
P1.2			CCU40. OUT1	ERU1. PDOUT1	U0C0. DOUT3	U0C0. HWIN3		POSIF0. IN1A		ERU1. 2B0	CCU40. IN1A	HRPWM0. C2INA		
P1.3		U0C0. MCLKOUT	CCU40. OUT0	ERU1. PDOUT0	U0C0. DOUT2	U0C0. HWIN2		POSIF0. IN0A		ERU1. 2A0	CCU40. IN0A	HRPWM0. C0INB		
P1.4	WWDT. SERVICE_OUT	CAN. N0_TXD	CCU80. OUT33	CCU81. OUT20	U0C0. DOUT1	U0C0. HWIN1	U0C0. DX0B	CAN. N1_RXDD	ERU0. 2B0		CCU41. IN0C	HRPWM0. BL0A		
P1.5	CAN. N1_TXD	U0C0. DOUT0	CCU80. OUT23	CCU81. OUT10	U0C0. DOUT0	U0C0. HWIN0	U0C0. DX0A	CAN. N0_RXDA	ERU0. 2A0	ERU1. 0A0	CCU41. IN1C	DSD. DIN2B		
P1.6		U0C0. SCLKOUT					DSD. DIN2A							

Table 12 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P1.7		U0C0. DOUT0	DSD. MCLK2	U1C1. SELO2				DSD. MCLK2A			DSD. MCLK0C			
P1.8		U0C0. SELO1	DSD. MCLK1	U1C1. SCLKOUT				DSD. MCLK1A			DSD. MCLK0D	DSD. MCLK2D	DSD. MCLK3D	
P1.9	U0C0. SCLKOUT		DSD. MCLK0	U1C1. DOUT0				DSD. MCLK0A			DSD. MCLK1C	DSD. MCLK2C	DSD. MCLK3C	
P1.10	ETH0. MDC	U0C0. SCLKOUT	CCU81. OUT21								CCU41. IN2C			
P1.11		U0C0. SELO0	CCU81. OUT11		ETH0. MDO	ETH0. MDIC					CCU41. IN3C			
P1.12	ETH0. TX_EN	CAN. N1_TXD	CCU81. OUT01											
P1.13	ETH0. TXD0	U0C1. SELO3	CCU81. OUT20				CAN. N1_RXDC							
P1.14	ETH0. TXD1	U0C1. SELO2	CCU81. OUT10											
P1.15	SCU. EXTCLK	DSD. MCLK2	CCU81. OUT00	U1C0. DOUT0	DB. ETM_TRACEDATA3			DSD. MCLK2B		ERU1. 1A0				
P2.0	CAN. N0_TXD	CCU81. OUT21	DSD. CGPWMN	LEDTS0. COL1	ETH0. MDO	ETH0. MDIB			ERU0. 0B3		CCU40. IN1C			
P2.1		CCU81. OUT11	DSD. CGPWMP	LEDTS0. COL0	DB.TDO/ TRACESWO		ETH0. CLK_RMIIA			ERU1. 0B0	CCU40. IN0C			ETH0. CLKRXA
P2.2	VADC. EMUX00	CCU81. OUT01	CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	LEDTS0. TSIN0A	ETH0. RXD0A	U0C1. DX0A	ERU0. 1B2		CCU41. IN3A			
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	LEDTS0. TSIN1A	ETH0. RXD1A	U0C1. DX2A	ERU0. 1A2	POSIF1. IN2A	CCU41. IN2A			
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	LEDTS0. TSIN2A	ETH0. RXERA	U0C1. DX1A	ERU0. 0B2	POSIF1. IN1A	CCU41. IN1A	HRPWM0. BL1A		
P2.5	ETH0. TX_EN	U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	LEDTS0. TSIN3A	ETH0. RXDVA	U0C1. DX0B	ERU0. 0A2	POSIF1. IN0A	CCU41. IN0A	HRPWM0. BL2A		ETH0. CRS_DVA
P2.6			CCU80. OUT13	LEDTS0. COL3			DSD. DIN1B	CAN. N1_RXDA	ERU0. 1B3		CCU40. IN3C			
P2.7	ETH0. MDC	CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2			DSD. DIN0B			ERU1. 1B0	CCU40. IN2C			
P2.8	ETH0. TXD0		CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	LEDTS0. TSIN4A	DAC. TRIGGER5				CCU40. IN0B	CCU40. IN1B	CCU40. IN2B	CCU40. IN3B
P2.9	ETH0. TXD1		CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	LEDTS0. TSIN5A	DAC. TRIGGER4				CCU41. IN0B	CCU41. IN1B	CCU41. IN2B	CCU41. IN3B
P2.10	VADC. EMUX10													
P2.14	VADC. EMUX11	U1C0. DOUT0	CCU80. OUT21		DB. ETM_TRACECLK			U1C0. DX0D			CCU43. IN0B	CCU43. IN1B	CCU43. IN2B	CCU43. IN3B
P2.15	VADC. EMUX12		CCU80. OUT11	LEDTS0. LINE6	LEDTS0. EXTENDED6	LEDTS0. TSIN6A	ETH0. COLA	U1C0. DX0C			CCU42. IN0B	CCU42. IN1B	CCU42. IN2B	CCU42. IN3B

Table 12 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P3.0		U0C1. SCLKOUT	CCU42. OUT0				U0C1. DX1B				CCU80. IN2C	CCU81. IN0C		
P3.1		U0C1. SELO0					U0C1. DX2B		ERU0. 0B1		CCU80. IN1C			
P3.2	USB. DRIVEVBUS	CAN. N0_TXD		LEDTS0. COLA					ERU0. 0A1		CCU80. IN0C			
P3.3		U1C1. SELO1	CCU42. OUT3					DSD. DIN3B			CCU42. IN3A	CCU80. IN3B		
P3.4		U1C1. SELO2	CCU42. OUT2	DSD. MCLK3				DSD. MCLK3B			CCU42. IN2A	CCU80. IN0B		
P3.5		U1C1. SELO3	CCU42. OUT1	U0C1. DOUT0					ERU0. 3B1		CCU42. IN1A			
P3.6		U1C1. SELO4	CCU42. OUT0	U0C1. SCLKOUT	DB. ETM_TRACEDATA0				ERU0. 3A1		CCU42. IN0A			
P4.0			DSD. MCLK1		DB. ETM_TRACEDATA1		U1C1. DX1C	DSD. MCLK1B	U0C1. DX0E					
P4.1		U1C1. MCLKOUT	DSD. MCLK0	U0C1. SELO0	DB. ETM_TRACEDATA2			DSD. MCLK0B			DSD. MCLK1D			
P5.0		DSD. CGPWMN	CCU81. OUT33					ETH0. RXD0D	U0C0. DX0D		CCU81. IN0A	CCU81. IN1A	CCU81. IN2A	CCU81. IN3A
P5.1	U0C0. DOUT0	DSD. CGPWMP	CCU81. OUT32					ETH0. RXD1D			CCU81. IN0B			
P5.2			CCU81. OUT23					ETH0. CRS_DVD			CCU81. IN1B			ETH0. RXDVD
P5.7			CCU81. OUT02	LEDTS0. COLA										
P14.0							VADC. G0CH0							
P14.1							VADC. G0CH1							
P14.2							VADC. G0CH2	VADC. G1CH2						
P14.3							VADC. G0CH3	VADC. G1CH3			CAN. N0_RXDB			
P14.4							VADC. G0CH4		VADC. G2CH0					
P14.5							VADC. G0CH5		VADC. G2CH1		POSIF0. IN2B			
P14.6							VADC. G0CH6				POSIF0. IN1B		G0ORC6	
P14.7							VADC. G0CH7				POSIF0. IN0B		G0ORC7	
P14.8					DAC. OUT_0			VADC. G1CH0		VADC. G3CH2	ETH0. RXD0C			

Table 12 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P14.9					DAC. OUT_1			VADC. G1CH1		VADC. G3CH3	ETH0. RXD1C			
P14.12								VADC. G1CH4						
P14.13								VADC. G1CH5						
P14.14								VADC. G1CH6					G1ORC6	
P14.15								VADC. G1CH7					G1ORC7	
P15.2									VADC. G2CH2					
P15.3									VADC. G2CH3					
P15.8										VADC. G3CH0	ETH0. CLK_RMIIC			ETH0. CLKRXC
P15.9										VADC. G3CH1	ETH0. CRS_DVC			ETH0. RXDVC
USB_DP														
USB_DM														
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT					WAKEUPA							
HIB_IO_1	HIBOUT	WWDT. SERVICE_OUT					WAKEUPB							
TCK						DB.TCK/ SWCLK								
TMS					DB.TMS/ SWDIO									
$\overline{\text{PORST}}$														
XTAL1							U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F				
XTAL2														
RTC_XTAL1									ERU0. 1B1					
RTC_XTAL2														

2.3 Power Connection Scheme

Figure 7. shows a reference power connection scheme for the XMC4400.

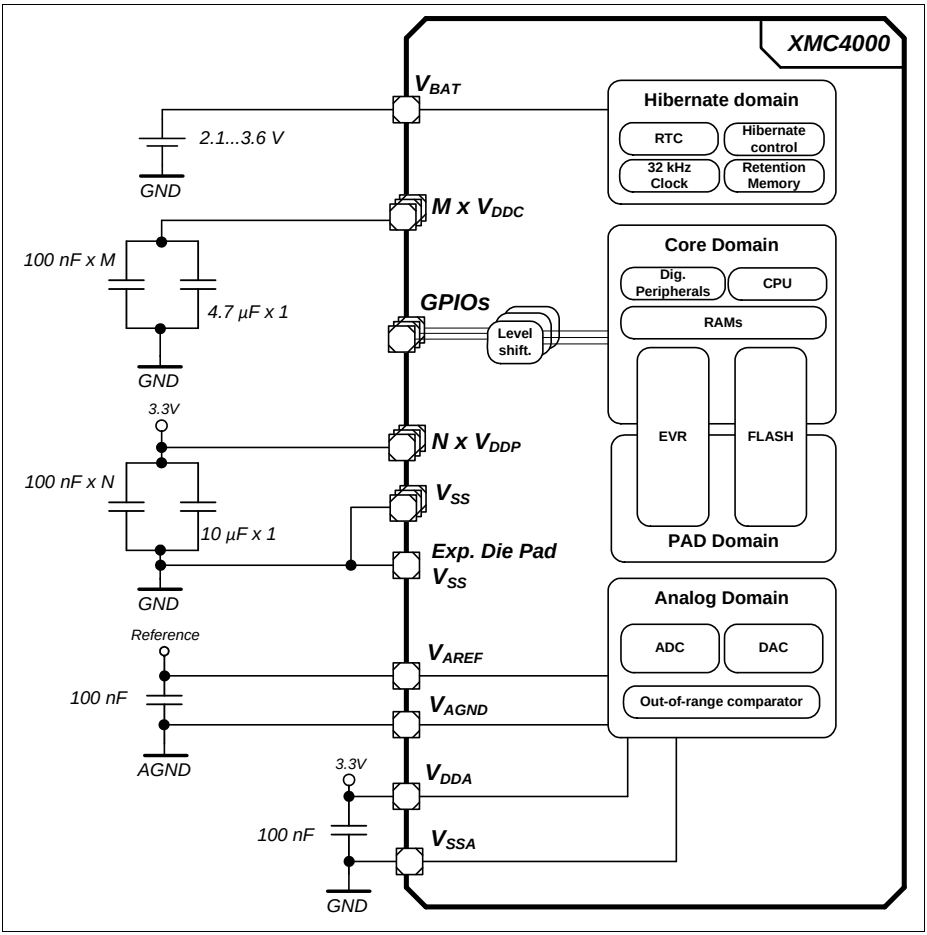

Figure 7 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS}. An additional 10 µF capacitor is connected to the V_{DDP} nets and an additional 4.7uF capacitor to the V_{DDC} nets.

The XMC4400 has a common ground concept, all V_{SS}, V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

V_{AGND} is the low potential to the analog reference V_{AREF}. Depending on the application it can share the common ground or have a different potential. In devices with shared V_{DDA}/V_{AREF} and V_{SSA}/V_{AGND} pins the reference is tied to the supply. Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT}, the V_{BAT} pin can also be connected directly to V_{DDP}.

3 Electrical Parameters

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4400 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4400 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4400 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 13 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition[1)]	ΣI_{IN}	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	SR	-100	–	+100	mA	

1) The port groups are defined in **Table 17**.

Figure 8 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

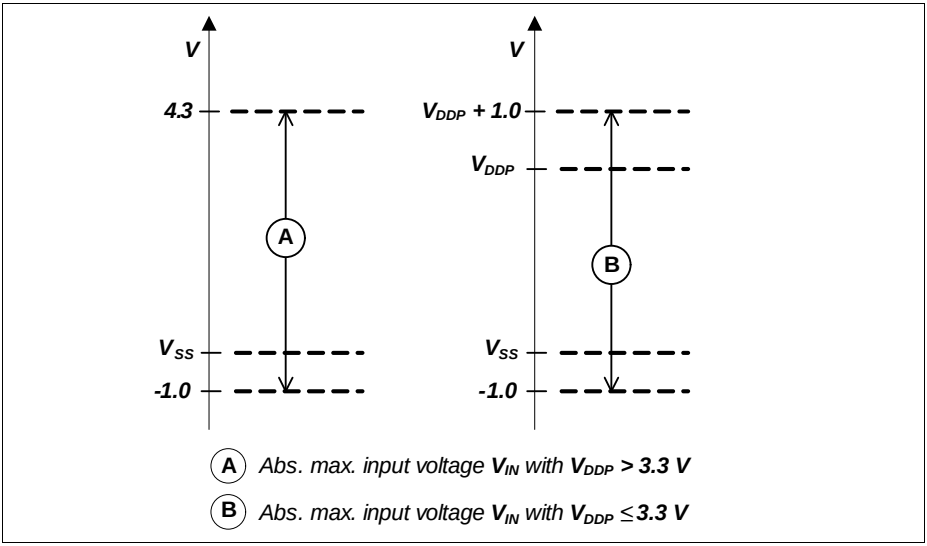

Figure 8 Absolute Maximum Input Voltage Ranges

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 14 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 14 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{OVG} SR	–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} < 0$ mA
		–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in **Table 17**.

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

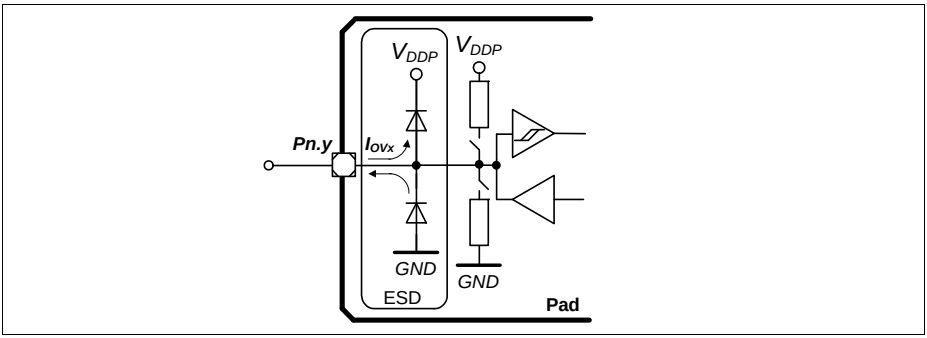

Figure 9 Input Overload Current via ESD structures

Table 15 and **Table 16** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 15 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V
A2	$V_{IN} = V_{DDP}$ + 0.7 V	$V_{IN} = V_{DDP}$ + 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V

Table 16 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{SS}$ - 1.0 V	$V_{IN} = V_{SS}$ - 0.75 V
A2	$V_{IN} = V_{SS}$ - 0.7 V	$V_{IN} = V_{SS}$ - 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ - 1.0 V	$V_{IN} = V_{DDP}$ - 0.75 V

Table 17 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[12:0], P3.[6:0]
2	P14.[15:0], P15.[9:2]
3	P2.[15:0], P5.[7:0]
4	P1.[15:0], P4.[1:0]

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 3.2.1**.

Table 18 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended
			A2 (e.g. ext. Bus)	80 MHz	15 pF	Series termination recommended

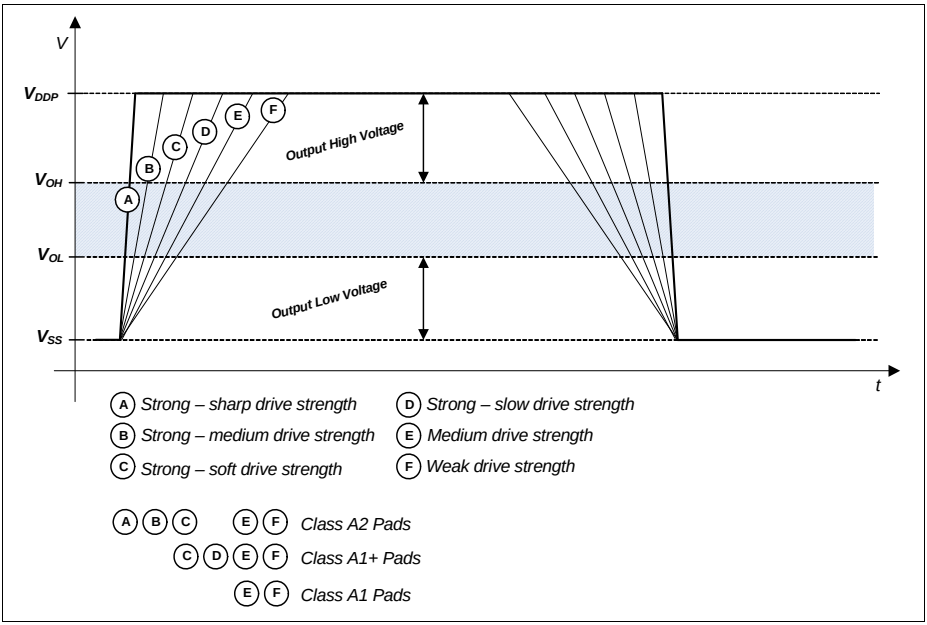

Figure 10 Output Slopes with different Pad Driver Modes

Figure 10 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4400. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 19 Operating Conditions Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient Temperature	T_A	SR	-40	–	85	°C	Temp. Range F
			-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP}	SR	3.13[1]	3.3	3.63[2]	V	
Core Supply Voltage	V_{DDC}	CC	–[1]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS}	SR	0	–	–	V	
ADC analog supply voltage	V_{DDA}	SR	3.0	3.3	3.6[2]	V	
Analog ground voltage for V_{DDA}	V_{SSA}	SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain[3]	V_{BAT}	SR	1.95[4]	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied too.
System Frequency	f_{SYS}	SR	–	–	120	MHz	
Short circuit current of digital outputs	I_{SC}	SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[5]	ΣI_{SC_PG}	SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D}	SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, **Section 3.3.2**.

2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) Different limits apply for LPAC operation, **Section 3.2.6**

4) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

5) The port groups are defined in **Table 17**.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Standard Pad Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ CC	150	–	µA	1) $V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	µA	2) $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-Up current	$\lvert I_{PUH}\rvert$ SR	–	10	µA	2) $V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	µA	1) $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	$HYSA$ SR	$0.1 \times V_{DDP}$	–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13	–	mA	V_{IN} = 1.0 V

1) Current required to override the pull device with the opposite logic level (“force current”). With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”). With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

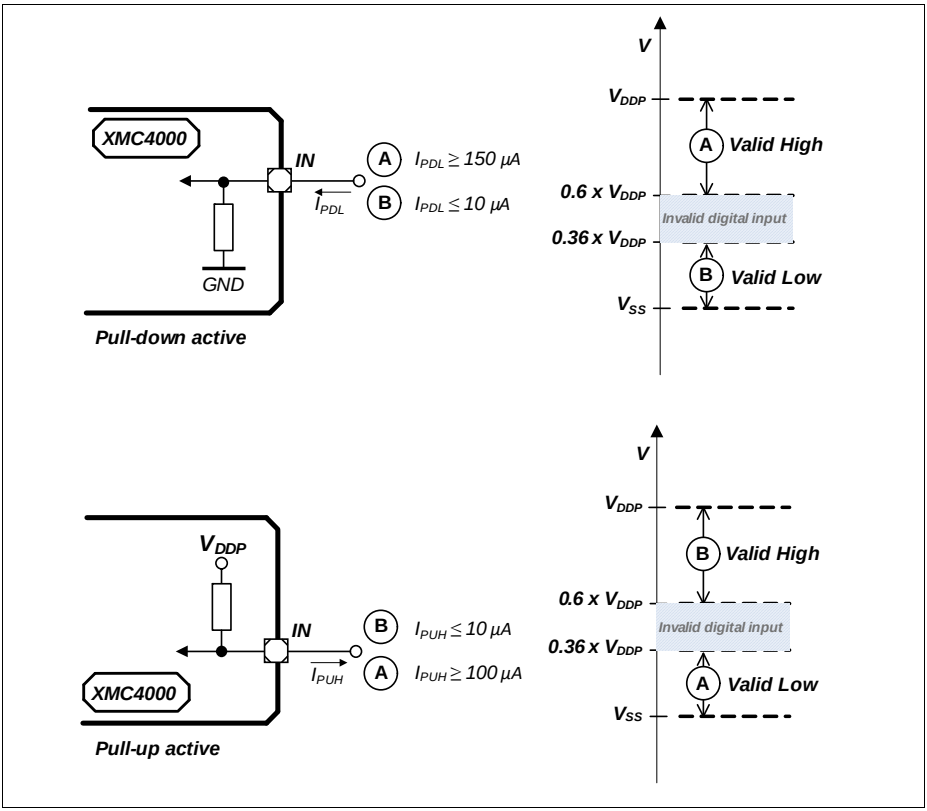

Figure 11 Pull Device Input Characteristics

Figure 11 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

Table 21 Standard Pads Class_A1

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZA1} CC	-500		500	nA	0 V ≤ V_{IN} ≤ V_{DDP}
Input high voltage	V_{IHA1} SR	0.6 × V_{DDP}		V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA1} SR	-0.3		0.36 × V_{DDP}	V	
Output high voltage, POD[1] = weak	V_{OHA1} CC	V_{DDP} - 0.4		–	V	I_{OH} ≥ -400 µA
		2.4		–	V	I_{OH} ≥ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	I_{OH} ≥ -1.4 mA
		2.4		–	V	I_{OH} ≥ -2 mA
Output low voltage	V_{OLA1} CC	–		0.4	V	I_{OL} ≤ 500 µA; POD[1] = weak
		–		0.4	V	I_{OL} ≤ 2 mA; POD[1] = medium
Fall time	t_{FA1} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
Rise time	t_{RA1} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium

1) POD = Pin Out Driver

Table 22 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZA1+} CC	-1		1	µA	0 V ≤ V_{IN} ≤ V_{DDP}
Input high voltage	V_{IHA1+} SR	0.6 × V_{DDP}		V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA1+} SR	-0.3		0.36 × V_{DDP}	V	

Table 22 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Output high voltage, POD[1] = weak	V_{OHA1+} CC	V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -400 µA
		2.4		–	V	$I_{OH} \geq$ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output high voltage, POD[1] = strong		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output low voltage	V_{OLA1+} CC	–		0.4	V	$I_{OL} \leq$ 500 µA; POD[1] = weak
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = medium
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = strong
Fall time	t_{FA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft;
Rise time	t_{RA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft

1) POD = Pin Out Driver

Table 23 Standard Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input Leakage current	I_{OZA2} CC	-6		6	µA	0 V ≤ V_{IN} < 0.5*V_{DDP} - 1 V; 0.5*V_{DDP} + 1 V <V_{IN} ≤ V_{DDP}
		-3		3	µA	0.5*V_{DDP} - 1 V < V_{IN} < 0.5*V_{DDP} + 1 V
Input high voltage	V_{IHA2} SR	0.6 × V_{DDP}		V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA2} SR	-0.3		0.36 × V_{DDP}	V	
Output high voltage, POD = weak	V_{OHA2} CC	V_{DDP} - 0.4		–	V	I_{OH} ≥ -400 µA
		2.4		–	V	I_{OH} ≥ -500 µA
Output high voltage, POD = medium		V_{DDP} - 0.4		–	V	I_{OH} ≥ -1.4 mA
		2.4		–	V	I_{OH} ≥ -2 mA
Output high voltage, POD = strong		V_{DDP} - 0.4		–	V	I_{OH} ≥ -1.4 mA
		2.4		–	V	I_{OH} ≥ -2 mA
Output low voltage, POD = weak	V_{OLA2} CC	–		0.4	V	I_{OL} ≤ 500 µA
Output low voltage, POD = medium		–		0.4	V	I_{OL} ≤ 2 mA
Output low voltage, POD = strong		–		0.4	V	I_{OL} ≤ 2 mA

Table 23 Standard Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Fall time	t_{FA2} CC	–		150	ns	C_L = 20 pF; POD = weak
		–		50	ns	C_L = 50 pF; POD = medium
		–		3.7	ns	C_L = 50 pF; POD = strong; edge = sharp
		–		7	ns	C_L = 50 pF; POD = strong; edge = medium
		–		16	ns	C_L = 50 pF; POD = strong; edge = soft
Rise time	t_{RA2} CC	–		150	ns	C_L = 20 pF; POD = weak
		–		50	ns	C_L = 50 pF; POD = medium
		–		3.7	ns	C_L = 50 pF; POD = strong; edge = sharp
		–		7.0	ns	C_L = 50 pF; POD = strong; edge = medium
		–		16	ns	C_L = 50 pF; POD = strong; edge = soft

Table 24 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZHIB} CC	-500		500	nA	0 V ≤ V_{IN} ≤ V_{BAT}
Input high voltage	V_{IHHIB} SR	0.6 × V_{BAT}		V_{BAT} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3		0.36 × V_{BAT}	V	
Input Hysteresis for HIB_IO pins[1)]	$HYSHIB$ CC	0.1 × V_{BAT}		–	V	V_{BAT} ≥ 3.13 V
		0.06 × V_{BAT}		–	V	V_{BAT} < 3.13 V
Output high voltage, POD[1)] = medium	V_{OHHIB} CC	V_{BAT} - 0.4		–	V	I_{OH} ≥ -1.4 mA
Output low voltage	V_{OLHIB} CC	–		0.4	V	I_{OL} ≤ 2 mA
Fall time	t_{FHIB} CC	–		50	ns	V_{BAT} ≥ 3.13 V C_L = 50 pF
		–		100	ns	V_{BAT} < 3.13 V C_L = 50 pF
Rise time	t_{RHIB} CC	–		50	ns	V_{BAT} ≥ 3.13 V C_L = 50 pF
		–		100	ns	V_{BAT} < 3.13 V C_L = 50 pF

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.2 Analog to Digital Converters (ADCx)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage[5]	V_{AREF} SR	V_{AGND} + 1	–	V_{DDA} + 0.05[1]	V	
Analog reference ground[5]	V_{AGND} SR	V_{SSM} - 0.05	–	V_{AREF} - 1	V	
Analog reference voltage range[2][5]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0\ V \le V_{AIN} \le 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \le V_{AIN} \le V_{DDA}$
Input leakage current at VAREF	I_{OZ2} CC	-1	–	1	µA	$0\ V \le V_{AREF} \le V_{DDA}$
Input leakage current at VAGND	I_{OZ3} CC	-1	–	1	µA	$0\ V \le V_{AGND} \le V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	30	MHz	V_{DDA} = 3.3 V
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the positive reference voltage input[5][6]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[5]	$C_{AREFTOT}$ CC	–	20	40	pF	

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Unadjusted Error	TUE CC	-4	–	4	LSB	12-bit resolution[7]; V_{DDA} = 3.3 V; V_{AREF} = V_{DDA}, dedicated pins for V_{DDA} and V_{AREF}
Differential Non-Linearity Error[8]	EA_{DNL} CC	-3	–	3	LSB	
Gain Error[8]	EA_{GAIN} CC	-4	–	4	LSB	
Integral Non-Linearity[8]	EA_{INL}CC	-3	–	3	LSB	
Offset Error[8]	EA_{OFF} CC	-4	–	4	LSB	
Total Unadjusted Error	TUE CC	-6	–	6	LSB	12-bit resolution[7]; V_{DDA} = 3.3 V; V_{AREF} = V_{DDA}, shared pin for V_{DDA} and V_{AREF} (PG-LQFP-64)
Differential Non-Linearity Error[8]	EA_{DNL} CC	-4.5	–	4.5	LSB	
Gain Error[8]	EA_{GAIN} CC	-6	–	6	LSB	
Integral Non-Linearity[8]	EA_{INL}CC	-4.5	–	4.5	LSB	
Offset Error[8]	EA_{OFF} CC	-6	–	6	LSB	
RMS Noise[9]	EN_{RMS} CC	–	1	2[10][11]	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150 °C
Charge consumption on V_{AREF} per conversion[5]	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA}[12]
ON resistance of the analog input path	R_{AIN} CC	–	700	1 200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	–	700	1 700	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).

2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.

3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 14**).
4) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}/2$ before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from $V_{AREF}/2$.
5) Applies to AINx, when used as alternate reference input.
6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.
8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.
9) This parameter is valid for soldered devices and requires careful analog board design.
10) Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS}.
11) Value is defined for one sigma Gauss distribution.
12) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of t_c = 550 ns results in a typical average current of I_{AREF} = 54.5 µA.

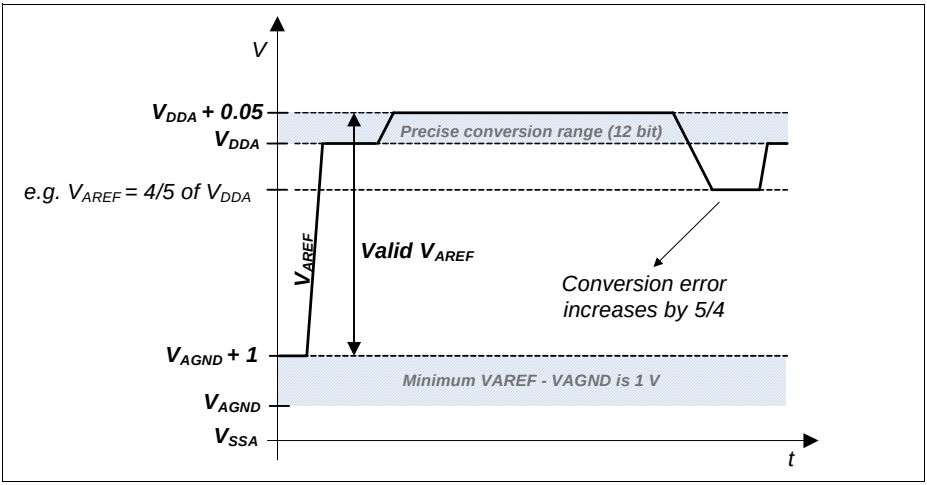

Figure 12 VADC Reference Voltage Range

The power-up calibration of the ADC requires a maximum number of 4 352 f_{ADCI} cycles.

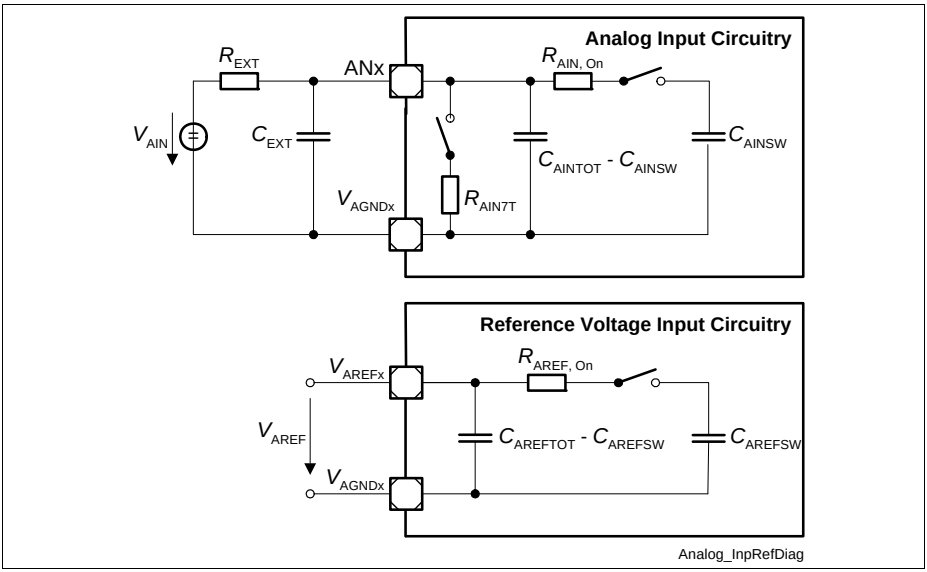

Figure 13 ADCx Input Circuits

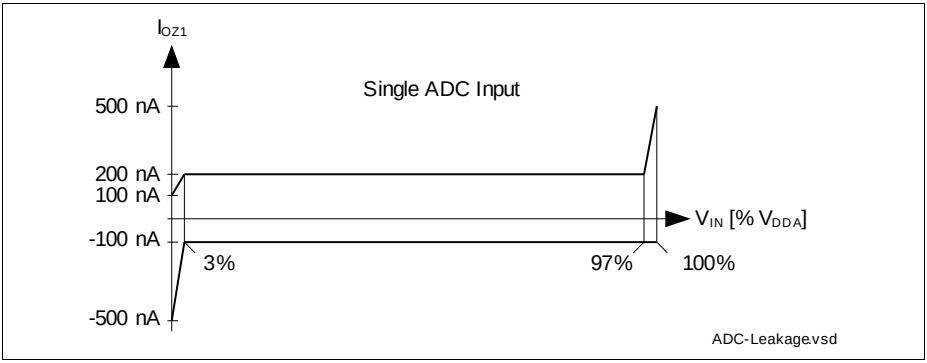

Figure 14 ADCx Analog Input Leakage Current

Conversion Time

Table 26 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time	t_C CC	$2 \times T_{ADC}$ + (2 + N + STC + PC +DM) × T_{ADCI}	µs	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions:
f_{ADC} = 120 MHz i.e. t_{ADC} = 8.33 ns, DIVA = 3, f_{ADCI} = 30 MHz i.e. t_{ADCI} = 33.3 ns
According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.3$ ns $+ 2 \times 8.33$ ns = 550 ns

12-bit uncalibrated conversion:
$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 33.3$ ns $+ 2 \times 8.33$ ns = 483 ns

10-bit uncalibrated conversion:
$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 33.3$ ns $+ 2 \times 8.33$ ns = 417 ns

8-bit uncalibrated:
$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 33.3$ ns $+ 2 \times 8.33$ ns = 350 ns

3.2.3 Digital to Analog Converters (DACx)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 DAC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
RMS supply current	I_{DD}	CC	–	2.5	4	mA	per active DAC channel, without load currents of DAC outputs
Resolution	RES	CC	–	12	–	Bit	
Update rate	f_{URATE_A}	CC	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy
Update rate	f_{URATE_F}	CC	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy
Settling time	t_{SETTLE}	CC	–	1	2	µs	at full scale jump, output voltage reaches target value ± 20 LSB
Slew rate	SR	CC	2	5	–	V/µs	
Minimum output voltage	V_{OUT_MIN}	CC	–	0.3	–	V	code value unsigned: 000_H; signed: 800_H
Maximum output voltage	V_{OUT_MAX}	CC	–	2.5	–	V	code value unsigned: FFF_H; signed: $7FF_H$
Integral non-linearity[1)]	INL	CC	-5.5	±2.5	5.5	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Differential non-linearity	DNL	CC	-2	±1	2	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF

Table 27 DAC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Offset error	ED_{OFF}	CC		±20		mV	
Gain error	ED_{G_IN}	CC	-5	0	5	%	
Startup time	$t_{STARTUP}$	CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1}	CC	2.5	5	–	MHz	verified by design
Output sourcing current	I_{OUT_SOURCE}	CC	–	-30	–	mA	
Output sinking current	I_{OUT_SINK}	CC	–	0.6	–	mA	
Output resistance	R_{OUT}	CC	–	50	–	Ohm	
Load resistance	R_L	SR	5	–	–	kOhm	
Load capacitance	C_L	SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	*PSRR*	CC	–	56	–	dB	to V_{DDA} verified by design

1) According to best straight line method.

Conversion Calculation

Unsigned:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN})
Signed:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN}) - 2048

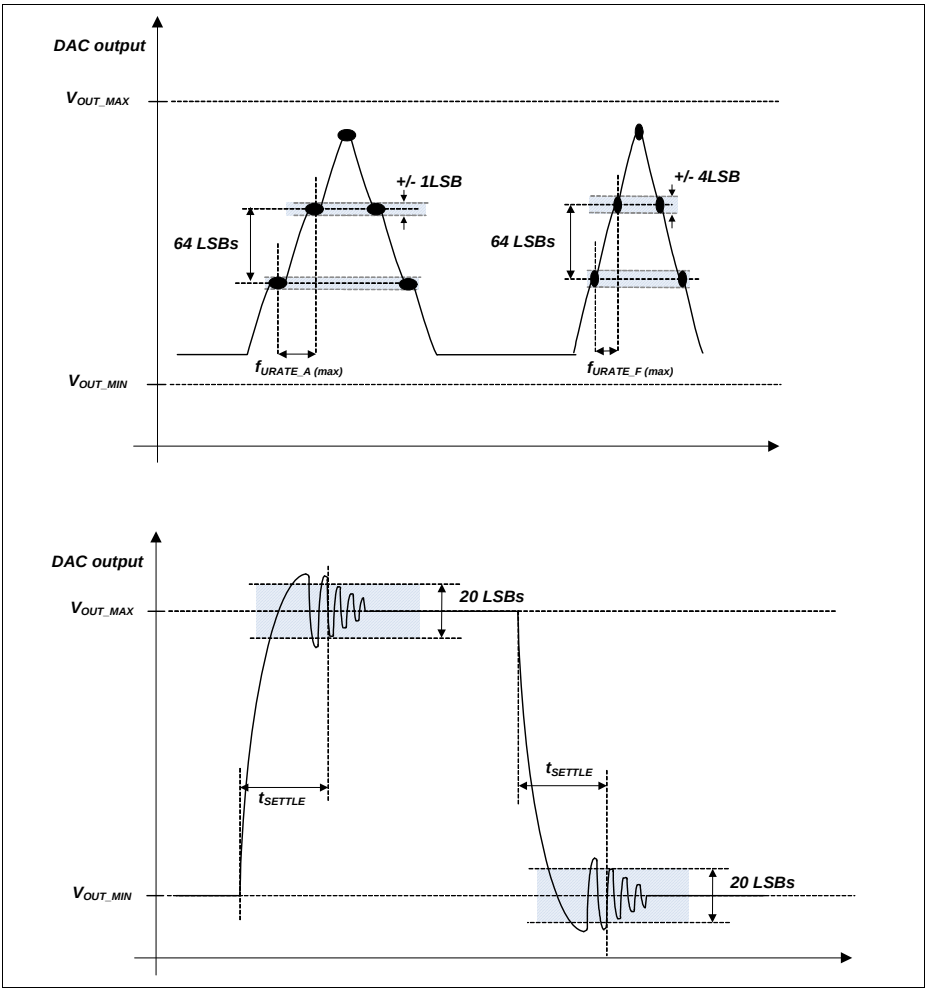

Figure 15 DAC Conversion Examples

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 28** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 28 ORC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	100	125	200	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	55	–	450	ns	$V_{AIN} \geq V_{AREF} + 200$ mV
			45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Always detected Overvoltage Pulse	t_{OPDD}	CC	440	–	–	ns	$V_{AIN} \geq V_{AREF} + 200$ mV
			90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	49	ns	$V_{AIN} \geq V_{AREF} + 200$ mV
			–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Release Delay	t_{ORD}	CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	t_{OED}	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.

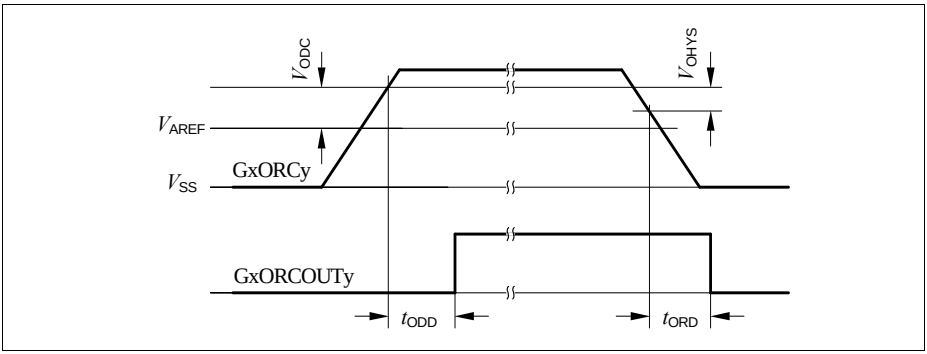

Figure 16 GxORCOUTy Trigger Generation

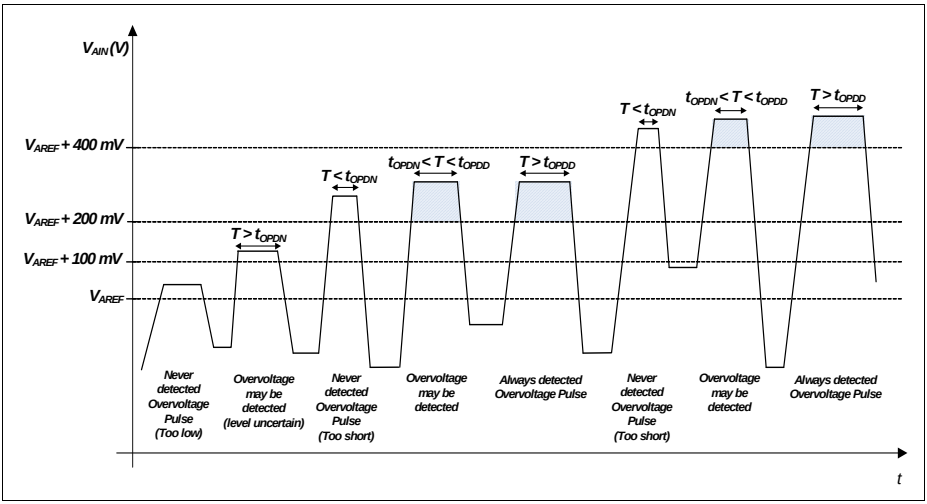

Figure 17 ORC Detection Ranges

3.2.5 High Resolution PWM (HRPWM)

The following chapters describe the operating conditions, characteristics and timing requirements, for all the components inside the HRPWM module. Each description is given for just one sub unit, e.g., one CSG or one HRC.

All the timing information is related to the module clock, f_{hrpwm}.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.2.5.1 HRC characteristics

Table 29 summarizes the characteristics of the HRC units.

Table 29 HRC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High resolution step size[1)2)]	t_{HRS} CC	–	150	–	ps	
Startup time (after reset release)	t_{start} CC	–	–	2	µs	

1) The step size for clock frequencies equal to 180, 120 and 80 MHz is 150 ps.

2) The step size for clock frequencies different from 180, 120 and 80 MHz but within the range from 180 to 64 MHz can be between 118 to 180 ps (fixed over process and operating conditions)

3.2.5.2 CMP and 10-bit DAC characteristics

The **Table 30** summarizes the characteristics of the CSG unit.

The specified characteristics require that the setup of the HRPWM follows the initialization sequence as documented in the Reference Manual.

Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAC Resolution	*RES* CC		10		bits	
DAC differential nonlinearity	*DNL CC*	-1	–	1.5	LSB	Monotonic behavior, See **Figure 18**
DAC integral nonlinearity	*INL* CC	-3	–	3	LSB	See **Figure 18**

Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSG Output Jitter	D_{CSG} CC	–	–	1	clk	
Bias startup time	t_{start} CC	–	–	98	us	
Bias supply current	I_{DDbias} CC	–	–	400	µA	
CSGy startup time	t_{CSGS} CC	–	–	2	µs	
Input operation current[1]	I_{DDCIN} CC	-10	–	33	µA	See **Figure 19**
High Speed Mode						
DAC output voltage range	V_{DOUT} CC	V_{SS}	–	V_{DDP}	V	
DAC propagation delay - Full scale	t_{FShs} CC	–	–	80	ns	See **Figure 20**
Input Selector propagation delay - Full scale	t_{Dhs} CC	–	–	100	ns	See **Figure 20**
Comparator bandwidth	t_{Dhs} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDhs} CC	–	–	940	µA	
Low Speed Mode						
DAC output voltage range	V_{DOUT} CC	0.1 × V_{DDP}[2]	–	V_{DDP}	V	
DAC propagation delay - Full Scale	t_{FSls} CC	–	–	160	ns	See **Figure 20**
Input Selector propagation delay - Full Scale	t_{Dls} CC	–	–	200	ns	See **Figure 20**
Comparator bandwidth	t_{Dls} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDls} CC	–	–	300	µA	

1) Typical input resistance R_{CIN} = 100kOhm.

2) The INL error increases for DAC output voltages below this limit.

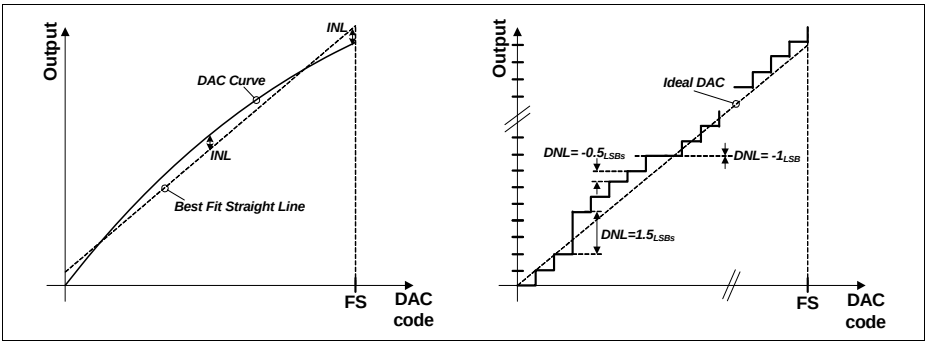

Figure 18 CSG DAC INL and DNL example

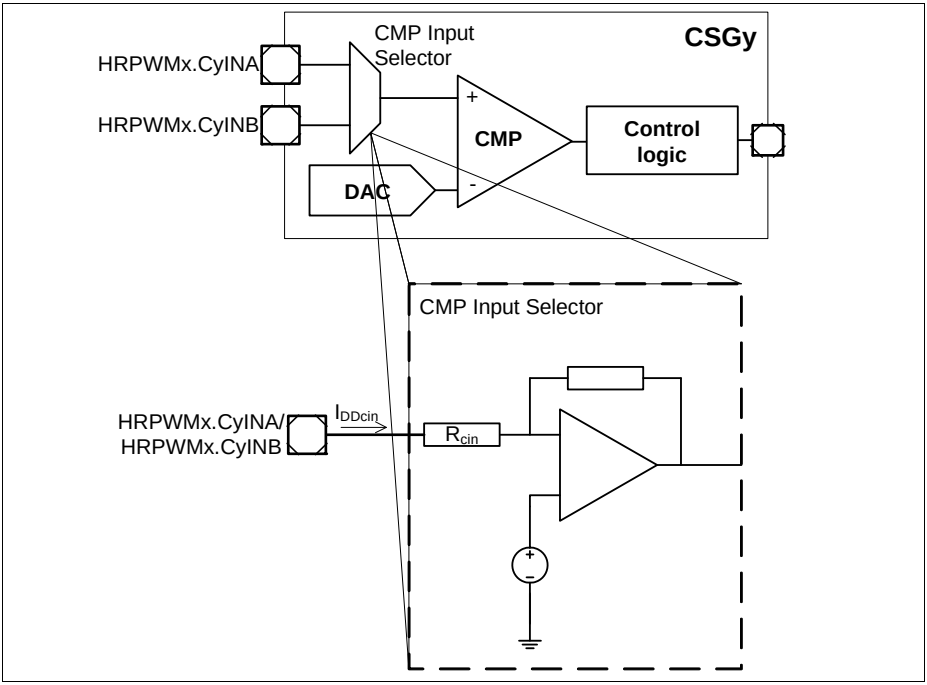

Figure 19 Input operation current

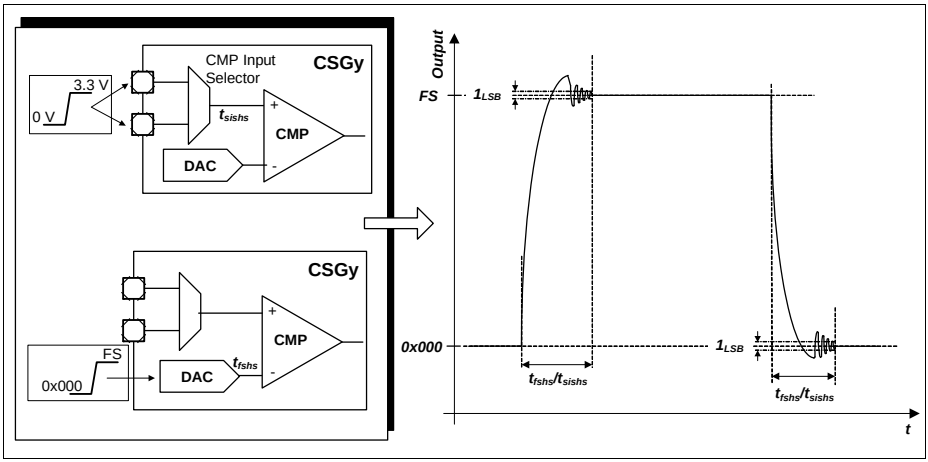

Figure 20 DAC and Input Selector Propagation Delay

3.2.5.3 Clocks

HRPWM DAC Conversion Clock

The DAC conversion clock can be generated internally or it can be controlled via a HRPWM module pin.

Table 31 External DAC conversion trigger operating conditions

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency	f_{etrg}	SR	–	–	30[2)]	MHz	
ON time	t_{onetrg}	SR	$2T_{ccu}$[1)2)]	–	–	ns	
OFF time	$t_{offetrg}$	SR	$2T_{ccu}$[1)2)]	–	–	ns	

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

CSG External Clock

It is possible to select an external source, that can be used as a clock for the slope generation, HRPWMx.ECLKy. This clock is synchronized internally with the module clock and therefore the external clock needs to meet the criterion described on **Table 32**.

Table 32 External clock operating conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency	f_{eclk} SR	–	–	$f_{hrpwm}/4$	MHz	
ON time	t_{oneclk} SR	$2T_{ccu}$ 1)2)	–	–	ns	
OFF time	$t_{offeclk}$ SR	$2T_{ccu}$ 1)2)	–	–	ns	Only the rising edge is used

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

3.2.6 Low Power Analog Comparator (LPAC)

The Low Power Analog Comparator (LPAC) triggers a wake-up event from Hibernate state or an interrupt trigger during normal operation. It does so by comparing V_{BAT} or another external sensor voltage V_{LPS} with a pre-programmed threshold voltage.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 33 Low Power Analog Comparator Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{BAT} supply voltage range for LPAC operation	V_{BAT} SR	2.1	–	3.6	V	
Sensor voltage range	V_{LPCS} CC	0	–	1.2	V	
Threshold step size	V_{th} CC	–	18.75	–	mV	
Threshold trigger accuracy	ΔV_{th} CC	–	–	±10	%	for V_{th} > 0.4 V
Conversion time	t_{LPCC} CC	–	–	250	µs	
Average current consumption over time	I_{LPCAC} CC	–	–	15	µA	conversion interval 10 ms1)
Current consumption during conversion	I_{LPCC} CC	–	150	–	µA	1)

1) Single channel conversion, measuring V_{BAT} = 3.3 V, 8 cycles settling time

3.2.7 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 34 Die Temperature Sensor Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature sensor range	T_{SR}	SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	ΔT_{LE}	CC	–	±1	–	°C	per $\Delta T_J \leq 30$ °C
Offset Error	ΔT_{OE}	CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V[1]
Measurement time	t_M	CC	–	–	100	µs	
Start-up time after reset inactive	t_{TSST}	SR	–	–	10	µs	

1) At V_{DDP_max} = 3.63 V the typical offset error increases by an additional ΔT_{OE} = ±1 °C.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

Temperature T_{DTS} = (RESULT - 605) / 2.05 [°C]

This formula and the values defined in **Table 34** apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

3.2.8 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 35 USB OTG VBUS and ID Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	V_{IN} CC	0.0	–	5.25	V	
A-device VBUS valid threshold	V_{B1} CC	4.4	–	–	V	
A-device session valid threshold	V_{B2} CC	0.8	–	2.0	V	
B-device session valid threshold	V_{B3} CC	0.8	–	4.0	V	
B-device session end threshold	V_{B4} CC	0.2	–	0.8	V	
VBUS input resistance to ground	R_{VBUS_IN} CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	R_{VBUS_PU} CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	R_{VBUS_PD} CC	656	–	–	Ohm	
USB.ID pull-up resistor	R_{UID_PU} CC	14	–	25	kOhm	
VBUS input current	I_{VBUS_IN} CC	–	–	150	µA	$0\ V \le V_{IN} \le 5.25\ V$: T_{AVG} = 1 ms

Table 36 USB OTG Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input low voltage	V_{IL}	SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH}	SR	2.0	–	–	V	
Input high voltage (floating) [1]	V_{IHZ}	SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS}	CC	0.2	–	–	V	
Differential common mode range	V_{CM}	CC	0.8	–	2.5	V	
Output low voltage	V_{OL}	CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH}	CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI}	CC	900	–	1 575	Ohm	
DP pull-up resistor (upstream port receiving)	R_{PUA}	CC	1 425	–	3 090	Ohm	
DP, DM pull-down resistor	R_{PD}	CC	14.25	–	24.8	kOhm	
Input impedance DP, DM	Z_{INP}	CC	300	–	–	kOhm	$0\ V \le V_{IN} \le V_{DDP}$
Driver output resistance DP, DM	Z_{DRV}	CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DM.

3.2.9 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal (see **Figure 21**) or in direct input mode (see **Figure 22**).

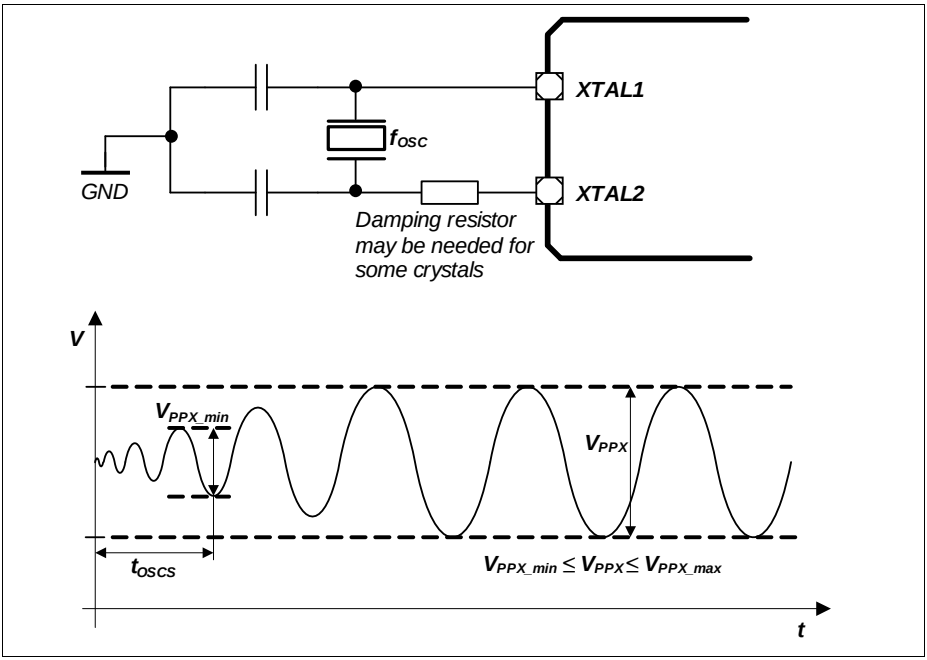

Figure 21 Oscillator in Crystal Mode

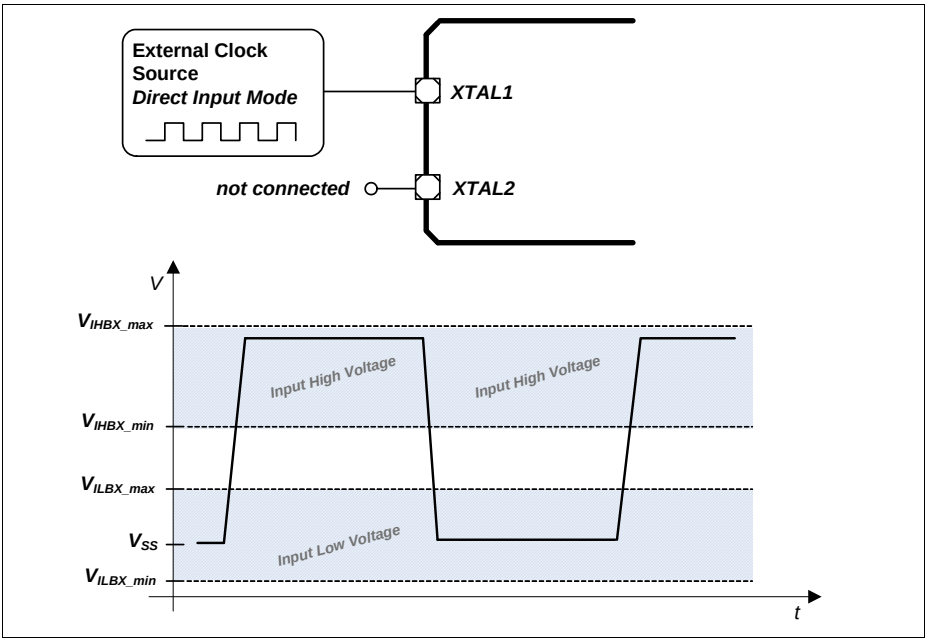

Figure 22 Oscillator in Direct Input Mode

Table 37 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1)2)]	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.5	–	V_{DDP} + 0.5	V	
Input amplitude (peak-to-peak) at XTAL1[2)3)]	V_{PPX} SR	0.4 × V_{DDP}	–	V_{DDP} + 1.0	V	
Input high voltage at XTAL1[4)]	V_{IHBX}SR	1.0	–	V_{DDP} + 0.5	V	
Input low voltage at XTAL1[4)]	V_{ILBX} SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down 0 V ≤ V_{IX} ≤ V_{DDP}

1) t_{OSCS} is defined from the moment the oscillator is enabled wih SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of 0.4 * V_{DDP}.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

Table 38 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[1)2)3)]	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	V_{BAT} + 0.3	V	
Input amplitude (peak-to-peak) at RTC_XTAL1[2)4)]	V_{PPX} SR	0.4	–	–	V	
Input high voltage at RTC_XTAL1[5)]	V_{IHBX}SR	0.6 × V_{BAT}	–	V_{BAT} + 0.3	V	
Input low voltage at RTC_XTAL1[5)]	V_{ILBX} SR	-0.3	–	0.36 × V_{BAT}	V	
Input Hysteresis for RTC_XTAL1[5)6)]	V_{HYSX} CC	0.1 × V_{BAT}		–	V	3.0 V ≤ V_{BAT} < 3.6 V
		0.03 × V_{BAT}		–	V	V_{BAT} < 3.0 V
Input leakage current at RTC_XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down 0 V ≤ V_{IX} ≤ V_{BAT}

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 400 mV.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) For a reliable start of the oscillation in crystal mode it is required that $V_{BAT} \geq 3.0$ V. A running oscillation is maintained across the full V_{BAT} voltage range.

4) If the shaper unit is enabled and not bypassed.

5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.10 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 39 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	113	–	mA	120 / 120 / 120
			–	102	–		120 / 60 / 60
			–	82	–		60 / 60 / 120
			–	61	–		24 / 24 / 24
			–	51	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	53	–	mA	120 / 120 / 120
			–	50	–		120 / 60 / 60
Active supply current[2)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} in MHz	I_{DDPA}	CC	–	80	–	mA	120 / 120 / 120
			–	80	–		120 / 60 / 60
			–	65	–		60 / 60 / 120
			–	55	–		24 / 24 / 24
			–	50	–		1 / 1 / 1

Table 39 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[3] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	104	–	mA	120 / 120 / 120
		–	93	–		120 / 60 / 60
		–	78	–		60 / 60 / 120
		–	57	–		24 / 24 / 24
		–	46	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Sleep supply current[4] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	72	–	mA	120 / 120 / 120
		–	71	–		120 / 60 / 60
		–	61	–		60 / 60 / 120
		–	52	–		24 / 24 / 24
		–	46	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Deep Sleep supply current[5] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	8	–	mA	24 / 24 / 24
		–	5	–		4 / 4 / 4
		–	4	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	4.5	–		100 / 100 / 100 [6]
Hibernate supply current RTC on[7]	I_{DDPH} CC	–	12.8	–	µA	V_{BAT} = 3.3 V
		–	9.0	–		V_{BAT} = 2.4 V
		–	7.7	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8]	I_{DDPH} CC	–	12.0	–	µA	V_{BAT} = 3.3 V
		–	8.4	–		V_{BAT} = 2.4 V
		–	7.0	–		V_{BAT} = 2.0 V
Worst case active supply current[9]	I_{DDPA} CC	–	–	170 [10]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	–[11]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	–	30	mA	V_{DDP} = 3.6 V, T_J = 150 °C

Table 39 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Power Dissipation	P_{DISS}	CC	–	–	1	W	V_{DDP} = 3.6 V, T_J = 150 °C
Wake-up time from Sleep to Active mode	t_{SSA}	CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode			–	–	–	ms	Defined by the wake-up of the Flash module, see **Section 3.2.11**
Wake-up time from Hibernate mode			–	–	–	ms	Wake-up via power-on reset event, see **Section 3.3.2**

1) CPU executing code from Flash, all peripherals idle.
2) CPU executing code from Flash. Ethernet, USB and CCU clock off.
3) CPU in sleep, all peripherals idle, Flash in Active mode.
4) CPU in sleep, Flash in Active mode.
5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
6) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
7) OSC_ULP operating with external crystal on RTC_XTAL
8) OSC_ULP off, Hibernate domain operating with OSC_SI clock
9) Test Power Loop: f_{SYS} = 120 MHz, CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.
   The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
10) I_{DDP} decreases typically by 5 mA when f_{SYS} decreases by 10 MHz, at constant T_J
11) Sum of currents of all active converters (ADC and DAC)

Peripheral Idle Currents

Test conditions:

- f_{sys} and derived clocks at 120 MHz
- V_{DDP} = 3.3 V, T_a =25 °C
- all peripherals are held in reset (see the PRSTAT registers in the Reset Control Unit of the SCU)
- the peripheral clocks are disabled (see CGATSTAT registers in the Clock Control Unit of the SCU
- no I/O activity
- the given values are a result of differential measurements with asserted and deasserted peripheral reset and enabled clock of the peripheral under test

The tested peripheral is left in the state after the peripheral reset is deasserted, no further initialisation or configuration is done. E.g. no timer is running in the CCUs, no communication active in the USICs, etc.

Table 40 Peripheral Idle Currents

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PORTS ETH USB FCE WDT POSIFx	I_{PER} CC	–	≤ 0.3	–	mA	
MultiCAN ERU LEDTSCU0 CCU4x CCU8x		–	≤ 1.0	–		
DAC (digital)[1)]		–	1.3	–		
USICx		–	3.0	–		
DSD VADC (digital)[1)]		–	4.5	–		
DMAx		–	6.0	–		

1) The current consumption of the analog components are given in the dedicated Data Sheet sections of the respective peripheral.

3.2.11 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 41 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	t_{ERP} CC	–	5	5.5	s	
Erase Time per 64 Kbyte Sector	t_{ERP} CC	–	1.2	1.4	s	
Erase Time per 16 Kbyte Logical Sector	t_{ERP} CC	–	0.3	0.4	s	
Program time per page[1)]	t_{PRP} CC	–	5.5	11	ms	
Erase suspend delay	t_{FL_ErSusp} CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	µs	
Wake-up time	t_{WU} CC	–	–	270	µs	
Read access time	t_a CC	20	–	–	ns	For operation with $1 / f_{CPU} < t_a$ wait states must be configured[2)]
Data Retention Time, Physical Sector[3)4)]	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector[3)4)]	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles

Table 41 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Retention Time, User Configuration Block (UCB)[3)4)]	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	N_{EPS4} CC	10000	–	–	cycles	BA-marking devices only! Cycling distributed over life time[5)]

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.

2) The following formula applies to the wait state configuration: FCON.WSPFLASH × (1 / f_{CPU}) ≥ t_a.

3) Storage and inactive time included.

4) Values given are valid for an average weighted junction temperature of T_J = 110°C.

5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

3.3 AC Parameters

3.3.1 Testing Waveforms

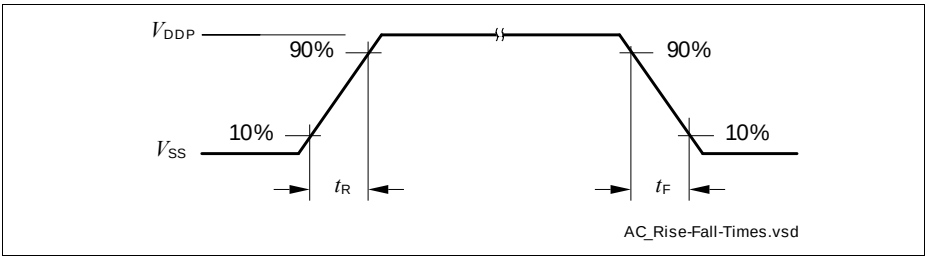

Figure 23 Rise/Fall Time Parameters

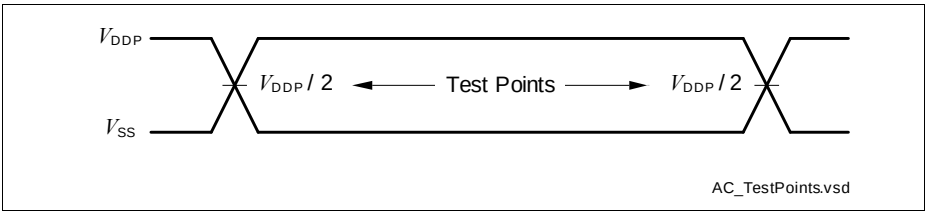

Figure 24 Testing Waveform, Output Delay

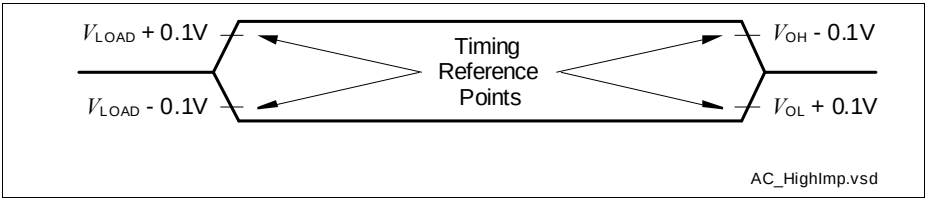

Figure 25 Testing Waveform, Output High Impedance

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

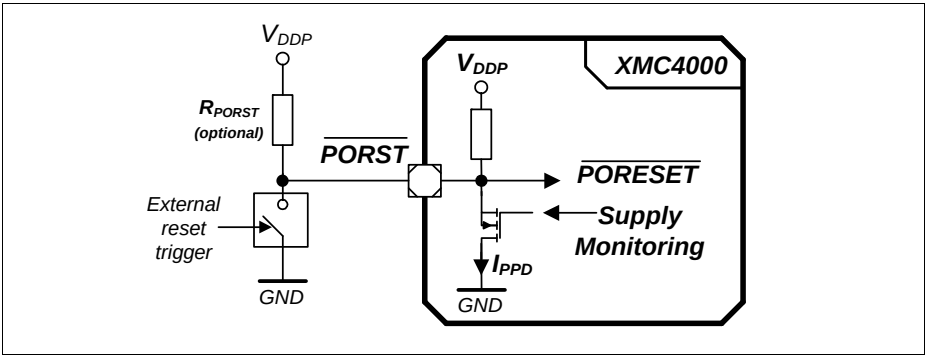

Figure 26 $\overline{\text{PORST}}$ Circuit

Table 42 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79[1]	–	3.05[2]	V	[3]
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	µs	
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	µs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

2) Maximum threshold for reset deassertion.
3) The V_{DDP} monitoring has a typical hysteresis of V_{PORHYS} = 180 mV.

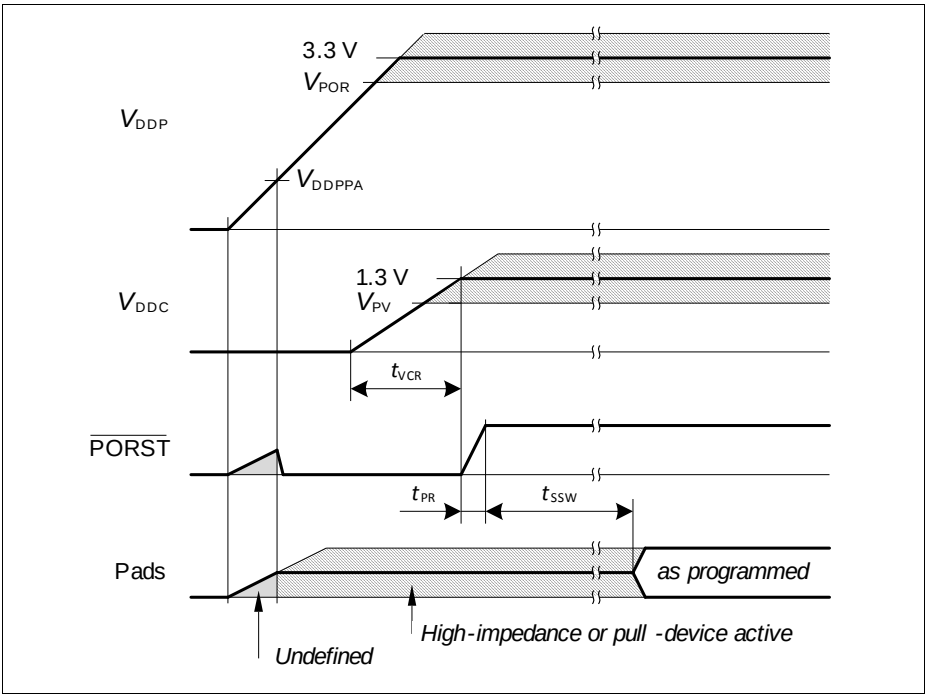

Figure 27 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU}. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 43 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	3	4.7	6	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 120 MHz, main PLL f_{VCO} = 480 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)
24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)
24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

3.3.4 Phase Locked Loop (PLL) Characteristics

Main and USB PLL

Table 44 PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	–	–	±5	ns	accumulated over 300 cycles f_{SYS} = 120 MHz
Duty Cycle[1)]	D_{DC} CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	
VCO input frequency	f_{REF} CC	4	–	16	MHz	
VCO frequency range	f_{VCO} CC	260	–	520	MHz	
PLL lock-in time	t_L CC	–	–	400	µs	

1) 50% for even K2 divider values, 50±(10/K2) for odd K2 divider values.

3.3.5 Internal Clock Source Characteristics

Fast Internal Clock Source

Table 45 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1)2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V ≤ V_{DDP} ≤ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

Slow Internal Clock Source

Table 46 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OSI} CC	–	32.768	–	kHz	
Accuracy	Δf_{OSI} CC	-4	–	4	%	V_{BAT} = const. 0 °C ≤ T_A ≤ 85 °C
		-5	–	5	%	V_{BAT} = const. T_A < 0 °C or T_A > 85 °C
		-5	–	5	%	2.4 V ≤ V_{BAT}, T_A = 25 °C
		-10	–	10	%	1.95 V ≤ V_{BAT} < 2.4 V, T_A = 25 °C
Start-up time	t_{OSIS} CC	–	50	–	µs	

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 47 JTAG Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period	t_1	SR	25	–	–	ns	
TCK high time	t_2	SR	10	–	–	ns	
TCK low time	t_3	SR	10	–	–	ns	
TCK clock rise time	t_4	SR	–	–	4	ns	
TCK clock fall time	t_5	SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6	SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7	SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8	CC	–	–	13	ns	C_L = 50 pF
			3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18}	CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9	CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10}	CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

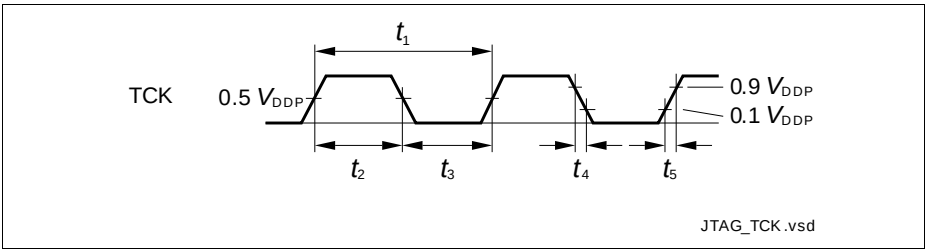

Figure 28 Test Clock Timing (TCK)

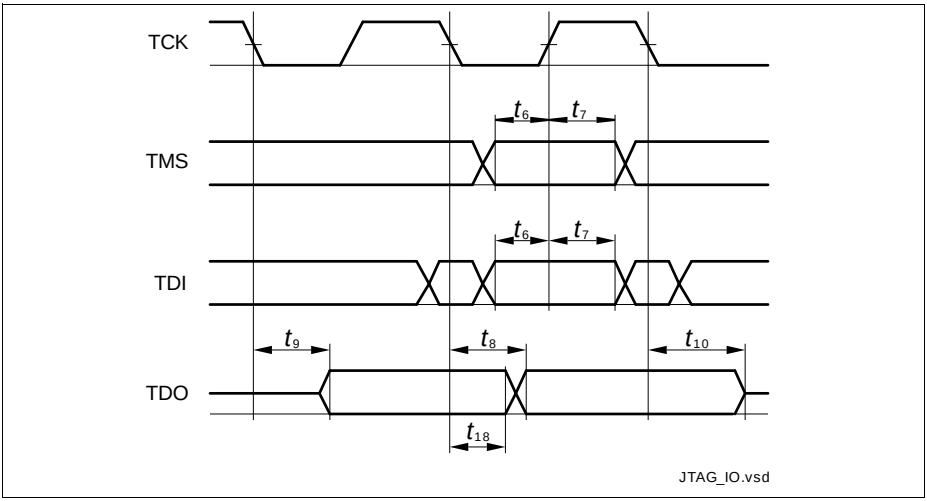

Figure 29 JTAG Timing

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 48 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	t_{SC}	SR	25	–	–	ns	C_L = 30 pF
			40	–	–	ns	C_L = 50 pF
SWDCLK high time	t_1	SR	10	–	500000	ns	
SWDCLK low time	t_2	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	t_5	CC	–	–	17	ns	C_L = 50 pF
			–	–	13	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	CC	3	–	–	ns	

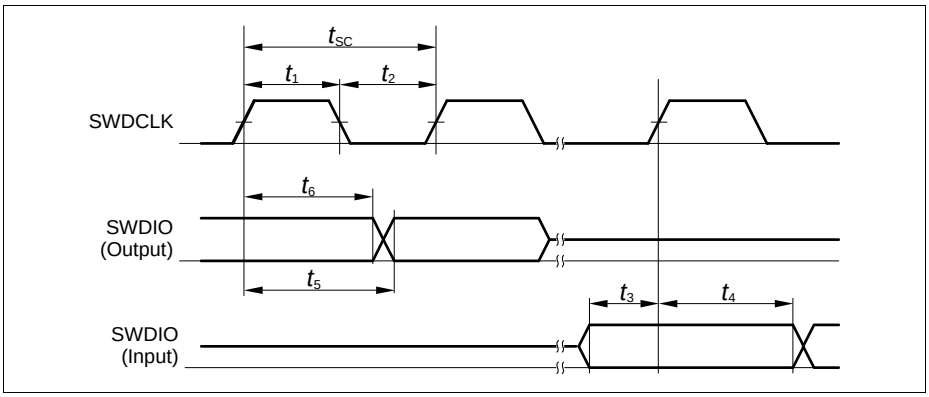

Figure 30 SWD Timing

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The Data timing are to the active clock edge, in half-rate clocking mode that is the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15$ pF.

Table 49 ETM Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TRACECLK period	t_1 CC	16.7	–	–	ns	–
TRACECLK high time	t_2 CC	2	–	–	ns	–
TRACECLK low time	t_3 CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	t_4 CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	t_5 CC	–	–	3	ns	–
TRACEDATA output valid time	t_6 CC	-2	–	3	ns	–

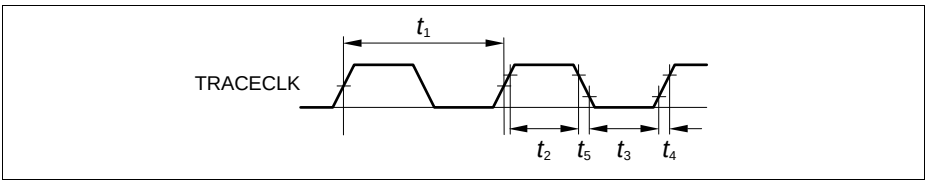

Figure 31 ETM Clock Timing

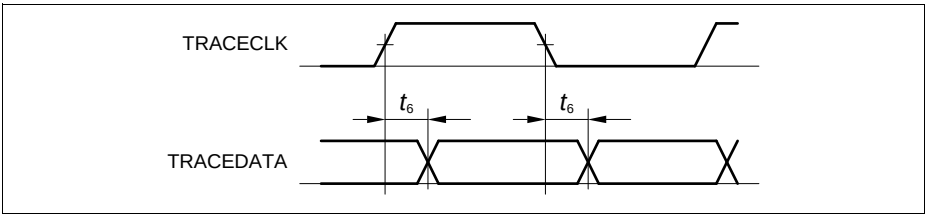

Figure 32 ETM Data Timing

3.3.9 Peripheral Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD).
The data timing is relative to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 50 DSD Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
MCLK period in master mode	t_1	CC	33.3	–	–	ns	$t_1 \geq 4 \times t_{PERIPH}$ [1]
MCLK high time in master mode	t_2	CC	9	–	–	ns	$t_2 > t_{PERIPH}$ [1]
MCLK low time in master mode	t_3	CC	9	–	–	ns	$t_3 > t_{PERIPH}$ [1]
MCLK period in slave mode	t_1	SR	33.3	–	–	ns	$t_1 \geq 4 \times t_{PERIPH}$ [1]
MCLK high time in slave mode	t_2	SR	t_{PERIPH}	–	–	ns	[1]
MCLK low time in slave mode	t_3	SR	t_{PERIPH}	–	–	ns	[1]
DIN input setup time to the active clock edge	t_4	SR	t_{PERIPH} + 4	–	–	ns	[1]
DIN input hold time from the active clock edge	t_5	SR	t_{PERIPH} + 3	–	–	ns	[1]

1) $t_{PERIPH} = 1 / f_{PERIPH}$

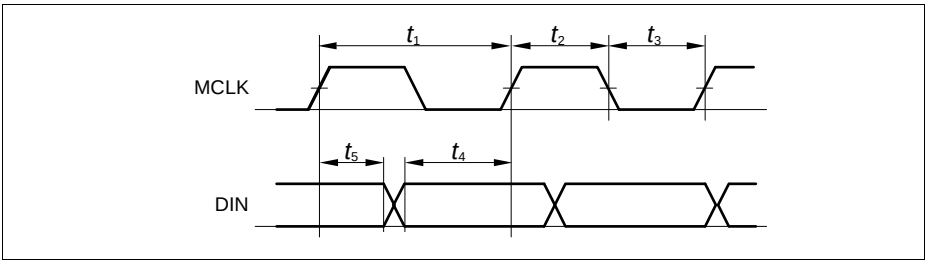

Figure 33 DSD Data Timing

3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 51 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	t_{SYS} - 6.5[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	t_{SYS} - 8.5[1)]	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	1	–	–	ns	

1) $t_{SYS} = 1 / f_{PB}$

Table 52 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10}	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11}	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0	–	24	ns	

1) These input timing are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

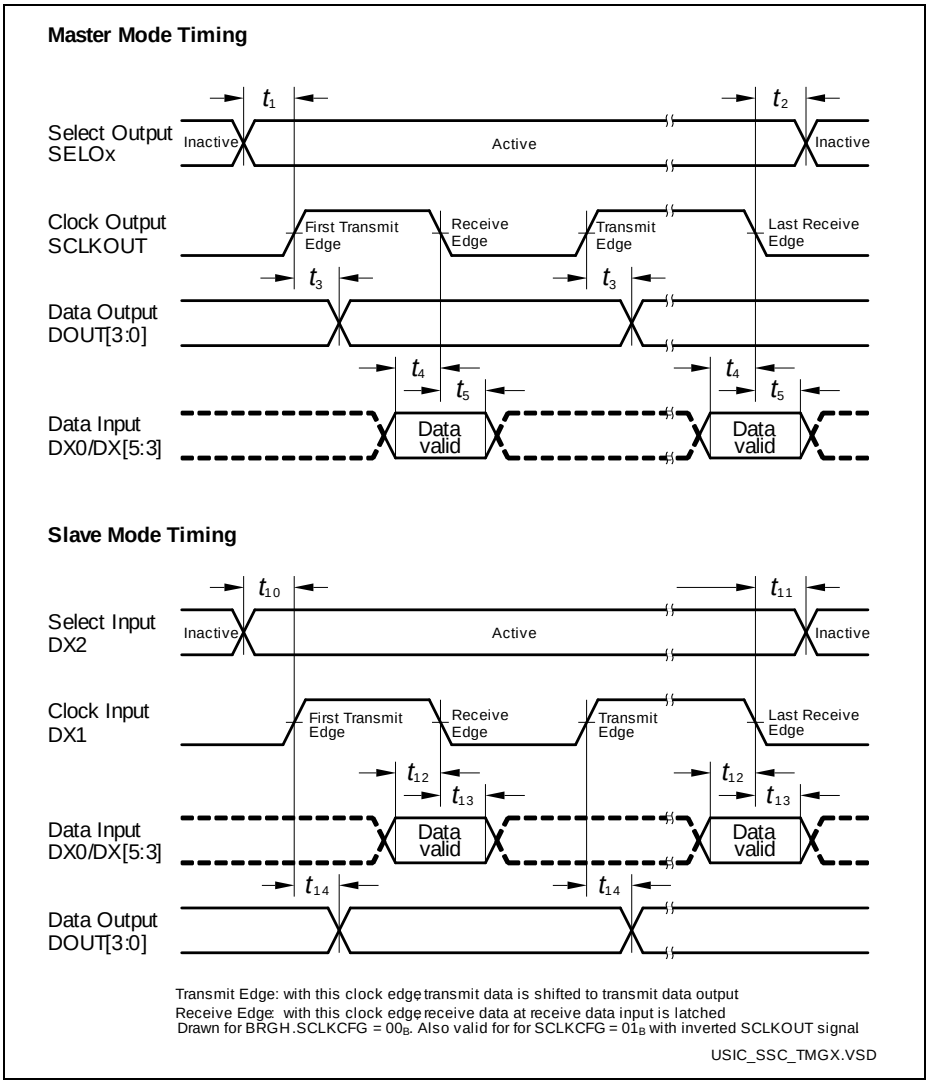

Figure 34 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 53 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 54 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b 2)	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b 2)	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

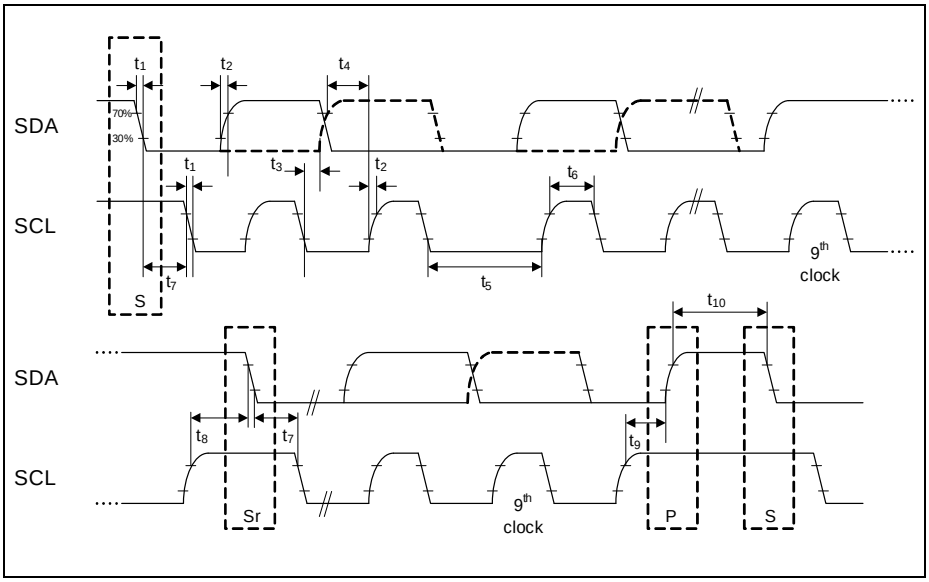

Figure 35 USIC IIC Stand and Fast Mode Timing

3.3.9.4 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 55 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	33.3	–	–	ns	
Clock HIGH	t_2 CC	0.35 x t_{1min}	–	–	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	–	–	ns	
Hold time	t_4 CC	0	–	–	ns	
Clock rise time	t_5 CC	–	–	0.15 x t_{1min}	ns	

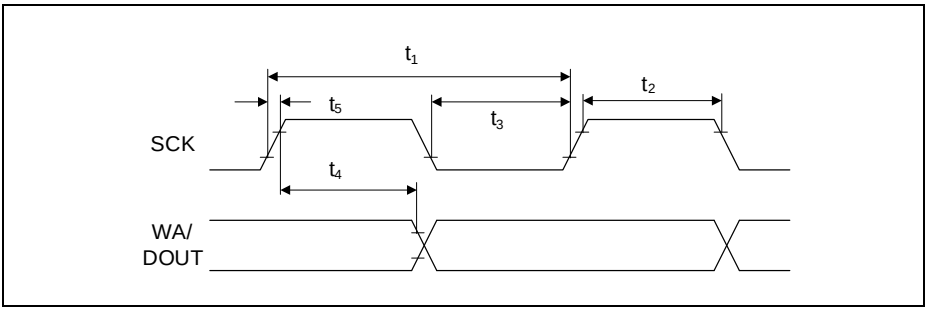

Figure 36 USIC IIS Master Transmitter Timing

Table 56 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	–	–	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	–	–	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	–	–	ns	
Hold time	t_{10} SR	0	–	–	ns	

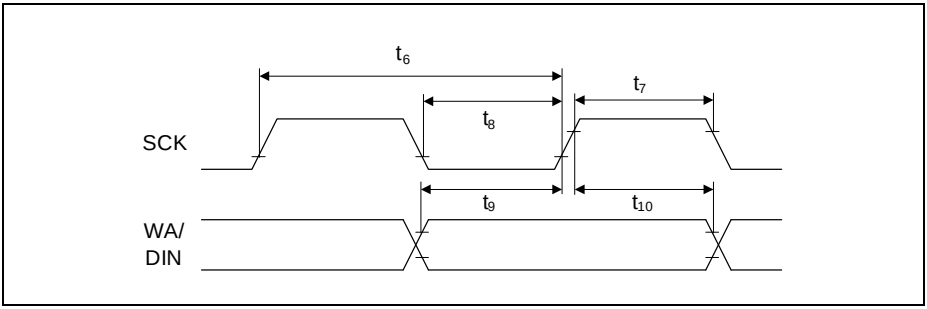

Figure 37 USIC IIS Slave Receiver Timing

3.3.10 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 57 USB Timing Parameters (operating conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Rise time	t_R	CC	4	–	20	ns	C_L = 50 pF
Fall time	t_F	CC	4	–	20	ns	C_L = 50 pF
Rise/Fall time matching	t_R/t_F	CC	90	–	111.11	%	C_L = 50 pF
Crossover voltage	V_{CRS}	CC	1.3	–	2.0	V	C_L = 50 pF

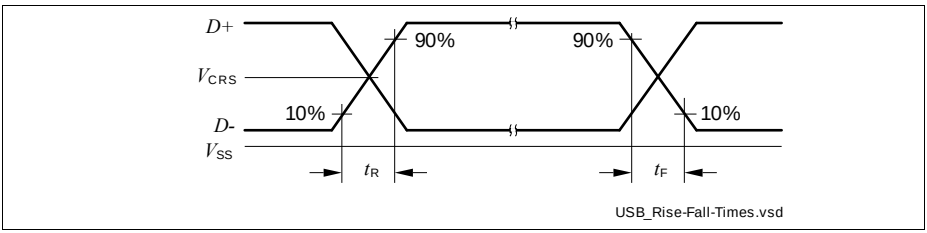

Figure 38 USB Signal Timing

3.3.11 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.11.1 ETH Measurement Reference Points

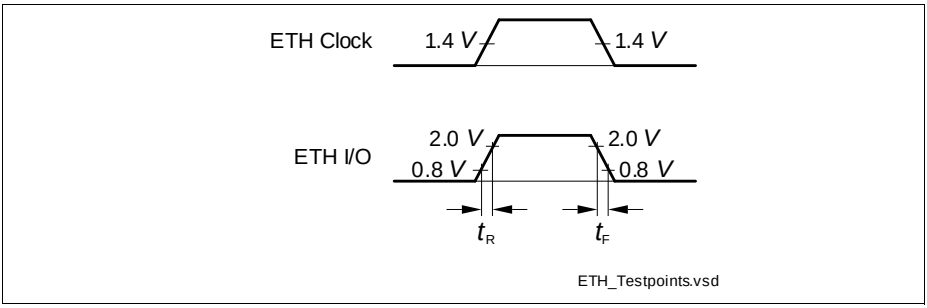

Figure 39 ETH Measurement Reference Points

3.3.11.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 58 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2	CC	160	–	–	ns	
ETH_MDC low time	t_3	CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4	CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5	CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6	SR	0	–	300	ns	

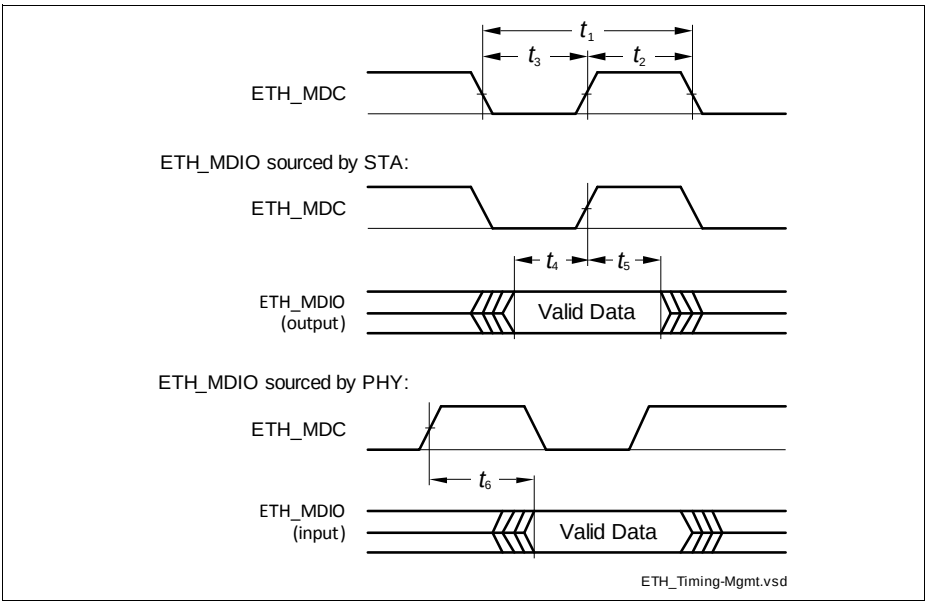

Figure 40 ETH Management Signal Timing

3.3.11.3 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 59 ETH RMII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13}	SR	20	–	–	ns	C_L = 25 pF; 50 ppm
ETH_RMII_REF_CL clock high time	t_{14}	SR	7	–	13	ns	C_L = 25 pF
ETH_RMII_REF_CL clock low time	t_{15}	SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time	t_{16}	SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time	t_{17}	SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18}	CC	4	–	15	ns	

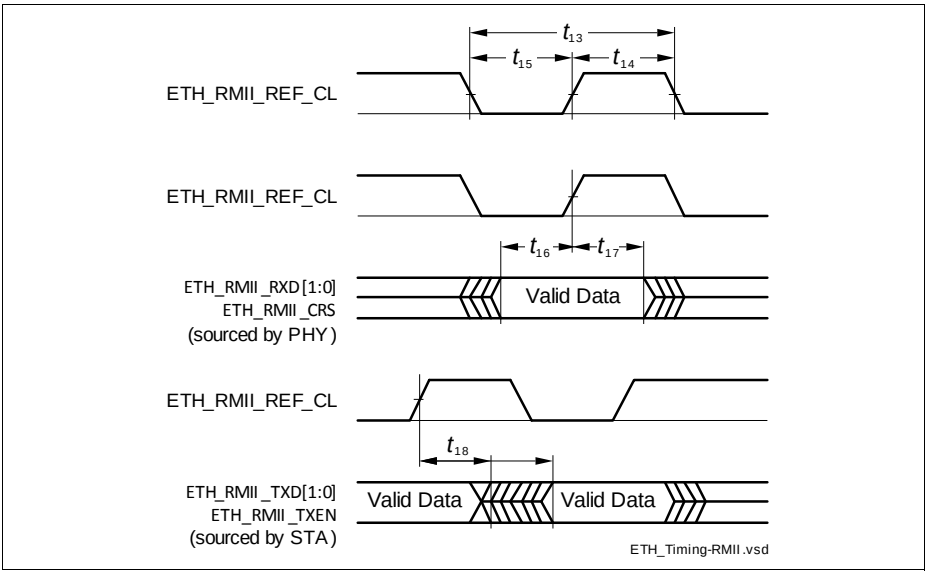

Figure 41 ETH RMII Signal Timing

4 Package and Reliability

The XMC4400 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 60 provides the thermal characteristics of the packages used in XMC4400.

Table 60 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad dimensions (including U-Groove where applicable)	Ex × Ey CC	-	7.0 × 7.0	mm	PG-LQFP-100-11
		-	7.0 × 7.0	mm	PG-LQFP-100-25
		-	5.8 × 5.8	mm	PG-LQFP-64-19
		-	5.7 × 5.7	mm	PG-TQFP-64-19
Exposed Die Pad dimensions excluding U-Groove	Ax × Ay CC	-	6.2 × 6.2	mm	PG-LQFP-100-25
Thermal resistance Junction-Ambient $T_J \leq 150$ °C	$R_{\Theta JA}$ CC	-	20.5	K/W	PG-LQFP-100-11[1)]
		-	20.0	K/W	PG-LQFP-100-25[1)]
		-	30.0	K/W	PG-LQFP-64-19[1)]
		-	22.5	K/W	PG-TQFP-64-19[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4400 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

The availability of different packages for different devices types is listed in **Table 1**, specific packages for different device markings are listed in **Table 2**.

The exposed die pad dimensions are listed in **Table 60**.

Table 61 Differences PG-LQFP-100-11 to PG-LQFP-100-24

Change	PG-LQFP-100-11	PG-LQFP-100-25
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	20.5 K/W	20.0 K/W
Lead Width	$0.22^{\pm 0.05}$ mm	$0.2^{+0.07}_{-0.03}$ mm
Lead Thickness	$0.15^{+0.05}_{-0.06}$ mm	$0.127^{+0.073}_{-0.037}$ mm
Exposed Die Pad outer dimensions	7.0 mm × 7.0 mm	7.0 mm × 7.0 mm
Exposed Die Pad U-Groove inner dimensions	n.a.	6.2 mm × 6.2 mm

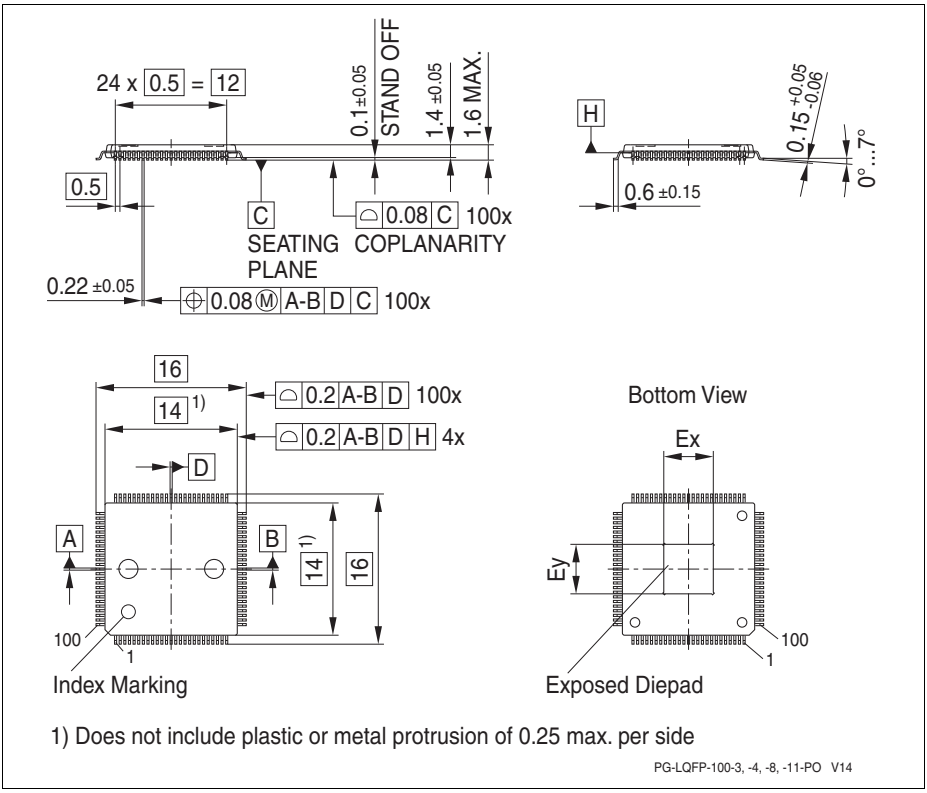

Figure 42 PG-LQFP-100-11 (Plastic Green Low Profile Quad Flat Package)

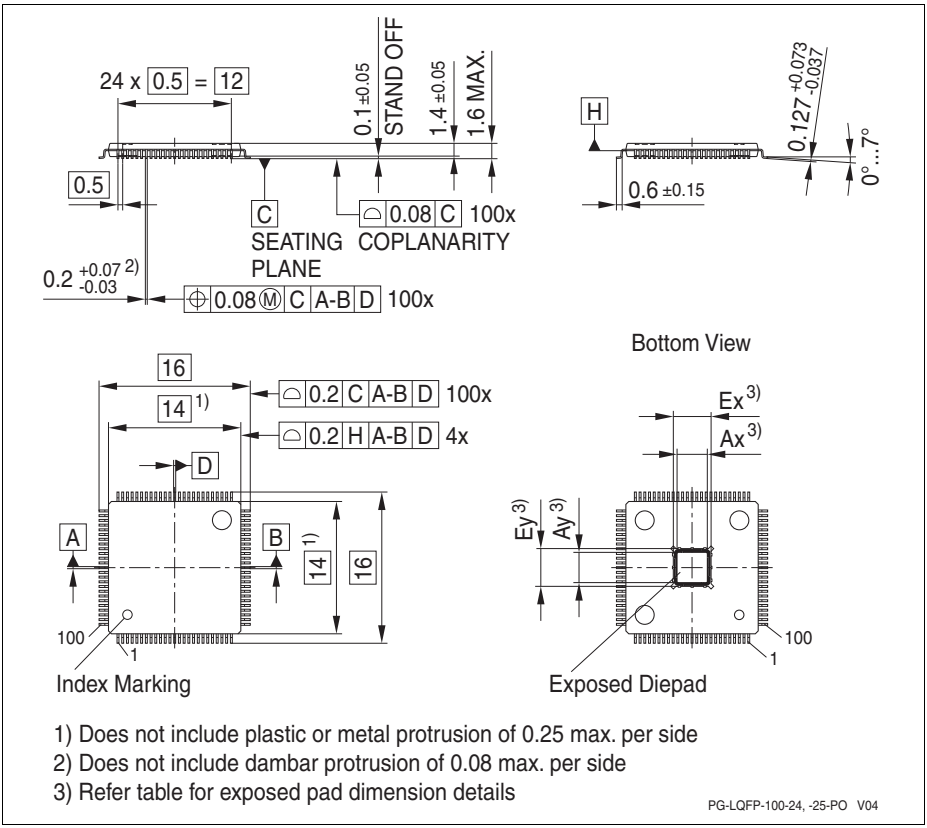

Figure 43 PG-LQFP-100-25 (Plastic Green Low Profile Quad Flat Package)

Table 62 Differences PG-LQFP-64-19 to PG-TQFP-64-19

Change	PG-LQFP-64-19	PG-TQFP-64-19
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	30.0 K/W	22.5 K/W
Package thickness	$1.4^{\pm 0.05}$ mm	$1.0^{\pm 0.05}$ mm
	1.6 mm MAX	1.2 mm MAX
Lead Width	$0.22^{\pm 0.05}$ mm	$0.2^{+0.07}_{-0.03}$ mm
Lead Thickness	$0.15^{+0.05}_{-0.06}$ mm	$0.127^{+0.07}_{-0.04}$ mm
Exposed Die Pad outer dimensions	5.8 mm × 5.8 mm	5.7 mm × 5.7 mm
Exposed Die Pad U-Groove inner dimensions	n.a.	4.9 mm × 4.9 mm

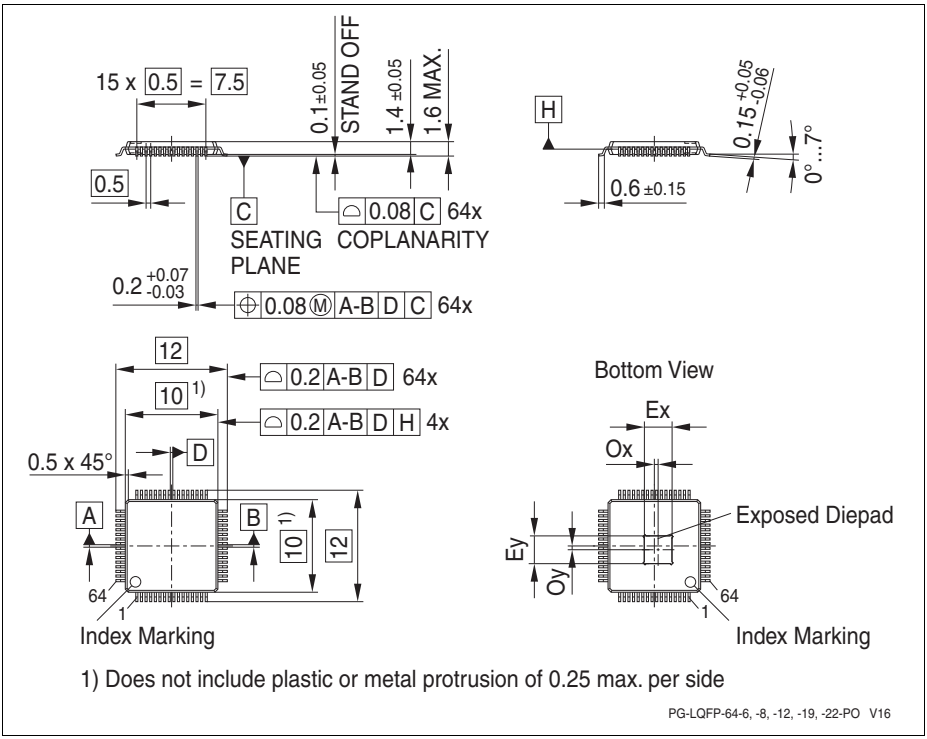

Figure 44 PG-LQFP-64-19 (Plastic Green Low Profile Quad Flat Package)

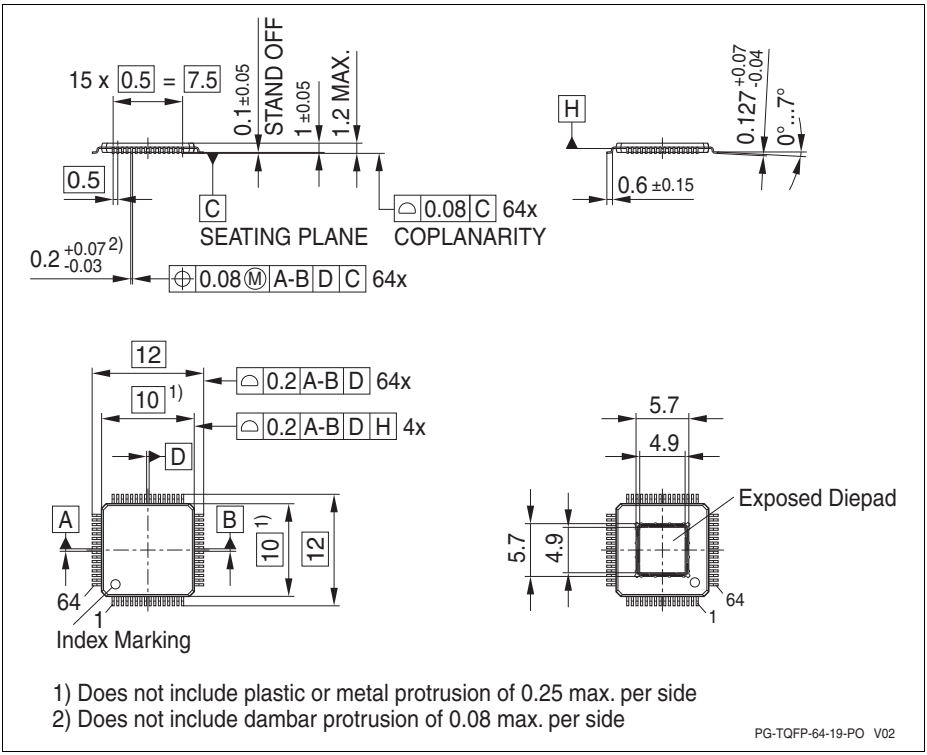

Figure 45 PG-TQFP-64-19 (Plastic Green Low Profile Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**

5 Quality Declarations

The qualification of the XMC4400 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 63 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D

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