EZ-PD™ PMG1-S1 Power Delivery MCU

EZ-PD™ PMG1 family general description

EZ-PD™ PMG1 (Power Delivery Microcontroller Gen1) is a family of high-voltage USB-C Power Delivery (PD) microcontrollers (MCU). These chips include an Arm® Cortex®-M0/M0+ CPU and USB-C PD controller along with analog and digital peripherals. EZ-PD™ PMG1 is targeted for any embedded system that provides/consumes power to/from a high-voltage USB-C PD port and leverages the microcontroller to provide additional control capability. **Figure 1** illustrates the EZ-PD™ PMG1 family segmentation.

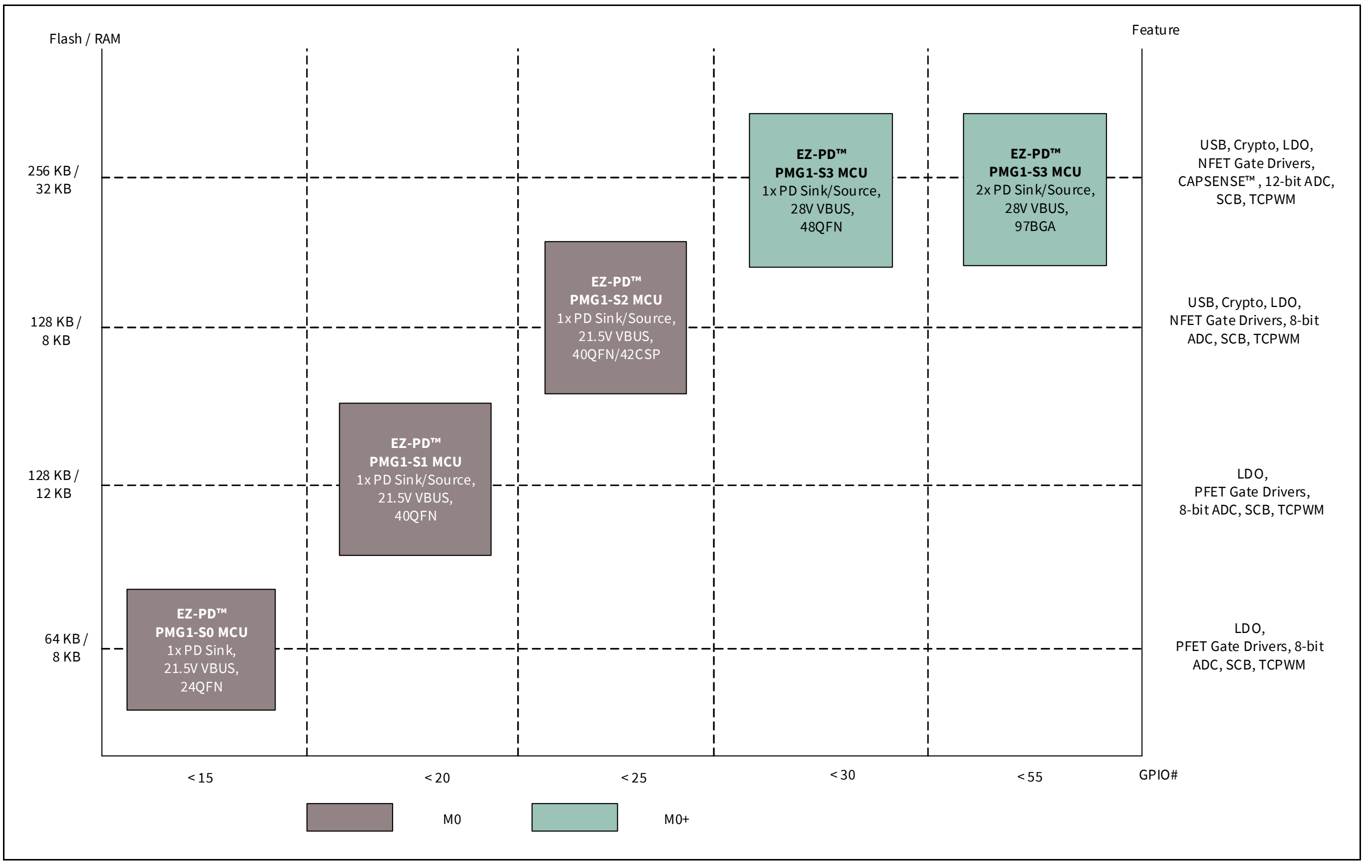

Figure 1 EZ-PD™ PMG1 family segmentation

Table 1 shows the comparison of features of different MCUs of the EZ-PD™ PMG1 family.

Table 1 Comparison of features of different MCUs of the EZ-PD™ PMG1 family

Subsystem or range	Item	EZ-PD™ PMG1-S0	EZ-PD™ PMG1-S1	EZ-PD™ PMG1-S2	EZ-PD™ PMG1-S3
CPU and Memory Subsystem	Core	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0+
	Max Freq (MHz)	48	48	48	48
	Flash (KB)	64	128	128	256
	SRAM (KB)	8	12	8	32
Power Delivery	Power Delivery Ports	1	1	1	1 port for 48-QFN 2 ports for 97-BGA
	Role	Sink	DRP	DRP	DRP
	MOSFET Gate Drivers	2x PFET	2x PFET	2x NFET	Flexible 2x NFET
	Fault Protections	VBUS OVP and UVP	VBUS OVP, UVP, and OCP. SCP and RCP (for Source Configuration only).	VBUS OVP, UVP, and OCP	VBUS OVP, UVP, and OCP. SCP and RCP (for Source Configuration only).
USB	Integrated Full Speed USB 2.0 Device with Billboard Class Support	No	No	Yes	Yes
Voltage Range	Supply (V)	VDDD (2.7–5.5) VBUS (4–21.5)	VSYS (2.75–5.5) VBUS (4–21.5)	VSYS (2.7–5.5) VBUS (4–21.5)	VSYS (2.8–5.5) VBUS (4–28)
	IO (V)	1.71–5.5	1.71–5.5	1.71–5.5	1.71–5.5
Digital	SCB (configurable as I2C/UART/SPI)	2	4	4	7 for 48-QFN (out of which only 5 can be configured as SPI and UART) 8 for 97-BGA
	TCPWM Block (configurable as timer, counter or pulse-width modulator)	4	2	4	7 for 48-QFN 8 for 97-BGA
	Hardware Authentication Block (Crypto)	No	No	Yes (AES-128/192/256, SHA1, SHA2-224, SHA2-256, PRNG, CRC)	Yes (AES-128, SHA2-256, TRNG, Vector Unit)
Analog	ADC	2x 8-bit SAR	1x 8-bit SAR	2x 8-bit SAR	2x 8-bit SAR 1x 12-bit SAR
	On-chip Temperature Sensor	Yes	Yes	Yes	Yes

Table 1 Comparison of features of different MCUs of the EZ-PD™ PMG1 family *(continued)*

Subsystem or range	Item	EZ-PD™ PMG1-S0	EZ-PD™ PMG1-S1	EZ-PD™ PMG1-S2	EZ-PD™ PMG1-S3
Direct Memory Access (DMA)	DMA	No	No	No	Yes
GPIO	Max # of I/O	12 (10 + 2 Fail-Safe)	17 (15 + 2 Fail-Safe)	20 (18 + 2 Fail-Safe)	26 (24 + 2 Fail-Safe) for 48-QFN 50 (48 + 2 Fail-Safe) for 97-BGA
Charging Standards	Charging Standards	-	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC, AFC and Quick Charge 3.0
	Charging Sink	BC 1.2, Apple Charging (AC)	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC
ESD Protection	ESD Protection	Yes (up to ±8-kV Contact Discharge, up to ±15-kV Air Discharge, human body model (HBM), and charged device model (CDM)	Yes (HBM, CDM)	Yes (up to ± 8-kV Contact Discharge, up to ±15-kV Air Discharge, HBM, CDM)	Yes (HBM and CDM)
Packages	Package Options	24-pin QFN (4 × 4 mm, 0.5 mm pitch)	40-pin QFN (6 × 6 mm, 0.5 mm pitch)	40-pin QFN (6 × 6 mm, 0.5 mm pitch) 42-pin CSP (2.63 × 3.18 mm, 0.4 mm pitch)	48-pin QFN (6 × 6 mm, 0.5 mm pitch) 97-BGA (6 × 6 mm, 0.5 mm and 0.65 mm pitch)

The rest of this document discusses the EZ-PD™ PMG1-S1 device in detail.

EZ-PD™ PMG1-S1 general description

EZ-PD™ PMG1-S1 includes 128-KB flash, a complete Type-C USB PD transceiver with all termination resistors R_P, R_D, and dead battery R_D. It is available in a 40-pin QFN package.

Features

- USB PD
  - Supports latest USB PD 3.0 specification
  - Fast role swap (FRS)
  - Extended data messaging (EDM)
- Type-C
  - Integrated current sources for downstream facing port (DFP)[1] role (R_P).
    - Default current at 500 / 900 mA
    - 1.5 A
    - 3 A
  - Integrated R_D resistor for UFP[2] role
  - Integrated VCONN FETs to power EMCA cables
  - Integrated dead battery termination
  - Integrated high-voltage protection on CC and SBU pins to protect against accidental shorts to the VBUS pin on the Type-C connector
- Legacy charging (source and sink)
  - BCv1.2
  - Apple
- Mux
  - Integrated USB2.0 analog mux for USB 2.0 high-speed (HS) data
  - Integrated SBU analog Mux for alternate modes (Display port)
- Integrated VBUS load switch controller
  - Supports up to 20 V on VBUS provider path
  - Slew rate controlled gate driver, tolerant to 24 V, to drive external VBUS PFET on the provider path
  - Gate Driver, tolerant to 24 V, to drive external VBUS PFET on the consumer path
  - Configurable hardware-controlled VBUS overvoltage protection (OVP), undervoltage protection (UVP), over-current protection (OCP), short circuit protection (SCP), and reverse current protection (RCP)
  - VBUS high-side current sense amplifier capable of measuring current across 5-mΩ series resistance
  - In response to FRS request, turns off consumer PFET and turns on provider PFET
- LDO
  - Integrated high-voltage LDO operational up to 21.5 V for dead battery mode operation
- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex® -M0 CPU
  - 128-KB Flash
  - 12-KB SRAM
- Integrated digital blocks
  - Two integrated timers and counters to meet response times required by the USB PD protocol
  - Four run-time serial communication blocks (SCBs) with reconfigurable I^2C, SPI, or UART functionality

Notes
1. DFP refers to power source.
2. UFP refers to power sink.

- Clocks and oscillators
  - Integrated oscillator eliminating the need for an external clock
- Operating range
  - VSYS (2.75 V–5.5 V)
  - VBUS (4 V–21.5 V)
- Hot-swappable I/Os
  - I^2C pins from SCB0 are hot-swappable
- Packages
  - 6.0 mm × 6.0 mm, 0.5 mm, 40-pin QFN
  - Supports industrial temperature range (–40°C to +85°C)

Block diagram

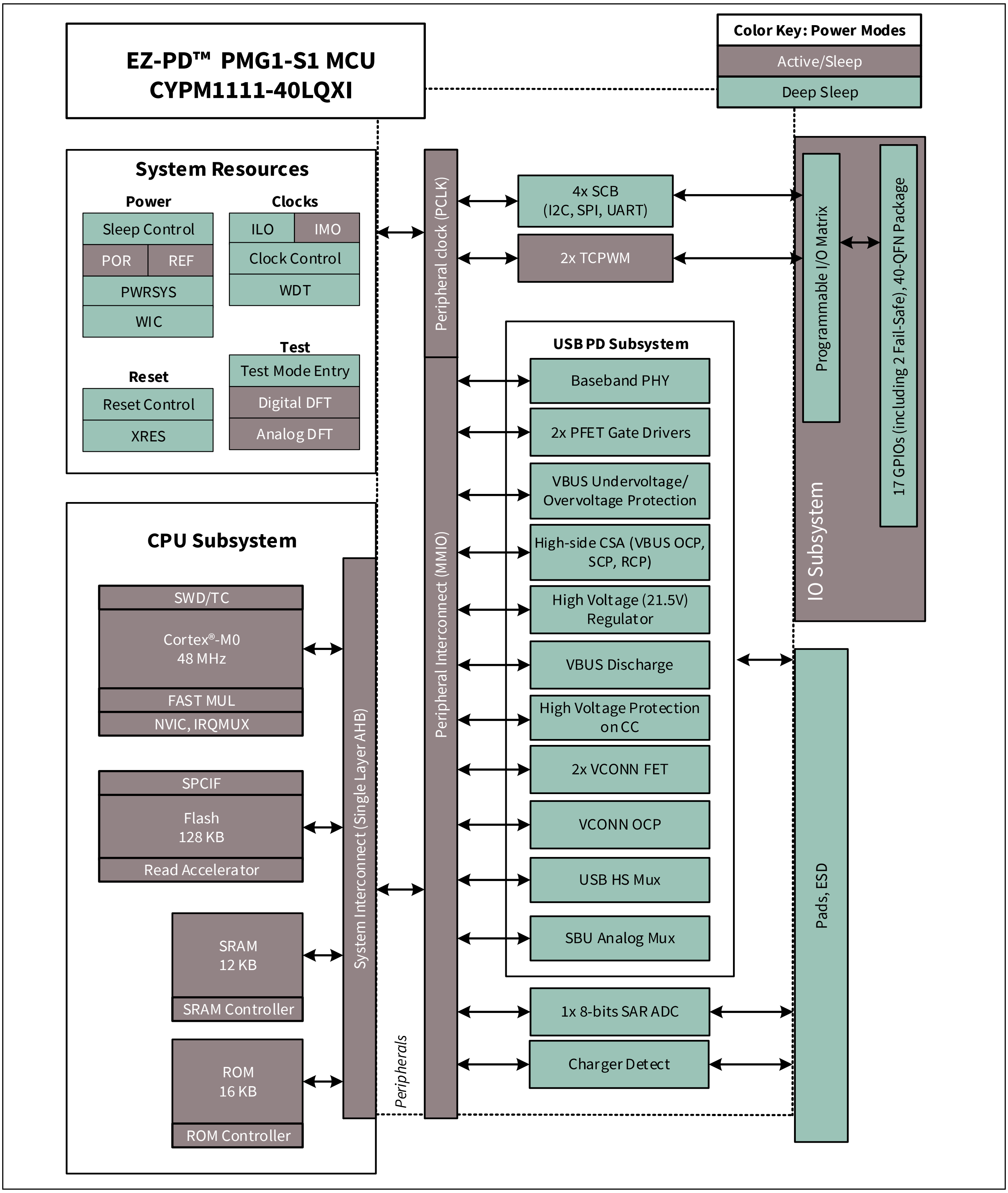

Table of contents

1 Development support

The EZ-PD™ PMG1 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit **EZ-PD™ PMG1 MCU** webpage to find out more.

1.1 Documentation

A suite of documentation supports the EZ-PD™ PMG1 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software user guide: A step-by-step guide for using ModusToolbox™ software. The software user guide shows you how ModusToolbox™ software build process works in detail, how to use source control with ModusToolbox™ software, and much more.

Component datasheets: The flexibility of EZ-PD™ PMG1 allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all the information needed to select and use a particular component, including functional description, API documentation, example codes, and AC/DC specifications.

Application notes: This includes the getting started application note and the hardware design guidelines.

Technical reference manual: The technical reference manual (TRM) contains all the technical detail you need to use a EZ-PD™ PMG1 device, including a complete description of all EZ-PD™ PMG1 registers. The TRM is available in the Documentation section at **EZ-PD™ PMG1 MCU** webpage.

1.2 Online

In addition to print documentation, the **EZ-PD™ PMG1 MCU forums** connect you with fellow users and experts in EZ-PD™ PMG1 from around the world, 24 hours a day, 7 days a week.

1.3 Tools

With industry standard cores, programming, and debugging interfaces, the EZ-PD™ PMG1 MCU family is part of a development tool ecosystem.

Visit us at **ModusToolbox™ software** for the latest information on the revolutionary, easy to use Eclipse IDE for ModusToolbox™ , supported third party compilers, programmers, debuggers, and development kits.

1.4 Eclipse IDE for ModusToolbox™

ModusToolbox™ software is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the Eclipse IDE for ModusToolbox™. The Eclipse IDE for ModusToolbox™ brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox™, you can enable and configure device resources and middleware libraries, write C/C++/assembly source code, and program and debug the device.

For additional details on using the Infineon tools, refer to **AN232553 - Getting started with EZ-PD™ PMG1 MCU on ModusToolbox™ software** and the documentation and help integrated into ModusToolbox™ software. As **Figure 2** shows, with the Eclipse IDE for ModusToolbox™, you can:

1. Create a new application based on a list of template applications, filtered by kit or device, or browse the collection of code examples online.
2. Configure device resources in Device Configurator to build your hardware system design in the workspace.
3. Add software components or middleware.
4. Develop your application firmware.

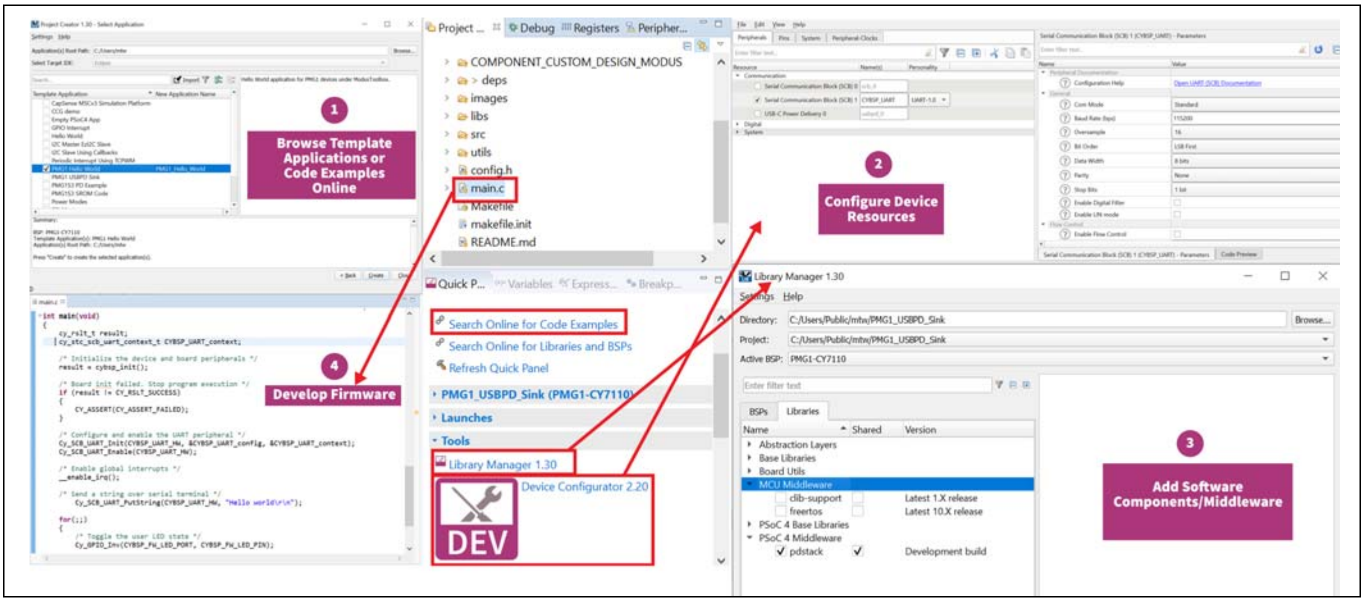

Figure 2 Eclipse IDE for ModusToolbox™ and middleware

2 Functional overview

2.1 USB PD subsystem (SS)

2.1.1 USB PD physical layer

The EZ-PD™ PMG1-S1 USB PD subsystem, as shown in **Figure 3**, consists of the USBPD physical layer (PHY) block and supporting circuits. The PHY consists of a transmitter and receiver that communicates using BMC and 4b/5b encoded/decoded data over the CC channel based on the PD 3.0 specification. All communication is half-duplex. The PHY practices collision avoidance to minimize communication errors on the channel.

In addition, the EZ-PD™ PMG1-S1 USBPD block includes all termination resistors (R_P and R_D) and their switches as required by the USB Type-C specification. R_P and R_D resistors are required for connection detection, plug orientation detection, and for establishing the USB source/sink roles.

The integrated R_P resistor enables EZ-PD™ PMG1-S1 to be configured as a Source. The R_P resistor is implemented as a current source and can be programmed to support the complete range of current capacity on the VBUS defined in the USB Type-C spec.

The R_D resistor is used to identify EZ-PD™ PMG1-S1 as a sink in a dual role power (DRP) application. The dead battery R_D resistor on CC pins is required when the part is not powered for dead battery termination detection and charging.

To support the latest USB PD 3.0 specification, EZ-PD™ PMG1-S1 includes fast role swap (FRS). The FRS feature enables externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed.

For more details about FRS, refer to Section 6.3.19 in the **USB PD 3.0 specification**.

EZ-PD™ PMG1-S1 is designed to be fully interoperable with revision 3.0 of the USB Power Delivery specification as well as revision 2.0 of the USB Power Delivery specification.

EZ-PD™ PMG1-S1 supports Extended Messages containing data of up to 260 bytes. The Extended Messages will be larger than expected by the USBPD 2.0 hardware. To accommodate Revision 2.0 based systems, a Chunking mechanism is implemented such that messages are limited to Revision 2.0 sizes unless it is discovered that both systems support longer message lengths.

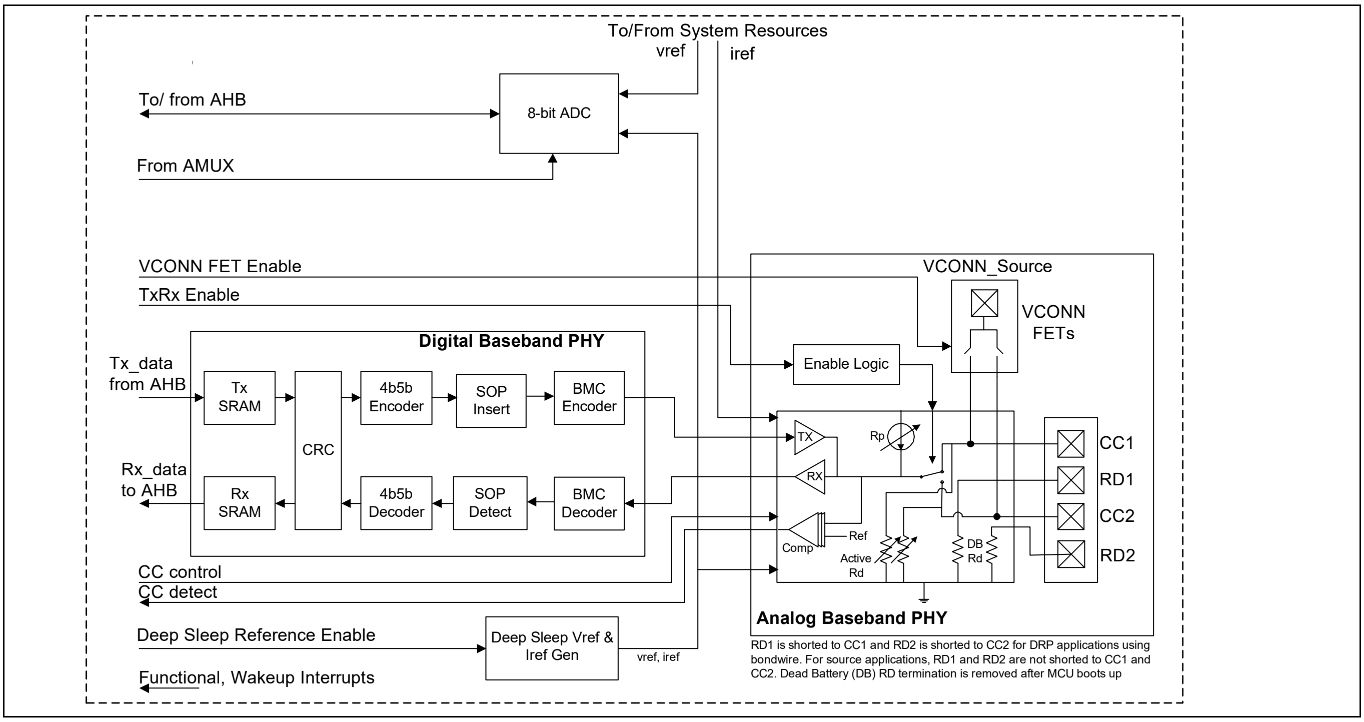

Figure 3 USB PD subsystem

2.1.2 VCONN FET

EZ-PD™ PMG1-S1 has a power supply input, VCONN_Source, for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs to power either CC1 or CC2 pins. These FETs can provide 1.5-W power over VCONN on the CC1 and CC2 pins for the active EMCA cables. EZ-PD™ PMG1-S1 also includes overcurrent protection (OCP) on VCONN.

2.1.3 ADC

The USB PD subsystem contains one 8-bit 125 ksps successive approximation register analog-to-digital converter (SAR ADC). The ADC includes an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex buses, an internal bandgap voltage, and an internal voltage proportional to the absolute temperature. All GPIOs on the chip have access to the ADC through the chip-wide analog mux bus. The CC1 and CC2 pins are not available to connect to the mux bus.

2.1.4 USB 2.0 Mux

The HS mux contains a 2x2 cross bar switch to route the system DP and DM lines to the Type-C top or bottom port based on the CC (Type-C plug) orientation. The unused DPLUS and DMINUS top or bottom lines can be connected to a UART (Debug) port. The maximum operating frequency of UART must be 1 Mbps.

The USB 2.0 mux also contains charger detection/emulation for detecting USB BC1.2 and Apple terminations. The charger detection block is connected to the DP and DM from the system as shown in **Figure 4**.

To meet the HS eye diagram requirements with sufficient margin, follow these guidelines:

- It is recommended to keep the total USB HS signal trace lengths (USB 2.0 host to EZ-PD™ PMG1-S1 + EZ-PD™ PMG1-S1 to Type-C connector pins) to 4 inches.
- Total USB HS signal trace lengths can be increased up to 8 inches by adjusting the drive strength on the USB 2.0 host.
- The differential impedance across the DP/DM signal traces shall be 90 Ω.
- Trace width shall be 6 mils.
- Air Gap (distance between lines) shall be 8 mils.

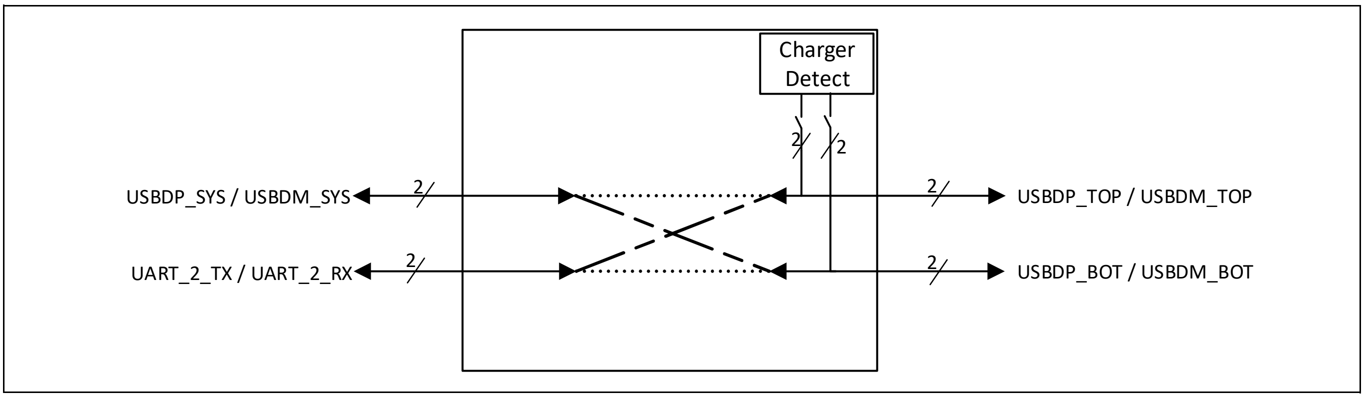

Figure 4 DP/DM switch block diagram

2.1.5 SBU Mux

EZ-PD™ PMG1-S1 integrates SBU 4x2 Mux that enables selection between the Display Port alternate mode and Type-C orientation as shown in **Figure 5**. Type-C facing SBU pins are protected from accidental short to high-voltage VBUS.

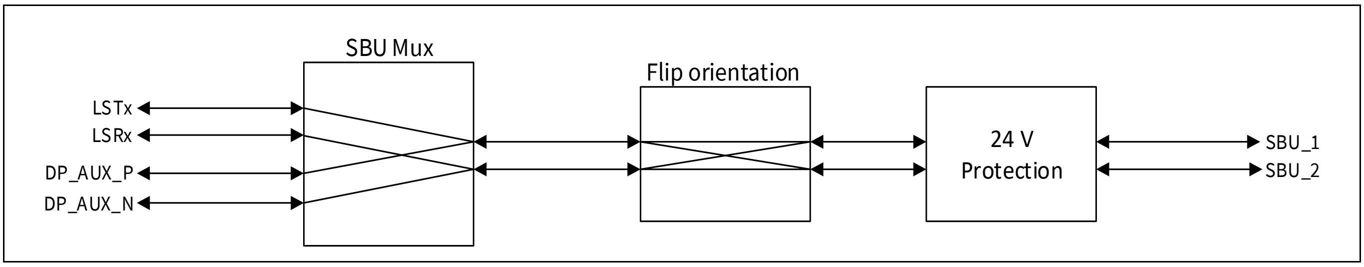

Figure 5 SBU cross bar switch internal block diagram

2.1.6 VBUS discharge

EZ-PD™ PMG1-S1 also has integrated VBUS discharge circuit. It is used to discharge VBUS to meet the USB PD specification timing on a detach condition or negative voltage transition.

2.1.7 VBUS regulator

EZ-PD™ PMG1-S1 can operate from two power supplies – VSYS and VBUS. EZ-PD™ PMG1-S1 integrates the regulator (that supports up to 21.5 V) to derive operating supply voltage. The VSYS always takes priority over VBUS. In the absence of VSYS, the regulator powers EZ-PD™ PMG1-S1 from VBUS.

2.1.8 Gate driver for VBUS PFET on consumer path

EZ-PD™ PMG1-S1 has an integrated PFET gate driver to drive external PFETs on the VBUS consumer path. The gate driver can drive only low or high-Z, thus requiring an external pull-up. This pin is VBUS voltage-tolerant.

2.1.9 Charger detect

EZ-PD™ PMG1-S1 integrates battery charger emulation and detection for USB BC.1.2 and Apple charge.

2.1.10 High-voltage tolerant SBU and CC lines

The chip supports high-voltage tolerant SBU and CC lines. In the case of SBU/CC short to VBUS through connectors, these lines will be protected internally.

2.1.11 VBUS load switch controller for provider path

The load switch controller supports up to 20 V on the VBUS provider path.

2.1.12 RCP

EZ-PD™ PMG1-S1 integrates the RCP circuitry that has the capability of sensing reverse current that lasts for more than 10 µs and protects the system by shutting down the gate automatically upon detection of such events.

EZ-PD™ PMG1-S1 provides RCP circuitry that can detect reverse current flow from connector VBUS_C to provider VBUS_P.

The RCP event is recognized whenever VBUS_C > VBUS_P while provider FET is ON, causing current to flow from connector VBUS to provider VBUS. After recognizing the RCP event, the provider FET is shut down thus isolating the provider and connector VBUS.

EZ-PD™ PMG1-S1 has three distinct mechanisms to detect the reverse current as shown in **Figure 6**.

- Mechanism 1: A comparator senses the voltage drop across external Rsense through pins CSP and CSN. This comparator signals an RCP event whenever CSN > CSP by the Vcsa_rcp voltage given in **Table 34**. The output of this comparator RCP1 is shown in **Figure 6**.
- Mechanism 2: A comparator senses the voltage drop across provider FET through CSN and VBUS pin of EZ-PD™ PMG1-S1. This comparator signals an RCP event whenever VBUS > CSN by the Vcomp_rcp voltage given in **Table 34**. The output of this comparator RCP2 is shown in **Figure 6**.
- Mechanism 3: A comparator senses the 20% voltage of the CSN pin and compares it against Vref = 1.15 V for 5-V provider VBUS application. This comparator signals an RCP event whenever CSN voltage goes above Vbus_-max_det voltage given in **Table 34** for a 5-V application. The output of this comparator RCP3 is shown in **Figure 6**. Note that Vref is programmable and the voltage divider has an option to use 10% or 20% value. For a higher voltage of the provider, the VBUS device automatically adjusts this threshold.

When any one of the three comparator outputs show an RCP event, then the provider FET is turned OFF. The firmware has an option to enable or disable the individual mechanism depending on the application.

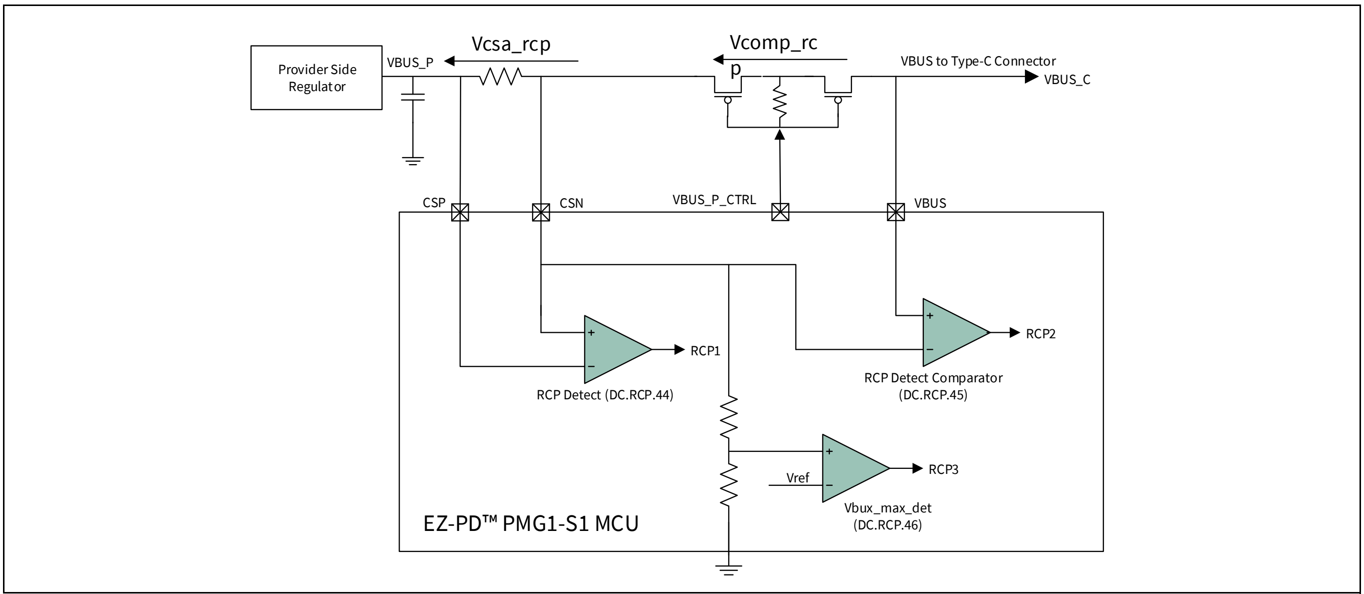

Figure 6 RCP mechanism

2.1.13 CSA

EZ-PD™ PMG1-S1 MCU chip has an integrated high-side current sense amplifier that is capable of detecting current in the order of 100 mA across a 5-mΩ external resistor in the provider path. This is used to monitor the current load and detect system faults such as OCP and SCP while sourcing VBUS to the sink on the Type C port so that the PD controller can shut down the Provider FET to protect devices.

2.1.14 Slew-rate controllable gate driver

EZ-PD™ PMG1-S1 has a programmable slew-rate controllable gate driver, which can help in limiting the in-rush currents during connect events.

2.1.15 OVP and UVP on VBUS

EZ-PD™ PMG1-S1 implements an undervoltage/overvoltage (UVOV) detection circuit for the VBUS supply. The threshold for OV and UV detection can be set independently. Both UV and OV detectors have programmable thresholds and are controlled by the firmware. The inputs to the OV comparator are a division (8% or 10%) of VBUS supply voltage and a reference voltage. The reference voltage is configurable in the range (200 mV to 2190 mV) in steps of 10 mV.

The inputs to the UV comparator are a division (10% or 20%) of VBUS supply voltage and a reference voltage. The reference voltage is configurable in the range (200 mV to 2190 mV) in steps of 10 mV.

2.1.16 OCP on VBUS

EZ-PD™ PMG1-S1 integrates a high-side current sense amplifier to detect overcurrent on the VBUS. The VBUS load is sensed using an external 5-mΩ sense resistor connected between the “CSP” and “CSN” pins and compared against the OCP detector threshold. The OCP detector threshold is programmable and controlled by the firmware.

2.2 CPU and memory subsystem

2.2.1 CPU

The Cortex®-M0 CPU in EZ-PD™ PMG1-S1 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD™ PMG1-S1 has four break-point (address) comparators and two watchpoint (data) comparators.

2.2.2 Flash

The EZ-PD™ PMG1-S1 device has a 128-KB flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait-states (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

2.2.3 SROM

A supervisory ROM that contains boot and configuration routines is provided.

2.2.4 SRAM

EZ-PD™ PMG1-S1 supports 12-KB SRAM.

2.3 Peripherals

EZ-PD™ PMG1-S1 has four SCBs, which can each implement an I^2C, UART, or SPI interface.

I^2C mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I^2C bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes. The I^2C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. The required rise and fall times for different I^2C speeds are guaranteed by using appropriate pull-up resistor values depending on VDDD, bus capacitance, and resistor tolerance.

For detailed information on how to calculate the optimum pull-up resistor value for your design, refer to the UM10204 I^2C bus specification and user manual (the latest revision is available at **www.nxp.com**).

EZ-PD™ PMG1-S1 is not completely compliant with the I^2C spec for the following:

- Only SCB0 is fail-safe. SCB1, SCB2, and SCB3 GPIO cells are not fail-safe because a high logic level on these GPIOs can back-power the MCU. Therefore, PMG1-S1 cannot be powered up independently of the rest of the I^2C system.
- Fast Mode Plus has an IOL specification of 20 mA at a VOL of 0.4 V. The GPIO cells can sink a maximum of 8-mA IOL with a VOL maximum of 0.6 V.
- Fast Mode and Fast Mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.

UART mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

2.4 Timer/counter/PWM block (TCPWM)

EZ-PD™ PMG1-S1 has two TCPWM blocks. Each TCPWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

2.5 GPIO

EZ-PD™ PMG1-S1 has 17 GPIOs that includes the SCB and SWD pins, which can also be used as GPIOs. The GPIO block implements the following:

- Seven drive strength modes
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (6 for EZ-PD™ PMG1-S1 since it has six ports).

2.5.1 Fail-Safe GPIOs

EZ-PD™ PMG1-S1 has two pins (16 and 17) which are fail-safe GPIOs. These are P5.0 and P5.1, which are the I^2C pins for SCB0. The fail-safe feature ensures that, in the absence of VBUS/VSYS power, a logic high level on these pins due to I^2C line activity will not back-power the MCU. Therefore, SCB0 can be used for communication with external controller when PMG1-S1 needs to be independently powered from rest of the I^2C system.

3 Power system overview

Figure 7 provides an overview of the EZ-PD™ PMG1-S1 power system. EZ-PD™ PMG1-S1 can operate from two possible external supply sources: VBUS (4 V to 21.5 V) or VSYS (2.75 V to 5.5 V). The VBUS supply is regulated inside the chip with a LDO. The switched supply, VDDD, is used directly inside some analog blocks and further regulated down to VCCD, which powers majority of the core. EZ-PD™ PMG1-S1 has two different power modes: Active and Deep Sleep. Transitions between these power modes are managed by the power system. A separate power domain, VDDIO, is provided for the GPIOs. The VDDD and VCCD pins, both outputs of regulators, are brought out for connecting a 1-µF and 0.1-µF capacitor respectively for the regulator stability only. The VCCD pin is not supported as a power supply. VDDD can source 2 mA (max) for external load. In EZ-PD™ PMG1-S1, VDDD shall be shorted to VDDIO on PCB.

Table 2 EZ-PD™ PMG1-S1 power modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or Sleep Controller is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
DEEP SLEEP	Main regulator and most blocks are shut off. DeepSleep regulator powers logic, but only the low-frequency clock is available.

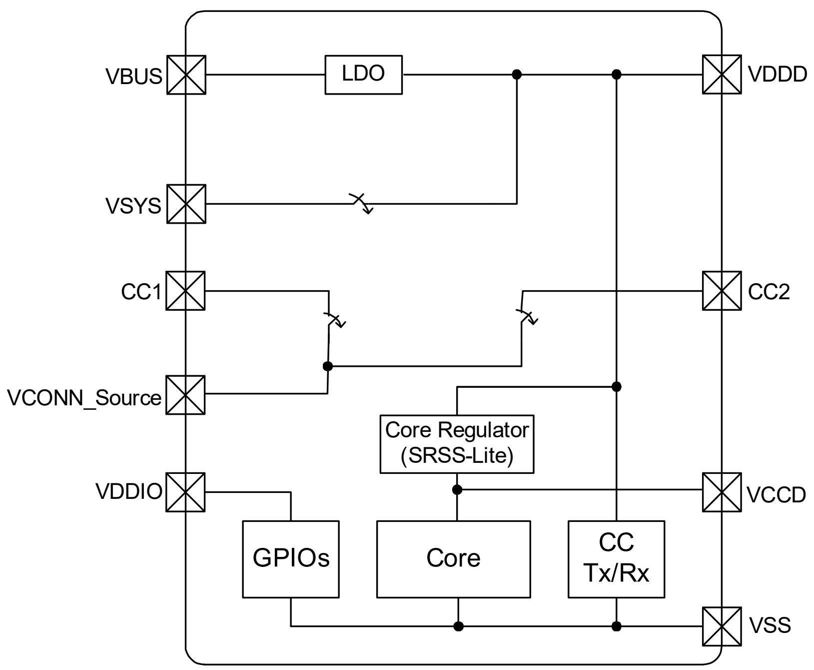

Figure 7 EZ-PD™ PMG1-S1 power system

4 Pinouts

Table 3 Pinout for CYPM1111-40LQXI

Group	40-QFN	Pin name	Alternate functions (HSIOM_PORT_SEL)								Description
			ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1	DS #2	DS #3	
GPIO	2	P1.0			scb1_uart_rx		swd_clk		scb1_spi_select		GPIO, SCB1, serial wire debug clock
	3	P1.1	ext_clk_0		scb1_uart_tx	tcpwm0_overflow			scb1_spi_mosi	scb1_i2c_sda	GPIO, TCPWM0, SCB1, serial wire debug clock, external clock connection
	4	P1.2	tcpwm0_line	tcpwm0_compare_match	scb1_uart_cts				scb1_spi_miso	scb1_i2c_scl	GPIO, TCPWM0, SCB1
	5	P1.3			scb1_uart_rts	tcpwm1_overflow			scb1_spi_clk		GPIO, TCPWM1, SCB1
	6	P1.4	tcpwm1_line	tcpwm1_compare_match			swd_data				GPIO, TCPWM1, serial wire debug data
	13	P2.0			scb3_uart_cts			scb3_spi_select		scb3_i2c_scl	GPIO, SCB3
	14	P2.1			scb3_uart_rts			scb3_spi_mosi		scb3_i2c_sda	GPIO, SCB3
	15	P2.2			scb0_uart_cts			scb0_spi_select			GPIO, SCB0
	18	P3.0			scb0_uart_rx		usbpd_hpd	scb0_spi_clk			GPIO, SCB0, Hot Plug Detect for DisplayPort Alt mode
	20	P3.1			scb2_uart_cts				scb2_spi_select	scb2_i2c_sda	GPIO, SCB2
	21	P3.2			scb2_uart_rts				scb2_spi_mosi	scb2_i2c_scl	GPIO, SCB2
	29	P4.0	ext_clk_1		scb2_uart_tx				scb2_spi_miso		GPIO, SCB2, external clock connection
	30	P4.1			scb2_uart_rx				scb2_spi_clk		GPIO, SCB2
	16	P5.0			scb0_uart_rts		swd_data(alt)	scb0_spi_mosi		scb0_i2c_sda	GPIO, SCB0, serial wire debug data (alternate)
	17	P5.1			scb0_uart_tx		swd_clk(alt)	scb0_spi_miso		scb0_i2c_scl	GPIO, SCB0, serial wire debug clock (alternate)
Reset	10	XRES									Reset input to the MCU
Muxes/ switches	34	SBU_2									GPIO, Type-C auxiliary signal for DisplayPort – connector side
	35	SBU_1									GPIO, Type-C auxiliary signal for DisplayPort – connector side
	36	AUX_P									GPIO, Type-C auxiliary signal for DisplayPort – system side
	37	AUX_N									GPIO, Type-C auxiliary signal for DisplayPort – system side
	38	P0.0/LSTX			scb3_uart_tx			scb3_spi_miso			GPIO, SCB3
	39	P0.1/LSRX			scb3_uart_rx			scb3_spi_clk			GPIO, SCB3

Table 3 **Pinout for CYPM1111-40LQXI** *(continued)*

Group	40-QFN	Pin name	Alternate functions (HSIOM_PORT_SEL)								Description
			ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1	DS #2	DS #3	
USB FS	23	USBDP_SYS									Connection to USB 2.0 DP line of the host/device
	24	USBDM_SYS									Connection to USB 2.0 DM line of the host/device
	25	USBDM_BOT									Connection to Type-C D- bottom pin. Keep trace length less than 2 inch
	26	USBDP_BOT									Connection to Type-C D+ bottom pin. Keep trace length less than 2 inch
	27	USBDM_TOP									Connection to Type-C D- top pin. Keep trace length less than 2 inch
	28	USBDP_TOP									Connection to Type-C D+ top pin. Keep trace length less than 2 inch
USB PD Type-C	9	CC1									Connect to Type-C CC1 pin. Filter noise with 390-pF capacitor to GND
	7	CC2									Connect to Type-C CC2 pin. Filter noise with 390-pF capacitor to GND
VBUS OCP/SCP/RCP	1	CSP									Current Sense Positive input pin. Connect this pin to a higher potential compared to CSN pin
	40	CSN									Current Sense Negative input pin
VBUS PFET control	11	VBUS_P_CTRL									Slew Rate controlled output pin for enable/disable Provider side PFET 0: Path ON, High Z: Path OFF
	12	VBUS_C_CTRL									Output pin to enable/disable Consumer side PFET 0: Path ON, High Z: Path OFF
Power	19	VSYS									Supply input (2.75 V–5.5 V) for PD subsystem and System resources.
	22	VBUS									Supply input (4 V–21.5 V) for VBUS to 3.3-V regulator. This pin also discharges VBUS using internal pull-down and also has monitors for overvoltage and undervoltage conditions.
	8	VCONN_source									4.85-V to 5.5-V supply input to power EMCA cables. Connected to CC1 or CC2 using low impedance switches. NA for UFP/Sink only applications
	31	VDDD									Output of VBUS to 3.3-V regulator or connected to VSYS using switch. Bypass with cap to gnd. This pin can drive 2-mA external load.
	32	VDDIO									1.71 V–5.5 V supply for I/Os
	33	VCCD									1.8-V regulator output for filter capacitor. This pin cannot drive external load
GND	EPAD	VSS									Ground

Table 4 provides the various configuration options for the serial interfaces.

Table 4 SCBs and their functionality

Port	40-pin QFN	SCB function			GPIO functionality
Pin	Pin number	UART	SPI	I2C	
P5.0	16	UART_0_RTS	SPI_0_MOSI	I2C_0_SDA	GPIO
P5.1	17	UART_0_TX	SPI_0_MISO	I2C_0_SCL	GPIO
P3.0	18	UART_0_RX	SPI_0_CLK	–	GPIO
P2.2	15	UART_0_CTS	SPI_0_SEL	–	GPIO
P1.0	2	UART_1_RX	SPI_1_SEL	–	SWD_CLK/GPIO
P1.1	3	UART_1_TX	SPI_1_MOSI	I2C_1_SDA	GPIO
P1.2	4	UART_1_CTS	SPI_1_MISO	I2C_1_SCL	GPIO
P1.3	5	UART_1_RTS	SPI_1_CLK	–	GPIO
P3.1	20	UART_2_CTS	SPI_2_SEL	I2C_2_SDA	GPIO
P3.2	21	UART_2_RTS	SPI_2_MOSI	I2C_2_SCL	GPIO
P4.0	29	UART_2_TX	SPI_2_MISO	–	GPIO
P4.1	30	UART_2_RX	SPI_2_CLK	–	GPIO
P2.0	13	UART_3_CTS	SPI_3_SEL	I2C_3_SCL	GPIO
P2.1	14	UART_3_RTS	SPI_3_MOSI	I2C_3_SDA	GPIO
P0.0	38	UART_3_TX	SPI_3_MISO	–	GPIO
P0.1	39	UART_3_RX	SPI_3_CLK	–	GPIO

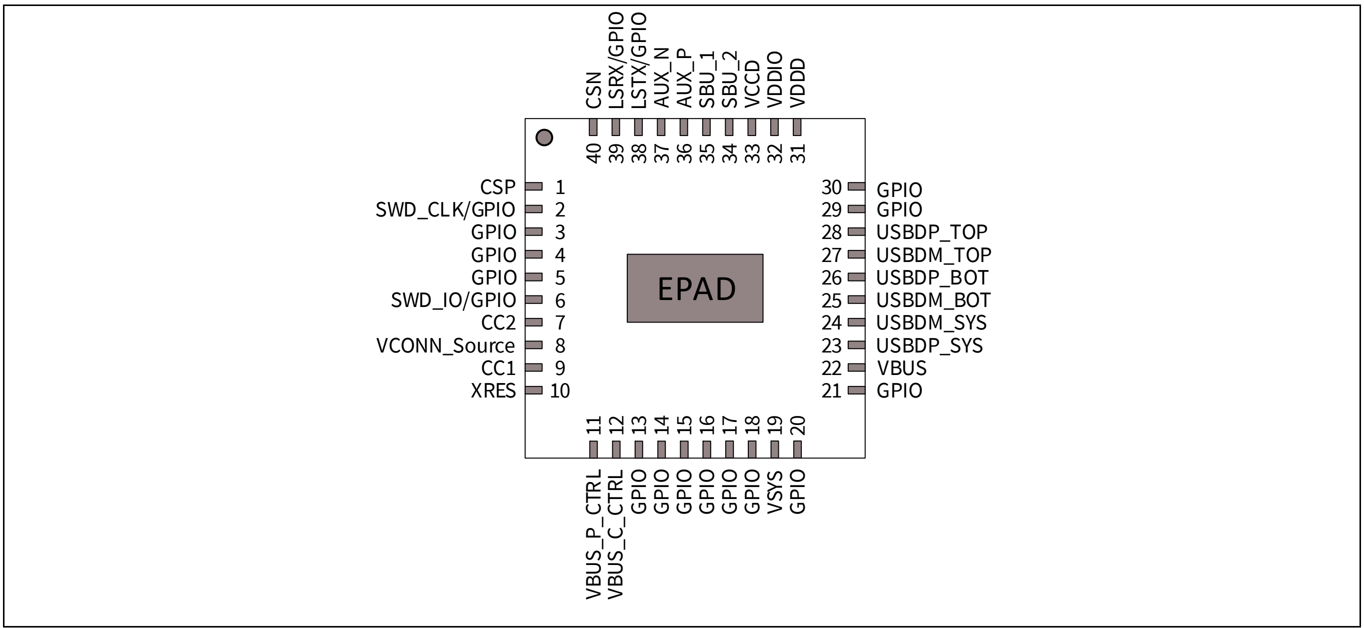

Figure 8 40-pin QFN pin map (top view) for CYPM1111-40LQXI

5 Application diagrams

Figure 9 illustrates a Sink application using EZ-PD™ PMG1-S1. It has two main parts: a USB Type-C receptacle that sinks power to the application and a load used as the output power.

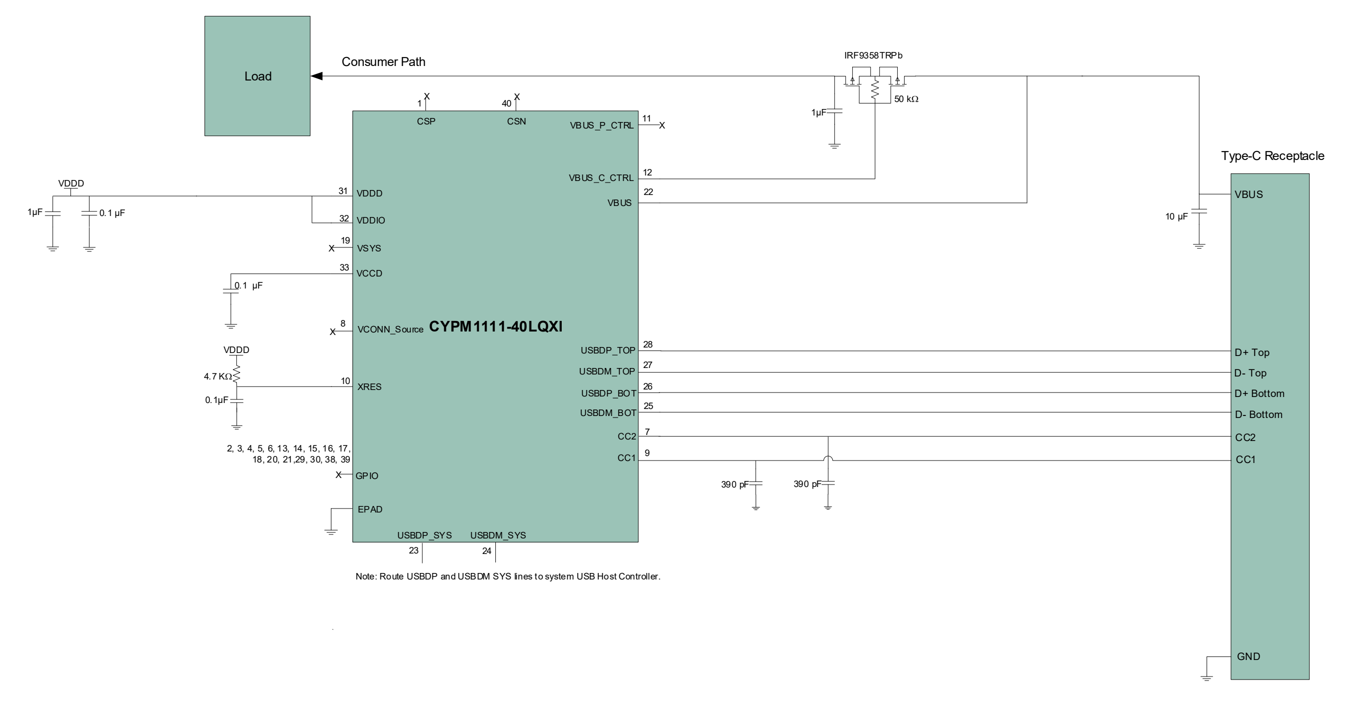

Figure 9 EZ-PD™ PMG1-S1-based sink application diagram

Figure 10 illustrates a DRP application using EZ-PD™ PMG1-S1. In such applications, the Type-C port is used as a power provider and a power consumer. There are VBUS FETs for providing or consuming power over VBUS.

The VBUS pin of EZ-PD™ PMG1-S1 has an in-built VBUS monitoring circuit that can detect OVP and UVP on VBUS. In addition to this, the 5-mΩ resistor between power source and provider FETs can detect overcurrent on the VBUS. The EZ-PD™ PMG1-S1 device also has integrated VCONN FETs for applications that need to provide power for accessories and cables.

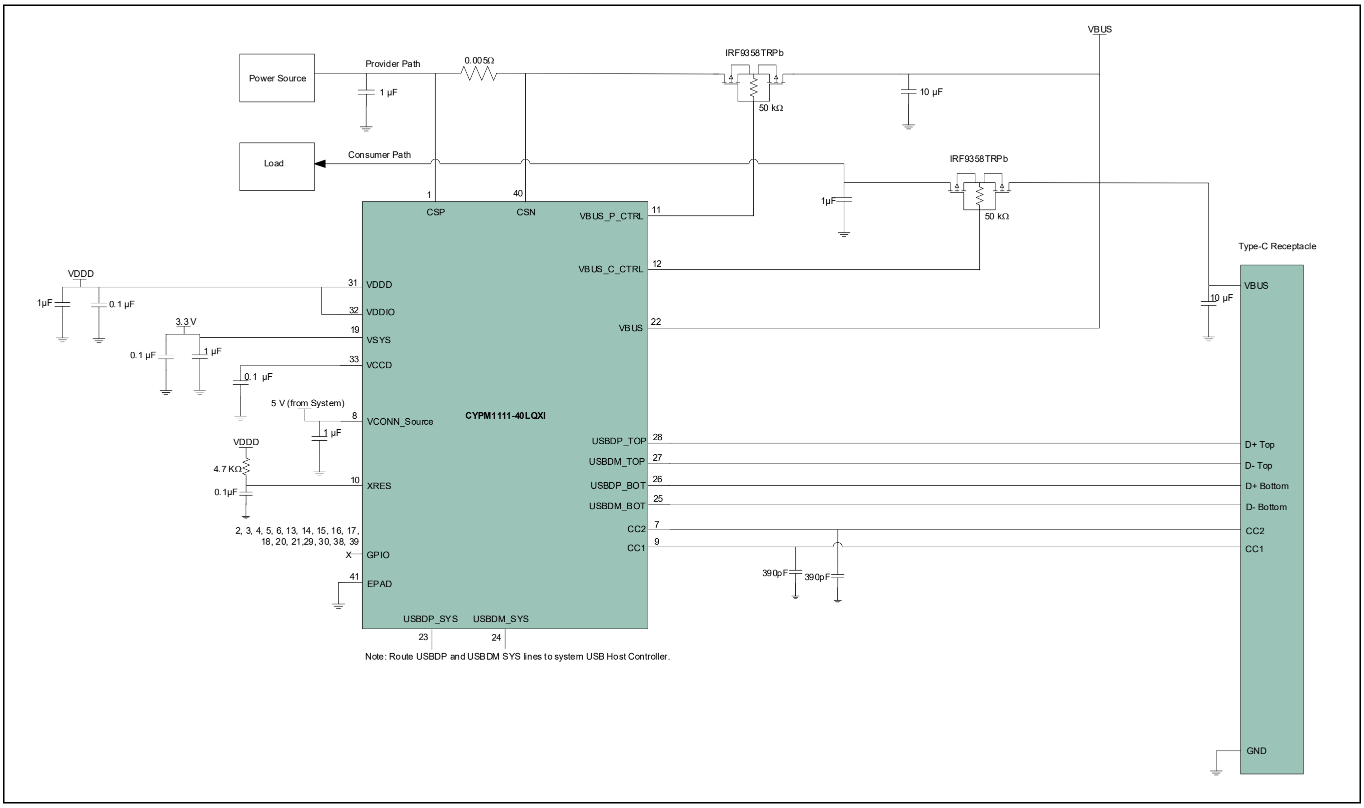

Figure 10 **EZ-PD™ PMG1-S1-based DRP application diagram**

6 Electrical specifications

6.1 Absolute maximum ratings

Table 5 Absolute maximum ratings[3]

Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
V_{SYS_MAX}	Supply relative to V_{SS}	–	–	6	V[4]	–
$V_{CONN\_SOURCE\_MAX}$	Max supply voltage relative to V_{SS}	–	–	6	V	
V_{BUS_MAX}	Max V_{BUS} voltage relative to Vss	–	–	24	V	
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	V_{DDD}	V	
V_{GPIO_ABS}	Inputs to GPIO, DP/DM mux (USBDP/DM_SYS, USBDP/DM_TOP/BOT/SBU_1/SBU_2)	–0.5[5]	–	V_{DDIO} + 0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model (ESD-HBM)	2200	–	–	V	–
ESD_HBM_SBU	Electrostatic discharge human body model for SBU1, SBU2 pins	1100	–	–	V	Only applicable to SBU1 and SBU2 pins
ESD_CDM	Electrostatic discharge charged device model (ESD-CDM)	500	–	–	V	–
LU	Pin current for latch-up	–200	–	200	mA	–
$V_{CC\_PIN\_ABS}$	Max voltage on CC1 and CC2 pins	–	–	24	V	–
$V_{SBU\_PIN\_ABS}$	Max voltage on SBU1 and SBU2 pins	–	–	24	V	–
$V_{GPIO\_FAILSAFE\_ABS}$	Fail-Safe pins (16, 17) voltage	–0.5	–	6	V	–

Notes

3. Usage above the absolute maximum conditions listed in **Table 5** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
4. All voltages are relative to Ground unless otherwise specified.
5. In a system, if the negative spike exceeds the minimum voltage specified here, it is recommended to add Schottky diode to clamp the negative spike.

6.2 Pin based absolute maximum ratings

Table 6 Pin based absolute maximum ratings

S. No	Pin (40 QFN)	Name	Absolute minimum (V)	Absolute maximum (V)	Remarks
1	2	P1.0	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
2	3	P1.1	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
3	4	P1.2	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
4	5	P1.3	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
5	6	P1.4	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
6	13	P2.0	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
7	14	P2.1	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
8	15	P2.2	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
9	16	P5.0	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
10	17	P5.1	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
11	18	P3.0	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
12	20	P3.1	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
13	21	P3.2	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
14	29	P4.0	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
15	30	P4.1	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
16	38	P0.0	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
17	39	P0.1	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
18	9	CC1	–0.5	24	–
19	7	CC2	–0.5	24	–
20	23	USBDP_SYS	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
21	24	USBDM_SYS	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
22	25	USBDM_BOT	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
23	26	USBDP_BOT	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
24	27	USBDM_TOP	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
25	28	USBDP_TOP	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
26	11	VBUS_P_CTRL	–0.5	24	This is an output only pin
27	12	VBUS_C_CTRL	–0.5	24	This is an output only pin
28	34	SBU_2	–0.5	24	–
29	35	SBU_1	–0.5	24	–
30	36	AUX_P	–0.5	6	–
31	37	AUX_N	–0.5	6	–
32	1	CSP	–0.5	6	–
33	40	CSN	–0.5	6	–
34	10	XRES	–0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
35	8	VCONN_Source	–	6	–
36	19	VSYS	–	6	–

Table 6 Pin based absolute maximum ratings *(continued)*

S. No	Pin (40 QFN)	Name	Absolute minimum (V)	Absolute maximum (V)	Remarks
37	22	VBUS	–	24	–
38	31	VDDD	–	6	This is an output only pin
39	32	VDDIO	–	VDDD	–
40	33	VCCD	–	1.95	This is an output only pin
41	EPAD	VSS	–	–	–

6.3 Device-level specifications

All specifications are valid for –40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

6.3.1 DC specifications

Table 7 DC specifications (operating conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#23	V_{SYS}	–	2.75	–	5.5	V	UFP applications
SID.PWR#23_A	V_{SYS}	–	3	–	5.5	V	DFP/DRP applications
SID.PWR#22	V_{BUS}	–	4	–	21.5	V	–
SID.PWR#1	V_{DDD}	Regulated output voltage when V_{SYS} powered	V_{SYS} – 0.05	–	V_{SYS}	V	–
SID.PWR#1_A	V_{DDD}	Regulated output voltage when V_{BUS} powered	3	–	3.65	V	–
SID.PWR#26	V_{5V}	–	4.85	–	5.5	V	–
SID.PWR#13	V_{DDIO}	–	V_{DDD}	–	V_{DDD}	V	–
SID.PWR#24	V_{CCD}	Regulated output voltage (for Core Logic)	–	1.8	–	V	–
SID.PWR#15	C_{EFC}	Regulator bypass capacitor for V_{CCD}	–	100	–	nF	X5R ceramic
SID.PWR#16	C_{EXC}	Regulator bypass capacitor for V_{DDD}	–	1	–	µF	
Active Mode, V_{SYS} = 2.75 V to 5.5 V. Typical values measured at V_{SYS} = 3.3 V							
SID.PWR#4	I_{DD12}	Supply current	–	10	–	mA	T_A = 25°C, CC I/O IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, PD port active
Deep Sleep Mode, V_{SYS} = 2.75 V to 3.6 V							
SID34	I_{DD29}	V_{SYS} = 2.75 to 3.6 V, I^2C, wakeup and WDT on.	–	150	–	µA	V_{SYS} = 3.3 V, T_A = 25°C,
SID_DS1	I_{DD_DS1}	V_{SYS} = 3.3 V, CC wakeup on, Type-C not connected.	–	100	–	µA	Power source = V_{SYS}, Type-C not attached, CC enabled for wakeup, R_P and R_D connected at 70-ms intervals by CPU.
SID_DS3	I_{DD_DS2}	V_{SYS} = 3.3 V, CC wakeup on, DP/DM ON with ADC/CSA/UVOV On	–	500	–	µA	IDD_DS1 + DP/DM, CC ON, ADC/CSA/UVOV ON
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	50	–	µA	Power Source = V_{SYS} = 3.3 V, Type-C Not Attached, T_A = 25°C

6.3.2 CPU

Table 8 CPU specifications (guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	F_{CPU}	CPU input frequency	–	–	48	MHz	All V_{DDD}
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–	µs	Guaranteed by characterization
SYS.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	

6.3.3 GPIO

Table 9 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, $V_{DDIO} < 2.7$ V	0.7 × V_{DDIO}	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, $V_{DDIO} < 2.7$ V	–	–	0.3 × V_{DDIO}	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq 2.7$ V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq 2.7$ V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.6	–	–	V	I_{OH} = –4 mA at 3-V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.5	–	–	V	I_{OH} = –1mA at 1.8-V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDIO}
SID.GIO#35A	$V_{OL\_I2C\_2}$	Output low voltage			0.4	V	I_{OL} = 3 mA, $V_{DDIO} > 2$ V
SID.GIO#35B	$V_{OL\_I2C\_3}$	Output low voltage			0.6[6]	V	I_{OL} = 6 mA, $V_{DDIO} > 1.71$ V
SID.GIO#35C	V_{OL1_20mA}	Output low voltage			0.4	V	I_{OL} = 20 mA, $V_{DDIO} > 3.0$ V, Applicable for fail-safe pins only
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 10 mA (IOL_LED) at 3-V V_{DDIO}
SID.GIO#5	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	+25°C T_A, All V_{DDIO}
SID.GIO#6	Rpd	Pull-down resistor when enabled	3.5	5.6	8.5	kΩ	+25°C T_A, All V_{DDIO}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDIO}
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3	7	pF	–
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL	15	40	–	mV	$V_{DDIO} > 2.7$ V. Guaranteed by characterization.

Table 9 GPIO DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDIO}	–	–	mV	V_{DDIO} < 4.5 V
SID.GIO#44A	$V_{HYSCMOS55}$	Input hysteresis CMOS	200	–	–	mV	V_{DDIO} > 4.5 V

Table 10 GPIO AC specifications (guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID.GIO#46	T_{RISES}	Rise time in Slow Strong mode	10	–	60	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID.GIO#47	T_{FALLS}	Fall time in Slow Strong mode	10	–	60	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID.GIO#48	F_{GPIO_OUT1}	GPIO F_{OUT}; 3.3 V ≤ V_{DDIO} ≤ 5.5 V. Fast Strong mode.	–	–	16	MHz	90/10%, 25-pF load
SID.GIO#49	F_{GPIO_OUT2}	GPIO F_{OUT}; 1.7 V ≤ V_{DDIO} ≤ 3.3 V. Fast Strong mode.	–	–	16	MHz	90/10%, 25-pF load
SID.GIO#50	F_{GPIO_OUT3}	GPIO F_{OUT}; 3.3 V ≤ V_{DDIO} ≤ 5.5 V. Slow Strong mode.	–	–	7	MHz	90/10%, 25-pF load
SID.GIO#51	F_{GPIO_OUT4}	GPIO F_{OUT}; 1.7 V ≤ V_{DDIO} ≤ 3.3 V. Slow Strong mode.	–	–	3.5	MHz	90/10%, 25-pF load
SID.GIO#52	F_{GPIO_IN}	GPIO input operating frequency; 1.7 V ≤ V_{DDIO} ≤ 5.5 V.	–	–	16	MHz	90/10% V_{IO}

6.3.4 XRES

Table 11 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	0.05× V_{DDIO}	–	mV	Guaranteed by characterization

Note

6. To drive full bus load at 400 kHz, 6-mA I_{OL} is required at 0.6-V V_{OL}. Parts not meeting this specification can still function, but not at 400 kHz and 400 pF.

6.4 Digital peripherals

6.4.1 Pulse width modulation (PWM) for GPIO pins

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Table 12 PWM AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

6.4.2 I^2C

Table 13 Fixed I^2C AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

6.4.3 UART

Table 14 Fixed UART AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

6.4.4 SPI

Table 15 Fixed SPI AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	F_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 16 Fixed SPI master mode AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 17 Fixed SPI slave mode AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	48 + (3 × T_{SCB})	ns	$T_{SCB} = T_{CPU}$
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK Valid edge	100	–	–	ns	–

6.4.5 Memory

Table 18 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#4	T_{ROW_WRITE}	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#3	T_{ROW_ERASE}	Row erase time	–	–	13	ms	–
SID.MEM#8	$T_{ROWPROGRAM}$	Row program time after erase	–	–	7	ms	25°C to 55°C, All V_{DDD}
SID178	$T_{BULKERASE}$	Bulk erase time (128 KB)	–	–	35	ms	Guaranteed by design
SID180	$T_{DEVPROG}$	Total device program time	–	–	25	s	Guaranteed by design
SID.MEM#6	F_{END}	Flash endurance	100k	–	–	cycles	–
SID182	F_{RET1}	Flash retention, $T_A \leq 55°C$, 100K P/E cycles	20	–	–	years	–
SID182A	F_{RET2}	Flash retention, $T_A \leq 85°C$, 10K P/E cycles	10	–	–	years	–
SID182B	F_{RET3}	Flash retention, $T_A \leq 105°C$, 10K P/E cycles	3	–	–	years	–

6.5 System resources

6.5.1 Power-on reset (POR) with brown out

Table 19 Imprecise POR (IPOR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4	V	

Table 20 Precise POR (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	

6.5.2 SWD interface

Table 21 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.SWD#1	F_SWDCLK1	$3.3\ V \le V_{DDIO} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	$1.8\ V \le V_{DDIO} \le 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	

6.5.3 Internal main oscillator

Table 22 IMO AC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 48 MHz (trimmed)	–	–	±2	%	$2.7\ V \le V_{DDD} < 5.5\ V$. $-25°C \le T_A \le 85°C$
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	–
SID.CLK#1	F_{IMO}	IMO frequency	–	48	–	MHz	–

6.5.4 Internal low-speed oscillator

Table 23 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

6.5.5 PD

Table 24 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.DC.cc_shvt.1	vSwing	Transmitter output high voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter output low voltage		–	0.075	V	–
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33	–	75	Ω	–
SID.DC.cc_shvt.4	zBmcRx	Receiver input impedance	10	–		MΩ	Guaranteed by design
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64	–	96	µA	–
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5A at 5 V advertisement	165.6	–	194.4	µA	–
SID.DC.cc_shvt.7	Idac_3a	Source current for 3A at 5 V advertisement	303.6	–	356.4	µA	–
SID.DC.cc_shvt.8	R_D	Pull down termination resistance when acting as UFP (upstream facing port)	4.59	–	5.61	kΩ	–
SID.DC.cc_shvt.9	Rd_db	Pull down termination resistance when acting as UFP, with dead battery	4.08	–	6.12	kΩ	–
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108	–		kΩ	–
SID.DC.cc_shvt.11	DFP_de-fault_0p2	CC voltages on DFP side-Standard USB	0.15	–	0.25	V	–
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35	–	0.45	V	–
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75	–	0.85	V	–
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3A	2.45	–	2.75	V	–
SID.DC.cc_shvt.15	UFP_de-fault_0p66	CC voltages on UFP side-Standard USB	0.61	–	0.7	V	–
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16	–	1.31	V	–

Table 24 PD DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.DC.cc_shvt.17	Vattach_ds	Deep sleep attach threshold	0.3	–	0.6	%	–
SID.DC.cc_shvt.18	Rattach_ds	Deep sleep pull-up resistor	10	–	50	kΩ	–
SID.DC.cc_shvt.30	FS_0p53	Voltage threshold for fast swap detect	0.49	–	0.58	V	–

6.5.6 ADC

Table 25 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}	–	V_{DDDmax}	V	Reference voltage generated from V_{DDD}
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04	V	Reference voltage generated from deep sleep reference

6.5.7 Charger detect

Table 26 Charger detect DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DC.CHGDET.1	VDAT_REF	Data detect voltage in charger detect mode	250	–	400	mV	–
DC.CHGDET.2	VDM_SRC	Dn voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.3	VDP_SRC	Dp voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.4	IDM_SINK	Dn sink current in charger detect mode	25	–	175	µA	–
DC.CHGDET.5	IDP_SINK	Dp sink current in charger detect mode	25	–	175	µA	–
DC.CHGDET.6	IDP_SRC	Data contact detect current source	7	–	13	µA	–
DC.CHGDET.32	RDM_UP	Dp/Dn pull-up resistance	0.9	–	1.575	kΩ	–
DC.CHGDET.31	RDM_DWN	Dp/Dn pull-down resistance	14.25	–	24.8	kΩ	–
DC.CHGDET.29	RDAT_LKG	Data line leakage on Dp/Dn	300	–	500	kΩ	–
DC.CHGDET.34	VSETH	Logic Threshold	1.26	–	1.54	V	–
DC.pmg1s1.dpdm.14	RDCP_DAT	Dedicated charging port resistance across DP and DN	–	–	40	Ω	

6.5.8 V_{SYS} switch

Table 27 V_{SYS} switch specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.DC.VDDDSW.1	Res_sw	Resistance from supply input to output supply V_{DDD}	–	–	1.5	Ω	Measured with a load current of 5 mA to 10 mA on V_{DDD}.

6.5.9 CSA

Table 28 CSA DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.csa_scp.42	SCP_6A	Short circuit current detect @ 6A	–	±10	–	%	–
DC.csa_scp.43	SCP_10A	Short circuit current detect @10A	–	±10	–	%	–
OP.csa_scp.11	Rsense	External sense register	–	5	–	mΩ	1% accuracy
DC.csa_scp.44	Iocp_1A	OCP Trip threshold for 1A with Rsense = 5 mΩ	–	130 ±20%	–	%	1A PD contracts OCP set at 130% of contract value or user programmable
	Iocp_1A	OCP Trip threshold for 1A with Rsense = 10 mΩ	–	130 ±10%	–	%	1A PD contracts OCP set at 130% of contract value or user programmable
DC.csa_scp.45	Iocp_5A	OCP Trip threshold for 2A, 3A, 4A and 5A contracts with Rsense = 5/10 mΩ	–	130 ±10%	–	%	2A, 3A, 4A, and 5A PD contracts OCP set at 130% of contract value OR user programmable
DC.rcp_scp.7a	I_csainn_lk	CSP pin input leakage when RCP and CSA blocks are OFF	–	–	10	µA	For provider V_{BUS} = 5 V
DC.rcp_scp.6a	I_csainp_lk	CSN pin input leakage when RCP and CSA blocks are OFF	–	–	80	µA	For provider V_{BUS} = 5 V
DC.sys.1	I_CSP_RCP_ON _CSA_OFF	CSP pin current when RCP block is ON and SCP is OFF	–	–	20	µA	For provider V_{BUS} = 5 V
DC.sys.2	I_CSN_RCP_ON _CSA_OFF	CSN pin current when RCP block is ON and SCP is OFF	–	–	100	µA	For provider V_{BUS} = 5 V
DC.sys.3	I_CSP_CSA_ON	CSP pin current when RCP block is OFF and SCP is ON	–	–	30	µA	For provider V_{BUS} = 5 V
DC.sys.4	I_CSN_CSA_ON	CSN pin current when RCP block is OFF and SCP is ON	–	–	100	µA	For provider V_{BUS} = 5 V
DC.sys.5	I_CSP_RCP_ON _CSA_ON	CSP pin current when RCP block is ON and SCP is ON	–	–	50	µA	For provider V_{BUS} = 5 V. Guaranteed by design.
DC.sys.6	I_CSP_RCP_ON _CAS_ON	CSN pin current when RCP block is ON and SCP is ON	–	–	120	µA	For provider V_{BUS} = 5 V. Guaranteed by design.

6.5.10 V_{BUS} UV/OV

Table 29 V_{BUS} UV/OV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold accuracy in active mode using bandgap reference	–	±3	–	%	–
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold accuracy in deep sleep mode using deep sleep reference	–	±5	–	%	–
SID.COMP_ACC	COMP_ACC	Comparator input offset at 4s	–15	–	15	mV	–

6.5.11 Consumer side PFET gate driver

Table 30 Consumer side PFET gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.PGDO.1	Rpd	Resistance when “pull_dn” enabled	–	–	5	kΩ	–
DC.pgdo_pd_isnk.12	iout_0	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 1	–	2	–	µA	–
DC.pgdo_pd_isnk.13	iout_1	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 2	–	4	–	µA	–
DC.pgdo_pd_isnk.14	iout_2	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 4	–	8	–	µA	–
DC.pgdo_pd_isnk.15	iout_3	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 8	–	16	–	µA	–
DC.pgdo_pd_isnk.16	iout_4	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 16	–	32	–	µA	–
DC.pgdo_pd_isnk.17	iout_5	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 32	–	63	–	µA	–
DC.pgdo_pd_isnk.18	iout_6	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 64	–	126	–	µA	–
DC.pgdo_pd_isnk.19	iout_7	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 128	–	252	–	µA	–
DC.pgdo_pd_isnk.20	iout_8	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 256	–	504	–	µA	–

Table 30 Consumer side PFET gate driver DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DC.pgdo_pd_isnk.21	iout_9	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 512	–	1008	–	µA	–
DC.pgdo_pd_isnk.22	iout_10	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 1024	–	2016	–	µA	–

Table 31 Consumer side PFET gate driver AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ac.pgdo.2	Tr_discharge	Discharge Rate of output node	–	–	5	V/µs	Guaranteed by design
SID.ac.pgdo.sys_1	Tsoft_on	Consumer FET turn-ON delay for soft start	–	5	–	ms	–

6.5.12 Provider side PFET gate driver

Table 32 Provider side PFET gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DC.pgdo_pu_1	Rpd	Pull-down resistance when enabled using strongest pull-down strength, using the “STRONG_EN =1” field in the USBPD_PGDO_PD_ISNK_CFG register	–	–	2	kΩ	–
DC.pgdo_pu.2	Rpu	Pull-up resistance	–	1	2	kΩ	–
DC.pgdo_pd_isnk.1	Rpd_0	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 1	–	6830	–	Ω	–
DC.pgdo_pd_isnk.2	Rpd_1	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 2	–	3760	–	Ω	–
DC.pgdo_pd_isnk.3	Rpd_2	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 4	–	1900	–	Ω	–
DC.pgdo_pd_isnk.4	Rpd_3	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 8	–	1000	–	Ω	–
DC.pgdo_pd_isnk.5	Rpd_4	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 16	–	660	–	Ω	–
DC.pgdo_pd_isnk.6	Rpd_5	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 32	–	1700	–	Ω	–
DC.pgdo_pd_isnk.7	Rpd_6	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 64	–	900	–	Ω	–

Table 32 Provider side PFET gate driver DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DC.pgdo_pd_isnk.8	Rpd_7	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 128	–	630	–	Ω	–
DC.pgdo_pd_isnk.9	Rpd_8	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 256	–	560	–	Ω	–
DC.pgdo_pd_isnk.10	Rpd_9	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 512	–	530	–	Ω	–
DC.pgdo_pd_isnk.11	Rpd_10	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 1024	–	520	–	Ω	–

Table 33 Provider side PFET gate driver AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
AC.pgdo_pu.1	Tpu	Pull-up delay	–	10	35	µs	For pull-up load of 4-nF capacitor and 50-kΩ resistor
AC.pgdo_pu.2	Tpd	Pull-down delay	–	–	2	µs	–
AC.pgdo_pu.3	SRpu	Output slew rate measured from 20% to 80% of output rising waveform.	–	–	8	V/µs	Cload = 4 nF, Vout = 0 V to 24 V, external pull-up of 50 kΩ
AC.pgdo_pu.4	SRpd	Output slew rate measured from 80% to 20% of output falling waveform.	–	–	8	V/µs	Cload = 4 nF, Vout = 24 V to 0 V, external pull-up of 50 kΩ
AC.pgdo.sys_1	Tsoft_on	Provider FET turn-ON delay for soft start	–	5	–	ms	–

6.5.13 Provider side PFET RCP

Table 34 Provider side PFET RCP DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.RCP.44	Vcsa_rcp	Voltage across external Rsense between CSP/CSN for which RCP condition detected (CSN higher than CSP by Vcsa_rcp)	–	2	6	mV	–
DC.RCP.45	Vcomp_rcp	Voltage across V_{BUS} and CSN pins for which RCP condition is detected	20	–	130	mV	–
DC.RCP.46	Vbus_max_det	Voltage on CSN pin during provider FET ON (source) for which RCP condition is detected (this threshold is user programmable	5.55	5.75	5.95	V	This spec is for 5-V provider V_{BUS} voltage. For higher voltages, firmware changes this threshold based on V_{BUS} contract voltage.

Table 35 Provider side PFET RCP, SCP AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
AC.RCP_SYS.1	Toff_scp	Provider PFET switching off after short circuit current detect through provider PFET	–	10	–	µs	Provider FET turns off with gate pull-up of 50 kΩ and total gate cap of 4 nF.
AC.RCP_SYS.1	Toff_rcp	Provider PFET switching off after reverse current detect through provider PFET	–	10	–	µs	Provider FET turns off with gate pull-up of 50 kΩ and total gate cap of 4 nF.
AC.RCP_SYS.2	Ton	Recovery time to turn-ON PFET RCP condition is removed	–	55	80	µs	–

Table 36 V_{BUS} **provider transition specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
AC.tr.1	Ton	V_{BUS} Low to High (10% to 90%) for provider FET	–	5	–	ms	0 to 5-V transition, system-level with external PFET with gate pull-up of 50 kΩ and total gate cap of 4 nF.
AC.tr.2	FR_Ton	V_{BUS} Low to High (10% to 90%) during FR swap	–	50	150	µs	0 to 5-V transition, system-level with external PFET with gate pull-up of 50 kΩ and total gate cap of 4 nF.
AC.tr.3	Toff	VBUS_P_CTRL High to Low (90% to 10%) using internal active pull-up	–	11	–	µs	5 to 0-V transition, system-level with external PFET with gate pull-up of 50 kΩ and total gate cap of 4 nF.

6.5.14 SBU Mux

Table 37 **SBU Mux DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DC.pmg1s1.20sbu.1	Ron1	On resistance of AUXP/N to SBU1/2 switch @ 3.3-V input	–	4	7	Ω	–
DC.pmg1s1.20sbu.2	Ron2	On resistance of AUXP/N to SBU1/2 switch @ 1-V input	–	3	5	Ω	–
DC.pmg1s1.20sbu.3	lsb	Block leakage current (VPUMP + VDDD + VCCD)	–	–	15	µA	–
DC.pmg1s1.20sbu.15	icc	Block ICC when switch fully ON	–	15	125	µA	–
DC.pmg1s1.20sbu.16	OVP_threshold	Overvoltage protection detection threshold above VDDIO	200	–	1200	mV	–
DC.pmg1s1.20sbu.17	lsx_ron_3p3	On resistance of LSTX/LSRX to SBU1/2 switch @ 3.3-V input	–	8.5	17	Ω	–
DC.pmg1s1.20sbu.18	lsx_ron_1	On resistance of LSTX/LSRX to SBU1/2 switch @ 1-V input	–	5.5	11	Ω	–
DC.pmg1s1.20sbu.19	aux_ron_flat_fs	Switch On flat resistance of AUX_P/N to SBU1/2 switch (from 0 to 3.3 V)	–	–	2.5	Ω	–
DC.pmg1s1.20sbu.20	aux_ron_flat_hs	Switch On flat resistance of AUX_P/N to SBU1/2 switch (from 0 to 1 V)	–	–	0.5	Ω	–

Table 37 SBU Mux DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DC.pmg1s1.20sbu.21	lsx_ron_flat_fs	Switch On flat resistance of LSTX/LSRX to SBU1/2 switch (from 0 to 3.3 V)	–	5	–	Ω	–
DC.pmg1s1.20sbu.22	lsx_ron_flat_hs	Switch On flat resistance of LSTX/LSRX to SBU1/2 switch (from 0 to 1 V)	–	0.5	–	Ω	–

Table 38 SBU Mux AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
AC.pmg1s1.20sbu.1	Con	Switch ON capacitance	–	–	120	pF	Guaranteed by design
AC.pmg1s1.20sbu.2	Coff	Switch OFF capacitance Connector side	–	–	80	pF	Guaranteed by design
AC.pmg1s1.20sbu.3	Off_isolation	Switch isolation at F = 1 MHz	–50	–	–	dB	Guaranteed by design
AC.pmg1s1.20sbu.4	TON	SBU switch turn-ON time	–	–	200	µs	Guaranteed by design
AC.pmg1s1.20sbu.5	TOFF	SBU switch turn-OFF time	–	–	400	µs	Guaranteed by design
AC.pmg1s1.20sbu.3_ aux	Off_isolation_AC_aux	Switch isolation at F = 1 MHz, from AUX to SBU pins	–50	–	–	dB	Guaranteed by design
AC.pmg1s1.20sbu.6	Off_isolation_tran_dB	Coupling on sbu1, 2 terminated to 50 W, switch-OFF, 1-MHz rail-to-rail toggling on LSTX/LSRX	–40	–	–	dB	Guaranteed by design
AC.pmg1s1.20sbu.6_ aux	Off_isolation_tran_d-B_aux	Coupling on sbu1, 2 terminated to 50 W, switch-OFF, 1-MHz rail-to-rail toggling on AUX_P/AUX_N	–30	–	–	dB	Guaranteed by design
AC.pmg1s1.20sbu.7	X_talk_AC	Cross talk of Switch at F = 1 MHz, SBU1/2 to SBU2/1 when is data transferred from LSTX/RX	–50	–	–	dB	Guaranteed by design
AC.pmg1s1.20sbu.7_ aux	X_talk_AC_aux	Cross talk of Switch at F = 1 MHz, SBU1/2 to SBU2/1 when is data transferred from AUXP/AUXN	–50	–	–	dB	Guaranteed by design

Table 38 SBU Mux AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
AC.pmg1s1.20sbu.8	X_talk_tran_dB	Coupling on SBU2 (1)When Data is transferred from LSX to SBU1 (2)Rail-to-rail data on SBU1(2), static signal on SBU2(1)	–30	–	–	dB	Guaranteed by design
AC.pmg1s1.20sbu.8_ aux	X_talk_tran_d- B_aux	Coupling on SBU2 (1)When Data is transferred from AUX to SBU1 (2)Rail-to-rail data on SBU1(2), static signal on SBU2(1)	–30	–	–	dB	Guaranteed by design

6.5.15 USB 2.0 Mux

Table 39 USB 2.0 Mux DC specifications

(Charger detect block is disconnected from USBDP_TOP, USBDM_TOP, USBDP_BOT and USBDM_BOT through switch)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.pmg1s1.dpdm.1	RON_HS	DP/DM on resistance (0 to 0.5 V) - HS mode	–	–	8	Ω	–
DC.pmg1s1.dpdm.2	RON_FS	DP/DM on resistance (0 to 3.3 V) - FS mode	–	–	12	Ω	–
DC.pmg1s1.dpdm.5	Con_FS	Switch on capacitance at 6 MHz - FS mode	–	–	50	pF	Guaranteed by design
DC.pmg1s1.dpdm.6	Con_HS	Switch on capacitance at 240 MHz - HS mode	–	–	10	pF	–
DC.pmg1s1.dpdm.9	ileak_pin	Pin leakage at DP/DM connector side and host side	–	–	1	µA	–
DC.pmg1s1.dpdm.11	RON_FLAT_HS	DP/DM on flat resistance in HS mode (0 to 0.4 V)	–	–	0.5	Ω	Guaranteed by design
DC.pmg1s1.dpdm.12	RON_FLAT_FS	DP/DM on flat resistance in FS mode (0 to 3.3 V)	–	–	4	Ω	Guaranteed by design

Table 40 USB 2.0 Mux AC specifications

(Charger detect block is disconnected from USBDP_TOP, USBDM_TOP, USBDP_BOT and USBDM_BOT through switch)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
AC.pmg1s1.dpdm.1	BW_3dB_HS	3-db bandwidth	700	–	–	MHz	Guaranteed by design
AC.pmg1s1.dpdm.2	BW_3dB_FS	3-db bandwidth	100	–	–	MHz	Guaranteed by design
AC.pmg1s1.dpdm.5	T_{ON}	DP/DM switch turn-on time	–	–	200	µs	–
AC.pmg1s1.dpdm.6	T_{OFF}	DP/DM switch turn-off time	–	–	0.4	µs	Guaranteed by design
AC.pmg1s1.dpdm.7	T_{ON_VPUMP}	DP/DM charge pump startup time	–	–	200	µs	Guaranteed by characterization
AC.pmg1s1.dpdm.8	Off_isolation_HS	Switch-off isolation for HS	–20	–	–	dB	Guaranteed by design
AC.pmg1s1.dpdm.9	Off_isolation_FS	Switch-off isolation for FS	–50	–	–	dB	Guaranteed by design
AC.pmg1s1.dpdm.10	X_talk	Cross talk of switch From FS to HS at F=12 MHz	–50	–	–	dB	Guaranteed by design

6.5.16 VCONN switch

Table 41 VCONN switch DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DC.pmg1s1.20VCONN.1	Ron	Switch ON resistance at VCONN_Source = 5 V with 215-mA load current	–	0.7	1.3	Ω	–
DC.pmg1s1.20VCONN.9	I_{OCP}	Overcurrent detection range for CC1/CC2	550	–	–	mA	–
DC.pmg1s1.20VCONN.10	OVP_threshold	CC1, CC2 overvoltage protection detection threshold above V_{DDD} or VCONN_Source, whichever is higher	200	–	1200	mV	–
DC.pmg1s1.20VCONN.11	OVP_hysteresis	Overvoltage detection hysteresis	50	–	200	mV	Guaranteed by design

Table 41 VCONN switch DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DC.pmg1s1.20VCONN.12	OCP_hysteresis	Overcurrent detection hysteresis	20	–	60	mA	–
DC.pmg1s1.20VCONN.14	OVP_threshold_on	Overvoltage detection threshold above VCONN_Source of CC1/2, with CC1 or CC2 switch enabled. Same threshold triggers reverse current protection circuit	200	–	700	mV	–

Table 42 VCONN switch AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
AC.pmg1s1.20VCONN.1	T_{ON}	VCONN switch turn-on time	–	–	200	µs	–
AC.pmg1s1.20VCONN.2	T_{OFF}	VCONN switch turn-off time	–	–	3	µs	Guaranteed by design

6.5.17 V_{BUS}

Table 43 V_{BUS} discharge specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VBUS.DISC.1	Ron1	20-V NMOS ON resistance	1500	–	3000	Ω	–
SID.VBUS.DISC.2	Ron2	20-V NMOS ON resistance	750	–	1500	Ω	–
SID.VBUS.DISC.3	Ron3	20-V NMOS ON resistance	500	–	1000	Ω	–
SID.VBUS.DISC.4	Ron4	20-V NMOS ON resistance	375	–	750	Ω	–
SID.VBUS.DISC.5	Ron5	20-V NMOS ON resistance	300	–	600	Ω	–

7 Ordering information

Table 44 lists the EZ-PD™ PMG1-S1 part numbers and features.

Table 44 EZ-PD™ PMG1-S1 ordering information

MPN	Application	Type-C ports	Termination resistor: R_{D-DB}	Role	Package	Si ID
CYPM1111-40LQXI CYPM1111-40LQXIT	DRP applications	1	R_P[7], R_D[8], R_{D-DB}[9]	DRP	40-pin QFN	0x2A20

7.1 Ordering code definitions

The part numbers are of the form CYPM1ABC-DEFGHIJ where the fields are defined as follows.

Table 45 Ordering code definitions

Field	Description	Values	Meaning
CY	Cypress prefix	CY	Company ID
PM	Marketing code	PM	PM = Power Delivery MCU family
1	MCU Family generation	1	Product family generation
A	Family	0	S0
		1	S1
		2	S2
		3	S3
B	PD ports	1	1-PD port
		2	2-PD port
C	Application specific	X	Application specific
DE	Pin	XX	Number of pins in the package
FG	Package code	LQ	QFN
		BZ	BGA
		FN	CSP
H	Lead free	X	Lead: X = Pb-free
I	Temperature range	I	Industrial
J	Only for T&R	T	Tape and reel

Notes

7. Termination resistor denoting a Source.
8. Termination resistor denoting an accessory or Sink.
9. Termination resistor denoting dead battery termination.

8 Packaging

Table 46 Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
T_J	Operating junction temperature	Industrial	–40	25	100	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	–	19.3	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	–	13.6	°C/W

Table 47 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
40-pin QFN	260°C	30 seconds

Table 48 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
40-pin QFN	MSL 3

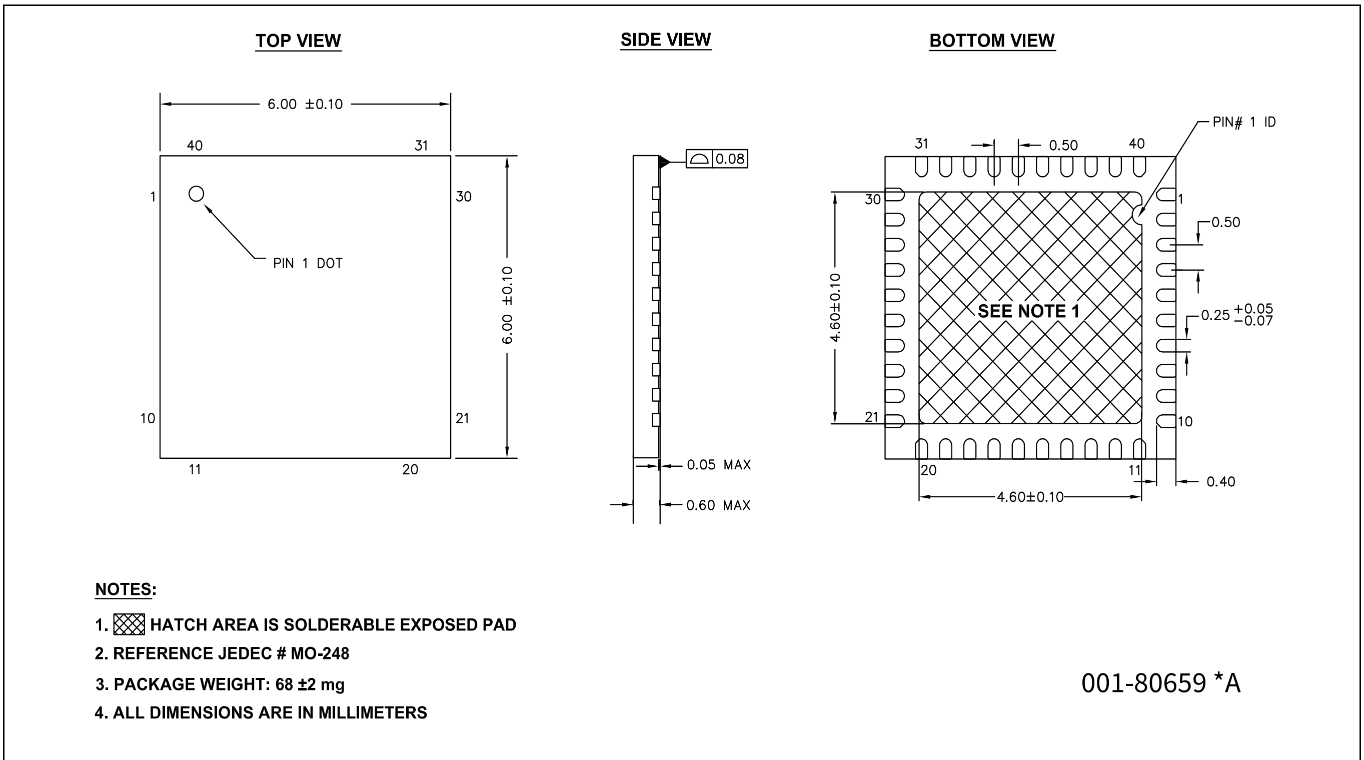

Figure 11 40-pin QFN (6 × 6 × 0.5 mm), LR40A/LQ40A 4.6 × 4.6 E-PAD (Sawn) package outline (PG-VQFN-40), 001-80659

9 Acronyms

Table 49 Acronyms used in this document

Acronym	Description
ACT	active mode
ADC	analog-to-digital converter
AES	advanced encryption standard
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
BOD	Brown out Detect
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
CSA	current sense amplifier
DFP	downstream facing port
DP	DisplayPort, digital display interface developed by Video Electronics Standards Association
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access
DRP	dual role power
DS	deep sleep mode
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FRS	fast role swap
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt

Table 49 Acronyms used in this document *(continued)*

Acronym	Description
NVIC	nested vectored interrupt controller
OCP	overcurrent protection
opamp	operational amplifier
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PRNG	pseudo random number generation
PWM	pulse-width modulator
RAM	random-access memory
RCP	reverse current protection, supported in Source Configuration only
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SBU	sideband use
SCB	serial communication block
SCL	I^2C serial clock
SCP	short circuit protection, supported in Source Configuration only
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer counter pulse-width modulator
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UFP	upstream facing port
USB	Universal Serial Bus
USBIO	USB input/output, EZ-PD™ PMG1-S1 pins used to connect to a USB port
UVP	undervoltage protection
XRES	external reset I/O pin

10 Document conventions

10.1 Units of measure

Table 50 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kiloohm
Mbps	megabits per second
MHz	megahertz
MΩ	megaohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of change
*E	2023-07-12	Updated **Figure 11** title: Added the package name. Publish to web.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-07-12
Published by

Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email:
erratum@infineon.com

Document reference
002-31597 Rev. *E