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The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY9AAA0N Series

32-bit Arm® Cortex®-M3 FM3 Microcontroller

The CY9AAA0N Series are highly integrated 32-bit microcontrollers that dedicated for embedded controllers with low-power consumption mode and competitive cost.
The CY9AAA0N Series are based on the Arm® Cortex®-M3 Processor with on-chip Flash memory and SRAM, and has peripheral functions such as LCD Controller, Motor Control Timers, ADCs, DACs and Communication Interfaces (UART, CSIO, I²C).

The products which are described in this data sheet are placed into TYPE7 product categories in FM3 Family Peripheral Manual.

Features

32-bit Arm® Cortex®-M3 Core

- Processor version: r2p1
- Up to 20MHz Operation Frequency
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 channel NMI (non-maskable interrupt) and 32 channels' peripheral interrupts and 8 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- Up to 128 Kbytes
- Read cycle: 0 wait-cycle
- Security function for code protection

[SRAM]

This series contains a total of up to 16 Kbyte on-chip SRAM that is connected to System bus of Cortex-M3 core.

- SRAM1: Up to 16 Kbytes

LCD controller (LCDC)

- Selectable from 44 SEG × 4 COM (Max) or 40 SEG × 8 COM (Max)
- Internal divide resistor is contained (selectable from 10 kΩ or 100 kΩ for the resistor value)
- LCD drive power supply (bias) pin (VV4 to VV0)
- Interrupt function synchronized with the LCD module frame frequency
- With blinking function
- Inverted display function

Multi-function Serial Interface (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- UART
- CSIO
- I²C

[UART]

- Full duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[I²C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

A/D Converter (Max 16 channels)

[12-bit A/D Converter]

- Successive Approximation type
- Conversion time: Min 1.0 μs
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4 steps)

D/A Converter (Max 2 channels)

- R-2R type
- 10-bit resolution

Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 84 high-speed general-purpose I/O Ports@100 pin Package
- Some ports are 5V tolerant I/O
  See List of Pin Functions and I/O Circuit Type to confirm the corresponding pins.

Multi-function Timer

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch.
- Input capture × 4ch.
- Output compare × 6ch.
- A/D activation compare × 1ch.
- Waveform generator × 3ch.
- 16-bit PPG timer × 3ch.
  IGBT mode is contained.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

HDMI-CEC/Remote Control Receiver (Up to 2 channels)

- HDMI- CEC receiver / Remote control receiver
  - Operating modes supporting the following standards can be selected
    - SIRCS
    - NEC/Association for Electric Home Appliances
    - HDMI-CEC
  - Capable of adjusting detection timings for start bit and data bit
  - Equipped with noise filter
- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

External Interrupt Controller Unit

- Up to 16 external interrupt input pins
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

The Hardware watchdog timer is clocked by the built-in Low-speed CR oscillator. Therefore, the Hardware watchdog is active in any low-power consumption mode except RTC, Stop, Deep Standby RTC and Deep Standby Stop modes.

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock: 4 MHz to 20 MHz
- Sub Clock: 32.768 kHz
- Built-in High-speed CR Clock: 4 MHz
- Built-in Low-speed CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series includes 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Six low-power consumption modes supported.

- Sleep
- Timer
- RTC
- Stop
- Deep Standby RTC
- Deep Standby Stop

The back up register is 16 byte

Debug

Serial Wire JTAG Debug Port (SWJ-DP)

Power Supply

Wide range voltage:

VCC = 1.8 V to 5.5 V
VCC = 2.2 V to 5.5 V (when LCDC is used)

Contents

1. Product Lineup

Memory size

Product name		CY9AFAA1 N	CY9AFAA2L/N
On-chip Flash memory		64 Kbytes	128 Kbytes
On-chip SRAM	SRAM1	12 Kbytes	16 Kbytes

Function

Product name			CY9AFAA2L	CY9AFAA1N CY9AFAA2N
Pin count			64	100
CPU			Cortex-M3	
	Freq.		20 MHz	
Power supply voltage range			1.8 V to 5.5 V	
LCD Controller (LCDC)			24SEG×4COM (Max) or 20SEG×8COM (Max)	44SEG×4COM (Max) or 40SEG×8COM (Max)
Multi-function Serial Interface (UART/CSIO/I²C)			8ch. (Max)	
Base Timer (PWC/ Reload timer/PWM/PPG)			8ch. (Max)	
MF-Timer	A/D activation compare	1ch.	1 unit (Max)	
	Input capture	4ch.		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG (IGBT mode)	3ch.		
HDMI-CEC/ Remote Control Receiver			2ch. (Max)	
Real-time clock (RTC)			1 unit	
Watchdog timer			1ch. (SW) + 1ch. (HW)	
External Interrupts			8 pins (Max)+ NMI × 1	16 pins (Max)+ NMI × 1
General-purpose I/O ports			52 pins (Max)	84 pins (Max)
12-bit A/D converter			9ch. (1 unit)	16ch. (1 unit)
10-bit D/A converter			2ch. (Max)	
CSV (Clock Super Visor)			Yes	
LVD (Low-Voltage Detector)			2ch.	
Built-in CR	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SWJ-DP	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use. See Electrical Characteristics 12.4 AC Characteristics (12.4.3) Built-in CR Oscillation Characteristics for accuracy of built-in CR.*

2. Packages

Package \ Product name	CY9AFAA2L	CY9AFAA1N CY9AFAA2N
LQFP: LQG064 (0.65mm pitch)	❍	-
LQFP: LQI100 (0.5mm pitch)	-	❍

❍: Supported

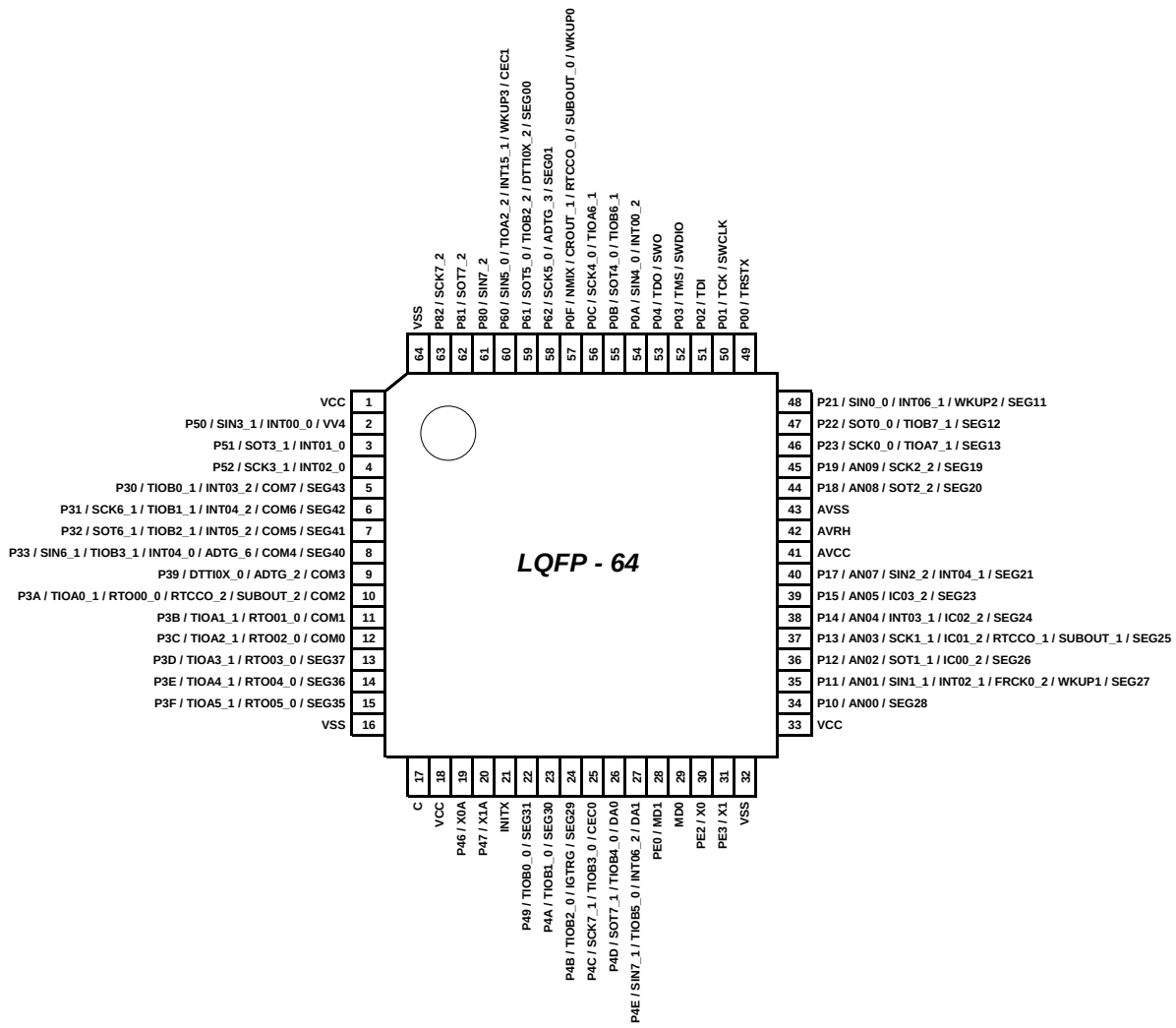
Note:

- *See Package Dimensions for detailed information on each package.*

3. Pin Assignment

LQD064

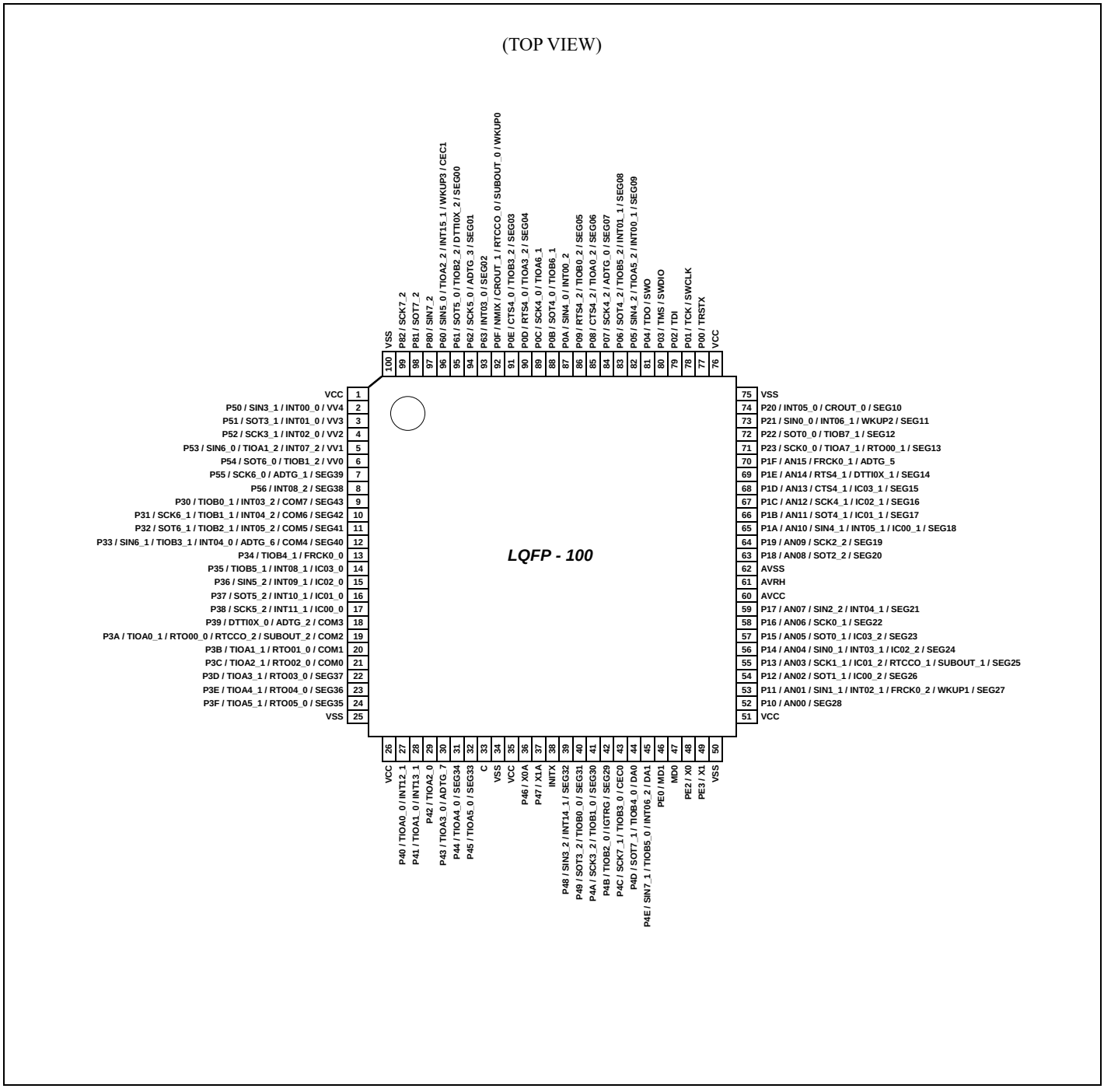
(TOP VIEW)



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LQI100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
1	1	VCC	-	
2	2	P50 INT00_0 SIN3_1 VV4	R	W
-	3	P51 INT01_0 SOT3_1 (SDA3_1) VV3	R	W
3	-	P51 INT01_0 SOT3_1 (SDA3_1)	E	F
-	4	P52 INT02_0 SCK3_1 (SCL3_1) VV2	R	W
4	-	P52 INT02_0 SCK3_1 (SCL3_1)	E	F
-	5	P53 SIN6_0 TIOA1_2 INT07_2 VV1	R	W
-	6	P54 SOT6_0 (SDA6_0) TIOB1_2 VV0	R	V
-	7	P55 SCK6_0 (SCL6_0) ADTG_1 SEG39	J	U
-	8	P56 INT08_2 SEG38	J	S

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
5	9	P30 TIOB0_1 INT03_2 COM7 SEG43	K	S
6	10	P31 TIOB1_1 SCK6_1 (SCL6_1) INT04_2 COM6 SEG42	K	S
7	11	P32 TIOB2_1 SOT6_1 (SDA6_1) INT05_2 COM5 SEG41	K	S
8	12	P33 INT04_0 TIOB3_1 SIN6_1 ADTG_6 COM4 SEG40	K	S
-	13	P34 FRCK0_0 TIOB4_1	E	H
-	14	P35 IC03_0 TIOB5_1 INT08_1	E	F
-	15	P36 IC02_0 SIN5_2 INT09_1	E	F
-	16	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1	E	F

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
-	17	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1	E	F
9	18	P39 DTTI0X_0 ADTG_2 COM3	L	U
10	19	P3A RTO00_0 (PPG00_0) TIOA0_1 RTCCO_2 SUBOUT_2 COM2	L	U
11	20	P3B RTO01_0 (PPG00_0) TIOA1_1 COM1	L	U
12	21	P3C RTO02_0 (PPG02_0) TIOA2_1 COM0	L	U
13	22	P3D RTO03_0 (PPG02_0) TIOA3_1 SEG37	J	U
14	23	P3E RTO04_0 (PPG04_0) TIOA4_1 SEG36	J	U
15	24	P3F RTO05_0 (PPG04_0) TIOA5_1 SEG35	J	U
16	25	VSS	-	
-	26	VCC	-	

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
-	27	P40	E	F
		TIOA0_0		
		INT12_1		
-	28	P41	E	F
		TIOA1_0		
		INT13_1		
-	29	P42	E	H
		TIOA2_0		
-	30	P43	E	H
		TIOA3_0		
		ADTG_7		
-	31	P44	J	U
		TIOA4_0		
		SEG34		
-	32	P45	J	U
		TIOA5_0		
		SEG33		
17	33	C	-	
-	34	VSS	-	
18	35	VCC	-	
19	36	P46	D	M
		X0A		
20	37	P47	D	N
		X1A		
21	38	INITX	B	C
-	39	P48	J	S
		INT14_1		
		SIN3_2		
		SEG32		
22	40	P49	J	U
		TIOB0_0		
		SEG31		
-		SOT3_2 (SDA3_2)		
23	41	P4A	J	U
		TIOB1_0		
		SEG30		
-		SCK3_2 (SCL3_2)		

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
24	42	P4B	J	U
		TIOB2_0		
		SEG29		
		IGTRG		
25	43	P4C	G	Q
		TIOB3_0		
		SCK7_1 (SCL7_1)		
		CEC0		
26	44	P4D	O	Z
		TIOB4_0		
		SOT7_1 (SDA7_1)		
		DA0		
27	45	P4E	O	Y
		TIOB5_0		
		INT06_2		
		SIN7_1		
		DA1		
28	46	PE0	C	P
		MD1		
29	47	MD0	H	D
30	48	PE2	A	A
		X0		
31	49	PE3	A	B
		X1		
32	50	VSS	-	
33	51	VCC	-	
34	52	P10	Q	J
		AN00		
		SEG28		
35	53	P11	Q	L
		AN01		
		SIN1_1		
		INT02_1		
		FRCK0_2		
		WKUP1		
		SEG27		
36	54	P12	Q	J
		AN02		
		SOT1_1 (SDA1_1)		
		IC00_2		
		SEG26		

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
37	55	P13	Q	J
		AN03		
		SCK1_1 (SCL1_1)		
		IC01_2		
		RTCCO_1		
		SUBOUT_1		
		SEG25		
38	56	P14	Q	K
		AN04		
		INT03_1		
		IC02_2		
		SEG24		
-		SIN0_1		
39	57	P15	Q	J
		AN05		
		IC03_2		
		SEG23		
-		SOT0_1 (SDA0_1)		
-	58	P16	Q	J
		AN06		
		SCK0_1 (SCL0_1)		
		SEG22		
40	59	P17	Q	K
		AN07		
		SIN2_2		
		INT04_1		
		SEG21		
41	60	AVCC	-	
42	61	AVRH	-	
43	62	AVSS	-	
44	63	P18	Q	J
		AN08		
		SOT2_2 (SDA2_2)		
		SEG20		
45	64	P19	Q	J
		AN09		
		SCK2_2 (SCL2_2)		
		SEG19		

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
-	65	P1A	Q	K
		AN10		
		SIN4_1		
		INT05_1		
		IC00_1		
		SEG18		
-	66	P1B	Q	J
		AN11		
		SOT4_1 (SDA4_1)		
		IC01_1		
		SEG17		
-	67	P1C	Q	J
		AN12		
		SCK4_1 (SCL4_1)		
		IC02_1		
		SEG16		
-	68	P1D	Q	J
		AN13		
		CTS4_1		
		IC03_1		
		SEG15		
-	69	P1E	Q	J
		AN14		
		RTS4_1		
		DTTI0X_1		
		SEG14		
-	70	P1F	F	X
		AN15		
		ADTG_5		
		FRCK0_1		
46	71	P23	J	U
		SCK0_0 (SCL0_0)		
		TIOA7_1		
		SEG13		
-		RTO00_1		
47	72	P22	J	U
		SOT0_0 (SDA0_0)		
		TIOB7_1		
		SEG12		

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
48	73	P21 SIN0_0 INT06_1 WKUP2 SEG11	J	T
-	74	P20 INT05_0 CROUT_0 SEG10	J	S
-	75	VSS	-	
-	76	VCC	-	
49	77	P00 TRSTX	E	E
50	78	P01 TCK SWCLK	E	E
51	79	P02 TDI	E	E
52	80	P03 TMS SWDIO	E	E
53	81	P04 TDO SWO	E	E
-	82	P05 TIOA5_2 SIN4_2 INT00_1 SEG09	J	S
-	83	P06 TIOB5_2 SOT4_2 (SDA4_2) INT01_1 SEG08	J	S
-	84	P07 ADTG_0 SEG07 SCK4_2 (SCL4_2)	J	U
-	85	P08 TIOA0_2 CTS4_2 SEG06	J	U

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
-	86	P09	J	U
		TIOB0_2		
		RTS4_2		
		SEG05		
54	87	P0A	G	F
		SIN4_0		
		INT00_2		
55	88	P0B	G	H
		SOT4_0 (SDA4_0)		
		TIOB6_1		
56	89	P0C	G	H
		SCK4_0 (SCL4_0)		
		TIOA6_1		
-	90	P0D	J	U
		RTS4_0		
		TIOA3_2		
		SEG04		
-	91	P0E	J	U
		CTS4_0		
		TIOB3_2		
		SEG03		
57	92	P0F	E	I
		NMIX		
		CROUT_1		
		RTCCO_0		
		SUBOUT_0		
		WKUP0		
-	93	P63	J	S
		INT03_0		
		SEG02		
58	94	P62	J	U
		SCK5_0 (SCL5_0)		
		ADTG_3		
		SEG01		
59	95	P61	J	U
		SOT5_0 (SDA5_0)		
		TIOB2_2		
		DTTI0X_2		
		SEG00		

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-100			
60	96	P60	G	R
		SIN5_0		
		TIOA2_2		
		INT15_1		
		WKUP3		
		CEC1		
61	97	P80	G	H
		SIN7_2		
62	98	P81	G	H
		SOT7_2 (SDA7_2)		
63	99	P82	G	H
		SCK7_2 (SCL7_2)		
64	100	VSS	-	

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
ADC	ADTG_0	A/D converter external trigger input pin	-	84
	ADTG_1		-	7
	ADTG_2		9	18
	ADTG_3		58	94
	ADTG_4		-	-
	ADTG_5		-	70
	ADTG_6		8	12
	ADTG_7		-	30
	ADTG_8		-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	34	52
	AN01		35	53
	AN02		36	54
	AN03		37	55
	AN04		38	56
	AN05		39	57
	AN06		-	58
	AN07		40	59
	AN08		44	63
	AN09		45	64
	AN10		-	65
	AN11		-	66
	AN12		-	67
	AN13		-	68
	AN14		-	69
	AN15		-	70

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	-	27
	TIOA0_1		10	19
	TIOA0_2		-	85
	TIOB0_0	Base timer ch.0 TIOB pin	22	40
	TIOB0_1		5	9
	TIOB0_2		-	86
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	-	28
	TIOA1_1		11	20
	TIOA1_2		-	5
	TIOB1_0	Base timer ch.1 TIOB pin	23	41
	TIOB1_1		6	10
	TIOB1_2		-	6
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	-	29
	TIOA2_1		12	21
	TIOA2_2		60	96
	TIOB2_0	Base timer ch.2 TIOB pin	24	42
	TIOB2_1		7	11
	TIOB2_2		59	95
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	-	30
	TIOA3_1		13	22
	TIOA3_2		-	90
	TIOB3_0	Base timer ch.3 TIOB pin	25	43
	TIOB3_1		8	12
	TIOB3_2		-	91
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	-	31
	TIOA4_1		14	23
	TIOA4_2		-	-
	TIOB4_0	Base timer ch.4 TIOB pin	26	44
	TIOB4_1		-	13
	TIOB4_2		-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	-	32
	TIOA5_1		15	24
	TIOA5_2		-	82
	TIOB5_0	Base timer ch.5 TIOB pin	27	45
	TIOB5_1		-	14
	TIOB5_2		-	83
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	56	89
	TIOB6_1	Base timer ch.6 TIOB pin	55	88
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	-	-
	TIOA7_1		46	71
	TIOA7_2		-	-
	TIOB7_0	Base timer ch.7 TIOB pin	-	-
	TIOB7_1		47	72
	TIOB7_2		-	-

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
Debugger	SWCLK	Serial wire debug interface clock input pin	50	78
	SWDIO	Serial wire debug interface data input / output pin	52	80
	SWO	Serial wire viewer output pin	53	81
	TRSTX	JTAG reset input pin	49	77
	TCK	JTAG test clock input pin	50	78
	TDI	JTAG test data input pin	51	79
	TMS	JTAG test mode state input/output pin	52	80
	TDO	JTAG debug data output pin	53	81
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2
	INT00_1		-	82
	INT00_2		54	87
	INT01_0	External interrupt request 01 input pin	3	3
	INT01_1		-	83
	INT02_0	External interrupt request 02 input pin	4	4
	INT02_1		35	53
	INT03_0	External interrupt request 03 input pin	-	93
	INT03_1		38	56
	INT03_2		5	9
	INT04_0	External interrupt request 04 input pin	8	12
	INT04_1		40	59
	INT04_2		6	10
	INT05_0	External interrupt request 05 input pin	-	74
	INT05_1		-	65
	INT05_2		7	11
	INT06_1	External interrupt request 06 input pin	48	73
	INT06_2		27	45
	INT07_2	External interrupt request 07 input pin	-	5
	INT08_1	External interrupt request 08 input pin	-	14
	INT08_2		-	8
	INT09_1	External interrupt request 09 input pin	-	15
	INT10_1	External interrupt request 10 input pin	-	16
	INT11_1	External interrupt request 11 input pin	-	17
	INT12_1	External interrupt request 12 input pin	-	27
	INT13_1	External interrupt request 13 input pin	-	28
	INT14_1	External interrupt request 14 input pin	-	39
	INT15_1	External interrupt request 15 input pin	60	96
	NMIX	Non-Maskable Interrupt input pin	57	92

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
GPIO	P00	General-purpose I/O port 0	49	77
	P01		50	78
	P02		51	79
	P03		52	80
	P04		53	81
	P05		-	82
	P06		-	83
	P07		-	84
	P08		-	85
	P09		-	86
	P0A		54	87
	P0B		55	88
	P0C		56	89
	P0D		-	90
	P0E		-	91
	P0F		57	92
	P10	General-purpose I/O port 1	34	52
	P11		35	53
	P12		36	54
	P13		37	55
	P14		38	56
	P15		39	57
	P16		-	58
	P17		40	59
	P18		44	63
	P19		45	64
	P1A		-	65
	P1B		-	66
	P1C		-	67
	P1D		-	68
	P1E		-	69
	P1F		-	70
	P20	General-purpose I/O port 2	-	74
	P21		48	73
	P22		47	72
	P23		46	71

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
GPIO	P30	General-purpose I/O port 3	5	9
	P31		6	10
	P32		7	11
	P33		8	12
	P34		-	13
	P35		-	14
	P36		-	15
	P37		-	16
	P38		-	17
	P39		9	18
	P3A		10	19
	P3B		11	20
	P3C		12	21
	P3D		13	22
	P3E		14	23
	P3F		15	24
	P40	General-purpose I/O port 4	-	27
	P41		-	28
	P42		-	29
	P43		-	30
	P44		-	31
	P45		-	32
	P46		19	36
	P47		20	37
	P48		-	39
	P49		22	40
	P4A		23	41
	P4B		24	42
	P4C		25	43
	P4D		26	44
	P4E		27	45
	P50	General-purpose I/O port 5	2	2
	P51		3	3
	P52		4	4
	P53		-	5
	P54		-	6
	P55		-	7
	P56		-	8
	P60	General-purpose I/O port 6	60	96
	P61		59	95
	P62		58	94
	P63		-	93
	P80	General-purpose I/O port 8	61	97
	P81		62	98
	P82		63	99
	PE0	General-purpose I/O port E	28	46
	PE2		30	48
	PE3		31	49

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	48	73
	SIN0_1		-	56
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0 when it is used in an I^2C (operation mode 4).	47	72
	SOT0_1 (SDA0_1)		-	57
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I^2C (operation mode 4).	46	71
	SCK0_1 (SCL0_1)		-	58
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	35	53
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I^2C (operation mode 4).	36	54
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I^2C (operation mode 4).	37	55
Multi-function Serial 2	SIN2_2	Multi-function serial interface ch.2 input pin	40	59
	SOT2_2 (SDA2_2)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I^2C (operation mode 4).	44	63
	SCK2_2 (SCL2_2)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I^2C (operation mode 4).	45	64

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	2	2
	SIN3_2		-	39
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I^2C (operation mode 4).	3	3
	SOT3_2 (SDA3_2)		-	40
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I^2C (operation mode 4).	4	4
	SCK3_2 (SCL3_2)		-	41
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	54	87
	SIN4_1		-	65
	SIN4_2		-	82
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I^2C (operation mode 4).	55	88
	SOT4_1 (SDA4_1)		-	66
	SOT4_2 (SDA4_2)		-	83
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I^2C (operation mode 4).	56	89
	SCK4_1 (SCL4_1)		-	67
	SCK4_2 (SCL4_2)		-	84
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	-	90
	RTS4_1		-	69
	RTS4_2		-	86
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	-	91
	CTS4_1		-	68
	CTS4_2		-	85

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	60	96
	SIN5_2		-	15
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I²C (operation mode 4).	59	95
	SOT5_2 (SDA5_2)		-	16
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I²C (operation mode 4).	58	94
	SCK5_2 (SCL5_2)		-	17
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	-	5
	SIN6_1		8	12
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I²C (operation mode 4).	-	6
	SOT6_1 (SDA6_1)		7	11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I²C (operation mode 4).	-	7
	SCK6_1 (SCL6_1)		6	10
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	27	45
	SIN7_2		61	97
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I²C (operation mode 4).	26	44
	SOT7_2 (SDA7_2)		62	98
	SCK7_1 (SCL7_1)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I²C (operation mode 4).	25	43
	SCK7_2 (SCL7_2)		63	99

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of Multi-function timer 0	9	18
	DTTI0X_1		-	69
	DTTI0X_2		59	95
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	-	13
	FRCK0_1		-	70
	FRCK0_2		35	53
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes a channel number.	-	17
	IC00_1		-	65
	IC00_2		36	54
	IC01_0		-	16
	IC01_1		-	66
	IC01_2		37	55
	IC02_0		-	15
	IC02_1		-	67
	IC02_2		38	56
	IC03_0		-	14
	IC03_1		-	68
	IC03_2		39	57
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	10	19
	RTO00_1 (PPG00_1)		-	71
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	11	20
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	12	21
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	13	22
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	14	23
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	15	24
	IGTRG	PPG IGBT mode external trigger input pin	24	42

Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
LCD Controller	VV0	LCD controller power supply I/O pin	-	6
	VV1		-	5
	VV2		-	4
	VV3		-	3
	VV4		2	2
	COM0	LCD controller common output pin	12	21
	COM1		11	20
	COM2		10	19
	COM3		9	18
	COM4		8	12
	COM5		7	11
	COM6		6	10
	COM7		5	9
	SEG00	LCD controller segment output pin	59	95
	SEG01		58	94
	SEG02		-	93
	SEG03		-	91
	SEG04		-	90
	SEG05		-	86
	SEG06		-	85
	SEG07		-	84
	SEG08		-	83
	SEG09		-	82
	SEG10		-	74
	SEG11		48	73
	SEG12		47	72
	SEG13		46	71
	SEG14		-	69
	SEG15		-	68
	SEG16		-	67
	SEG17		-	66
	SEG18		-	65
	SEG19		45	64
	SEG20		44	63
	SEG21		40	59
	SEG22		-	58
	SEG23		39	57
	SEG24		38	56
	SEG25		37	55
	SEG26		36	54
	SEG27		35	53
	SEG28		34	52
	SEG29		24	42
	SEG30		23	41
	SEG31		22	40
	SEG32		-	39
	SEG33		-	32
	SEG34		-	31
	SEG35		15	24

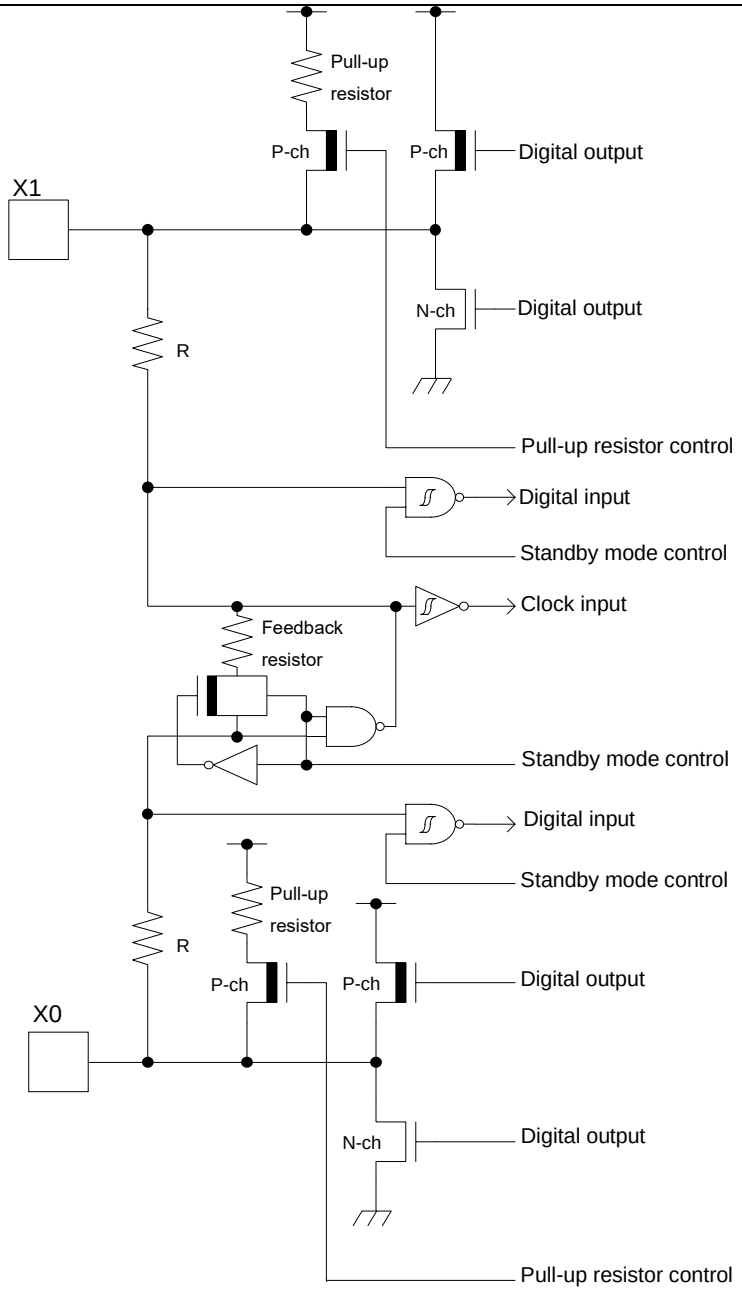
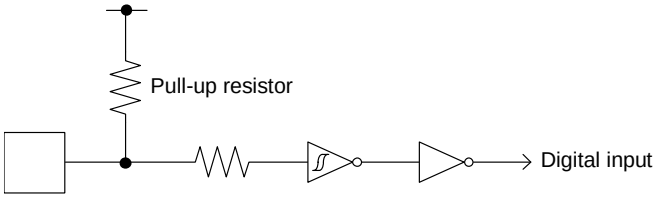
Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
LCD Controller	SEG36	LCD controller segment output pin	14	23
	SEG37		13	22
	SEG38		-	8
	SEG39		-	7
	SEG40		8	12
	SEG41		7	11
	SEG42		6	10
	SEG43		5	9
Real-time clock	RTCCO_0	Pulse output pin of Real-time clock	57	92
	RTCCO_1		37	55
	RTCCO_2		10	19
	SUBOUT_0	Sub clock output pin	57	92
	SUBOUT_1		37	55
	SUBOUT_2		10	19
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	57	92
	WKUP1	Deep standby mode return signal input pin 1	35	53
	WKUP2	Deep standby mode return signal input pin 2	48	73
	WKUP3	Deep standby mode return signal input pin 3	60	96
DAC	DA0	D/A converter ch.0 analog output pin	26	44
	DA1	D/A converter ch.1 analog output pin	27	45
HDMI-CEC/ Remote Control Reception	CEC0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	25	43
	CEC1	HDMI-CEC/Remote Control Reception ch.1 input/output pin	60	96

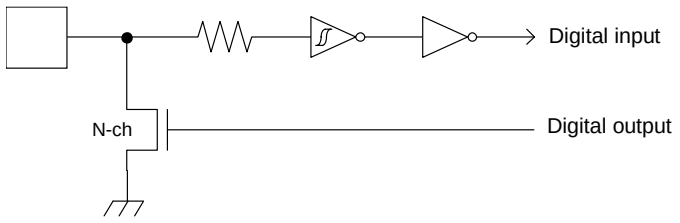
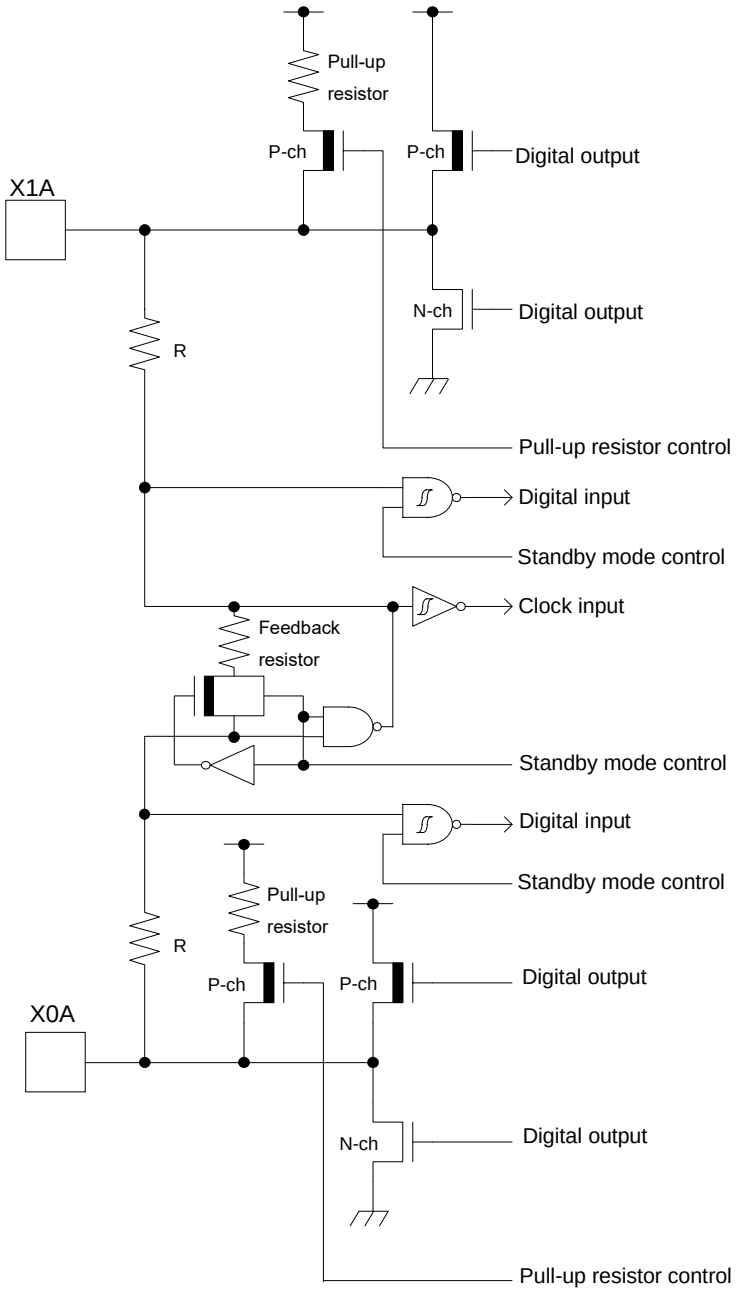
Pin function	Pin name	Function description	Pin No	
			LQFP-64	LQFP-100
Reset	INITX	External Reset Input Pin. A reset is valid when INITX = L.	21	38
Mode	MD0	Mode 0 pin. During normal operation, MD0 = L must be input. During serial programming to Flash memory, MD0 = H must be input.	29	47
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = L must be input.	28	46
Power	VCC	Power supply pin	1	1
	VCC		-	26
	VCC		18	35
	VCC		33	51
	VCC		-	76
GND	VSS	GND pin	16	25
	VSS		-	34
	VSS		32	50
	VSS		-	75
	VSS		64	100
Clock	X0	Main clock (oscillation) input pin	30	48
	X0A	Sub clock (oscillation) input pin	19	36
	X1	Main clock (oscillation) I/O pin	31	49
	X1A	Sub clock (oscillation) I/O pin	20	37
	CROUT_0	Built-in High-speed CR-osc clock output port	-	74
	CROUT_1		57	92
Analog Power	AVCC	A/D converter and D/A converter analog power supply pin	41	60
	AVRH	A/D converter analog reference voltage input pin	42	61
Analog GND	AVSS	A/D converter and D/A converter GND pin	43	62
C pin	C	Power supply stabilization capacity pin	17	33

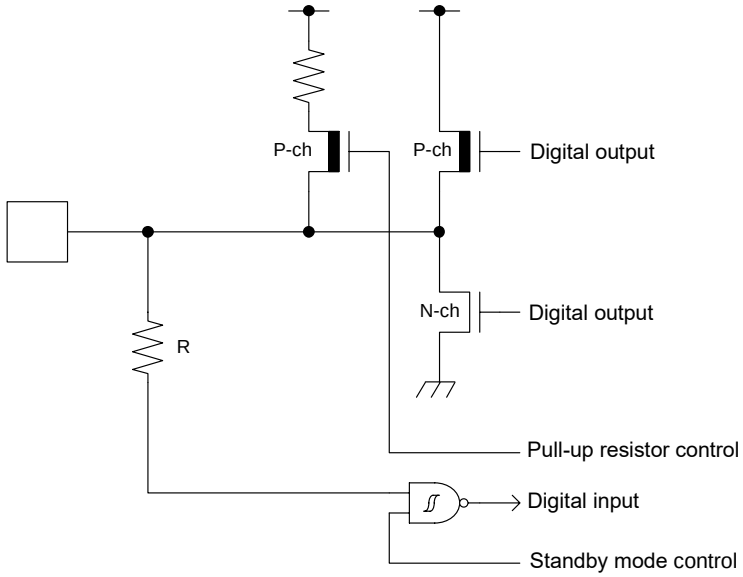
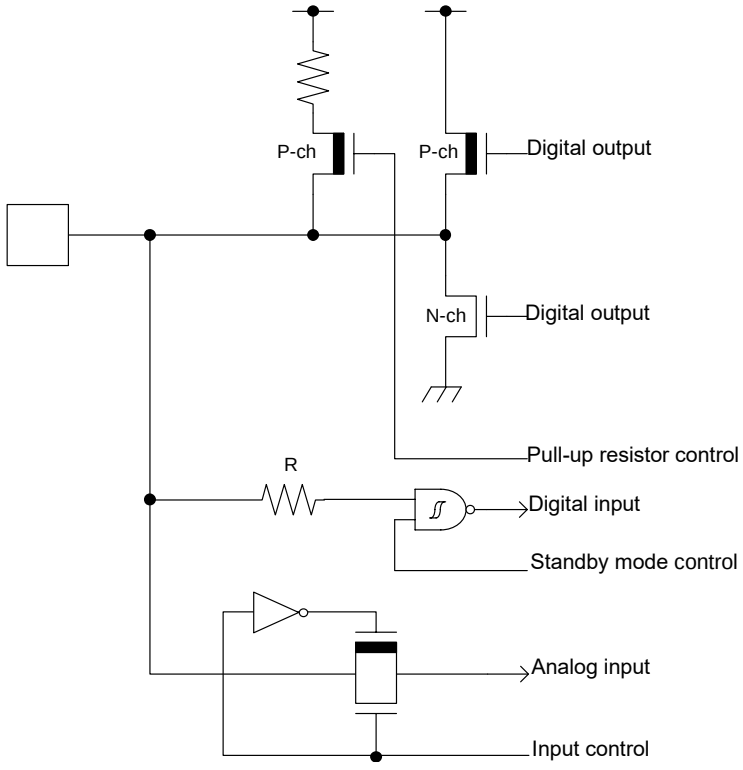
Note:

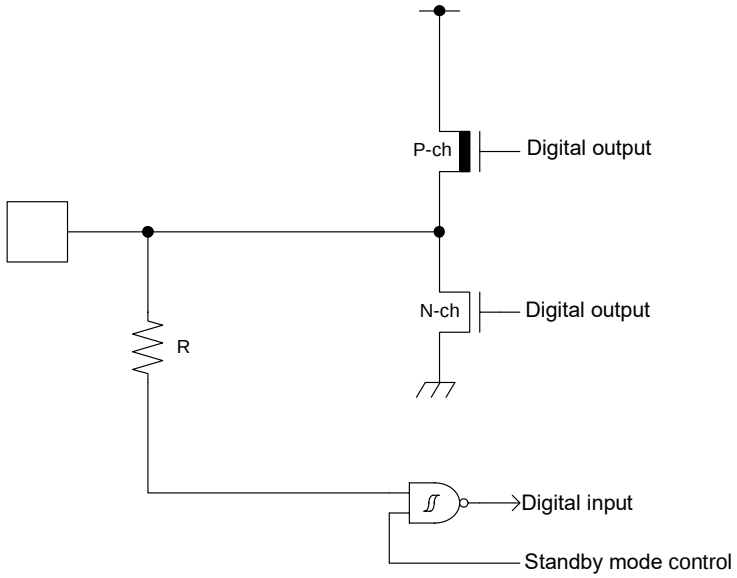
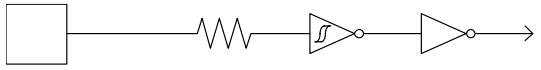
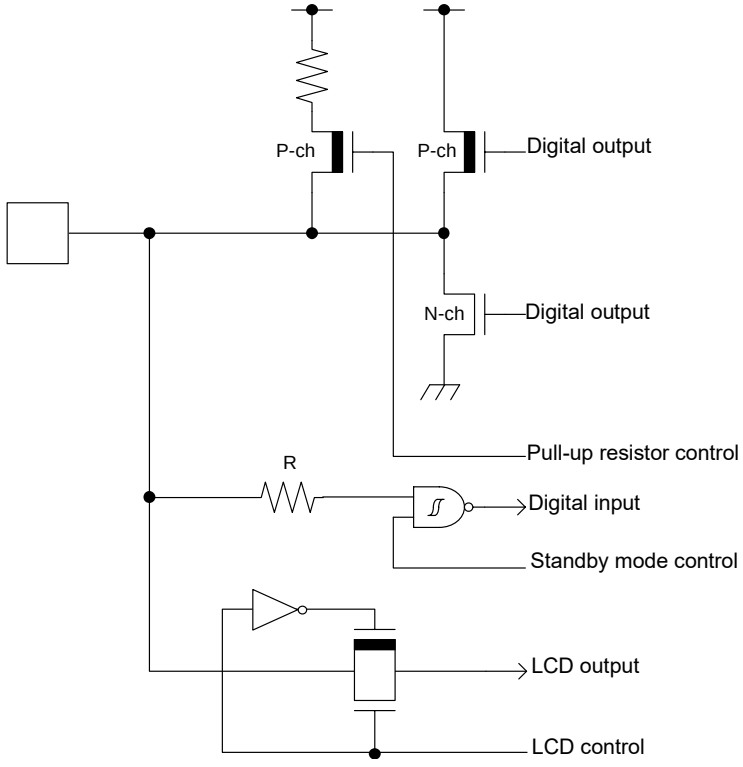
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

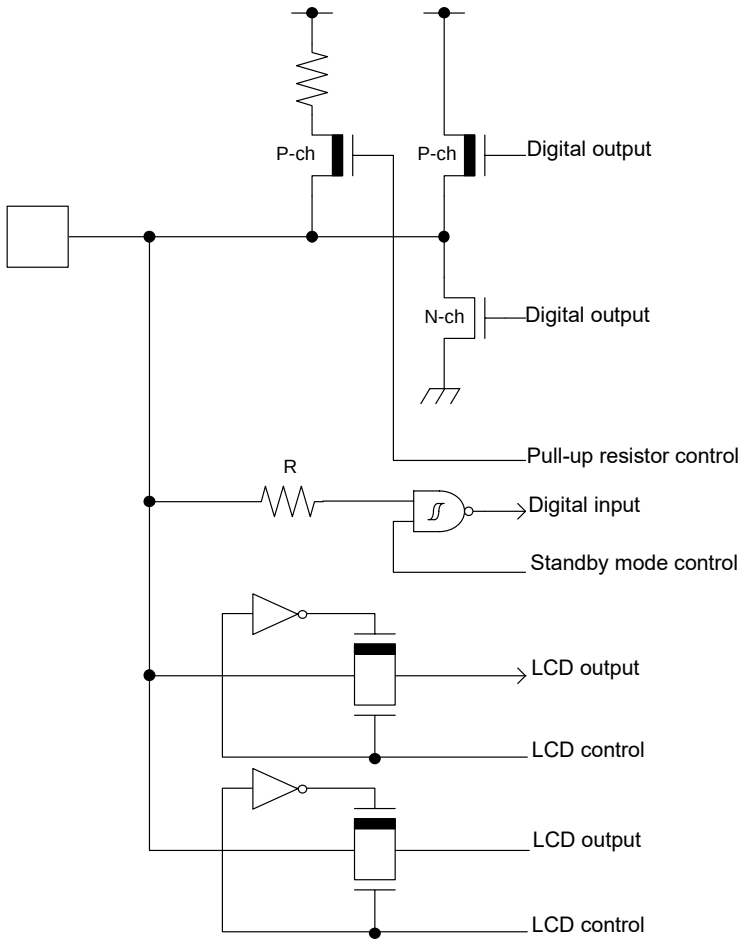
4. I/O Circuit Type

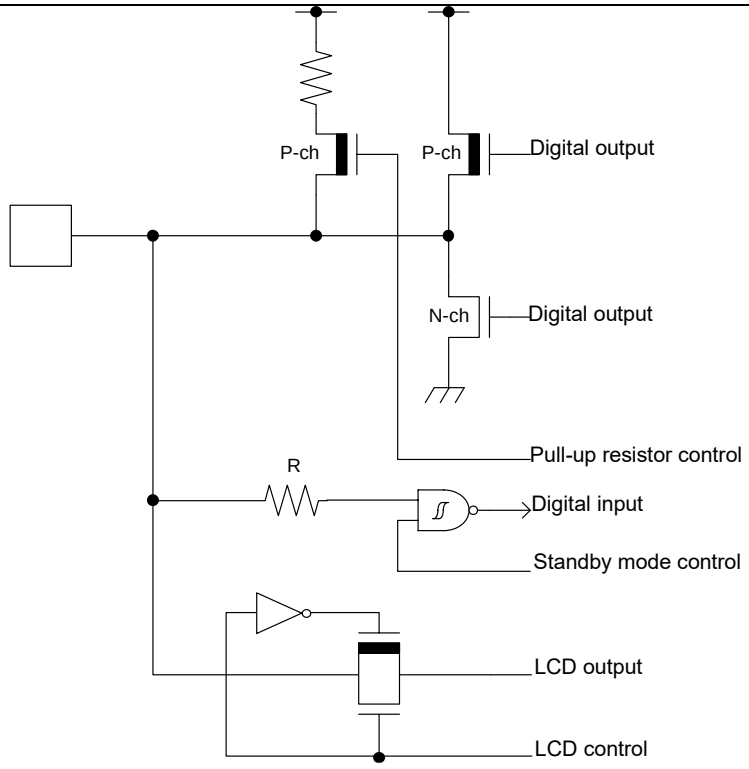
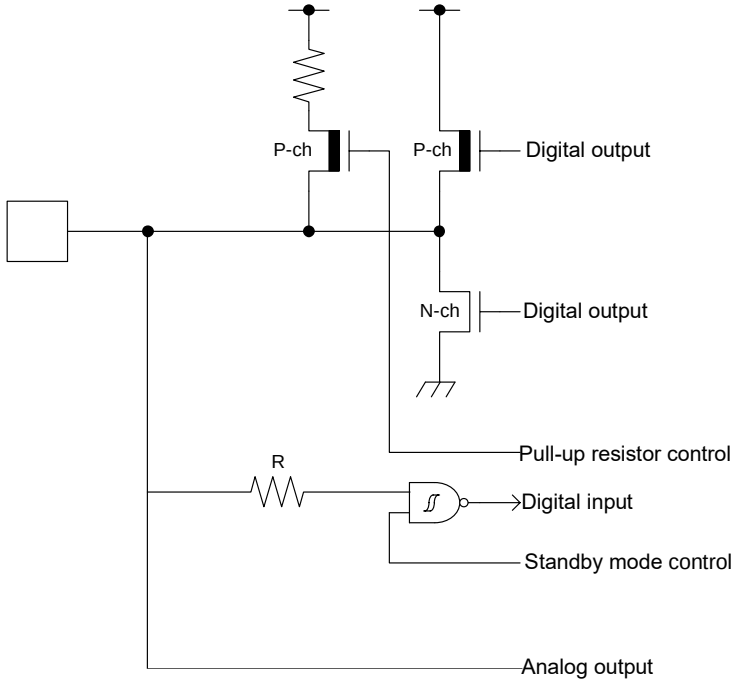
Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function. When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1 MΩ • With standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50 kΩ

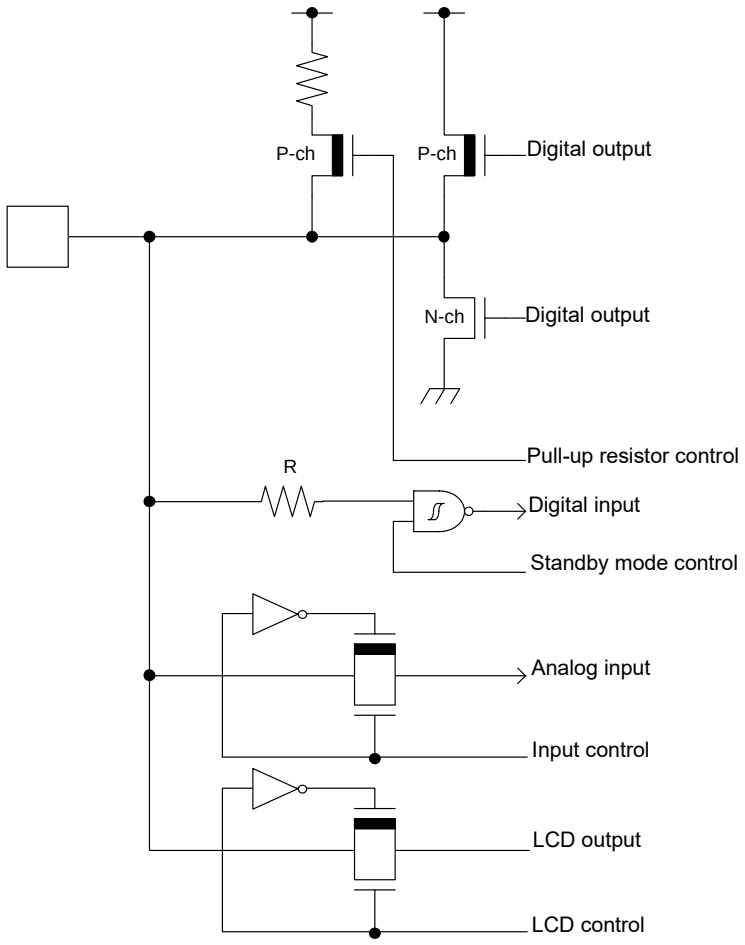
Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5 MΩ • With standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA

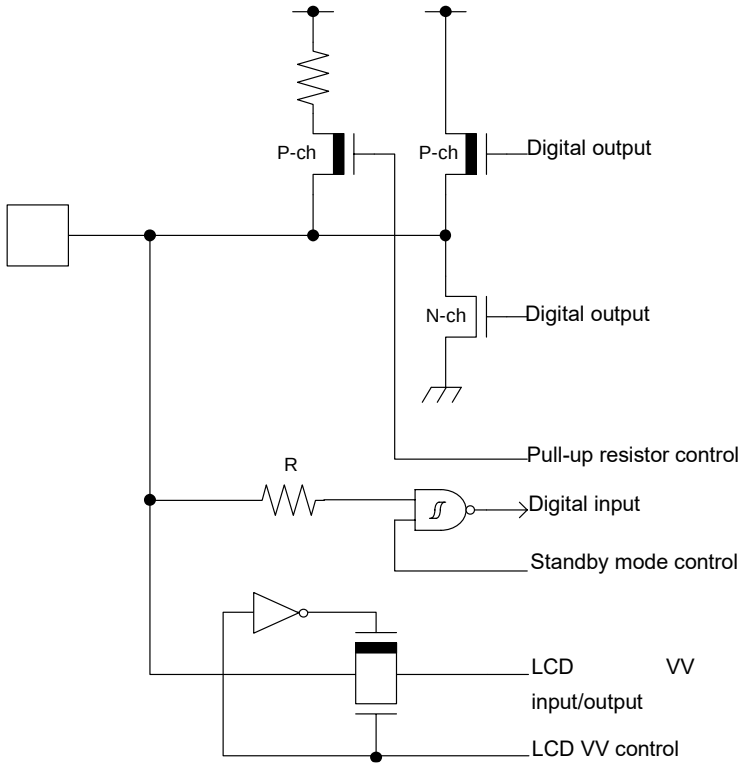
Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With standby mode control • 5 V tolerant input • I_{OH} = -4 mA, I_{OL} = 4 mA • Available to control PZR registers. P0B, P0C, P4C, P60, P81, P82 only. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
H		CMOS level hysteresis input
J		• CMOS level output • CMOS level hysteresis input • With input control • LCD segment output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
K		• CMOS level output • CMOS level hysteresis input • With input control • LCD common output • LCD segment output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
L		• CMOS level output • CMOS level hysteresis input • With input control • LCD common output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA
O		• CMOS level output • CMOS level hysteresis input • With input control • Analog output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
Q		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • LCD segment output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
R		• CMOS level output • CMOS level hysteresis input • With input control • LCD VV input/output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress Inc. recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress Inc. packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

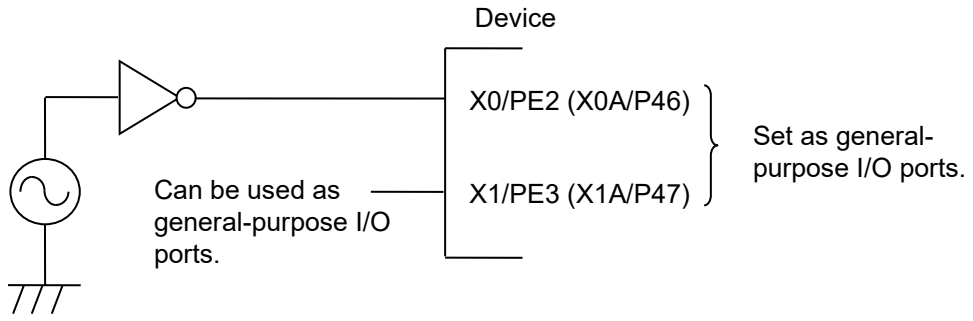
It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Using an external clock

To use the external clock, set general-purpose I/O ports to input the clock to X0/PE2 and X0A/P46 pin.

- Example of Using an External Clock

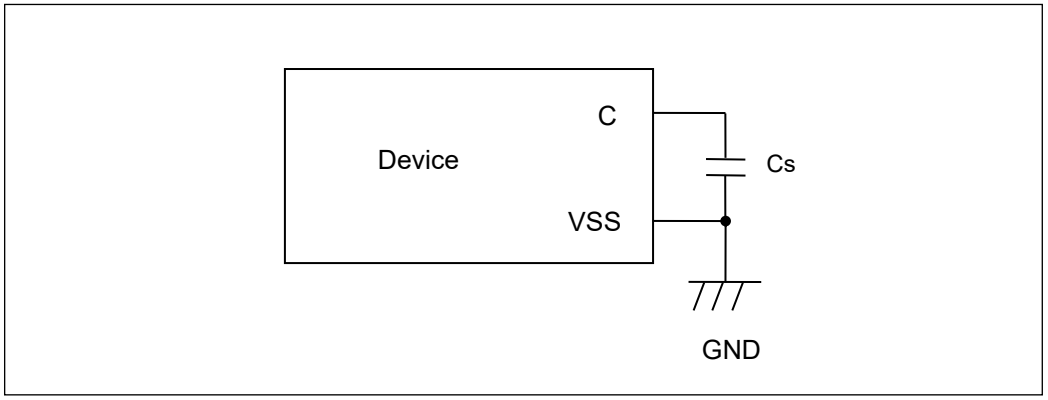


Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7µF would be recommended for this series.



Mode pins (MD0, MD1)

Connect the MD pin (MD0, MD1) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on: VCC → AVCC → AVRH

Turning off: AVRH → AVCC → VCC

Serial Communication

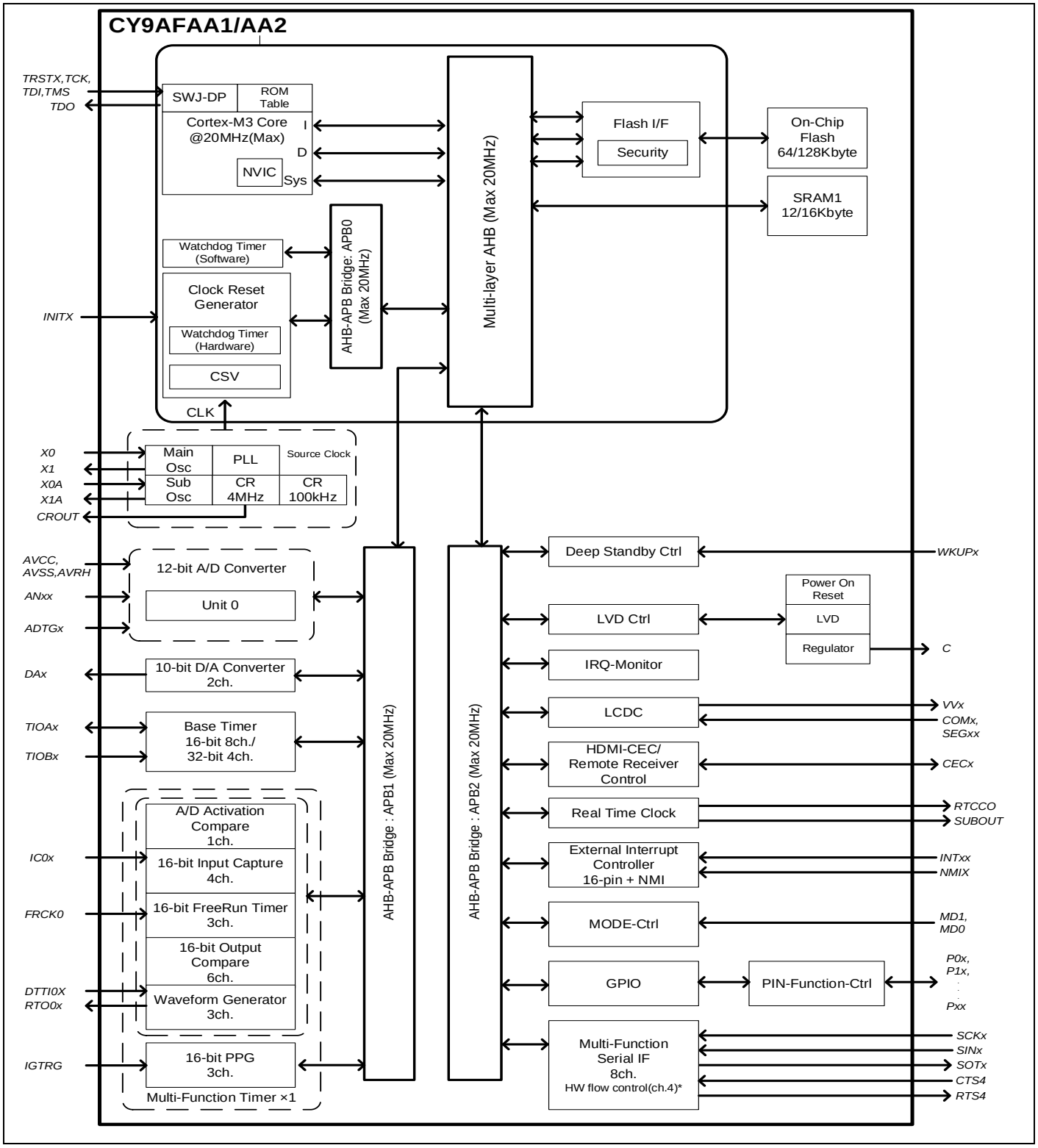
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash memory products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

7. Block Diagram



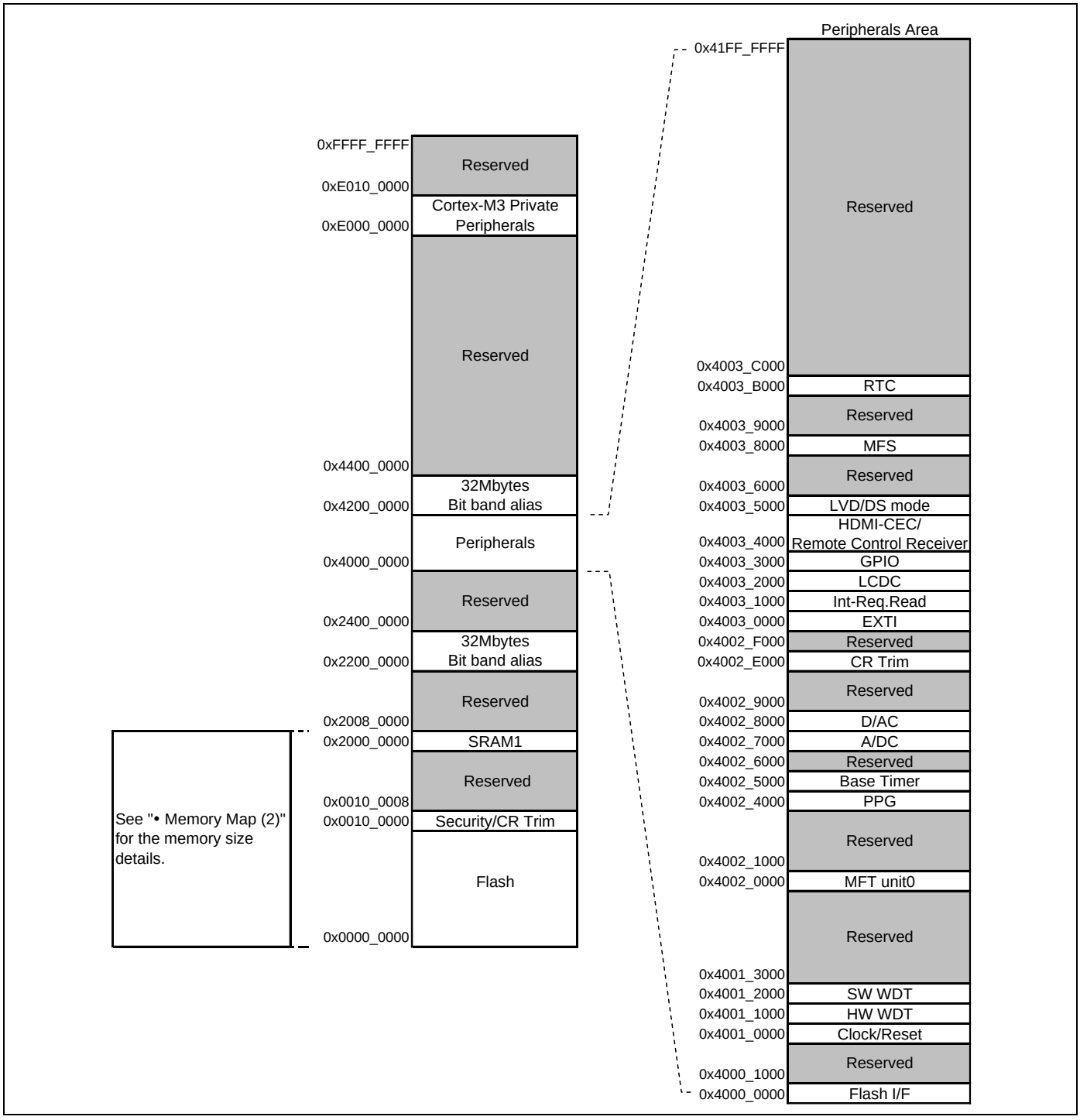
*: For the CY9AFAA1L and CY9AFAA2L, Multi-function Serial Interface does not support hardware flow control in these products.

8. Memory Size

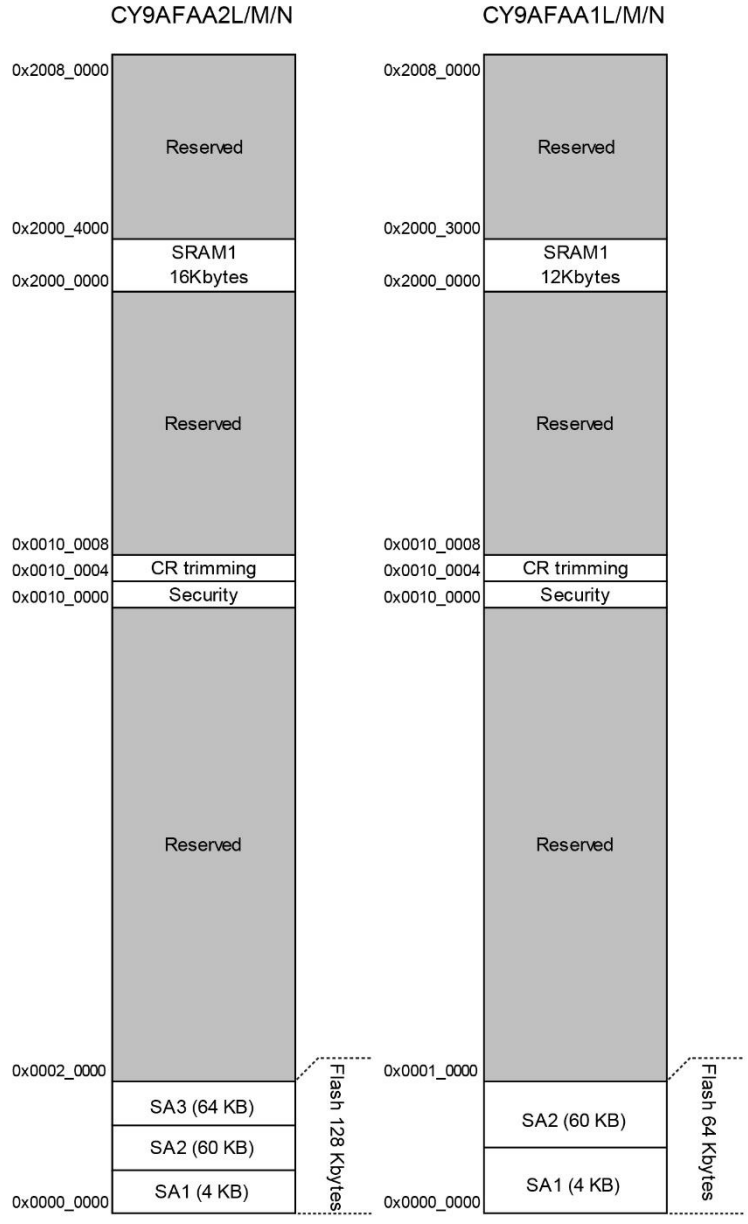
See Memory size in Product Lineup to confirm the memory size.

9. Memory Map

Memory Map (1)



Memory Map (2)



*: See CY 9AAA0N/1A0N/A30N/130N/130L SERIES, FLASH PROGRAMMING SPECIFICATIONS to confirm the detail of Flash memory.

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Reserved
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Reserved
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_8FFF		D/A Converter
0x4002_9000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt
0x4003_1000	0x4003_1FFF		Interrupt Source Check Register
0x4003_2000	0x4003_2FFF		LCD Controller
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/ Remote Control Receiver
0x4003_5000	0x4003_50FF		Low-Voltage Detector
0x4003_5100	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial
0x4003_9000	0x4003_9FFF		Reserved
0x4003_A000	0x4003_AFFF		Reserved
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_1FFF		Reserved
0x4006_2000	0x4006_2FFF		Reserved
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x41FF_FFFF		Reserved

10. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX = 0

  This is the period when the INITX pin is the L level.

- INITX = 1

  This is the period when the INITX pin is the H level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep Standby mode, pins switch to the general-purpose I/O port.

List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state / When oscillation stops*1, output maintains previous state / Internal input fixed at 0	Hi-Z / Input enabled / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state
B	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	Output maintain previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
F	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state
G	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled			Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
H	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state
I	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									Maintain previous state
J	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Output maintains previous state / Internal input fixed at 0

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0
	Resource other than above selected						Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0		Output maintains previous state / Internal input fixed at 0
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected Internal input fixed at 0
	External interrupt enabled selected						Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected						Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0		Output maintains previous state / Internal input fixed at 0
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
M	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state / When oscillation stops*2, output maintains previous state / Internal input fixed at 0	Hi-Z / Input enabled / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, output maintains previous state / Internal input fixed at 0	Hi-Z / Input enabled / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When Return from Deep Standby STOP mode, GPIO is selected
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state
N	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
O	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0		Maintain previous state
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	Maintain previous state	Hi-Z / Input enabled	Maintain previous state
Q	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
R	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected						Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state
S	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Output maintains previous state / Internal input fixed at 0

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
T	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected Internal input fixed at "0"
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled			Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Output maintains previous state / Internal input fixed at 0
U	Resource selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Output maintains previous state / Internal input fixed at 0
V	Resource selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0
	GPIO selected							Output maintains previous state / Internal input fixed at 0		

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
W	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		
X	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state
Y	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled		Maintain previous state	Maintain previous state			
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
Z	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled		Maintain previous state	Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state

*1: Oscillation is stopped at Sub Run mode, Low-speed CR Run mode, Sub Sleep mode, Low-speed CR Sleep mode, Sub Timer mode, Low-speed CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Oscillation is stopped at Stop mode and Deep Standby Stop mode.

*3: Maintain previous state at Timer mode. GPIO selected Internal input fixed at 0 at RTC mode, Stop mode.

*4: Maintain previous state at Timer mode. Hi-Z/Internal input fixed at 0 at RTC mode, Stop mode.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V_{CC}	Vss - 0.5	Vss + 6.5	V	
Analog power supply voltage*1,*3	AV_{CC}	Vss - 0.5	Vss + 6.5	V	
Analog reference voltage*1,*3	AVRH	Vss - 0.5	Vss + 6.5	V	
LCD input voltage*1,*3	VV4 to VV0	Vss - 0.5	Vss + 6.5	V	
Input voltage*1	V_I	Vss - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		Vss - 0.5	Vss + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	Vss - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	Vss - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current*4	I_{OL}	-	10	mA	
L level average output current*5	I_{OLAV}	-	4	mA	
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*4	I_{OH}	-	-10	mA	
H level average output current*5	I_{OHAV}	-	- 4	mA	
H level total maximum output current	$\sum I_{OH}$	-	-100	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	-50	mA	
Power consumption	P_D	-	400	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that Vss = AVss = 0 V.

*2: V_{CC} must not drop below Vss - 0.5 V.

*3: Be careful not to exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

WARNING:

– *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
Do not exceed any of these ratings.

11.2 Recommended Operating Conditions

(Vss = AVss = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	1.8	5.5	V	*1
				2.2	5.5		*2
LCD input voltage		VV4	-	2.2	V_{CC}	V	
Analog power supply voltage		AV_{CC}	-	1.8	5.5	V	$AV_{CC} = V_{CC}$
Analog reference voltage		AVRH	-	2.7	AV_{CC}	V	$AV_{CC} \geq 2.7$ V
				AV_{CC}			$AV_{CC} < 2.7$ V
Smoothing capacitor		C_S	-	1	10	µF	For built-in Regulator *3
Operating Temperature	LQD064, LQG064, LQH080, LQJ080, LQI100, PQH100	T_A	-	- 40	+ 85	°C	

*1: When LCD is not used

*2: When LCD is used

*3: See C Pin in Handling Devices for the smoothing capacitor.

WARNING:

– *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

11.3 DC Characteristics

11.3.1 Current Rating

(V_{CC} = AV_{CC} = 1.8V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*3	Max*4		
Power supply current	I_{CC}	VCC	PLL Run mode	CPU: 20 MHz, Peripheral: 20 MHz, Flash memory 0 Wait, FRWTR.RWT = 00, FSYNDN.SD = 000	19	24	mA	*1, *5
				CPU: 20 MHz, Peripheral: clock stopped, NOP operation	9.5	12.5	mA	*1, *5
			High-speed CR Run mode	CPU/Peripheral: 4 MHz*2 Flash memory 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	4.5	5	mA	*1
			Sub Run mode	CPU/Peripheral: 32 kHz, Flash memory 0 Wait, FRWTR.RWT = 00, FSYNDN.SD = 000	0.25	0.55	mA	*1, *6
			Low-speed CR Run mode	CPU/Peripheral: 100 kHz, Flash memory 0 Wait, FRWTR.RWT = 00, FSYNDN.SD = 000	0.3	0.95	mA	*1
	I_{CCS}		PLL Sleep mode	Peripheral: 20 MHz	8	10.5	mA	*1, *5
			High-speed CR Sleep mode	Peripheral: 4 MHz*2	2	2.5	mA	*1
			Sub Sleep mode	Peripheral: 32 kHz	0.2	0.45	mA	*1, *6
			Low-speed CR Sleep mode	Peripheral: 100 kHz	0.25	0.65	mA	*1

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: T_A=+25°C, V_{CC}=3.3 V

*4: T_A=+85°C, V_{CC}=5.5 V

*5: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*3		
Power supply current	I_{CCT}	VCC	Main Timer mode	T_A = + 25°C, When LVD is off	0.9	3.3	mA	*1, *4
				T_A = + 85°C, When LVD is off	1.5	3.5	mA	*1, *4
			Sub Timer mode	T_A = + 25°C, When LVD is off	7.5	60	µA	*1, *5
				T_A = + 85°C, When LVD is off	16	150	µA	*1, *5
	I_{CCR}		RTC mode	T_A = + 25°C, When LVD is off	1.5	6.5	µA	*1, *5
				T_A = + 85°C, When LVD is off	6	79	µA	*1, *5
	I_{CCH}		Stop mode	T_A = + 25°C, When LVD is off	0.6	5	µA	*1
				T_A = + 85°C, When LVD is off	4.2	77	µA	*1
	I_{CCRD}		Deep Standby RTC mode	T_A = + 25°C, When LVD is off	1.3	4.5	µA	*1, *5
				T_A = + 85°C, When LVD is off	3	22	µA	*1, *5
	I_{CCHD}		Deep Standby Stop mode	T_A = + 25°C, When LVD is off	0.4	3	µA	*1
				T_A = + 85°C, When LVD is off	1.4	20	µA	*1

*1: When all ports are fixed.

*2: V_{CC}=3.3 V

*3: V_{CC}=5.5 V

*4: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*5: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Low Voltage Detection Current

(V_{CC} = AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ*	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	For occurrence of reset or for occurrence of interrupt in normal mode operation	10	20	µA	When not detected
			For occurrence of reset and for occurrence of interrupt in normal mode operation	14	30	µA	
			For occurrence of interrupt in low-power mode operation	0.3	2	µA	When not detected

*: When V_{CC}=3.3V

Flash Memory Current

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	10.8	11.9	mA	

A/D Converter Current

(V_{CC} = AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	1.4	2.5	mA	
			At stop	0.1	0.35	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	0.5	1.5	mA	
			At stop	0.1	0.3	µA	

D/A Converter Current

(V_{CC} = AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{DDA}	AVCC	At D/A 1ch. operation AV_{CC}=3.3 V	314	440	µA	*1, *2
			At D/A 1ch. operation AV_{CC}=5.0 V	476	670	µA	*1, *2
	I_{DSA}		At D/A stop	-	1.0	µA	*1

*1: No-load

*2: Generates the max current by the CODE about 0x200

11.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 1.8V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	MD0, MD1 PE0, PE2, PE3, P46, P47, P3A, P3B, P3C, P3D, P3E, P3F, INITX	-	V_{CC}× 0.8	-	V_{CC}+ 0.3	V	
		P0A, P0B, P0C, P4C, P60, P80, P81, P82	-	V_{CC}× 0.7	-	V_{SS}+ 5.5	V	5V tolerant
		CMOS hysteresis input pins other than the above	-	V_{CC}× 0.7	-	V_{CC}+ 0.3	V	
L level input voltage (hysteresis input)	V_{ILS}	MD0, MD1 PE0, PE2, PE3, P46, P47, INITX	-	V_{SS}- 0.3	-	V_{CC}× 0.2	V	
		CMOS hysteresis input pins other than the above	-	V_{SS}- 0.3	-	V_{CC}× 0.3	V	
H level output voltage	V_{OH}	Pxx	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC}- 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 1 mA					
L level output voltage	V_{OL}	Pxx	V_{CC} ≥ 4.5 V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 2 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
		CEC0, CEC1	V_{CC} = AV_{CC} = AVRH = V_{SS} = AV_{SS} = 0.0 V	-	-	+ 1.8		
Pull-up resistor value	R_{PU}	Pull-up pin	V_{CC} ≥ 4.5 V	25	50	100	kΩ	
			V_{CC} < 4.5 V	40	100	400		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

11.3.3 LCD Characteristics

(V_{CC} = 2.2V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
VV0 to VV3 Output voltage (1/4 bias)	V_{VV0}	VV0	When using internal dividing register	0	-	V_{VV4} × 5%	V	
	V_{VV1}	VV1		V_{VV4} × 1/4 -10%	-	V_{VV4} × 1/4 +10%		
	V_{VV2}	VV2		V_{VV4} × 1/2 -10%	-	V_{VV4} × 1/2 +10%		
	V_{VV3}	VV3		V_{VV4} × 3/4 -10%	-	V_{VV4} × 3/4 +10%		
VV0 to VV3 Output voltage (1/3 bias)	V_{VV0}	VV0	When using internal dividing register	0	-	V_{VV4} × 5%	V	
	V_{VV1}	VV1		V_{VV4} × 1/3 -10%	-	V_{VV4} × 1/3 +10%		
	V_{VV2}	VV2		V_{VV4} × 2/3 -10%	-	V_{VV4} × 2/3 +10%		
	V_{VV3}	VV3		V_{VV4} × 2/3 -10%	-	V_{VV4} × 2/3 +10%		
VV0 to VV3 Output voltage (1/2 bias)	V_{VV0}	VV0	When using internal dividing register	0	-	V_{VV4} × 5%	V	
	V_{VV1}	VV1		V_{VV4} × 1/2 -10%	-	V_{VV4} × 1/2 +10%		
	V_{VV2}	VV2		V_{VV4} × 1/2 -10%	-	V_{VV4} × 1/2 +10%		
	V_{VV3}	VV3		V_{VV4} × 1/2 -10%	-	V_{VV4} × 1/2 +10%		
VV4 Active current (1/4 bias)	I_{R100K}	VV4	When using 100 kΩ internal dividing register	-	15	35	µA	
	I_{R10K}	VV4	When using 10 kΩ internal dividing register	-	130	250	µA	
VV4 Active current (1/3 bias)	I_{R100K}	VV4	When using 100 kΩ internal dividing register	-	18	45	µA	
	I_{R10K}	VV4	When using 10 kΩ internal dividing register	-	170	350	µA	
VV4 Active current (1/2 bias)	I_{R100K}	VV4	When using 100 kΩ internal dividing register	-	27	75	µA	
	I_{R10K}	VV4	When using 10 kΩ internal dividing register	-	250	500	µA	
VV4 Static current	Ioff_vv4	VV4	When LCD stops	-	-	0.5	µA	
VV0 Output Voltage in using external resistor	V_{VV0E}	VV0	I_{OL}=1mA	-	-	1.0	V	

11.4 AC Characteristics

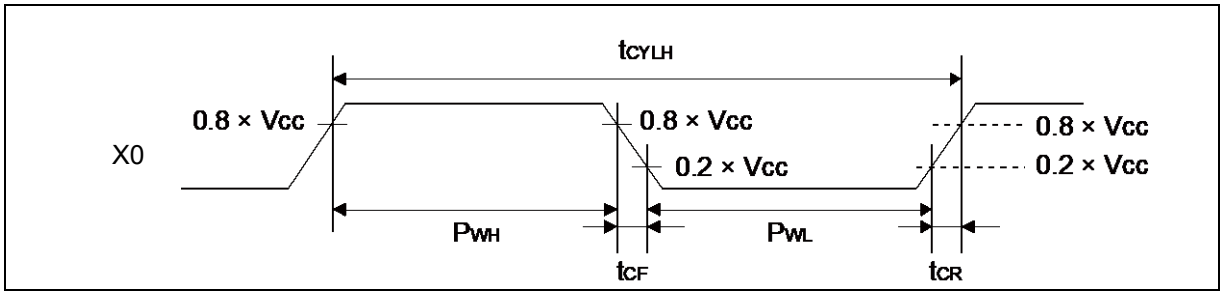
11.4.1 Main Clock Input Characteristics

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 2.0$ V	4	20	MHz	When crystal oscillator is connected
			$V_{CC} < 2.0$ V	4	4	MHz	
			$V_{CC} \geq 4.5$ V	4	20	MHz	When using external clock
			$V_{CC} < 4.5$ V	4	16	MHz	
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5$ V	50	250	ns	When using external clock
			$V_{CC} < 4.5$ V	62.5	250	ns	
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
	f_{CM}	-	-	-	20	MHz	Master clock
	f_{CC}	-	-	-	20	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	20	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	20	MHz	APB1 bus clock*2
	f_{CP2}	-		-	20	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	50	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	50	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	50	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	50	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

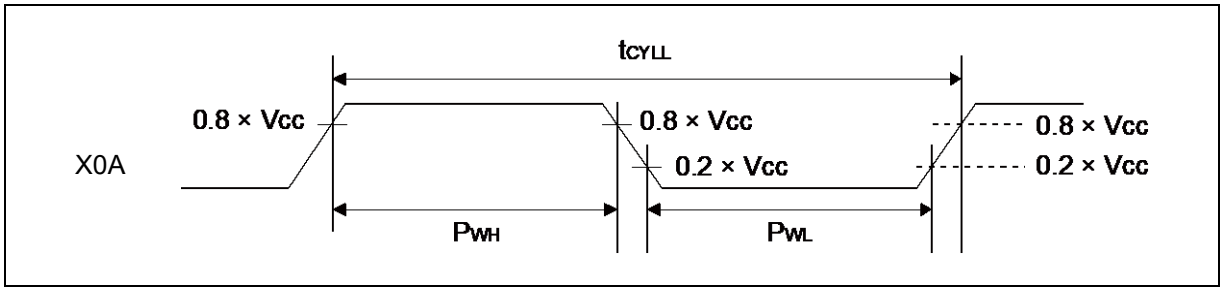
*2: For about each APB bus which each peripheral is connected to, see Block Diagram in this data sheet.



11.4.2 Sub Clock Input Characteristics

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



11.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions		Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_{CRH}	$V_{CC} \geq$ 2.2 V	T_A = + 25°C	3.92	4	4.08	MHz	When trimming*1
			T_A = - 40°C to + 85°C	3.8	4	4.2		
			T_A = - 40°C to + 85°C	2.3	-	7.03		When not trimming
		V_{CC} < 2.2 V	T_A = + 25°C	3.4	4	4.6	MHz	When trimming*1
			T_A = - 40°C to + 85°C	3.16	4	4.84		
			T_A = - 40°C to + 85°C	2.3	-	7.03		When not trimming
Frequency stabilization time	t_{CRWT}	-		-	-	10	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

*2: This is the time to stabilize the frequency of High-speed CR clock after setting trimming value. This period is able to use High-speed CR clock as source clock.

Built-in Low-speed CR

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

11.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	20	MHz	
PLL multiplication rate	-	1	-	5	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	10	-	20	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	20	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

11.4.5 Operating Conditions of Main PLL (In the case of using the built-in High-speed CR for the input clock of the Main PLL)

(V_{CC} = 2.2V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	3	-	4	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	11.4	-	16.8	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	16.8	MHz	

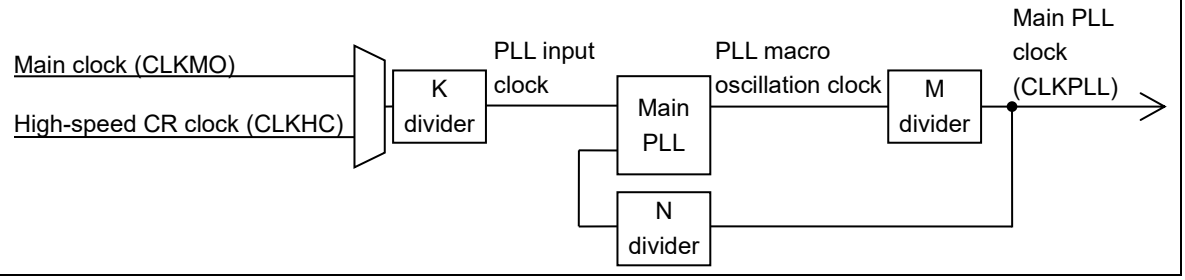
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

Note:

− *Make sure to input to the Main PLL source clock, the High-speed CR clock (CLKHC) that the frequency has been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.*

Main PLL connection



11.4.6 Reset Input Characteristics

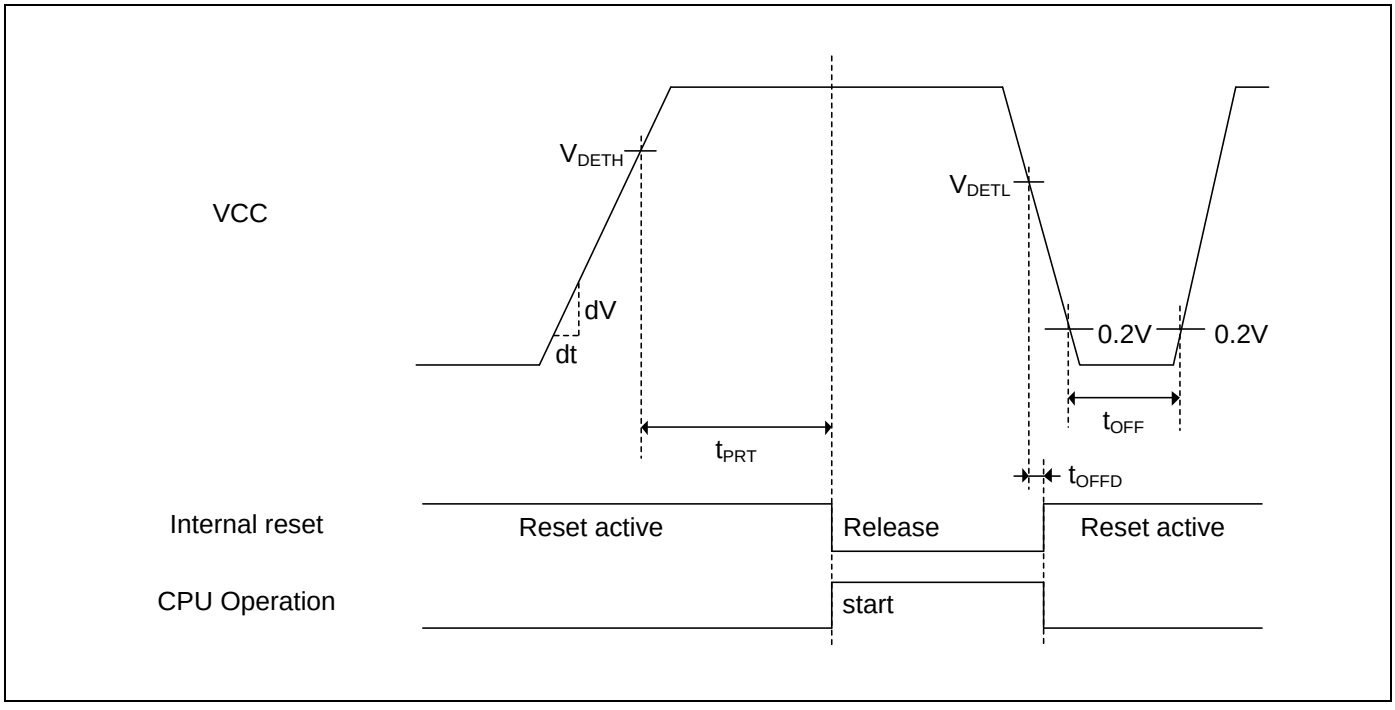
(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	
				1.5	-	ms	When RTC mode or Stop mode
				1.5	-	ms	When Deep Standby mode

11.4.7 Power-on Reset Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	VCC	0.1	-	-	V/ms	
Power supply shut down time	t_{OFF}		1	-	-	ms	
Reset release voltage	V_{DETH}		1.44	1.60	1.76	V	When voltage rises
Reset detection voltage	V_{DETL}		1.39	1.55	1.71	V	When voltage drops
Time until releasing Power-on reset	t_{PRT}		0.46	-	11.4	ms	dV/dt ≥ 0.1mV/µs
Reset detection delay time	t_{OFFD}		-	-	0.4	ms	dV/dt ≥ -0.04mV/µs

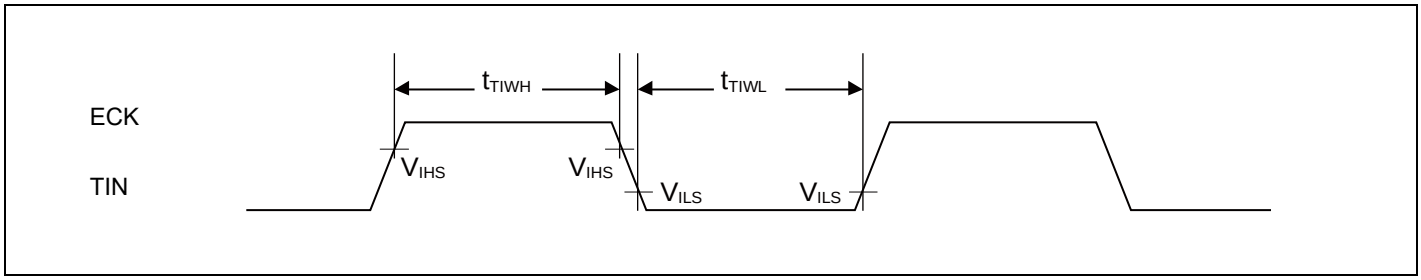


11.4.8 Base Timer Input Timing

Timer input timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

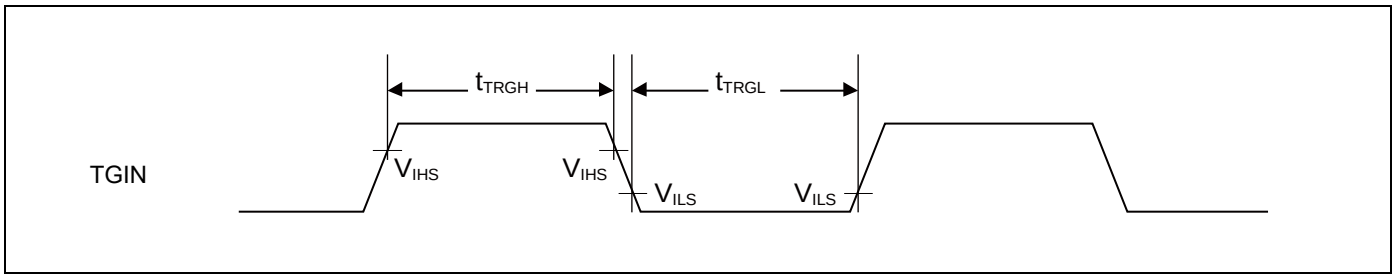
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which the Base Timer is connected to, see Block Diagram in this data sheet.

11.4.9 CSIO/UART Timing

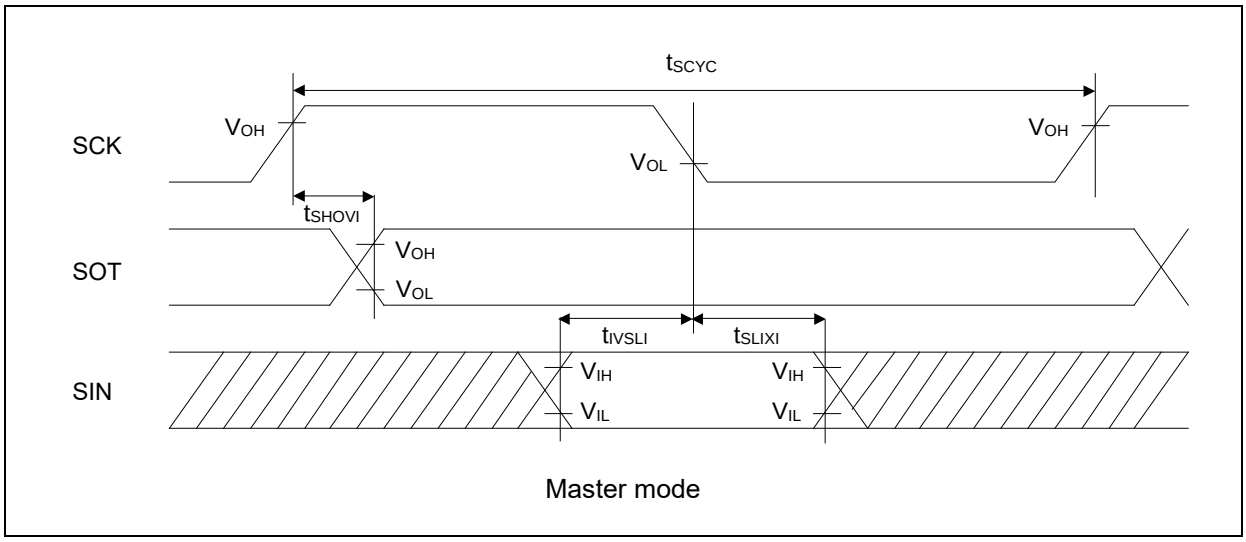
CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

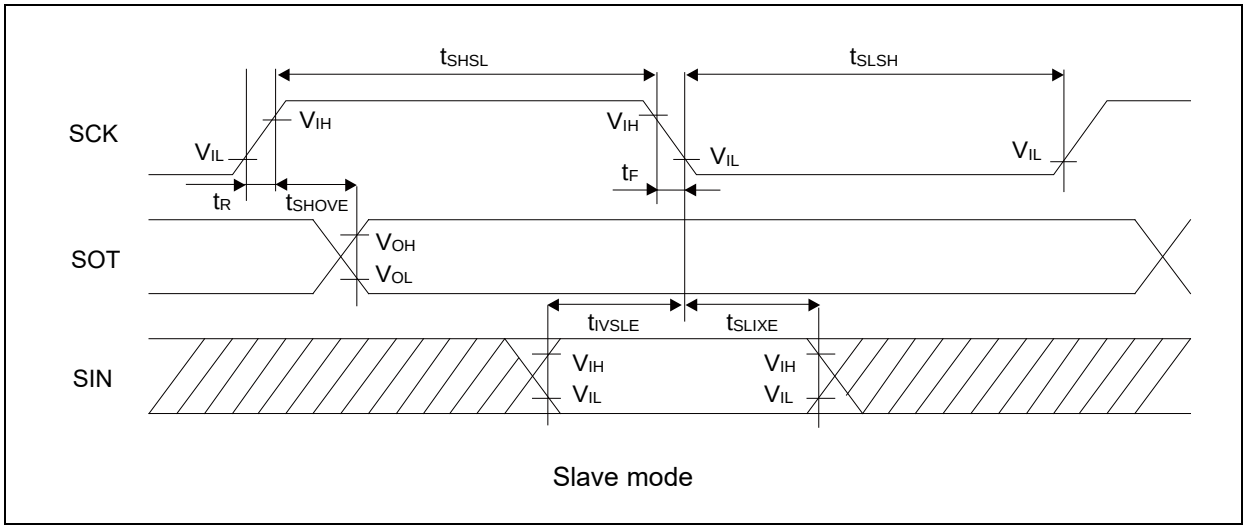
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		2.7 V ≤V_{CC}< 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	Min	Max	
Baud rate	-	-	-	-	5	-	5	-	5	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ -10	-	$2t_{CYCP}$ -10	-	$2t_{CYCP}$ -10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	75	-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 50 pF.*



Master mode



Slave mode

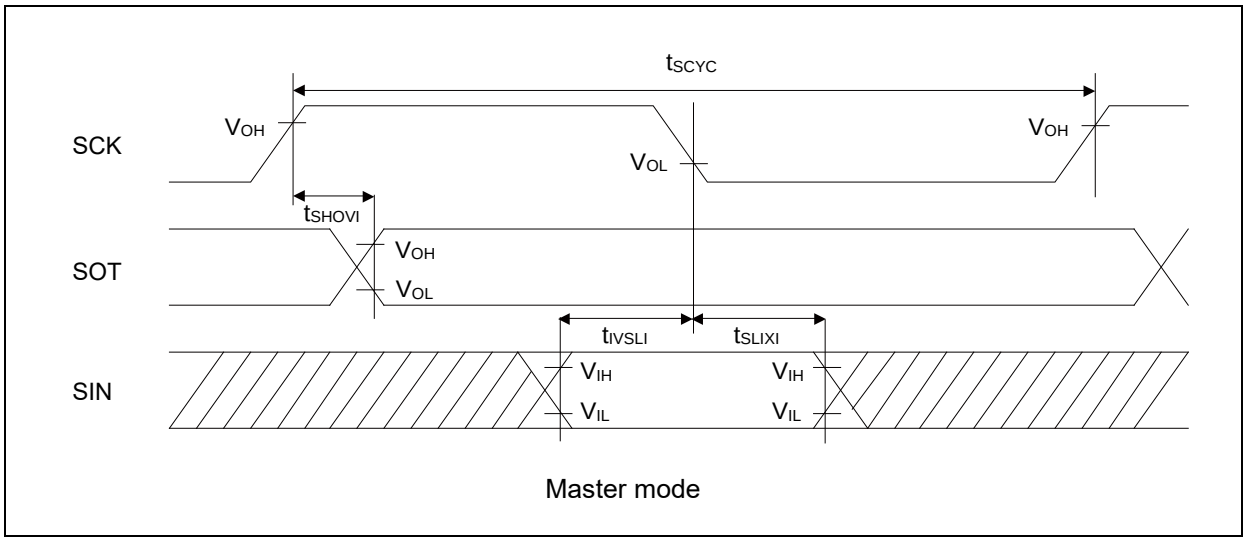
CSIO (SPI = 0, SCINV = 1)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

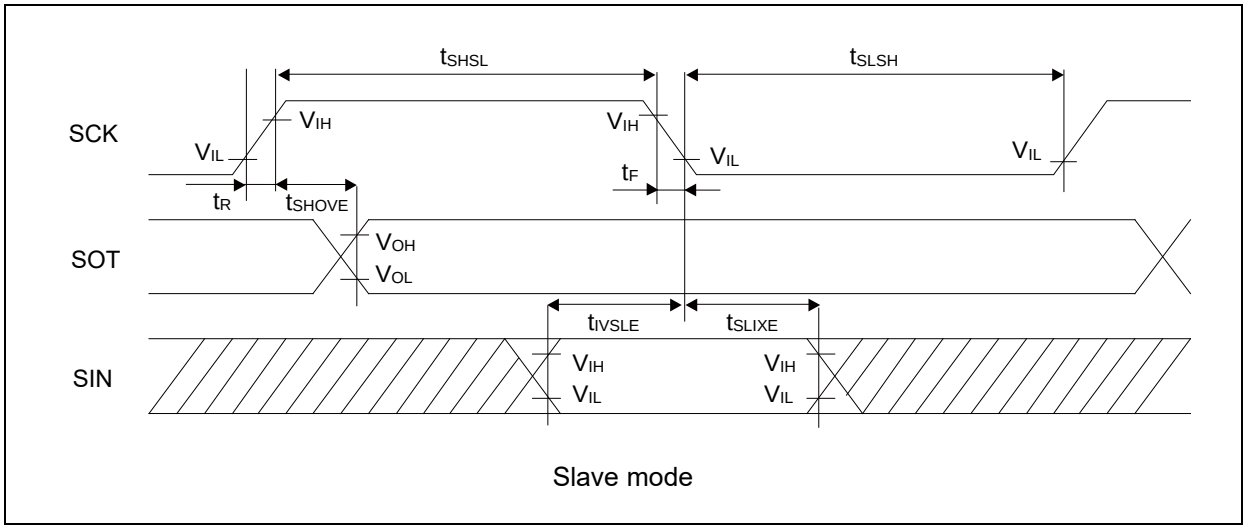
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		2.7 V ≤ V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	Min	Max	
Baud rate	-	-	-	-	5	-	5	-	5	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	75	-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 50 pF.*



Master mode



Slave mode

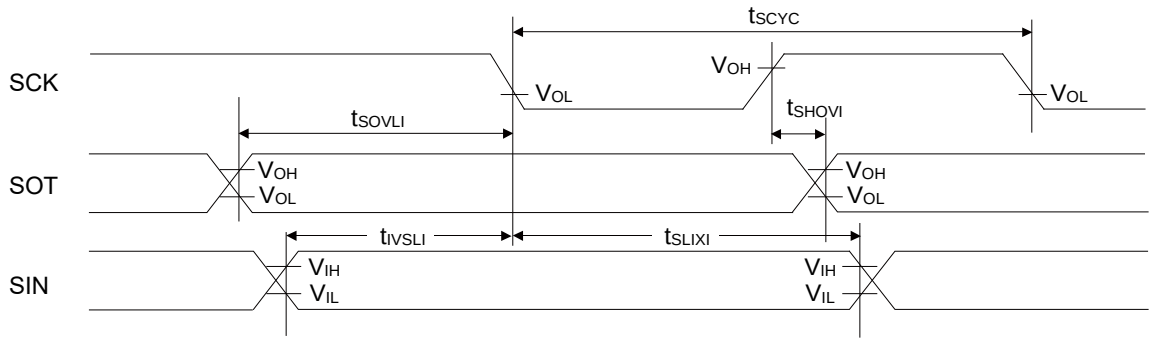
CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

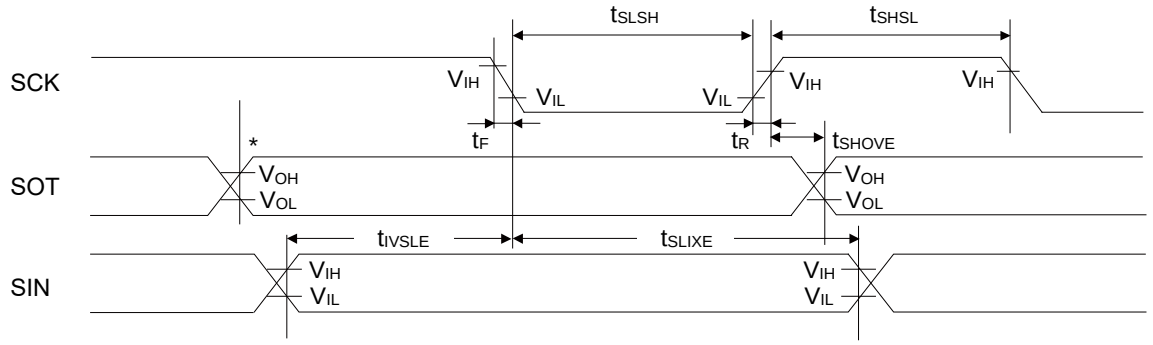
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		2.7 V ≤ V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	Min	Max	
Baud rate	-	-	-	-	5	-	5	-	5	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	75	-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 50 pF.*



Master mode



Slave mode

*: Changes when writing to TDR register

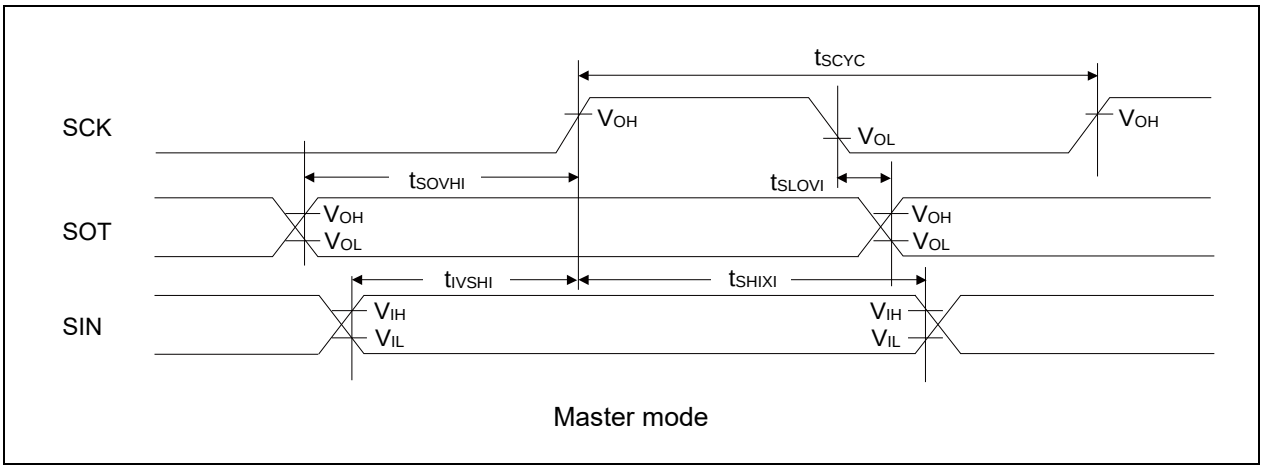
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

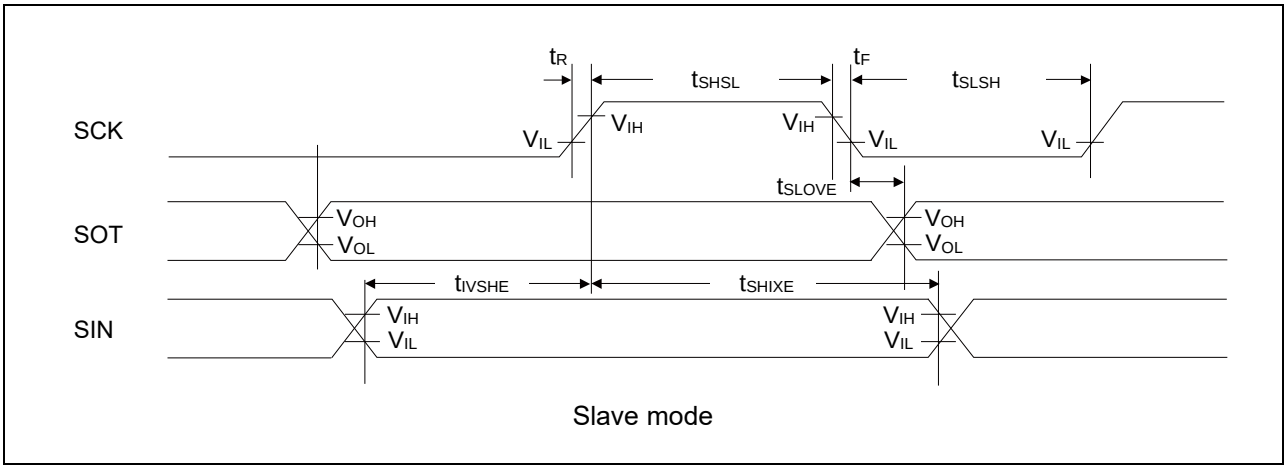
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		2.7 V ≦ V_{CC} < 4.5 V		V_{CC} ≧ 4.5 V		Unit
				Min	Max	Min	Max	Min	Max	
Baud rate	-	-	-	-	5	-	5	-	5	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	75	-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 50 pF.*



Master mode

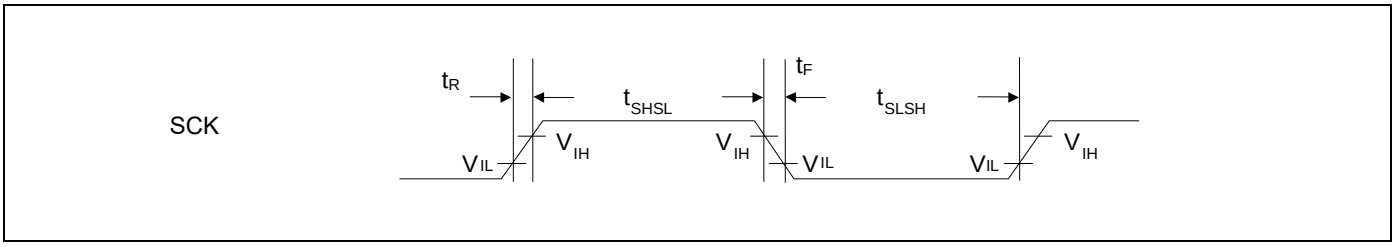


Slave mode

UART external clock input (EXT = 1)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 50 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



11.4.10 External Input Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

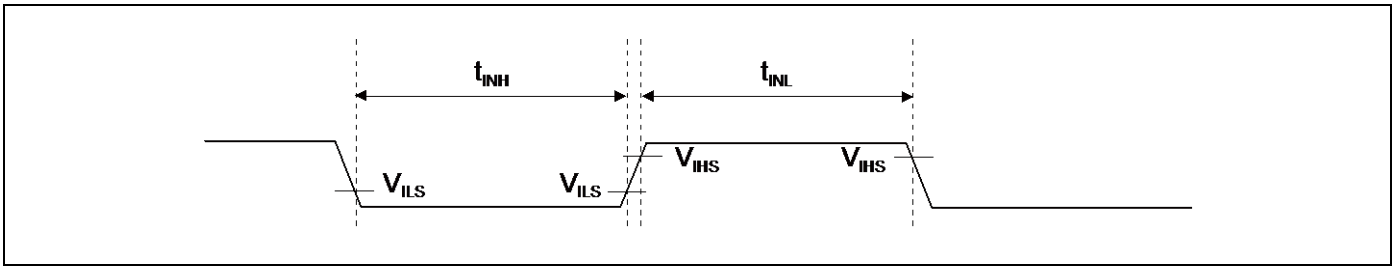
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		IGTRG	-	$2t_{CYCP}$*1	-	ns	PPG IGBT mode
		INTxx, NMIX	*2	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
			*3	500	-	ns	
		WKUPx	*4	500	-	ns	Deep standby wake up

*1: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which the A/D converter, Multi-function Timer, PPG, External interrupt, Deep Standby mode Controller are connected to, see Block Diagram in this data sheet.

*2: When in Run mode, in Sleep mode.

*3: When in Timer mode, in RTC mode, in Stop mode.

*4: When in Deep Standby RTC mode, in Deep Standby Stop mode.



11.4.11 I²C Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

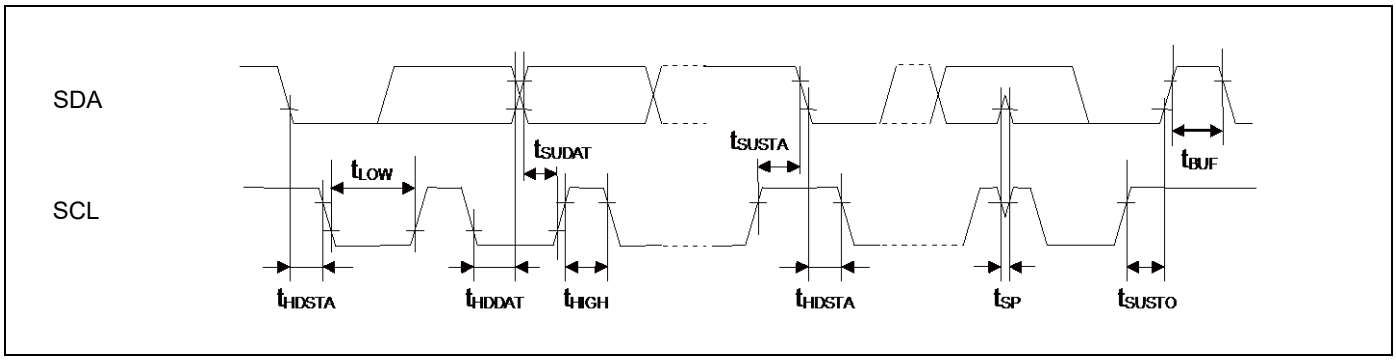
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 50 pF, R = (V_P/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between STOP condition and START condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively. V_P indicates the power supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

*4: t_{CYCP} is the APB bus clock cycle time. About the APB bus number which I²C is connected to, see Block Diagram in this data sheet. To use Standard-mode, set the APB bus clock at 2 MHz or more. To use Fast-mode, set the APB bus clock at 8 MHz or more.



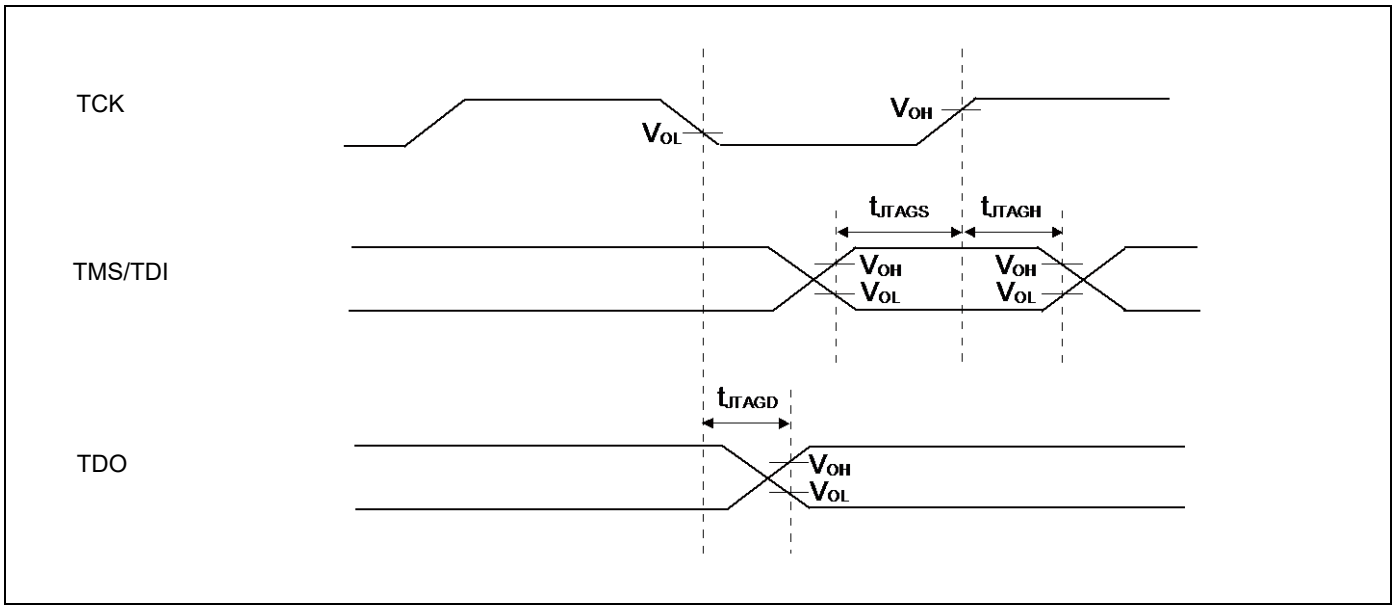
11.4.12 JTAG Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS,TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS,TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	30	ns	
			2.7 V ≤ $V_{CC} < 4.5$ V	-	45		
			$V_{CC} < 2.7$ V	-	60		

Note:

- *When the external load capacitance C_L = 50 pF.*



11.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 1.8V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	INL	-	-	± 2.5	± 3.0	LSB	AV_{CC} ≥ 2.7 V
			-	± 3.5	± 4.0	LSB	AV_{CC} < 2.7 V
Differential Nonlinearity	DNL	-	-	± 1.8	± 1.9	LSB	AV_{CC} ≥ 2.7 V
			-	± 2.7	± 2.9	LSB	AV_{CC} < 2.7 V
Zero transition voltage	V_{ZT}	ANxx	-	± 9	± 20	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 9	AVRH ± 20	mV	
Conversion time*1	-	-	1.0	-	-	µs	AV_{CC} ≥ 2.7 V
			4.0				AV_{CC} < 2.7 V
Sampling time*2	t_S	-	0.3	-	10	µs	AV_{CC} ≥ 2.7 V
			1.2				AV_{CC} < 2.7 V
Compare clock cycle*3	t_{CCK}	-	50	-	1000	ns	AV_{CC} ≥ 2.7 V
			200				AV_{CC} < 2.7 V
Period of operation enable state transitions	t_{STT}	-	-	-	1	µs	
Analog input capacity	C_{AIN}	-	-	-	15	pF	
Analog input resistor	R_{AIN}	-	-	-	0.9	kΩ	AV_{CC} ≥ 4.5 V
					1.6		2.7 V ≤ AV_{CC} < 4.5 V
					4.0		AV_{CC} < 2.7 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	0.3	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	AV_{CC} ≥ 2.7 V
			AV_{CC}				AV_{CC} < 2.7 V

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

The condition of the minimum conversion time is the following.

AV_{CC} ≥ 2.7 V, HCLK=20 MHz sampling time: 0.3 µs, compare time: 0.7 µs

AV_{CC} < 2.7 V, HCLK=20 MHz sampling time: 1.2 µs, compare time: 2.8 µs

Ensure that it satisfies the value of the sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting*4 of the sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM3 Family Peripheral Manual Analog Macro Part.

The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.

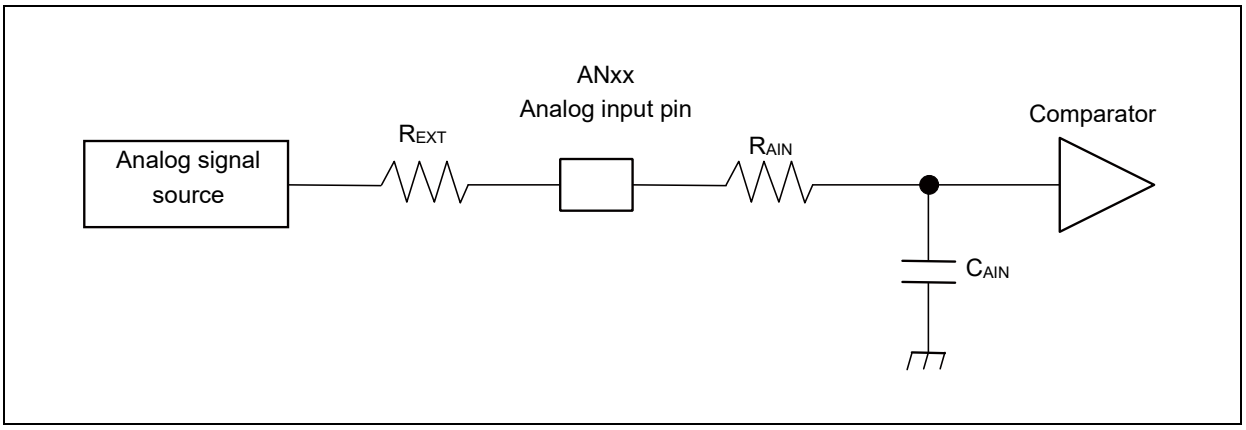
For the number of the APB bus to which the A/D Converter is connected, see Block Diagram.

The Base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: A necessary sampling time changes by external impedance.

Ensure to set the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistor of A/D = 0.9 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V
Input resistor of A/D = 1.6 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V
Input resistor of A/D = 4.0 kΩ at 1.8 V ≤ AV_{CC} < 2.7 V

C_{AIN}: Input capacity of A/D = 15 pF at 1.8 V ≤ AV_{CC} ≤ 5.5 V

R_{EXT}: Output impedance of external circuit

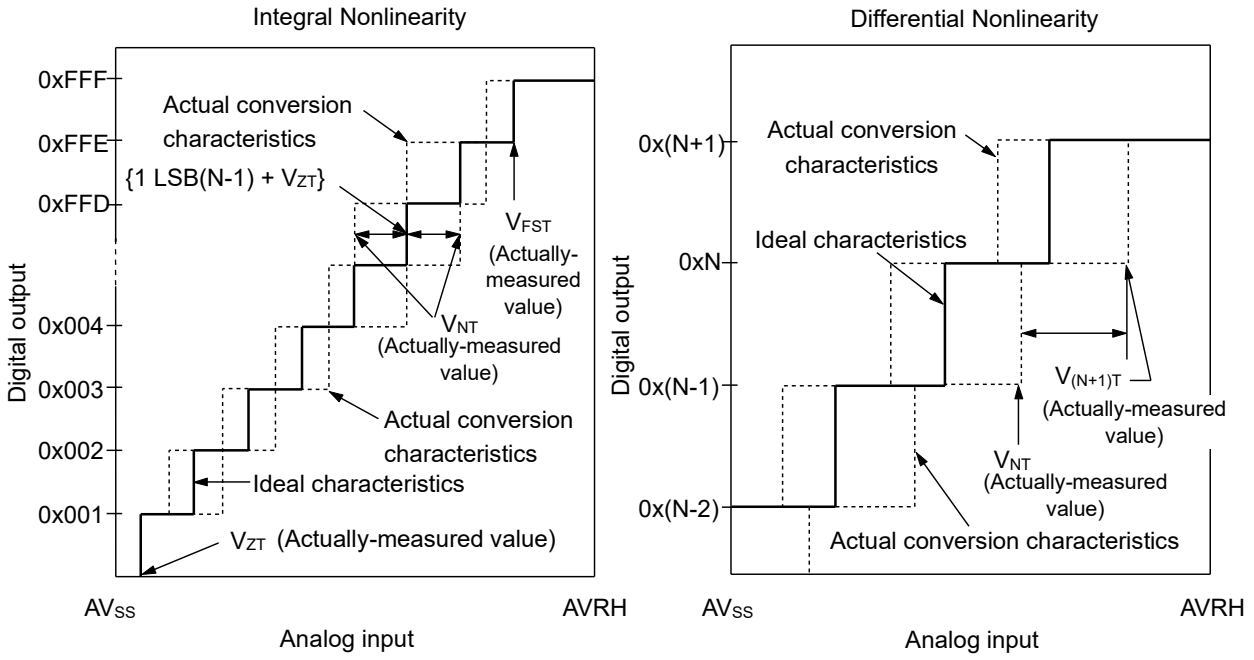
(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000←→0b000000000001) and the full-scale transition point (0b111111111110←→0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

11.6 10-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 1.8V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	10	bit	
Conversion time	t_{C20}		0.37	0.53	0.69	µs	Load 20 pF
	t_{C100}		1.87	2.67	3.47	µs	Load 100 pF
Integral Nonlinearity	INL		-4.0	-	+4.0	LSB	*
Differential Nonlinearity	DNL		-0.9	-	+0.9	LSB	*
Output Voltage offset	V_{OFF}		-	-	10.0	mV	Code is 0x000
			-50.0	-	+5.5	mV	Code is 0x3FF
Analog output impedance	R_O		2.45	3.50	5.5	kΩ	D/A operation
			5.0	9.0	-	MΩ	D/A stop
Output undefined period	t_R		-	-	250	ns	

*: No-load

11.7 Low-Voltage Detection Characteristics

11.7.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V_{DLR}	SVHR = 0001	1.43	1.53	1.63	V	When voltage drops
Released voltage	V_{DHR}		1.53	1.63	1.73	V	When voltage rises
Detected voltage	V_{DLR}	SVHR = 0100	1.80	1.93	2.06	V	When voltage drops
Released voltage	V_{DHR}		1.90	2.03	2.16	V	When voltage rises
LVD stabilization wait time	t_{LVDRW}	-	-	-	633 × t_{CYCP} *	µs	
Detection delay time	t_{LVDRD}	dV/dt ≥ -4mV/µs	-	-	60	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

11.7.2 Interrupt of Low-Voltage Detection

Normal mode

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V_{DLI}	SVHI = 0000	1.87	2.00	2.13	V	When voltage drops
Released voltage	V_{DHI}		1.97	2.10	2.23	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0001	1.96	2.10	2.24	V	When voltage drops
Released voltage	V_{DHI}		2.06	2.20	2.34	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0010	2.05	2.20	2.35	V	When voltage drops
Released voltage	V_{DHI}		2.15	2.30	2.45	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0011	2.15	2.30	2.45	V	When voltage drops
Released voltage	V_{DHI}		2.25	2.40	2.55	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0100	2.24	2.40	2.56	V	When voltage drops
Released voltage	V_{DHI}		2.34	2.50	2.66	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0101	2.33	2.50	2.67	V	When voltage drops
Released voltage	V_{DHI}		2.43	2.60	2.77	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0110	2.43	2.60	2.77	V	When voltage drops
Released voltage	V_{DHI}		2.53	2.70	2.87	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0111	2.61	2.80	2.99	V	When voltage drops
Released voltage	V_{DHI}		2.71	2.90	3.09	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1000	2.80	3.00	3.20	V	When voltage drops
Released voltage	V_{DHI}		2.90	3.10	3.30	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1001	2.99	3.20	3.41	V	When voltage drops
Released voltage	V_{DHI}		3.09	3.30	3.51	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1010	3.36	3.60	3.84	V	When voltage drops
Released voltage	V_{DHI}		3.46	3.70	3.94	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1011	3.45	3.70	3.95	V	When voltage drops
Released voltage	V_{DHI}		3.55	3.80	4.05	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1100	3.73	4.00	4.27	V	When voltage drops
Released voltage	V_{DHI}		3.83	4.10	4.37	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1101	3.83	4.10	4.37	V	When voltage drops
Released voltage	V_{DHI}		3.93	4.20	4.47	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1110	3.92	4.20	4.48	V	When voltage drops
Released voltage	V_{DHI}		4.02	4.30	4.58	V	When voltage rises
LVD stabilization wait time	t_{LVDIW}	-	-	-	633 × t_{CYCP} *	µs	
Detection delay time	t_{LVDID}	dV/dt ≥ - 4mV/µs	-	-	60	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

Low-power mode

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V_{DLIL}	SVHI = 0000	1.80	2.00	2.20	V	When voltage drops
Released voltage	V_{DHIL}		1.90	2.10	2.30	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0001	1.89	2.10	2.31	V	When voltage drops
Released voltage	V_{DHIL}		1.99	2.20	2.41	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0010	1.98	2.20	2.42	V	When voltage drops
Released voltage	V_{DHIL}		2.08	2.30	2.52	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0011	2.07	2.30	2.53	V	When voltage drops
Released voltage	V_{DHIL}		2.17	2.40	2.63	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0100	2.16	2.40	2.64	V	When voltage drops
Released voltage	V_{DHIL}		2.26	2.50	2.74	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0101	2.25	2.50	2.75	V	When voltage drops
Released voltage	V_{DHIL}		2.35	2.60	2.85	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0110	2.34	2.60	2.86	V	When voltage drops
Released voltage	V_{DHIL}		2.44	2.70	2.96	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0111	2.52	2.80	3.08	V	When voltage drops
Released voltage	V_{DHIL}		2.62	2.90	3.18	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1000	2.70	3.00	3.30	V	When voltage drops
Released voltage	V_{DHIL}		2.80	3.10	3.40	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1001	2.88	3.20	3.52	V	When voltage drops
Released voltage	V_{DHIL}		2.98	3.30	3.62	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1010	3.24	3.60	3.96	V	When voltage drops
Released voltage	V_{DHIL}		3.34	3.70	4.06	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1011	3.33	3.70	4.07	V	When voltage drops
Released voltage	V_{DHIL}		3.43	3.80	4.17	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1100	3.60	4.00	4.40	V	When voltage drops
Released voltage	V_{DHIL}		3.70	4.10	4.50	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1101	3.69	4.10	4.51	V	When voltage drops
Released voltage	V_{DHIL}		3.79	4.20	4.61	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1110	3.78	4.20	4.62	V	When voltage drops
Released voltage	V_{DHIL}		3.88	4.30	4.72	V	When voltage rises
LVD stabilization wait time	t_{LVDILW}	-	-	-	8039 × t_{CYCP} *	µs	
Detection delay time	t_{LVDILD}	dV/dt ≥ - 0.4mV/µs	-	-	800	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

11.8 Flash Memory Write/Erase Characteristics

11.8.1 Write / Erase time

(V_{CC} = 2.0V to 5.5V, T_A = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	1.6	7.5	s	Includes write time prior to internal erase
	Small Sector	0.4	2.1		
Half word (16-bit) write time		25	400	µs	Not including system-level overhead time.
Chip erase time		4	19.2	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximam value is guarantee value under 100,000 cycle of erase/write.

11.8.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20 *	
10,000	10 *	
100,000	5*	

*: At average + 85°C

11.9 Return Time from Low-Power Consumption Mode

11.9.1 Return Factor: Interrupt/WKUP

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

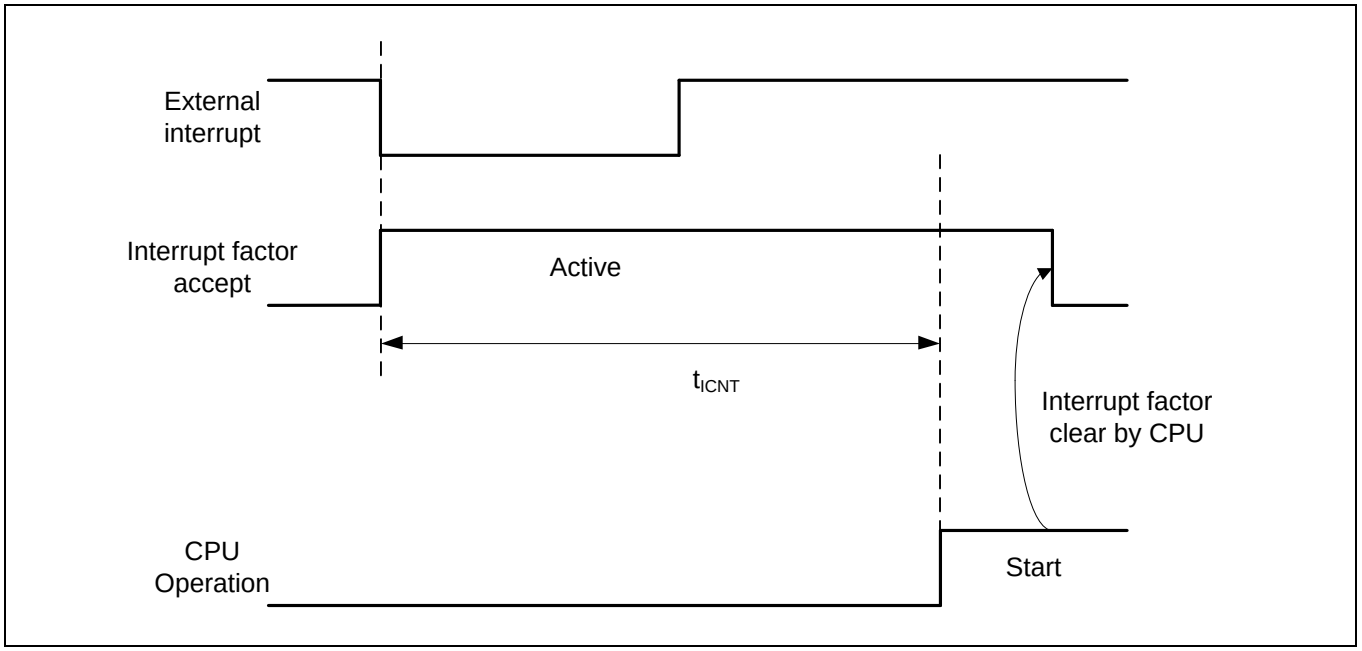
Return Count Time

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	t_{CYCC}		µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		630	1260	µs	
Sub Timer mode		630	1260	µs	
RTC mode, Stop mode		1083	2100	µs	
Deep Standby RTC mode Deep Standby Stop mode		1099	2127	µs	

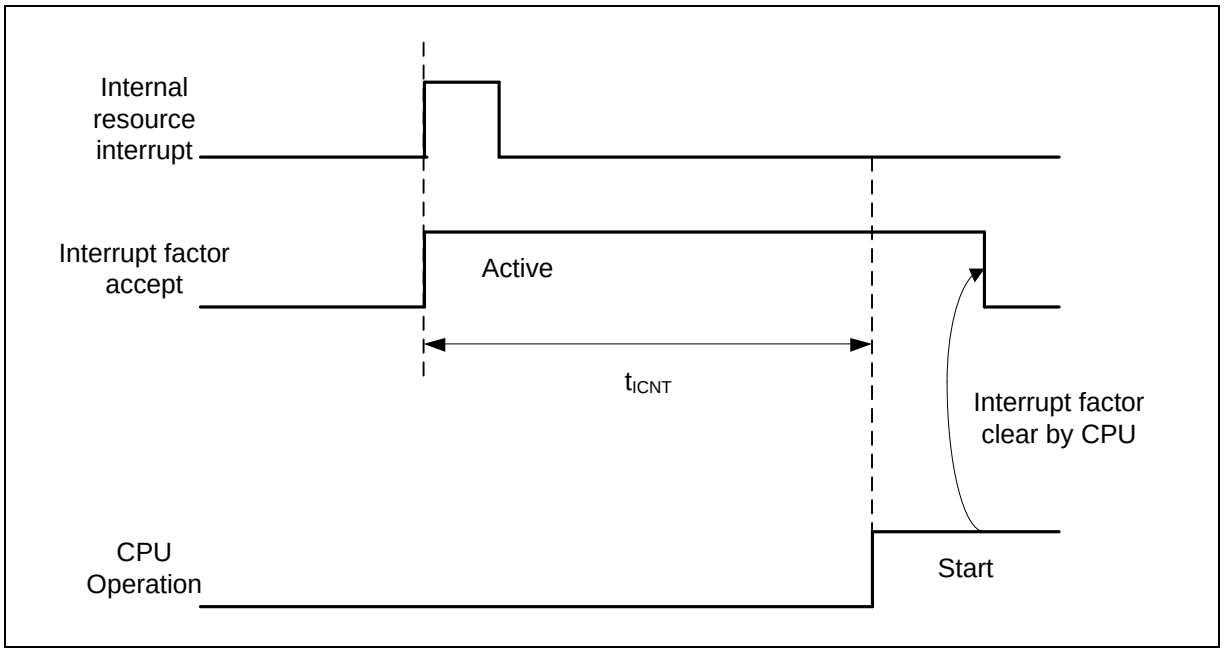
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.*

11.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

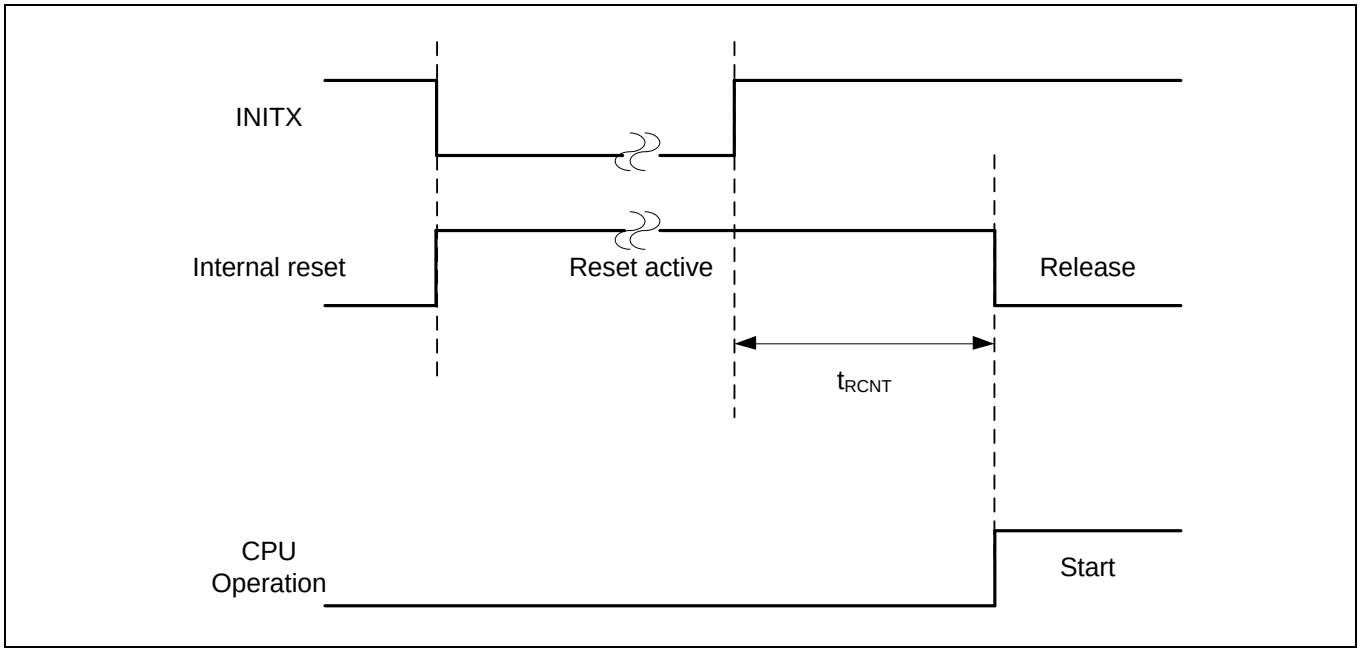
Return Count Time

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

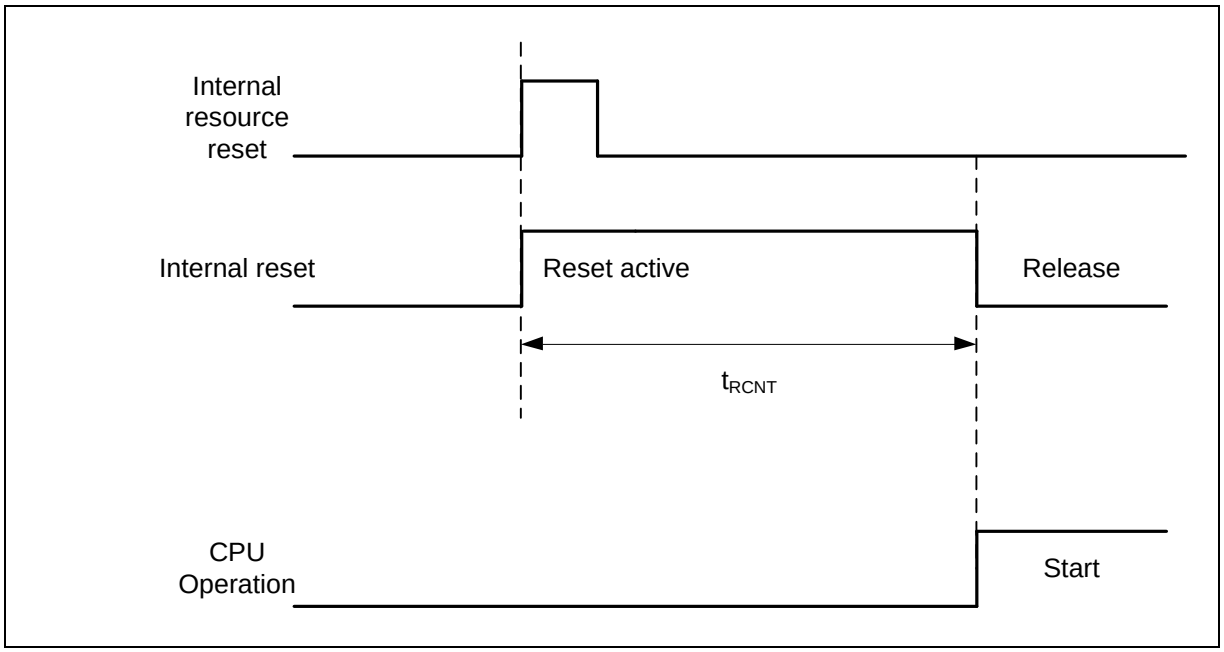
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	359	647	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		359	647	µs	
Low-speed CR Timer mode		929	1787	µs	
Sub Timer mode		929	1787	µs	
RTC/Stop mode		1099	2127	µs	
Deep Standby RTC mode Deep Standby Stop mode		1099	2127	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

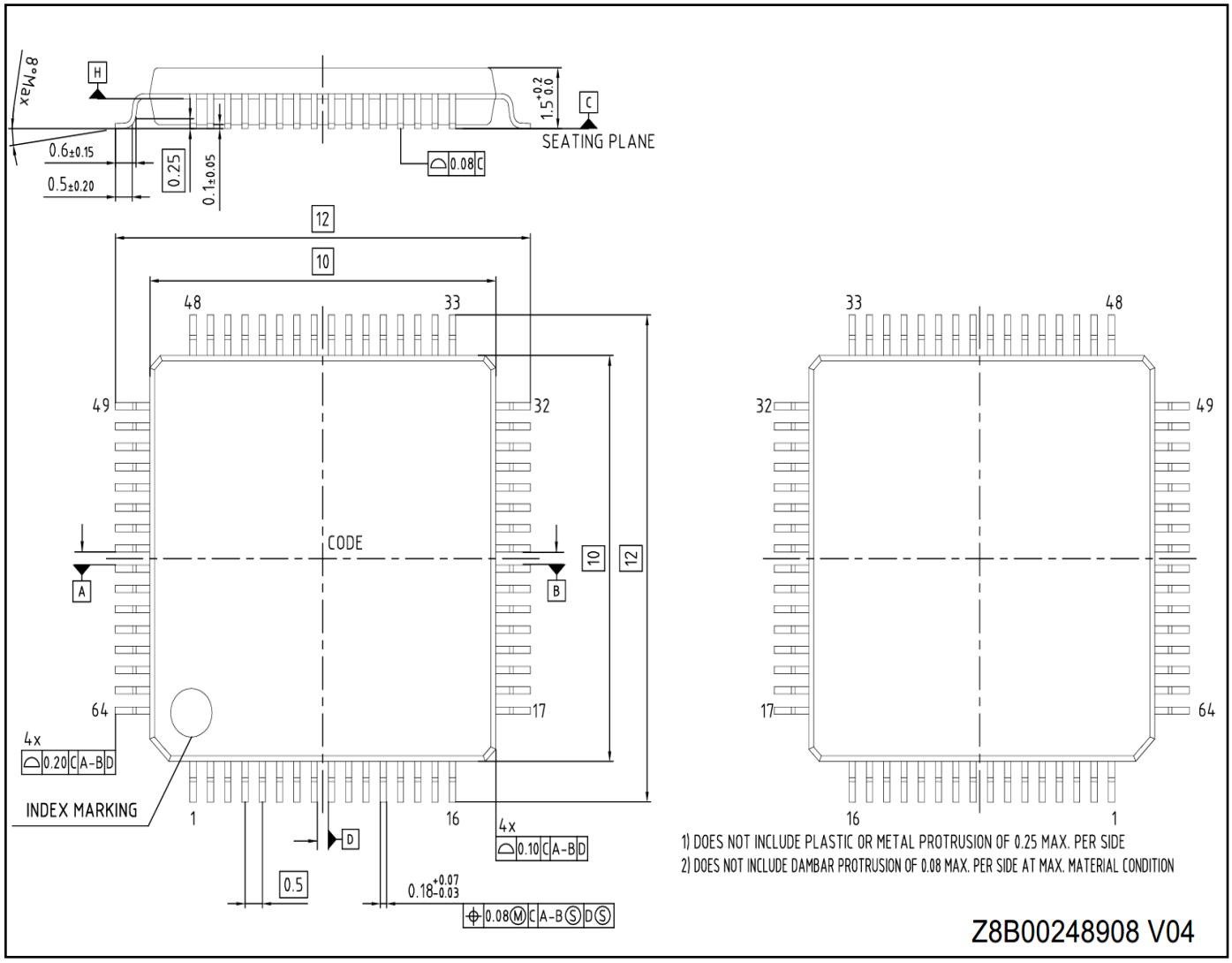
- *The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.*
- *The time during the power-on reset/low-voltage detection reset is excluded. See (6) Power-on Reset Timing in 4. AC Characteristics in Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.*
- *When in recovery from reset, CPU changes to the High-speed CR Run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

12. Ordering Information

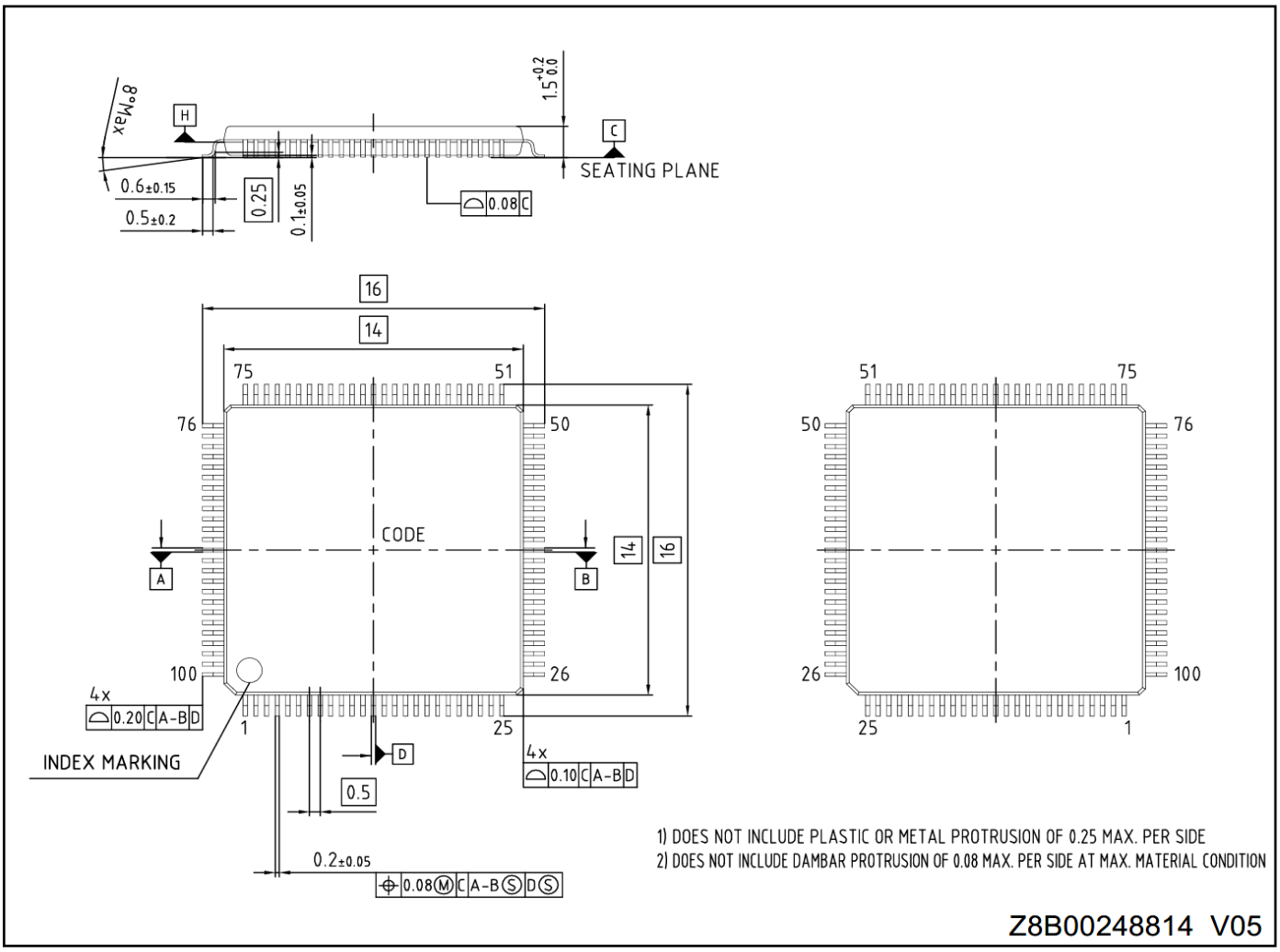
Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
CY9AFAA2LPMC1-G-UNE2	128 Kbyte	16 Kbyte	Plastic・LQFP (0.5mm pitch), 64-pin (LQD064)	Tray
CY9AFAA1NPMC-G-UNE2	64 Kbyte	12 Kbyte	Plastic・LQFP (0.5mm pitch), 100-pin (LQI100)	
CY9AFAA2NPMC-G-UNE2	128 Kbyte	16 Kbyte		

13. Package Dimensions

Package Type	Package Code
LQFP 64	LQD064



Package Type	Package Code
LQFP 100	LQI100



14. Errata

This chapter describes the errata for CY9AAA0N Series. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

14.1 Part Numbers Affected

Part Number
Initial Revision
CY9AFAA2LPMC1-G-SNE2, CY9AFAA2LPMC1-G-UNE2, CY9AFAA2MPMC-G-SNE2, CY9AFAA1NPMC-G-SNE2, CY9AFAA1NPMC-G-UNE2, CY9AFAA2NPMC-G-SNE2, CY9AFAA2NPMC-G-UNE2

14.2 Qualification Status

Product Status: In Production − Qual.

14.3 Errata Summary

This table defines the errata applicability to available devices.

Items	Part Number	Silicon Revision	Fix Status
[14.4.1] HDMI-CEC polling message issue	Refer to 14.1	Initial Rev	Next silicon is not planned
[14.4.2] RTC delay issue	Refer to 14.1	Initial Rev	Next silicon is not planned

14.4 Errata Detail

14.4.1 HDMI-CEC polling message issue

■PROBLEM DEFINITION
Error#1) While MCU sends a Polling Message, it always returns a NACK to a message coming to the MCU from another node.

Error#2) MCU always waits for 7-bit signal free on CEC line before it drives the line even when the last line initiator was another node.

■PARAMETERS AFFECTED
N/A

■TRIGGER CONDITION(S)
This error always happens.

■SCOPE OF IMPACT
MCU does not reply properly to another node.

■WORKAROUND
The software workaround is applied to Error #1.

1. Store 0x0 to SFREE register.
2. Monitor CEC line with GPIO and wait until 1 lasts for the signal free time.
3. Store frame data to TXDATA register and store 0x0F to RCADR1 or RCADR2 register.

It sends a message after 3~4 clocks of 32.768 kHz clock when TXDATA is stored 0x0F.

If the device receives a frame from another node within 2~3 clocks after storing TXDATA, the bus error occurs and if the device receives a frame from another node within 3~4 clocks after storing TXDATA, the arbitration lost occurs. In these cases:

4-A-1. Set RCADR1 or RCADR2 to former value from 0x0F to reply ACK

4-A-2. Return back to step 2 above

If the device receives a frame from another node within 1~2 clocks after storing TXDATA, take these steps.

4-B-1. Monitor CEC line with GPIO after 50us from storing TXDATA

4-B-2. Set TXEN to 1 -> 0 -> 1 immediately when GPIO finds state low on the CEC line

4-B-3. Set RCADR1 or RCADR2 to former value from 0x0F to reply ACK

4-B-4. Return back to step 2 above

For Error #2, there is no software workaround, but signal free time of fixed 7-bit does not violate HDMI-CEC specification. The specification says signal free time must be more than and equals to 5-bit.

■FIX STATUS
The user uses the workaround to avoid the issue. The next silicon fixing the issue is not planned.

14.4.2 RTC delay issue

■PROBLEM DEFINITION
RTC delays when software reset or APB2 reset occurs.

■PARAMETERS AFFECTED
N/A

■TRIGGER CONDITION(S)
This error happens when software reset or APB2 reset occurs.

■SCOPE OF IMPACT
RTC delays and does not time correctly.

■WORKAROUND
RTC block is supplied with sub-clock. Both software reset and APB2 reset disable two clocks of sub-clock to RTC block. The workaround is to count occurrence of software and APB2 reset and calculate how many clocks of sub-clock were disabled and add one second to RTC counter when accumulated disabled sub-clock period reaches one second.

■FIX STATUS
The user uses the workaround to avoid the issue. The next silicon fixing the issue is not planned.

Major Changes

Spansion Publication Number: DS706-00067

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
-	-	Changed from Preliminary to Full Producton
-	-	Deleted a part of QFN
66,67	ELECTRICAL CHARACTERISTICS 3.DC Characteristics (1) Current Rating	Revised the values of “TBD”
Revision 2.0		
2	Features · On-chip Memories	Changed the description of on-chip SRAM
7 - 33	Packages Pin Assignment List of Pin Functions	Deleted QFN package
45	Handling Devices Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
49	Memory Map · Memory map(2)	Added the summary of Flash memory sector
64 - 66	Electrical Characteristics 3. DC Characteristics (1) Current rating	· Changed the table format · Added Main Timer mode current · Added Flash Memory Current · Moved A/D Converter Current · Moved D/A Converter Current
67	Electrical Characteristics 3. DC Characteristics (2) Pin Characteristics	Added the input leak current of CEC port at power off
71	Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions of Main PLL (4-2) Operating Conditions of Main PLL	· Added the figure of Main PLL connection
72	Electrical Characteristics 4. AC Characteristics (6) Power-on Reset Timing	· Changed the figure of timing · Changed from Reset release delay time(t_{OND}) to Time until releasing Power-on reset(t_{PRT})
74 - 81	Electrical Characteristics 4. AC Characteristics (8) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
85	Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Added Conversion time at AV_{CC} < 2.7 V
89	Electrical Characteristics 7. Low-voltage Detection Characteristics	Deleted the figure
92	Electrical Characteristics 8. Flash Memory Write/Erase Characteristics	Change to the erase time of include write time prior to internal erase
93 - 96	Electrical Characteristics 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
97	Ordering Information	Changed notation of part number

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY9AAA0N Series 32-bit Arm® Cortex®-M3 FM3 Microcontroller
Document Number: 002-05673

<table>
<tr><th>Revision</th><th>ECN</th><th>Submission Date</th><th>Description of Change</th></tr>
<tr><td>**</td><td>-</td><td>06/30/2015</td><td>Migrated to Cypress and assigned document number 002-05673.
No change to document contents.</td></tr>
<tr><td>*A</td><td>5209465</td><td>04/07/2016</td><td>Updated to Cypress template.</td></tr>
<tr><td>*B</td><td>5513605</td><td>02/08/2017</td><td>Modified RTC description in “Features, Real-Time Clock(RTC)”:
Changed starting count value from 01 to 00. Deleted “second, or day of the week” in the Interrupt function (Page 2).
Changed package code as the following table in following section.
2. Package (Page 7)
3. Pin Assignment (Page 8 to 11)
12. Electrical Characteristics (Page 63)
13. Ordering Information (Page 97)
14. Package Dimensions (Page 98 to 103)
<table>
<tr><th>Before</th><th>After</th></tr>
<tr><td>FPT-64P-M38</td><td>LQD064</td></tr>
<tr><td>FPT-64P-M39</td><td>LQG064</td></tr>
<tr><td>FPT-80P-M37</td><td>LQH080</td></tr>
<tr><td>FPT-80P-M40</td><td>LQJ080</td></tr>
<tr><td>FPT-100P-M23</td><td>LQI100</td></tr>
<tr><td>FPT-100P-M06</td><td>PQH100</td></tr>
</table>
Added the Baud rate spec in “12.4.9 CSIO/UART Timing” (Page 64 to 70)
Changed Part numbers in 13. Ordering Information (Page 97)
“MB9AFAA2LPMC1-G-SNE2” to “MB9AFAA2LPMC1-G-UNE2”
“MB9AFAA2MPMC-G-SNE2” to “MB9AFAA2MPMC-G-UNE2”
“MB9AFAA1NPMC-G-SNE2” to “MB9AFAA1NPMC-G-UNE2”
“MB9AFAA2NPMC-G-SNE2” to “MB9AFAA2NPMC-G-UNE2”.
Added 15. Errata (Page 104 to 105).</td></tr>
<tr><td>*C</td><td>5768634</td><td>06/12/2017</td><td>Updated Cypress Logo and Copyright.</td></tr>
<tr><td>*D</td><td>5929772</td><td>10/16/2017</td><td>Corrected the following Analog output impedance MAX value (D/A operation)
4.55kΩ → 5.5kΩ
in chapter 12.6 10-bit D/A Converter.</td></tr>
<tr><td>*E</td><td>6565905</td><td>05/03/2019</td><td>Updated Document Title to read as “CY9AAA0N Series 32-bit Arm® Cortex®-M3 FM3 Microcontroller”.
Replaced “MB9AAA0N Series” with “CY9AAA0N Series” in all instances across the document.</td></tr>
</table>

			Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.
*F	8109665	02/20/2025	Updated Product Lineup, Packages, Pin Assignment, Memory Map, Block Diagram, Package Dimensions. Removed part numbers in all instances across the document: • CY9AFAA1LPMC1-G-SNE2 • CY9AFAA1LPMC-G-SNE2 • CY9AFAA2LPMC-G-SNE2 • CY9AFAA1MPMC-G-SNE2 • CY9AFAA2MPMC-G-UNE2 • CY9AFAA1MPMC1-G-SNE2 • CY9AFAA2MPMC1-G-SNE2 • CY9AFAA1NPF-G-SNE1 • CY9AFAA2NPF-G-SNE1 Replaced Package Dimensions • 002-11499 ** with Z8B00248908 V04 • 002-11500 *A with Z8B00248814 V05

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