CY8C41xx

Features

- 32-bit MCU subsystem
  - 48 MHz Arm® Cortex®-M0+ CPU with single-cycle multiply
  - Up to 64 KB of flash with read accelerator
  - Up to 8 KB of SRAM
- Programmable analog
  - Two opamps with reconfigurable high-drive external and high-bandwidth internal drive and Comparator modes and ADC input buffering capability. Opamps can operate in deep sleep low-power mode
  - 12-bit 1-Msps SAR ADC with differential and single-ended modes, and channel sequencer with signal averaging
  - Single-slope 10-bit ADC function provided by a capacitance sensing block
  - Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
  - Two low-power comparators that operate in Deep Sleep low-power mode
- Programmable digital
  - Programmable logic blocks allowing boolean operations to be performed on port inputs and outputs
- Low-power 1.71-V to 5.5-V operation
  - Deep Sleep mode with operational analog and 2.5-µA digital system current
- Capacitive sensing
  - Capacitive sigma-delta provides best-in-class signal-to-noise ratio (SNR) (>5:1) and water tolerance
  - Infineon-supplied software component makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense)
- LCD drive capability
  - LCD segment drive capability on GPIOs
- Serial communication
  - Three independent run-time reconfigurable serial communication blocks (SCBs) with re-configurable I^2C, SPI, or UART functionality
- Timing and pulse-width modulation
  - Five 16-bit Timer/Counter/Pulse-width Modulator (TCPWM) blocks
  - Center-aligned, edge, and pseudo-random modes
  - Comparator-based triggering of kill signals for motor drive and other high-reliability digital logic applications
  - Quadrature decoder
- Up to 36 programmable GPIO pins
  - 48LD TQFP, 44LD TQFP, 40L QFN, 32-lead QFN, and 35-ball WLCSP packages
  - Any GPIO pin can be CAPSENSE™, analog, or digital
  - Drive modes, strengths, and slew rates are programmable
- Clock sources
  - 32 kHz watch crystal oscillator (WCO)
  - ±2% internal main oscillator (IMO)
  - 32 kHz internal low-power oscillator (ILO)
- ModusToolbox™ software
  - Comprehensive collection of multi-platform tools and software libraries
  - Includes board support packages (BSPs), peripheral driver library (PDL), and middleware such as CAPSENSE™

- PSoC™ Creator design environment
  - Integrated development environment (IDE) provides schematic design entry and build, with analog and digital automatic routing
  - Application programming interface (API) components for all fixed-function and programmable peripherals
- Industry-standard tool compatibility
  - After schematic entry, development can be done with Arm®-based industry-standard development tools

Description

PSoC™ 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0+ CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC™ 4100S product family is a member of the PSoC™ 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CAPSENSE™) with best-in-class performance, programmable general-purpose continuous-time and switched-capacitor analog blocks, and programmable connectivity. PSoC™ 4100S products are upward compatible with members of the PSoC™ 4 platform for new applications and design needs.

Table of contents

1 Development ecosystem

1.1 PSoC™ 4 MCU resources

Infineon provides a wealth of data at www.infineon.com to help you select the right PSoC™ device and quickly and effectively integrate it into your design. The following is an abbreviated, hyperlinked list of resources for PSoC™ 4 MCU:

- **Overview**: PSoC™ Portfolio
- **Product selectors**: PSoC™ 4 MCU
- Application notes cover a broad range of topics, from basic to advanced level, and include the following:
  - AN79953: Getting Started With PSoC™ 4 MCU. This application note has a convenient flow chart to help decide which IDE to use: ModusToolbox™ software or PSoC™ Creator
  - AN88619: PSoC™ 4 hardware design considerations
  - AN73854: PSoC™ Creator - Introduction to bootloaders
  - AN89610: PSoC™ Arm® Cortex® code optimization
  - AN86233: PSoC™ 4 MCU low-power modes and power reduction techniques
  - AN57821: Mixed signal circuit board layout considerations
  - AN85951: PSoC™ 4 and PSoC™ 6 CAPSENSE™ design guide
- Code examples demonstrate product features and usage, and are also available on Infineon GitHub repositories.
- Reference manuals provide detailed descriptions of PSoC™ 4 MCU architecture and registers.
- PSoC™ 4 MCU programming specification provides the information necessary to program PSoC™ 4 MCU non-volatile memory.
- **Development tools**
  - ModusToolbox™ software enables cross platform code development with a robust suite of tools and software libraries.
  - PSoC™ Creator is a free Windows-based IDE. It enables concurrent hardware and firmware design of PSoC™ 3, PSoC™ 4, PSoC™ 5LP, and PSoC™ 6 MCU based systems. Applications are created using schematic capture and over 150 pre-verified, production-ready peripheral components.
  - CY8CKIT-041-41XX PSoC™ 4100S CAPSENSE™ Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields.
  - MiniProg4 and MiniProg3 all-in-one development programmers and debuggers.
- PSoC™ 4 MCU CAD libraries provide footprint and schematic support for common tools. IBIS models are also available.
- Training Videos are available on a wide range of topics including the PSoC™ 4 MCUs.
- Infineon developer community enables connection with fellow PSoC™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated PSoC™ 4 MCU community.

1.2 ModusToolbox™ software

ModusToolbox™ software is Infineon' comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code repositories on GitHub, including:

- Board support packages (BSPs) aligned with Infineon kits

- Low-level resources, including a peripheral driver library (PDL)
- Middleware enabling industry-leading features such as CAPSENSE™
- An extensive set of thoroughly tested code example applications

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional Eclipse IDE for ModusToolbox™, as Figure 1 shows. For information on using Infineon tools, refer to the documentation delivered with ModusToolbox™ software, and AN79953: Getting Started with PSoC™ 4 MCU.

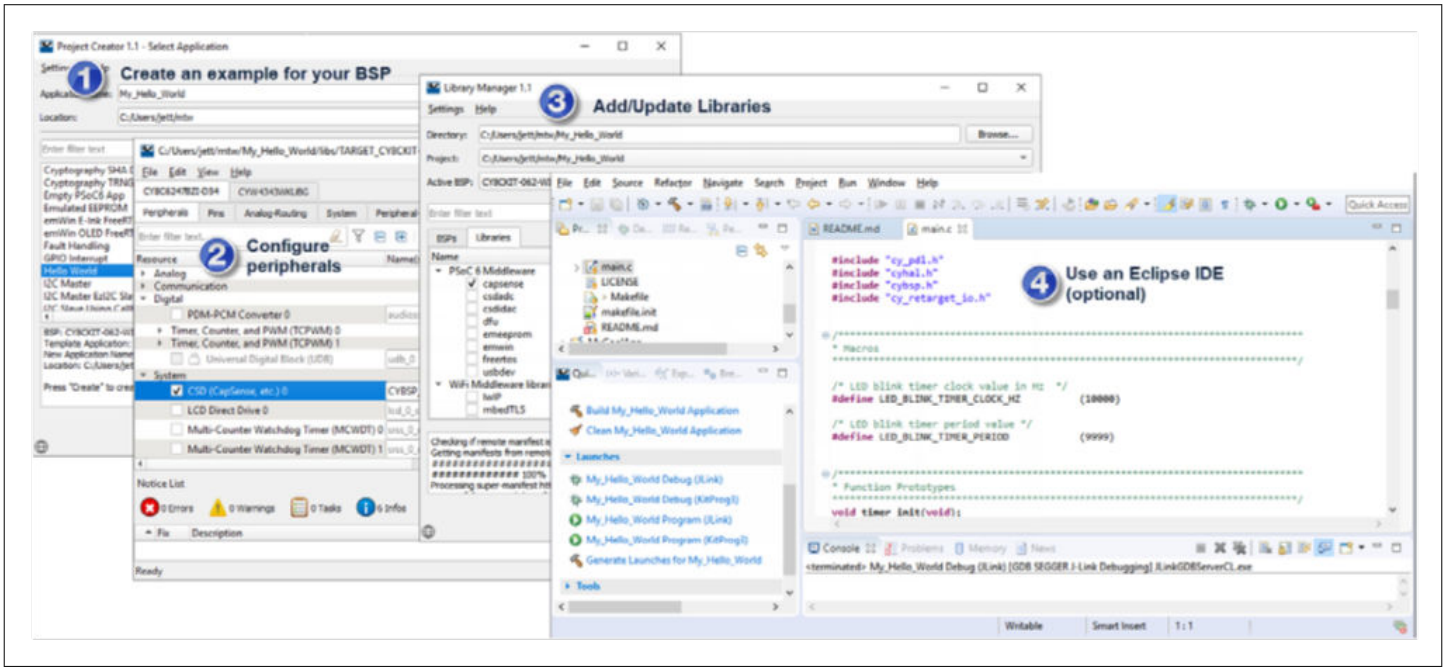


Figure 1 ModusToolbox™ software tools

1.3 PSoC™ Creator

PSoC™ Creator is a free Windows-based IDE. It enables you to design hardware and firmware systems concurrently, based on PSoC™ 4 MCU. As Figure 2 shows, with PSoC™ Creator you can:

1. Explore the library of 200+ components
2. Drag and drop component icons to complete your hardware system design in the main design workspace
3. Configure components using the component configuration tools and the component datasheets
4. Co-design your application firmware and hardware in the PSoC™ Creator IDE or build a project for a third-party IDE
5. Prototype your solution with the PSoC™ 4 pioneer kits. If a design change is needed, PSoC™ Creator and components enable you to make changes on-the-fly without the need for hardware revisions

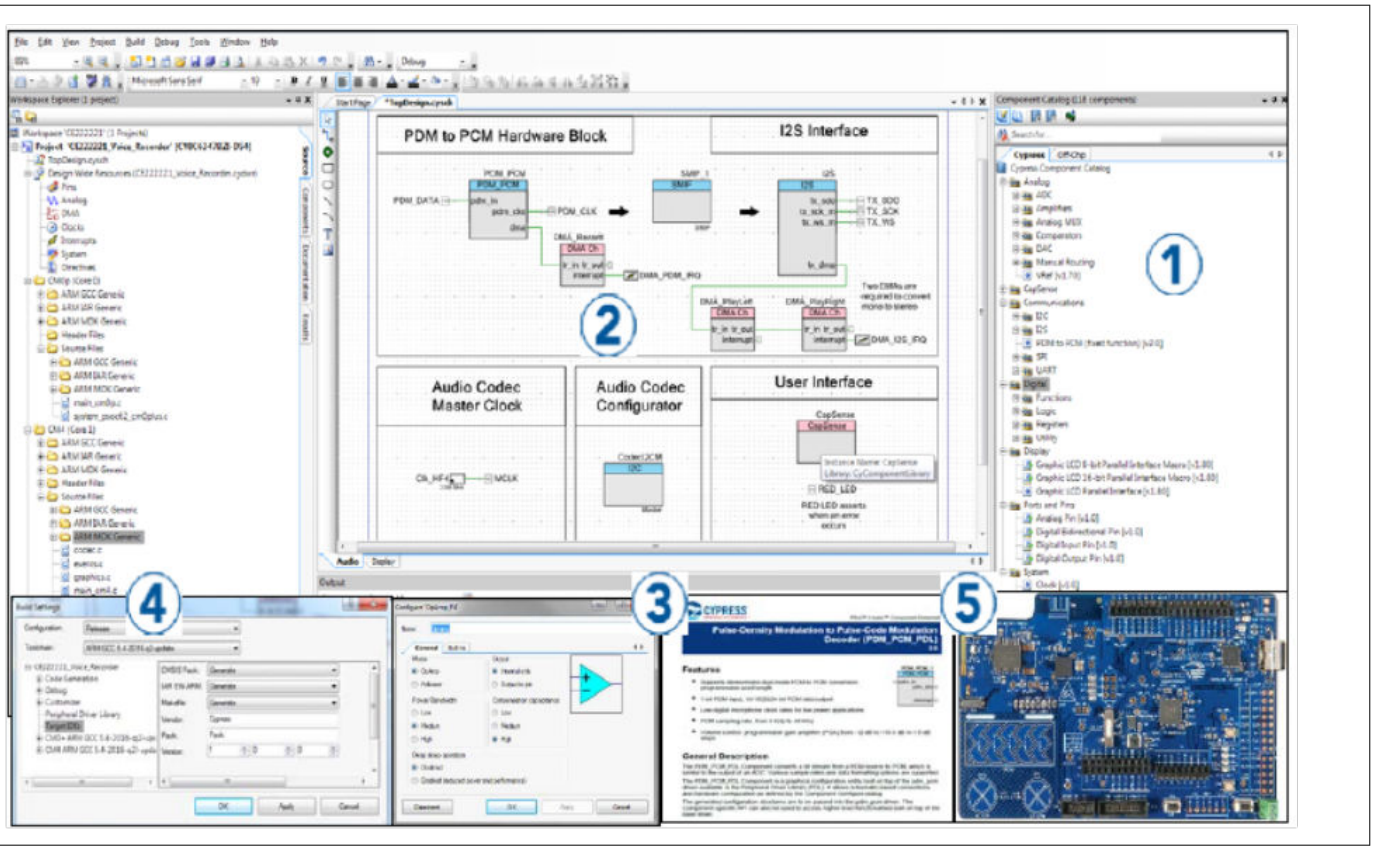


Figure 2 PSoC™ Creator schematic entry and components

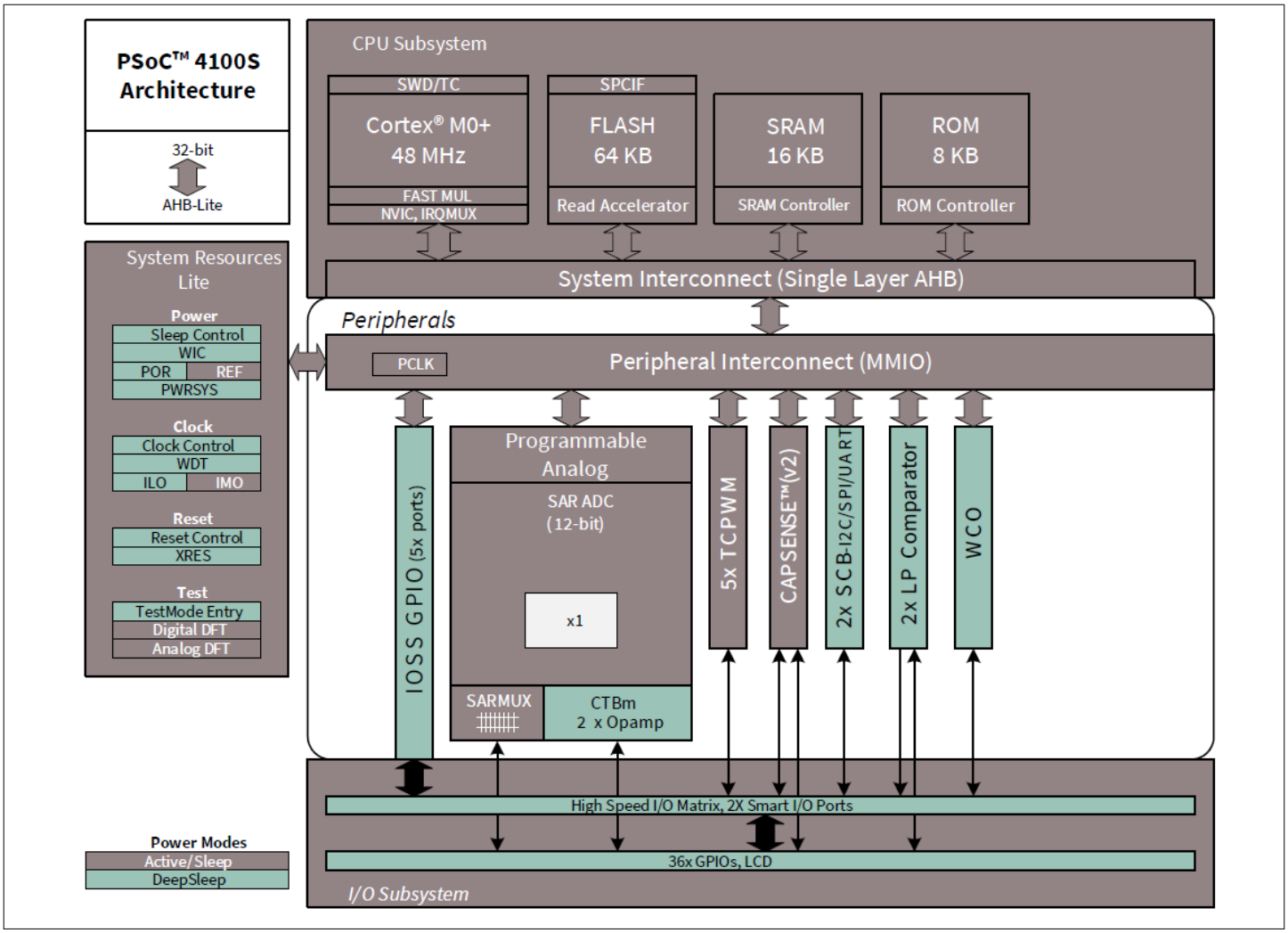


Figure 3 Block diagram

PSoC™ 4100S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® serial-wire debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC™ Creator IDE provides fully integrated programming and debug support for the PSoC™ 4100S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC™ 4100S provides a level of security not possible with multi-chip application solutions or with microcontrollers.

It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and

interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC™ 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC™ 4100S allows the customer to make.

2 Functional definition

2.1 CPU and memory subsystem

2.1.1 CPU

The Cortex®-M0+ CPU in the PSoC™ 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC™ 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

2.1.2 Flash

The PSoC™ 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

2.1.3 SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

2.1.4 SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

2.2 System resources

2.2.1 Power system

The power system is described in detail in the section Power. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC™ 4100S operates with a single external supply over the range of either 1.8 V ± 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC™ 4100S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched OFF; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

2.2.2 Clock system

PSoC™ 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC™ 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz watch crystal oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

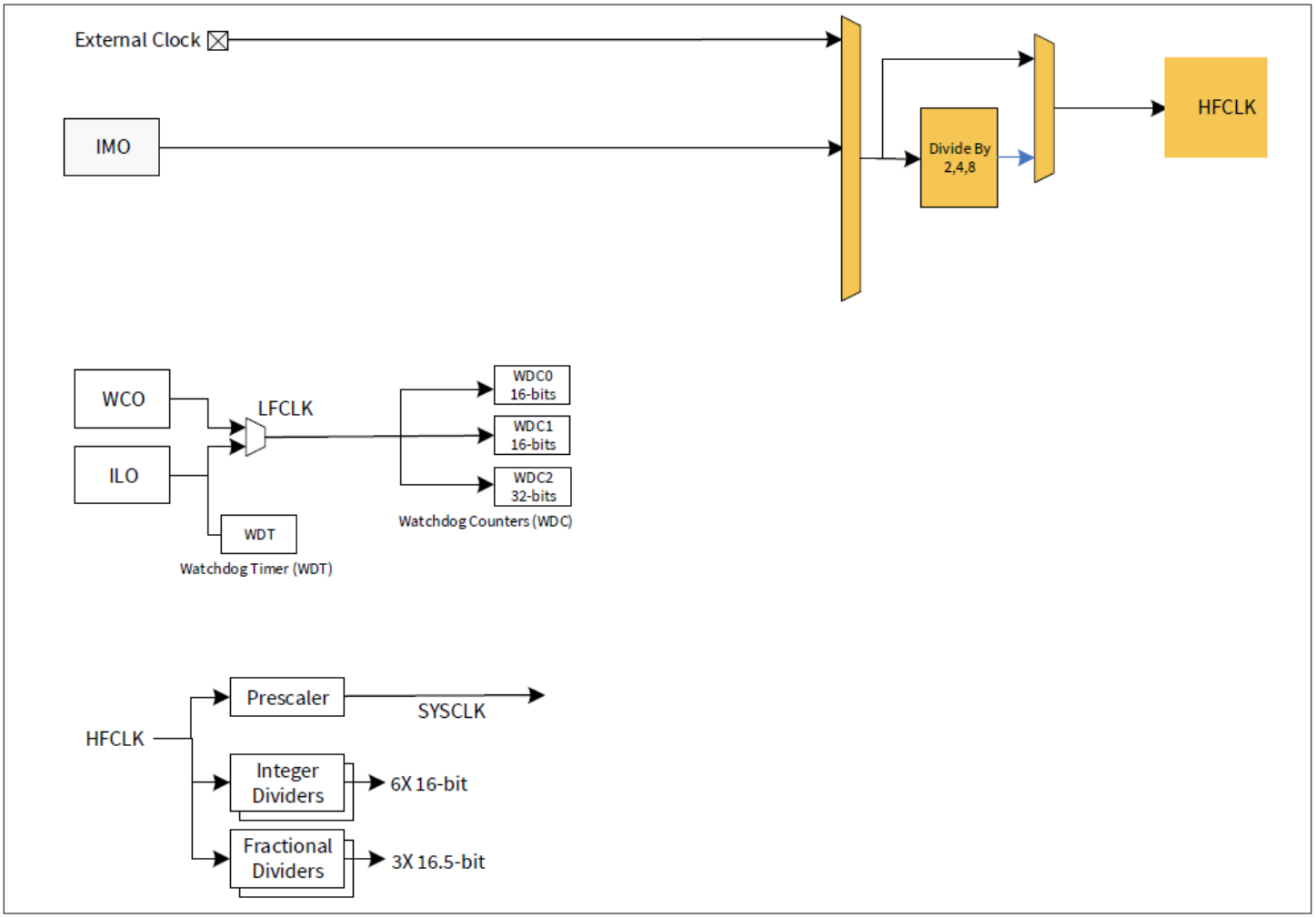


Figure 4 PSoC™ 4100S MCU clocking architecture

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC™ 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC™ Creator.

2.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4100S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Infineon provided calibration settings is ±2%.

2.2.4 ILO clock source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

2.2.5 Watch crystal oscillator (WCO)

The PSoC™ 4100S clock subsystem also implements a low-frequency (32 kHz watch crystal) oscillator that can be used for precision timing applications. The WCO block allows locking the IMO to the 32 kHz oscillator.

2.2.6 Watchdog timer and counters

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause Register, which is firmware readable. The watchdog counters can be used to implement a real-time clock using the 32-kHz WCO.

2.2.7 Reset

The PSoC™ 4100S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

2.3 Analog blocks

2.3.1 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The sample-and-hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

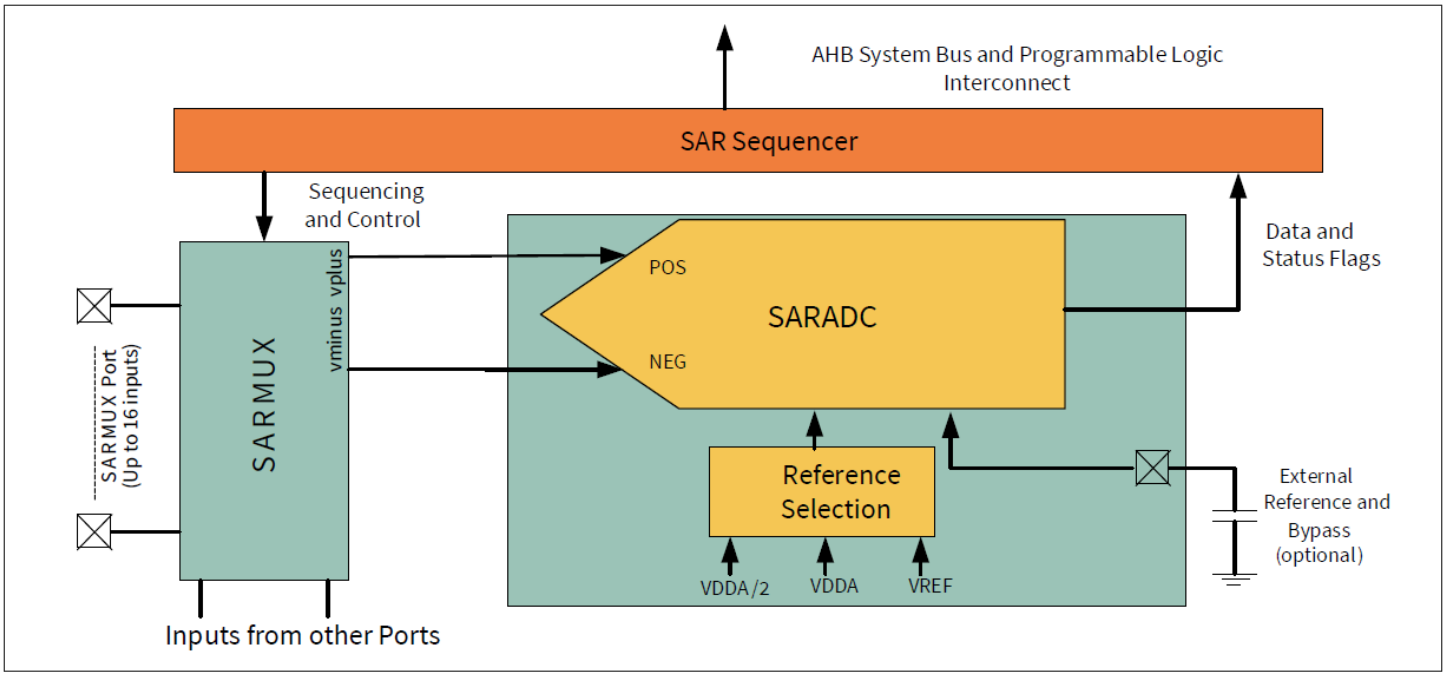


Figure 5 SAR ADC

2.3.2 Two opamps (continuous-time block; CTB)

The PSoC™ 4100S has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

2.3.3 Low-power comparators (LPC)

The PSoC™ 4100S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

2.3.4 Current DACs

The PSoC™ 4100S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

2.3.5 Analog multiplexed buses

The PSoC™ 4100S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O ports.

2.4 Programmable digital blocks

The smart I/O block is a fabric of switches and LUTs that allows boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

2.5 Fixed function digital

2.5.1 Timer/Counter/PWM (TCPWM) block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC™ 4100S.

2.5.2 Serial communication block (SCB)

The PSoC™ 4100S has three serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC™ 4100S and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

The PSoC™ 4100S is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not over-voltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

2.6 GPIO

The PSoC™ 4100S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down

- Strong pull-up with weak pull-down
- Open drain with strong pull-down
- Open drain with strong pull-up
- Strong pull-up with strong pull-down
- Weak pull-up with weak pull-down

- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC™ 4100S).

2.7 Special function peripherals

2.7.1 CAPSENSE™

CAPSENSE™ is supported in the PSoC™ 4100S through a CAPSENSE™ Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CAPSENSE™ function can thus be provided on any available pin or group of pins in a system under software control. A PSoC™ Creator component is provided for the CAPSENSE™ block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CAPSENSE™ block has two IDACs, which can be used for general purposes if CAPSENSE™ is not being used (both IDACs are available in that case) or if CAPSENSE™ is used without water tolerance (one IDAC is available).

The CAPSENSE™ block also provides a 10-bit slope ADC function which can be used in conjunction with the CAPSENSE™ function.

The CAPSENSE™ block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

2.7.2 LCD segment drive

The PSoC™ 4100S has an LCD controller, which can drive up to 4 commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM. Digital correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

3 Pinouts

Table 1 provides the pin list for PSoC™ 4100S for the 48LD TQFP, 44LD TQFP, 40L QFN, 32-lead QFN, and 35-ball CSP packages. All port pins support GPIO.

Table 1 Pin list

48LD TQFP		44LD TQFP		40L QFN		32-lead QFN		35-ball WLCSP	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
1	P1.7/VREF	44	P1.7/VREF	40	P1.7/VREF	1	P1.7/VREF	E7	P1.7/VREF
		1	VSSD						
2	P2.0	2	P2.0	1	P2.0	2	P2.0		
3	P2.1	3	P2.1	2	P2.1	3	P2.1		
4	P2.2	4	P2.2	3	P2.2	4	P2.2	D3	P2.2
5	P2.3	5	P2.3	4	P2.3	5	P2.3	E4	P2.3
6	P2.4	6	P2.4	5	P2.4			E5	P2.4
7	P2.5	7	P2.5	6	P2.5	6	P2.5	E6	P2.5
8	P2.6	8	P2.6	7	P2.6	7	P2.6	E3	P2.6
9	P2.7	9	P2.7	8	P2.7	8	P2.7	E2	P2.7
10	VSSD	10	VSSD	9	VSSD				
12	P3.0	11	P3.0	10	P3.0	9	P3.0	E1	P3.0
13	P3.1	12	P3.1	11	P3.1	10	P3.1	D2	P3.1
14	P3.2	13	P3.2	12	P3.2	11	P3.2	D1	P3.2
16	P3.3	14	P3.3	13	P3.3	12	P3.3	C1	P3.3
17	P3.4	15	P3.4	14	P3.4			C2	P3.4
18	P3.5	16	P3.5	15	P3.5				
19	P3.6	17	P3.6	16	P3.6				
20	P3.7	18	P3.7	17	P3.7				
21	VDDD	19	VDDD						
22	P4.0	20	P4.0	18	P4.0	13	P4.0	B1	P4.0
23	P4.1	21	P4.1	19	P4.1	14	P4.1	B2	P4.1
24	P4.2	22	P4.2	20	P4.2	15	P4.2	A2	P4.2
25	P4.3	23	P4.3	21	P4.3	16	P4.3	A1	P4.3
28	P0.0	24	P0.0	22	P0.0	17	P0.0	C3	P0.0
29	P0.1	25	P0.1	23	P0.1	18	P0.1	A5	P0.1
30	P0.2	26	P0.2	24	P0.2	19	P0.2	A4	P0.2
31	P0.3	27	P0.3	25	P0.3	20	P0.3	A3	P0.3
32	P0.4	28	P0.4	26	P0.4	21	P0.4	B3	P0.4
33	P0.5	29	P0.5	27	P0.5	22	P0.5	A6	P0.5

(table continues...)

Table 1 (continued) Pin list

48LD TQFP		44LD TQFP		40L QFN		32-lead QFN		35-ball WLCSP	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
34	P0.6	30	P0.6	28	P0.6	23	P0.6	B4	P0.6
35	P0.7	31	P0.7	29	P0.7			B5	P0.7
36	XRES	32	XRES	30	XRES	24	XRES	B6	XRES
37	VCCD	33	VCCD	31	VCCD	25	VCCD	A7	VCCD
38	VSSD					26	VSSD	B7	VSS
39	VDDD	34	VDDD	32	VDDD			C7	VDD
40	VDDA	35	VDDA	33	VDDA	27	VDD	C7	VDD
41	VSSA	36	VSSA	34	VSSA	28	VSSA	B7	VSS
42	P1.0	37	P1.0	35	P1.0	29	P1.0	C4	P1.0
43	P1.1	38	P1.1	36	P1.1	30	P1.1	C5	P1.1
44	P1.2	39	P1.2	37	P1.2	31	P1.2	C6	P1.2
45	P1.3	40	P1.3	38	P1.3	32	P1.3	D7	P1.3
46	P1.4	41	P1.4	39	P1.4			D4	P1.4
47	P1.5	42	P1.5					D5	P1.5
48	P1.6	43	P1.6					D6	P1.6

Note Pins 11, 15, 26, and 27 are No Connects (NC) on the 48LD TQFP.

Descriptions of the power pins are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ± 5%)

VDD: Power supply to all sections of the chip

VSS: Ground for all sections of the chip

3.1 Alternate pin functions

Each port pin can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CAPSENSE™ pin. The pin assignments are shown in Table 2.

Table 2 Alternate pin functions

Port/ Pin	Analog	Smart I/O	Alternate function 1	Alternate function 2	Alternate function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0

(table continues...)

Table 2 (continued) Alternate pin functions

Port/ Pin	Analog	Smart I/O	Alternate function 1	Alternate function 2	Alternate function 3	Deep Sleep 1	Deep Sleep 2
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						scb[2].spi_select0
P0.4	wco.wco_in			scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1		scb[1].spi_clk:1
P0.7			tcpwm.line[0]:2	scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0	ctb0_oa0+		tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0_oa0–		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0_oa0_out		tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	ctb0_oa1_out		tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.4	ctb0_oa1–						scb[0].spi_select1:1
P1.5	ctb0_oa1+						scb[0].spi_select2:1
P1.6	ctb0_oa0+						scb[0].spi_select3:1
P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1						scb[2].spi_clk
P2.0	sarmux[0]	SmartIo[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	SmartIo[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux[2]	SmartIo[0].io[2]					scb[1].spi_clk:2
P2.3	sarmux[3]	SmartIo[0].io[3]					scb[1].spi_select0:2

(table continues...)

Table 2 (continued) Alternate pin functions

Port/ Pin	Analog	Smart I/O	Alternate function 1	Alternate function 2	Alternate function 3	Deep Sleep 1	Deep Sleep 2
P2.4	sarmux[4]	SmartIo[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux[5]	SmartIo[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux[6]	SmartIo[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux[7]	SmartIo[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0		SmartIo[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		SmartIo[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		SmartIo[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		SmartIo[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		SmartIo[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		SmartIo[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		SmartIo[1].io[6]	tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		SmartIo[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

4 Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC™ 4100S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

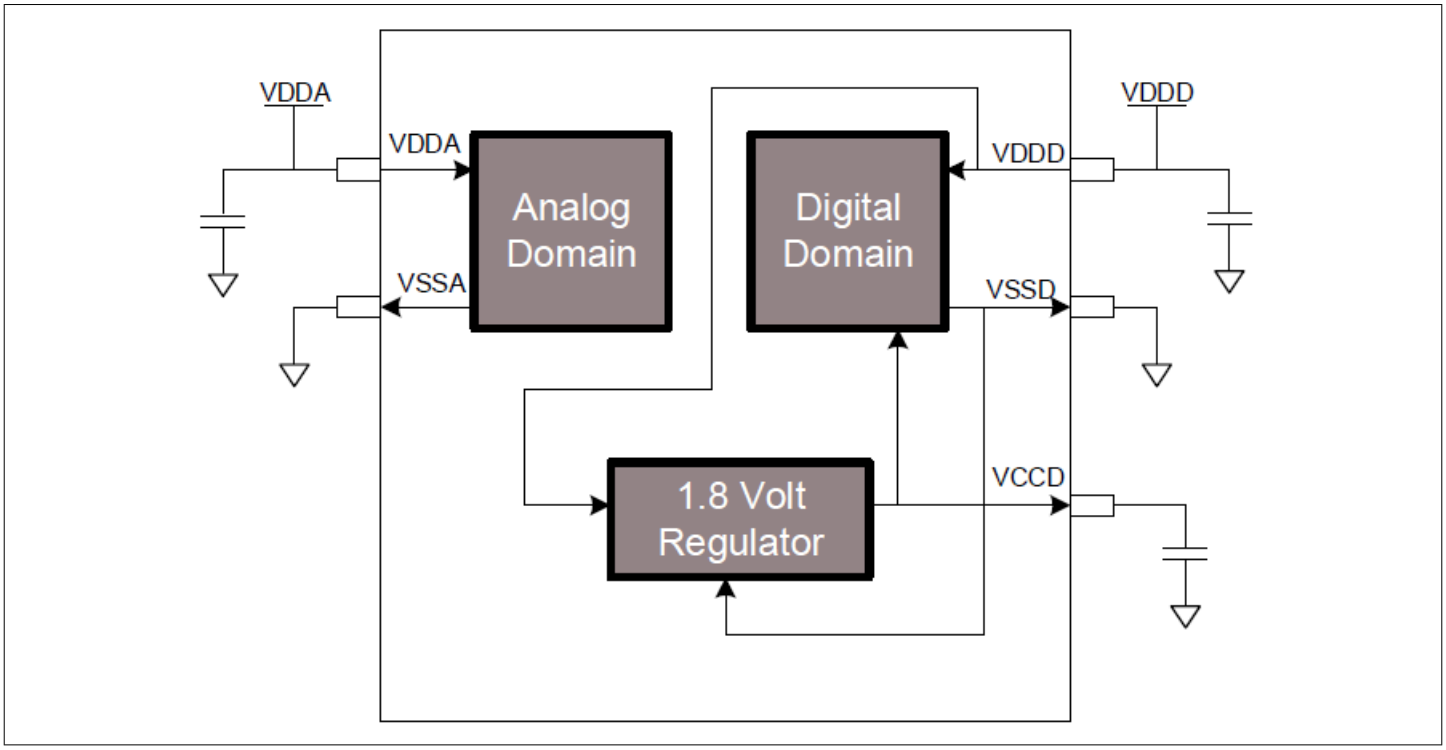


Figure 6 Power supply connections

There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is 1.8 V ± 5% (externally regulated; 1.71 V to 1.89 V, internal regulator bypassed).

4.1 Mode 1: 1.8 V to 5.5 V external supply

In this mode, the PSoC™ 4100S is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC™ 4100S supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

4.2 Mode 2: 1.8 V ± 5% external supply

In this mode, the PSoC™ 4100S is powered by an external power supply that must be within the range of 1.71 V to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 7 shows an example of a bypass scheme.

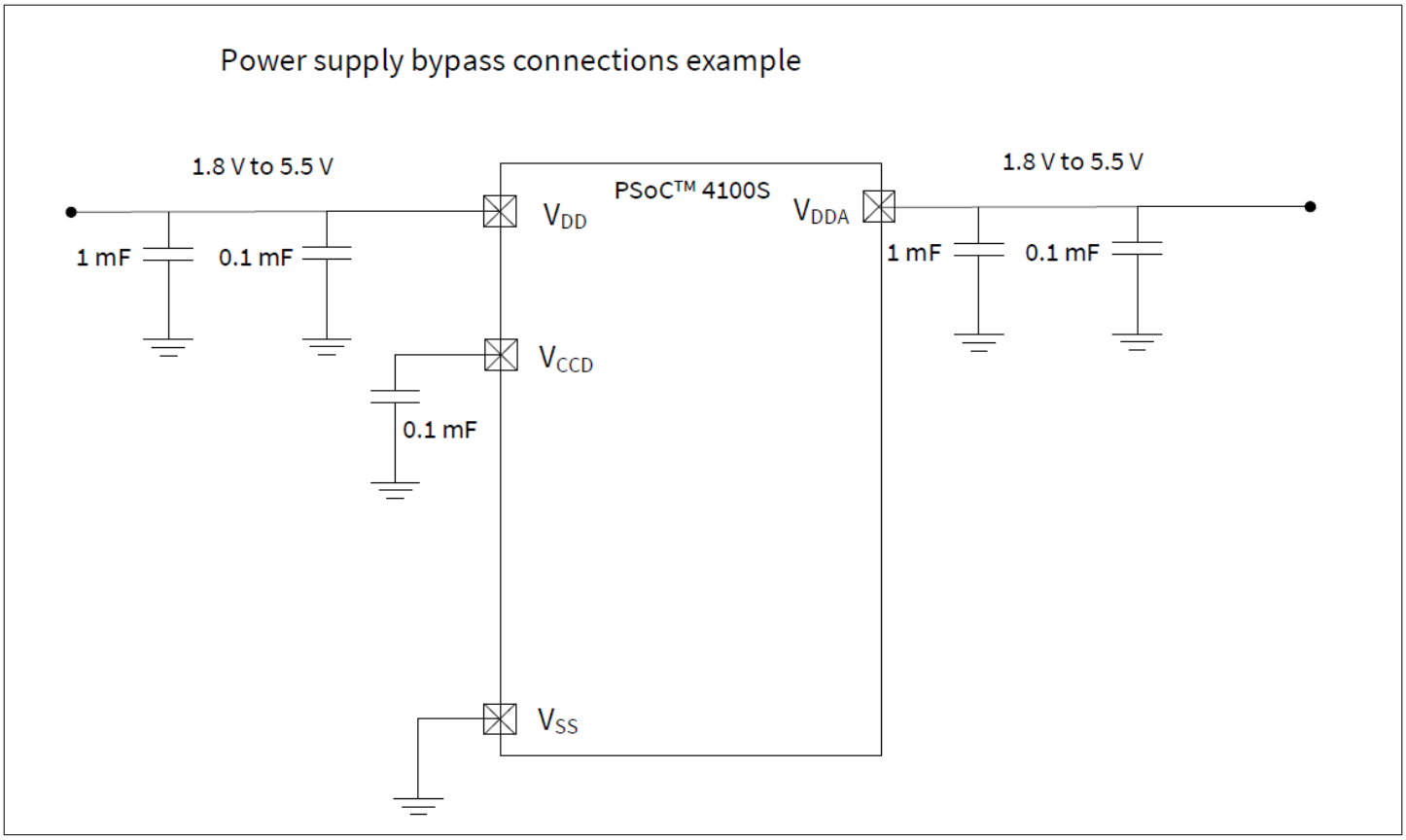


Figure 7 External supply range from 1.8 V to 5.5 V with internal regulator active

5 Electrical specifications

5.1 Absolute maximum ratings

Table 3 Absolute maximum ratings[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SS}	–0.5	–	6	V	–
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95		–
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} + 0.5		–
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–		–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

1) Usage above the absolute maximum conditions listed in Table 3 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

5.2 Device level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 125°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 4 DC specifications

Typical values measured at V_{DD} = 3.3 V and 25°C.

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	Internally regulated supply
SID255	V_{DD}	Power supply input voltage ($V_{CCD} = V_{DDD} = V_{DDA}$)	1.71	–	1.89		Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–		–
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–		

(table continues...)

Table 4 (continued) DC specifications

Typical values measured at V_{DD} = 3.3 V and 25°C.

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and 25°C.							
SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.8	2.7	mA	Max is at 85°C and 5.5 V
SID16	I_{DD8}	Execute from flash; CPU at 24 MHz	–	3.0	4.75		
SID19	I_{DD11}	Execute from flash; CPU at 48 MHz	–	5.4	6.85		
Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)							
SID22	IDD17	I^2C wakeup WDT, and comparators on	–	1.7	2.2	mA	6 MHz. Max is at 85°C and 5.5 V.
SID25	IDD20	I^2C wakeup, WDT, and comparators on.	–	2.2	2.5		12 MHz. Max is at 85°C and 5.5 V.
Sleep Mode, V_{DDD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	IDD23	I^2C wakeup, WDT, and comparators on	–	0.7	0.9	mA	6 MHz. Max is at 85°C and 5.5 V.
SID28A	IDD23A	I^2C wakeup, WDT, and comparators on	–	1	1.2		12 MHz. Max is at 85°C and 5.5 V.
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	60	µA	Max is at 3.6 V and 85°C.
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V (Regulator on)							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	60	µA	Max is at 5.5 V and 85°C.
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	65	µA	Max is at 1.89 V and 85°C.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–

Table 5 AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DD} \le 5.5$
SID49[1)]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	–
SID50[1)]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		–

1) Guaranteed by characterization.

5.2.1 GPIO

Table 6 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID57	V_{IH}[1]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}		
SID241	V_{IH}[1]	LVTTL input, V_{DDD} < 2.7 V	0.7 × V_{DDD}	–	–		–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}		–
SID243	V_{IH}[1]	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	V_{DDD} – 0.6	–	–		I_{OH} = 4 mA, V_{DDD} ≥ 3 V
SID60	V_{OH}	Output voltage high level	V_{DDD} – 0.5	–	–		I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 10 mA, V_{DDD} ≥ 3 V
SID62A	V_{OL}	Output voltage low level	–	–	0.4		I_{OL} = 3 mA, V_{DDD} ≥ 3 V
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DDD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67[2]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DDD} ≥ 2.7 V
SID68[2]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		V_{DD} < 4.5 V
SID68A[2]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		
SID69[2]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID69A[2]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

1) V_{IH} must not exceed V_{DDD} + 0.2 V.
2) Guaranteed by characterization.

Table 7 GPIO AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time in Fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in Fast strong mode	2	–	12		
SID72	T_{RISES}	Rise time in Slow strong mode	10	–	60	–	
SID73	T_{FALLS}	Fall time in Slow strong mode	10	–	60	–	
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V Fast strong mode	–	–	16.7		
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Slow strong mode	–	–	7		
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V Slow strong mode.	–	–	3.5		
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48		90/10% V_{IO}

5.2.2 XRES

Table 8 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}		
SID79	R_{PULLUP}	Pull-up resistor	–	60	–	kΩ	–
SID80	C_{IN}	Input capacitance	–	–	7	pF	–
SID81[1)]	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5 V
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

1) Guaranteed by characterization.

Table 9 XRES AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID83[1)]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–
BID194[1)]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

1) Guaranteed by characterization

5.3 Analog peripherals

5.3.1 CTBm Opamp

Table 10 CTBm Opamp specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
	I_{DD}	Opamp block current, external load					
SID269	I_{DD_HI}	Power = High	–	1100	1850	µA	–
SID270	I_{DD_MED}	Power = Medium	–	550	950		–
SID271	I_{DD_LOW}	Power = Low	–	150	350		–
	G_{BW}	Load = 20 pF, 0.1 mA V_{DDA} = 2.7 V					
SID272	G_{BW_HI}	Power = High	6	–	–	MHz	Input and output are 0.2 V to V_{DDA} – 0.2 V
SID273	G_{BW_MED}	Power = Medium	3	–	–		
SID274	G_{BW_LO}	Power = Low	–	1	–		
	I_{OUT_MAX}	V_{DDA} = 2.7 V, 500 mV from rail					
SID275	$I_{OUT\_MAX\_HI}$	Power = High	10	–	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID276	$I_{OUT\_MAX\_MID}$	Power = Medium	10	–	–		
SID277	$I_{OUT\_MAX\_LO}$	Power = Low	–	5	–		
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail					
SID278	$I_{OUT\_MAX\_HI}$	Power = High	4	–	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID279	$I_{OUT\_MAX\_MID}$	Power = Medium	4	–	–		
SID280	$I_{OUT\_MAX\_LO}$	Power = Low	–	2	–		
	I_{DD_Int}	Opamp block current, internal load					
SID269_I	$I_{DD\_HI\_Int}$	Power = High	–	1500	1700	µA	–
SID270_I	$I_{DD\_MED\_Int}$	Power = Medium	–	700	900		–

(table continues...)

Table 10 (continued) CTBm Opamp specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID271_I	$I_{DD\_LOW\_Int}$	Power = Low	–	–	–		–
	G_{BW}	V_{DDA} = 2.7 V	–	–	–		–
SID272_I	$G_{BW\_HI\_Int}$	Power = High	8	–	–	MHz	Output is 0.25 V to V_{DDA} – 0.25 V
		General opamp specs for both internal and external modes					
SID281	V_{IN}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA} – 0.2	V	–
SID282	V_{CM}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA} – 0.2		–
	V_{OUT}	V_{DDA} = 2.7 V					
SID283	V_{OUT_1}	Power = High, Iload = 10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID284	V_{OUT_2}	Power = High, Iload = 1 mA	0.2	–	V_{DDA} – 0.2		–
SID285	V_{OUT_3}	Power = Medium, Iload = 1 mA	0.2	–	V_{DDA} – 0.2		–
SID286	V_{OUT_4}	Power = Low, Iload = 0.1 mA	0.2	–	V_{DDA} – 0.2		–
SID288	V_{OS_TR}	Offset voltage, trimmed	–1.0	±0.5	1.0	mV	High mode, input 0 V to V_{DDA} – 0.2 V
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to V_{DDA} – 0.2 V
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to V_{DDA} – 0.2 V
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–		Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V_{DDA} – 0.2 V, Output is 0.2 V to V_{DDA} – 0.2 V

(table continues...)

Table 10 (continued) CTBm Opamp specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V_{DDD} = 3.6 V, high-power mode, input is 0.2 V to V_{DDA} – 0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, Power = High	–	72	–	nV/rtHz	Input and output are at 0.2 V to V_{DDA} – 0.2 V
SID295	VN3	Input-referred, 10 kHz, Power = High	–	28	–		
SID296	VN4	Input-referred, 100 kHz, Power = High	–	15	–		
SID297	C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V_{DDA} = 2.7 V	6	–	–	V/µs	–
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	–
	COMP_MODE	Comparator mode; 50 mV drive, T_{rise} = T_{fall} (approx.)					
SID300	TPD1	Response time; Power = High	–	150	–	ns	Input is 0.2 V to V_{DDA} – 0.2 V
SID301	TPD2	Response time; Power = Medium	–	500	–		
SID302	TPD3	Response time; Power = Low	–	2500	–		
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW					
SID_DS_1	$I_{DD\_HI\_M1}$	Mode 1, high current	–	1400	–	µA	25°C

(table continues...)

Table 10 (continued) CTBm Opamp specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID_DS_2	$I_{DD\_MED\_M1}$	Mode 1, medium current	–	700	–		
SID_DS_3	$I_{DD\_LOW\_M1}$	Mode 1, low current	–	200	–		
SID_DS_4	$I_{DD\_HI\_M2}$	Mode 2, high current	–	120	–		
SID_DS_5	$I_{DD\_MED\_M2}$	Mode 2, medium current	–	60	–		
SID_DS_6	$I_{DD\_LOW\_M2}$	Mode 2, low current	–	15	–		
SID_DS_7	$G_{BW\_HI\_M1}$	Mode 1, high current	–	4	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 0.2 V
SID_DS_8	$G_{BW\_MED\_M1}$	Mode 1, medium current	–	2	–		
SID_DS_9	$G_{BW\_LOW\_M1}$	Mode 1, low current	–	0.5	–		
SID_DS_10	$G_{BW\_HI\_M2}$	Mode 2, high current	–	0.5	–		
SID_DS_11	$G_{BW\_MED\_M2}$	Mode 2, medium current	–	0.2	–		
SID_DS_12	$G_{BW\_Low\_M2}$	Mode 2, low current	–	0.1	–		
SID_DS_13	$V_{OS\_HI\_M1}$	Mode 1, high current	–	5	–	mV	With trim 25°C, 0.2 V to V_{DDA} – 0.2 V
SID_DS_14	$V_{OS\_MED\_M1}$	Mode 1, medium current	–	5	–		
SID_DS_15	$V_{OS\_LOW\_M1}$	Mode 1, low current	–	5	–		
SID_DS_16	$V_{OS\_HI\_M2}$	Mode 2, high current	–	5	–		
SID_DS_17	$V_{OS\_MED\_M2}$	Mode 2, medium current	–	5	–		
SID_DS_18	$V_{OS\_LOW\_M2}$	Mode 2, low current	–	5	–		
SID_DS_19	$I_{OUT\_HI\_M1}$	Mode 1, high current	–	10	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, medium current	–	10	–		
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, low current	–	4	–		
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, high current	–	1	–		–
SID_DS_23	$I_{OUT\_MED\_M2}$	Mode 2, medium current	–	1	–		–
SID_DS_24	$I_{OUT\_LOW\_M2}$	Mode 2, low current	–	0.5	–		–

5.3.2 Comparator

Table 11 Comparator DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID84	$V_{OFFSET1}$	Input offset voltage, factory trim	–	–	±10	mV	–
SID85	$V_{OFFSET2}$	Input offset voltage, custom trim	–	–	±4		–
SID86	V_{HYST}	Hysteresis when enabled	–	10	35		–
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} – 0.1	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}		–
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} – 1.15		$V_{DDD} \geq 2.2$ V at –40°C
SID88	C_{MRR}	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq 2.7$ V
SID88A	C_{MRR}	Common mode rejection ratio	42	–	–		
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	–
SID248	I_{CMP2}	Block current, low power mode	–	–	100		–
SID259	I_{CMP3}	Block current in ultra low-power mode	–	–	6		$V_{DDD} \geq 2.2$ V at –40°C
SID90	Z_{CMP}	DC Input impedance of comparator	35	–	–	MΩ	–

Table 12 Comparator AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	–
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		–
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	µs	$V_{DDD} \geq 2.2$ V at –40°C

5.3.3 Temperature sensor

Table 13 Temperature sensor specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID93	TSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40°C to +85°C

5.3.4 SAR

Table 14 SAR specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SAR ADC DC specifications							
SID94	A_RES	Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		–
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	–
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}		–
SID103	A_INRES	Input resistance	–	–	2.2	kΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–
SID260	VREFSAR	Trimmed internal reference to SAR	1.188	1.2	1.212	V	–
SAR ADC AC specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–		Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	–
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A_samp/2	kHz	–
SID111	A_INL	Integral non linearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 V to V_{DD}
SID111A	A_INL	Integral non linearity. V_{DDD} = 1.71 V to 3.6 V, 1 Msps	–1.5	–	1.7		V_{REF} = 1.71 V to V_{DD}
SID111B	A_INL	Integral non linearity. V_{DD} = 1.71 V to 5.5 V, 500 ksps	–1.5	–	1.7		V_{REF} = 1 V to V_{DD}

(table continues...)

Table 14 (continued) SAR specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID112	A_DNL	Differential non linearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1	–	2.2		V_{REF} = 1 V to V_{DD}
SID112A	A_DNL	Differential non linearity. V_{DD} = 1.71 V to 3.6 V, 1 Msps	–1	–	2		V_{REF} = 1.71 V to V_{DD}
SID112B	A_DNL	Differential non linearity. V_{DD} = 1.71 V to 5.5 V, 500 ksps	–1	–	2.2		V_{REF} = 1 V to V_{DD}
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz
SID261	FSARINTREF	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution

5.3.5 CSD and IDAC

Table 15 CSD and IDAC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25°C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25		V_{DD} > 1.75 V (with ripple), 25°C T_A, Parasitic capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	µA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
SID.CSD#15	V_{REF}	Voltage reference for CSD and comparator	0.6	1.2	V_{DDA} – 0.6	V	V_{DDA} – 0.6 or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External voltage reference for CSD and comparator	0.6	–	V_{DDA} – 0.6		V_{DDA} – 0.6 or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	µA	–
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750		–

(table continues...)

Table 15 (continued) CSD and IDAC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ± 5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	V_{DDA} – 0.6		V_{DDA} – 0.6 or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	–
SID310	IDAC1INL	INL	–2	–	2		INL is ±5.5 LSB for V_{DDA} < 2 V
SID311	IDAC2DNL	DNL	–1	–	1		–
SID312	IDAC2INL	INL	–2	–	2		INL is ±5.5 LSB for V_{DDA} < 2 V
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. V_{DDA} > 2 V.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1 (7 bits) in medium range	34	–	41		LSB = 300-nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1 (7 bits) in high range	275	–	330		LSB = 2.4-µA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5		LSB = 75-nA typ.
SID314D	IDAC1CRT22	Output current of IDAC1 (7 bits) in medium range, 2X mode	69	–	82		LSB = 600-nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1 (7 bits) in high range, 2X mode	540	–	660		LSB = 4.8-µA typ.
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4		LSB = 37.5-nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41		LSB = 300-nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330		LSB = 2.4-µA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5		LSB = 75-nA typ.

(table continues...)

Table 15 (continued) CSD and IDAC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID315D	IDAC2CRT22	Output current of IDAC2 (7 bits) in medium range, 2X mode	69	–	82		LSB = 600-nA typ.
SID315E	IDAC2CRT32	Output current of IDAC2 (7 bits) in high range, 2X mode	540	–	660		LSB = 4.8-µA typ.
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5		LSB = 37.5-nA typ.
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82		LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	–
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6		LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8		LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10		Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

5.3.6 10-bit CapSense ADC

Table 16 10-bit CAPSENSE™ ADC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	–
SIDA98	A_GAINERR	Gain error	–	–	±2	%	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA99	A_OFFSET	Input offset voltage	–	–	3	mV	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA100	A_ISAR	Current consumption	–	–	0.25	mA	–
SIDA101	A_VINS	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	–
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	–
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	–
SIDA106	A_PSRR	Power supply rejection ratio	–	60	–	dB	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	–
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	21.3		Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	85.3		Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V_{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	V_{REF} = 2.4 V or greater

(table continues...)

Table 16 (continued) 10-bit CAPSENSE™ ADC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	–	–	1		–

5.4 Digital peripherals

5.4.1 Timer Counter Pulse-width Modulator (TCPWM)

Table 17 TCPWM specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events[1)]
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between Quadrature phase inputs

1) Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

5.4.2 I²C

Table 18 Fixed I²C DC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–

(table continues...)

Table 18 (continued) Fixed I²C DC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4		–

1) Guaranteed by characterization.

Table 19 Fixed I²C AC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Msps	–

1) Guaranteed by characterization.

5.4.3 SPI

Table 20 SPI DC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

1) Guaranteed by characterization.

Table 21 SPI AC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	FSPI	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	SID166
Fixed SPI Master Mode AC specifications							
SID167	TDMO	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC specifications							

(table continues...)

Table 21 (continued) SPI AC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	TDMI	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	TDSO	MISO valid after Sclock driving edge	–	–	42 + (3 × Tcpu)		$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	MISO valid after Sclock driving edge in External Clock mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL valid to first SCK valid edge	100	–	–		–

1) Guaranteed by characterization.

5.4.4 UART

Table 22 UART DC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312		–

1) Guaranteed by characterization.

Table 23 UART AC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

1) Guaranteed by characterization.

5.4.5 LCD

Table 24 LCD direct drive DC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–

(table continues...)

Table 24 (continued) LCD direct drive DC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID157	I_{LCDOP1}	LCD system operating current Vbias = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz. 25°C
SID158	I_{LCDOP2}	LCD system operating current Vbias = 3.3 V	–	2	–		32 × 4 segments. 50 Hz. 25°C

1) Guaranteed by characterization.

Table 25 LCD direct drive AC specifications[1)]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

1) Guaranteed by characterization.

5.5 Memory

5.5.1 Flash

Table 26 Flash DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 27 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID174	$T_{ROWWRITE}$[1)]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[1)]	Row erase time	–	–	16		–
SID176	$T_{ROWPROGRAM}$[1)]	Row program time after erase	–	–	4		–
SID178	$T_{BULKERASE}$[1)]	Bulk erase time (64 KB)	–	–	35		–
SID180[2)]	$T_{DEVPROG}$[1)]	Total device program time	–	–	7	Seconds	–
SID181[2)]	F_{END}	Flash endurance	100 K	–	–	Cycles	–
SID182[2)]	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	Years	–

(table continues...)

Table 27 (continued) Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID182A[2)]	–	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–		–
SID182B	–	Flash retention. $T_A \leq 105$ °C, 10K P/E cycles, ≤ three years at $T_A \geq 85$ °C	10	–	20	Years	–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		

1) It can take as much as 20 milliseconds to write to flash. During this time the device should not be Reset, or Flash operations may be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
2) Guaranteed by characterization.

5.6 System resources

5.6.1 Power-on reset (POR)

Table 28 Power-on reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up and power-down
SID185[1)]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	–
SID186[1)]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4		–

1) Guaranteed by characterization.

Table 29 Brown-out detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190[1)]	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.48	–	1.62	V	–
SID192[1)]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

1) Guaranteed by characterization

5.6.2 SWD interface

Table 30 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7		SWDCLK ≤ 1/3 CPU clock frequency
SID215[1)]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID216[1)]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–		–
SID217[1)]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T		–
SID217A[1)]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		–

1) Guaranteed by characterization.

5.6.3 IMO

Table 31 IMO DC specifications

(Guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180		–

Table 32 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID223[2)]	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2.0	%	At –40°C to 85°C, for industrial temperature range and original extended industrial range parts
SID223A[1) 2)]			–	–	±2.5	%	At –40°C to 105°C, for all extended industrial temperature range parts
SID223B[1) 2)]			–	–	±2.0	%	At –30°C to 105°C, for enhanced IMO extended industrial temperature range parts

(table continues...)

Table 32 (continued) IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID223C[1) 2)]			–	–	±1.5	%	At –20°C to 105°C, for enhanced IMO extended industrial temperature range parts
SID223D[1) 2)]			–	–	±1.25	%	At 0°C to 85°C, for enhanced IMO extended industrial temperature range parts
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

1) The enhanced IMO extended temperature range parts replace the original extended industrial temperature range parts. For details on how to identify enhanced IMO extended temperature range parts, please refer to KBA235887.
2) Evaluated by characterization. Does not take into account soldering or board-level effects.

5.6.4 ILO

Table 33 ILO DC specifications

(Guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID231[1)]	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	–

1) Guaranteed by characterization.

Table 34 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234[1)]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236[1)]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

1) Guaranteed by characterization.

5.6.5 WCO

Table 35 WCO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID398	FWCO	Crystal frequency	–	32.768	–	kHz	–
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	–
SID401	PD	Drive level	–	–	1	µW	–

(table continues...)

Table 35 (continued) WCO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID402	TSTART	Startup time	–	–	500	ms	–
SID403	CL	Crystal load capacitance	6	–	12.5	pF	–
SID404	C0	Crystal shunt capacitance	–	1.35	–		–
SID405	IWCO1	Operating current (high power mode)	–	–	8	mA	–
SID406	IWCO2	Operating current (low power mode)	–	–	1		–

5.6.6 External clock

Table 36 External clock specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID305[1)]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306[1)]	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	–

1) Guaranteed by characterization.

5.6.7 Block

Table 37 Block specs

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID262[1)]	$T_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	–

1) Guaranteed by characterization.

5.6.8 Smart I/O

Table 38 Smart I/O pass-through time (Delay in Bypass mode)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in Bypass mode	–	–	1.6	ns	–

6 Ordering information

The products for the PSoC™ 4100S family are listed in the following table.

Table 39 Ordering information

Category	Product	Features													Package					Temperature Range (°C)
		Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	ADC Sample rate	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	35-ball WLCSP (0.35mm pitch)	32-lead FN	40L QFN	48LD TQFP	44LD TQFP	
4124	CY8C4124FNI-S403T	24	16	4	2	0	1	0		2	5	2	8	31	X	–	–	–	–	–40°C to 85°C
	CY8C4124FNI-S413T	24	16	4	2	1	1	0		2	5	2	16	31	X	–	–	–	–	–40°C to 85°C
	CY8C4124LQI-S412T	24	16	4	2	1	1	0		2	5	2	16	27	–	X	–	–	–	–40°C to 85°C
	CY8C4124LQI-S413T	24	16	4	2	1	1	0		2	5	2	16	34	–	–	X		–	–40°C to 85°C
	CY8C4124AZI-S413T	24	16	4	2	1	1	0		2	5	2	16	36	–	–	–	X	–	–40°C to 85°C
	CY8C4124FNI-S433T	24	16	4	2	1	1	1	806 ksps	2	5	2	16	31	X	–	–	–	–	–40°C to 85°C
	CY8C4124FNQ-S433T	24	16	4	2	1	1	1	806 ksps	2	5	2	16	31	X	–	–	–	–	–40°C to 105°C
	CY8C4124LQI-S432T	24	16	4	2	1	1	1	806 ksps	2	5	2	16	27	–	X	–	–	–	–40°C to 85°C
	CY8C4124LQI-S433T	24	16	4	2	1	1	1	806 ksps	2	5	2	16	34	–	–	X	–	–	–40°C to 85°C
	CY8C4124AZI-S433T	24	16	4	2	1	1	1	806 ksps	2	5	2	16	36	–	–	–	X	–	–40°C to 85°C
4125	CY8C4125FNI-S423T	24	32	4	2	0	1	1	806 ksps	2	5	2	16	31	X	–	–	–	–	–40°C to 85°C
	CY8C4125LQI-S422T	24	32	4	2	0	1	1	806 ksps	2	5	2	16	27	–	X	–	–	–	–40°C to 85°C
	CY8C4125LQI-S423T	24	32	4	2	0	1	1	806 ksps	2	5	2	16	34	–	–	X	–	–	–40°C to 85°C
	CY8C4125AZI-S423T	24	32	4	2	0	1	1	806 ksps	2	5	2	16	36	–	–	–	X	–	–40°C to 85°C

(table continues...)

Table 39 (continued) Ordering information

Category	Product	Features													Package					Temperature Range (°C)
		Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	ADC Sample rate	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	35-ball WLCSP (0.35mm pitch)	32-lead FN	40L QFN	48LD TQFP	44LD TQFP	
	CY8C4125AXI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	36	–	–	–		X	–40°C to 85°C
	CY8C4125FNI-S413T	24	32	4	2	1	1	0		2	5	2	16	31	X	–	–	–	–	–40°C to 85°C
	CY8C4125LQI-S412T	24	32	4	2	1	1	0		2	5	2	16	27	–	X	–	–	–	–40°C to 85°C
	CY8C4125LQI-S413T	24	32	4	2	1	1	0		2	5	2	16	34	–	–	X	–	–	–40°C to 85°C
	CY8C4125AZI-S413T	24	32	4	2	1	1	0		2	5	2	16	36	–	–	–	X	–	–40°C to 85°C
	CY8C4125FNI-S433T	24	32	4	2	1	1	1	806 ksps	2	5	2	16	31	X	–	–	–	–	–40°C to 85°C
	CY8C4125FNQ-S433T	24	32	4	2	1	1	1	806 ksps	2	5	2	16	31	X	–	–	–	–	–40°C to 105°C
	CY8C4125LQI-S432	24	32	4	2	1	1	1	806 ksps	2	5	2	16	27	–	X	–	–	–	–40°C to 85°C
	CY8C4125LQQ-S432	24	32	4	2	1	1	1	806 ksps	2	5	2	16	27	–	X	–	–	–	–40°C to 105°C
	CY8C4125LQI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	34	–	–	X	–	–	–40°C to 85°C
	CY8C4125AZI-S433T	24	32	4	2	1	1	1	806 ksps	2	5	2	16	36	–	–	–	X	–	–40°C to 85°C
	CY8C4125AZQ-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	36	–	–	–	X	–	–40°C to 105°C
	CY8C4125AXI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	36	–	–	–	–	X	–40°C to 85°C
4126	CY8C4126AZI-S423T	24	64	8	2	0	1	1	806 ksps	2	5	3	16	36	–	–	–	X	–	–40°C to 85°C
	CY8C4126AZQ-S423	24	64	8	2	0	1	1	806 ksps	2	5	3	16	36	–	–	–	X	–	–40°C to 105°C

(table continues...)

Table 39 (continued) Ordering information

Category	Product	Features													Package					Temperature Range (°C)
		Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	ADC Sample rate	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	35-ball WLCSP (0.35mm pitch)	32-lead FN	40L QFN	48LD TQFP	44LD TQFP	
	CY8C4126AXI-S423	24	64	8	2	0	1	1	806 ksps	2	5	3	16	36	–	–	–	–	X	–40°C to 85°C
	CY8C4126AZI-S433T	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36	–	–	–	X	–	–40°C to 85°C
	CY8C4126AZQ-S433	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36	–	–	–	X	–	–40°C to 105°C
	CY8C4126AXI-S433	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36	–	–	–	–	X	–40°C to 85°C
	CY8C4126AXQ-S433	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36	–	–	–	–	X	–40°C to 105°C
4145	CY8C4145AZI-S423T	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36	–	–	–	X	–	–40°C to 85°C
	CY8C4145AZQ-S433	48	32	4	2	1	1	1	1 Msps	2	5	2	16	36	–	–	–	X	–	–40°C to 105°C
	CY8C4145AXI-S423	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36	–	–	–	–	X	–40°C to 85°C
	CY8C4145AXI-S433	48	32	4	2	1	1	1	1 Msps	2	5	2	16	36	–	–	–	–	X	–40°C to 85°C
	CY8C4145AXQ-S433	48	32	4	2	1	1	1	1 Msps	2	5	2	16	36	–	–	–	–	X	–40°C to 105°C
4146	CY8C4146FNI-S423T	48	64	8	2	0	1	1	1 Msps	2	5	3	16	31	X	–	–	–	–	–40°C to 85°C
	CY8C4146LQI-S422T	48	64	8	2	0	1	1	1 Msps	2	5	3	16	27	–	X	–	–	–	–40°C to 85°C
	CY8C4146LQQ-S422	48	64	8	2	0	1	1	1 Msps	2	5	3	16	27	–	X	–	–	–	–40°C to 105°C
	CY8C4146LQI-S423T	48	64	8	2	0	1	1	1 Msps	2	5	3	16	34	–	–	X	–	–	–40°C to 85°C
	CY8C4146AZI-S423T	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36	–	–	–	X	–	–40°C to 85°C

(table continues...)

Table 39 (continued) Ordering information

Category	Product	Features													Package					Temperature Range (°C)
		Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	ADC Sample rate	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	35-ball WLCSP (0.35mm pitch)	32-lead FN	40L QFN	48LD TQFP	44LD TQFP	
	CY8C4146AZQ-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36	–	–	–	X	–	–40°C to 105°C
	CY8C4146AXI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36	–	–	–	–	X	–40°C to 85°C
	CY8C4146AXQ-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36	–	–	–	–	X	–40°C to 105°C
	CY8C4146FNI-S433T	48	64	8	2	1	1	1	1 Msps	2	5	3	16	31	X	–	–	–	–	–40°C to 85°C
	CY8C4146FNQ-S433T	48	64	8	2	1	1	1	1 Msps	2	5	3	16	31	X	–	–	–	–	–40°C to 105°C
	CY8C4146LQI-S432T	48	64	8	2	1	1	1	1 Msps	2	5	3	16	27	–	X	–	–	–	–40°C to 85°C
	CY8C4146LQQ-S432T	48	64	8	2	1	1	1	1 Msps	2	5	3	16	27	–	X	–	–	–	–40°C to 105°C
	CY8C4146LQI-S433T	48	64	8	2	1	1	1	1 Msps	2	5	3	16	34	–	–	X	–	–	–40°C to 85°C
	CY8C4146AZI-S433T	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36	–	–	–	X	–	–40°C to 85°C
	CY8C4146AZQ-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36	–	–	–	X	–	–40°C to 105°C
	CY8C4146AXI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36	–	–	–	–	X	–40°C to 85°C
	CY8C4146AXQ-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36	–	–	–	–	X	–40°C to 105°C

The nomenclature used in the preceding table is based on the following part numbering convention:

Table 40 Nomenclature

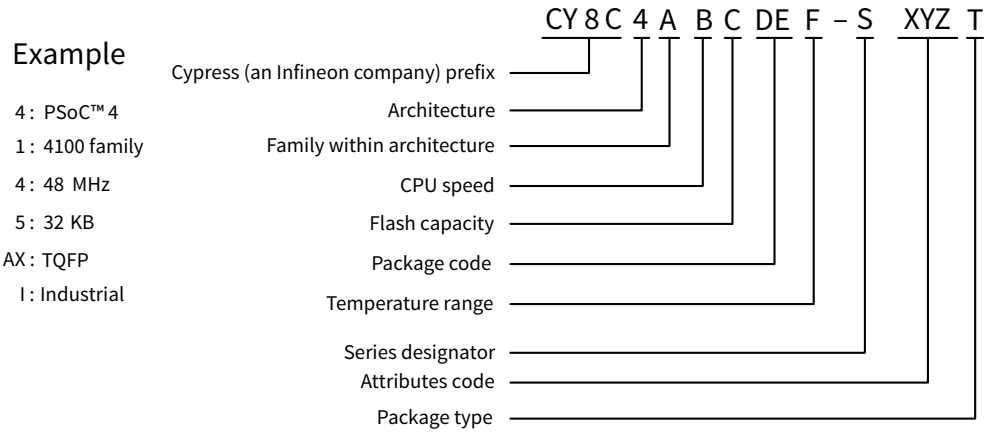
Field	Description	Values	Meaning
CY8C	Prefix		

(table continues...)

Table 40 (continued) Nomenclature

Field	Description	Values	Meaning
4	Architecture	4	PSoC™ 4
A	Family	1	4100 Family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package code	AX	TQFP (0.8 mm pitch)
		AZ	TQFP (0.5 mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature range	I	Industrial
		Q	Extended Industrial
S	Series designator	S	S-Series
		M	M-Series
		L	L-Series
XYZ	Attributes code	000-999	Code of feature set in the specific family
T	Package type		Tray
		T	Tape and Reel

The following is an example of a part number.



7 Packaging

The PSoC™ 4100S is offered in 48LD TQFP, 44LD TQFP, 40L QFN, 32-lead QFN, and 35-ball WLCSP packages. Table 41 provides the package dimensions and Infineon drawing numbers.

Table 41 Package list

Spec ID	Package	Description	Package drawing
BID20	48LD TQFP	7 × 7 × 1.4-mm height with 0.5-mm pitch	51-85135
BID20A	44LD TQFP	10 × 10 × 1.6-mm height with 0.8-mm pitch	51-85064
BID27	40L QFN	6 × 6 × 0.6-mm height with 0.5-mm pitch	001-80659
BID34A	32-lead QFN	5 × 5 × 0.6-mm height with 0.5-mm pitch	001-42168
BID34D	35-ball WLCSP	2.6 × 2.1 × 0.48-mm height with 0.35-mm pitch	002-09958

Table 42 Package thermal characteristics

Parameter	Description	Package	Min	Typ	Max	Unit	Details/ conditions
T_A	Operating ambient temperature	-	-40	25	105	°C	–
T_J	Operating junction temperature	–	-40	–	125		–
T_{JA}	Package θ_{JA}	48LD TQFP	–	74.8	–	°C/W	–
T_{JC}	Package θ_{JC}	48LD TQFP	–	35.7	–		–
T_{JA}	Package θ_{JA}	44LD TQFP	–	57.2	–		–
T_{JC}	Package θ_{JC}	44LD TQFP	–	17.5	–		–
T_{JA}	Package θ_{JA}	40L QFN	–	17.8	–		–
T_{JC}	Package θ_{JC}	40L QFN	–	2.8	–		–
T_{JA}	Package θ_{JA}	32-lead QFN	–	19.9	–		–
T_{JC}	Package θ_{JC}	32-lead QFN	–	4.3	–		–
T_{JA}	Package θ_{JA}	35-ball WLCSP	–	43	–		–
T_{JC}	Package θ_{JC}	35-ball WLCSP	–	0.3	–		–

Table 43 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
All	260°C	30 seconds

Table 44 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All except WLCSP	MSL 3
35-ball WLCSP	MSL 1

7.1 Package diagrams

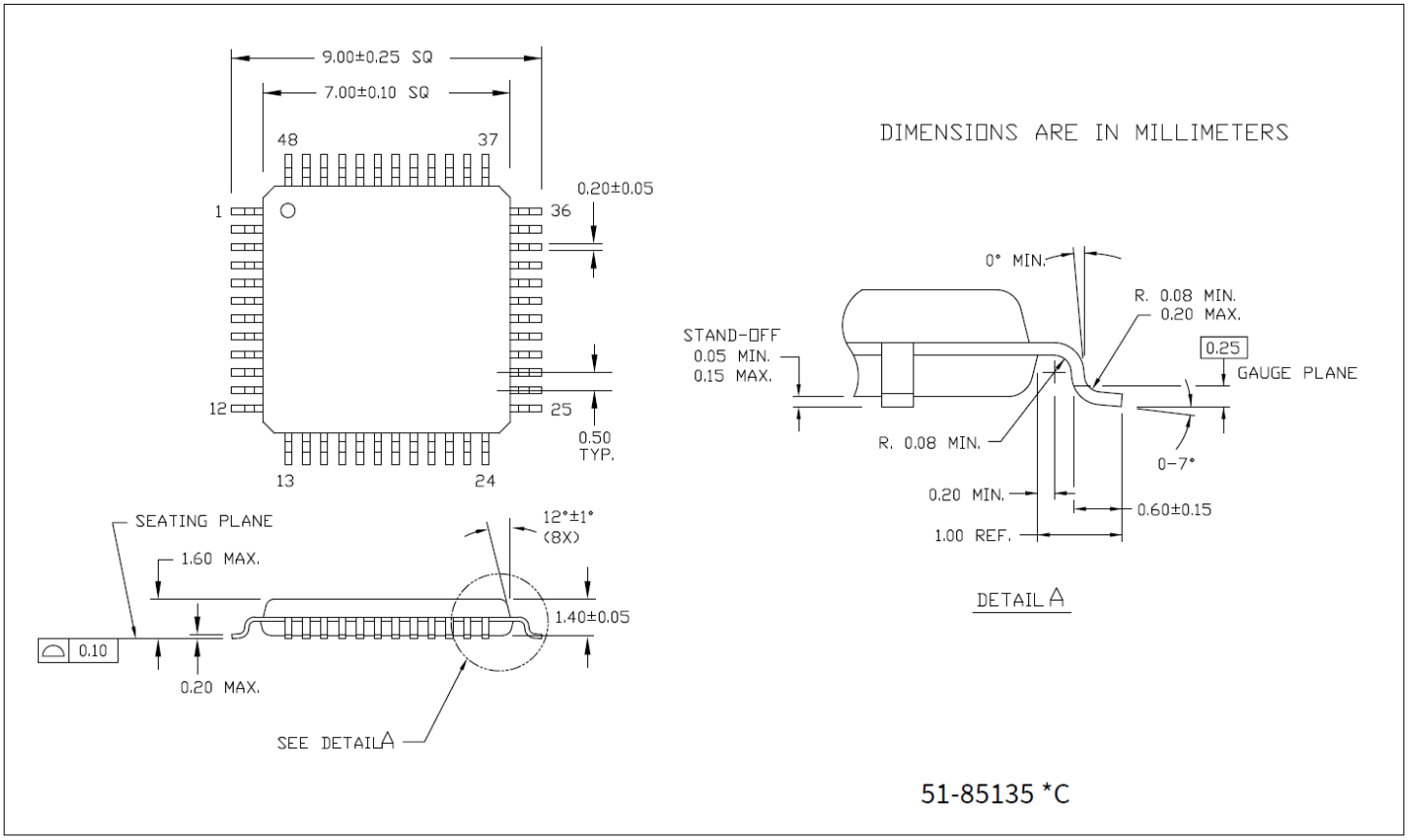


Figure 8 48LD TQFP 7×7×1.4 MM A48 package outline (PG-TQFP-48), 51-85135

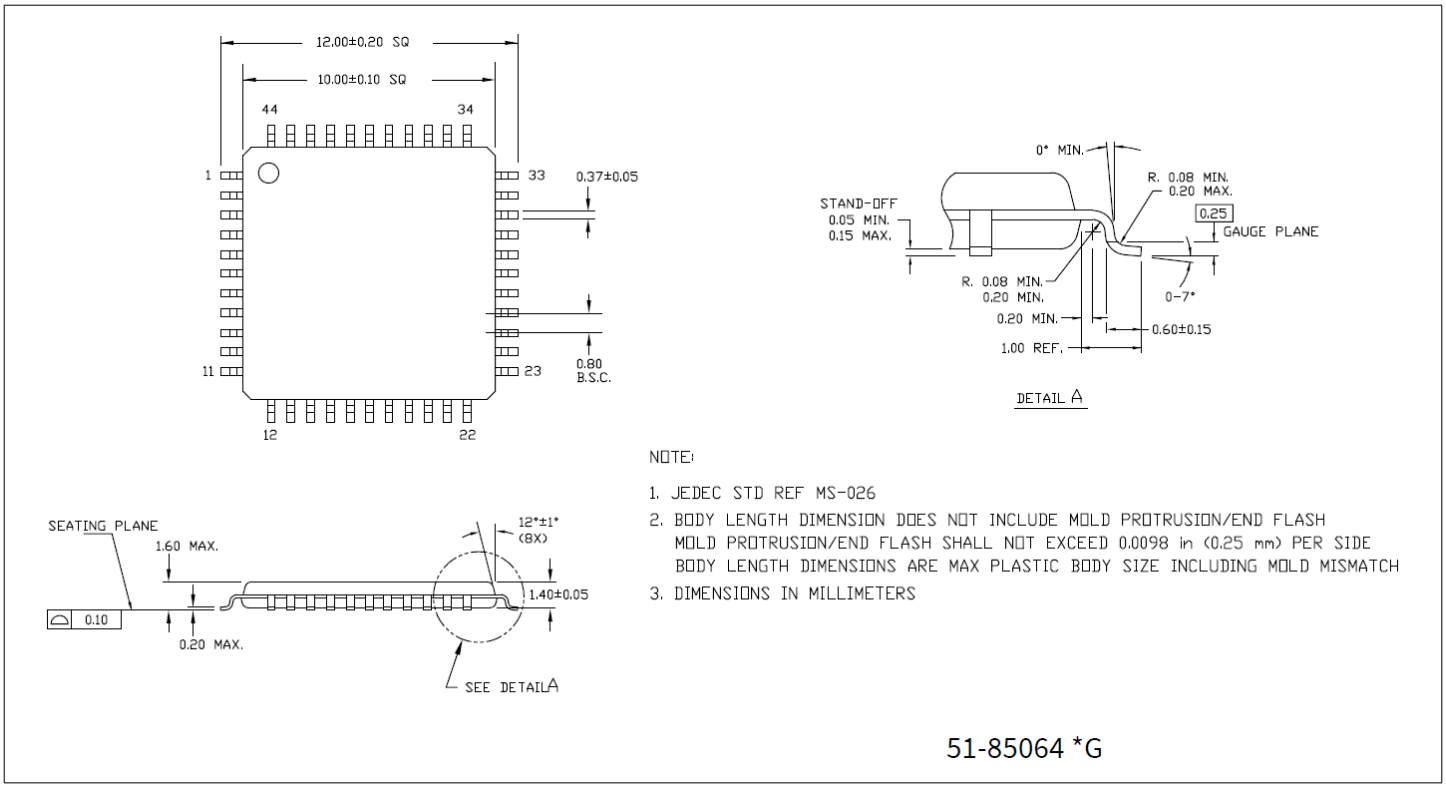


Figure 9 44LD TQFP 10×10×1.4 MM A44S package outline (PG-TQFP-44), 51-85064

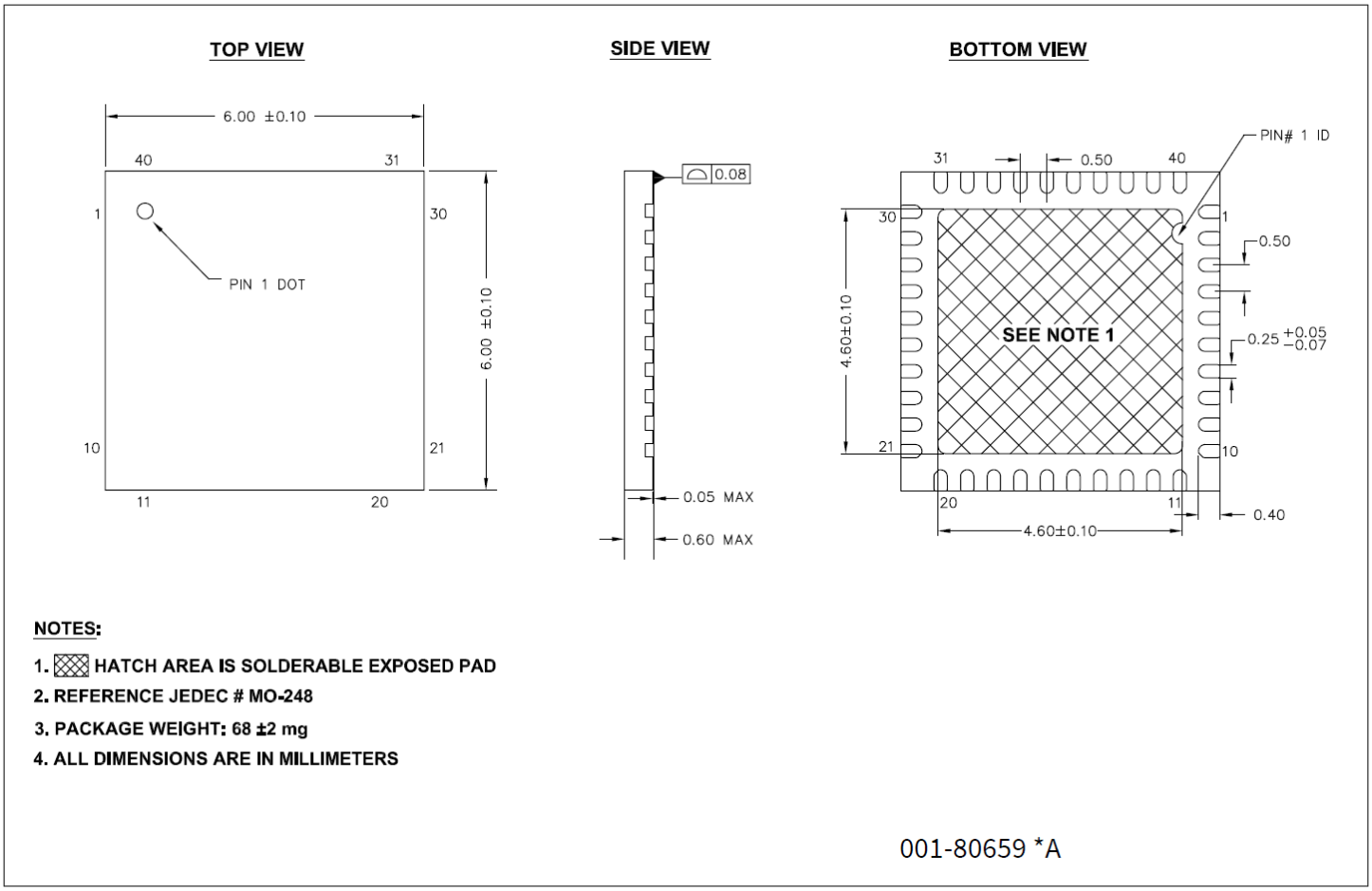
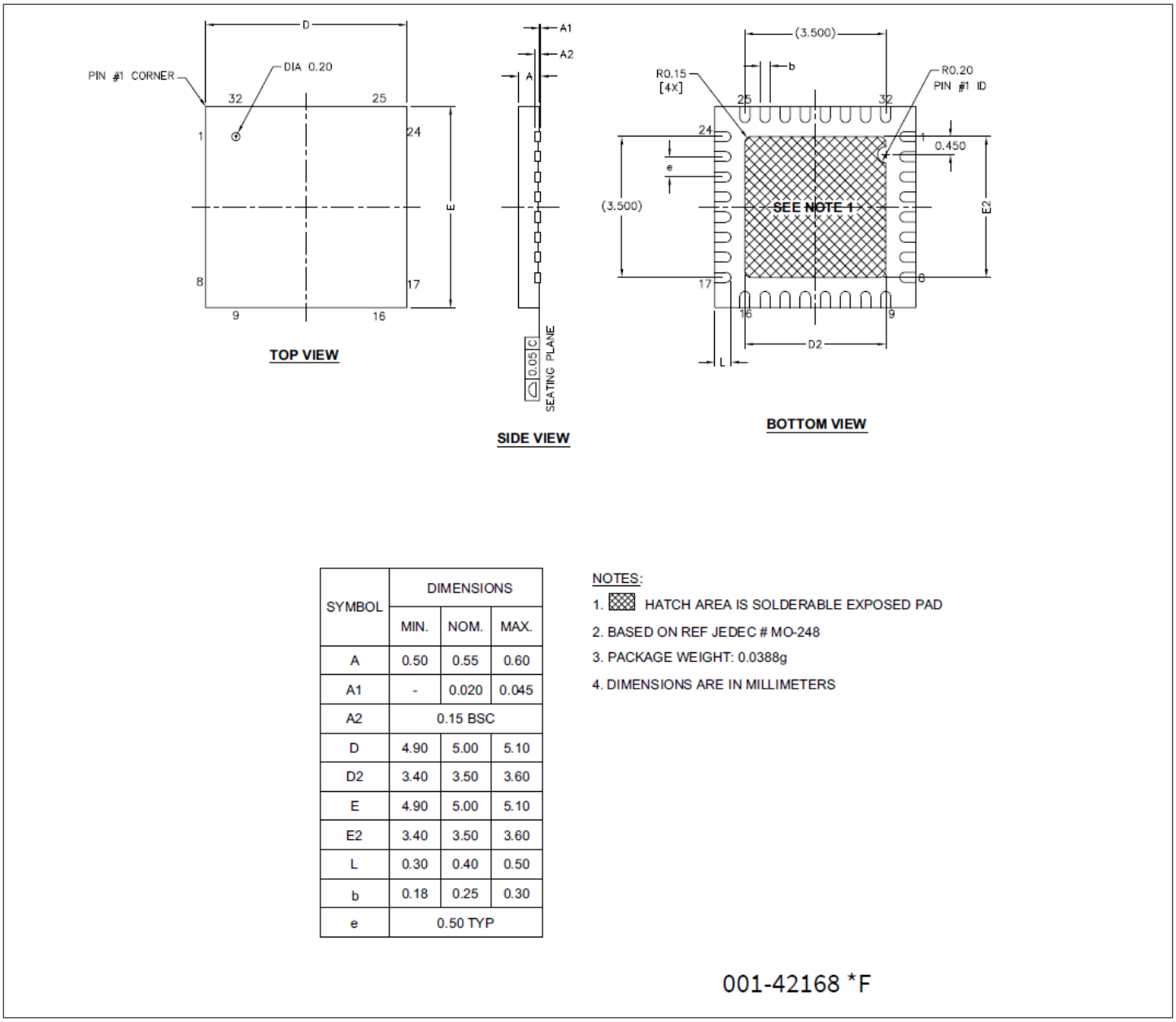


Figure 10 **40L QFN 6×6×0.6 MM LR40A/LQ40A 4.6×4.6 E-PAD (SAWN) package outline (PG-VQFN-40), 001-80659**

***Note**: The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.*



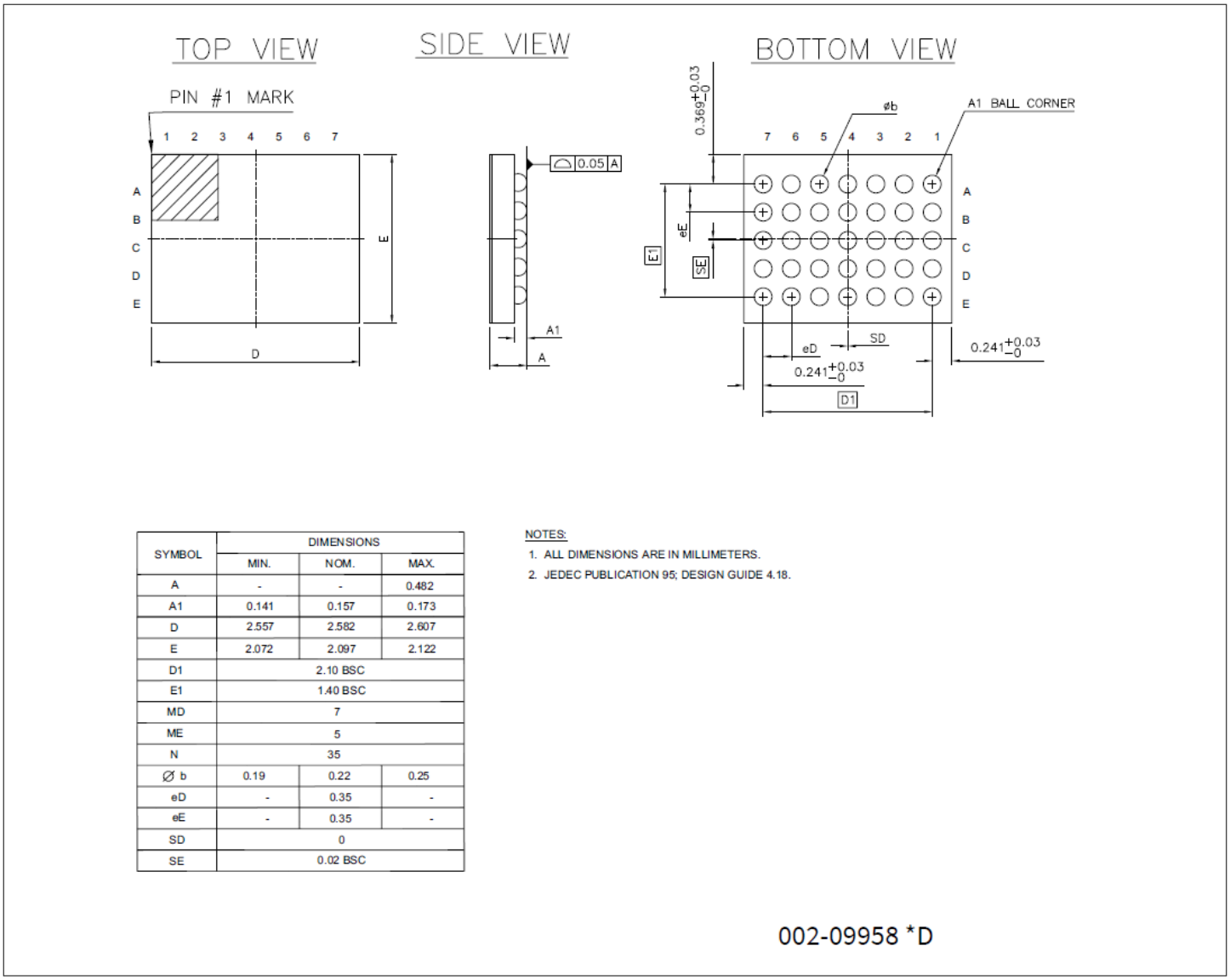
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	-	0.020	0.045
A2	0.15 BSC		
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.30	0.40	0.50
b	0.18	0.25	0.30
e	0.50 TYP		

NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *F

Figure 11 32 LEAD QFN 5.0×5.0×0.55 MM LQ32/LQ32B 3.5×3.5 MM EPAD (SAWN) package outline (PG-VQFN-32), 001-42168

***Note**: The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.*



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.482
A1	0.141	0.157	0.173
D	2.557	2.582	2.607
E	2.072	2.097	2.122
D1	2.10 BSC		
E1	1.40 BSC		
MD	7		
ME	5		
N	35		
Ø b	0.19	0.22	0.25
eD	-	0.35	-
eE	-	0.35	-
SD	0		
SE	0.02 BSC		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. JEDEC PUBLICATION 95; DESIGN GUIDE 4.18.

002-09958 *D

Figure 12 35 BALL WLCSP 2.582×2.097×0.482MM, FN35B package outline (SG-XFWLB-35), 002-09958

8 Acronyms

Table 45 Acronyms used in this document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame

(table continues...)

Table 45 (continued) Acronyms used in this document

Acronym	Description
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC™ pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt

(table continues...)

Table 45 (continued) Acronyms used in this document

Acronym	Description
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC™	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I2C serial clock
SDA	I2C serial data

(table continues...)

Table 45 (continued) Acronyms used in this document

Acronym	Description
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	universal serial bus
USBIO	USB input/output, PSoC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

9 Document conventions

9.1 Units of measure

Table 46 Units of measure

Symbol	Unit of measure
°C	degrees celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond

(table continues...)

Table 46 (continued) Units of measure

Symbol	Unit of measure
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Document revision	Date	Description of changes
**	2015-08-28	New datasheet.
*A	2015-10-30	Updated Pinouts: Updated Table 1. Updated Electrical specifications: Updated Analog peripherals: Updated Comparator: Updated Table 11. Updated Table 12. Updated 10-bit CAPSENSE™ ADC: Updated Table 16. Updated Ordering information: Updated part numbers. Completing Sunset Review
*B	2015-12-08	Changed status from Advance to Preliminary.
*C	2015-12-22	Updated Features: Updated description under “32-bit MCU Subsystem” and “Serial Communication”. Updated Pinouts: Updated Table 1. Updated Table 2. Updated Ordering information: No change in part numbers. Replaced “36 WLCSP (0.35 mm pitch)” with “35-WLCSP”. Updated Packaging: Replaced “36-ball WLCSP package” with “35-ball WLCSP package” in all instances. Completing Sunset Review.
*D	2016-02-16	Updated Packaging: Updated Table 42. Replaced TBD with 002-09958 *A. Added Errata. Updated to new template. Completing Sunset Review.

Document revision	Date	Description of changes
*E	2016-03-15	Updated Electrical specifications: Updated Device level specifications: Updated XRES: Updated Table 8. Updated Table 9. Updated Analog peripherals: Updated CSD and IDAC: Updated Table 15. Updated 10-bit CAPSENSE™ ADC: Updated Table 16. Updated Memory: Updated Flash: Updated Table 27. Completing Sunset Review.
*F	2016-07-27	Updated Electrical specifications: Updated Analog peripherals: Updated CSD and IDAC: Updated Table 15. Updated 10-bit CAPSENSE™ ADC: Updated Table 16. Removed Errata. Completing Sunset Review. Release to web.
*G	2016-10-13	Added 44LD TQFP package related information related information in all instances across the document. Updated Packaging: Added 51-85064 *G.
*H	2017-01-09	Updated Functional definition: Updated Analog blocks: Updated 12-bit SAR ADC: Updated Figure 5. Updated Programmable digital blocks: Updated description. Updated Pinouts: Updated description. Updated Electrical specifications: Updated Device level specifications: Updated Table 4. Updated Ordering information: Updated part numbers. Completing Sunset Review.

Document revision	Date	Description of changes
*I	2017-04-26	Updated Packaging: spec 002-09958 – Changed revision from *C to *D. Updated to new template.
*J	2018-02-14	Updated Features: Updated description under “Timing and Pulse-Width Modulation”. Added “Clock Sources”. Updated Development ecosystem: Updated description. Updated Block diagram. Updated Functional definition: Updated System resources: Updated Clock system: Updated Figure 4. Updated Pinouts: Updated Table 2. Updated Ordering information: Updated part numbers. Updated Packaging: spec 001-42168 – Changed revision from *E to *F. Updated to new template.
*K	2018-04-03	Updated Functional definition: Updated System resources: Updated Clock system: Updated Figure 4. Updated Watchdog timer and counters: Replaced “Watchdog Timer” with “Watchdog timer and counters” in heading. Updated description.

Document revision	Date	Description of changes
*L	2018-10-30	Updated Features: Updated description under “32-bit MCU Subsystem”. Updated Block diagram (Corrected typo). Updated Functional definition: Updated System resources: Updated Watch Crystal Oscillator (WCO): Updated description. Updated Electrical specifications: Updated Analog peripherals: Updated CTBm Opamp: Updated Table 10. Updated SAR: Updated Table 14. Updated CSD and IDAC: Updated Table 15. Updated Digital peripherals: Updated SPI: Updated Table 21. Completing Sunset Review.
*M	2019-07-05	Added extended industrial temperature range related information in all instances across the document. Updated Electrical specifications: Updated Memory: Updated Flash: Updated Table 27. Updated Ordering information: Updated part numbers.
*N	2020-11-10	Updated Features: Added “ModusToolbox™ software”. Updated Development ecosystem: Added ModusToolbox™ software. Updated PSoC™ Creator: Updated description. Updated Table 27: Updated SID182B. Updated Table 32: Added SID223A. Updated Ordering information: Updated part numbers. Completing Sunset Review.
*O	2022-07-28	Updated Table 32: Updated spec SID223 and SID223A. Added specs SID223B through SID223D. Updated Ordering information: Updated part numbers. Migrated to Infineon template.
*P	2023-01-23	Updated the footnotes in IMO AC specifications.

Document revision	Date	Description of changes
*Q	2024-02-27	Added note under 40L and 32-lead QFN package diagrams. Removed extra pin "DN" and pin name "VSSD" from 40L QFN column in Table 1. Content migrated to PRISMA. Fixed broken links. Updated the title to “PSoC™ 4100S based on Arm® Cortex®-M0+ CPU”. Updated packaging diagram titles with IFX package code for Figure 8, Figure 9, Figure 10, Figure 11, and Figure 12. Updated package information in Table 39, Table 41, and Table 42. Updated package information across the datasheet. Updated CY8C4146LQQ-S422T to CY8C4146LQQ-S422 in Ordering information.

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-02-27

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2024 Infineon Technologies AG

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-niy1693212753938

Important notice

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.