HMC610LP4 / 610LP4E

RMS POWER DETECTOR 75 dB, DC - 3.9 GHz

Typical Applications

The HMC610LP4(E) is ideal for:

- Log –> Root-Mean-Square (RMS) Conversion
- Received Signal Strength Indication (RSSI)
- Transmitter Signal Strength Indication (TSSI)
- RF Power Amplifier Efficiency Control
- Receiver Automatic Gain Control
- Transmitter Power Control

Features

±1 dB Detection Accuracy to 3.9 GHz

Input Dynamic Range: -60 dBm to +15 dBm

RF Signal Wave shape & Crest Factor Independent

Operates with Single-Ended or Differential Input

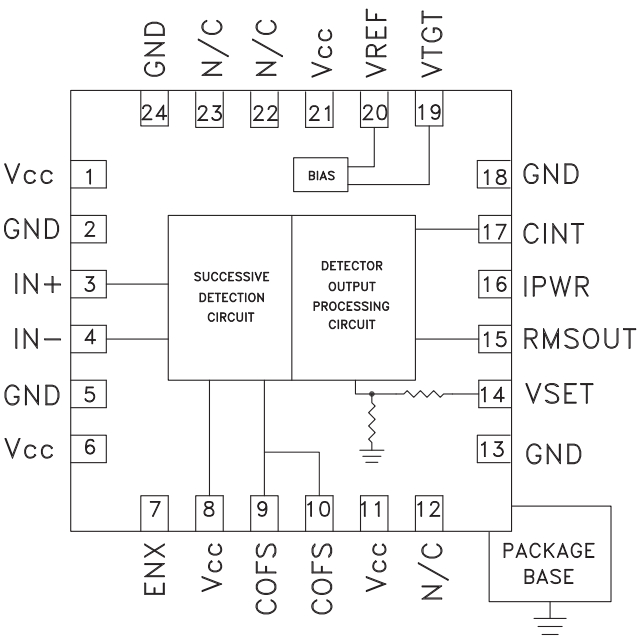
+5V Operation from -40°C to +85°C

Excellent Temperature Stability

Power-Down Mode

24 Lead 4x4mm SMT Package: 16mm²

Functional Diagram



General Description

The HMC610LP4E Power Detector is designed for RF power measurement, and control applications for frequencies up to 3.9 GHz. The detector provides a "true RMS" representation of any RF/IF input signal. The output is a temperature compensated monotonic, representation of real signal power, measured with a differential input sensing range of 75 dB, or 72 dB of single-ended sensing range.

The HMC610LP4E is ideally suited to those wide bandwidth, wide dynamic range applications, requiring repeatable measurement of real signal power, especially where RF/IF wave shape and/or crest factor change with time.

Electrical Specifications, T_A = +25C, Vcc= 5V

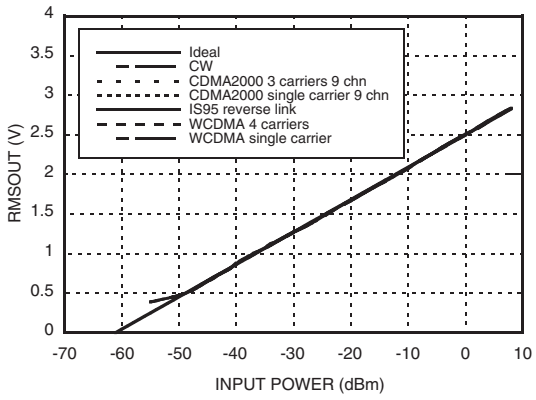
Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Dynamic Range (± 1 dB measurement error)								
Input Frequency	< 900	1900	2200	2700	3000	3500	3900	MHz
Differential Input Configuration [1]	> 75	70	67	66	67	56	48	dB
Input Signal Frequency	< 900	1300 ± 300		2300 ± 300		3300 ± 300		MHz
Single-Ended Input Configuration	66 [2]	72 [3]		69 [3]		65 [3]		dB
Deviation vs. Temperature: Deviation is measure from reference, which is the same CW input at 25 °C								
[1] Differential Input Interface with 1:1 Balun Transformer (over full input frequency range)					± 0.6			dB
[2] Wideband Single-Ended Input Interface suitable for input signal frequencies below 1000 MHz					± 0.3			dB
[3] Tuned Single-Ended Input Interface suitable for input signal frequencies above 1000 MHz					± 0.5			dB

Table 2: Electrical Specifications [II],

HMC610LP4E Evaluation Kit (Diff. Input Config.), TA = +25C, Vcc= +5V, C_{INT} = 0.1 µF, Unless Otherwise Noted.

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Signal Frequency	900	1900	2200	2700	3000	3500	3900	MHz
Modulation Deviation (Deviation measured from reference, which is measured with CW input at equivalent input signal power)								
CDMA2000 3 Carriers, 9 Channels	0.1	0.08	0.1	0.14	0.2	0.25	0.3	dB
CDMA2000 1 Carrier, 9 Channels	0.15	0.12	0.15	0.18	0.25	0.3	0.35	dB
IS95 Reverse Link	0.05	0.05	0.1	0.1	0.1	0.15	0.2	dB
WCDMA 1 Carrier	0.1	0.14	0.12	0.18	0.2	0.3	0.3	dB
WCDMA 4 Carrier	0.2	0.22	0.24	0.24	0.3	0.4	0.4	dB
Differential Input Configuration Logarithmic Slope and Intercept								
Logarithmic Slope	36.5	37.3	37.8	39.3	40.5	43.5	47.5	mV/dB
Logarithmic Intercept	-72	-70	-69	-65	-62	-57	-53	dBm
Max. Input Power ar ± 1 dB Error	>+15	+10	+7	+10	+12	+8	+4	dBm
Min. Input Power at ± 1 dB Error	-60	-60	-60	-56	-52	-48	-44	dBm
Single-Ended Input Configuration Logarithmic Slope & Intercept								
Input Signal Frequency	< 900 [2]	1300 ± 300 [3]		2300 ± 300 [3]		3300 ± 300 [3]		MHz
Logarithmic Slope	37.3	36.4		37.9		41.9		mV/dB
Logarithmic Intercept	-70	-69		-67		-60		dBm
Max. Input Power at ±1.25 dB Error	7	15		13		15		dBm
Min. Input Power at ±1.25 dB Error	-59	-57		-56		-50		dBm
[2] Wideband Single-Ended Input Interface suitable for input signal frequencies below 1000 MHz								
[3] Tuned Single-Ended Input Interface suitable for input signal frequencies above 1000 MHz								

RMSOUT vs. Pin with Different Modulations @ 3000 MHz



RMSOUT Error vs. Pin with Different Modulations @ 3000 MHz

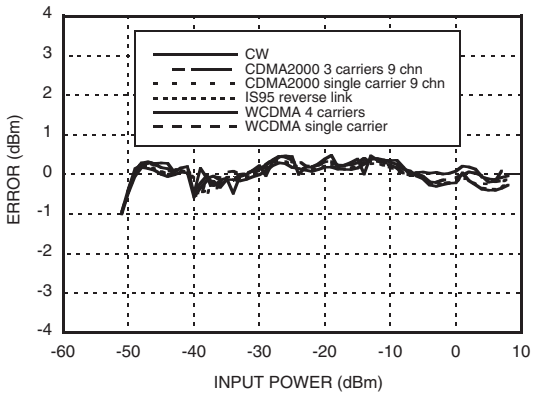


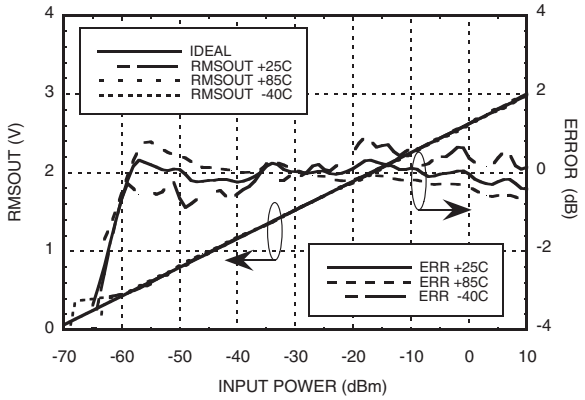
Table 3: Electrical Specifications [III],

HMC610LP4E Evaluation Kit (Diff. Input Config.), TA = +25C, Vcc= +5V, C_{INT} = 0.1 µF, Unless Otherwise Noted.

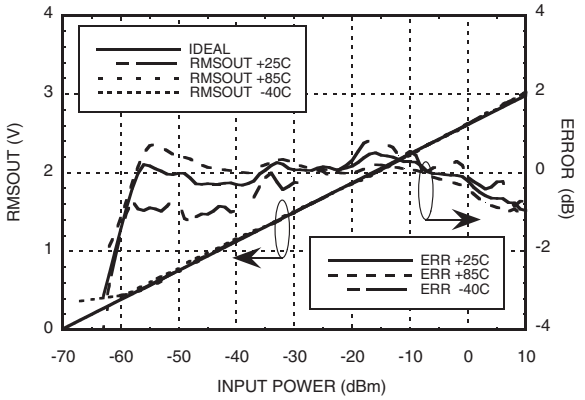
Parameter	Conditions	Min.	Typ.	Max.	Units
Differential Input Configuration					
Input Network Return Loss [1]	[1]		>10		dB
Input Resistance between IN+ and IN-	Between pins 3 and 4		200		Ω
Input Voltage Range	$V_{DIFFIN} = V_{IN+} - V_{IN-}$			2.25	V
Single-Ended Input Configuration					
Input Network Return Loss [2]	[2], [3]		>10		dB
Input Voltage Range	$V_{SEin} = V_{IN+}$			1.4	V
RMSOUT Output					
Output Voltage Range	RL - 1kΩ, CL = 4.7pF			3.2	V
Source/Sink Current Compliance	RMSOUT held at VCC/2		8 / -0.4		mA
Max. Load Capacitance	With C_{INT} = 0		35		pF
Output Slew Rate (rise / fall)	With C_{INT} = 0, Cofs = 0		15 (200)		10^6 V/s
V_{SET} Input (Negative Feedback Terminal)					
Input Voltage Range				3.2	V
Input Resistance			54		kΩ
V_{REF} Output (Reference Voltage)					
V_{REF} Output Voltage			2.0		V
V_{REF} Error	Over Full Temperature Range		± 50		mV
V_{TGT} Input (RMS Target Interface)					
Input Voltage Range				3.65	V
Input Resistance			>1		MΩ
ENX Logic Input (Power Down Control)					
Input High Voltage	Standby Mode Active	3.9			V
Input Low Voltage	Normal Operation			1.2	V
Input High Current				1	µA
Input Low Current				1	µA
Input Capacitance			0.5		pF
Power Supply					
Supply Voltage		4.5	5	5.5	V
Supply Current with Pin = -70 dBm	Over Full Temperature Range		65	96	mA
Supply Current with Pin = 0 dBm	Over Full Temperature Range		79	118	mA
Standby Mode Supply Current	ENX = Hi		0.5		mA

[1] Performance of differential input configuration is limited by balun. Balun used is MACOM ETC1-1-13 good over 4.5 MHz to 3000 MHz
[2] Using Wideband Single-Ended Input Interface suitable for input signal frequencies below 1000 MHz
[3] Using Tuned Single-Ended Input Interface suitable for input signal frequencies above 1000 MHz

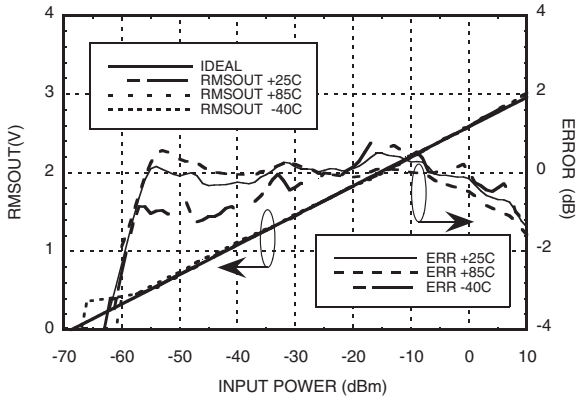
RMSOUT & Error vs. Pin @ 900 MHz [1]



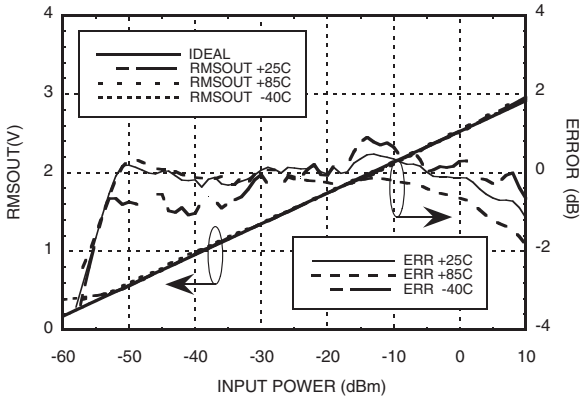
RMSOUT & Error vs. Pin @ 1900 MHz [1]



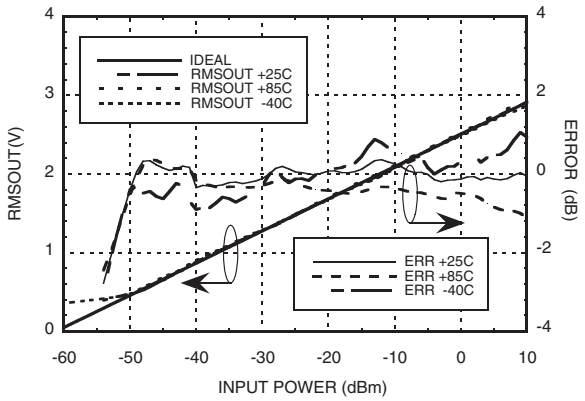
RMSOUT & Error vs. Pin @ 2200 MHz [1]



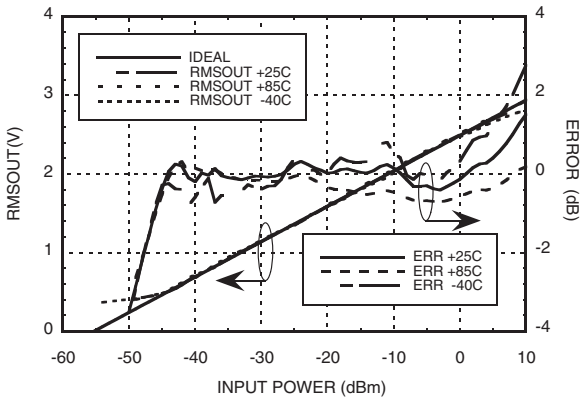
RMSOUT & Error vs. Pin @ 2700 MHz [1]



RMSOUT & Error vs. Pin @ 3000 MHz [1]

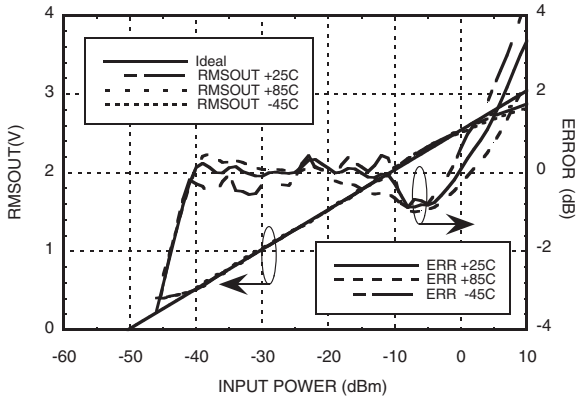


RMSOUT & Error vs. Pin @ 3500 MHz [1]

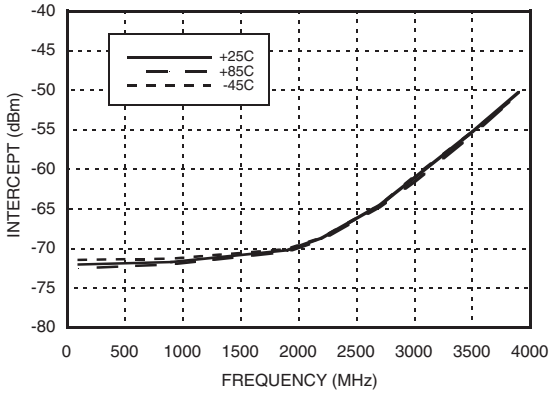


[1] CW input waveform, into differential input interface with 1:1 Balun

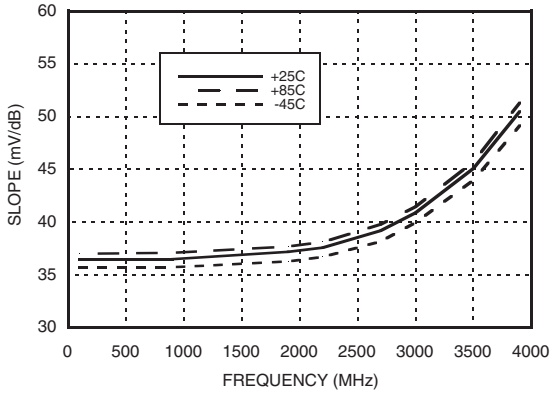
RMSOUT & Error vs. Pin @ 3900 MHz [1]



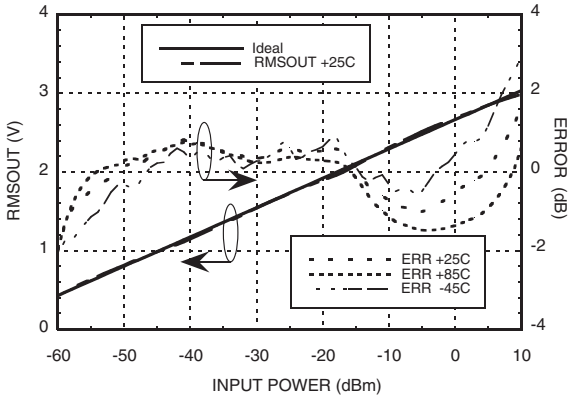
Differential Intercept vs. Frequency [1]



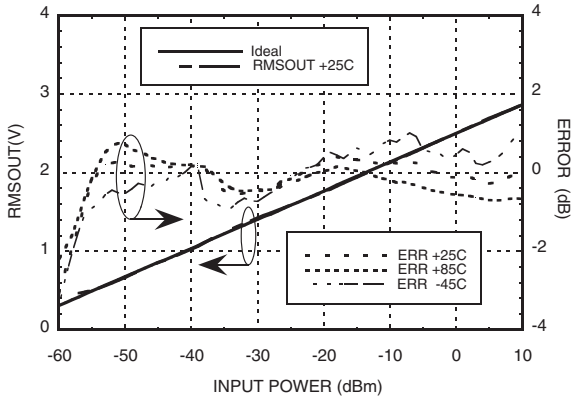
Differential Slope vs. Frequency [1]



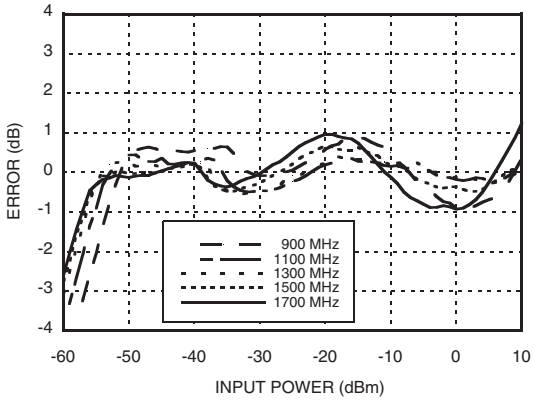
RMSOUT & Error vs. Pin @ 900 MHz Using Wideband SE-Interface [1]



RMSOUT & Error vs. Pin @ 1300 MHz Using Tuned SE-Interface f_{TUNE} = 1300 MHz [1]

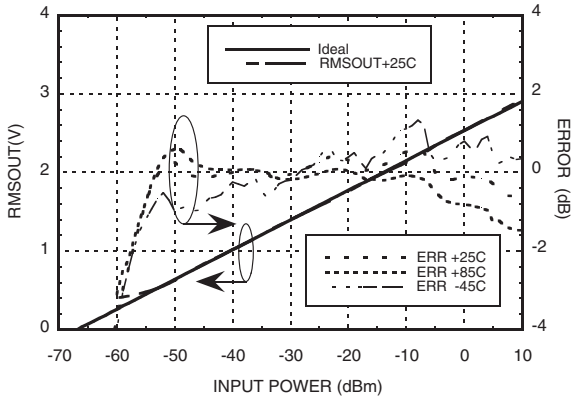


Error vs. Pin Using Tuned SE-Interface: 1300 ± 300 MHz [1]

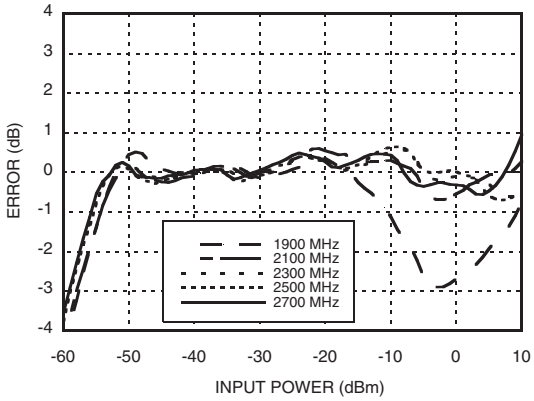


[1] CW input waveform.

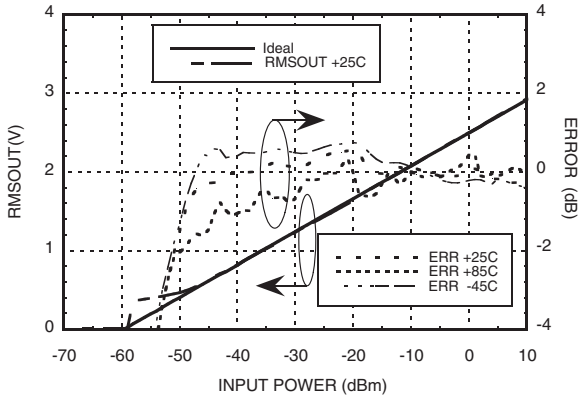
RMSOUT & Error vs. Pin @ 2300 MHz Using Tuned SE-Interface, f_{TUNE} = 2300 MHz [1]



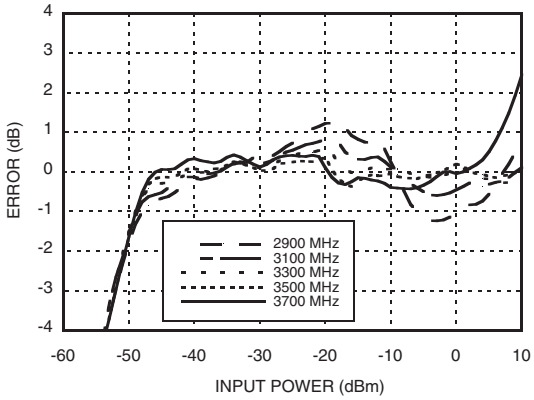
Error vs. Pin Using Tuned SE-Interface: 2300 ± 300 MHz [1]



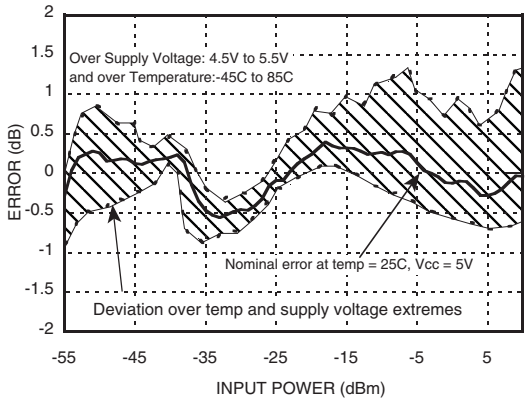
RMSOUT & Error vs. Pin @ 3300 MHz Using Tuned SE-Interface, f_{TUNE} = 3300 MHz [1]



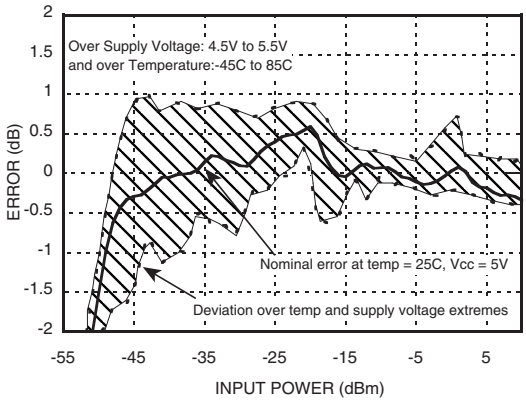
Error vs. Pin Using Tuned SE-Interface: 3300 ± 300 MHz [1]



Error over Supply Voltage & Temperature Using Tuned SE-Interface Centered on 1300 MHz [1]

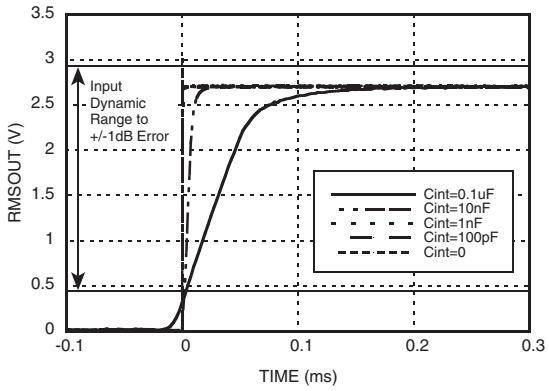


Error over Supply Voltage & Temperature Using Tuned SE-Interface Centered on 3300 MHz [1]

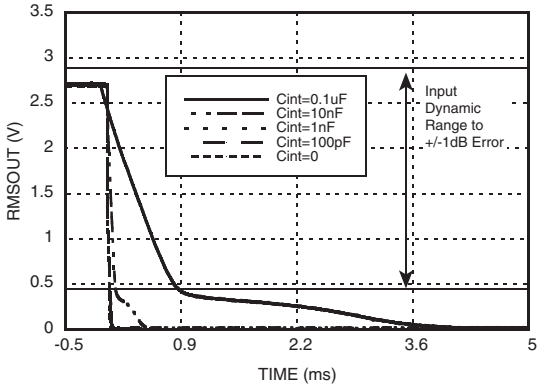


[1] CW input waveform.

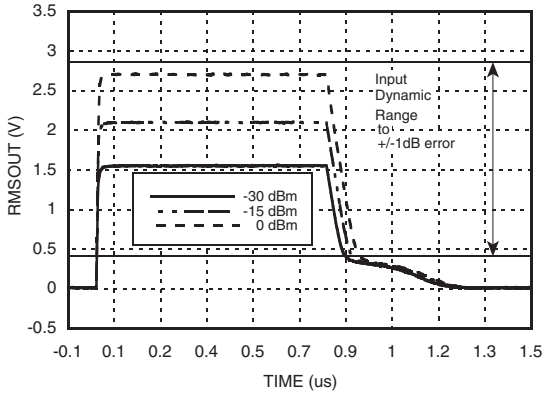
Output Rise-Time to RF Burst [6]



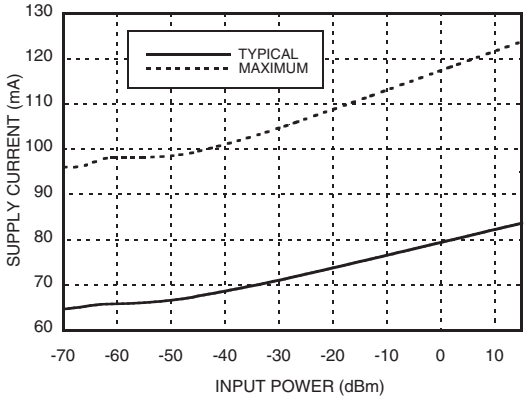
Output Fall-Time to RF Burst [6]



Output Response to RF Burst [7]

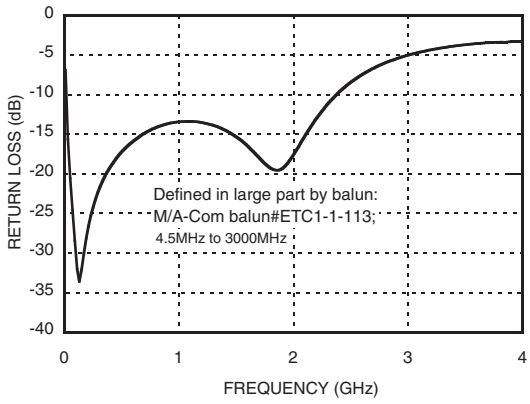


Typical Supply Current vs. Input Power, Vcc = 5V



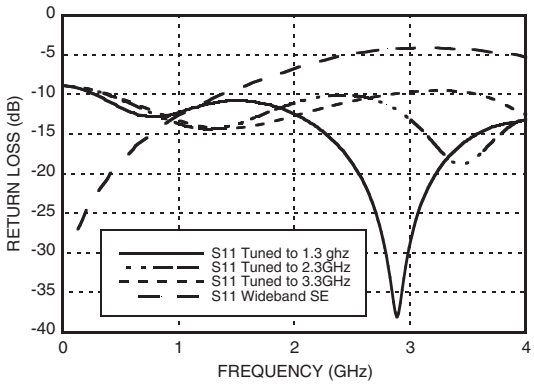
Differential Input Return Loss

Using Evaluation PCB w/ Differential Input Interface



Single-Ended Input Return Loss

Using Evaluation PCB w/Single-Ended Input Interface



[6] Input @ 900 MHz, 0 dBm; Vdd = 5V, C_{OFS} = 1nF

[7] Input @ 900 MHz, C_{INT} = 10nF, C_{OFS} = 1nF, Vcc = 5V

HMC610LP4 / 610LP4E

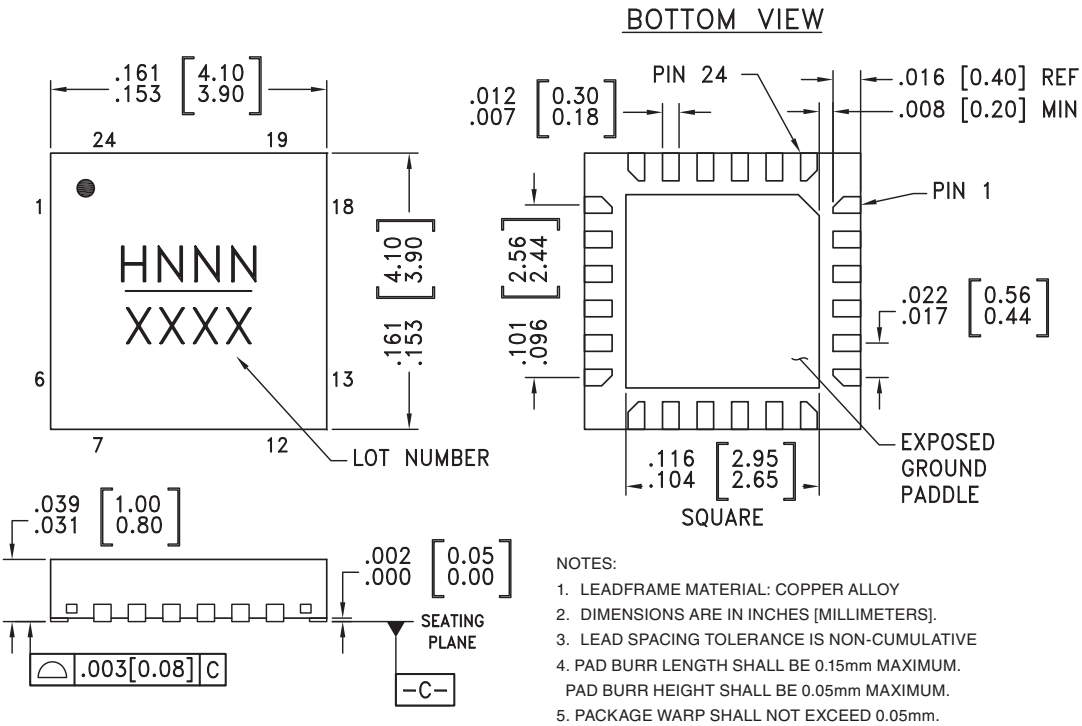
RMS POWER DETECTOR 75 dB, DC - 3.9 GHz

Absolute Maximum Ratings

Supply Voltage	5.6V
RF Input Power	20 dBm
Max. Input Voltage	2.25 Vrms
Channel / Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 22.72 mW/°C above 85°C)	0.91 Watts
Thermal Resistance (R_{th}) (junction to ground paddle)	44.02 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



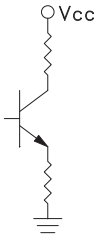
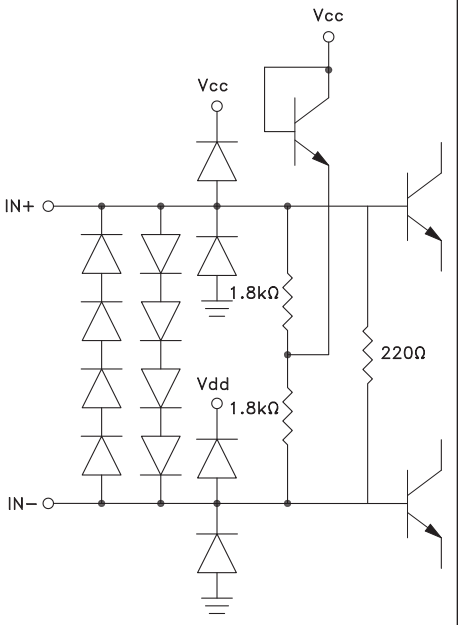
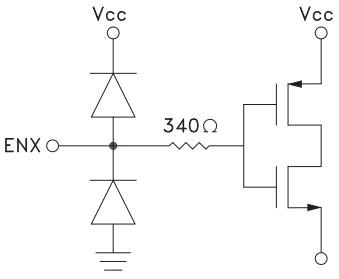
NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC610LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H610 XXXX
HMC610LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H610 XXXX

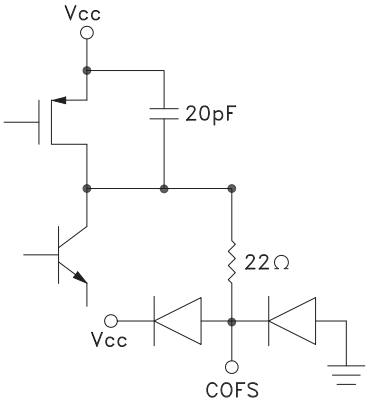
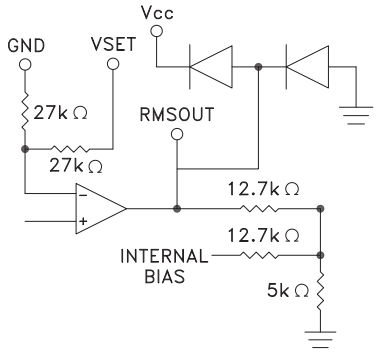
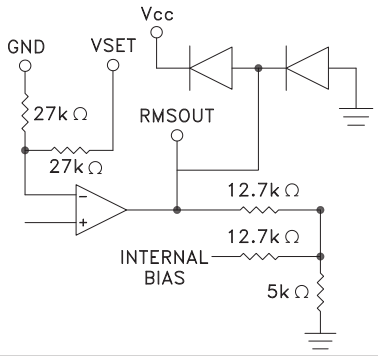
[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

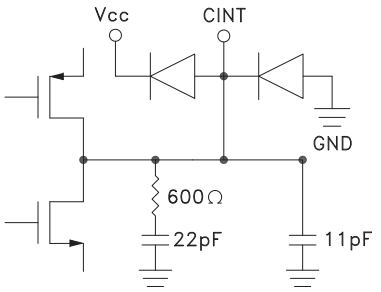
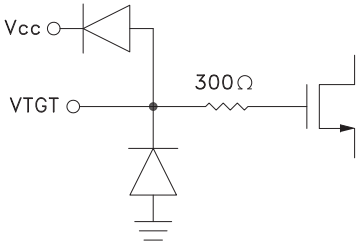
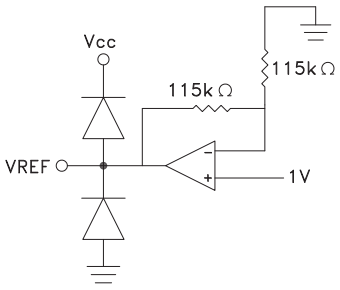
Pin Number	Function	Description	Interface Schematic
1, 6, 8, 11, 21	Vcc	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	
2, 5, 13, 16, 18, 24	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	
3, 4	IN+, IN-	RF Input pins. See application information for input interfacing.	
7	ENX	Disable pin. Connect to GND for normal operation. Applying voltage V>0.8 Vdd will initiate power saving mode.	

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

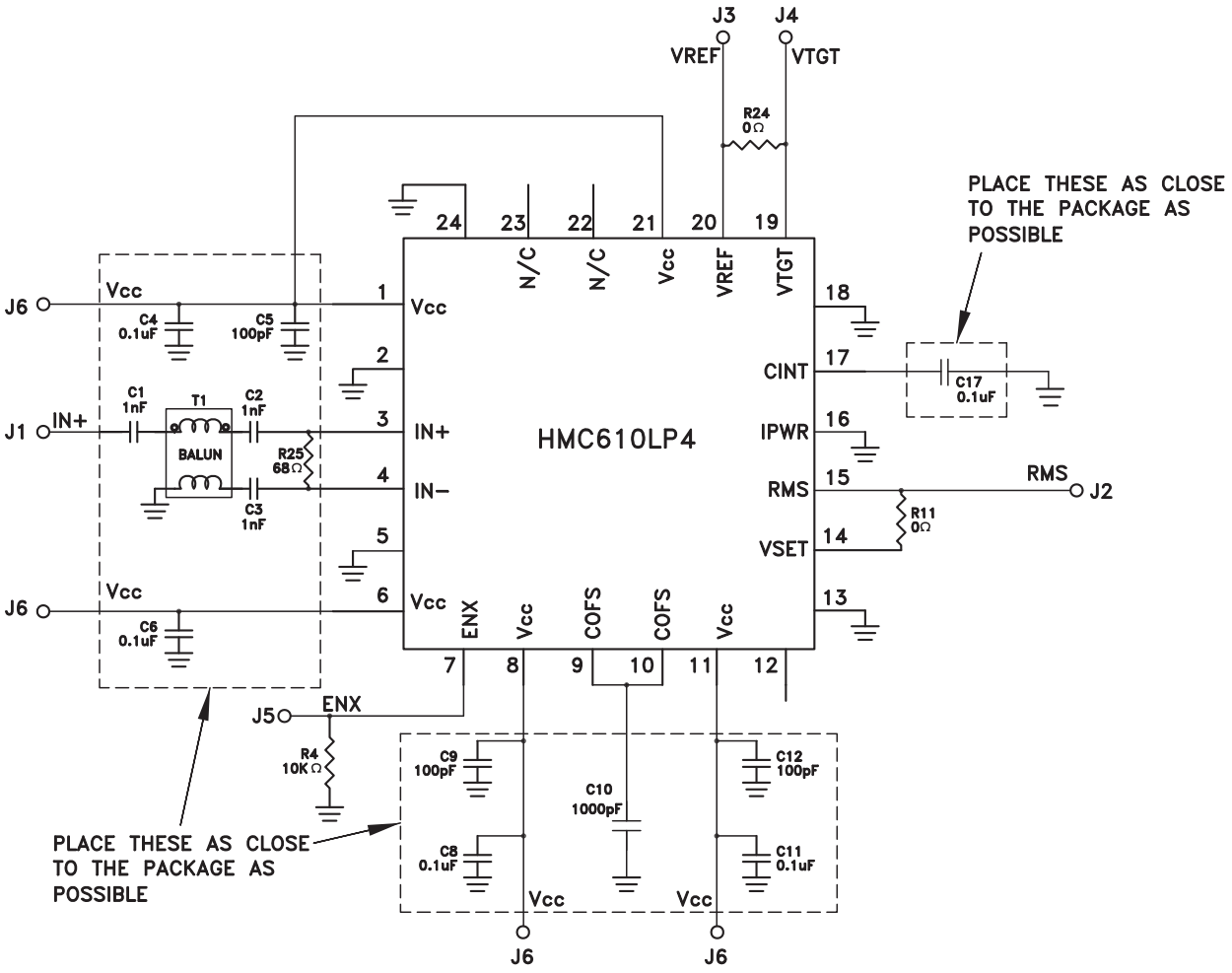
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
9, 10	COFS	Input high pass filter capacitor. Connect to common via a capacitor to determine 3 dB point of input signal high-pass filter.	
14	VSET	VSET input. Short this pin to RMSOUT for normal operation.	
12, 22, 23	N / C	These pins are not connected internally.	
15	RMSOUT	Logarithmic output that converts the input power to a DC level. Short this pin to VSET for normal operation.	
16	IPWR	Ground for proper operation	

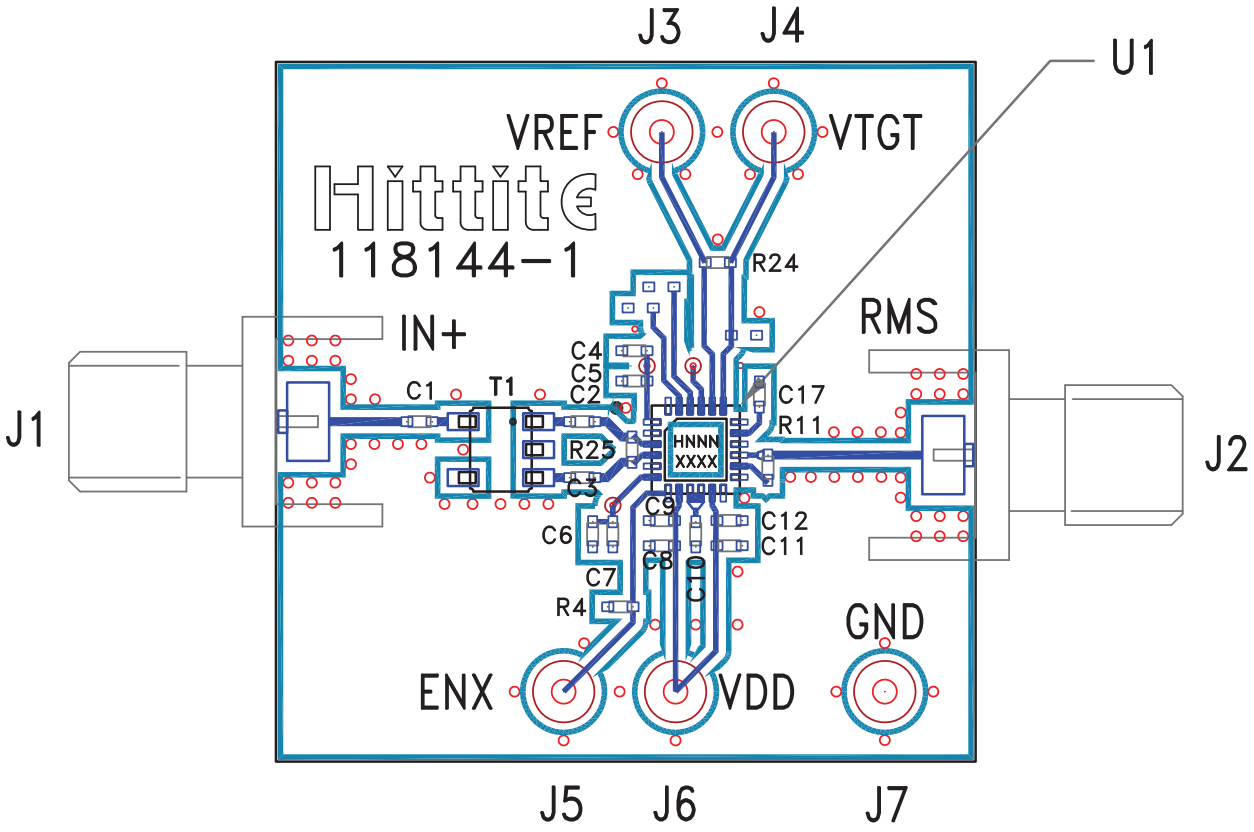
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
17	CINT	Connection for ground referenced loop filter integration capacitor. See application schematic.	
19	VTGT	Use of lower target voltage reduces error for complex signals with large crest factors. Normally connected to VREF.	
20	VREF	Reference voltage output.	

Application Circuit - Differential Configuration



Evaluation PCB - Differential Input Configuration



List of Materials for Evaluation PCB 118147 [1]

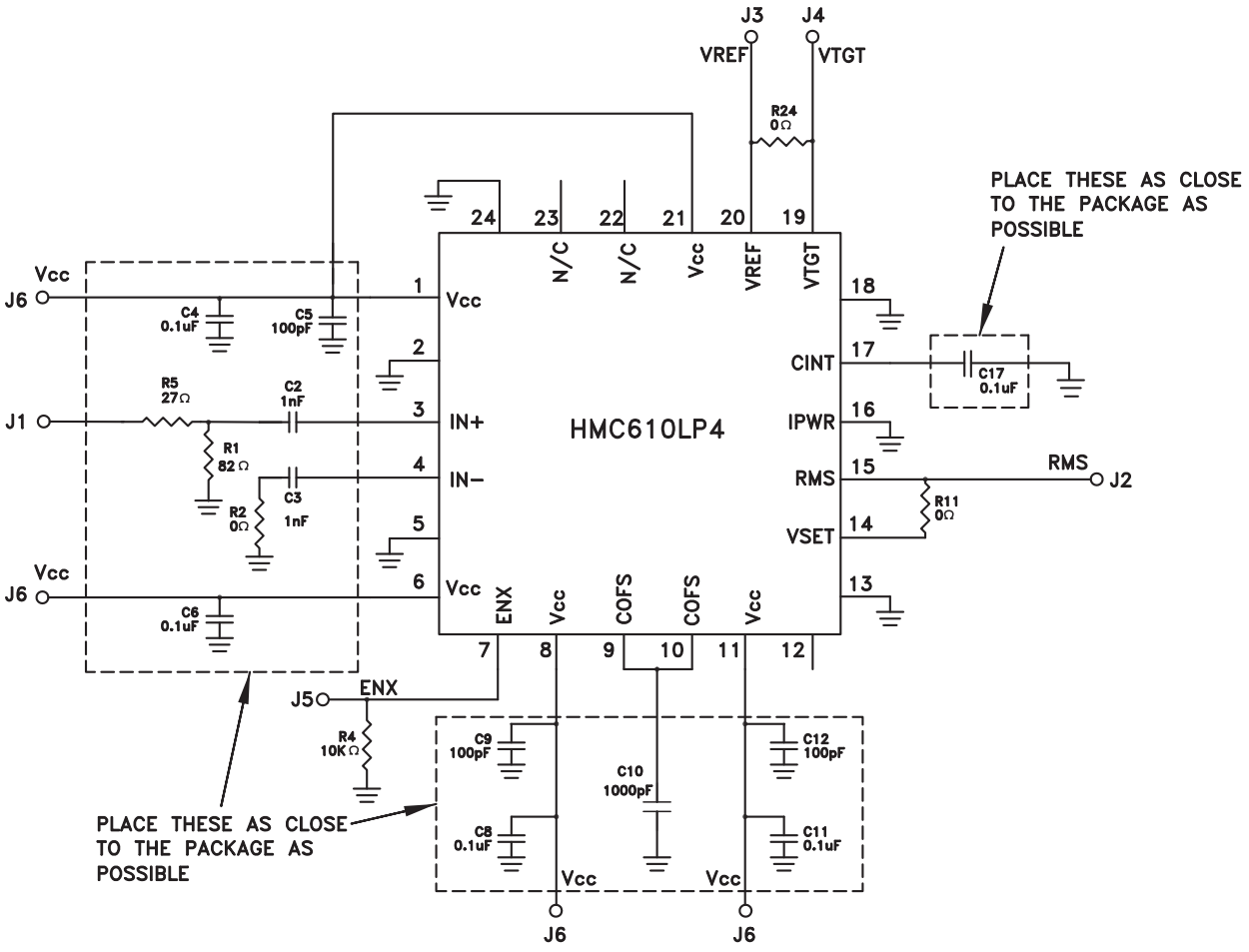
Item	Description
J1 - J2	PC Mount SMA connector
J3 - J7	DC Pins
C1 - C3	1 nF Capacitor, 0402 Pkg.
C4, C6, C8, C11, C17	0.1 µF Capacitor, 0402 Pkg.
C5, C9, C12	100 PF Capacitor, 0402 Pkg.
C10	1000 PF Capacitor, 0402 Pkg.
R25	68 Ω Resistor, 0402 Pkg.
R11, R24	0 Ω Resistor, 0402 Pkg.
R4	10k Ω Resistor, 0402 Pkg.
T1	1:1 Balun, M/A-COM ETC1-1-13
U1	HMC610LP4 / HMC610LP4E Logarithmic Detector / Controller
PCB [2]	118144 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

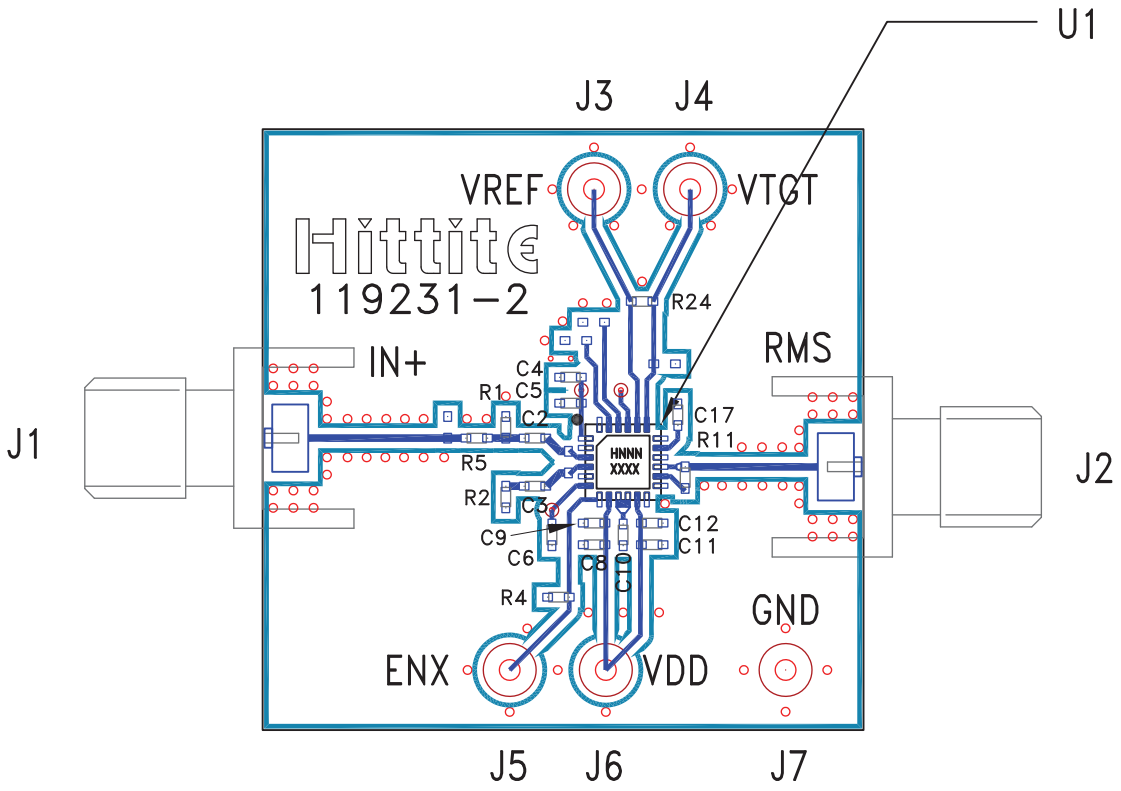
[2] Circuit Board Material: Arlon 25R

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit - Single Ended Configuration



Evaluation PCB - Single-Ended



List of Materials for Evaluation PCB 119233 [1]

Item	Description
J1 - J2	PC Mount SMA connector
J3 - J7	DC Pins
C2 - C3	1 nF Capacitor, 0402 Pkg.
C4, C6, C8, C11, C17	0.1 µF Capacitor, 0402 Pkg.
C5, C9, C12	100 PF Capacitor, 0402 Pkg.
C10	1000 PF Capacitor, 0402 Pkg.
R1	82 Ω Resistor, 0402 Pkg.
R5	27 Ω Resistor, 0402 Pkg.
R2, R11, R24	0 Ω Resistor, 0402 Pkg.
R4	10k Ω Resistor, 0402 Pkg.
U1	HMC610LP4 / HMC610LP4E Logarithmic Detector / Controller
PCB [2]	119231 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

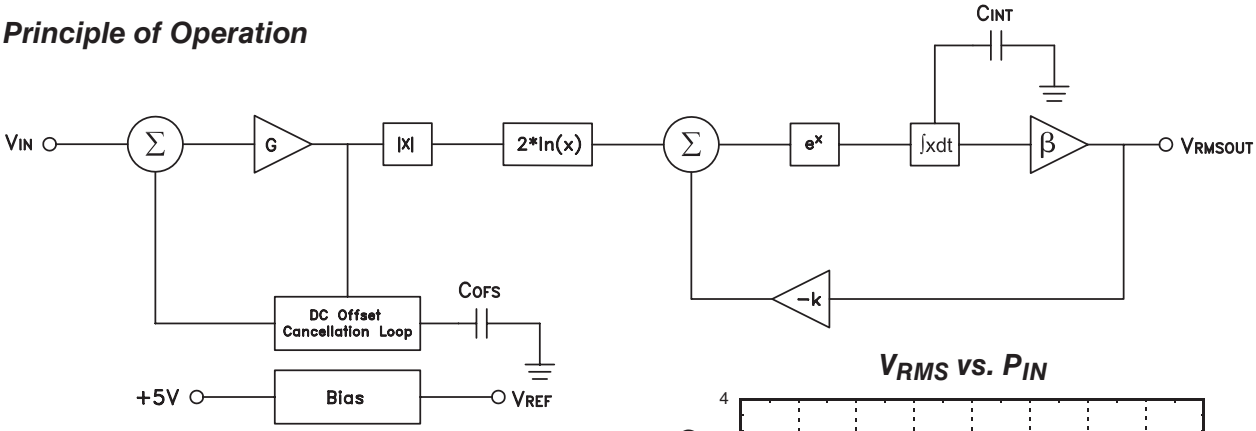
[2] Circuit Board Material: Arlon 25R

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Board is configured with wideband single-ended interface suitable for input signal frequencies below 1000 MHz. Refer to section on tuning single-ended interface in application information for operating with signals above 1000 MHz.

Application Information

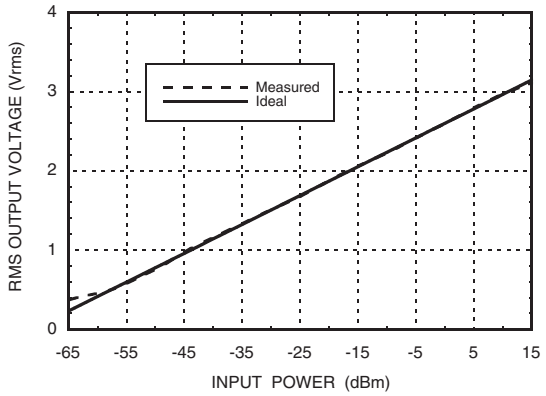
Principle of Operation



$$V_{RMSOUT} = \frac{1}{k}\ln\left(\beta k G^2 \int {V_{IN}}^2 dt\right)$$

P_{IN} = V_{RMS} / [log-slope] + [log-intercept], dBm

V_{RMS} vs. P_{IN}



Monolithic true-RMS detectors are in-effect analog calculators, calculating the RMS value of the input signal, unlike other types of power detectors which are designed to respond to the RF signal envelope. At the core of an RMS detector is a full-wave rectifier, log/antilog circuit, and an integrator. The RMS output signal is directly proportional to the logarithm of the time-average of V_{IN}^2. The bias block also contains temperature compensation circuits which stabilize output accuracy over the entire operating temperature range. The DC offset cancellation circuit actively cancels internal offsets so that even very small input signals can be measured accurately.

Configuration For The Typical Application

The RF input can be connected in either a differential or single-ended configuration: see “RF Input Interface” section for details on each input configuration.

Typically the RMS output signal is connected directly to V_{SET}, providing a Pin→V_{RMS} transfer characteristic slope of 36.5mV/dBm. The log-slope is not adjustable internally, however an external method for adjusting log-slope, and log-intercept is described in the “log-slope and intercept” section.

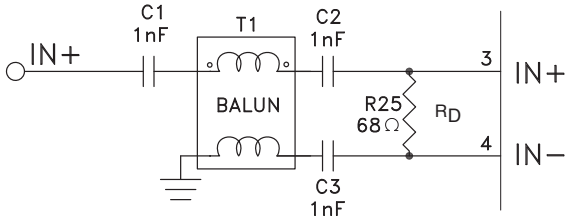
V_{TGT} is also typically connected directly to V_{REF}, however the V_{TGT} voltage can be adjusted to optimize output accuracy: see “Adjusting V_{TGT} for greater precision” section for details.

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements: refer to the “System Calibration” section for more details.

RF Input Interface

The IN+ and IN- pins are differential RF inputs, which can be externally configured as differential or single-ended input. Power match components are placed at these input terminals, along with DC blocking capacitors. The coupling capacitor values also set the lower spectral boundary of the input signal bandwidth. The inputs can be reactively matched (refer to input return loss graphs), but a resistor network should be sufficient for good wideband performance.

Selecting resistor values for Differential Interface:



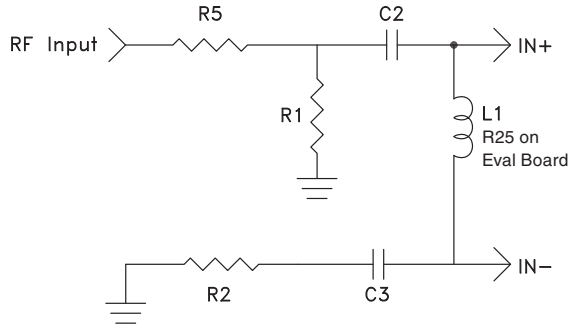
The value of R_{25} depends on the balun used; if the balun is 50Ω on both sides of the SE-Diff conversion,

then $R_{25} = \frac{220 * R_M}{220 - R_M}$, Ω , where

R_M = the desired power match impedance in ohms

For R_M = 50 Ω, R_{25} = 64.7 Ω ≈ 68 Ω

Single-Ended Input Interface



Tuned SE-interface: for signal frequencies > 900MHz

Choose L and C elements from the following graph for narrowband tuning of the SE-interface: R5 = 27Ω, R1 = 82Ω, C2 = 100 pF, R2 = 0Ω, L1, C3 - see graph.

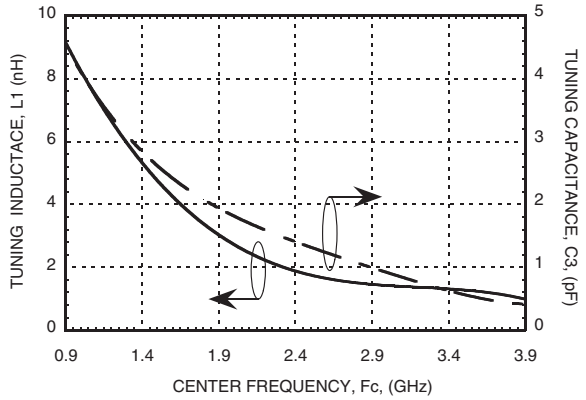
Wideband SE-interface: for signal frequencies < 900MHz

R5 = 27Ω, R1 = 82Ω,

C2, C3 are 1nF decoupling caps.

R2 is 0Ω, and R25 is open

Tuning SE Input Interface: f_C ±300 MHz



For wideband (un-tuned) input interfaces, choose the input decoupling capacitor values by first determining the lowest spectral component the power detector is required to sense, ƒL.

Input decoupling capacitor value $\approx \frac{1}{\pi \times f_L \times 3.2}$, Farads, where ƒL is in Hertz.

Ex. If the power detector needs to sense down to 10MHz, the decoupling capacitor value should be 1/(π*10E6*3.2) = 10nF

A DC bias (Vcc-0.7V) is present on the IN+ and IN- pins, and should not be overridden.

RMS Output Interface and Transient Response

Output transient response is determined by the integration capacitance (C_{INT}), and output load conditions. Using larger values of C_{INT} will narrow the operating bandwidth of the integrator, resulting in a longer averaging time-interval and a more filtered output signal; however it will also slow the power detector's transient response. A larger C_{INT} value favors output accuracy over speed. For the fastest possible transient settling times, leave the C_{INT} pin free of any external capacitance. This configuration will operate the integrator at its widest possible bandwidth, resulting in short averaging time-interval and an output signal with little filtering. Most applications will choose to have some external integration capacitance, maintaining a balance between speed and accuracy. Furthermore, error performance over crest factor is degraded when C_{INT} is very small (for C_{INT}<100pF).

Modulation and deviation results in Electrical Specification Table 2 are given for C_{INT} = 0.1 μF.

Start by selecting C_{INT} using the following expression, and then adjust the value as needed, based on the application's preference for faster transient settling or output accuracy.

C_{INT} = 1500 μF / (2*π*f_{LAM}), in Farads, where f_{LAM}= lowest amplitude-modulation component frequency in Hertz.

Example: when f_{LAM}= 10 kHz, C_{INT} = 1500μF/(2*π*10kHz) = 24nF ~ 22nF

Input signal is 1900MHz CW-tone switched on and off

Table: Transient Response vs. C_{INT} & C_{OFS} Capacitance:

C_{INT}	C_{OFS}	RMSOUT Rise-Time Over Dynamic Range	Pin = -26 dBm	RMSOUT Fall-Time Pin = -11 dBm	Pin = 4 dBm
0	0 pF	15 ns	0.2 µs	0.3 µs	1.4 µs
82 pF	0 pF	65 ns	0.5 µs	0.7 µs	1.4 µs
820 pF	0 pF	0.83 µs	5 µs	8 µs	10 µs
10 nF	0 pF	3.2 µs	20 µs	30 µs	36 µs
100 nF	0 pF	69 µs	400 µs	580 µs	775 µs
0	1 nF	15 ns	1.0 µs	17 µs	28 µs
82 pF	1 nF	65 ns	1.2 µs	17 µs	28 µs
820 pF	1 nF	0.83 µs	6 µs	17 µs	28 µs
10 nF	1 nF	3.2 µs	60 µs	80 µs	105 µs
100 nF	1 nF	69 µs	500 µs	700 µs	900 µs

RMS is loaded with 1kΩ, 4pF, and V_{TGT} = V_{REF},

D.R. is input dynamic range to ±1 dB error

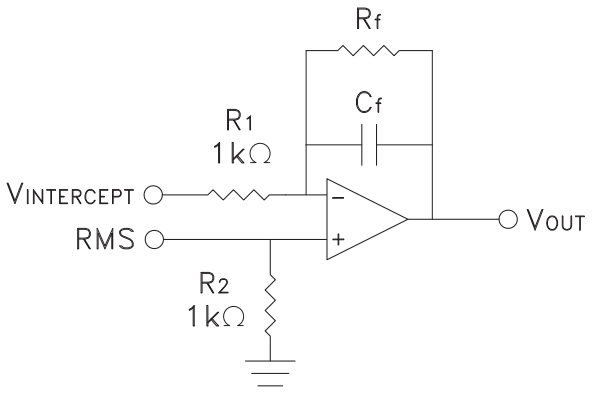
Transient response can also be slewed by the RMS output if it is excessively loaded: keep load resistance above 375Ω. An optimal load resistance of approximately 500Ω to 1kΩ will allow the output to move as quickly as it is able. For increased load drive capability, consider a buffer amplifier on the RMS output.

Using an integrating amplifier on the RMS output allows for an alternative treatment for faster settling times. An external amplifier optimized for transient settling can also provide additional RMS filtering, when operating HMC610LP4 with a lower C_{INT} capacitance value.

Log-Slope and Intercept

The HMC610LP4 is set with a Pin –> RMS transfer characteristic slope set to 36.5mV/dBm by design (otherwise referred to as the log-slope). Connect the RMS pin directly to VSET pin. The Pin –> RMS transfer characteristic is not adjustable internally, but both slope and intercept can be adjusted quite easily by using an external integrating amplifier such as the one shown below. Avoid loading the RMS output with a capacitive load above 35pF, when CINT<100pF.

Figure: External Integrating Amplifier with log-slope and log-intercept control.



$V_{INTERCEPT}$ is a DC voltage used to adjust the log-intercept point.

$$G(s) = \frac{R_f}{R_1(1 + sR_fC_f)}$$, adjusts log-slope

$V_{OUT}(s)$= RMSOUT X (1 + G(s)) - $V_{INTERCEPT}$ X G(s), V

$$f_c = \frac{1}{2\pi R_f C_f}$$, Hz = cut-off frequency

Rf is in Ohms
Cf is in Farads

DC Offset Compensation Loop

Internal DC offsets, which are input signal dependant, require continuous cancellation. Offset cancellation is a critical function needed for maintenance of measurement accuracy and sensitivity. The DC offset cancellation loop performs this function, and its response is largely defined by the capacitance off the C_{OFS} pin. Setting DC offset cancellation, loop bandwidth strives to strike a balance between offset cancellation accuracy, and loop response time. A larger value of C_{OFS} results in a more precise offset cancellation, but at the expense of a slower offset cancellation response. A smaller value of C_{OFS} tilts the performance trade-off towards a faster offset cancellation response. The optimal loop bandwidth setting will allow internal offsets to be cancelled at a minimally acceptable speed.

DC Offset Cancellation Loop ≈ $\frac{1}{\pi(5000)(C_{OFS} + 20\times10^{12})}$ Bandwidth , Hz

For example: loop bandwidth for DC cancellation with C_{OFS} = 1nF, bandwidth is ~62 kHz

Note:
The measurement error produced by internal DC offsets cannot be measured at any single operating point, in terms of input signal frequency and level, with repeatability. Measurement error must be calculated to a best fit line, over the entire operating range (again, in terms of signal level and frequency).

Standby Mode

The ENX can be used to force the power detector into a low-power standby mode. In this mode, the entire power detector is powered-down. As ENX is deactivated, power is restored to all of the circuits. There is no memory of previous conditions. Coming-out of stand-by, C_{INT} and C_{OFS} capacitors will require recharging, so if large capacitor values have been chosen, the wake-up time will be lengthened.

Adjusting V_{TGT} for greater precision

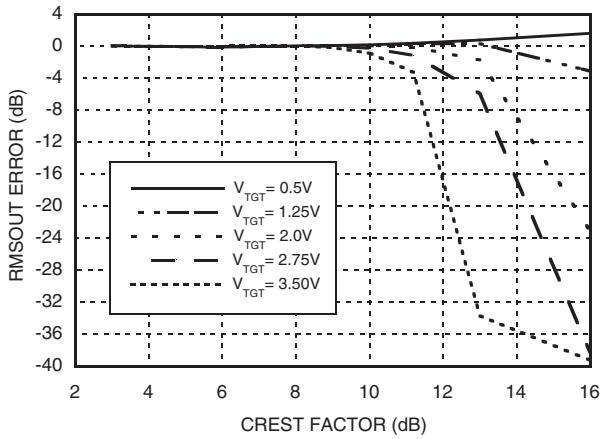
There are two competing aspects of performance, for which V_{TGT} can be used to set a preference. Depending on which aspect of precision is more important to the application, the V_{TGT} pin can be used to find a compromise between two sources of RMS output error: internal DC offset cancellation error and deviation at high crest factors (>10 dB).

- Increasing V_{TGT} input voltage will improve internal DC offset cancellation, but deviation at high crest factors will increase slightly. A 50% increase in V_{TGT} should produce an 18% improvement in RMS precision due to improved DC offset cancellation performance.
- Decreasing V_{TGT} input voltage will reduce errors at high crest factors, but DC offset cancellation performance will be slightly degraded. See "RMS Output Error vs. Crest Factor" graph.

If input signal crest factor is not expected to exceed 10 dB, you can improve RMS precision by increasing V_{TGT} voltage. Keep in mind that changing V_{TGT} also adjusts the log-intercept point, which shifts the "input dynamic range". The best set-point for V_{TGT} will be the lowest voltage that still maintains the "input dynamic range" over the required range of input power. This new V_{TGT} set-point should optimize DC offset correction performance.

RMS Output Error vs. Crest Factor

Worst Case Conditions
using circuit described in " Application & Evaluation PCB Schematic" section



V_{TGT} Influence on DC Offset Compensation

VT	Error due to Internal DC Offsets
1.0V	Nominal +0.2 dB
1.5V	Nominal +0.1 dB
2.0V	Nominal
3.0V	Nominal -0.06 dB
3.5V	Nominal -0.1 dB

If error performance for crest factors >10 dB requires optimization, set V_{TGT} for the maximum tolerable error at the highest expected crest factor. Increasing V_{TGT} beyond that point will unnecessarily compromise internal DC offset cancellation performance. After changing V_{TGT}, re-verify that the "input dynamic range" still covers the required range of input power.

V_{TGT} should be referenced to V_{REF} for best performance. It is recommended to use a temperature stable DC amplifier between V_{TGT} and V_{REF} to create $V_{TGT} > V_{REF}$. The V_{REF} pin is a temperature compensated voltage reference output, only intended for use with V_{TGT}.

System Calibration

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements. When performing this calibration, choose at least two test points: near the top end and bottom-end of the measurement range. It is best to measure the calibration points in the regions (of frequency and amplitude) where accuracy is most important. Derive the log-slope and log-intercept, and store them in non-volatile memory.

System Calibration *(Continued)*

For example if the following two calibration points were measured at 2.35 GHz:

With Vrms = 2.34V at Pin= -7dBm,	Now performing a power measurement:
and Vrms=1.84V at Pin= -16dBm	Vrms measures 2.13V
slope calibration constant = SCC	[Measured Pin] = [Measured Vrms]*SCC + ICC
SCC = (-16+7)/(1.84-2.34) = 18 dB/V	[Measured Pin] = 2.13*18.0 – 49.12 = -10.78dBm
intercept calibration constant = ICC	An error of only 0.22dB
ICC = Pin – SCC*Vrms = -7 – 18.0 * 2.34 = -49.12dBm	

Factory system calibration measurements should be made using an input signal representative of the application. If the power detector will operate over a wide range of frequencies, choose a central frequency for calibration.

Layout Considerations

- Mount RF input coupling capacitors close to the IN+ and IN- pins.
- Solder the heat slug on the package underside to a grounded island which can draw heat away from the die with low thermal impedance. The grounded island should be at RF ground potential.
- Connect power detector ground to the RF ground plane, and mount the supply decoupling capacitors close to the supply pins.

Definitions:

- Log-slope: slope of P_{IN} –> V_{RMS} transfer characteristic. In units of mV/dB
- Log-intercept: x-axis intercept of P_{IN} –> V_{RMS} transfer characteristic. In units of dBm.
- RMS Output Error: The difference between the measured P_{IN} and actual P_{IN} using a line of best fit.

  [measured_P_{IN}] = [measured_V_{RMS}] / [best-fit-slope] + [best-fit-intercept], dBm
- Input Dynamic Range: the range of average input power for which there is a corresponding RMS output voltage with “RMS Output Error” falling within a specific error tolerance.
- Crest Factor: Peak power to average power ratio for time-varying signals.

Notes: