0 Document History

Version	Comment	Date
1.0	Initial Version: Fork from 20150402_TPD_SMA130_non_NDA_v1.0_preliminary Changes as compared to TPD: - Disclaimer extended - Document name changed	29.09.2015

Triaxial Accelerometer

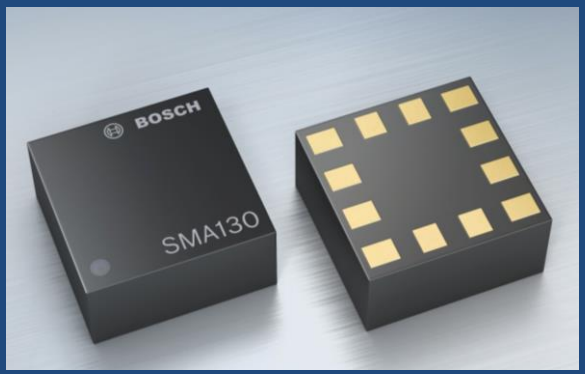
for Non-Safety Automotive Applications

SMA130

Robert Bosch GmbH, Reutlingen, Germany

Part No.: 0 273 141 234

Document No.: 1 279 929 821



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Content

1 Introduction

The SMA130 is a triaxial, low-g accelerometer for non-safety related applications, e.g. for motion control in the passenger compartment. Within one package, the SMA130 offers the detection of acceleration in three perpendicular axes. The digital standard serial peripheral interface (SPI) of the SMA130 allows for bi-directional data transmission.

Basic Description

Sensor	Bosch Part Nr.	Type	Range	Resolution
SMA130	0 273 141 234	Accelerometer	±2, ±4, ±8, ±16 g	14 bit

Key Features

Triaxial accelerometer	Versatile, leading edge triaxial 14bit accelerometer for reduced PCB space and simplified signal routing
Small package	LGA, 12 pins, footprint 2.0 x 2.0 mm², height 0.95 mm
Common voltage supplies	VDD voltage range: 1.62 ... 3.6 V
Digital interface	SPI, TWI (compatible with I^2C)
Consumer electronics suite	MSL1, RoHS compliant, halogen- and Pb-free
Operating temperature	-40 ... +85 °C
Programmable functionality	Acceleration range selectable Low-pass filter bandwidths selectable
On-chip temperature sensor	Factory trimmed, 8-bit

Bosch wishes to point out that the system/product was not developed according to ISO 26262 standards, and has therefore been approved by Bosch only for applications that are not safety-related.

2 Technical Description

2.1 Working Principle of the Sensing Element (MEMS)

The accelerometer SMA130 consists of an evaluation circuitry (ASIC) and a micro-mechanical sensing element (MEMS) within a standard LGA package.

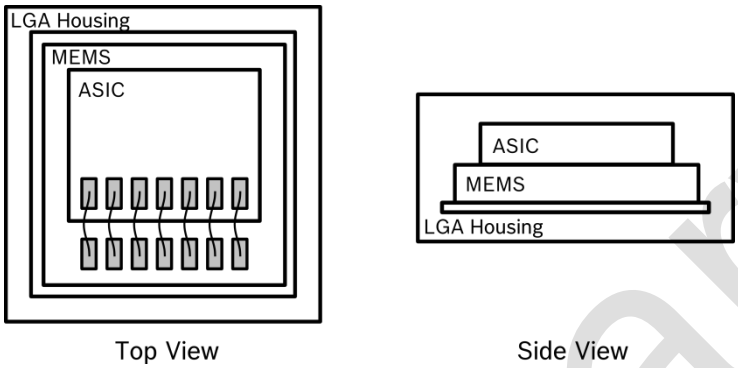


Figure 2-1: Schematics of the SMA130 mechanical design (left: top view; right: side view). The SMA130 consists of a readout ASIC stacked on top of its sensitive MEMS element.

2.2 Block Diagram

Figure 2-2 shows the basic building blocks of the SMA130. An acceleration signal along the sensitive axis of the MEMS element causes a change of the capacitances of the MEMS element. This change is converted into a digital serial bit stream which is further processed and which can be accessed via SPI.

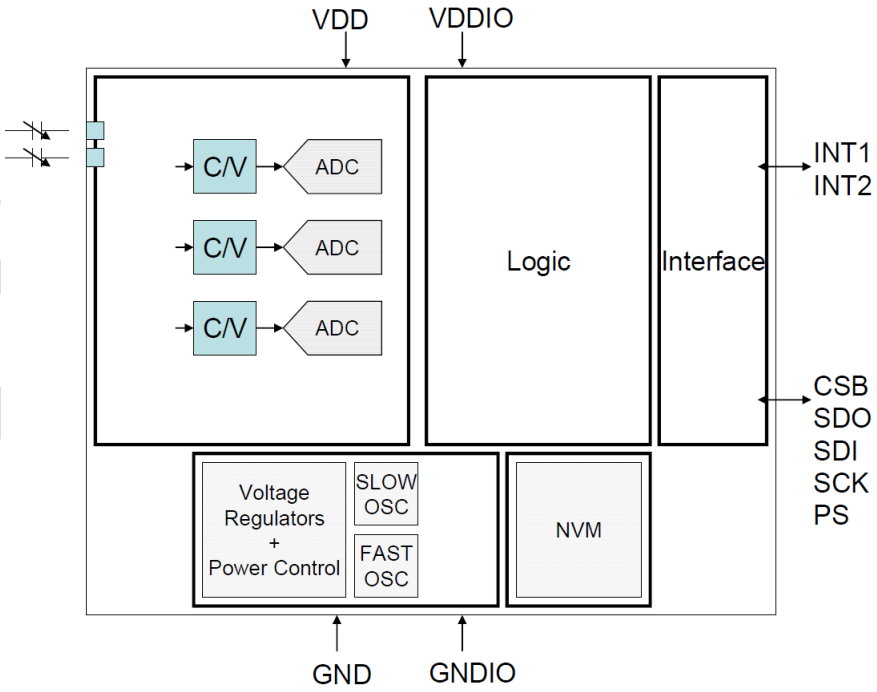


Figure 2-2: Simplified block diagram of the SMA130.

2.3 Signal Path

The SMA130 offers temperature and acceleration data for all three spatial dimensions. For the latter, the differential capacitance change (C) of the corresponding sensing element is detected. This signal corresponds to the voltage (V) entering the hybrid algorithmic analog-digital-converter (ADC), translating the formerly analog signal into a digital serial bit stream at a rate of 400 kHz. Then, the detected signal is translated into a data word of 14 bit and enters the digital signal processor (DSP).

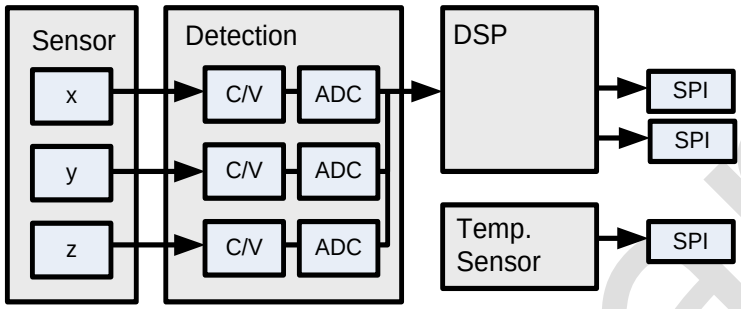


Figure 2-3: Simplified signal path of the SMA130.

Within the DSP (see Figure 2-4), the data is corrected for the analog-digital conversion, gained and offset corrected. A low-pass filter engine provides an adjustable data bandwidth. Here, theith the sampling rate is directly connected with the selected bandwidth.

The low-pass engine can be bypassed so that unfiltered data is accessible.

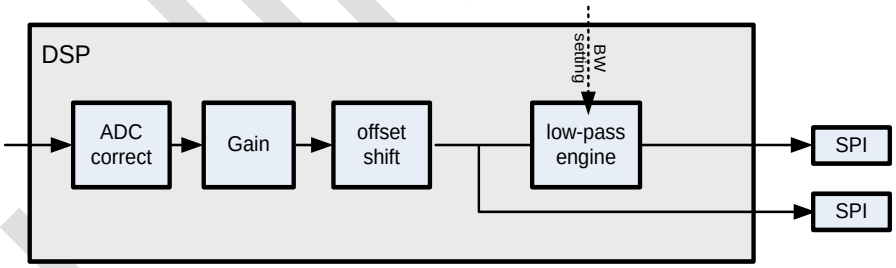


Figure 2-4: Simplified DSP element.

2.4 Power Management

The SMA130 has two distinct power supply pins:

- VDD is the main power supply for the internal blocks.
- VDDIO is a separate power supply pin mainly used for the supply of the interface.

There are no limitations regarding the voltage levels of both pins relative to each other as long as each of them is within the specified operating range. Furthermore, the device can be completely switched off (VDD = 0 V) while keeping the VDDIO supply on (VDDIO > 0 V) or vice versa.

In the case that the VDDIO supply is switched off, all interface pins (CSB, SDI, SCK, PS) must be kept close to GNDIO potential.

The SMA130 provides a **power-on reset (POR)** generator. It resets the logic part and the register values after powering on VDD and VDDIO. After POR, all settings are reset to the default values. All application specific settings which are not equal to the default settings have to be reset to their designated values after POR.

There are no constraints on the switching sequence of VDD and VDDIO. In the case that the TWI interface be used, a direct electrical connection between VDDIO and the PS pin is needed in order to ensure reliable protocol selection. For SPI mode, the PS pin must be directly connected to GNDIO.

2.5 Soft Reset

A soft reset causes all user configuration settings to be overwritten with their default values and the sensor to enter normal mode.

A soft reset is initiated by writing the value 0xB6 to register 0x14 (BGW_SOFTRESET).

2.6 Sensor Data

2.6.1 Accelerometer

The data representation of the SMA130 follows two's complement representation.

For each axis, the 14 bits of acceleration data are split into a MSB upper part (one byte containing bits <13:6> of acceleration data) and a LSB lower part (one byte containing bits <5:0> of acceleration data, one *undefined* bit with random data which is to be ignored and a *new_data* flag). Registers 0x02 (ACCD_X_LSB) and 0x03 (ACCD_X_MSB) contain the acceleration data for the x-channel, registers 0x04 (ACCD_Y_LSB) and 0x05 (ACCD_Y_MSB) for the y-channel and 0x06 (ACCD_Z_LSB) and 0x07 (ACCD_Z_MSB) for the z-channel. It is recommended to always start reading out the acceleration data registers with the LSB part first.

In order to ensure data integrity, a **shadowing procedure** can be enabled. In this case, the content of the MSB register is locked by reading the corresponding LSB register until the MSB register is read as well. This means that the MSB register always has to be read in order to remove the data lock. Shadowing can be disabled (enabled) by writing 1 (0) to bit 6 (*shadow_dis*) in the register 0x13 (ACCD_HBW). For disabled shadowing, the content of both the MSB and the LSB register is updated by new values immediately. Unused bits of the LSB registers may have any value and should be ignored.

New data can be identified by bit 0 (*new_data* flag) of each LSB register. It is set if the data registers have been updated and reset if either the corresponding MSB or LSB part is read.

Two different streams of acceleration data are available, **unfiltered and filtered** data. The unfiltered data is sampled with 2 kHz. The sampling rate (output data rate ODR) of the filtered data depends on the selected filter bandwidth (BW) and is always twice the selected bandwidth (BW = ODR/2). Which kind of data is stored in the acceleration data registers depends on bit 7 (*data_high_bw*) in register 0x13 (ACCD_HBW). If bit 7 is 0 (1), filtered (unfiltered) data is stored in the registers. Both data streams are offset-compensated.

The **bandwidth** of filtered acceleration data is determined by setting bits <4:0> (*bw*) in register 0x10 (PMU_BW) as shown in the following table.

bw	Bandwidth	Update Time
00xxx	*)	-
01000	7.81 Hz	64 ms
01001	15.63 Hz	32 ms
01010	31.25 Hz	16 ms
01011	62.5 Hz	8 ms
01100	125 Hz	4 ms
01101	250 Hz	2 ms
01110	500 Hz	1 ms
01111	unfiltered	0.5 ms
1xxxx	*)	-

*) The *bw* settings 00xxx and 1xxxx are both reserved. *bw* = 00xxx results in a bandwidth of 7.81 Hz, *bw* = 1xxxx results in an unfiltered signal. It is recommended to actively set an appropriate, application specific bandwidth and to use the *bw* range from 01000 to 01111.

The acceleration measurement **range** can be selected via bits <3:0> (*range*) in register 0x0F (PMU_RANGE) according to the table below.

range	Acceleration Measurement Range	Resolution
0011	±2 g	4096 LSB/g
0101	±4 g	2048 LSB/g
1000	±8 g	1024 LSB/g
1100	±16 g	512 LSB/g
others	reserved	-

2.6.2 Temperature Sensor

The temperature sensor data are given in two's complement representation with a data width of 8 bits. Temperature data can be read from register 0x08 (ACCD_TEMP).

3 Application

Proper function of the sensor in the overall system must be validated by the customer.

3.1 Sensing Axes Orientation

If the sensor is accelerated in the sensing directions indicated in Figure 3-1, the corresponding channels of the device will deliver a positive acceleration signal (dynamic acceleration). If the sensor is at rest and the force of gravity is acting along the indicated sensing directions, the output of the corresponding acceleration channels will be negative (static acceleration).

Example:

If the sensor is at rest or at uniform motion in a gravity field according to Figure 3-1, the output signals are

- ±0 g for the x-channel,
- ±0 g for the y-channel and
- +1 g for the z-channel.

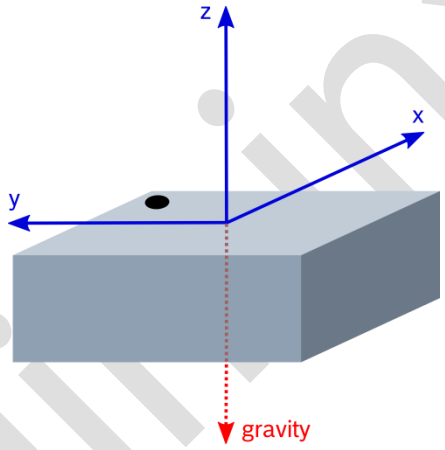
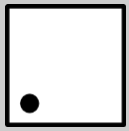
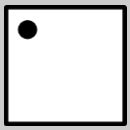
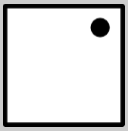
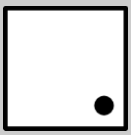


Figure 3-1: Orientation of the sensing axes.

The table below lists all corresponding output signals on x, y and z while the sensor is at rest or at uniform motion in a gravity field under assumption of a ±2 g range setting and a top down gravity vector as shown above.

Sensor orientation (gravity vector ↓)						
Output signal x	0 g 0 LSB	1 g 4096 LSB	0 g 0 LSB	-1 g - 4096 LSB	0 g 0 LSB	0 g 0 LSB
Output signal y	-1 g - 4096 LSB	0 g 0 LSB	1 g 4096 LSB	0 g 0 LSB	0 g 0 LSB	0 g 0 LSB
Output signal z	0 g 0 LSB	0 g 0 LSB	0 g 0 LSB	0 g 0 LSB	1 g 4096 LSB	-1 g - 4096 LSB

3.2 Pin-out

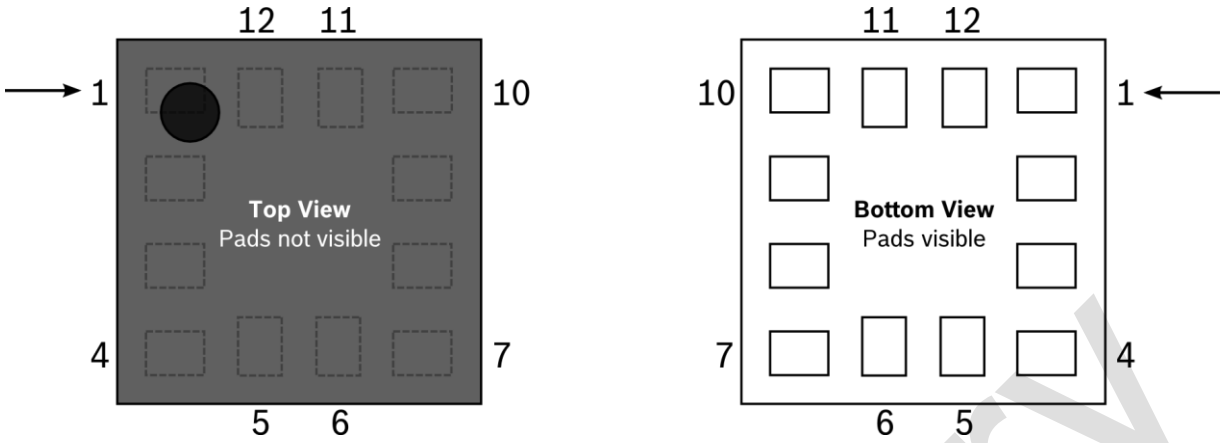


Figure 3-2: Pin-out top view (left) and bottom view (right). The arrow marks pin 1.

Pin	Name	I/O Type	Description	Connect to - SPI -	Connect to - TWI -
1	SDO	Digital out	SPI: serial data out TWI: address select	SDO	GND for default address
2	SDx	Digital I/O	SPI: SDI (serial data in) TWI: SDA (serial data I/O)	SDI	SDA
3	VDDIO	Supply	Digital I/O supply voltage	VDDIO	VDDIO
4	NC	-	-	GND	GND
5	INT1	Digital out	Interrupt pin 1	INT1 / DNC	INT1 / DNC
6	INT2	Digital out	Interrupt pin 2	INT2 / DNC	INT2 / DNC
7	VDD	Supply	Power supply analog & digital domain	VDD	VDD
8	GNDIO	Ground	Ground for I/O	GND	GND
9	GND	Ground	Ground for analog & digital domain	GND	GND
10	CSB	Digital in	SPI: chip select TWI: DNC	CSB	DNC (float)
11	PS	Digital in	Protocol select	GND	VDDIO
12	SCx	Digital in	Serial clock	SCK	SCL

DNC: Do not connect

INTx: If not needed, DNC

3.3 Dimensions and Weight

Dimensions [mm]: width: 2.0; length: 2.0; height 0.95
Weight [mg]: 9.3

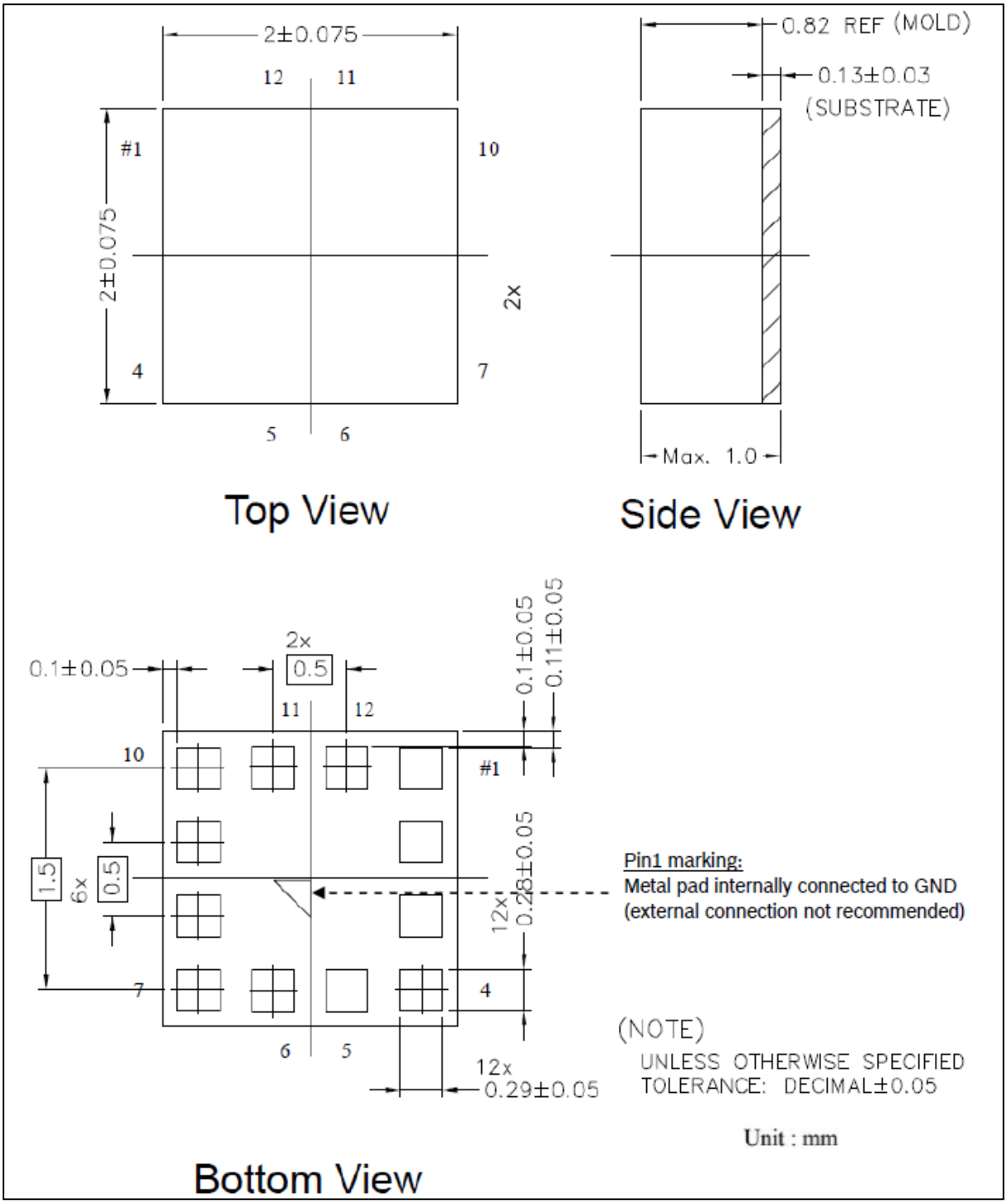


Figure 3-3: SMA130 package outline drawing.

3.4 Marking

tbd

3.5 Footprint

For the design of the landing patterns, the dimensioning as shown in Figure 3-4 is recommended.

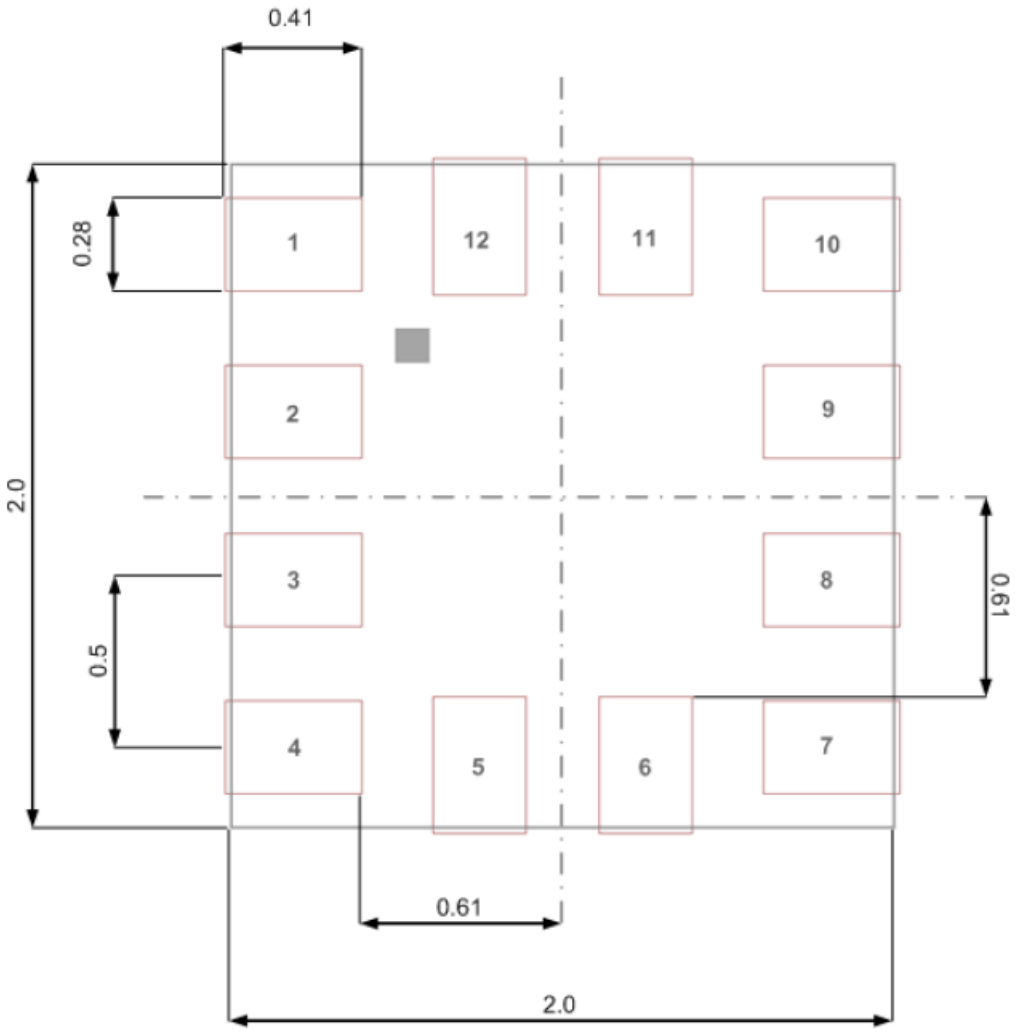


Figure 3-4: SMA130 footprint. All dimensions are given in mm.

The same tolerances as given for the outline dimensions (Section 3.3, Figure 3-3) should be assumed.

A wiring no-go area in the top layer of the PCB below the sensor is strongly recommended (e.g. no vias, wires or other metal structures).

3.6 SPI Connection Diagram

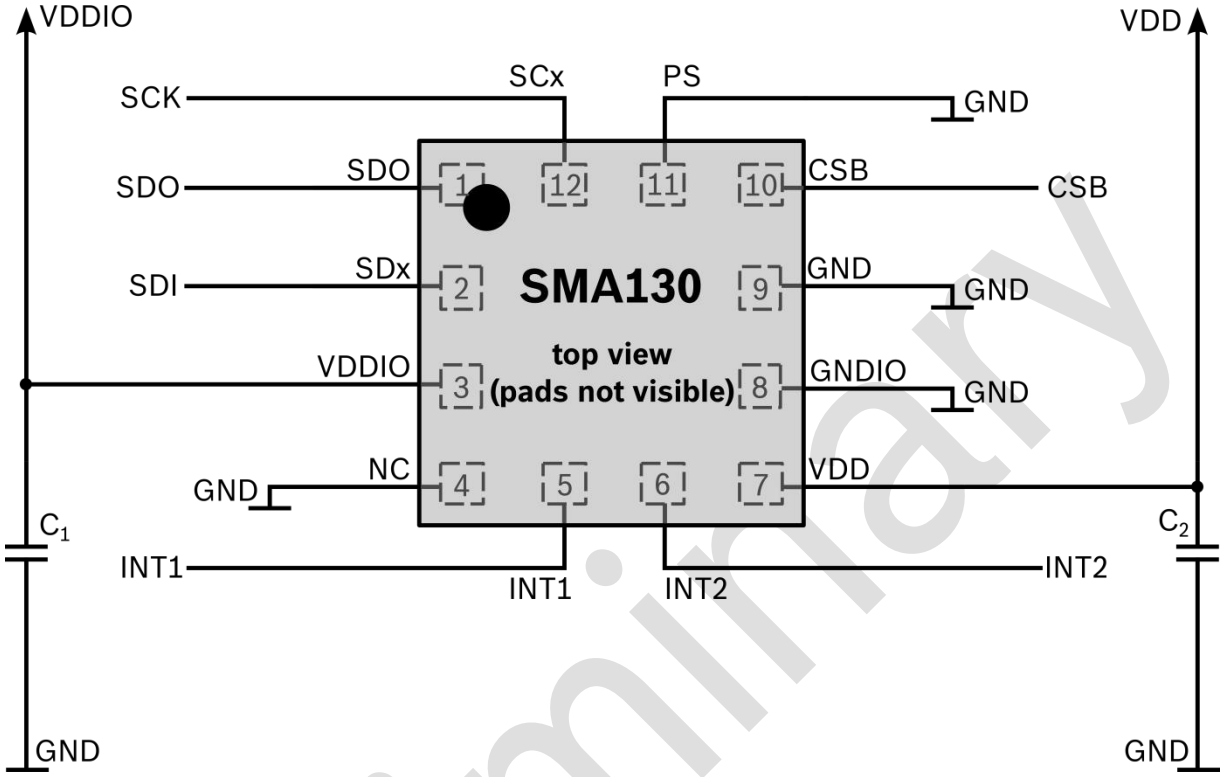


Figure 3-5: SPI connection diagram.

C_1, C_2: 100 nF

3.7 TWI Connection Diagram

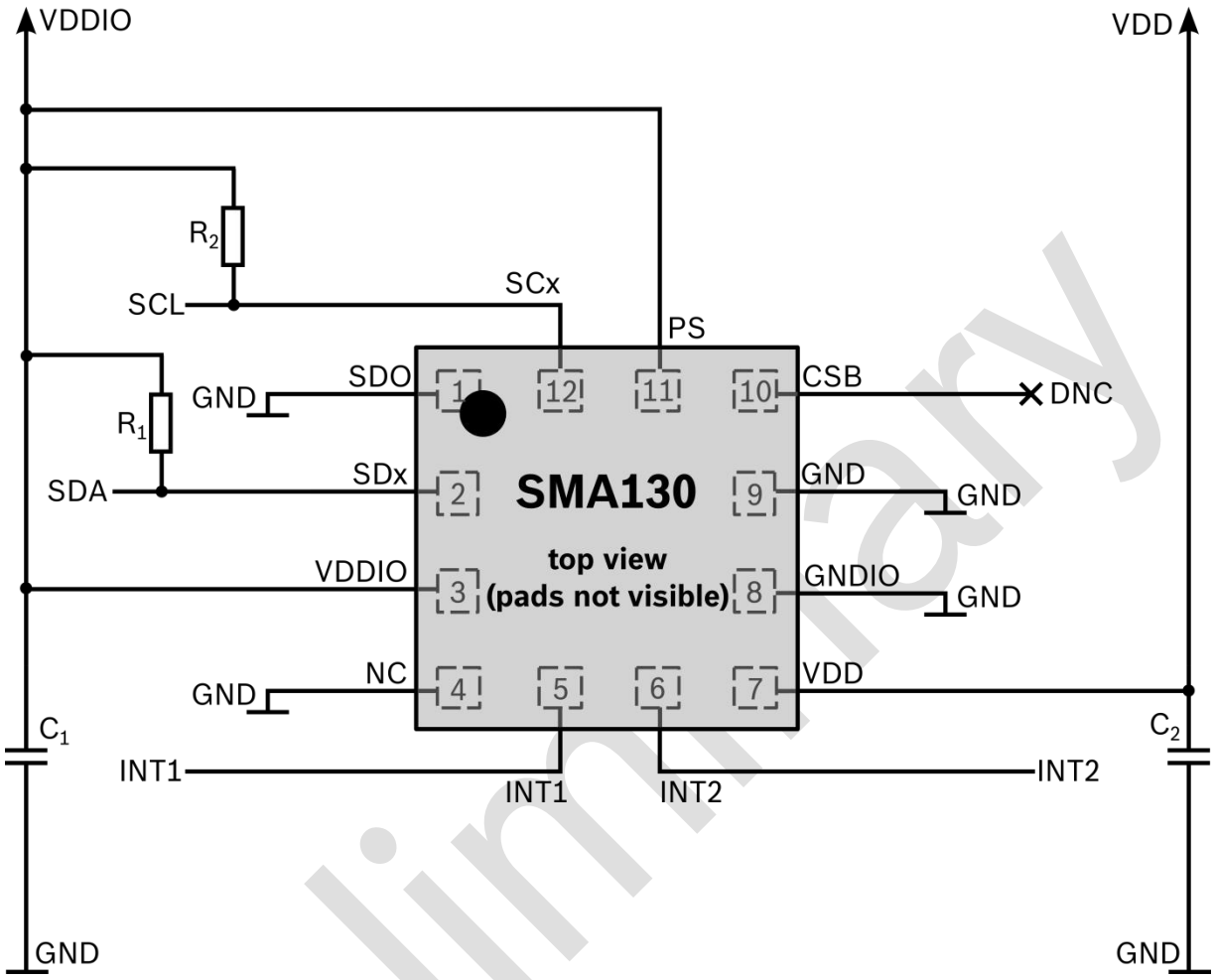


Figure 3-6: TWI connection diagram.

C_1, C_2: 100 nF
R_1, R_2: pull-up resistors

4 Specified Parameters

The data in this chapter, unless otherwise noted, apply for the valid operation conditions given in Section 4.2. All following figures include voltage, temperature and lifetime effects if not noted otherwise. All figures except for sensitivity are only valid without an external stimulus being applied. All operation conditions are only valid if no failure flags indicate any malfunction. All figures except for the noise itself exclude noise effects.

Proper function of the sensor in the overall system must be validated by the customer.

In any case, the electrical stability (power supply and EMC) of each system design including the SMA130 must be evaluated in advance to guarantee proper functionality during operation.

In any case, the mechanical stability of each system design including the SMA130 must be evaluated in advance to guarantee proper functionality during operation.

4.1 Absolute Maximum Ratings

Any values beyond the given ratings may seriously damage the device. The sensor must be discarded when exceeding these limits.

ABSOLUTE MAXIMUM RATINGS				
Parameter	**Condition**	**Min**	**Max**	**Units**
Voltage at supply pin	VDD Pin	-0.3	4.25	V
Voltage at supply pin	VDDIO Pin	-0.3	4.25	V
Voltage at any logic pin	Non-supply pin	-0.3	VDDIO + 0.3	V
Mechanical shock	Free fall onto hard surfaces		1.2	m
Mechanical shock	Duration ≤ 1 ms		2000	g
ESD	HBM, at any pin		2	kV
ESD	CDM		500	V
ESD	MM		200	V

4.2 Operating Conditions

OPERATING CONDITIONS						
Parameter	**Symbol**	**Condition**	**Min**	**Typical**	**Max**	**Units**
Supply voltage internal domains	VDD		1.62	2.4	3.6	V
Supply voltage I/O domain	VDDIO		1.2	2.4	3.6	V
Voltage input low level	V_{IL}				0.3 VDDIO	-
Voltage input high level	V_{IH}		0.7 VDDIO			-
Voltage output low level	V_{OL}	I_{OL} = 3 mA			0.2 VDDIO	-
Voltage output high level	V_{OH}	I_{OH} = 3 mA, SPI	0.8 VDDIO			-
Total supply current	I_{DD}	T = 25 °C, ODR_{max}, VDD = VDDIO = 2.4 V		130	tbd	µA
Start-up time	$T_{s,up}$	POR, ODR_{max}		tbd	tbd (3 ms)	ms
Operating temperature	T		-40		85	°C
Lifetime		According to AEC-Q100 grade 3 requirements				

4.3 Accelerometer Output Signal

ACCELEROMETER OUTPUT SIGNAL (all data for range tbd, BW tbd)						
Parameter	**Sym-bol**	**Condition / Comment**	**Min**	**Typi-cal**	**Max***	**Units**
Measurement range	g_{FS}	selectable		±2 ±4 ±8 ±16		g
Sensitivity	S_{2g} S_{4g} S_{8g} S_{16g}	g_{FS2g}, T = 25 °C g_{FS4g}, T = 25 °C g_{FS8g}, T = 25 °C g_{FS16g}, T = 25 °C		4096 2048 1024 512		LSB/g
Sensitivity error		including temp., axis and lifetime effects		tbd		%
Sensitivity error		T = 25 °C over lifetime		tbd		%
Sensitivity temperature drift	TCS	nominal VDD supply, over full temp. range		0.015		%/K
Zero-g offset		including temp., axis and lifetime effects		tbd		mg
Zero-g offset		T = 25 °C over lifetime		50		mg
Zero-g offset temperature drift	TCO	nominal VDD supply, over full temp. range		±1.0		mg
Bandwidth	BW	selectable 2nd order filter		8 16 31 63 125 250 500		Hz
Output data rate	ODR_{max}	unfiltered		2000		Hz
Nonlinearity	NL	best fit straight line, no life-time		tbd		mg
Noise rms		T = 25 °C, nominal VDD supply, no lifetime		tbd		mg
Noise density		T = 25 °C, nominal VDD supply, no lifetime		120		µg/√Hz
Cross axis sensitivity		including temp., axis and lifetime effects		1		%
Temperature sensor measurement range			-40		+85	°C
Temperature sensor slope				0.5		K/LSB

Temperature sensor offset		T = 25 °C		±2		K

* For specified maximum values, please refer to the Technical Customer Documentation.

5 Communication

The SMA130 supports two serial digital interface protocols for communication as a slave with a host device, SPI and I^2C compatible TWI. The active interface is selected by the state of the protocol select (PS) pin: 0 (1) selects SPI (TWI).

Both interfaces share the same pins. The mapping for each interface is given in the table below.

Pin	Name	Use with SPI	Use with TWI	Description
1	SDO	SDO	Address	SPI: serial data output TWI: used to set LSB of TWI address
2	SDx	SDI	SDA	SPI: serial data input TWI: serial data
10	CSB	CSB	Unused	SPI: chip select (enable) TWI: do not connect
12	SCx	SCK	SCL	Serial clock

The electrical specifications of the interface pins are shown in the table below.

Parameter	Symbol	Condition	Min	Typical	Max	Units
Pull-up resistance, CSB pin	R_{up}	Internal pull-up resistance to VDDIO	75	100	125	kΩ
Input capacitance	C_{in}			5	10	pF
TWI bus load capacitance (max. drive capability)	C_{TWI_load}				400	pF

5.1 Serial Peripheral Interface (SPI)

The timing specification for SPI of the SMA130 is given in the table below.

Parameter	Symbol	Condition	Min	Max	Units
Clock frequency	f_{SPI}	max. load on SDI or SDO = 25 pF, VDDIO ≥ 1.62 V		10	MHz
Clock frequency	f_{SPI}	max. load on SDI or SDO = 25 pF, VDDIO < 1.62 V		7.5	MHz
SCK low pulse	t_{SCKL}		20		ns
SCK high pulse	t_{SCKH}		20		ns
SDI setup time	t_{SDI_setup}		20		ns
SDI hold time	t_{SDI_hold}		20		ns
SDO output delay	t_{SDO_OD}	load = 25 pF, VDDIO ≥ 1.62 V		30	ns
SDO output delay	t_{SDO_OD}	load = 25 pF, VDDIO < 1.62 V		50	ns
SDO output delay	t_{SDO_OD}	load = 250 pF, VDDIO > 2.4 V		40	ns
CSB setup time	t_{CSB_setup}		20		ns
CSB hold time	t_{CSB_hold}		40		ns
Idle time between write accesses	$t_{IDLE\_wacc\_nm}$		2		µs

Figure 5-1 shows the definition of the SPI timings.

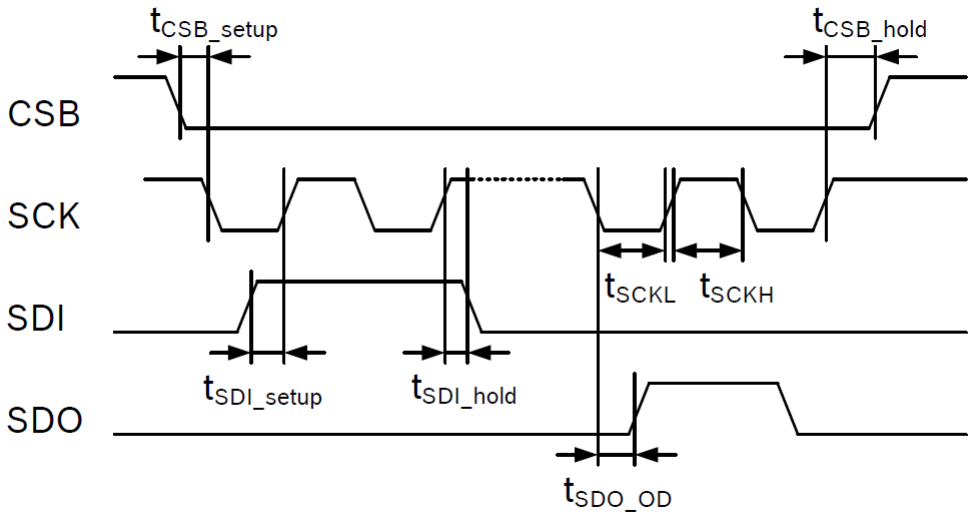


Figure 5-1: SPI timing diagram.

The SPI interface of the SMA130 is compatible with two modes, 00 and 11. The automatic selection between [CPOL = 0 and CPHA = 0] and [CPOL = 1 and CPHA = 1] is controlled based on the value of SCK after a falling edge of CSB. For single byte read as well as write operations, 16-bit protocols are used. The SMA130 also supports multiple-byte read operations.

For the standard SPI configuration, CSB (chip select low active), SCK (serial clock), SDI (serial data input) and SDO (serial data output) pins are used. The communication starts when CSB is pulled low by the SPI master and stops when CSB is pulled high. SCK is also controlled by the SPI master. SDI and SDO are driven at the falling edge of SCK and should be captured at the rising edge of SCK.

The basic write operation waveform for SPI configuration is depicted in Figure 5-2. During the full write cycle, SDO remains in high-impedance state.

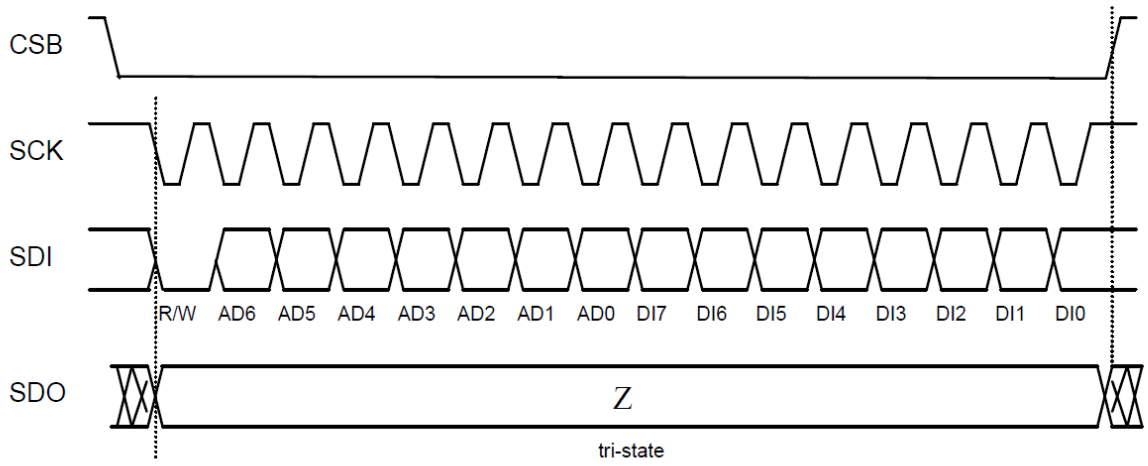


Figure 5-2: Basic SPI write sequence (mode 11).

The basic read operation waveform for SPI configuration is depicted in Figure 5-3.

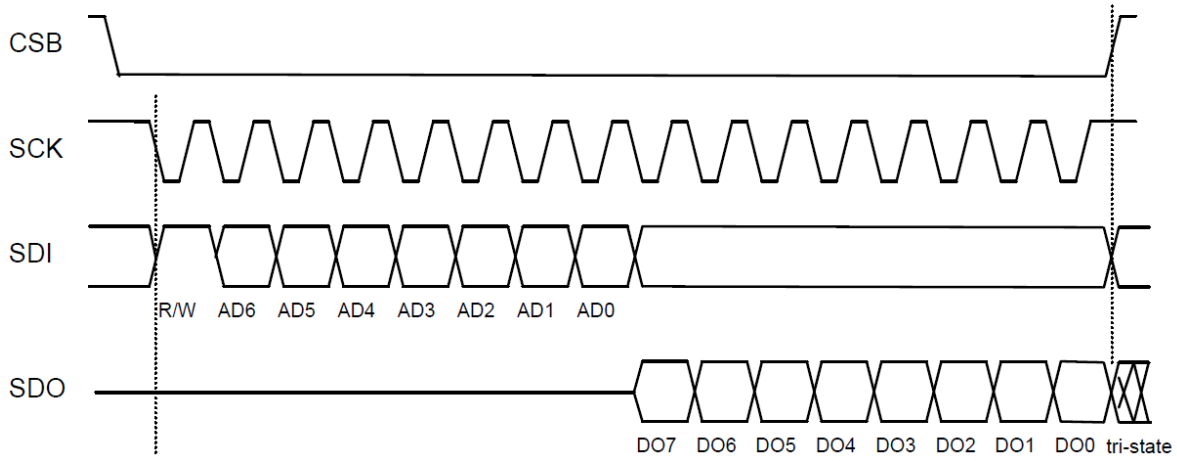


Figure 5-3: Basic SPI read sequence (mode 11).

The data bits are used as follows:

Bit 15: Read/write bit. When 0, the data SDI is written into the chip. When 1, the data SDO from the chip is read.

Bits <14:8>: Address AD(6:0).

Bits <7:0>: When in write mode, these are the data SDI which will be written into the address. When in read mode, these are the data SDO which are read from the address.

Multiple read operations are possible by keeping CSB low and continuing the data transfer. Only the first register address has to be written. Addresses are automatically incremented after each read access as long as CSB stays active low.

The principle of a multiple read operation is shown in Figure 5-4.

	Control byte								Data byte								Data byte								Data byte								
Start	RW	Register adress (02h)							Data register - adress 02h								Data register - adress 03h								Data register - adress 04h								Stop
CSB = 0	1	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CSB = 1

Figure 5-4: SPI multiple read.

5.2 Two-Wire Interface (TWI)

The TWI bus uses SCL (= SCx pin, serial clock) and SDA (= SDx pin, serial data input and output) signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free.

With some exceptions, the TWI interface of the SMA130 is compatible to the I²C specification UM10204 Rev. 03 (19 June 2007), available at http://www.nxp.com:

- The SMA130 supports the I²C standard and fast mode, but only the 7-bit address mode.
- For VDDIO = 1.2 ... 1.8 V the granted voltage output levels are slightly relaxed compared to the specification.
- The internal data hold time (t_{HDDAT}) of 300 ns is not met under all operation conditions. The device achieves a minimum value of 120 ns across process corners and temperature.
- The minimum data fall time (t_F) of ≥ 20 ns cannot be met.
- Only single byte write is supported.
- Detection of a stop condition is not supported. All data transfer protocols are fully operational by means of detecting the start condition only.
- The device does not support the high-impedance mode while VDDIO is tied to GND.
- The device does not perform clock stretching, i.e., clock frequencies may not exceed the one specified in the parameter section, and wait times between subsequent write accesses (as specified in Section 5.3) have to be ensured by the bus master.

The default TWI address of the SMA130 is 0x18 (0011000). It is used if the SDO pin is pulled to GND. The alternative address 0x19 (0011001) is selected by pulling the SDO pin to VDDIO.

The TWI timing specification for the SMA130 is given in the table below.

Parameter	Symbol	Min	Max	Units
Clock frequency	f_{SCL}		400	kHz
SCL low period	t_{LOW}	1.3		µs
SCL high period	t_{HIGH}	0.6		µs
SDA setup time	t_{SUDAT}	0.1		µs
SDA hold time	t_{HDDAT}	0.0		µs
Setup time for a repeated start condition	t_{SUSTA}	0.6		µs
Hold time for a start condition	t_{HDSTA}	0.6		µs
Setup time for a stop condition	t_{SUSTO}	0.6		µs
Time before a new transmission can start	t_{BUF}	1.3		µs
Idle time between write accesses	$t_{IDLE\_wacc\_nm}$	2		µs

Figure 5-5 shows the definition of the TWI timing given in the table above.

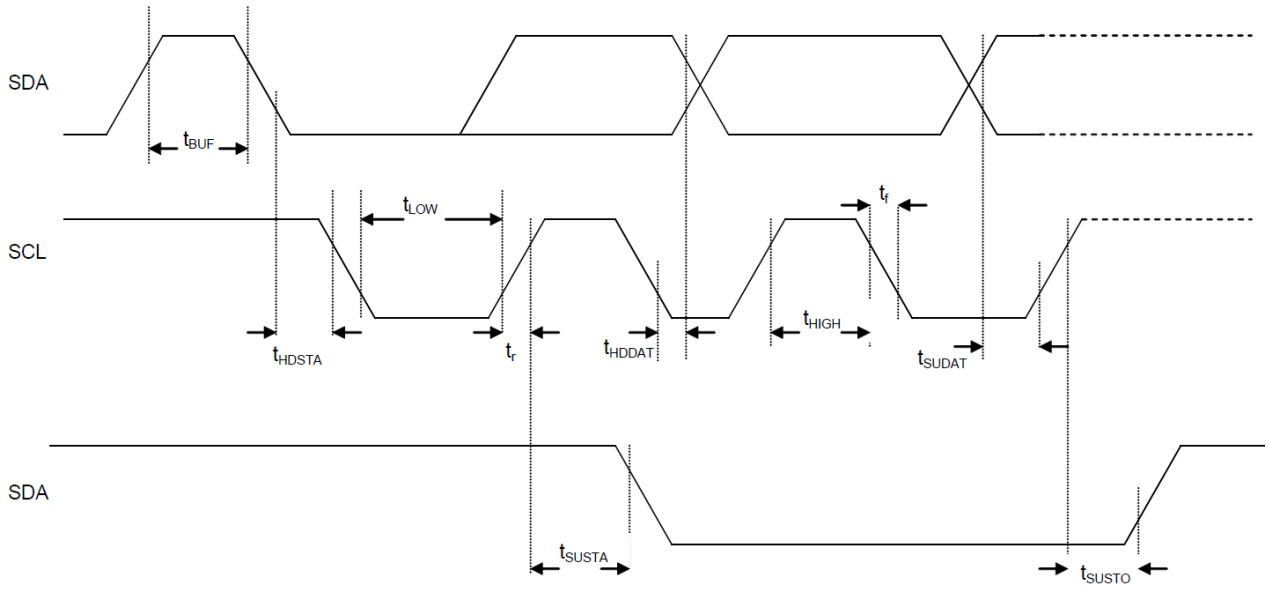


Figure 5-5: SMA130 TWI timing specification.

The TWI protocol works as follows:

START: Data transmission on the bus begins with a high to low transition on the SDA line while SCL is held high (start condition (S) indicated by the TWI bus master). Once the start signal is transferred by the master, the bus is considered busy.

STOP: Each data transfer should be terminated by a stop signal (P) generated by the master. The stop condition is a low to high transition on the SDA line while SCL is held high.

ACK: Each byte of data transferred must be acknowledged. It is indicated by an acknowledge bit sent by the receiver. The transmitter must release the SDA line (no pull down) during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

In the following diagrams these abbreviations are used:

S	Start
P	Stop
ACKS	Acknowledge by slave
ACKM	Acknowledge by master
NACKM	Not acknowledge by master
RW	Read / Write

A start (S) immediately followed by a stop (P) (without SCK toggling from VDDIO to GND) is not supported and not recognized by the SMA130.

TWI write access can be used to write a data byte in one sequence.

The sequence begins with a start condition generated by the master, followed by 7 bits of slave address and a write bit (RW = 0). The slave sends an acknowledge bit (ACK = 0) and releases the bus. Then the master sends the one byte register address. The slave again acknowledges the transmission and waits for the 8 bits of data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol. Figure 5-6 shows an example of a TWI write access.

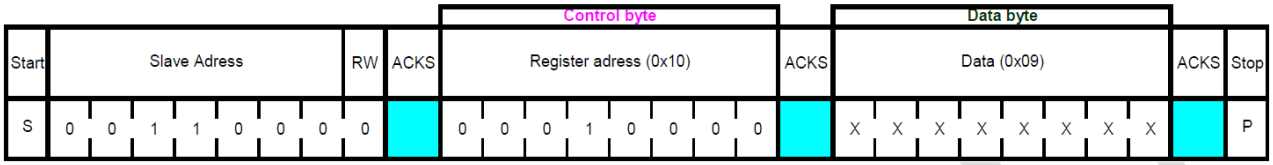


Figure 5-6: TWI write access.

TWI read access can be used to read one or multiple data bytes in one sequence.

A read sequence consists of a one-byte TWI write phase followed by the TWI read phase. Both parts of the transmission must be separated by a repeated start condition (Sr). The TWI write phase addresses the slave and sends the register address to be read. After the slave acknowledges the transmission, the master again generates a start condition and sends the slave address together with a read bit (RW = 1). Then the master releases the bus and waits for the data bytes to be read out from the slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACKM (ACK = 1) from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a stop condition and terminate the transmission.

The register address is automatically incremented. Hence, more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the latest TWI write command. By default the start address is set as 0x00. In this way, repetitive multi-byte reads from the same starting address are possible.

In order to prevent the TWI slave from locking up the TWI bus, a watchdog timer (WDT) is implemented. The WDT observes internal TWI signals and resets the TWI interface if the bus is locked up. Activity and timer period of the WDT can be configured via bits 2 (*i2c_wdt_en*) and 1 (*i2c_wdt_sel*) in register 0x34 (BGW_ WDT).

- Writing 1 (0) to *i2c_wdt_en* activates (de-activates) the WDT.
- Writing 0 (1) to *i2c_wdt_sel* selects a timer period of 1 ms (50 ms).

Figure 5-7 shows an example of a TWI multiple read access.

Figure 5-7: TWI multiple read access.

5.3 Access Restrictions (SPI and TWI)

In order to allow for the correct internal synchronization of data written to the SMA130, certain access restrictions apply for consecutive write accesses or a write/read sequence through the SPI and TWI interface.

As illustrated in Figure 5-8, an interface idle time of at least 2 µs is required following a write operation when the device operates.

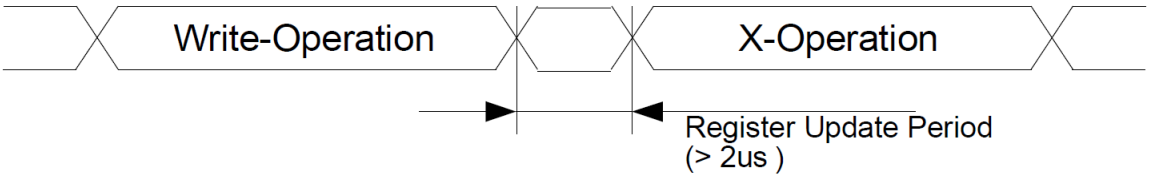


Figure 5-8: Post-write access timing constraints.

5.4 Self-Test

The self-test feature allows for checking the sensor functionality by applying electrostatic forces to the sensor core instead of external accelerations. By physically deflecting the seismic mass, the entire signal path of the sensor is tested. Activation of the self-test results in a static offset in the acceleration data. Any external acceleration or gravitational force which is applied to the sensor during a self-test will be observed in the sensor output as a superposition of the acceleration and the self-test signal.

Before enabling the self-test, the acceleration measurement range should be set to **4 g**.

The self-test is activated for **each axis separately** by setting bits <1:0> (*self_test_axis*) of register 0x32 (PMU_SELF_TEST) to 01 for the x-axis, 10 for the y-axis or 11 for the z-axis. For *self_test_axis* = 00, the self-test is disabled. The **direction of the deflection** is controlled via bit 2 (*self_test_sign*). The deflection is negative (positive) when setting *self_test_sign* to 0 (1).

After enabling the self-test, a **waiting time of 50 ms** is mandatory before the acceleration data are interpreted.

For a proper interpretation of the self-test signals, it is recommended to perform the self-test for both the positive and the negative direction and to then calculate the difference of the resulting acceleration values. The minimum difference for each axis is shown in the table below. The actually measured signal differences can be significantly larger.

	x-axis	y-axis	z-axis
minimum difference signal	800 mg	800 mg	400 mg

After performing a self-test, a reset of the device is recommended. If the reset cannot be performed, the following sequence must be kept to prevent unwanted interrupt generation:

1. Disable interrupts.
2. Change parameters of interrupts.
3. Wait for at least 50 ms.
4. Enable desired interrupts.

6 Register Description

6.1 General Remarks

The entire communication with the device is performed by reading from and writing to registers. Registers have a width of 8 bits. They are mapped to a common space of 64 addresses from 0x00 up to 0x3F. Within this range some registers are either completely or partially marked as 'reserved'. Any reserved bit is ignored when it is written and no specific value is guaranteed when the bit is read. It is recommended not to use registers which are completely marked as 'reserved' at all. Furthermore it is recommended to mask out (logical and with zero) reserved bits of registers which are partially marked as reserved.

Registers with addresses from 0x00 up to 0x0E are read-only. Any attempt to write to those registers will be ignored. There are bits within some registers that trigger internal sequences. These bits are configured for write-only access and read as 0. An example for such a write-only access is the entire register 0x14 (BGW_SOFTRESET).

6.2 Register Map

Figure 6-1 shows the register map of the SMA130.

Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Default
0x34						i2c_wdt_en	i2c_wdt_sel		0x00
0x32						self_test_sign	self_test_axis <1:0>		0x00
0x20					int2_od	int2_lvl	int1_od	int1_lvl	0x05
0x1E			int_src_data						0x00
0x1A	int2_data							int1_data	0x00
0x17				data_en					0x00
0x14	softreset								0x00
0x13	data_high_bw	shadow_dis							0x00
0x10	bw <4:0>								0x0F
0x0F	range <3:0>								0x03
0x0A	data_int								0x00
0x08	temp <7:0>								0x00
0x07	acc_z_msb <13:6>								0x00
0x06	acc_z_lsb <5:0>							new_data_z	0x00
0x05	acc_y_msb <13:6>								0x00
0x04	acc_y_lsb <5:0>							new_data_y	0x00
0x03	acc_x_msb <13:6>								0x00
0x02	acc_x_lsb <5:0>							new_data_x	0x00
0x00	chip_id <7:0>								0xFB

	w/r
	write only
	ready only
	common w/r registers *)
	reserved

*) Application specific settings not equal to the default settings. Must be reset to designated values after POR or soft-reset.

Figure 6-1: SMA130 register map.

6.2.1 Register 0x00 (BGW_CHIPID)

This register contains the chip identification code.

Name	0x00	BGW_CHIPID		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*chip_id* <7:4>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*chip_id* <3:0>			

chip_id <7:0>: Fixed value 11111011

6.2.2 Register 0x02 (ACCD_X_LSB)

This register contains the least significant bits of the x-channel acceleration readout value. When reading out x-channel acceleration values, data consistency is guaranteed if the ACCD_X_LSB is read out before the ACCD_X_MSB and *shadow_dis* = 0. In this case, after the ACCD_X_LSB has been read, the value in the ACCD_X_MSB register is locked until the ACCD_X_MSB has been read. Acceleration data may be read from register ACCD_X_LSB at any time except during power-up.

Name	0x02	ACCD_X_LSB		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_x_lsb* <5:2>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_x_lsb* <1:0>		*undefined*	*new_data_x*

acc_x_lsb <5:0>: Least significant 6 bits of the acceleration x-channel read-back value (two's complement format)

undefined: Random data, to be ignored

new_data_x: 0: acceleration value has not been updated since it has been read out last
1: acceleration value has been updated since it has been read out last

6.2.3 Register 0x03 (ACCD_X_MSB)

This register contains the most significant bits of the x-channel acceleration readout value. When reading out x-channel acceleration values, data consistency is guaranteed if the ACCD_X_LSB is read out before the ACCD_X_MSB and *shadow_dis* = 0. In this case, after the ACCD_X_LSB has been read, the value in the ACCD_X_MSB register is locked until the ACCD_X_MSB has been read. Acceleration data may be read from register ACCD_X_MSB at any time except during power-up.

Name	**0x03**	**ACCD_X_MSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_x_msb* <13:10>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_x_msb* <9:6>			

acc_x_msb <11:4>: Most significant 8 bits of the acceleration x-channel read-back value (two's complement format)

6.2.4 Register 0x04 (ACCD_Y_LSB)

This register contains the least significant bits of the y-channel acceleration readout value. When reading out y-channel acceleration values, data consistency is guaranteed if the ACCD_Y_LSB is read out before the ACCD_Y_MSB and *shadow_dis* = 0. In this case, after the ACCD_Y_LSB has been read, the value in the ACCD_Y_MSB register is locked until the ACCD_Y_MSB has been read. Acceleration data may be read from register ACCD_Y_LSB at any time except during power-up.

Name	**0x04**	**ACCD_Y_LSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_y_lsb* <5:2>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_y_lsb* <1:0>		*undefined*	*new_data_y*

acc_y_lsb <5:0>: Least significant 6 bits of the acceleration y-channel read-back value (two's complement format)

undefined: Random data, to be ignored

new_data_y: 0: acceleration value has not been updated since it has been read out last
1: acceleration value has been updated since it has been read out last

6.2.5 Register 0x05 (ACCD_Y_MSB)

This register contains the most significant bits of the y-channel acceleration readout value. When reading out y-channel acceleration values, data consistency is guaranteed if the ACCD_Y_LSB is read out before the ACCD_Y_MSB and *shadow_dis* = 0. In this case, after the ACCD_Y_LSB has been read, the value in the ACCD_Y_MSB register is locked until the ACCD_Y_MSB has been read. Acceleration data may be read from register ACCD_Y_MSB at any time except during power-up.

Name	**0x05**	**ACCD_Y_MSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_y_msb* <13:10>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_y_msb* <9:6>			

acc_y_msb <13:6>: Most significant 8 bits of the acceleration y-channel read-back value (two's complement format)

6.2.6 Register 0x06 (ACCD_Z_LSB)

This register contains the least significant bits of the z-channel acceleration readout value. When reading out z-channel acceleration values, data consistency is guaranteed if the ACCD_Z_LSB is read out before the ACCD_Z_MSB and *shadow_dis* = 0. In this case, after the ACCD_Z_LSB has been read, the value in the ACCD_Z_MSB register is locked until the ACCD_Z_MSB has been read. Acceleration data may be read from register ACCD_Z_LSB at any time except during power-up.

Name	**0x06**	**ACCD_Z_LSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_z_lsb* <5:2>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_z_lsb* <1:0>		*undefined*	*new_data_z*

acc_z_lsb <5:0>: Least significant 6 bits of the acceleration z-channel read-back value (two's complement format)

undefined: Random data, to be ignored

new_data_z: 0: acceleration value has not been updated since it has been read out last
1: acceleration value has been updated since it has been read out last

6.2.7 Register 0x07 (ACCD_Z_MSB)

This register contains the most significant bits of the z-channel acceleration readout value. When reading out z-channel acceleration values, data consistency is guaranteed if the ACCD_Z_LSB is read out before the ACCD_Z_MSB and *shadow_dis* = 0. In this case, after the ACCD_Z_LSB has been read, the value in the ACCD_Z_MSB register is locked until the ACCD_Z_MSB has been read. Acceleration data may be read from register ACCD_Z_MSB at any time except during power-up.

Name	**0x07**	**ACCD_Z_MSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_z_msb* <13:10>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_z_msb* <9:6>			

acc_z_msb <13:6>: Most significant 8 bits of the acceleration z-channel read-back value (two's complement format)

6.2.8 Register 0x08 (ACCD_TEMP)

This register contains the current chip temperature as a 8 bit data word in two's complement format. A readout value of temp <7:0> = 0x00 corresponds to a temperature of 23 °C.

Name	**0x08**	**ACCD_TEMP**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	*temp* <7:4>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	*temp* <3:0>			

temp <7:0>: Temperature value (two's complement format)

6.2.9 Register 0x0A (INT_STATUS_1)

This register contains the interrupt status flag *data_int* of the new data interrupt.

The new data interrupt allows for synchronous reading of acceleration data. It is generated after a new value of z-axis acceleration data has been stored in the data register.

The interrupt is cleared automatically when the next data acquisition cycle starts. The interrupt status is 0 for a minimum of 50 µs. It is fixed to the non-latched mode.

The interrupt function associated with the status flag has to be enabled via setting bit 4 (*data_en*) in register 0x17 (INT_EN_1) to 1.

Name	**0x0A**	**INT_STATUS_1**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*data_int*	*reserved*		

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*reserved*			

data_int: Data ready interrupt status
0: inactive
1: active

reserved: Random data, to be ignored

6.2.10 Register 0x0F (PMU_RANGE)

This register allows for the selection of the accelerometer g-range.

Name	**0x0F**	**PMU_RANGE**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1
Content	*range* <3:0>			

range <3:0>: Selection of the accelerometer g-range

		Resolution [LSB/g]
0011:	±2 g	4096
0101:	±4 g	2048
1000:	±8 g	1024
1100:	±16 g	512

All other settings: reserved (do not use)

reserved: Write 0

6.2.11 Register 0x10 (PMU_BW)

This register allows for the selection of the acceleration data filter bandwidth.

Name	0x10	PMU_BW		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			*bw* <4>

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1
Content	*bw* <3:0>			

bw <4:0>: Selection of the data filter bandwidth

00xxx:	7.81 Hz	01010:	31.25 Hz	01101:	250 Hz
01000:	7.81 Hz	01011:	62.50 Hz	01110:	500 Hz
01001:	15.63 Hz	01100:	125.00 Hz	01111:	ODR_{max}
				1xxxx:	ODR_{max}

reserved: Write 0

6.2.12 Register 0x13 (ACCD_HBW)

This register controls the acceleration data acquisition and data output format.

Name	0x13	ACCD_HBW		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0 (1 in 8-bit mode)	0	0
Content	*data_high_bw*	*shadow_dis*	*reserved*	

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

data_high_bw: Data-read from the acceleration data registers
1: unfiltered
0: filtered

shadow_dis: The shadowing mechanism for the acceleration data output registers. When shadowing is enabled, the content of the acceleration data component in the MSB register is locked when the component in the LSB is read, thereby ensuring the integrity of the acceleration data during read-out. The lock is removed when the MSB is read.
1: disable
0: enable

reserved: Write 0

6.2.13 Register 0x14 (BGW_SOFTRESET)

This register controls the user triggered reset of the sensor.

Name	0x14	BGW_SOFTRESET		
Bit	7	6	5	4
Read/Write	W	W	W	W
Reset Value	0	0	0	0
Content	*softreset*			

Bit	3	2	1	0
Read/Write	W	W	W	W
Reset Value	0	0	0	0
Content	*softreset*			

softreset: Writing 0xB6 to the register triggers a reset. Other values are ignored. After a delay, all user configuration settings are overwritten with their default values. Please note that all application specific settings which are not equal to the default settings (refer to the register map in Section 6.2) must be reconfigured to their designated values.

6.2.14 Register 0x17 (INT_EN_1)

This register enables the new data interrupt. See bit *data_int* in register 0x0A (INT_STATUS_1).

Name	0x17	INT_EN_1		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			*data_en*

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

data_en: Data ready interrupt
0: disabled
1: enabled

reserved: Write 0

6.2.15 Register 0x1A (INT_MAP_1)

This register controls which interrupt signals are mapped to the INT1 and INT2 pins.

Name	0x1A	INT_MAP_1		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*int2_data*	*reserved*		

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			*int1_data*

int2_data: Map data ready interrupt to the INT2 pin
0: disabled
1: enabled

int1_data: Map data ready interrupt to the INT1 pin
0: disabled
1: enabled

reserved: Write 0

6.2.16 Register 0x1E (INT_SRC)

This register controls the data source definition for interrupts with selectable data source.

Name	0x1E	INT_SRC		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*		*int_src_data*	*reserved*

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

int_src_data: Data for new data interrupt
0: filtered
1: unfiltered

reserved: Write 0

6.2.17 Register 0x20 (INT_OUT_CTRL)

This register controls the electrical behavior and configuration of the interrupt pins.

Name	**0x20**	**INT_OUT_CTRL**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1
Content	*int2_od*	*int2_lvl*	*int1_od*	*int1_lvl*

int2_od: Behavior for the INT2 pin
0: push-pull
1: open drain

int2_lvl: Level for the INT2 pin
0: active low
1: active high

int1_od: Behavior for the INT1 pin
0: push-pull
1: open drain

int1_lvl: Level for the INT1 pin
0: active low
1: active high

reserved: Write 0

6.2.18 Register 0x32 (PMU_SELF_TEST)

This register contains the settings for the sensor self-test configuration and trigger.

Name	0x32	PMU_SELF_TEST		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*	*self_test_sign*	*self_test_axis* <1:0>	

self_test_sign: Select the sign of the self-test excitation
1: positive
0: negative

self_test_axis <1:0>: Select the axis to be self-tested
00: self-test disabled
01: x-axis
10: y-axis
11: z-axis

When a self-test is performed, only the acceleration data readout value of the selected axis is valid; after the self-test has been enabled, a delay of at least 50 ms is necessary for the read-out value to settle.

reserved: Write 0

6.2.19 Register 0x34 (BGW_WDT)

This register contains settings for the digital interfaces.

Name	0x34	BGW_ WDT		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*	*i2c_wdt_en*	*i2c_wdt_sel*	*reserved*

i2c_wdt_en: Watchdog timer at the SDA pin in TWI mode
0: disable
1: enable

i2c_wdt_sel: Watchdog timer period
0: 1 ms
1: 50 ms

reserved: Write 0

7 Handling and Storage

Sensors with visible damages (housing, connectors, pins, etc.) and sensors which might have exceeded the absolute maximum ratings (e.g. dropped down from a height of more than 1.2 m onto a hard surface) must not be mounted in the vehicle. These sensors must be scrapped.

7.1 Moisture Sensitivity Level (MSL)

The moisture sensitivity level (MSL) of BOSCH SMA130 corresponds to JEDEC Level 1, see also

- IPC/JEDEC J-STD-020C "Joint Industry Standard: Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"
- IPC/JEDEC J-STD-033A "Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitivity Surface Mount Devices"

The sensor IC fulfils the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, i.e. reflow soldering with a peak temperature up to 260°C.

7.2 Mounting Recommendations

MEMS sensors in general are high-precision measurement devices which consist of electronic as well as mechanical structures. BOSCH sensor devices are designed for precision, efficiency and mechanical robustness.

However, in order to achieve best possible results of your design, the following recommendations should be taken into consideration when mounting the sensor on a printed circuit board (PCB).

In order to evaluate and optimize the considered placement position of the sensor on the PCB it is recommended to use additional tools during the design in phase, e.g.:

- Regarding thermal aspects: infrared camera
- Regarding mechanical stress: warpage measurements and/or FEM-simulations
- Regarding shock robustness: drop test of the devices after soldering on the target application PCB

Recommendations in Detail

- It is recommended to keep a reasonable distance between the sensor mounting location on the PCB and the critical points described in the following examples. The exact value for a "reasonable distance" depends on many customer specific variables and must therefore be determined case by case.
- It is not recommended to place the sensor directly under or next to push-button contacts as this can result in mechanical stress.
- It is not recommended to place the sensor in direct vicinity of extremely hot spots regarding temperature (e.g. a µController or a graphic chip) as this can result in heating up the PCB and consequently also the sensor.
- It is not recommended to place the sensor in direct vicinity of a mechanical stress maximum (e.g. in the center of a diagonal crossover). Mechanical stress can lead to bending of the PCB and the sensor.

- Do not mount the sensor too closely to a PCB anchor point where the PCB is attached to a shelf (or similar) as this could also result in mechanical stress. To reduce potential mechanical stress, minimize redundant anchor points and/or loosen respective screws.
- Avoid mounting the sensor in areas where resonant amplitudes (vibrations) of the PCB are likely or to be expected.
- Please avoid partial coverage of the sensor by any kind of (epoxy) resin, as this can possibly result in mechanical stress.
- Avoid mounting (and operation) of the sensor in the vicinity of strong magnetic, strong electric and/or strong infrared radiation fields (IR).
- Avoid electrostatic charging of the sensor and of the device in which the sensor is mounted.

In case you have any questions regarding the mounting of the sensor on your PCB or the evaluation and/or optimization of the considered placement position of the sensor on your PCB, do not hesitate to contact us.

If the above mentioned recommendations cannot be realized appropriately, a specific in-line offset calibration after placement of the device onto your PCB might help to minimize potentially remaining effects.

7.3 Soldering Guidelines

Repair and manual soldering of the sensor is not permitted.

7.3.1 Reflow Soldering Recommendation for Sensors in LGA Package

Please make sure that the edges of the LGA substrate of the sensor are free of solder material. Avoid solder material forming a high meniscus covering the edge of the LGA substrate (see Figure 7-1).

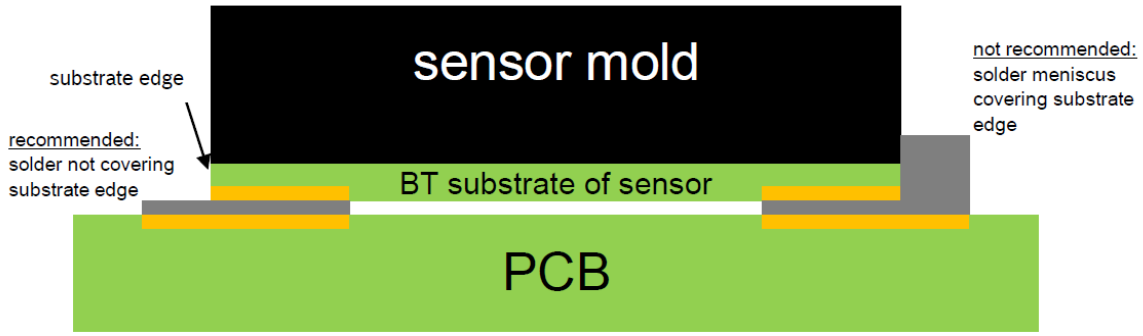


Figure 7-1: Reflow soldering recommendation.

7.3.2 Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Average ramp-up rate (Ts_{max} to Tp)	3 °C/s max.
Preheat - Temperature min (Ts_{min}) - Temperature max (Ts_{max}) - Time (ts_{min} to ts_{max})	 150 °C 200 °C 60 s – 80 s

Time maintained above: - Temperature (T_L) - Time (t_L)	 217 °C 60 s – 150 s
Peak classification temperature (Tp)	260 °C
Time within 5 °C of actual peak	20 s – 40 s
Ramp-down rate	6 °C/s max.
Time 25 °C to peak temperature	8 min max.

Note: All temperatures refer to the topside of the package, measured on the package body surface.

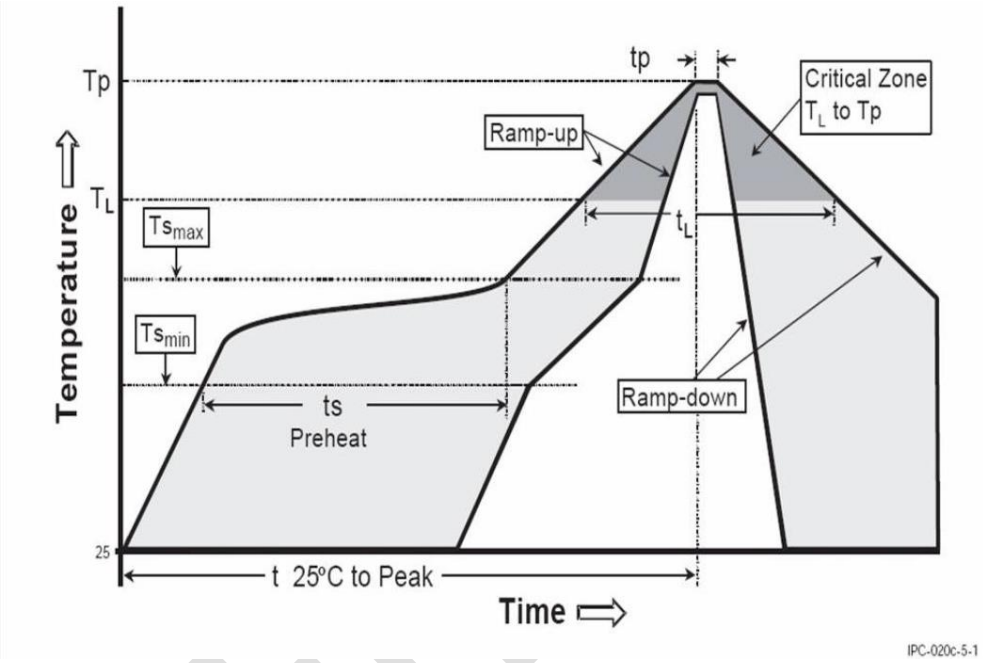


Figure 7-2: Soldering profile.

7.3.3 Multiple Reflow Soldering Cycles

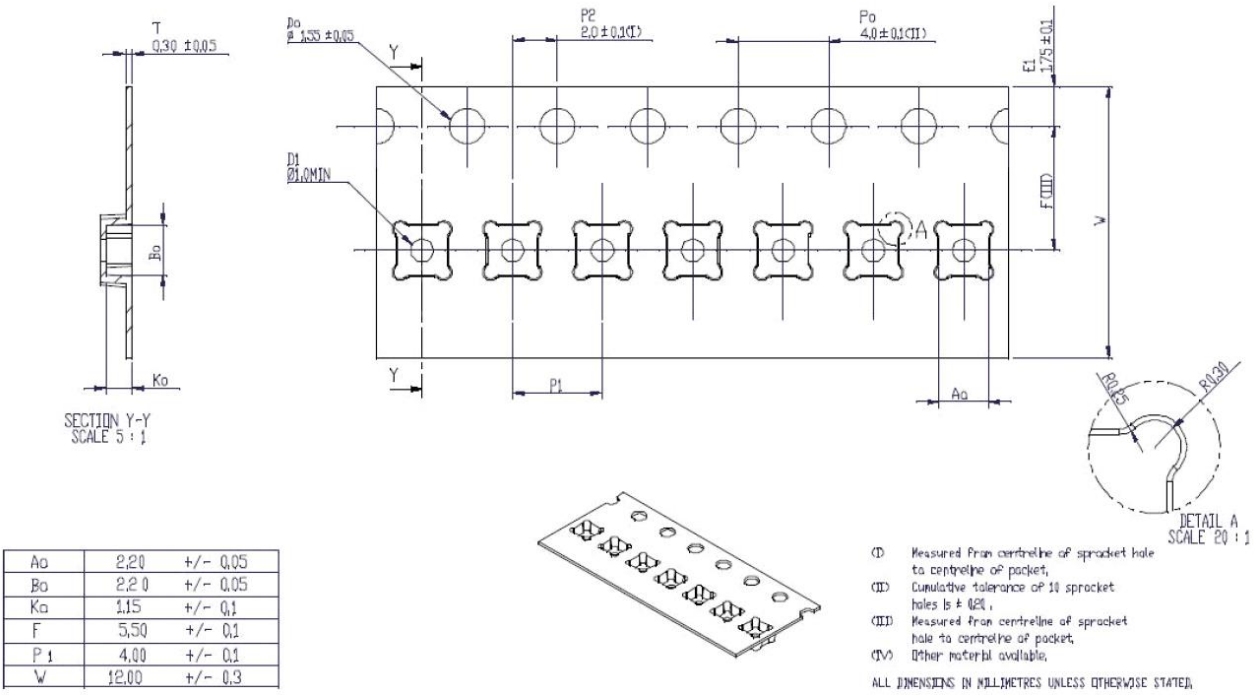
The product can withstand up to 3 reflow soldering cycles in total.

This could be a situation where a PCB is mounted with devices from both sides (i.e., 2 reflow cycles necessary) and where, in the next step, an additional re-work cycle could be required (1 reflow).

7.4 Tape on Reel

7.4.1 Tape on Reel Specification

The SMA130 is shipped in a standard cardboard box.
The box dimensions for one reel are L x W x H = 35 cm x 35 cm x 6 cm.
SMA130 quantity: 10000 pieces per reel. Please handle with care.



Ao	2,20	+/- 0,05
Bo	2,20	+/- 0,05
Ko	1,15	+/- 0,1
F	5,50	+/- 0,1
P 1	4,00	+/- 0,1
W	12,00	+/- 0,3

Figure 7-3: Tape and reel dimensions in mm.

7.4.2 Orientation within the Reel

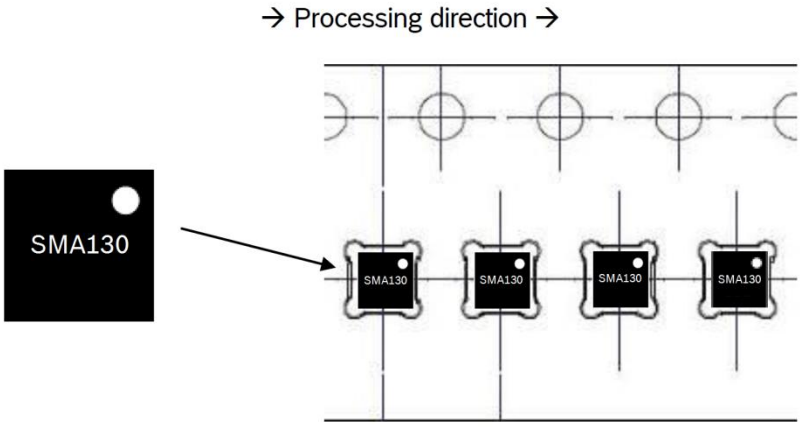


Figure 7-4: Orientation of the SMA130 devices relative to the tape.

7.5 Further Important Mounting and Assembly Recommendations

The SMA130 is designed to sense accelerations with high accuracy even at low amplitudes and contains highly sensitive structures inside the sensor element. The MEMS sensor can tolerate mechanical shocks up to several thousand g's. However, these limits might be exceeded in conditions with extreme shock loads such as e.g. hammer blow on or next to the sensor, dropping the sensor onto hard surfaces etc.

We strongly recommend to avoid any g forces beyond the limits specified in the data sheet during transport, handling and mounting of the sensors in a defined and qualified installation process.

This device has built-in protections against high electrostatic discharges or electric fields (2 kV HBM); however, anti-static precautions should be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be connected to a defined logic voltage level.

8 Test Specifications

8.1 Environmental Safety

The SMA130 sensor meets the requirements of the EC restriction of hazardous substances (RoHS) directive, see also:

Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Halogen content

The SMA130 is halogen-free. For more details on the analysis results, please contact your Bosch representative.

8.2 Qualification

The SMA130 passed the following qualification: TBD.

9 Legal Disclaimer

Assessment of products returned from field

Returned products are considered good if they fulfill the specifications / test data for 0-mileage and field listed in this document.

Engineering Samples

Engineering samples are marked with (e) or (E). Samples may vary from the valid technical specifications of the series product contained in this data sheet. Therefore, they are not intended or fit for resale to third parties or for use in end products. Their sole purpose is internal client testing. The testing of an engineering sample may in no way replace the testing of a series product. Bosch assumes no liability for the use of engineering samples. The purchaser shall indemnify Bosch from all claims arising from the use of engineering samples.

Product Usage

The SMA130 is tested and qualified according to Section 8. The SMA130 only has to be used within the parameters of this product data sheet. In particular, the SMA130 is not fit for use in life-sustaining or safety sensitive systems. Safety sensitive systems are those for which a malfunction may lead to bodily harm or significant property damage. The resale and/or use of products are at the purchaser's own risk and responsibility. The examination of the SMA130 is the sole responsibility of the purchaser.

The purchaser shall indemnify Bosch from all third party claims arising from any product use not covered by the parameters of this product data sheet or not approved by Bosch and reimburse Bosch for all costs in connection with such claims.

The purchaser must monitor the market for the purchased products, particularly with regard to product safety, and inform Bosch without delay of all security relevant incidents.

Application Examples and Hints

With respect to any application examples, advice, normal values, and/or any information regarding the application of the device, Bosch hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights or copyrights of any third party. The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. They are provided for illustrative purposes only and no evaluation regarding infringement of intellectual property rights or copyrights or regarding functionality, performance or error has been made.