AKM   # AK7755

DSP with Mono ADC Stereo CODEC + Mic/Lineout Amp

1. General Description

The AK7755 is a highly integrated digital signal processor, including a mono ADC, a stereo audio CODEC, a MIC pre-amplifier, a line-out amplifier and digital audio I/F. The audio DSP has 2560step at fs = 48kHz parallel processing power. As the AK7755 is a RAM based DSP, it is programmable for user requirements such as high performance hands free function and acoustic effects. The AK7755 is available in a space saving small 36-pin QFN package.

2. Features

☐ **DSP**
- **Word length: 24-bit (Data RAM 24-bit floating point)**
- **Instruction cycle: 8.1ns (2560fs at fs=48kHz)**
- **Multiplier 24 x 24 → 48-bit (double precision available)**
- **Divider 20 / 20 → 20-bit (with floating point normalization function)**
- **ALU: 52-bit arithmetic operation (with overflow margin 4-bit)**
- **Program RAM: 4096 × 36-bit**
- **Coefficient RAM: 2048 × 24-bit**
- **Data RAM: 2048 × 24-bit (24-bit floating point)**
- **Offset Register: 32 × 13-bit**
- **Delay RAM: 8192 × 24-bit**
- **Accelerator Coefficient RAM: 2048 × 20-bit**
- **Accelerator Data RAM: 2048 × 16-bit**
- **JX pins (Interrupt)**
- **Master/Slave Operation**
- **Master Clock: 2560fs**
                (Internally Generated by PLL from 32, 48, 64, 128, 256 and 384fs clock)
☐ **Two Digital Interfaces (I/F1, I/F2)**
- **Digital Signal Input Port (4ch): MSB justified 24-bit, LSB justified 24/20/16-bit, I²S**
- **Digital Signal Output Port (6ch): MSB justified 24-bit, LSB justified 24/20/16-bit, I²S**
- **Short / Long Frame**
- **24-bit linear, 8-bit A-law, 8-bit μ-law**
- **TDM 256fs (8ch) MSB justified and I²S formats**
☐ **Stereo 24-bit ADC:**
- **Sampling Frequency: fs=8kHz ~ 96kHz**
- **ADC Characteristics S/(N+D): 91dB,   DR, S/N: 102dB**
- **Two-Channel Analog Input Selector (Differential, Single-ended Input)**
- **Channel Independent Mic Analog Gain Amplifier**
                (0~18dB (2dB Step), 18~36dB (3dB Step))
- **Analog DRC (Dynamic Range Control)**
- **Channel Independent Digital Volume (24~-103dB, 0.5dB Step Mute)**
- **Digital HPF for DC Offset Cancelling**
☐ **Mono 24-bit ADC**
- **Sampling Frequency: 8kHz ~ 96kHz**
- **ADC Characteristics S/(N+D): 90dB; DR, S/N: 100dB**
- **Line Amplifier: 21dB ~ -21dB, 3dB Step**
- **Digital Volume (24dB ~ -103dB, 0.5dB step, Mute)**
- **Digital HPF for DC Offset Cancelling**

☐ **Stereo 24-bit DAC**
- **Sampling Frequency: fs=8kHz ~ 96kHz**
- **Digital Volume (12dB ~ -115dB, 0.5step, Mute)**
- **Digital De-emphasis Filter (tc=50/15us, fs=32kHz, 44.1kHz, 48kHz)**

☐ **Line Output**
- **Single-ended Output**
- **S/(N+D): 91dB,   DR, S/N: 106dB**
- **Stereo Analog Volume (+0dB ~ -28dB, 2.0dB step, Mute)**

☐ **Analog Mixer**

☐ **Digital Mixer**

☐ **4ch Digital Microphone Interface**

☐ **I^{2}C Bootloader**
- **EEPROM Mat Selectable**

☐ **μP Interface: SPI, I^{2}C-bus (400kHz Fast Mode)**

☐ **Power supply**
> **Analog (AVDD): 3.0V ~ 3.6V (typ. 3.3V)**
> **Digital1 (DVDD): 1.14V ~ 1.3V (typ. 1.2V)**
> > **(External Power Supply or Internal Regulator is selectable)**
> **I/F (TVDD): 1.7V ~ 3.6V (typ. 3.3V)**

☐ **Operating Temperature Range: -40°C ~ 85°C**

☐ **Package: 36-pin QFN (0.5mm pitch)**

3. Table of Contents

4. Block Diagram and Functions

■ Block Diagram
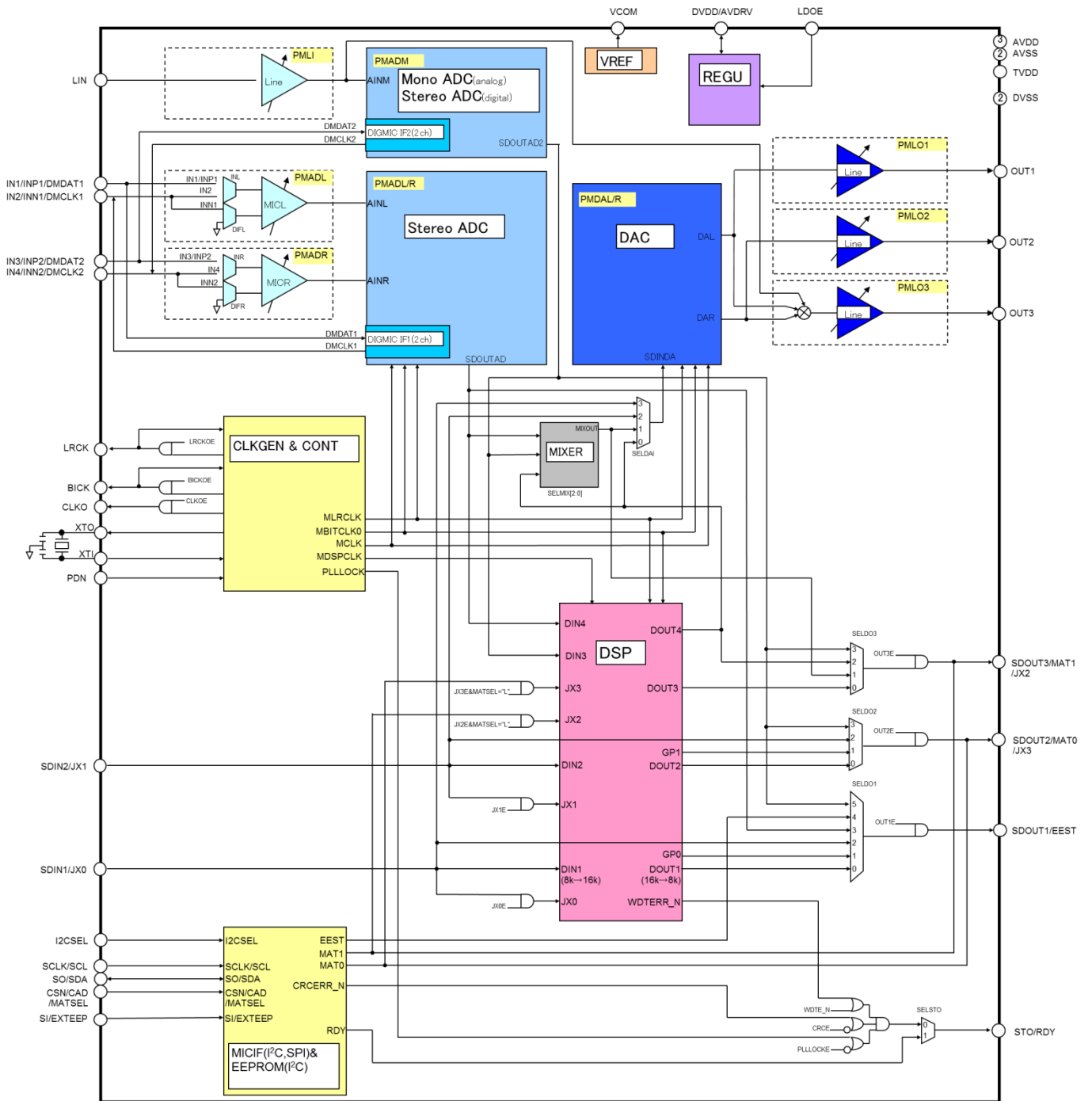
Figure 1. Block Diagram

■ DSP Block Diagram
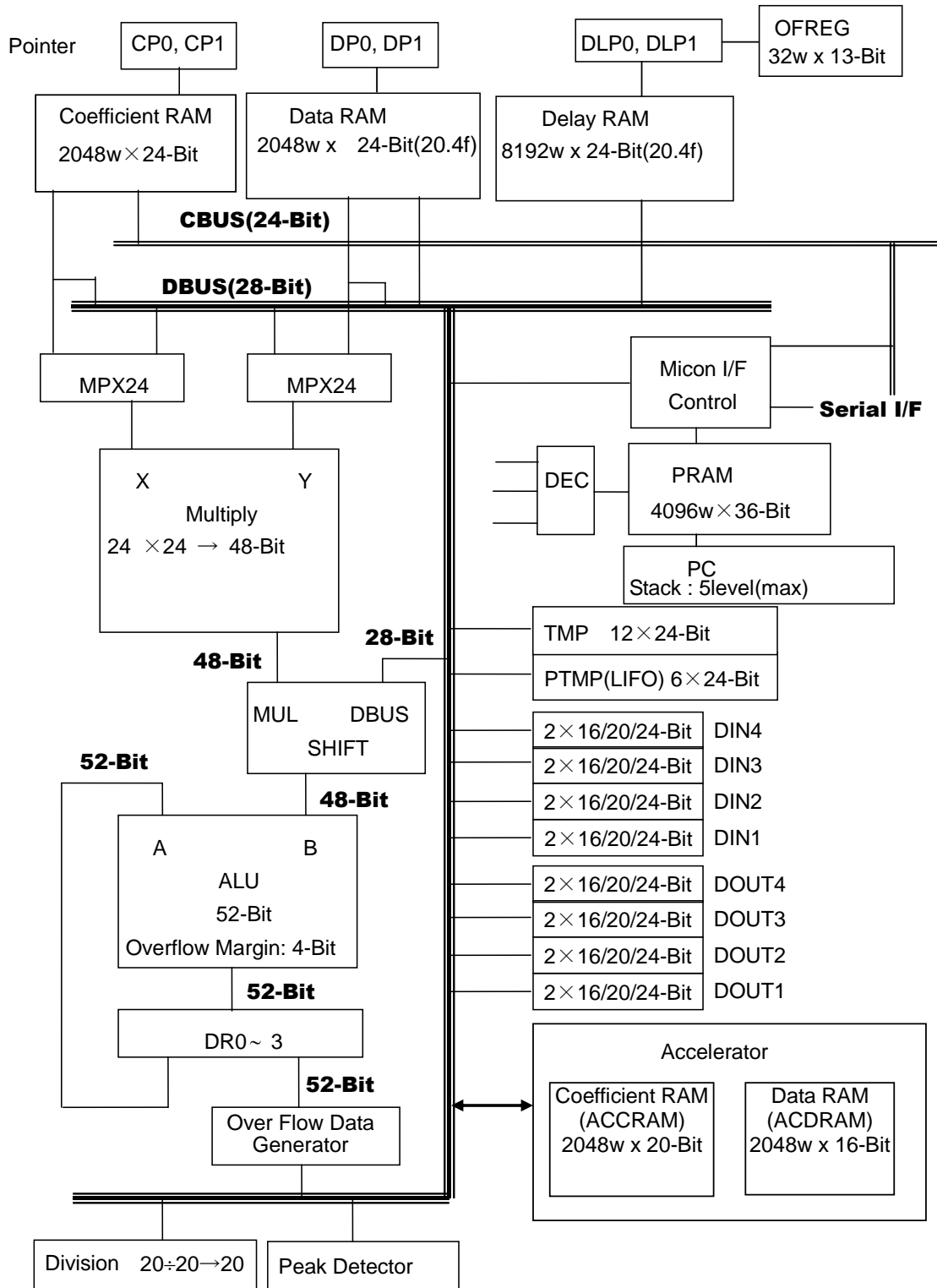
Figure 2. DSP Block Diagram

5. Pin Configurations and Functions

■ **Ordering Guide**

AK7755EN/VN   -40 ~ +85°C   36-pin QFN (0.5mm pitch)
AKD7755   Evaluation Board for AK7755

■ **Pin Layout**

Figure 3. Pin Layout

I2CSEL pin = "L"

PIN	
☐	Input
▨	Output
◪	I/O
⊟	Power

I2CSEL pin = "H", EXTEEP pin = "L"

PIN	
☐	Input
▨	Output
◪	I/O
⊟	Power
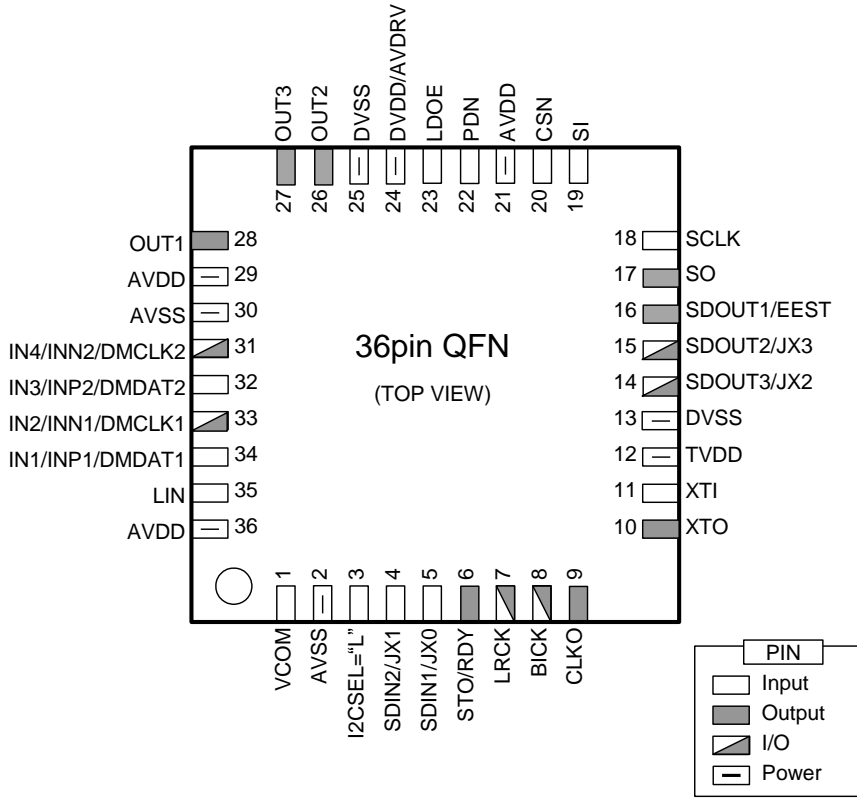
I2CSEL pin = "H", EXTEEP pin = "H", MATSEL pin = "L"

I2CSEL pin = "H", EXTEEP pin = "H", MATSEL pin = "H"

■ Pin Functions

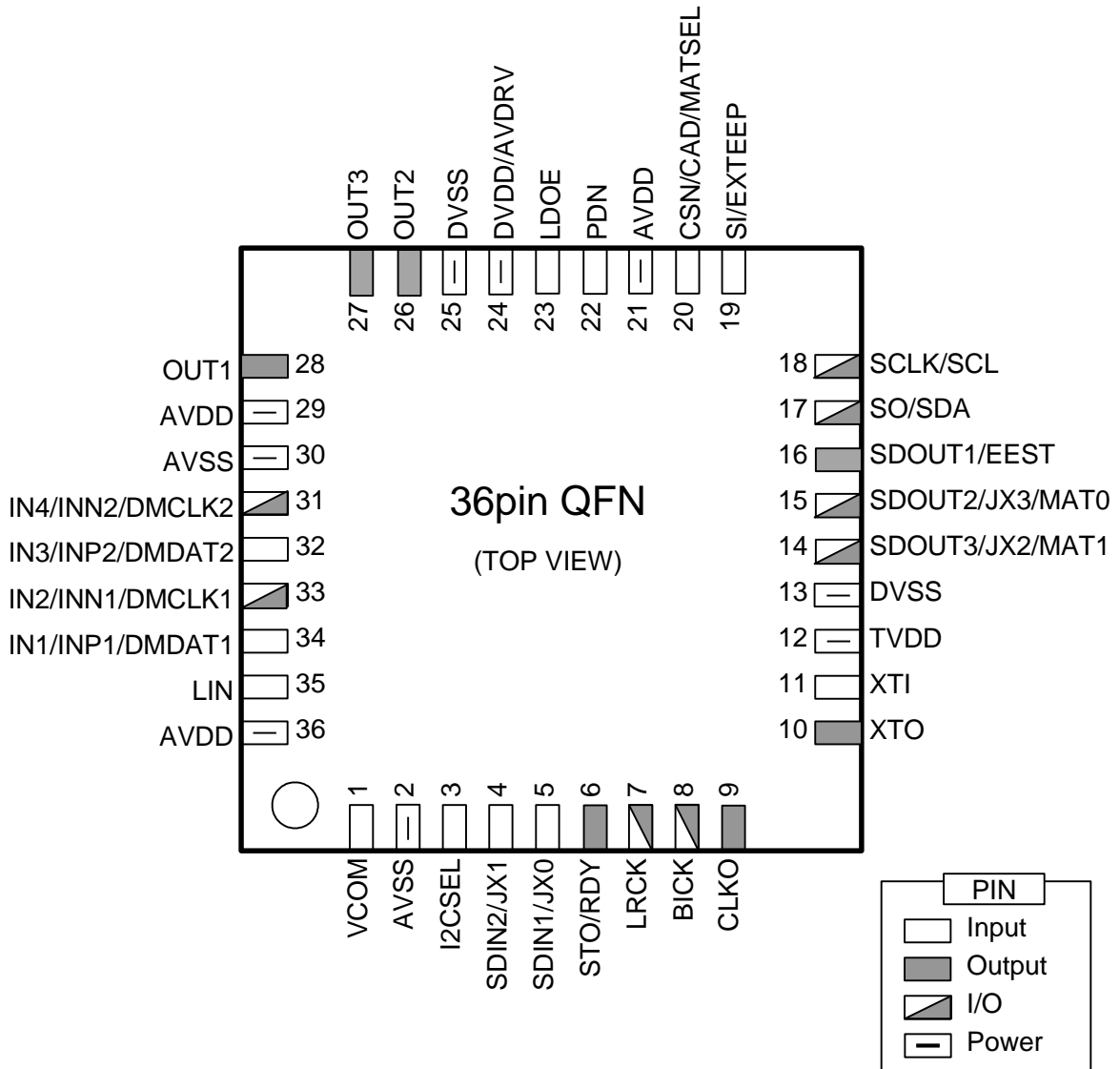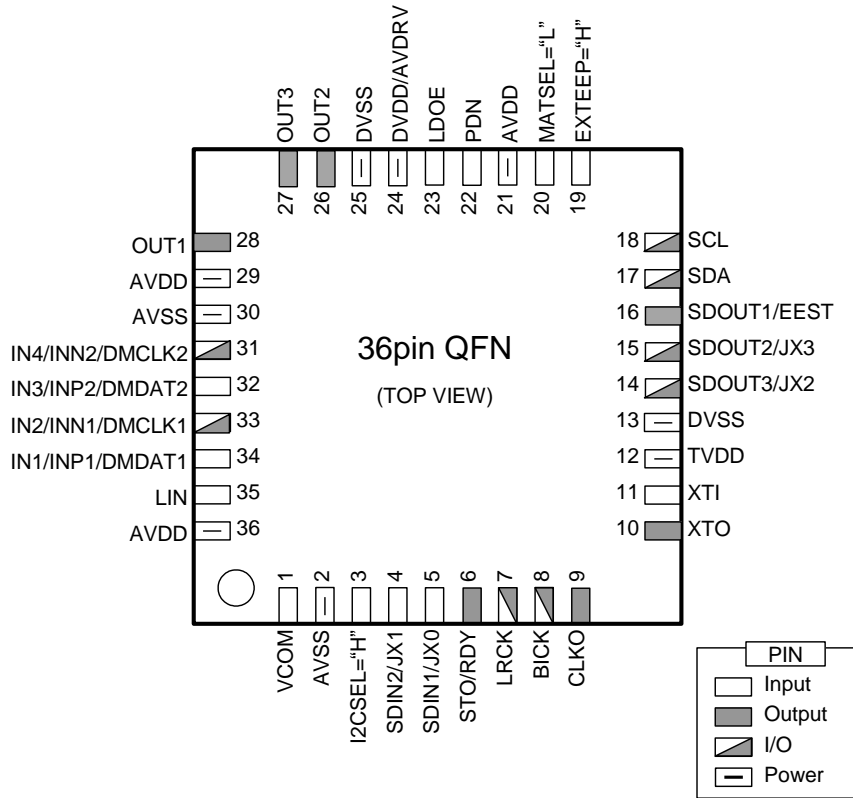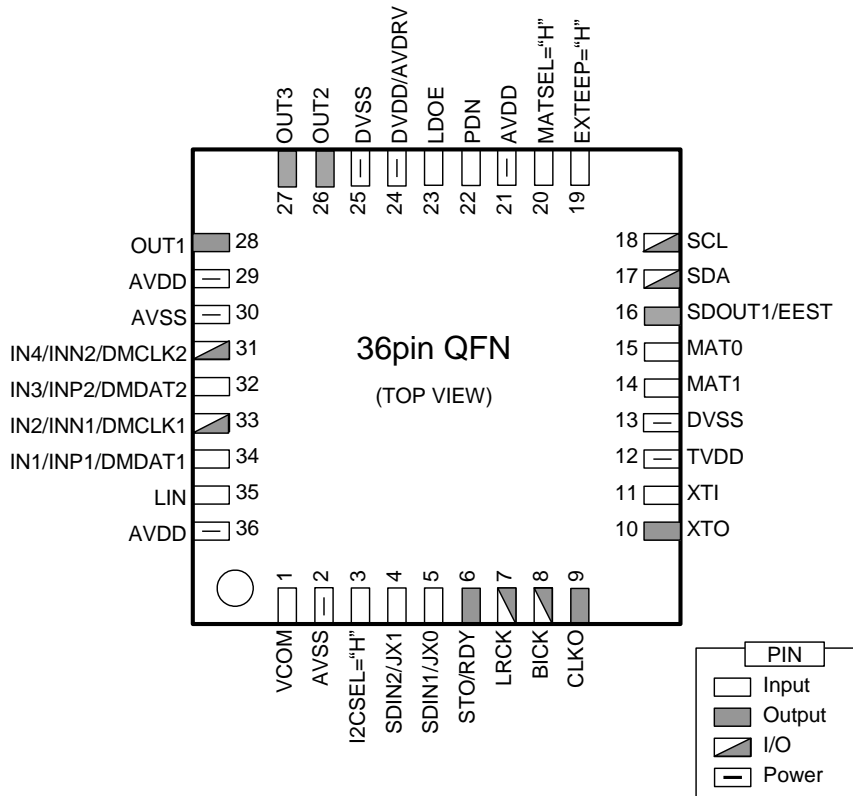| No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin of Analog Block ▪ Connect a 2.2μF capacitor between AVSS. ▪ Do not connect to an external circuit.
2	AVSS	-	Analog Ground Pin 0V
3	I2CSEL	I	I²C-BUS Select Pin ▪ I2CSEL pin = "L": SPI Interface ▪ I2CSEL pin = "H": I²C-bus Interface The I2CSEL pin must be fixed to "L" (DVSS) or "H" (TVDD).
4	SDIN2	I	Serial Data Input2 Pin
	JX1	I	External Conditional Jump1 Pin (JX1E bit = "1")
5	SDIN1	I	Serial Data Input1 Pin
	JX0	I	External Conditional Jump0 Pin (JX0E bit = "1")
6	STO	O	Status Output Pin
	RDY	O	RDY Pin
7	LRCK	I/O	LR Channel Select Pin (Internal pull-down)
8	BICK	I/O	Serial Bit Clock Output Pin (Internal pull-down)
9	CLKO	O	Clock Output Pin
10	XTO	O	Crystal oscillator output pin ▪ When a crystal oscillator is used, connect it between XTI and XTO. ▪ When a crystal oscillator is not used, leave this pin as open.
11	XTI	I	Crystal oscillator input pin ▪ When a crystal oscillator is used, connect it between XTI and XTO. ▪ When a crystal oscillator is not used, connect this pin to the external clock or leave open.
12	TVDD	-	Digital IO Power Supply Pin: 1.7~3.6V (typ. 3.3V)
13	DVSS	I	Ground Pin 0V
14	SDOUT3	O	Serial Data Output3 Pin
	JX2	I	External Conditional Jump2 Pin (JX2E bit = "1")
	MAT1	I	I2CSEL pin = EXTEEP pin = MATSEL pin = "H" EEPROM Download Mat Select Address1
15	SDOUT2	O	Serial Data Output2 Pin
	JX3	I	External Conditional Jump3 Pin (JX3E bit = "1")
	MAT0	I	I2CSEL pin = EXTEEP pin = MATSEL pin = "H" EEPROM Download Mat Select Address0
16	SDOUT1	O	Serial Data Output1 Pin
	EEST	O	EEPROM Interface Status
17	SO	O	SO Pin (I2CSEL pin = "L")
	SDA	I/O	I²CBUS Interface (I2CSEL pin = "H")
18	SCLK	I	Serial Data Clock Pin for SPI Interface (I2CSEL pin = "L") ▪ Set this pin to "H" when there is no clock input.
	SCL	I/O	I²CBUS Interface Pin (I2CSEL pin = "H") EEPROM Download This becomes an output pin when EXTEEP pin = "H".
19	SI	I	Serial Data Input Pin for SPI Interface (I2CSEL pin = "L") ▪ Set this pin to "L" when not used.
	EXTEEP	I	EEPROM Download Control Pin (I2CSEL pin = "H")

20	CSN	I	ChipSelectN Pin for SPI Interface (I2CSEL pin = "L") ▪ Set this pin to "H" when the AK7755 is in power-down mode or when the microprocessor I/F is not used.
	CAD	I	I2CBUS Address Pin (I2CSEL pin = "H")
	MATSEL	I	EEPROM Mat Select Pin (I2CSEL pin = EXTEEP pin = "H")
21	AVDD	-	Analog Power Supply Pin: (typ. 3.3V)
22	PDN	I	Power-down N Pin ▪ The AK7755 can be powered-down by this pin. ▪ Set this pin to "L" upon power-up the AK7755.

23	LDOE	I	LDO Select Pin
			   LDOE pin = "L": 24 pin External 1.2V Power Supply
			   LDOE pin = "H": 24 pin LDO Output (LDO Drive)
			   The LDOE pin must be fixed to "L(DVSS)" or "H(TVDD)".

24	DVDD	I	Power Supply Pin for Digital Core: (typ. 1.2V)
	AVDRV	O	LDO Output (LDOE pin = "H") Connect a 1uF capacitor between this pin and DVSS. This pin must not be connected to an external circuit.
25	DVSS	-	Ground Pin 0V
26	OUT2	O	Line Output 2 Pin
27	OUT3	O	Line Output 3 Pin
28	OUT1	O	Line Output 1 Pin
29	AVDD	-	Analog Power Supply Pin: 3.3V (typ)
30	AVSS	-	Analog Ground Pin 0V
31	IN4/INN2	I	ADC Input Pin (AINE bit = "1")
	DMCLK2	O	Digital MIC Clock Output 2 Pin (DMIC2 bit = "1")
32	IN3/INP2	I	ADC Input Pin (AINE bit = "1")
	DMDAT2	I	Digital MIC Clock Input 2 Pin (DMIC2 bit = "1")
33	IN2/INN1	I	ADC Input Pin (AINE bit = "1")
	DMCLK1	O	Digital MIC Clock Output 1 Pin (DMIC1 bit = "1")
34	IN1/INP1	I	ADC Input Pin (AINE bit = "1")
	DMDAT1	I	Digital MIC Clock Input 1 Pin (DMIC1 bit = "1")
35	LIN	I	Mono ADC Input Pin
36	AVDD	-	Analog Power Supply Pin: 3.3V (typ)

Note 1. All digital input pins must not be allowed to float. If analog input pins are not used, leave them open. The I2CSEL pin, LDOE pin and CAD/MATSEL pin should be fixed to "L" (DVSS) or "H" (TVDD).

■ **Handling of Unused Pin**

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LIN, IN1/INP1/DMDAT1, IN2/INN1/DMCLK1, IN3/INP2/DMDAT2, IN4/INN2/DMCLK2, OUT1, OUT2, OUT3	These pins must be open.
Digital	STO/RDY, CLKO, XTI, XTO, SDOUT3/ JX2/MAT1, SDOUT2/JX3/MAT0, SDOUT1/EEST, SO/SDA, LRCK, BICK	These pins must be open.
	I2CSEL, SDIN2/JX1, SDIN1/JX0, SCLK/SCL, SI/EXTEEP, CSN/CAD/MATSEL, LDOE	These pins must be connected to DVSS.

6. Absolute Maximum Ratings

(AVSS=DVSS=0V; Note 2)

Parameter	Symbol	min	max	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(I/F)	TVDD	-0.3	4.3	V
Digital2(Core)	ΔTVDD	-0.3	1.6	V
DVSS-AVSS (Note 2)	ΔGND	-0.3	0.3	V
Input Current, Any Pin Except Supplies	IIN	−	±10	mA
Analog Input Voltage (Note 3)	VINA	-0.3	(AVDD+0.3)≤4.3	V
Digital Input Voltage (Note 4)	VIND	-0.3	(TVDD+0.3)≤4.3	V
Ambient Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 2. All voltages with respect to ground. AVSS and DVSS must be the same voltage.
Note 3. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
Note 4. The maximum digital input voltage is smaller value between (DVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
         Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS=0V; Note 2)

Parameter	Symbol	min	typ	max	Unit
Power Supplies					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(I/F)	TVDD	1.7	3.3	3.6	V
Digital2(Core)	DVDD	1.14	1.2	1.3	V

Note 5. AVDD and TVDD must be powered up first before DVDD when DVDD is supplied externally
    (LDOE pin = "L"). In this case, the power-up sequence between AVDD and TVDD is not critical.
    When using the internal regulator (LDOE pin = "H"), the power-up sequence between AVDD and
    TVDD is not critical. But all power supplies must be ON before starting operation of the AK7755 by
    PDN pin = "H".
Note 6. Do not turn off the power supply of the AK7755 with the power supply of the surrounding device
    turned on. Pull-up of SDA and SCL pins must not exceed TVDD.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC Amplifier Gain

(Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V)

	Parameter		min	typ	max	Unit
MIC AMP	Input Impedance		14	20		kΩ
	Gain	MGNL[3:0]bits=0h, MGNR[3:0]bits=0h		0		dB
		MGNL[3:0]bits=1h, MGNR[3:0]bits=1h		2		dB
		MGNL[3:0]bits=2h, MGNR[3:0]bits=2h		4		dB
		MGNL[3:0]bits=3h, MGNR[3:0]bits=3h		6		dB
		MGNL[3:0]bits=4h, MGNR[3:0]bits=4h		8		dB
		MGNL[3:0]bits=5h, MGNR[3:0]bits=5h		10		dB
		MGNL[3:0]bits=6h, MGNR[3:0]bits=6h		12		dB
		MGNL[3:0]bits=7h, MGNR[3:0]bits=7h		14		dB
		MGNL[3:0]bits=8h, MGNR[3:0]bits=8h		16		dB
		MGNL[3:0]bits=9h, MGNR[3:0]bits=9h		18		dB
		MGNL[3:0]bits=Ah, MGNR[3:0]bits=Ah		21		dB
		MGNL[3:0]bits=Bh, MGNR[3:0]bits=Bh		24		dB
		MGNL[3:0]bits=Ch, MGNR[3:0]bits=Ch		27		dB
		MGNL[3:0]bits=Dh, MGNR[3:0]bits=Dh		30		dB
		MGNL[3:0]bits=Eh, MGNR[3:0]bits=Eh		33		dB
		MGNL[3:0]bits=Fh, MGNR[3:0]bits=Fh		36		dB

2. Line-in Amplifier Gain

(Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V)

	Parameter		min	typ	max	Unit
Line-in AMP	Input Impedance		14	20		kΩ
	Gain (Note 7)	LIGN[3:0]bits=0h		0		dB
		LIGN[3:0]bits=1h		-3		dB
		LIGN[3:0]bits=2h		-6		dB
		LIGN[3:0]bits=3h		-9		dB
		LIGN[3:0]bits=4h		-12		dB
		LIGN[3:0]bits=5h		-15		dB
		LIGN[3:0]bits=6h		-18		dB
		LIGN[3:0]bits=7h		-21		dB
		LIGN[3:0]bits=8h		N/A		dB
		LIGN[3:0]bits=9h		+3		dB
		LIGN[3:0]bits=Ah		+6		dB
		LIGN[3:0]bits=Bh		+9		dB
		LIGN[3:0]bits=Ch		+12		dB
		LIGN[3:0]bits=Dh		+15		dB
		LIGN[3:0]bits=Eh		+18		dB
		LIGN[3:0]bits=Fh		+21		dB

Note 7. If the output signal of line-in amplifier is input to the analog mixer, +18dB gain is added to the signal at the mixer.

3. MIC Amp + ADC

Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V;
Signal Frequency 1kHz; Sampling Rate fs=48kHz; Measurement Frequency =20Hz to 20kHz
Sampling Rate fs=96kHz; Measurement Frequency =20Hz to 40kHz
CKM mode0(CKM[2:0]= "000"); BITFS[1:0]= "00" (64fs); DSM bit = "0"; Differential Input Mode

	Parameter		min	typ	max	Unit
MIC Amp + ADC	Resolution				24	Bit
	Dynamic Characteristics (Differential Input mode)					
	S/(N+D) (-1dBFS) (Note 14)	Fs=48kHz (Note 12)	80	91		dB
		Fs=48kHz (Note 13)		88		
		Fs=96kHz (Note 12)		89		
		Fs=96kHz (Note 13)		85		
	Dynamic Range (Note 8)	Fs=48kHz (A-weighted) (Note 12)	94	102		dB
		Fs=48kHz (A-weighted) (Note 13)		93		
		Fs=96kHz (Note 12)		95		
		Fs=96kHz (Note 13)		89		
	S/N	Fs=48kHz (A-weighted) (Note 12)	94	102		dB
		Fs=48kHz (A-weighted) (Note 13)		93		
		Fs=96kHz (Note 12)		95		
		Fs=96kHz (Note 13)		89		
	Inter-Channel Isolation (Note 9)		90	105		dB
	DC accuracy (Differential Input)					
	Channel Gain Mismatch			0.0	0.3	dB
	Analog Input					
	Input Voltage (Differential Input) (Note 10)	(Note 12)	±2.00	±2.20	±2.40	Vp-p
		(Note 13)		±0.277		
	Input Voltage (Single-ended Input) (Note 11)	(Note 12)	2.00	2.20	2.40	Vp-p
		(Note 13)		0.277		

Note 8. S/(N+D) when -60dB FS signal is applied.
Note 9. Indicates inter-channel isolation between Lch and Rch when –1dBFS signal is input.
Note 10. INP1/INN1 and INP2/INN2 pins.
Note 11. IN1, IN2, IN3 and IN4 pins.
Note 12. MGNL/R[3:0] bits = 0h (0dB)
Note 13. MGNL/R[3:0] bits = 9h (18dB)
Note 14. When setting DSM bit = "1", S/(N+D) performance of the ADC degrades if an ADC and a DAC are simultaneously operated by the sampling frequency with fs = 8k, 12k, or 24kHz. However, this deterioration does not occur if ADC and DAC are not operated simultaneously. When DSM bit is set to "0" (default), S/(N+D) performance of the ADC is not deterioraded even if the ADC and DAC are operated simultaneously.

4. Line-in Amp + ADC

Ta=25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V;

Signal Frequency 1kHz; Sampling Rate fs=48kHz; Measurement Frequency =20Hz to 20kHz

Sampling Rate fs=96kHz; Measurement Frequency =20Hz to 40kHz

CKM mode0(CKM[2:0]= "000"); BITFS[1:0]= "00" (64fs);

	Parameter		min	typ	max	Unit
Line-in Amp + ADC	Resolution				24	Bit
	Dynamic Characteristics					
	S/(N+D) (-1dBFS)	Fs=48kHz (Note 17)	77	90		dB
		Fs=48kHz (Note 18)		86		
		Fs=96kHz (Note 17)		88		
		Fs=96kHz (Note 18)		85		
	Dynamic Range (Note 15)	Fs=48kHz (A-weighted) (Note 17)	92	100		dB
		Fs=48kHz (A-weighted) (Note 18)		90		
		Fs=96kHz (Note 17)		95		
		Fs=96kHz (Note 18)		86		
	S/N	Fs=48kHz (A-weighted) (Note 17)	92	100		dB
		Fs=48kHz (A-weighted) (Note 18)		90		
		Fs=96kHz (Note 17)		95		
		Fs=96kHz (Note 18)		86		
	Analog Input					
	Input Voltage (Note 16)	(Note 17)	2.00	2.20	2.40	Vp-p
		(Note 18)		0.277		

Note 15. S/(N+D) when -60dB FS signal is applied.

Note 16. The Lin pin.

Note 17. LIGN[3:0] bits = 0h (0dB)

Note 18. LIGN[3:0] bits = Eh (+18 dB)

5. Line-out AMP Gain

Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V

		Parameter	min	typ	max	Unit
Line-out AMP	Gain	LOVOL1[3:0]bits=0h, LOVOL2[3:0]bits=0h, LOVOL3[3:0]bits=0h		mute		dB
		LOVOL1[3:0]bits=1h, LOVOL2[3:0]bits=1h, LOVOL3[3:0]bits=1h		-28		dB
		LOVOL1[3:0]bits=2h, LOVOL2[3:0]bits=2h, LOVOL3[3:0]bits=2h		-26		dB
		LOVOL1[3:0]bits=3h, LOVOL2[3:0]bits=3h, LOVOL3[3:0]bits=3h		-24		dB
		LOVOL1[3:0]bits=4h, LOVOL2[3:0]bits=4h, LOVOL3[3:0]bits=4h		-22		dB
		LOVOL1[3:0]bits=5h, LOVOL2[3:0]bits=5h, LOVOL3[3:0]bits=5h		-20		dB
		LOVOL1[3:0]bits=6h, LOVOL2[3:0]bits=6h, LOVOL3[3:0]bits=6h		-18		dB
		LOVOL1[3:0]bits=7h, LOVOL2[3:0]bits=7h, LOVOL3[3:0]bits=7h		-16		dB
		LOVOL1[3:0]bits=8h, LOVOL2[3:0]bits=8h, LOVOL3[3:0]bits=8h		-14		dB
		LOVOL1[3:0]bits=9h, LOVOL2[3:0]bits=9h, LOVOL3[3:0]bits=9h		-12		dB
		LOVOL1[3:0]bits=Ah, LOVOL2[3:0]bits=Ah, LOVOL3[3:0]bits=Ah		-10		dB
		LOVOL1[3:0]bits=Bh, LOVOL2[3:0]bits=Bh, LOVOL3[3:0]bits=Bh		-8		dB
		LOVOL1[3:0]bits=Ch, LOVOL2[3:0]bits=Ch, LOVOL3[3:0]bits=Ch		-6		dB
		LOVOL1[3:0]bits=Dh, LOVOL2[3:0]bits=Dh, LOVOL3[3:0]bits=Dh		-4		dB
		LOVOL1[3:0]bits=Eh, LOVOL2[3:0]bits=Eh, LOVOL3[3:0]bits=Eh		-2		dB
		LOVOL1[3:0]bits=Fh, LOVOL2[3:0]bits=Fh, LOVOL3[3:0]bits=Fh		0		dB

6. DAC+Line-out Amp

Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V;
Signal Frequency 1kHz; Sampling Rate fs=48kHz; Measurement Frequency =20Hz to 20kHz
Sampling Rate fs=96kHz; Measurement Frequency =20Hz to 40kHz
CKM mode0(CKM[2:0]=000); BITFS[1:0] bits = "00"; LOVOL1/2/3[3:0] bits = Fh(0dB);

	Parameter		min	typ	max	Unit
DAC	Resolution				24	Bit
	Dynamic Characteristics 1 (OUT1, OUT2, OUT3)					
	S/(N+D) (0 dBFS)	fs=48kHz	80	91		dB
		fs=96kHz		89		
	Dynamic Range (Note 19)	fs=48kHz (A-weighted)	100	106		dB
		fs=96kHz		101		
	S/N	fs=48kHz (A-weighted)	100	106		dB
		fs=96kHz		101		
	Inter-Channel Isolation (f=1kHz) (Note 20)		90	110		dB
	DC accuracy					
	Channel Gain Mismatch			0.0	0.5	dB
	Analog Output					
	Output Voltage (Note 21)		2.28	2.51	2.74	Vp-p
	Load Resistance		10			kΩ
	Load Capacitance				30	pF

Note 19. S/(N+D) when -60dB FS signal is applied.
Note 20. Indicates inter-channel isolation between Lch and Rch of DAC when –1dBFS signal is input.
Note 21. Full-scale output voltage. The output voltage is proportional to AVDD (AVDD x 0.76).

■ DC Characteristics

(Ta= -40 to 85°C, AVDD=3.3V, DVDD=1.2V, TVDD=1.7 to 3.6V, AVSS=DVSS=0V)

Parameter	Symbol	min	typ	max	Unit
High Level Input Voltage	VIH	80%TVDD			V
Low Level Input Voltage	VIL			20%TVDD	V
SCL, SDA High Level Input Voltage	VIH	70%TVDD			V
SCL, SDA Low Level Input Voltage	VIL			30%TVDD	V
DMDAT1, DMDAT2 High Level Input Voltage (DMIC1, DMIC2 bit = "1")	VIH2	65%AVDD			V
DMDAT1, DMDAT2 Low Level Input Voltage (DMIC1, DMIC2 bit = "1")	VIL2			35%AVDD	V
High Level Output Voltage Iout= -100μA (Note 22)	VOH	TVDD-0.3			V
Low Level Output Voltage Iout=100μA (Note 23)	VOL			0.3	V
SDA Low Level Output Voltage Iout=3mA — TVDD≥2.0V	VOL			0.4	V
SDA Low Level Output Voltage Iout=3mA — TVDD<2.0V	VOL			20%TVDD	V
DMCLK1, DMCLK2 High Level Output Voltage Iout = -80μA (DMIC1, DMIC2 bit = "1")	VOH2	AVDD-0.4			V
DMCLK1, DMCLK2 Low Level Output Voltage Iout = 80μA (DMIC1, DMIC2 bit = "1")	VOL2			0.4	V
Input Leak Current (Note 24)	Iin			±10	μA
Input Leak Current at Pulled-down Pins (Note 25)	Iid		77		μA
Input Leak Current at XTI pin	Iix		17		μA

Note 22. Except XTO pin
Note 23. Except SDA and XTO pins.
Note 24. Internal Pulled-down pins, except the XTI pin
Note 25. The LRCK, BICK, SDOUT2/JX3/MAT0 and SDOUT3/JX2/MAT1 pins are internal pulled-down pins (typ. 43 kΩ@3.3V).

■ Power Consumptions

(Ta=25°C, AVDD=3.0 to 3.6V (typ=3.3V, max=3.6V), TVDD=1.7 to 3.6V (typ=3.3V, max=3.6V), DVDD=1.14 to 1.3V (typ=1.2V, max=1.3V), AVSS=DVSS=0V)

Parameter	Symbol	min	typ	max	Unit
Power consumptions in operation 1 (Note 26) (LDOE pin = "L")	AVDD		16	24	mA
	TVDD		3	4.5	mA
	DVDD		25	40	mA
Power consumptions in operation 2 (Note 26) (LDOE pin = "H")	AVDD		48	72	mA
	TVDD		3	4.5	mA
Power consumptions in power-down (PDN pin= "L", LDOE pin = "L")	AVDD		10		μA
	TVDD		10		μA
	DVDD		200		μA
Power consumptions in power-down (PDN pin= "L", LDOE pin = "H")	AVDD		1		μA
	TVDD		1		μA

Note 26. DVDD power consumption will be changed depending on DSP programs.
(e.g. It will be 6mA when using AKM's Hands Free program.)

■ **Digital Filter Characteritics**

1. ADC

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, fs=48kHz (Note 27))

Parameter		Symbol	min	typ	max	Unit
Passband (Note 28)	+0.14dB ~ −0.12dB	PB	0		20.7	kHz
	-0.87dB			21.6		kHz
	-3.0dB			22.8		kHz
Stopband		SB	28.4			kHz
Passband Ripple (Note 28)		PR			±0.14	dB
Stopband Ripple (Note 29, Note 30)		SA	65			dB
Group Delay Distortion		ΔGD		0		μs
Group Daley (Ts=1/fs)		GD		12.5		Ts

Note 27. The passband and stopband frequencies scale with "fs" (system sampling rate). The characteristic of the high pass filter is not included.

Note 28. The passband is from DC to 18.9kHz when fs=48kHz.

Note 29. The stopband is 28kHz to 3.044MHz when fs=48kHz.

Note 30. When fs = 48kHz, the analog modulator samples the input signal at 3.072MHz. There is no attenuation of an input signal in band (n x 3.072MHz ±21.99kHz; n=0, 1, 2, 3…) of integer times of the sampling frequency by the digital filter.

2. DAC

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, fs=48kHz)

Parameter		Symbol	min	typ	max	Unit
Passband (Note 31)	(±0.05dB)	PB	0		21.7	kHz
	(-6.0dB)			24		kHz
Stopband (Note 31)		SB	26.2			kHz
Passband Ripple		PR			±0.05	dB
Stopband Attenuation		SA	64			dB
Group Delay (Ts=1/fs) (Note 32)		GD		24		Ts
Digital Filter + Analog Filter						
Amplitude Characteristics 20Hz to 20.0kHz				±0.5		dB

Note 31. The passband and stopband frequencies are proportional to "fs" (system sampling rate), and represents PB=0.4535 × fs(@±0.05dB) and SB=0.5465 × fs, respectively.

Note 32. The digital filter delay is calculated as the time from setting data into the input register until an analog signal is output.

■ Switching Characteristics

1. System Clock

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter		Symbol	min	typ	max	Unit
a) with a Crystal Oscillator:						
CKM[2:0]bits=0h		fXTI		11.2896 12.288		MHz
CKM[2:0]bits=1h		fXTI		16.9344 18.432		MHz
b) with an External Clock						
Duty Cycle			40	50	60	%
CKM[2:0]bits=0h,2h		fXTI	11.0	11.2896 12.288	12.4	MHz
CKM[2:0]bits=1h		fXTI	16.5	16.9344 18.432	18.6	MHz
LRCK Frequency (Note 33)		fs	8	48	96	kHz
BICK Frequency (Note 34)						
TDM256 bit = "0" (Normal Interface)	High Level Width	tBCLKH	64			ns
	Low Level Width	tBCLKL	64			ns
	Frequency	fBCLK	0.23	3.072	6.2	MHz
TDM256 bit = "1" (TDM Interface)	High Level Width	tBCLKH	32			ns
	Low Level Width	tBCLKL	32			ns
	Frequency	fBCLK	1.8	12.288	12.3	MHz

Note 33. LRCK frequency and sampling rate (fs) should be the same.
Note 34. When BICK is the source of the master clock, it should be synchronized to LRCK and have stable frequency.
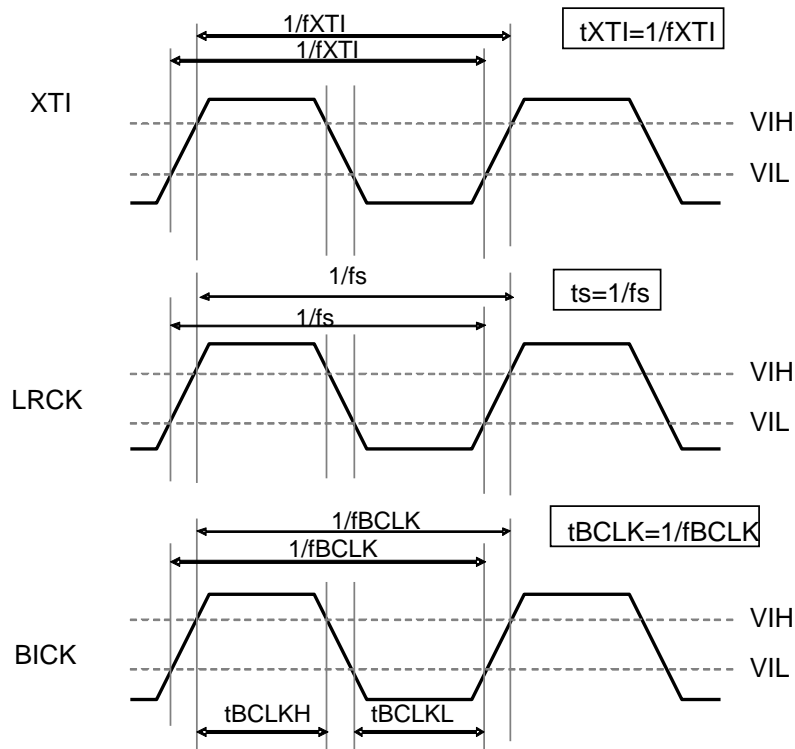

Figure 4. System Clock Timing

2. Power Down

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V)

Parameter	Symbol	min	typ	max	Unit
PDN Pulse Width (Note 35)	tRST	600			ns

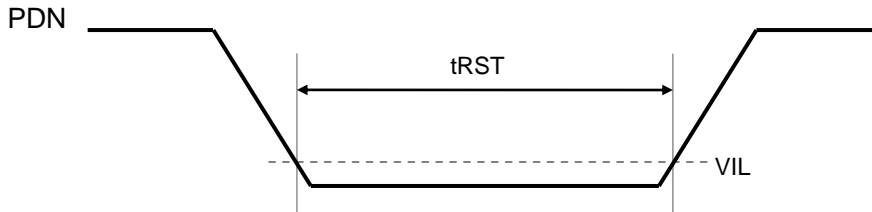Note 35. The PDN pin must be set "L" when power up the AK7755.

Figure 5. Reset Timing

3. Serial Data Interface

SDIN1, SDIN2, SDOUT1, SDOUT2, SDOUT3

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK (Note 36)	tBLRD	20			ns
Delay Time from LRCK to BICK "↑" (Note 36)	tLRBD	20			ns
Serial Data Input Latch Setup Time	tBSIDS	20			ns
Serial Data Input Latch Hold Time	tBSIDH	20			ns
Delay Time from LRCK to Serial Data Output (Note 37)	tLRD			20	ns
Delay Time from BICK "↓" to LRCK Output (Note 38)	tBSOD			20	ns
Master Mode					
BICK Frequency	fBCLK		32, 48 64, 256		fs
BICK Duty Cycle			50		%
Delay Time from BICK "↓" to LRCK (Note 38)	tMBL	-12		12	ns
Serial Data Input Latch Setup Time	tBSIDS	20			ns
Serial Data Input Latch Hold Time	tBSIDH	20			ns
Delay Time from LRCK to Serial Data Output (Note 37)	tLRD			20	ns
Delay Time from BICK "↓" or "↑"to LRCK Output (Note 38)	tBSOD			20	ns
SDINn → SDOUTn (n=1, 2)					
Delay Time from SDINn to SDOUTn Output	tIOD			60	ns

Note 36. BICK edge must not occur at the same time as LRCK edge.
　　　If BICK polarity was inverted, the counting edge of BICK will be "↓".
Note 37. Except I²S.
Note 38. When the polarity of BICK is inverted, delay time is from BICK1 "↑".
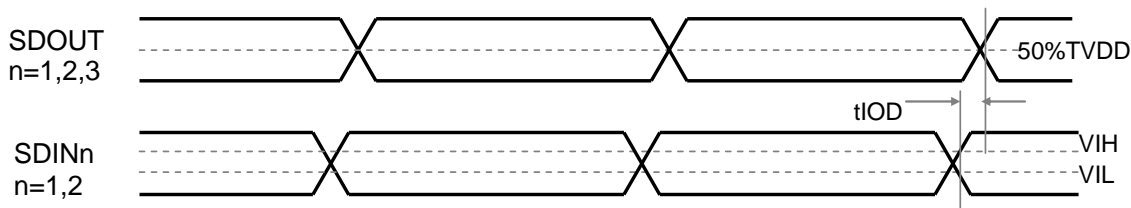

Figure 6. Serial Interface Delay Time from SDINn to SDOUTn Output
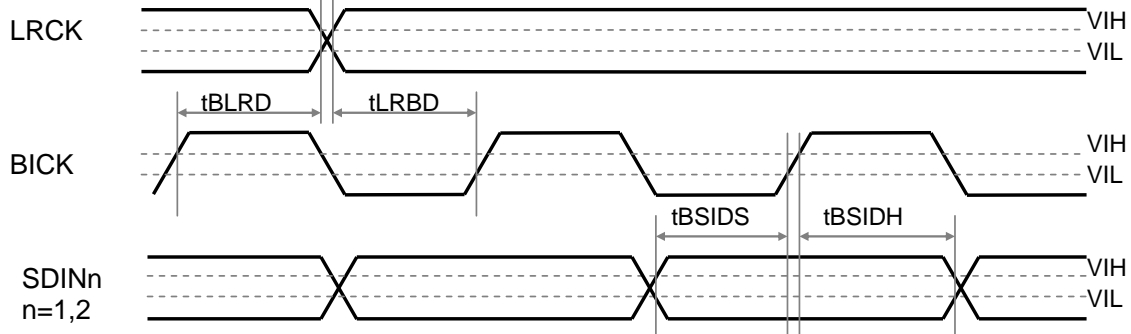
3-1. Slave Mode

Figure 7. Serial Interface Input Timing in Slave Mode
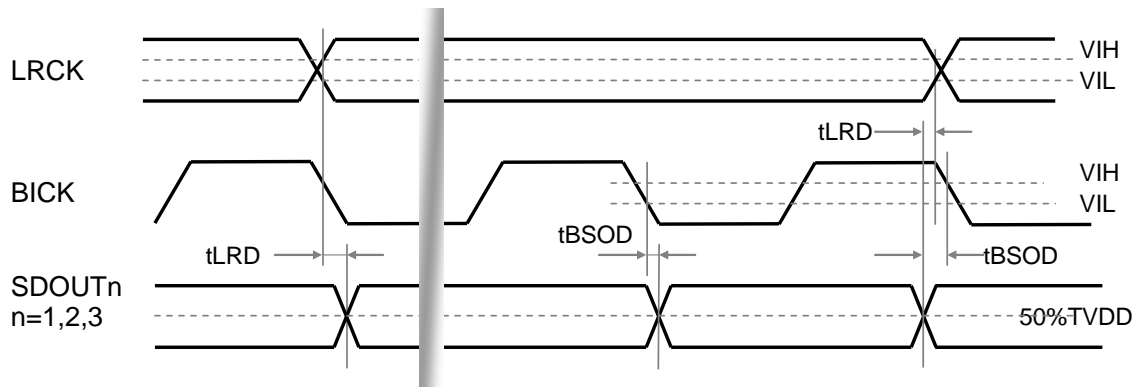

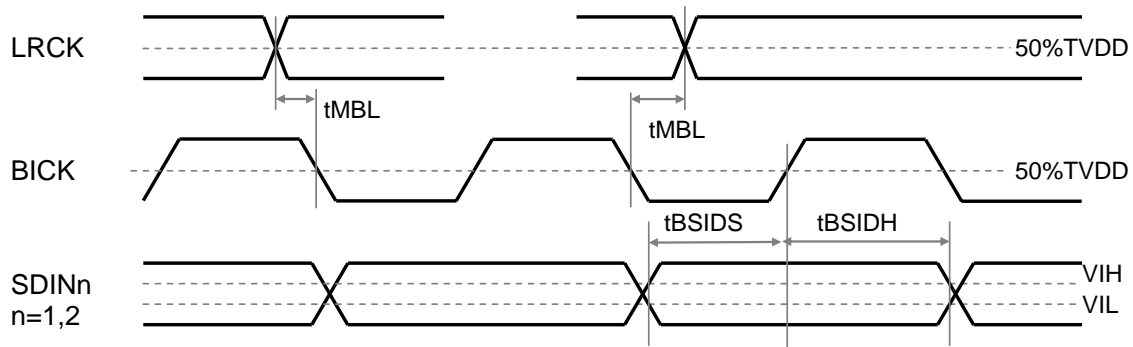Figure 8. Serial Interface Output Timing in Slave Mode

3-2. Master Mode

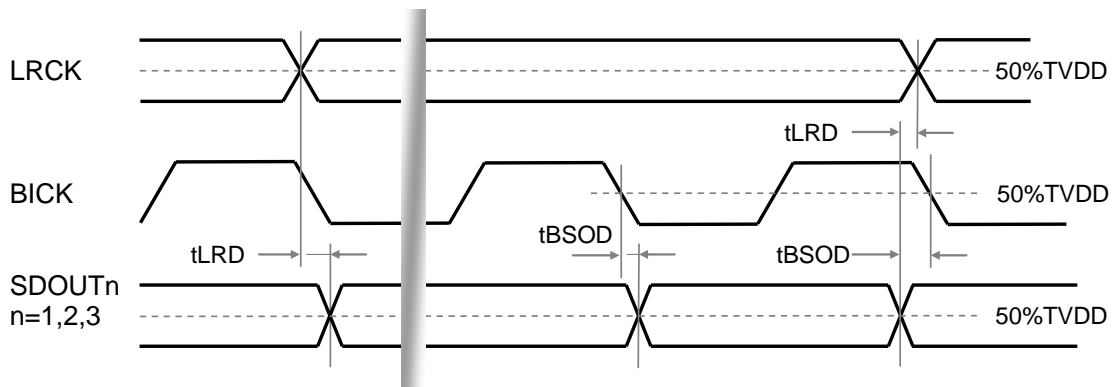Figure 9. Serial Interface Input Timing in Master Mode

Figure 10. Serial Interface Output Timing in Master Mode

4. SPI Interface

4-1. Clock Reset (CKRESETN bit = "0")

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcontroller Interface Signal					
SCLK Frequency	fSCLK			3	MHz
SCLK Low Level Width	tSCLKL	160			ns
SCLK High Level Width	tSCLKH	160			ns
Microcontroller → AK7755					
CSN High Level Width	tWRQH	300			ns
Time from CSN "↑" to PDN "↑"	tRST	360			ns
Time from PDN"↑" to CSN "↓"	tIRRQ	1			ms
Time from RQN"↓" to SCLK"↓"	tWSC	360			ns
Time from SCLK"↑" to CSN"↑"	tSCW	480			ns
SI Latch Setup Time	tSIS	120			ns
SI Latch Hold Time	tSIH	120			ns
AK7755 → Microcontroller					
SO Output Delay Time from SCLK "↓"	tSOS			120	ns
SO Output Hold Time from SCLK "↑" (Note 39)	tSOH	120			ns

Note 39. Except when input the eighth bit of the command code.

4-2. PLL Lock (CKRESETN bit = "1")

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcontroller Interface Signal					
SCLK Frequency	fSCLK			6	MHz
SCLK Low Level Width	tSCLKL	72			ns
SCLK High Level Width	tSCLKH	72			ns
Microcontroller → AK7755					
CSN High Level Width	tWRQH	150			ns
Time from CSN "↑" to PDN "↑"	tRST	180			ns
Time from PDN"↑" to CSN "↓"	tIRRQ	1			ms
Time from RQN"↓" to SCLK"↓"	tWSC	150			ns
Time from SCLK"↑" to CSN"↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	60			ns
SI Latch Hold Time	tSIH	60			ns
AK7755 → Microcontroller					
SO Output Delay Time from SCLK "↓"	tSOS			60	ns
SO Output Hold Time from SCLK "↑" (Note 39)	tSOH	60			ns

Note 40. It takes 10ms at maximum until PLL is locked, after setting CKRESETN bit to "1" from "0".
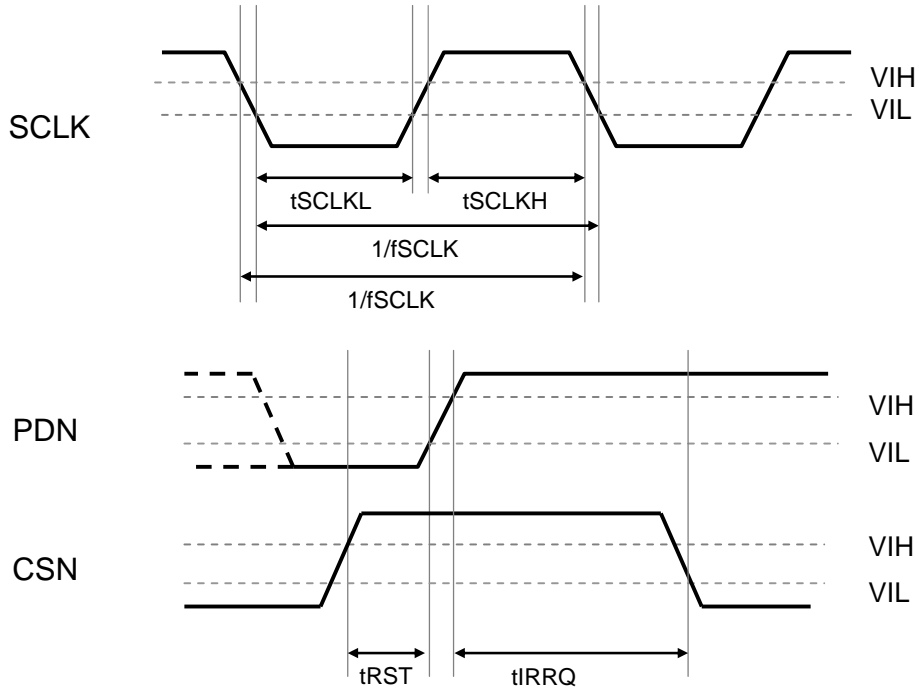
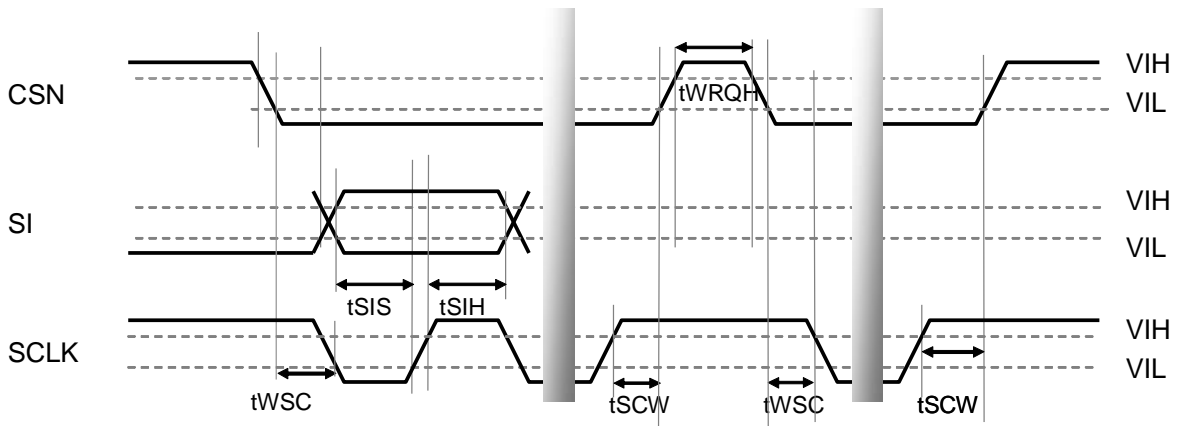Figure 11. SPI Interface Timing 1

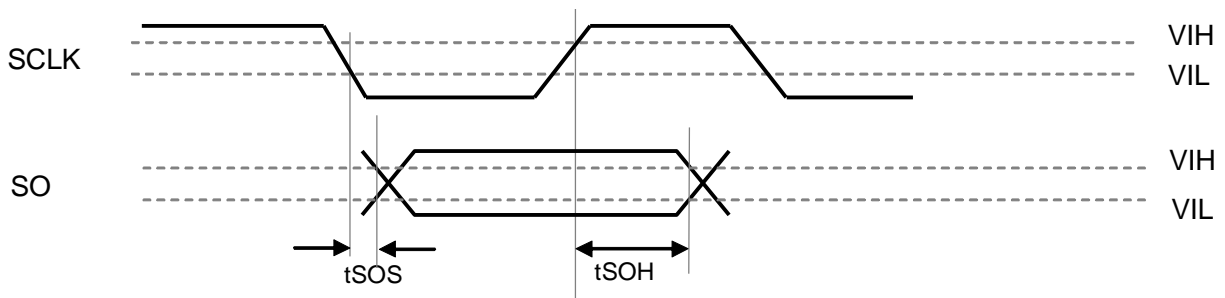Figure 12. SPI Interface Timing 2 (Microcontroller → AK7755)

Figure 13. SPI Interface Timing 3 (AK7755 → Microcontroller)

5. I²C-BUS Interface

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
I2C Timing					
SCL clock frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF
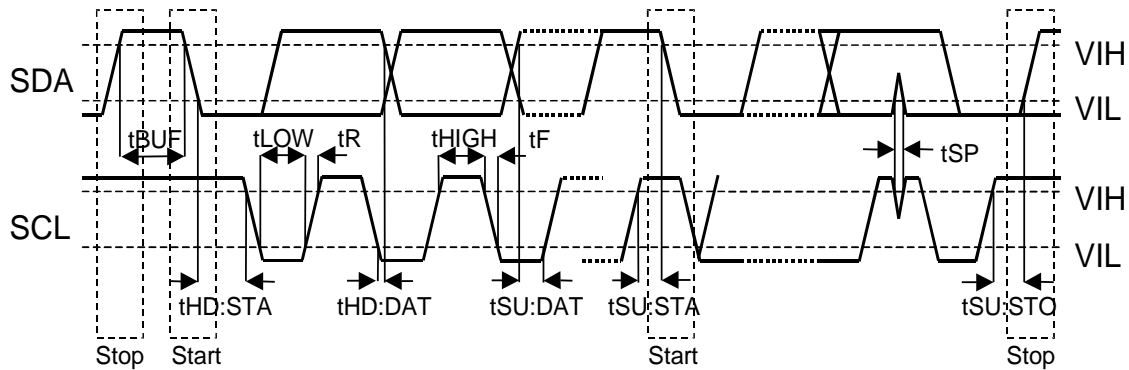
Figure 14. I²C BUS Interface Timing

6. Digital Microphone Interface

(AVDD=3.0~3.6V, TVDD=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V, Ta= -40°C~85°C; CL=100pF)

Parameter	Symbol	min	typ	max	Unit
DMDAT1, DMDAT2					
Serial Data Input Latch Setup Time	tDMDS	50			ns
Serial Data Input Latch Hold Time	tDMDH	0			ns
DMCLK1, DMCLK2					
Clock Frequency (Note 41)	fDMCK	0.5	64fs	6.2	MHz
Duty Cycle	dDMCK	40	50	60	%
Rise Time	tDMCKR			10	ns
Fall Time	tDMCKF			10	ns

Note 41. Clock frequency is determined by the sampling rate (fs) selected by DFS[2:0] bits.

$$fDMCK = 1 / tDMCK$$
$$dDMCK = 100 \times tDMCKL / tDMCK$$

DMCLKP1, DMCLKP2 bit = "1"

DMCLKP1, DMCLKP2 bit = "0"
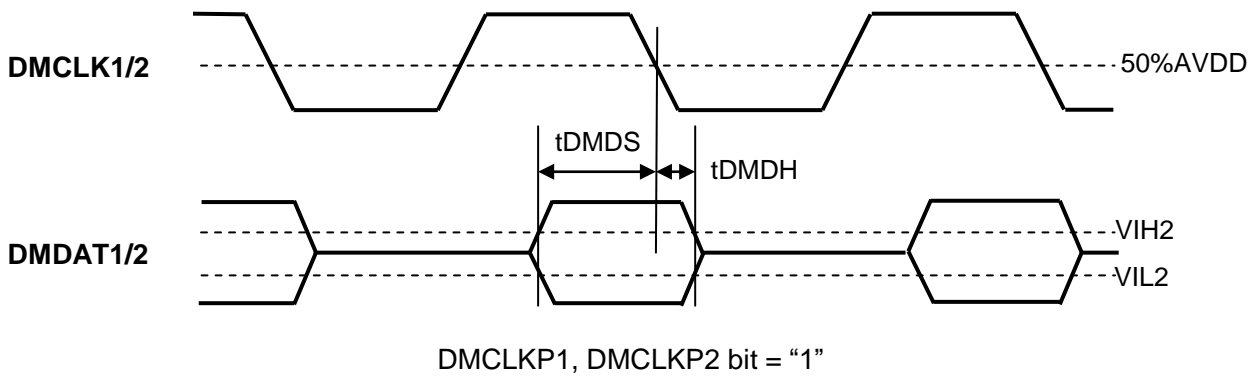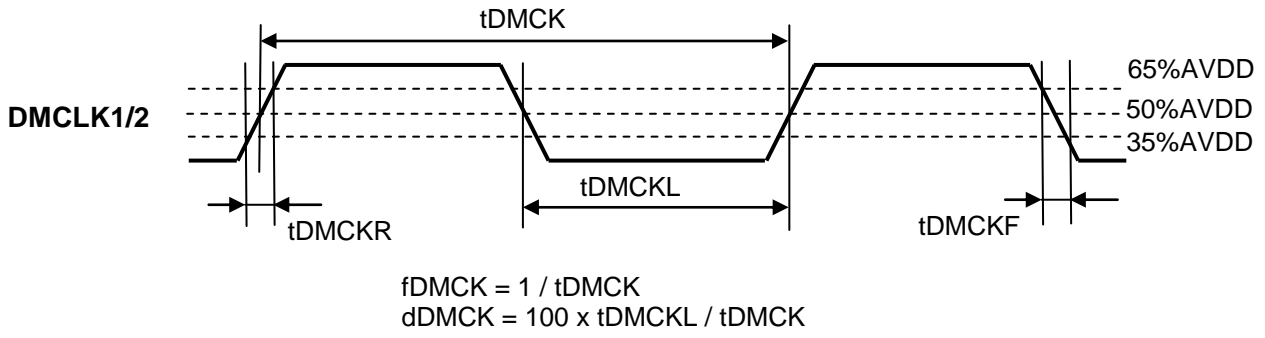
Figure 15. Digital Microphone Interface Timing Wave Form

9. Functional Description

■ System Clock

Master/Slave mode switching, clock source pin select for internal master clock (MCLK) generating clock (ICLK), and ICLK frequency change are controlled by CKM [2:0] clock mode select bits. CKM[2:0] bits can only be set during clock reset.

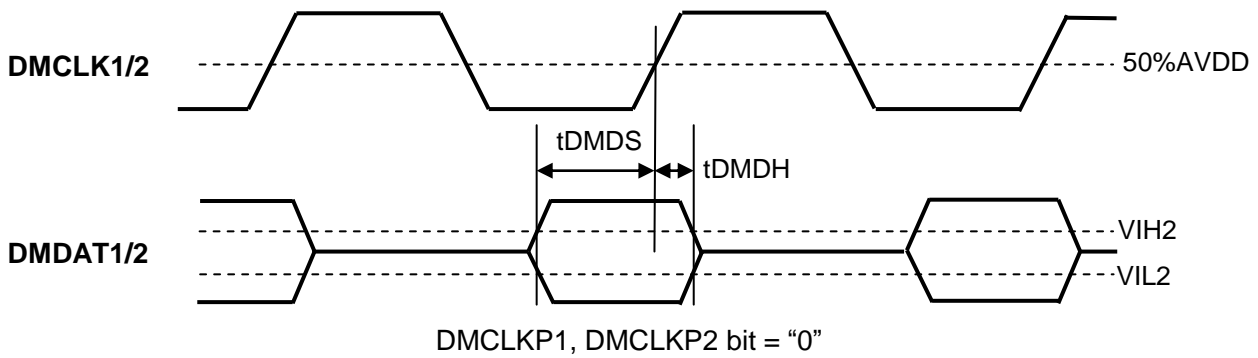| CKM mode	CKM [2:0]	Master Slave	ICLK Source	Sampling Frequency fs (Note 42)	Input pin(s) required for system clock	Use of crystal oscillator
0	000	Master	XTI	DFS[2:0]bits	XTI(12.288MHz)	Available
1	001	Master	XTI	DFS[2:0]bits	XTI(18.432MHz)	Available
2	010	Slave	XTI	DFS[2:0]bits	XTI(12.288MHz), BICK, LRCK	Not Available
3	011	Slave	BICK	DFS[2:0]bits	BICK, LRCK	Not Available
5	101	Slave	BICK	Fs=16kHz Fixed	BICK, LRCK(fs=8kHz)	Not Available

Note 42. The sampling frequency is set by DFS[2:0] bits (CONT00). The BICK frequency is set by BITFS[1:0] bits.

Note 43. In CKM mode 2, XTI, BICK and LRCK must be synchronized but the phase is not critical.

Note 44. CKM mode5 is the mode that operates DSP, ADC and DAC by 16kHz sampling frequency when LRCK sampling frequency is 8kHz. The BICK sampling frequency for LRCK is set by BITFS[1:0] bits.

1. Relationship between MCLK Generating Clock (ICLK) and MCLK
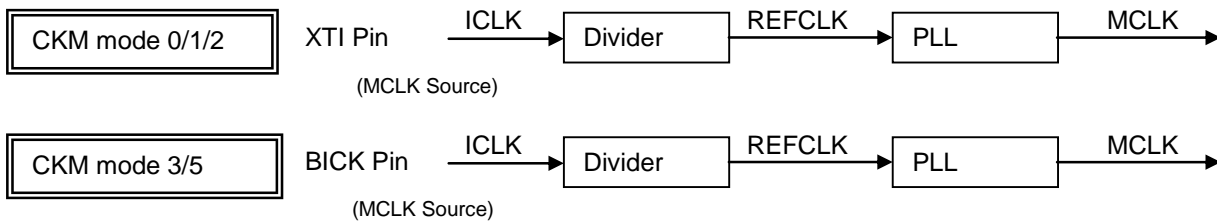
Figure 16. Relation Ship between ICLK and MCLK

2. Sampling Frequency Select

FS mode	DFS[2:0]	fs: Sampling Frequency
0	000	8kHz
1	001	12kHz (11.025kHz)
2	010	16kHz
3	011	24kHz (22.05kHz)
4	100	32kHz
5	101	48kHz (44.1kHz)
6	110	96kHz (88.2kHz)
7	111	N/A

2-1. Master Mode (CKM mode 0, 1: Using XTI Input Clock)

fs: Sampling Frequency

CKM mode	CKM [2:0]	XTI		Input Frequency Range (MHz)	Use of Chrystal Oscillator
		fs:48kHz series	fs:44.1kHz series		
0	000	12.288MHz	11.2896MHz	11.0 to 12.4	Available
1	001	18.432MHz	16.9344MHz	16.7 to 18.6	Available

Input system clock to the XTI pin by setting BITFS[1:0] bits. The internal counter which is synchronized to XTI generates LRCK(1fs) and BICK(64fs, 48fs, 32fs, 256fs). BICK frequency can be selected by BITFS[1:0] bits. The BICK output will be in two different frequencies if setting BITFS[1:0] bits = 1h (48kHz) when the sampling frequency is 12kHz, 24kHz, 48kHz or 96kHz (DFS[2:0]). LRCK and BICK are not output during system reset.
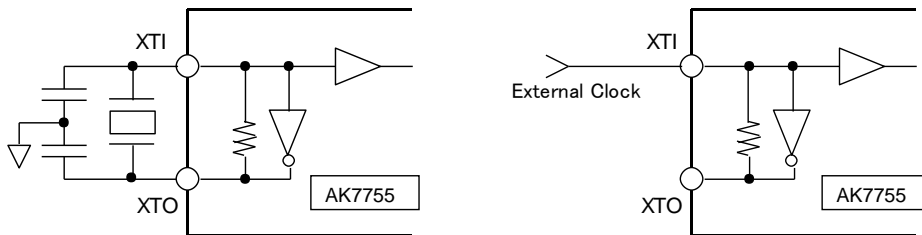
Figure 17. Using Crystal Oscillator (CKM mode 0/1)   Using External Clock (CKM mode 0/1)

2-2. Slave Mode1 (CKM mode 2: XTI Input Clock)

fs: sampling frequency

CKM mode	CKM [2:0]	XTI		Input Frequency Range (MHz)	Use of Chrystal Oscillator
		fs:48kHz	fs:44.1kHz		
2	010	12.288MHz	11.2896MHz	11.0 to 12.4	Not Available

Required System Clocks are XTI, LRCK and BICK. XTI and LRCK must be synchronized, but the phase between these clocks is not important. The system sampling rate is controlled by DFS[2:0] bits. The sampling frequency of BICK is set by BITFS[1:0] bits.

2-3. Slave Mode 2 (CKM mode 3: BICK Input Clock)

In CKM mode 3, required system clocks are BICK and LRCK. In this mode, BICK is used for clock source instead of XTI. This clock is multiplied directly by a PLL to generate the master clock (MCLK). Therefore BICK with two different frequencies cannot be used. BICK and LRCK must be synchronized. Set BICK frequency for LRCK by BITFS[1:0] bits. The sampling rate is determined by DFS[2:0] bits setting. In applications which do not need the XTI pin of the AK7755, leave this pin open.

2-4. Slave Mode 3 (CKM mode 5: BICK Input Clock)

CKM mode5 is the mode that operates DSP, ADC and DAC by 16kHz sampling frequency when LRCK sampling frequency is 8kHz. Set BICK frequency against LRCK by BITFS[1:0] bits. Each sampling frequency is fixed (LRCK = 8kHz, DSP/ADC/DAC = 16kHz).
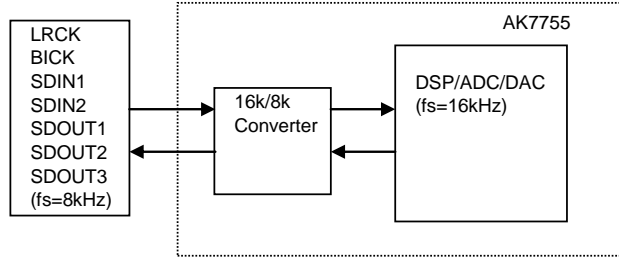
Figure 18. Slave Mode3 (CKM mode5) Sampling Frequency Setting

fs: Sampling Frequency

DFS [2:0]	fs	BITFS [1:0]	BICK	BICK Frequency	
				44.1kHz series	48kHz series
0h	8kHz	0h	64fs	470.4kHz	512kHz
0h	8kHz	1h	48fs	352.8kHz	384kHz
0h	8kHz	2h	32fs	235.2kHz	256kHz
0h	8kHz	3h	256fs	1881.6kHz	2048kHz
1h	12kHz	0h	64fs	705.6kHz	768kHz
1h	12kHz	1h	48fs	N/A	N/A
1h	12kHz	2h	32fs	352.8kHz	384kHz
1h	12kHz	3h	256fs	2822.4kHz	3072kHz
2h	16kHz	0h	64fs	940.8kHz	1024kHz
2h	16kHz	1h	48fs	705.6kHz	768kHz
2h	16kHz	2h	32fs	470.4kHz	512kHz
2h	16kHz	3h	256fs	3763.2kHz	4096kHz
3h	24kHz	0h	64fs	1.4112MHz	1.536MHz
3h	24kHz	1h	48fs	1058.4MHz	1.152MHz
3h	24kHz	2h	32fs	705.6kHz	768kHz
3h	24kHz	3h	256fs	5.6448MHz	6.144MHz
4h	32kHz	0h	64fs	1.8816MHz	2.048MHz
4h	32kHz	1h	48fs	1.4112MHz	1.536MHz
4h	32kHz	2h	32fs	0.9408MHz	1.024MHz
4h	32kHz	3h	256fs	7.5264MHz	8.192MHz
5h	48kHz	0h	64fs	2.8224MHz	3.072MHz
5h	48kHz	1h	48fs	2.1168MHz	2.304MHz
5h	48kHz	2h	32fs	1.4112MHz	1.536MHz
5h	48kHz	3h	256fs	11.2896MHz	12.288MHz
6h	96kHz	0h	64fs	5.6448MHz	6.144MHz
6h	96kHz	1h	48fs	4.2336MHz	4.608MHz
6h	96kHz	2h	32fs	2.8224MHz	3.072MHz
6h	96kHz	3h	256fs	22.5792MHz	24.576MHz
7h	N/A	—	—	—	—

(N/A: Not available)

Table 1. Clock Select

BITFS[1:0] bits = 0h @(LRIF[1:0] bits = 0h)

Figure 19. BITFS[1:0] bits = 0h(64fs) (LRIF[1:0]bits = 0h)

BITFS[1:0] bits = 1h @(LRIF[1:0] bits = 0h)

Figure 20. BITFS[1:0] bit s= 1h(48fs) (LRIF[1:0]bits = 0h)

BITFS[1:0] bits = 2h @(LRIF[1:0] bits = 0h)

Figure 21. BITFS[1:0] bits = 2h(32fs) (LRIF[1:0]bits = 0h)

Refer to Figure 40 and Figure 42 when BITFS[1:0] bits = 3h (256fs).

■ Control Register Settings

Control registers are reset by a power down release (PDN pin = "L" → "H"). Since control registers CONT00-CONT01 are related to clock generation, they must be changed during clock reset (CKRESETN bit (CONT01: D0) = "0"). CONT12-CONT19 can be written during operation. The other con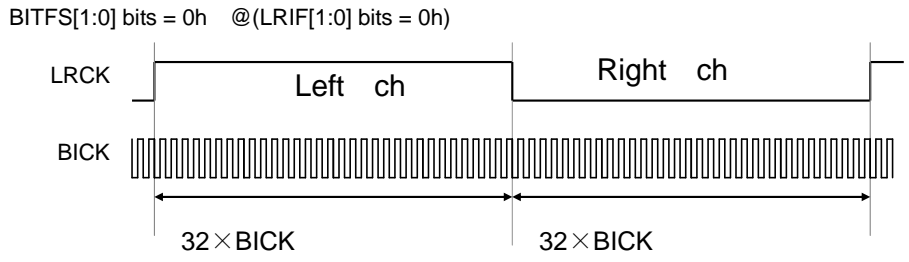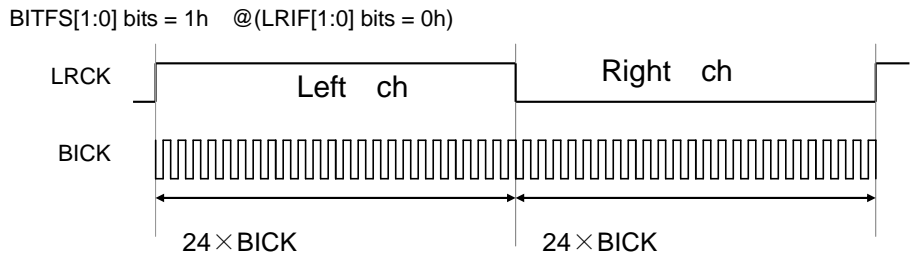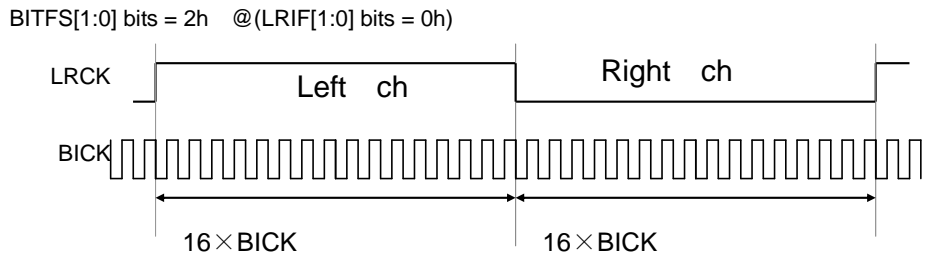trol registers must be changed during clock reset or system reset (CRESETN bit (CONT0F: D3) and DSPRESETN bit (CONT0F: D2) = "0") to avoid errors and noises.

CONT0D: D6, CONT1A: D4, CONT26: D0 and CONT2A: D7 bits must be set to "1" during system reset. Once these bits are set to "1", the value will be kept until power down the AK7755 (PDN pin = "L"). Do not write to the CONT1F-CONT25, CONT27-CONT29 and CONT2B-CONT3F registers.

CONT00-CONT1E, CONT26, CONT2A

Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
CONT00	0	CKM[2]	CKM[1]	CKM[0]	AINE	DFS[2]	DFS[1]	DFS[0]	00h
CONT01	JX2E	LRDOWN	BITFS[1]	BITFS[0]	CLKS[2]	CLKS[1]	CLKS[0]	CKRESETN	00h
CONT02	TDM256	BCKP	LRIF[1]	LRIF[0]	TDMMODE[1]	TDMMODE[0]	JX1E	JX0E	00h
CONT03	DIF2[1]	DIF2[0]	DOF2[1]	DOF2[0]	BANK[3]	BANK[2]	BANK[1]	BANK[0]	00h
CONT04	DRMS[1]	DRMS[0]	DRAM[1]	DRAM[0]	POMODE	0	WAVP[1]	WAVP[0]	00h
CONT05	ACCRAM CLRN	JX3E	FIRMODE1	FIRMODE2	SUBMODE1	SUBMODE2	MEMDIV[1]	MEMDIV[0]	00h
CONT06	DEM[1]	DEM[0]	DIFDA[1]	DIFDA[0]	0	DIF1[2]	DIF1[1]	DIF1[0]	00h
CONT07	DOF4[1]	DOF4[0]	DOF3[1]	DOF3[0]	0	DOF1[2]	DOF1[1]	DOF1[0]	00h
CONT08	SELDAI[1]	SELDAI[0]	SELDO3[1]	SELDO3[0]	SELDO2[1]	SELDO2[0]	SELMIX[1]	SELMIX[0]	00h
CONT09	DIFR	INR	DIFL	INL	LO3SW3	LO3SW2	LO3SW1	SELMIX[2]	00h
CONT0A	CLKOE	BICKE	LRCKE	0	0	OUT3E	OUT2E	OUT1E	00h
CONT0B	0	0	0	0	0	0	0	0	00h
CONT0C	DSM	0	ATSPAD	ATSPDA	0	SELDO1[2]	SELDO1[1]	SELDO1[0]	00h
CONT0D	STO	1	0	0	0	0	0	DLS	80h
CONT0E	PMADR	PMADL	PMAD2L	PMLO3	PMLO2	PMLO1	PMDAR	PMDAL	00h
CONT0F	0	0	PML1	LRDETN	CRESETN	DSPRESETN	PMAD2R	DLRDY	00h
CONT10	WDTEN	CRCE	PLLLOCKE	SOCFG	SELSTO	0	0	CKADJEN	00h
CONT11	CKADJ[7]	CKADJ[6]	CKADJ[5]	CKADJ[4]	CKADJ[3]	CKADJ[2]	CKADJ[1]	CKADJ[0]	00h
CONT12	MGNR[3]	MGNR[2]	MGNR[1]	MGNR[0]	MGNL[3]	MGNL[2]	MGNL[1]	MGNL[0]	00h
CONT13	LIGN[3]	LIGN[2]	LIGN[1]	LIGN[0]	LOVOL3[3]	LOVOL3[2]	LOVOL3[1]	LOVOL3[0]	00h
CONT14	LOVOL2[3]	LOVOL2[2]	LOVOL2[1]	LOVOL2[0]	LOVOL1[3]	LOVOL1[2]	LOVOL1[1]	LOVOL1[0]	00h
CONT15	VOLADL[7]	VOLADL[6]	VOLADL[5]	VOLADL[4]	VOLADL[3]	VOLADL[2]	VOLADL[1]	VOLADL[0]	30h
CONT16	VOLADR[7]	VOLADR[6]	VOLADR[5]	VOLADR[4]	VOLADR[3]	VOLADR[2]	VOLADR[1]	VOLADR[0]	30h
CONT17	VOLAD2L[7]	VOLAD2L[6]	VOLAD2L[5]	VOLAD2L[4]	VOLAD2L[3]	VOLAD2L[2]	VOLAD2L[1]	VOLAD2L[0]	30h
CONT18	VOLDAL[7]	VOLDAL[6]	VOLDAL[5]	VOLDAL[4]	VOLDAL[3]	VOLDAL[2]	VOLDAL[1]	VOLDAL[0]	18h
CONT19	VOLDAR[7]	VOLDAR[6]	VOLDAR[5]	VOLDAR[4]	VOLDAR[3]	VOLDAR[2]	VOLDAR[1]	VOLDAR[0]	18h
CONT1A	ADMUTE	AD2MUTE	DAMUTE	1	ADRCRE	ADRCLE	MICRZCE	MICLZCE	00h
CONT1B	AMGNR[3]	AMGNR[2]	AMGNR[1]	AMGNR[0]	AMGNL[3]	AMGNL[2]	AMGNL[1]	AMGNL[0]	00h
CONT1C	0	0	0	0	0	0	0	0	00h
CONT1D	VOLAD2R[7]	VOLAD2R[6]	VOLAD2R[5]	VOLAD2R[4]	VOLAD2R[3]	VOLAD2R[2]	VOLAD2R[1]	VOLAD2R[0]	30h
CONT1E	DMIC1	DMCLKP1	DMCLKE1	DMIC2	DMCLKP2	DMCLKE2	0	0	00h
CONT26	0	0	0	0	0	0	0	1	00h
CONT2A	1	0	0	0	0	0	0	0	00h

CONT00: Clock Setting 1, Analog Input Setting

Write during clock reset.

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C0h	40h	CONT00	0	CKM[2]	CKM[1]	CKM[0]	AINE	DFS[2]	DFS[1]	DFS[0]	00h

D6, D5, D4: CKM[2:0]   Clock Mode Setting

CKM mode	CKM [2:0]	Master Slave	Main Clock	fs	System Clock	
----------	-----------	--------------	------------	----	--------------	
0	000	Master	XTI=12.288MHz fixed	fs=8~96kHz	XTI	(default)
1	001	Master	XTI=18.432MHz fixed	fs=8~96kHz	XTI	
2	010	Slave	XTI=12.288MHz fixed	fs=8~96kHz	XTI, BICK, LRCK	
3	011	Slave	BICK	fs=8~96kHz	BICK, LRCK	
5	101	Slave	BICK	fs=16kHz	BICK, LRCK(fs=8kHz)	

TDM256 bit (CONT02: D7) = "1" cannot be used in CKM mode5.

D3: AINE Analog Input Setting (IN1/INP1, IN2/INN1, IN3/INP2, IN4/INN2 pin)
       0: Not Using Analog Input (default)
       1: Using Analog Input

   Set AINE bit to "1" first before other control register settings when using the IN1/INP1, IN2/INN1,
   IN3/INP2 and IN4/INN2 pins as analog inputs. The AK7755 starts charging to a capacitor connected to
   each pin by this setting.
   Set AINE bit to "0" when using digital microphones (DMIC1 or DMIC2 bit (CONT1E: D7, D4) = "1").

D2, D1, D0: DFS[2:0]   Sampling Frequency

DFS mode	DFS[2:0]	fs	
0	000	8kHz	(default)
1	001	12kHz	
2	010	16kHz	
3	011	24kHz	
4	100	32kHz	
5	101	48kHz	
6	110	96kHz	
7	111	N/A	

Multiply 44.1/48 to calculate the values for multiple sampling frequencies of 44.1kHz.

Write "0" into the "0" registers.

CONT01: Clock Setting 2 and JX2 Setting

Write during clock reset.

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C1h	41h	CONT01	JX2E	LRDOWN	BITFS[1]	BITFS[0]	CLKS[2]	CLKS[1]	CLKS[0]	CKRESETN	00h

D7: JX2E External Conditional Jump 2 Enable
    0: JX2 is Disabled (default), No. 14-pin output (SDOUT3) when OUT3E bit (CONT0A:D2) = "1"
    1: JX2 is Enabled, No. 14-pin Input

D6: LRDOWN   LRCK Sampling Frequency Select
    0: LRCK   Sampling frequency set by DFS[2:0] bits (CONT00: D2-D0). (default)
    1: LRCK   Half frequency of the setting value by DFS[2:0] bits
        The AK7755 can output LRCK which is half frequency of the setting value by DFS[2:0] bits in
        master mode (CKM mode 0, 1(CONT00: D6-D4)). This mode is used when
        LRCK/BICK/SDIN1/SDOUT1 is driven by fs= 8kHz while the AK7755 is driven by fs= 16kHz in
        master mode. LRDOWN bit = "1" cannot be set when TDM256 bit (CONT02: D7) = "1".

D5, D4: BITFS[1:0]   BICK fs Select

BITFS mode	BITFS [1:0]	BICK	Note	
0	00	64fs	512kHz(@fs=8kHz),3.072MHz(@fs=48kHz)	(default)
1	01	48fs	384kHz(@fs=8kHz),2.304MHz(@fs=48kHz)	
2	10	32fs	256kHz(@fs=8kHz),1.536MHz(@fs=48kHz)	
3	11	256fs	2.048MHz(@fs=8kHz),12.288MHz(@fs=48kHz)	

    This setting is valid in both slave and master modes.
    Set the BICK input sampling frequency against LRCK, in Slave mode (CKM2, 3 and 5).
    Set the BICK output sampling frequency against LRCK in Master mode (CKM0 and 1).
    The BICK output will be in two different frequencies if setting BITFS[1:0] bits = 1h (48kHz) when
    the sampling frequency is 12kHz, 24kHz, 48kHz or 96kHz (DFS[2:0]).

D3, D2, D1: CLKS[2:0]   CLKO Output Clock Select

CLKS mode	CLKS[2:0]	fs=48kHz	fs=44.1kHz	
0	000	12.288MHz	11.2896MHz	(default)
1	001	6.144MHz	5.6448MHz	
2	010	3.072MHz	2.8224MHz	
3	011	8.192MHz	7.5264MHz	
4	100	4.096MHz	3.7632MHz	
5	101	2.048MHz	1.8816MHz	
6	110	256fs	256fs	
7	111	XTI or BICK	XTI or BICK	

D0: CKRESETN Clock Reset
    0: Clock Reset (default)
    1: Clock Reset Release

CONT02: Serial Data Format, JX1, 0 Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C2h	42h	CONT02	TDM256	BCKP	LRIF[1]	LRIF[0]	TDM MODE[1]	TDM MODE[0]	JX1E	JX0E	00h

D7: TDM256, TDM Select
　　0: Normal Interface (default)
　　1: TDM Interface
　　　BICK is fixed to 256fs. Set BITFS[1:0] bits = 3h (CONT01: D5, D4). Format is selected by
　　　LRIF[1:0] bits setting (CONT02: D5, D4). In this mode, CKM mode 5(CONT00: D6-D4) is not
　　　available. TDM256 bit cannot be set to "1" when LRDOWN bit (CONT00: D6) = "1". In TDM
　　　mode, a 96kHz sampling frequency is not available. DFS[2:0] bits (CONT00: D2-D0) setting must
　　　be lower than 5h (48kHz).

D6: BCKP　　BICK Edge Select

BCKP bit	BICK edge referenced to LRCK edge	
0	falling (FE)	(default)
1	rising (RE)	

D5, D4: LRIF[1:0]　　LRCK I/F Format

Mode	LRIF[1:0]bit	Digital I/F Format	
0	00	Standard (MSB justified/ LSB justified)	(default)
1	01	I²S Compatible	
2	10	PCM Short Frame	
3	11	PCM Long Frame	

In standard format mode, MSB justified and 24/20/16 bit LSB justified formats are selectable by DIF1
bits (CONT06: D2-D0), DIF2 bits (CONT03: D7, D6), DIFDA bits (CONT06: D5, D4), DOF1 bits
(CONT07: D2-D0), DOF2 bits (CONT03: D5, D4), DOF3 bits (CONT07: D5, D4), and DOF4 bits
(CONT07: D7, D6). In other modes, MSB justified format should be selected by DIF1-2 bits, DAF bit
and DOF1-4 bits.

D3, D2: TDMMODE[1:0] DSPDIN3, DSPDIN4 Input Source Select (Valid when TDM256bit = "1")

Mode	TDMMODE [1:0]	DSPDIN4 Lch	DSPDIN4 Rch	DSPDIN3 Lch	DSPDIN3 Rch	
0	00	SDIN1 SLOT7	SDIN1 SLOT8	SDIN1 SLOT5	SDIN1 SLOT6	(default)
1	01	SDOUTAD Lch	SDOUTAD Rch	SDIN1 SLOT5	SDIN1 SLOT6	
2	10	SDOUTAD Lch	SDOUTAD Rch	SDOUTAD2 Lch	SDOUTAD2 Rch	
3	11	N/A	N/A	N/A	N/A	

D1: JX1E　　External Conditional Jump1 Enable
　　0: JX1 is invalid (default)
　　1: JX1 is valid

D0: JX0E　　External Conditional jump0 Enable
　　0: JX0 is invalid (default)
　　1: JX0 is valid

CONT03: Delay RAM, DSP Input / Output Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C3h	43h	CONT03	DIF2[1]	DIF2[0]	DOF2[1]	DOF2[0]	BANK[3]	BANK[2]	BANK[1]	BANK[0]	00h

D7, D6: DIF2[1:0] DSP DIN2 Input Format Select

DIF2 Mode	DIF2[1:0]	Input Data Format	
0	00	MSB (24-bit)	(default)
1	01	LSB 24-bit	
2	10	LSB 20-bit	
3	11	LSB 16-bit	

Set "00" for I^{2}S compatible, PCM Short and PCM Long formats.
Set "11" when BITFS[1:0] bits (CONT01: D5, D4) = 2h (32fs).

D5, D4: DOF2[1:0] DSP DOUT2 Output Format Select

DOF2 Mode	DOF2[1:0]	Output Data Format	
0	00	MSB (24-bit)	(default)
1	01	LSB 24-bit	
2	10	LSB 20-bit	
3	11	LSB 16-bit	

Set "00" for I^{2}S compatible, PCM Short and PCM Long formats.
Set "11" when BITFS[1:0] bits = 2h (32fs).

D3, D2, D1, D0: BANK[3:0]   DLRAM mode Setting

DLRAM Partition mode	BANK [3:0]	Delay RAM		
		Bank1	Bank0	
		Linear 20.4f	Ring 20.4f	
0	0000	0	8192 words	(default)
1	0001	1024 words	7168 words	
2	0010	2048 words	6144 words	
3	0011	3072 words	5120 words	
4	0100	4096 words	4096 words	
5	0101	5120 words	3072 words	
6	0110	6144 words	2048 words	
7	0111	7168 words	1024 words	
8	1000	8192 words	0	
9-15	1001 1111		N/A	

CONT04: Data RAM, CRAM Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C4h	44h	CONT04	DRMS[1]	DRMS[0]	DRAM[1]	DRAM[0]	POMODE	0	WAVP[1]	WAVP[0]	00h

D7, D6: DRMS[1:0]   Data RAM Size Setting

DRAM mode	DRMS [1:0]	DSP Data RAM	
		Bank1	Bank0
		Memory size[words]	Memory size[words]
0	00	512	1536	(default)
1	01	1024	1024
2	10	1536	512
3	11	N/A	

D5, D4: DRAM[1:0]   Data RAM Addressing mode Setting

Addressing mode	DRAM [1:0]	DSP Data RAM	
		Bank1 DP1	Bnak0 DP0
0	00	Ring	Ring	(default)
1	01	Ring	Linear
2	10	Linear	Ring
3	11	Linear	Linear

D3: POMODE   DLRAM Pointer 0 Select
   0: DBUS Immediate (default)
   1: OFREG

D1, D0: WAVP[1:0]   CRAM Memory Assignment

WAVP mode	WAVP[1:0]		FFT Point Number	
0	00	33word	128	(default)
1	01	65word	256
2	10	129word	512
3	11	257word	1024

Write "0" into the "0" registers.

CONT05: Accelerator Setting, JX3 Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C5h	45h	CONT05	ACCRAM CLRN	JX3E	FIR MODE1	FIR MODE2	SUB MODE1	SUB MODE2	MEM DIV[1]	MEM DIV[0]	00h

D7: ACCRAMCLRN   Accelerator CRAM Clear Setting
    0: Accelerator CRAM is cleared by 0 data after releasing reset. (default)
    1: Accelerator CRAM is not cleared after releasing reset.

D6: JX3E External Conditional Jump3 Enable
    0: JX3 Disable (default), No. 15 pin output (SDOUT2) when OUT2E bit (CONT0A:D1) = "1"
    1: JX3 Enable, No. 15 pin Input

D5: FIRMODE1   Accelerator Ch1 Operation Select
    0: Adaptive Filter (default)
    1: FIR Filter

D4: FIRMODE2   Accelerator Ch2 Operation Select
    0: Adaptive Filter (default)
    1: FIR Filter

D3: SUBMODE1   Accelerator Ch1 Mode Select
    0: Fullband (default)
    1: Subband

D2: SUBMODE2   Accelerator Ch2 Mode Select
    0: Fullband (default)
    1: Subband

D1, D0: MEMDIV[1:0]   Accelerator Memory Select

MODE	MEMDIV[1:0]	ch1	ch2	
0	00	2048	-	(default)
1	01	1792	256	
2	10	1536	512	
3	11	1024	1024	

Write "0" into the "0" registers.

CONT06: DAC De-emphasis, DAC and DSP Input Format Settings

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C6h	46h	CONT06	DEM[1]	DEM[0]	DIFDA[1]	DIFDA[0]	0	DIF1[2]	DIF1[1]	DIF1[0]	00h

D7, D6: DEM[1:0]   DAC De-emphasis Setting (50/15μs)

DEM mode	DEM[1:0]	Sampling Frequency fs	
0	00	OFF	(default)
1	01	48kHz	
2	10	44.1kHz	
3	11	32kHz	

D5, D4: DIFDA[1:0]   DAC Input Format Select

DIFDA mode	DIFDA[1:0]	Input Data Format	
0	00	MSB justified (24-bit)	(default)
1	01	LSB justified 24-bit	
2	10	LSB justified 20-bit	
3	11	LSB justified 16-bit	

Set "00" for I²S Compatible, PCM Short and PCM Long formats.
Set "11" when BITFS[1:0] bits (CONT01: D5, D4) =2h (32fs).
Set "00" when connecting MIXOUT or DSP-DOUT4 to DAC input.

D2, D1, D0: DIF1[2:0] DSP DIN1 Input Format Select

DIF1 Mode	DIF1[2:0]	Input Data Format	
0	000	MSB (24-bit)	(default)
1	001	LSB 24-bit	
2	010	LSB 20-bit	
3	011	LSB 16-bit	
4	100	MSB 8-bit μ-Law	
5	101	MSB 8-bit A-Law	
6	110	N/A	
7	111	N/A	

Set "000" for I²S Compatible, PCM Short and PCM Long formats.
Set "011" when BITFS[1:0]=2h (32fs).

Write "0" into the "0" registers.

CONT07: DSP Output Format Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C7h	47h	CONT07	DOF4[1]	DOF4[0]	DOF3[1]	DOF3[0]	0	DOF1[2]	DOF1[1]	DOF1[0]	00h

D7, D6: DOF4[1:0]   DSP DOUT4 Output Format Select

DOF4 mode	DOF4[1:0]	Output Data Format	
0	00	MSB justified (24-bit)	(default)
1	01	LSB justified 24-bit	
2	10	LSB justified 20-bit	
3	11	LSB justified 16-bit	

Set "00" for I^{2}S Compatible, PCM Short and PCM Long formats.
Set "11" when BITFS[1:0] bits (CONT01: D5, D4) =2h (32fs).
Set "00" when connecting to the DAC.

D5, D4: DOF3[1:0]   DSP DOUT3 Output Format Select

DOF3 mode	DOF3[1:0]	Output Data Format	
0	00	MSB justified (24-bit)	(default)
1	01	LSB justified 24-bit	
2	10	LSB justified 20-bit	
3	11	LSB justified 16-bit	

Set "00" for I^{2}S Compatible, PCM Short and PCM Long formats.
Set "11" when BITFS[1:0] bits=2h (32fs).

D2, D1, D0: DOF1[2:0] DSP DOUT1 Output Format Select

DOF1 mode	DOF1[2:0]	Output Data Format	
0	000	MSB (24-bit)	(default)
1	001	LSB 24-bit	
2	010	LSB 20-bit	
3	011	LSB 16-bit	
4	100	MSB 8-bit μ-Law	
5	101	MSB 8-bit A-Law	
6	110	N/A	
7	111	N/A	

Set "000" for I^{2}S Compatible, PCM Short and PCM Long formats.
Set "011" when BITFS[1:0] bits=2h (32fs).

Write "0" into the "0" registers.

CONT08: DAC Input, SDOUT2/3 Output, Digital Mixer Input Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C8h	48h	CONT08	SELDAI [1]	SELDAI [0]	SELDO3 [1]	SELDO3 [0]	SELDO2 [1]	SELDO2 [0]	SELMIX [1]	SELMIX [0]	00h

D7, D6: SELDAI[1:0]   DAC Input Select

SELDAI mode	SELDAI[1:0]	Input Data	
0	00	DSP DOUT4	(default)
1	01	MIXOUT	
2	10	SDIN2	
3	11	SDIN1	

Set DIFDA[1:0] bits (CONT06: D5, D4) = 0h when selecting DSP DOUT4 or MIXOUT.

D5, D4: SELDO3[1:0]   SDOUT3 pin Output Select

SELDO3 mode	SELDO3[1:0]	Output Data	
0	00	DSP DOUT3	(default)
1	01	MIXOUT	
2	10	DSP DOUT4	
3	11	SDOUTAD2	

The output format is fixed to MSB 24-bit when selecting SDOUTAD2 or MIXOUT.

D3, D2: SELDO2[1:0]   SDOUT2 pin Output Select

SELDO2 mode	SELDO2[1:0]	Output Data	
0	00	DSP DOUT2	(default)
1	01	GP1	
2	10	SDIN2	
3	11	SDOUTAD2	

The output format is fixed to MSB 24-bit when selecting SDOUTAD2.

(CONT09 D0), D1, D0: SELMIX[2:0] Digital Mixer Input Select

SELMIX mode	SELMIX[2:0]	MIXOUT Lch	MIXOUT Rch	
1	000	SDOUTAD Lch	SDOUTAD Rch	(default)
1	001	SDOUTAD Lch/2 + SDOUTAD2 Lch/2	SDOUTAD Rch	
2	010	SDOUTAD Lch	SDOUTAD Rch /2 + SDOUTAD2 Rch/2	
3	011	SDOUTAD2 Lch	SDOUTAD2 Rch	
4	100	DSP-DOUT4 Lch	SDOUTAD2 Rch	
5	101	SDOUTAD2 Lch	DSP-DOUT4 Rch	
6	110	DSP-DOUT4 Lch	SDOUTAD Rch	
7	111	SDOUTAD Lch	DSP-DOUT4 Rch	

CONT09: Analog Input / Output Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C9h	49h	CONT09	DIFR	INR	DIFL	INL	LO3SW3	LO3SW2	LO3SW1	SELMIX[2]	00h

D7, D6: DIFR, INR ADC Rch Analog Input

DIFR bit	INR bit	ADC Rch
0	0	IN3	(default)
0	1	IN4
1	X	INP2/INN2

D5, D4: DIFL, INL ADC Lch Analog Input

DIFL bit	INL bit	ADC Lch
0	0	IN1	(default)
0	1	IN2
1	X	INP1/INN1
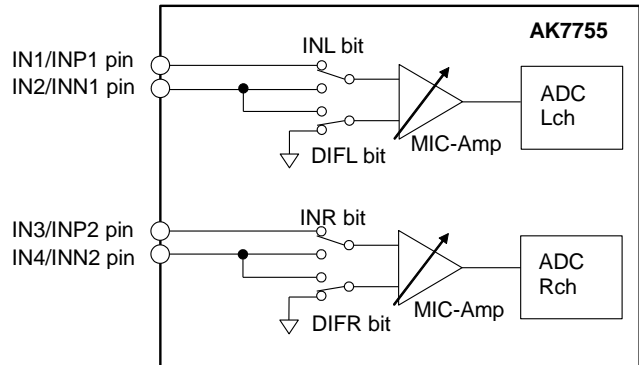
Figure 22. Analog Input Select

D3: LO3SW3   OUT3 Mixing Select 3
     0: LIN off (default)
     1: LIN on

D2: LO3SW2   OUT3 Mixing Select 2
     0: DAC Rch off (default)
     1: DAC Rch on

D1: LO3SW1   OUT3 Mixing Select 1
     0: DAC Lch off (default)
     1: DAC Lch on
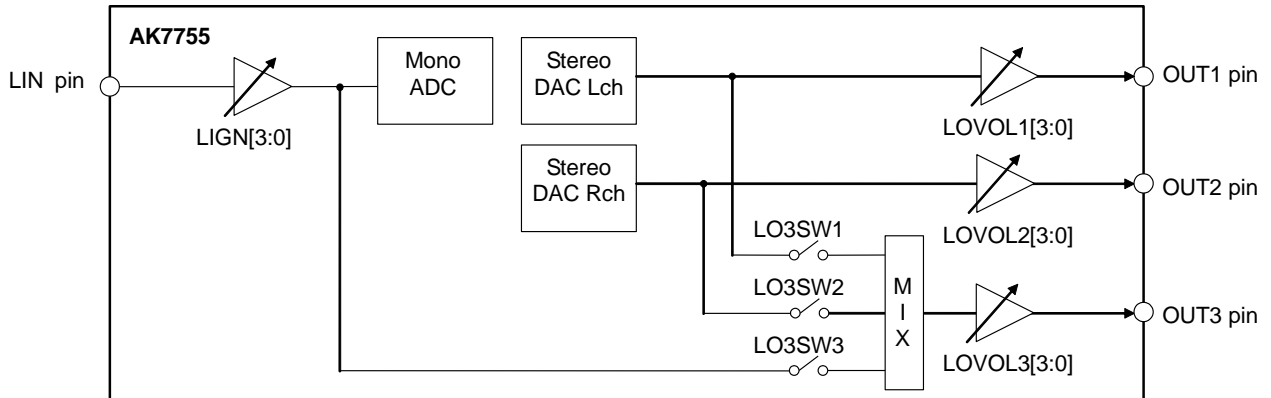
Figure 23. OUT3 Output Select

D0: SELMIX[2] Digital Mixer Input Select
     Refer to CONT08: D1, D0, SELMIX[2:0] bits

CONT0A: CLK and SDOUT Output Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
CAh	4Ah	CONT0A	CLKOE	BICKOE	LRCKOE	0	0	OUT3E	OUT2E	OUT1E	00h

D7: CLKOE   CLKO pin Setting
    0: CLKO = "L" (default)
    1: CLKO Output Enable

D6: BICKOE   BICK pin Output Setting
    0: BICK = "L" (default)
    1: BICK Output Enable
    This setting is invalid in Slave mode (CKM mode 2, 3, and 5 (CONT00: D6-D4)).

D5: LRCKOE   LRCK pin Output Setting
    0: LRCK = "L" (default)
    1: LRCK Output Enable
    This setting is invalid in Slave mode (CKM mode2, 3 and 5).

D2: OUT3E
    0: SDOUT3= "L" (default)
    1: SDOUT3 Output Enable   Valid when JX2E bit (CONT01: D7) = "0"

D1: OUT2E
    0: SDOUT2= "L" (default)
    1: SDOUT2 Output Enable   Valid when JX3E bit (CONT05: D6) = "0"

D0: OUT1E
    0: SDOUT1= "L" (default)
    1: SDOUT1 Output Enable

Write "0" into the "0" registers.

CONT0B: TEST Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
CBh	4Bh	CONT0B	0	0	0	0	0	0	0	0	00h

Write "0" into the "0" registers.

CONT0C: ADC, DAC Volume Transition Time and SDOUT1 Output Settings

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
CCh	4Ch	CONT0C	DSM	0	ATSPAD	ATSPDA	0	SELDO1[2]	SELDO1[1]	SELDO1[0]	00h

D7: DSM   Delta Sigma Module Sampling CLK Setting
   0: DSMCLK 256fs (default)
   1: DSMCLK 12.288MHz

   When setting DSM bit = "1", the out-of-band noise characteristics of the DAC improves at the setting of
   fs = 32kHz or less. However, S/(N+D) performance of the ADC degrades if an ADC and a DAC are
   simultaneously operated by the sampling frequency with fs = 8k, 12k, and 24kHz.

D5: ATSPAD   ADC Volume Transition Time Setting
   0: 1/fs (default)
   1: 4/fs

D4: ATSPDA   DAC Volume Transition Time Setting
   0: 1/fs (default)
   1: 4/fs

D2, D1, D0: SELDO1[2:0] SDOUT1 Pin Output Select

SELDO1 mode	SELDO1[2:0]	Output Data	
0	000	DSP DOUT1	(default)
1	001	GP0	
2	010	SDIN1	
3	011	SDOUTAD	
4	100	EEST	
5	101	SDOUTAD2	
6	110	N/A	
7	111	N/A	

The output format is fixed to MSB 24-bit when selecting SDOUTAD or SDOUTAD2.

Write "0" into the "0" registers.

CONT0D: STO Status Read and EEPROM Download Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
CDh	4Dh	CONT0D	STO	1	0	0	0	0	0	DLS	80h

D7: STO   Status Output
  0: Internal Error Status
  1: Normal Operation (default)
     This is a read only register.

D6: 1
     Thise bit should be set to "1" during system reset (CRESETN bit (CONT0F:D3) = "0" and
     DSPRESETN bit (CONT0F: D2) = "0").

D0: DLS   Start EEPROM Downloading
  0: Normal Operation (default)
  1: Start EEPROM Downloading
     This setting is valid when the I2CSEL pin= "H". Register settings and DSP programs can be
     downloaded from an external EEPROM by setting the EXTEEP pin = "H" or DLS bit = "1".
     However, when selecting memory mat (I2CSEL pin = MATSEL pin = "H"), downloading cannnot be
     executed by DLS bit.

Write "0" into the "0" registers.

CONT0E: ADC, DAC, Lineout Power Management

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
CEh	4Eh	CONT0E	PMADR	PMADL	PMAD2L	PMLO3	PMLO2	PMLO1	PMDAR	PMDAL	00h

D7: PMADR Power Management (MIC-Amp Rch + ADC Rch)
  0: Power-down (default)
  1: Start Normal Operation after releasing CODEC Reset (CRESETN bit (CONT0F: D3) = "1").

D6: PMADL Power Management (MIC-Amp Lch + ADC Lch)
  0: Power- down (default)
  1: Start Normal Operation after releasing CODEC Reset (CRESETN bit = "1").

D5: PMAD2L Power Management (ADC2 Lch)
  0: Power- down (default)
  1: Start Normal Operation after releasing CODEC Reset (CRESETN bit = "1").

D4: PMLO3 Lineout 3 Power Management
  0: Power- down (default)
  1: Normal Operation

D3: PMLO2 Lineout 2 Power Management
  0: Power- down (default)
  1: Normal Operation

D2: PMLO1 Lineout 1 Power Management
  0: Power- down (default)
  1: Normal Operation

D1: PMDAR Power Management (DAC Rch)
  0: Power- down (default)
  1: Start Normal Operation after releasing CODEC Reset (CRESETN bit = "1").

D0: PMDAL Power Management (DAC Lch)
  0: Power- down (default)
  1: Start Normal Operation after releasing CODEC Reset (CRESETN bit = "1").

CONT0F: Reset Settings, Lineout and Digital MIC2 Rch Power Managements

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
CFh	4Fh	CONT0F	0	0	PML1	LRDETN	CRESETN	DSPRESETN	PMAD2R	DLRDY	00h

D5: PMLI   Line-in Power Management
    0: Power-down (default)
    1: Normal Operation

D4: LRDETN   Slave Mode Automatic System Reset Setting
    0: LRCK Detect ON (default)
    1: LRCK Detect OFF
    When this bit is "0", if LRCK and BICK are stopped, the AK7755 enters system reset state
    automatically.

D3: CRESETN   CODEC Reset N
    0: CODEC Reset (default)
    1: CODEC Reset Release
    CODEC means the ADC and the DAC.

D2: DSPRESETN   DSP Reset N
    0: DSP Reset (default)
    1: DSP Reset Release
    The AK7755 is in system reset state when CRESETN bit = "0" and DSPRESETN bit = "0".

D1: PMAD2R Power Managements of ADC2 Rch (only when using digital microphone)
    0: Power-down (default)
    1: The AK7755 enters normal operation after releasing CODEC Reset (CRESETN bit = "1").

D0: DLRDY   DSP Download Ready
    0: Normal Operation (default)
    1: Program Downloading
    DSP programs and coefficient data can be downloaded by setting this bit to "1" during clock reset
    (CKRESETN bit = "0") or when the main clock is stopped. This bit must be set to "0" after finishing
    the downloading.

Write "0" into the "0" registers.

CONT10: Function Settings

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
D0h	50h	CONT10	WDTEN	CRCE	PLLLOCKE	SOCFG	SELSTO	0	0	CKADJEN	00h

D7: WDTEN   WDT (watchdog timer) Setting
     0: WDTE Enable (default)
     1: WDTE Disable

D6: CRCE   CRC (cyclic redundancy check) Setting
     0: CRC Disable (default)
     1: CRC Enable

D5: PLLLOCKE   PLL LOCK Detection
     0: PLL LOCK Disable (default)
     1: PLL LOCK Enable

D4: SOCFG   SO pin Hi-Z Select
     0: Hi-Z (default)
     1: CMOSL

D3: SELSTO   STO/RDY Pin Selecting Status Out
     0: STO (default)
     1: RDY

D0: CKADJEN Clock Adjustment Enable
     0: CKADJ DISABLE (default)
     1: CKADJ ENABLE

     Write this bit to "1" when setting CONT11 CKADJ[7:0] bits.

Write "0" into the "0" registers.

CONT11: DSPMCLK Availability Ratio Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
D1h	51h	CONT11	CK ADJ[7]	CK ADJ[6]	CK ADJ[5]	CK ADJ[4]	CK ADJ[3]	CK ADJ[2]	CK ADJ[1]	CK ADJ[0]	00h

D7-D0: CKADJ [7:0]   DSPMCLK Availability Ratio Setting
     Availability = (256-CKADJ) / 256
     0000_0000: 100% driving (Normal) (default)
     0000_0001: 99.6% driving
     • • •
     1000_0000: 50% driving
     • • •
     1111_1110: 0.8% driving
     1111_1111: 0.4% driving

     Set CONT10 CKADJEN bit to "1" when using this register.
     DSPMCLK must always be more than 10 times of SCLK.
     For example, when SCLK is 2MHz, the setting should be lower than 0hD6 (214) since CKADJ[7:0] < 256 – (2 x 10 x 256) / 122.88 = 214.33.

CONT12: Microphone Gain Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
D2h	52h	CONT12	MGNR[3]	MGNR[2]	MGNR[1]	MGNR[0]	MGNL[3]	MGNL[2]	MGNL[1]	MGNL[0]	00h

D7, D6, D5, D4:　MGNR[3:0] Microphone Input Rch Gain Setting

MGNR mode	MGNR[3:0]	Microphone Input Rch Gain	
0	0000	0dB	(default)
1	0001	2dB	
2	0010	4dB	
3	0011	6dB	
4	0100	8dB	
5	0101	10dB	
6	0110	12dB	
7	0111	14dB	
8	1000	16dB	
9	1001	18dB	
A	1010	21dB	
B	1011	24dB	
C	1100	27dB	
D	1101	30dB	
E	1110	33dB	
F	1111	36dB	

D3, D2, D1, D0:　MGNL[3:0] Microphone Input Lch Gain

MGNL mode	MGNL[3:0]	Microphone Input Lch Gain	
0	0000	0dB	(default)
1	0001	2dB	
2	0010	4dB	
3	0011	6dB	
4	0100	8dB	
5	0101	10dB	
6	0110	12dB	
7	0111	14dB	
8	1000	16dB	
9	1001	18dB	
A	1010	21dB	
B	1011	24dB	
C	1100	27dB	
D	1101	30dB	
E	1110	33dB	
F	1111	36dB	

CONT13: Line-in/Lineout 3 Volume Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
D3h	53h	CONT13	LIGN[3]	LIGN[2]	LIGN[1]	LIGN[0]	LOVOL3 [3]	LOVOL3 [2]	LOVOL3 [1]	LOVOL3 [0]	00h

・D7, D6, D5, D4: LIGN[3:0]   Line-in Volume Setting

LIGN mode	LIGN[3:0]	Line-in Volume Setting	
0	0000	0dB	(default)
1	0001	-3dB	
2	0010	-6dB	
3	0011	-9dB	
4	0100	-12dB	
5	0101	-15dB	
6	0110	-18dB	
7	0111	-21dB	
8	1000	N/A	
9	1001	+3dB	
A	1010	+6dB	
B	1011	+9dB	
C	1100	+12dB	
D	1101	+15dB	
E	1110	+18dB	
F	1111	+21dB	

・D3, D2, D1, D0: LOVOL3[3:0]   Line-out 3 Volume Setting

LOVOL3 mode	LOVOL3[3:0]	Line-out 3 Volume Setting	
0	0000	Mute	(default)
1	0001	-28dB	
2	0010	-26dB	
3	0011	-24dB	
4	0100	-22dB	
5	0101	-20dB	
6	0110	-18dB	
7	0111	-16dB	
8	1000	-14dB	
9	1001	-12dB	
A	1010	-10dB	
B	1011	-8dB	
C	1100	-6dB	
D	1101	-4dB	
E	1110	-2dB	
F	1111	0dB	

CONT14: Line-out 1, Line-out 2 Volume Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
D4h	54h	CONT14	LOVOL2[3]	LOVOL2[2]	LOVOL2[1]	LOVOL2[0]	LOVOL1[3]	LOVOL1[2]	LOVOL1[1]	LOVOL1[0]	00h

D7, D6, D5, D4: LOVOL2[3:0] Line-out 2 Volume Setting

LOVOL2 mode	LOVOL2[3:0]	Lineout 2 Volume Setting	
0	0h	Mute	(default)
1	1h	-28dB	
2	2h	-26dB	
3	3h	-24dB	
4	4h	-22dB	
5	5h	-20dB	
6	6h	-18dB	
7	7h	-16dB	
8	8h	-14dB	
9	9h	-12dB	
A	Ah	-10dB	
B	Bh	-8dB	
C	Ch	-6dB	
D	Dh	-4dB	
E	Eh	-2dB	
F	Fh	0dB	

D3, D2, D1, D0: LOVOL1[3:0] Line-out 1 Volume Setting

LOVOL1 mode	LOVOL1[3:0]	Lineout 1 Volume Setting	
0	0h	Mute	(default)
1	1h	-28dB	
2	2h	-26dB	
3	3h	-24dB	
4	4h	-22dB	
5	5h	-20dB	
6	6h	-18dB	
7	7h	-16dB	
8	8h	-14dB	
9	9h	-12dB	
A	Ah	-10dB	
B	Bh	-8dB	
C	Ch	-6dB	
D	Dh	-4dB	
E	Eh	-2dB	
F	Fh	0dB	

CONT15-16-17: ADC, ADC2 Lch Digital Volume Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
D5h	55h	CONT15	VOLADL[7]	VOLADL[6]	VOLADL[5]	VOLADL[4]	VOLADL[3]	VOLADL[2]	VOLADL[1]	VOLADL[0]	30h
D6h	56h	CONT16	VOLADR[7]	VOLADR[6]	VOLADR[5]	VOLADR[4]	VOLADR[3]	VOLADR[2]	VOLADR[1]	VOLADR[0]	30h
D7h	57h	CONT17	VOLAD2L[7]	VOLAD2L[6]	VOLAD2L[5]	VOLAD2L[4]	VOLAD2L[3]	VOLAD2L[2]	VOLAD2L[1]	VOLAD2L[0]	30h

Refer to "2-3. ADC, ADC2 digital volume".

CONT18-19: DAC Digital Volume Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
D8h	58h	CONT18	VOL DAL[7]	VOL DAL[6]	VOL DAL[5]	VOL DAL[4]	VOL DAL[3]	VOL DAL[2]	VOL DAL[1]	VOL DAL[0]	18h
D9h	59h	CONT19	VOL DAR[7]	VOL DAR[6]	VOL DAR[5]	VOL DAR[4]	VOL DAR[3]	VOL DAR[2]	VOL DAR[1]	VOL DAR[0]	18h

Refer to "2. DAC digital volume".

CONT1A: ADC/DAC MUTE, ADRC and Zero-cross Settings

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
DAh	5Ah	CONT1A	AD MUTE	AD2 MUTE	DA MUTE	1	ADRCRE	ADRCLE	MICRZCE	MICLZCE	00h

D7: ADMUTE   ADC MUTE Setting
    0: Stereo ADC MUTE Release (default)
    1: Stereo ADC MUTE

D6: ADMMUTE ADC2 MUTE Setting
    0: ADC2 MUTE Release (default)
    1: ADC2 MUTE

D5: DAMUTE   DAC MUTE Setting
    0: DAC MUTE Release (default)
    1: DAC MUTE

D4: 1
    Thise bit should be set to "1" during system reset (CRESETN bit (CONT0F: D3) = "0" and DSPRESETN bit (CONT0F: D2) = "0").

D3: ADRCRE   Analog Dynamic Range Controller Rch Enable Setting
    0: ADRC Rch DISABLE (default)
    1: ADRC Rch ENABLE

D2: ADRCLE   Analog Dynamic Range Controller Lch Enable Setting
    0: ADRC Lch DISABLE (default)
    1: ADRC Lch ENABLE

D1: MICRZCE   MICGAIN Rch Zero-corss Enable
    0: Rch Zero-cross Detection ON (default)
    1: Rch Zero-cross Detection OFF

D0: MICLZCE   MICGAIN Lch Zero-cross Enable
    0: Lch Zero-cross Detection ON (default)
    1: Lch Zero-cross Detection OFF

Write "0" into the "0" registers.

CONT1B: Microphone Gain Read Register when using ADRC

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
-	5Bh	CONT1B	AMGNR[3]	AMGNR[2]	AMGNR[1]	AMGNR[0]	AMGNL[3]	AMGNL[2]	AMGNL[1]	AMGNL[0]	00h

This register is a read only register.
AMGNR[3:0] bits will be valid when ADRCRE bit (CONT1A: D3) = "1", and AMGNL[3:0] will be valid when ADRCLE bit (CONT1A: D2) = "1". The microphone gain value set by DSP can be readout.

CONT1C: TEST Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
DCh	5Ch	CONT1C	0	0	0	0	0	0	0	0	00h

Write "0" into the "0" registers.

CONT1D: ADC2 Rch Digital Volume Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
DDh	5Dh	CONT1D	VOLAD2R[7]	VOLAD2R[6]	VOLAD2R[5]	VOLAD2R[4]	VOLAD2R[3]	VOLAD2R[2]	VOLAD2R[1]	VOLAD2R[0]	30h

Refer to "2-3. ADC2 Digital Volume".

CONT1E: Digital Microphone Interface Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
DDh	5Dh	CONT1D	DMIC1	DMCLKP1	DMCLKE1	DMIC2	DMCLKP2	DMCLKE2	0	0	00h

D7: DMIC1   Digital Microphone 1 Select
    0: Not Using DMIC1 (default)
    1: Using DMIC1
       When DMIC1 bit = "1" or DMIC2 bit = "1", pin number 31~ 34 become digital microphone interfaces, and analog inputs are not available.

D6: DMCLKP1   Digital Microphone 1 Channel Setting

DMCLKP1	DMCLK1 pin = "H"	DMCLK1 pin = "L"
0	Rch	Lch	(default)
1	Lch	Rch	

D5: DMCLKE1   Digital Microphone 1 Clock Setting
    0: DMCLK1 pin = "L" (default)
    1: DMCLK1 64fs (Output Enable)

・D4: DMIC2   Digital Microphone 2 Select
    0: Not Using DMIC2 (default)
    1: Using DMIC2
       When DMIC1 bit = "1" or DMIC2 bit = "1", pin number 31 ~ 34 become digital microphone interfaces, and analog inputs are not available.

・D3: DMCLKP2   Digital Microphone 2 Channel Setting

DMCLKP2	DMCLK2 pin = "H"	DMCLK2 pin = "L"
0	Rch	Lch	(default)
1	Lch	Rch	

・D2: DMCLKE2   Digital Microphone 2 Clock Setting
    0: DMCLK2 pin = "L" (default)
    1: DMCLK1 64fs (Output Enable)

Do not write data into CONT21 - CONT25.

CONT26

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
E6	66h	CONT26	0	0	0	0	0	0	0	1	00h

D0: 1
    Thise bit should be set to "1" during system reset (CRESETN bit (CONT0F: D3) = "0" and DSPRESETN bit (CONT0F: D2) = "0").

Write "0" into the "0" registers.

Do not write data into CONT27 - CONT29.

CONT2A

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
EA	6Ah	CONT2A	1	0	0	0	0	0	0	0	00h

D7: 1
    Thise bit should be set to "1" during system reset (CRESETN bit (CONT0F: D3) = "0" and DSPRESETN bit (CONT0F: D2) = "0").

Write "0" into the "0" registers.

Do not write data into CONT2B – CONT2F.

■ **Power-up Sequence**

1. When not downloading settings and programs from EEPROM

The AK7755 should be powered up when the PDN pin = "L". AVDD and TVDD must be powered up first before DVDD when DVDD is supplied externally (LDOE pin = "L"). In this case, the power-up sequence between AVDD and TVDD is not critical (Note 45). Control register settings are initialized by the PDN pin = "L".

After all power supplies are fed, the REF generation circuit (analog reference voltage source) and the regulator for driving internal digital circuits (only when LDOE pin = "H") start up by setting the PDN pin to "H". Control register access must be made after 1ms from the PDN pin = "H".

There is a possibility that a glitch occurs at the SO/SDA pin before the power supply for internal digital circuit is start up when the LDOE pin = "H". Do not make communication to other devises connected to the AK7755 by SPI or I2C bus for 1ms after changing the PDN pin = "H".

Set AINE bit (CONT00: D3) to "1" fist when using the IN1/INP1, IN2/INN1, IN3/INP2 and IN4/INN2 pins as analog inputs.

The PLL starts operation by a clock reset release (CKRESETN bit (CONT01: D0) = "0" → "1") and generates the internal master clock after setting control registers. Therefore, necessary system clock must be input and control register settings for CONT00 ~ CONT01 are must be finished before releasing the clock reset.

Interfacing with the AK7755 except control register settings should be made when PLL oscillation is stabilized after clock reset release (take a 10ms interval or confirm "H" level output of PLLLOCK signal from the STO/RDY pin) (Figure 24). However, DSP program and coefficient data can be written even when the system clock is stopped. DSP programs and coefficient data can be written in 1ms by setting DLRDY bit ="0" → "1" (CONT0F, D0). DLRDY bit (CONT0F: D0) must be set to "0" after the download (Figure 25).

When using a crystal oscillator in master mode, set the CKM[2:0] bits (CONT00: D6-D4) = 0h or 1h, and release the clock reset after crystal oscillation is stabilized. The stabilizing time of crystal oscillation is dependent on the crystal and external circuits.

The system clock must not be stopped except during the clock reset and power-down mode.
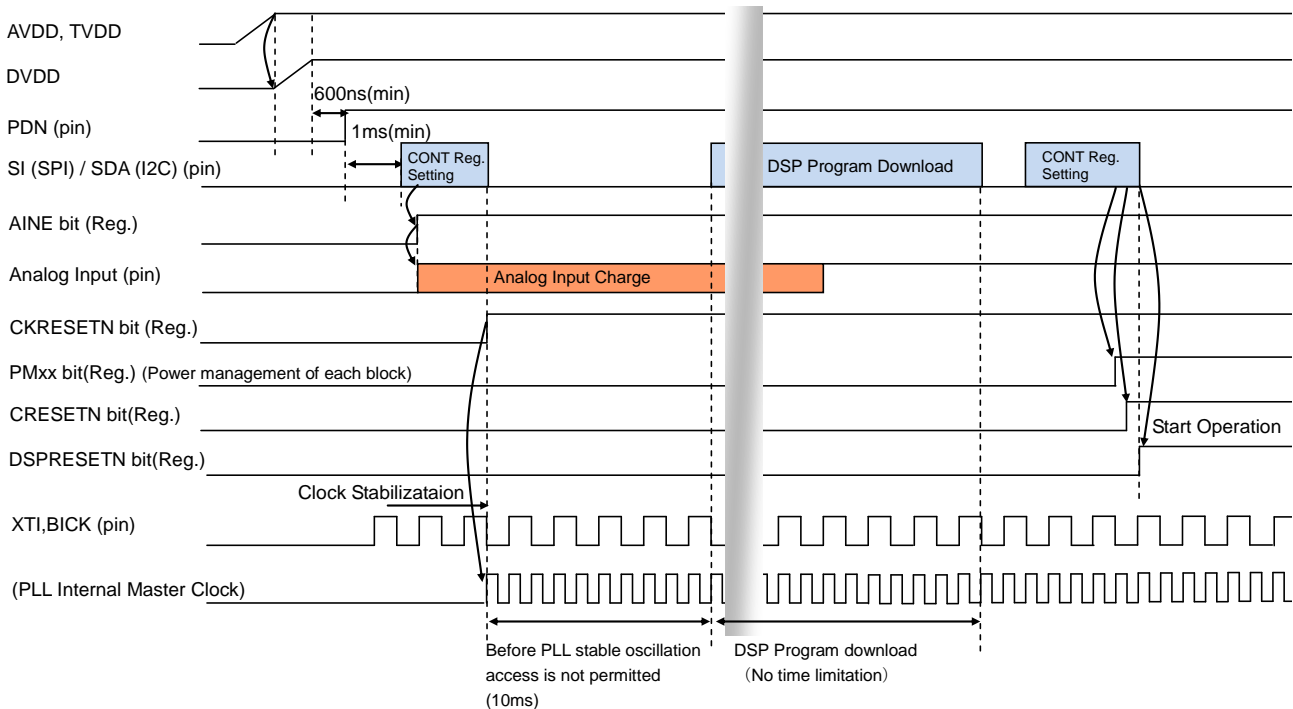
Figure 24. Power-up Sequence 1 (When not downloading from EEPROM)
(With External Power Supply (LDOE pin = "L"), No downloading from EEPROM)
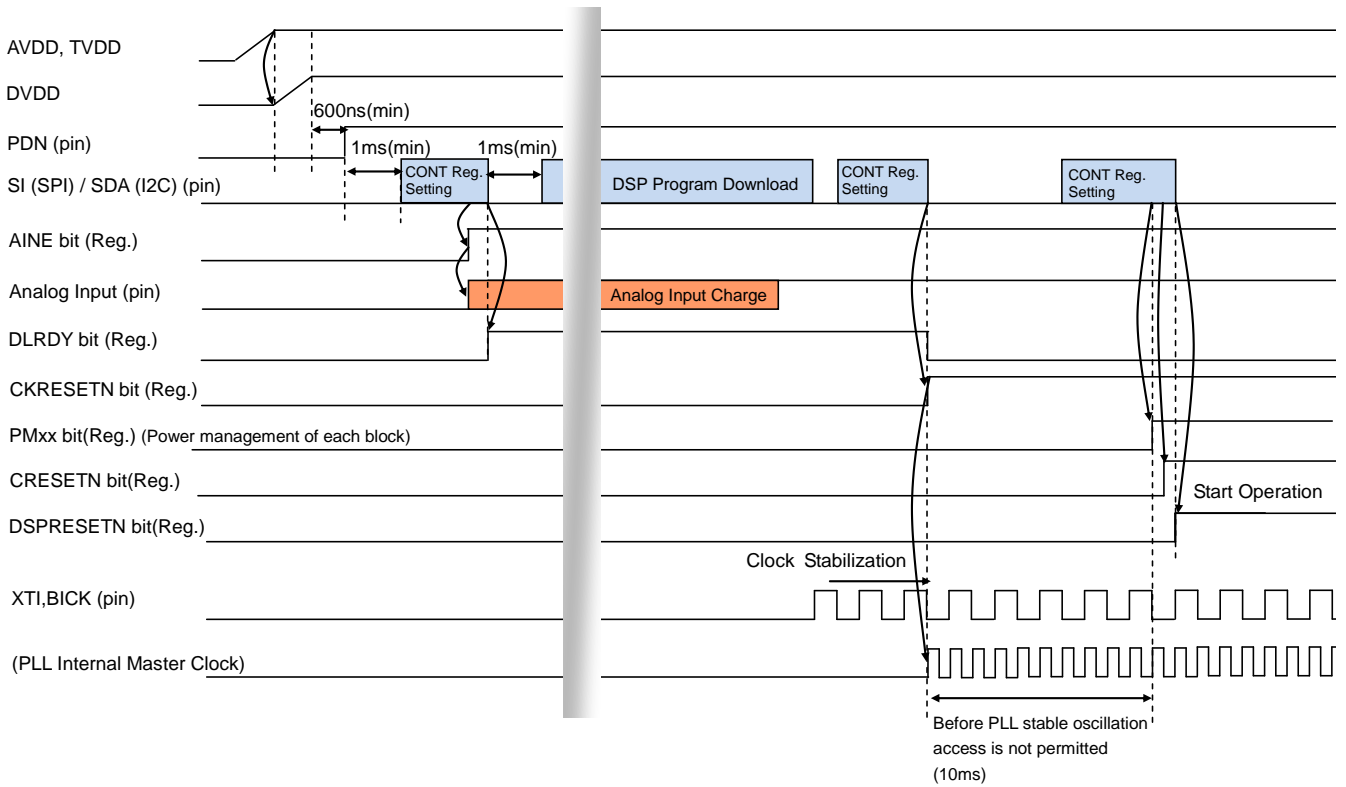
Figure 25. Power-up Sequence 2
(With External Power Supply (LDOE pin = "L"), DLRDY Setting, No downloading from EEPROM)

Note 45. When TVDD is powered up before AVDD while the SDIN2 pin = "H" (TVDD), a 6mA current at maximum (when TVDD = 3.6V, AVDD = 0V) flows to AVDD from the the SDIN2 pin. However, the current does not flow if the SDIN2 pin = "L" or if a condition of "TVDD - AVDD ≤ 0.3V" is satisfied while the SDIN2 pin = "H". The SDIN2 pin must be set to "L" if AVDD remains off while TVDD is turned on. This has to be followed in the power-down sequence too.

2. When downloading settings and programs from EEPROM

When downloading programs from an EEPROM, I²C interface (I2CSEL pin = "H") and a 12.288MHz clock input to the XTI pin are necessary, or a 12.288MHz crystal oscillator must be connected to the XTI and XTO pins. In this case, only CKM mode 0 and 2 (CONT00: D6-D4) are available. The AK7755 should be powered up when the PDN pin = "L". AVDD and TVDD must be powered up first before DVDD when DVDD is supplied externally (LDOE pin = "L"). In this case, the power-up sequence between AVDD and TVDD is not critical. Set the PDN pin to "H" to start the power supply circuits for REF (analog reference voltage source) generator and internal digital circuit (only when the LDOE pin = "H") after all power supplies are fed. There are three ways to start downloading control register settings, DSP programs and Coefficient RAM: by PDN pin (1) (Figure 26), by EXTEEP pin (2) (Figure 26) and by DLS bit (3) (Figure 27).
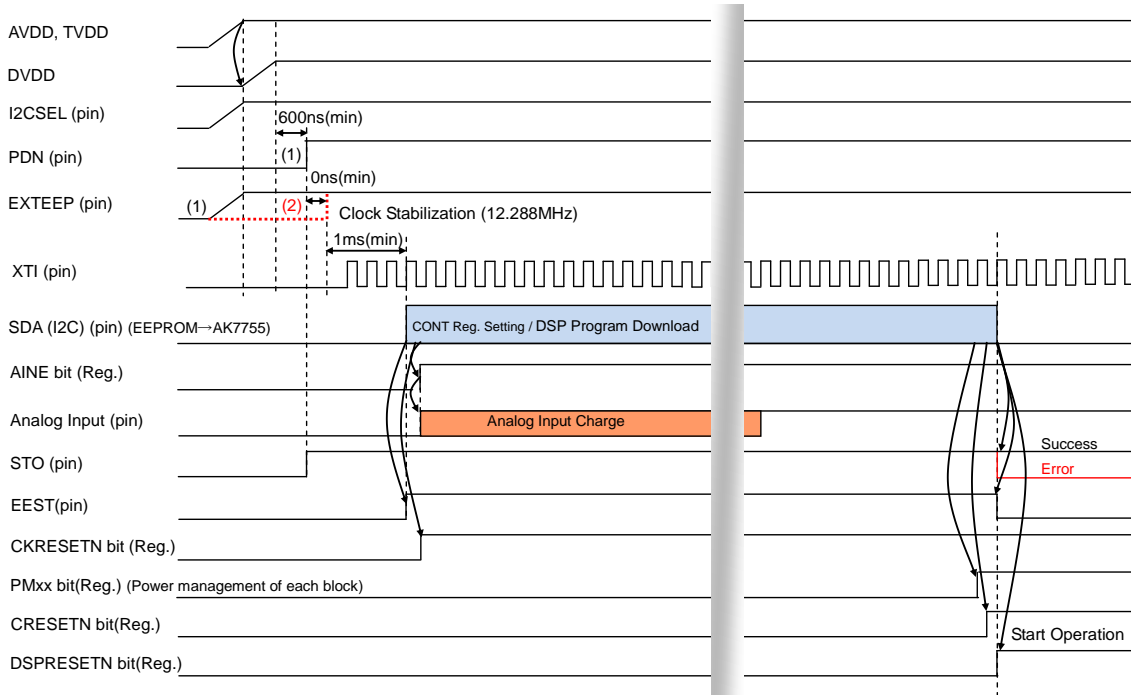
Figure 26. Power-up Sequence 3
(With External Power Supply (LDOE pin = "L"), Downloading from EEPROM (1)(2))

(1) Start Downloading by PDN pin
  Power ON (AVDD, TVDD), I2CSEL pin="H", EXTEEP pin="H"→ (DVDD→), PDN pin="L"→"H"

(2) Start Downloading EXTEEP pin (Dotted Line)
  Power ON (AVDD, TVDD), I2CSEL pin = "H" → (DVDD→), PDN pin = "L" → "H"
  → EXTEEP pin = "L" → "H"
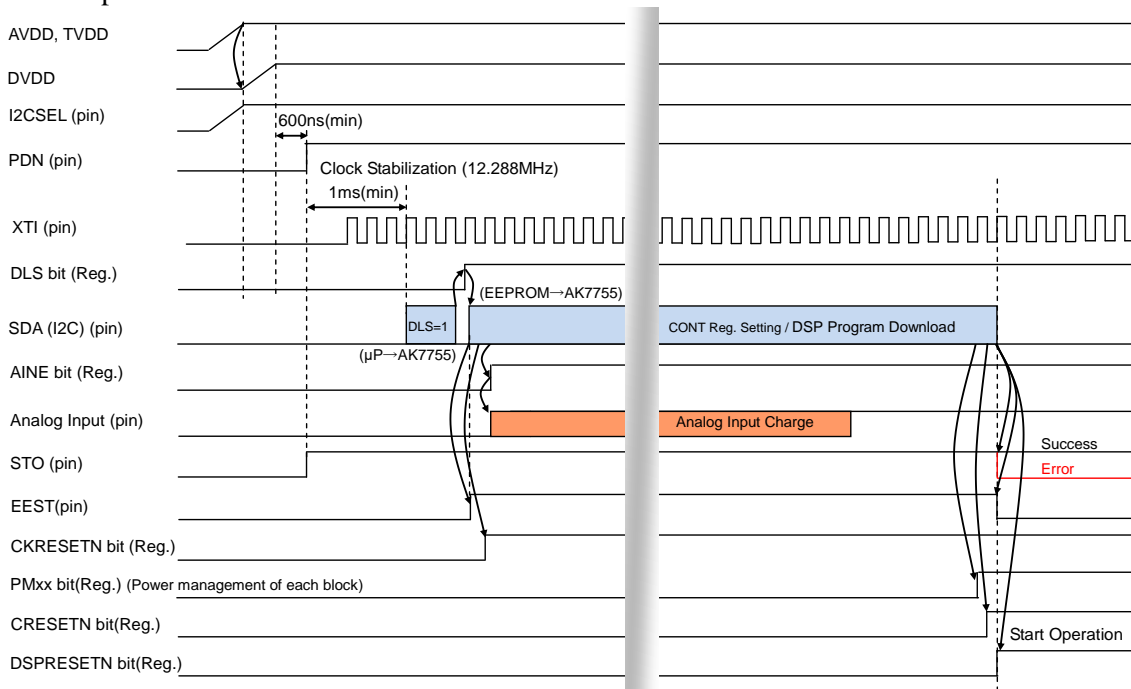
Figure 27. Power-up Sequence 4
(With External Power Supply (LDOE pin = "L"), Downloading from EEPROM (3))

(3) Start Downloading DLS bit
  Power ON (AVDD, TVDD), I2CSEL pin="H"→(DVDD→), PDN pin="L"→"H" →DLS bit = "0"→"1"

■ LDO (Internal Circuit Drive Regulator)

The AK7755 has a regulator for driving internal digital circuits (LDO). When using the LDO, the LDOE pin must be fixed to "H" and connect a 1μF (±30%) capacitor between the AVDRV pin and the VSS pin. The LDO starts operation by releasing power-down mode, and control register write/read can be made 1ms after the power-down release.

A glitch may occur at the SO/SDA pin before the regulator for driving internal digital circuits starts up. Do not communicate with other devices connected to the AK7755 by SPI bus or I2C bus within 1ms after setting the PDN pin = "H".

The AK7755 has an overcurrent protection circuit to avoid abnormal heat of the device that is caused by a short of the AVDRV pin to VSS and etc., and an overvoltage protection circuit to protect from exceeded voltage when the voltage to the AVDRV pin gets too high. When these protection circuits perform, internal circuits are powered down and the STO pin outputs "L". The internal circuit will not return to a normal operation until being reset by the PDN pin after removing the problems.
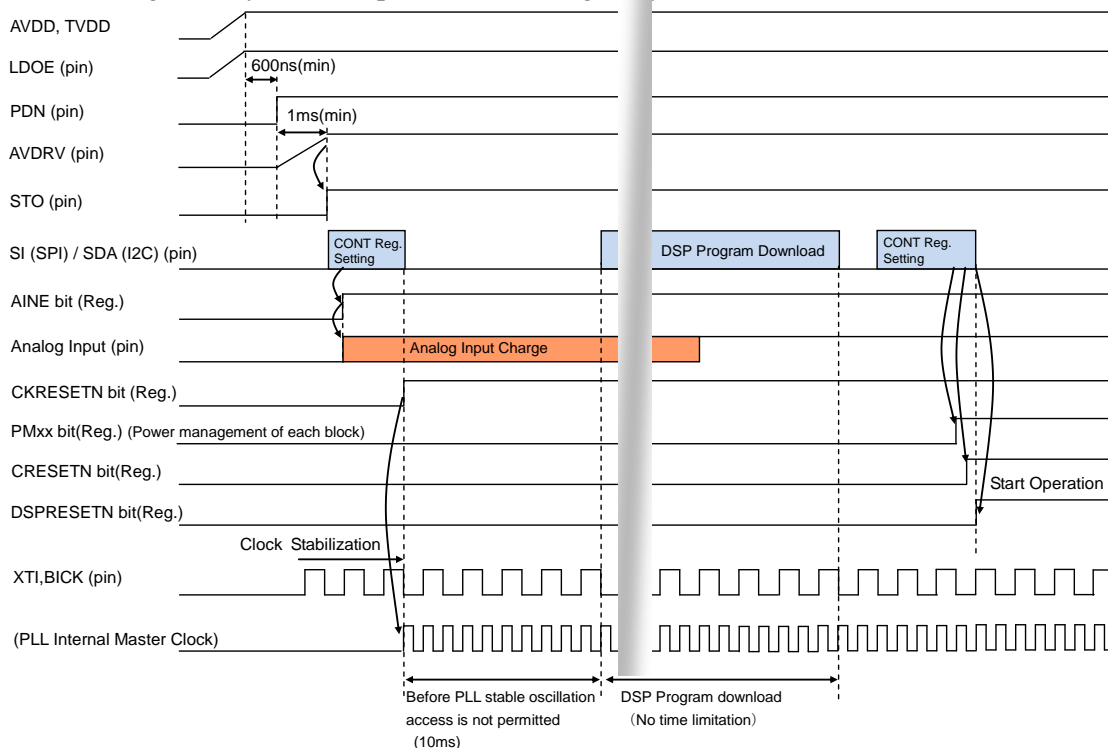
Figure 28. Power-up Sequence 5
(With LDO (LDOE pin = "H"), No downloading from EEPROM)

■ Power-down Sequence

The AK7755 should be powered down when the PDN pin = "L". Stop external clocks during this power-down state and then OFF the power supplies. Do not input external clocks when the power supplies are off (a current will flow through protection diodes). AVDD and TVDD must be powered down after DVDD when DVDD is supplied externally (LDOE pin = "L"). In this case, the power-down sequence between AVDD and TVDD is not critical.
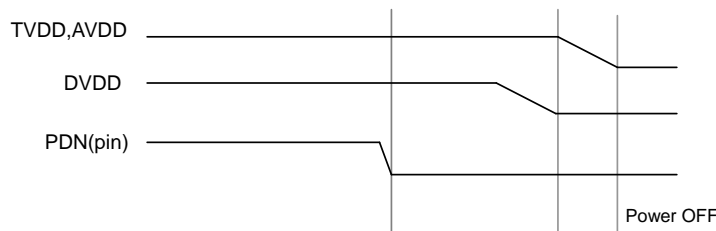
Figure 29. Power-down Sequence

■ Power-down and Reset

1. Power-down, Reset and Power Management of the AK7755

The AK7755 has four types of power-down and reset functions that are power-down (PDN pin), Clock reset (CKRESETN bit (CONT01:D0)), CODEC reset (CRESETN bit(CONT0F:D3)) and DSP reset (DSPRESETN bit(CONT0F:D2)). Each block can be powered-down by power management registers.

2. Power-down

The AK7755 is powered down by setting the PDN pin = "L". The PDN pin must be set to "L" when power up the AK7755. The statuses of output pins in power-down mode are shown below.

LDOE pin = "L" (External 1.2V supply mode)

No	Pin Name	I/O	Power-down Mode Status	No	Pin Name	I/O	Power-down Mode Status
1	VCOM	O	L	17	SO/SDA	I/O	Hi-Z
6	STO/RDY	O	H	18	SCLK/SCL	I/O	Hi-Z
7	LRCK	I/O	L	26	OUT3	O	Hi-Z
8	BICK	I/O	L	27	OUT2	O	Hi-Z
9	CLKO	O	L	28	OUT1	O	Hi-Z
10	XTO	O	H	31	IN4/INN2/DMCLK2	I/O	Hi-Z
11	XTI	I	H	32	IN3/INP2/DMDAT2	I	Hi-Z
14	JX2/SDOUT3/JX2/MAT1	I/O	L	33	IN2/INN1/DMCLK1	I/O	Hi-Z
15	SDOUT2/JX3/MAT1	I/O	L	34	IN1/INP1/DMDAT1	I	Hi-Z
16	SDOUT1	O	L				

Note 46. [I/O] indicates Input / Output attribute of each pin.

LDOE pin = "H" (LDO mode)

No	Pin Name	I/O	Power-down Mode Status	No	Pin Name	I/O	Power-down Mode Status
1	VCOM	O	L	17	SO/SDA	I/O	Hi-Z
6	STO/RDY	O	L	18	SCLK/SCL	I/O	Hi-Z
7	LRCK	I/O	L	24	AVDRV	O	L
8	BICK	I/O	L	26	OUT3	O	Hi-Z
9	CLKO	O	L	27	OUT2	O	Hi-Z
10	XTO	O	H	28	OUT1	O	Hi-Z
11	XTI	I	H	31	IN4/INN2/DMCLK2	I/O	Hi-Z
14	JX2/SDOUT3/JX2/MAT1	I/O	L	32	IN3/INP2/DMDAT2	I	Hi-Z
15	SDOUT2/JX3/MAT1	I/O	L	33	IN2/INN1/DMCLK1	I/O	Hi-Z
16	SDOUT1	O	L	34	IN1/INP1/DMDAT1	I	Hi-Z

3. Power-down Release

3-1. LDOE = "L" (External 1.2V supply mode)

DVDD, TVDD and AVDD should be supplied when the PDN pin = "L". By bringing the PDN pin "H" 600ns (min) after all power supplies are fed (DVDD, TVDD and AVDD), REF voltage circuit (Analog reference voltage) starts operation. Control register write / read should be made 1ms after bringing the PDN pin = "H" (Figure 24). AVDD and TVDD must be powered up first before DVDD. In this case, the power-up sequence between AVDD and TVDD is not critical.

3-2. LDOE = "H" (LDO mode)

TVDD and AVDD should be supplied when the PDN pin = "L". By bringing the PDN pin "H" 600ns (min) after TVDD and AVDD are fed, the power supply circuits for REF generator and internal digital circuit start operation. Control register write / read should be made 1ms after bringing the PDN pin = "H" (Figure 28).

4. Clock Reset

Clock reset is defined as when CKRESERN bit (CONT01: D0) = "0" after power-down release (PDN pin = "H"). The AK7755 is in the clock reset state after releasing power-down. At this time, all internal blocks of the AK7755, except the REF circuit and the power supply circuit for digital block, are in power-down mode. Even the PLL for internal master clock generation is not in operation.

Control register write/read should be made 1ms (min.) after power-down release. Clock generating control registers (CONT00 ~ CONT01) must be set during clock reset. AINE bit (CONT00: D3) should be set to "1" first when using the IN1/INP1, IN2/INN1, IN3/INP2 and IN4/INN2 pins as analog inputs. DSP program and coefficient RAM data writing to the DSP become available in 1ms by setting DLRDY bit (CONT0F: D0) = "0" → "1" during clock reset (CKRESETN bit = "0"). DLRDY bit must be set to "0" when finishing downloading. Necessary system clock (XTI@CKM mode0-2 or BICK@CKM mode 3, 5(CONT00: D6-D4)) must be input before releasing the clock reset (Figure 16). The PLL for internal master clock starts operation and generating master clock when the clock reset state is released (CKRESETN bit = "1"). Do not send DSP programs, coefficient data or a command code for system reset release from a microcontroller to the AK7755 until the PLL oscillation is stabilized (for 10ms or during Low output period of the PLLLOCK signal from the STO pin).

System clocks must be changed during a clock reset or in power-down mode (PDN pin = "L"). The AK7755 enters clock reset state by setting CKRESETN bit to "0" after system reset. The PLL and the internal clock are stopped by this clock reset and the clock change can be done safely. Change register settings and system clock frequencies during the clock reset. After a system clock is stabilized, the PLL starts operation by setting CKRESETN bit to "1".
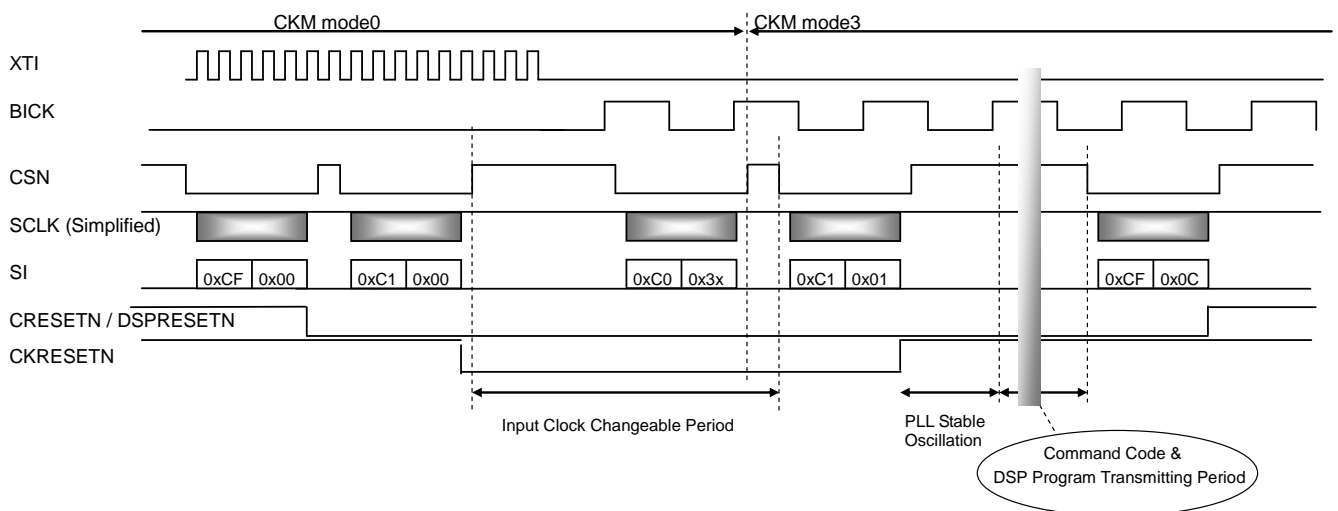
Figure 30. Clock Reset Sequence (e.g. CKM mode0 → CKM mode 3)

5. System Reset

System reset is defined as when CRESETN bit (CONT0F: D3) = "0" and DSPRESETN bit (CONT0F: D2) = "0" after clock reset is released (CKRESETN bit (CONT01: D0) = "1"). PRAM and CRAM downloading should be executed in this state. PRAM and CRAM accessing of the AK7755 should be made when PLL oscillation is stabilized after clock reset release (take a 10ms interval or confirm "H" level output of PLLLOCK signal from the STO pin).
System reset is released when either CODEC reset (CRESETN bit) or DSP reset (DSPRESETN bit) is released ("0" → "1") after DSP programs and coefficient data are transmitted.
After setting power management bits of necessary blocks and releasing CODEC reset (CRESETN bit = "1"), the ADC, DAC and DSP blocks will be in normal operation by releasing DSP reset (DSPRESETN bit = "1") (Note 47, Note 48). A system reset image is shown below.
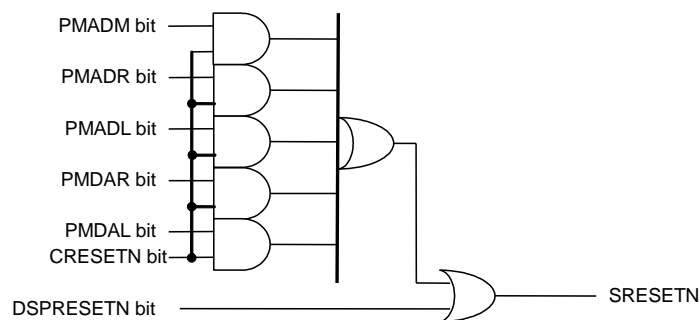
Figure 31. System Reset Structure

In slave mode, the AK7755 starts operation in synchronization of an LRCK rising edge (falling edge in I²S mode) when system reset is released. If LRCK and BICK are stopped, the AK7755 becomes the system reset state automatically. In this case, the system reset state is released if LRCK and BICK are input again.

Note 47. It is possible to release CODEC reset and DSP reset simultaneously (CRESETN bit = "1" and DSPRESETN bit = "1") because CRESETN bit and DSPRESETN bit are in the same register address. However, do not release CODEC reset during DSP reset release.
Note 48. If it is necessary to turn ON the DAC during ADC operation, the DAC must be powered up simultaneously with an ADC by setting PMDAL/R bit = "1". In this case, the DAC output should be controlled with PMLO1/2/3 bit or DAMUTE bit. However, there is no restriction on turning on the ADC while the DAC in operation.

6. Restriction of DSP reset

If a CRAM write operation is included in a DSP program, the CRAM write may fail rarely when the microprocessor executes DSP reset (DSPRESETN bit = "1" → "0") during DSP RUN. Therefore, there is a possibility that DSP processing may not be executed correctly after the next DSP reset release (DSPRESETN bit = "0" → "1").

Either countermeasure must be taken in the control flow if DSP reset is unavoidable because of the system requirement.
1. Re-write all of the CRAM data before releasing DSP reset.
2. Stop CRAM write operation in the DSP program before DSP reset.

■ RAM Clear

The AK7755 has a RAM clear function. After system reset release (during RUN), data RAM and delay RAM are cleared by "0" (RAM clear). The internal PLL must have a stable oscillation before system reset release. The required time to clear RAM is 400μs.

In the RAM clear sequence, it is possible to send commands to the DSP. (DSP is stopped during RAM clear sequence. The sent command is accepted automatically after this sequence is completed.)
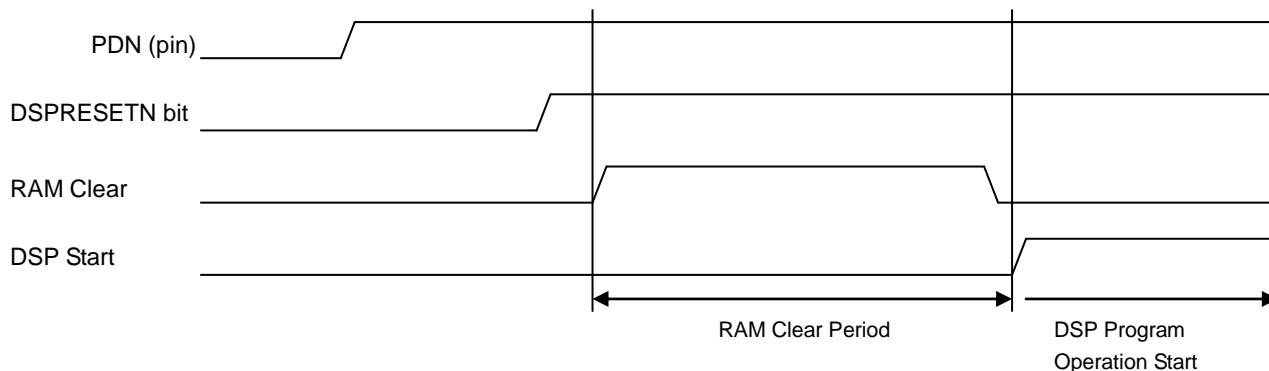
Figure 32. RAM Clear Sequence

■ Serial Data Interface

Serial audio data pins; the SDIN1, SDIN2, SDOUT1, SDOUT2 and SDOUT3 pins are interfaced with an external system by LRCK and BICK. Control register settings are needed to use these interfaces (Refer to Block Diagram (Figure 1) and Control register setting).

The data format is 2's compliment MSB first. I/O format supports MSB justified, LSB justified, I²S compatible and PCM format. (In I²S compatible/PCM mode, all audio data input and output pins are in I²S compatible/PCM format, respectively.)

The input (SDIN1 and SDIN2) format is 24-bit MSB justified at default. 24-bit/20-bit/16-bit LSB justified, I²S and PCM formats are also selectable by control register DIF[1:0] bits. The output (SDOUT1, ADOUT2 and SDOUT3) format is 24-bit MSB justified at default. 24-bit/20-bit/16-bit LSB justified, I²S and PCM formats are selectable by setting DOF[1:0] bits. The SDOUT1 also supports 8-bit MSB justified μ-Law and 8-bit MSB justifid A-Law formats. The output data of the ADC (SDOUTAD and SDOUTAD2) is fixed to 24-bit MSB justified.

mode	LRIF[1:0]	DIFDIF2, DIFDA[1:0] or DOF2, 3, 4[1:0]	DIF1[2:0] or DOF1[2:0]	BITFS[1:0]	Format
0	0h	0h	0h	0h	MSB 24-bit 64fs
1	0h	1h	1h	0h/1h	LSB 24-bit 64fs/48fs
2	0h	2h	2h	0h/1h	LSB 20-bit 64fs/48fs
3	0h	3h	3h	0h/1h/2h	LSB 16-bit 64fs/48fs/32fs
4	0h	N/A	4h	0h	MSB 8-bit μ-Law
5	0h	N/A	5h	0h	MSB 8-bit A-Law
6	1h	0h	0h	0h	I²S Compatible
7	2h	0h	0h	0h/3h	PCM Short Frame 64fs/256fs
8	3h	0h	0h	0h/3h	PCM Long Frame 64fs/256fs

Table 2. Serial Data Format Setting

Serial Data Format Examples

1. MSB justified (mode 0)
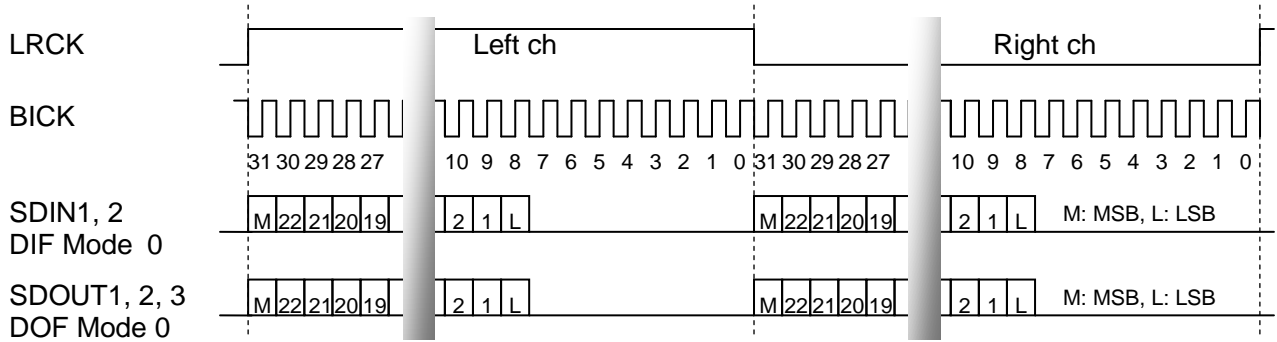
Figure 33. MSB Justified BICK 64fs

2. LSB justified (mode1, 2, 3)
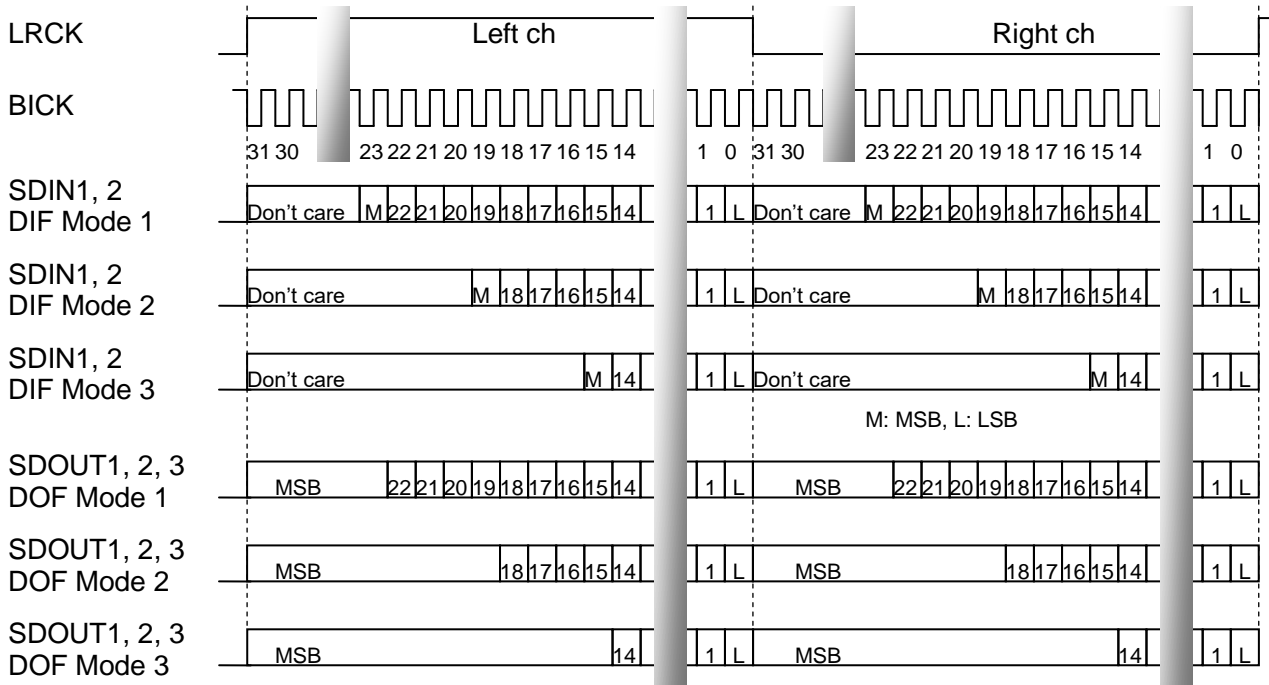
Figure 34. LSB Justified BICK 64fs

LRCK — Left ch — Right ch

BICK

23 22 21 20 19 18 17 16 15 14 13 12 11 10 ... 1 0 ... 23 22 21 20 19 18 17 16 15 14 13 12 11 10 ... 1 0

SDIN1,2 DIF mode1
M 22 21 20 19 18 17 16 15 14 13 12 11 10 | 1 L | M 22 21 20 19 18 17 16 15 14 13 12 11 10 | 1 L

SDIN1,2 DIF mode2
Don't care M 18 17 16 15 14 13 12 11 10 | 1 L | Don't care M 18 17 16 15 14 13 12 11 10 | 1 L

SDIN1,2 DIF mode3
Don't care M 14 13 12 11 10 | 1 L | Don't care M 14 13 12 11 10 | 1 L

M:MSB, L:LSB

SDOUT1,2,3 DOF mode1
M 22 21 20 19 18 17 16 15 14 13 12 11 10 | 1 L | M 22 21 20 19 18 17 16 15 14 13 12 11 10 | 1 L

SDOUT1,2,3 DOF mode2
MSB 18 17 16 15 14 13 12 11 10 | 1 L | MSB 18 17 16 15 14 13 12 11 10 | 1 L

SDOUT1,2,3 DOF mode3
MSB 14 13 12 11 10 | 1 L | MSB 14 13 12 11 10 | 1 L

Figure 35. LSB Justified BICK 48fs

LRCK — Left ch — Right ch

BICK

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

SDIN1,2 DIF mode3
M 14 13 12 11 10 9 8 7 6 5 4 3 2 1 L | M 14 13 12 11 10 9 8 7 6 5 4 3 2 1 L

SDOUT1,2,3 DOF mode3
M 14 13 12 11 10 9 8 7 6 5 4 3 2 1 L | M 14 13 12 11 10 9 8 7 6 5 4 3 2 1 L
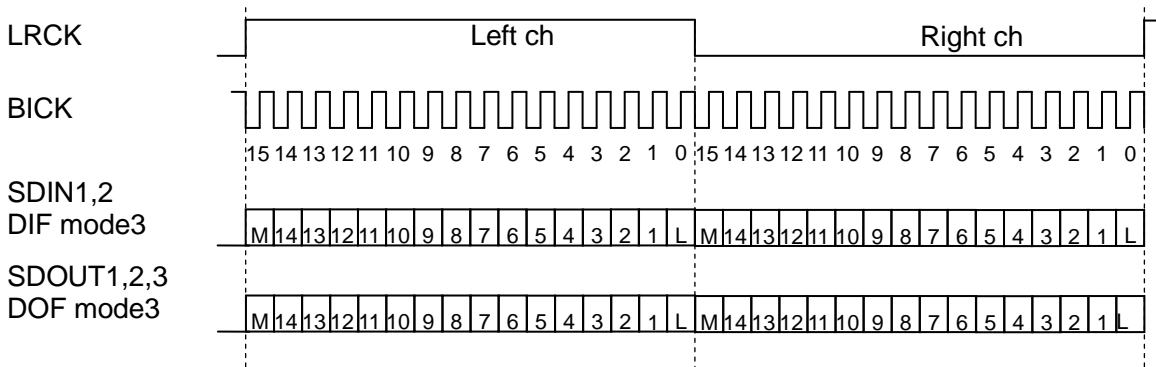
Figure 36. LSB Justified BICK 32fs

3. MSB 8-bit μ-Law、MSB 8-bit A-Law (mode 4,5)

LRCK — Left ch — Right ch

BICK

31 30 29 28 27 26 25 24 ... 7 6 5 4 3 2 1 0 31 30 29 28 27 26 25 24 ... 7 6 5 4 3 2 1 0

SDIN1 DIF mode4/5
M 6 5 4 3 2 1 L | M 6 5 4 3 2 1 L — M:MSB, L:LSB

SDOUT1 DOF mode4/5
M 6 5 4 3 2 1 L | M 6 5 4 3 2 1 L — M:MSB, L:LSB

SDIN2 DIF mode0
M 22 21 20 19 18 17 16 ... 1 L | M 22 21 20 19 18 17 16 ... 1 L — M:MSB, L:LSB

SDOUT2,3 DOF mode0
M 22 21 20 19 18 17 16 ... 1 L | M 22 21 20 19 18 17 16 ... 1 L — M:MSB, L:LSB
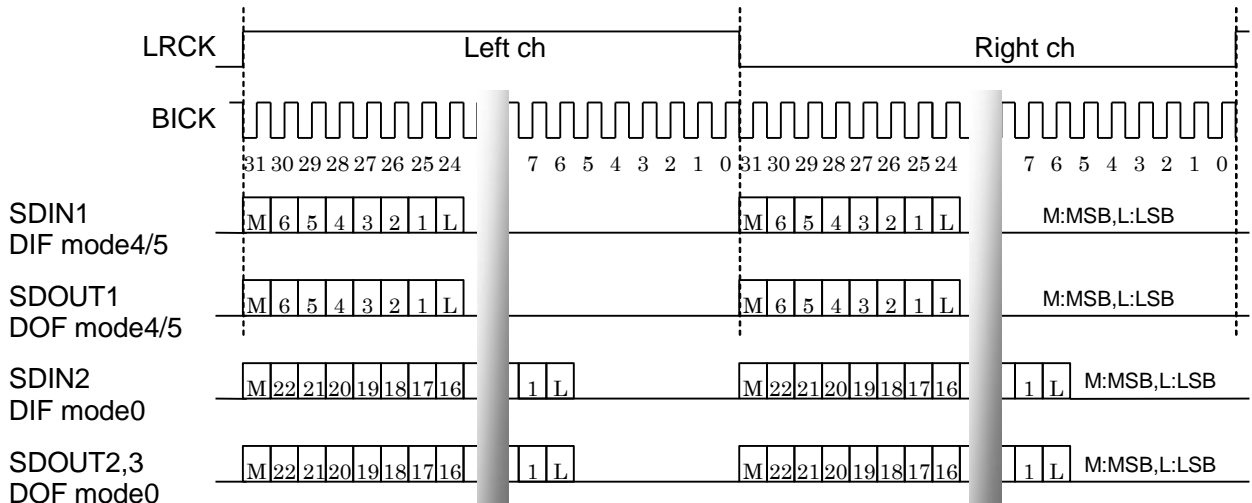
Figure 37. MSB Justified 8-bit μ-Law, 8-bit A-Law BICK 64fs

4. I²S (mode6)

LRCK

BICK

Left ch

Right ch

31 30 29 28 27   10 9 8 7 6 5 4 3 2 1 0   31 30 29 28 27   10 9 8 7 6 5 4 3 2 1 0

SDIN1, 2

M 22 21 20   3 2 1 L   M 22 21 20   3 2 1 L   M: MSB, L: LSB

SDOUT1, 2, 3

M 22 21 20   3 2 1 L   M 22 21 20   3 2 1 L   M: MSB, L: LSB
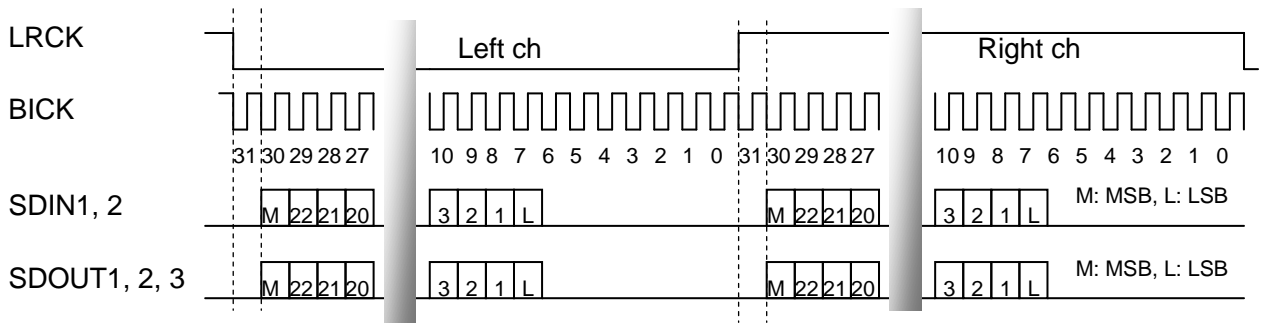
Figure 38. I²S BICK 64fs

5. PCM Short Frame (mode7)

LRCK   SF   tBCLK

BICK

63 62 61 60 59   42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27   10 9 8 7 6 5 4 3 2 1 0

SDIN1, 2

M 22 21 20 19   2 1 L   M 22 21 20 19   2 1 L

SDOUT1, 2, 3

M 22 21 20 19   2 1 L   M: MSB, L: LSB   M 22 21 20 19   2 1 L

Left ch   Right ch
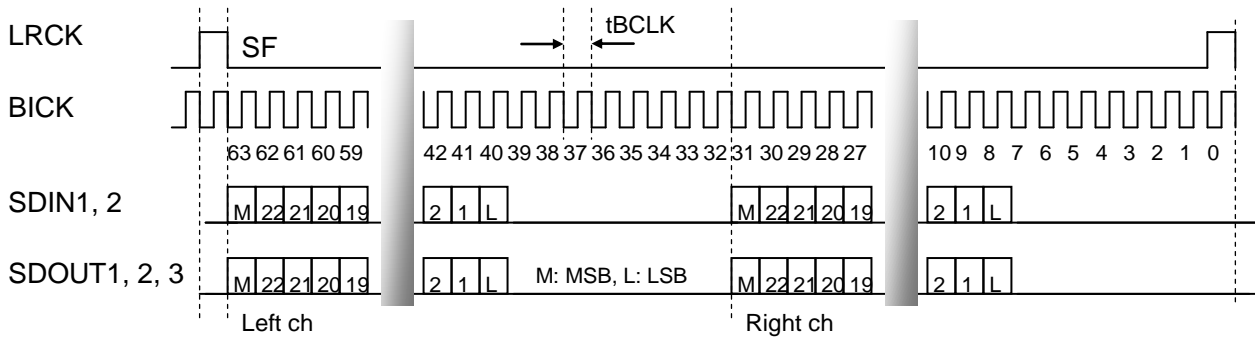
Figure 39. 64fs PCM Short Frame

LRCK   SF   tBCLK

BICK

255 254 253 252 251   234 233 232 231 230 229 228 227 226 225 224 223 222 221 220 219   202 201 200 199 198   3 2 1 0

SDIN1,2

M 22 21 20 19   2 1 L   M 22 21 20 19   2 1 L

SDOUT1,2,3

M 22 21 20 19   2 1 L   M:MSB,L:LSB   M 22 21 20 19   2 1 L

Left ch   Right ch

tBCLK × 32

tBCLK × 256
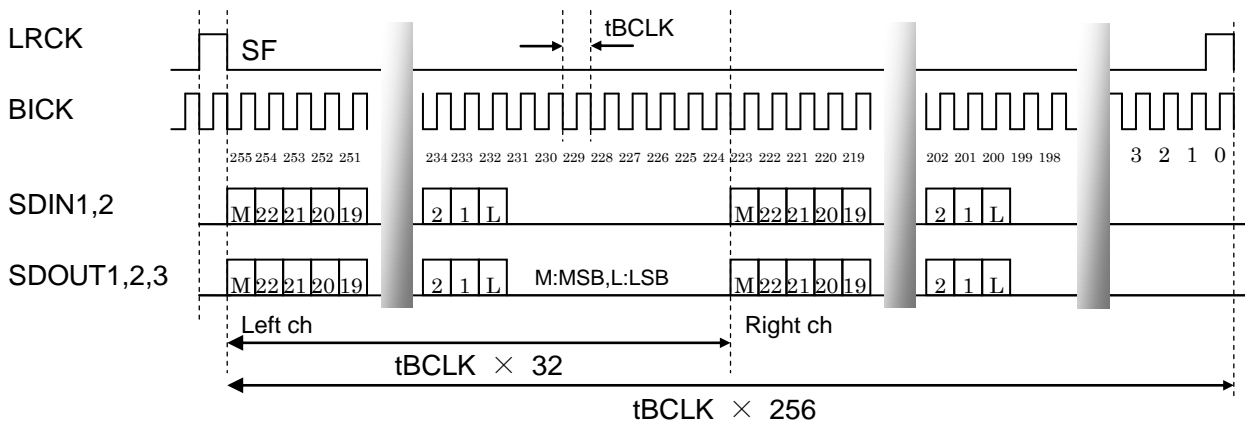
Figure 40. PCM Short Frame 256fs

6. PCM Long Frame (mode8)
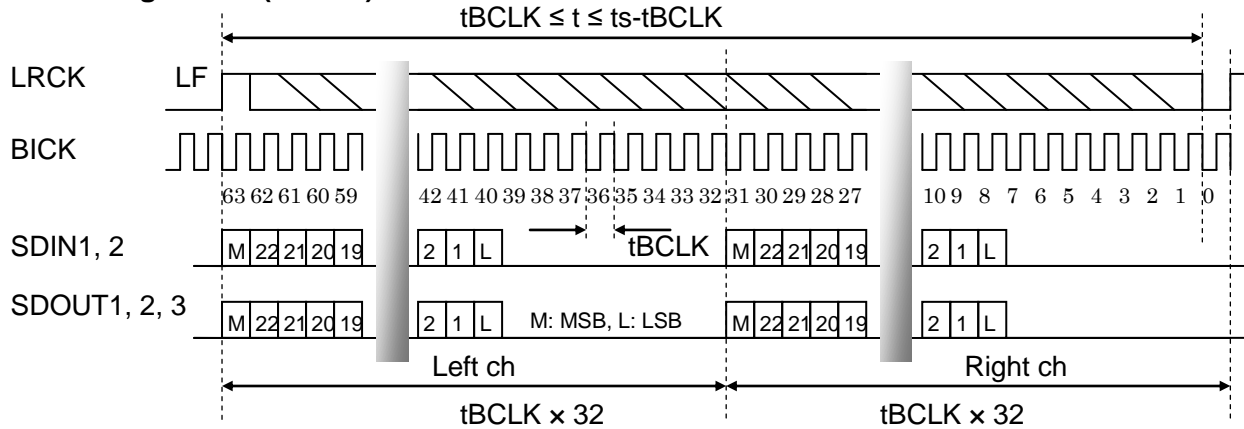
Figure 41. 64fs PCM Long Frame
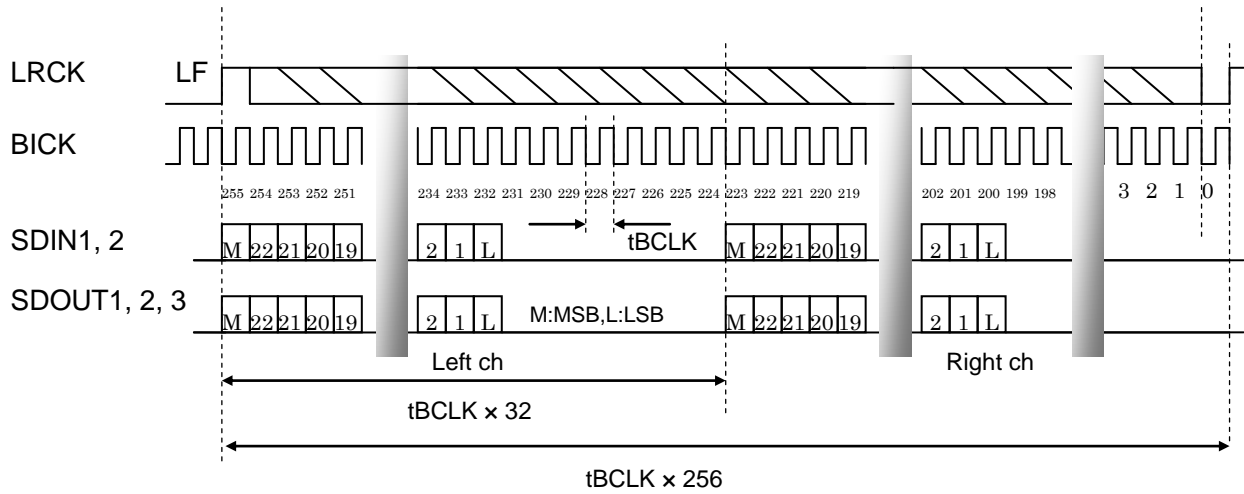
Figure 42. PCM Long Frame 256fs

7. TDM Mode

TDM interface formats shown below are available by setting TDM256 bit = "1". BITFS[1:0] bits should be set to 3h since BICK is fixed to 256fs.

Mode	LRIF[1:0]	TDMMODE[1:0]	Format	Note
0	0h	0h	MSB 24-bit	
1	0h	1h	MSB 24-bit	SLOT7 and 8 Inputs Not Available
2	0h	2h	MSB 24-bit	SLOT5, 6, 7 and 8 Inputs Not Available
3	1h	0h	I^{2}S Compatible	
4	1h	1h	I^{2}S Compatible	SLOT7 and 8 Inputs Not Available
5	1h	2h	I^{2}S Compatible	SLOT5, 6, 7 and 8 Inputs Not Available
6	2h	0h	PCM Short Frame	
7	2h	1h	PCM Short Frame	SLOT7 and 8 Inputs Not Available
8	2h	2h	PCM Short Frame	SLOT5, 6, 7 and 8 Inputs Not Available
9	3h	0h	PCM Long Frame	
10	3h	1h	PCM Long Frame	SLOT7 and 8 Inputs Not Available
11	3h	2h	PCM Long Frame	SLOT5, 6, 7 and 8 Inputs Not Available
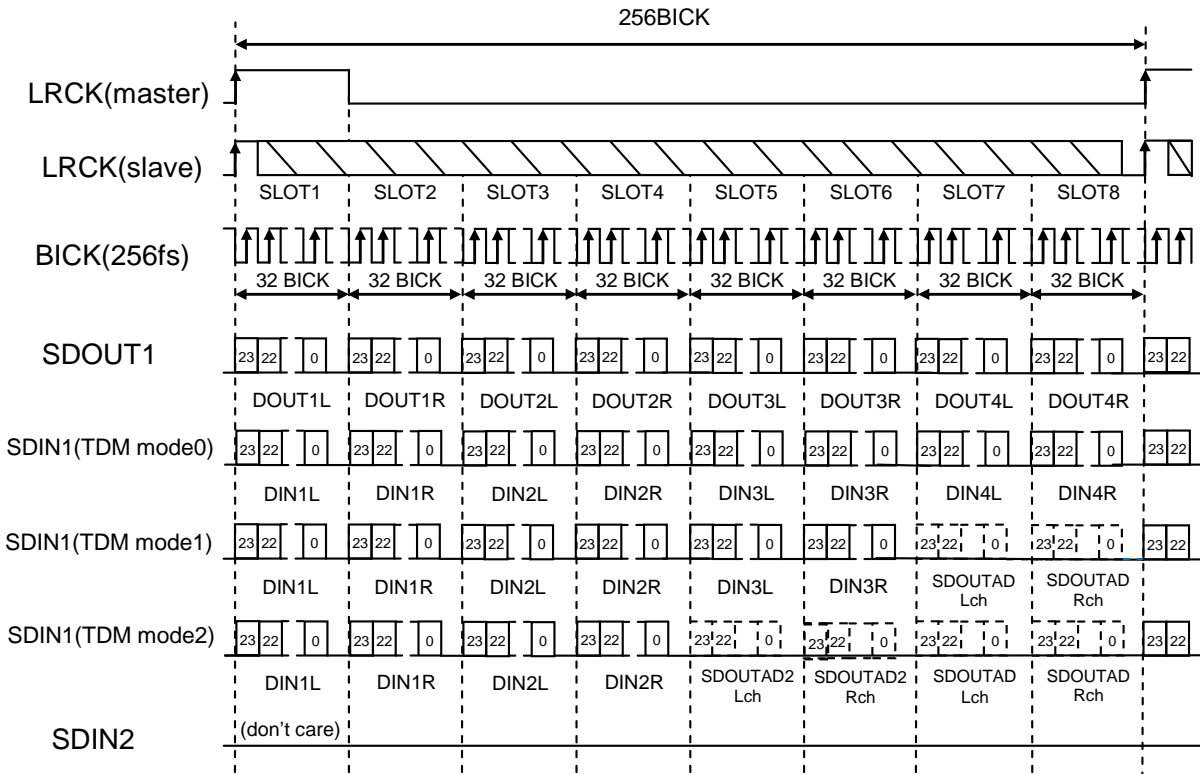
Figure 43. TDM mode MSB Justified 24-bit (Internal signals are indicated by dotted lines)
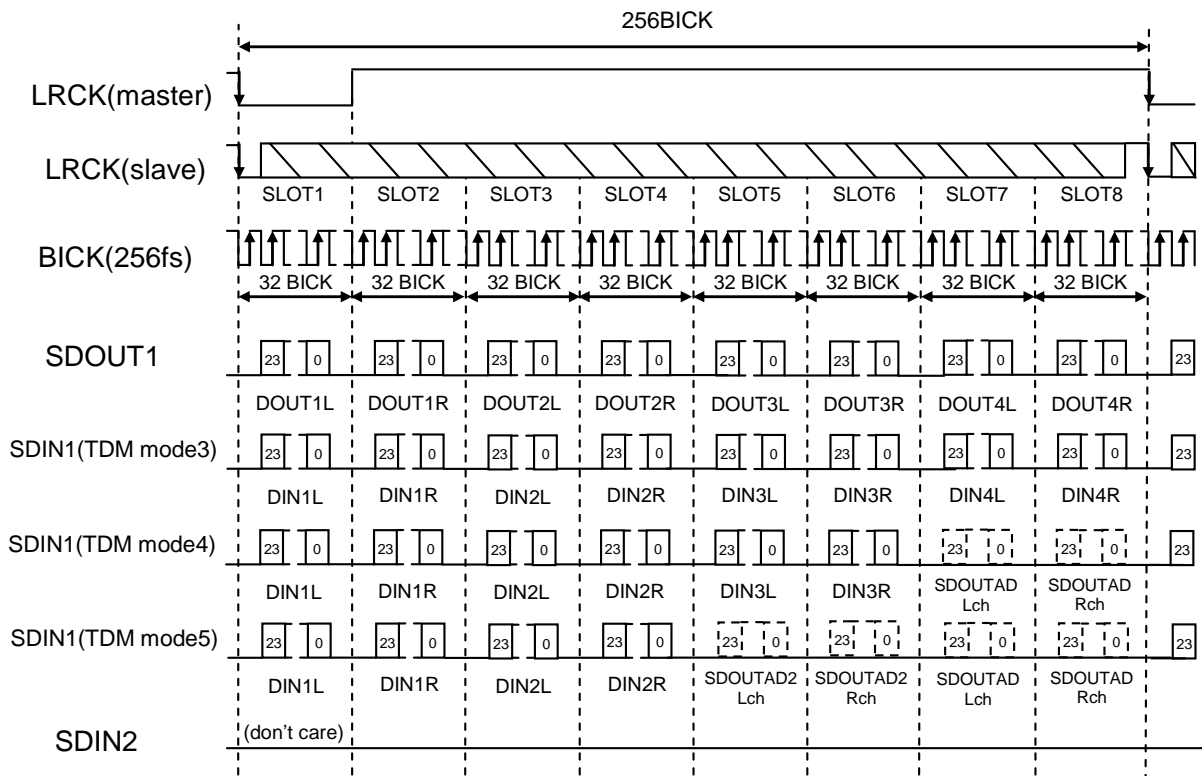
Figure 44. TDM mode I²S Compatible (Internal signals are indicated by dotted lines)
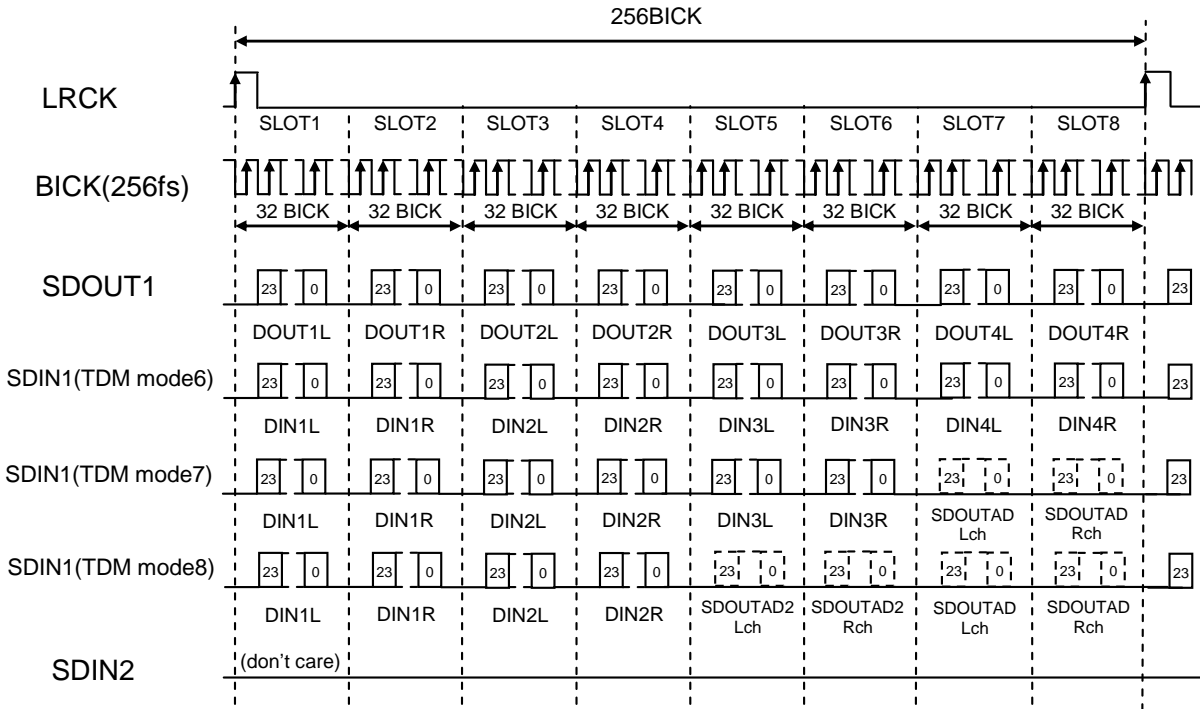
Figure 45. TDM mode PCM Short Frame (Internal signals are indicated by dotted lines)
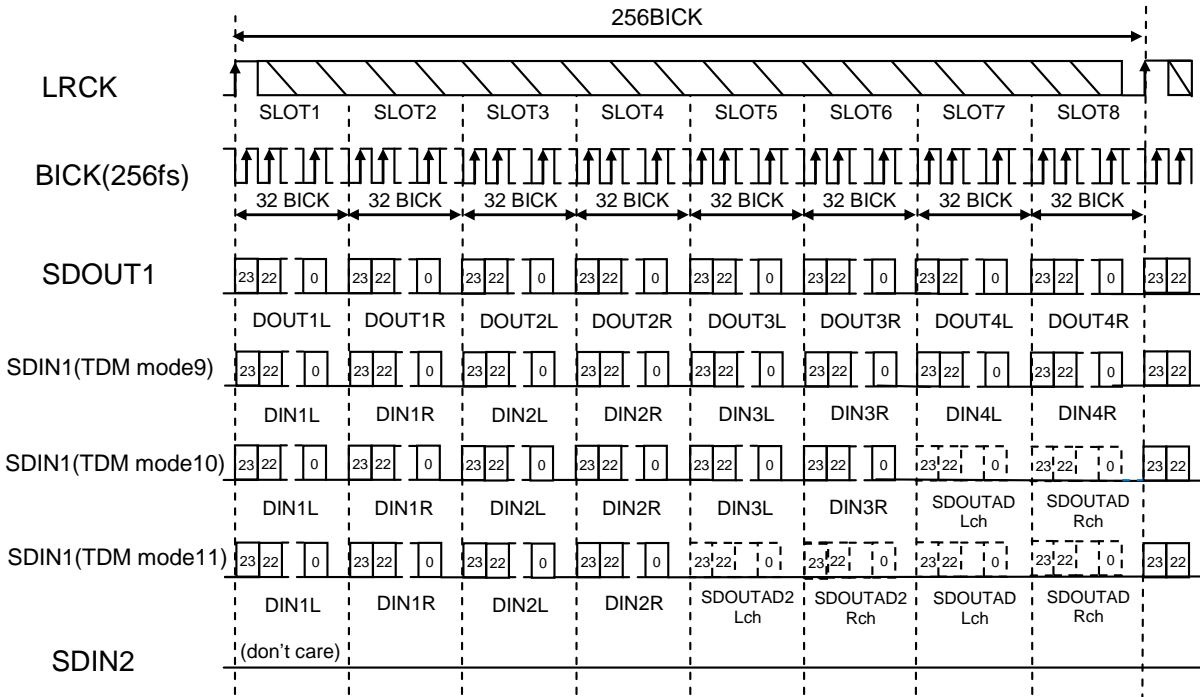
Figure 46. TDM mode PCM Long Frame (Internal signals are indicated by dotted lines)

■ μP Interface Setting and Pin Status

SPI or I²C bus interface mode can be selected by the I2CSEL pin. Pin statuses that are changed by I2CSEL pin setting are shown below.

	I2CSEL	PDN	SO/SDA	SCLK/SCL
SPI Interface	L	L	Hi-Z (CSN pin = "H")	Input
	L	H	Hi-Z (CSN pin = "H") function(CSN pin = "L")	Input
I²C BUS	H	L	"Hi-Z"→ pull-up	"Hi-Z"→ pull-up
	H	H	function	function

Note 49. The CSN pin must be set to "H" when not interfacing to a micro controller or the AK7755 is in power-down mode in SPI interface mode.

■ SPI Interface (I2CSEL pin = "L")

1. Configuration

The access format is: Command code (8bits) + Address + Data (MSB First).

	Bit Length	
Command Code	8	MSB bit is R/W flag. The following 7-bits indicate access area such as PRAM/ CRAM/Registers.
Address	16 or 0	Valid only for those cases where accessed areas have addresses such as PRAM /CRAM/OFREG. When no address is assigned, there is no data.
Data	Later Section	Write or Read data

SOPCFG bit selects SO output (Hi-z or Low) during CSN pin = "H".

•Write operation
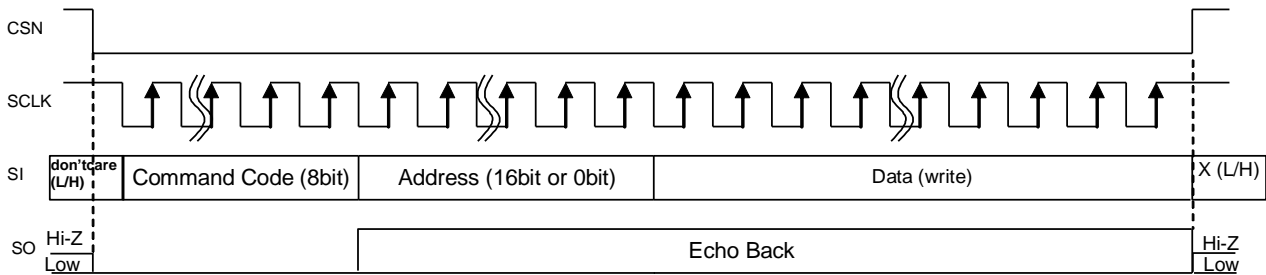
Figure 47. SPI Interface Write

•Read operation
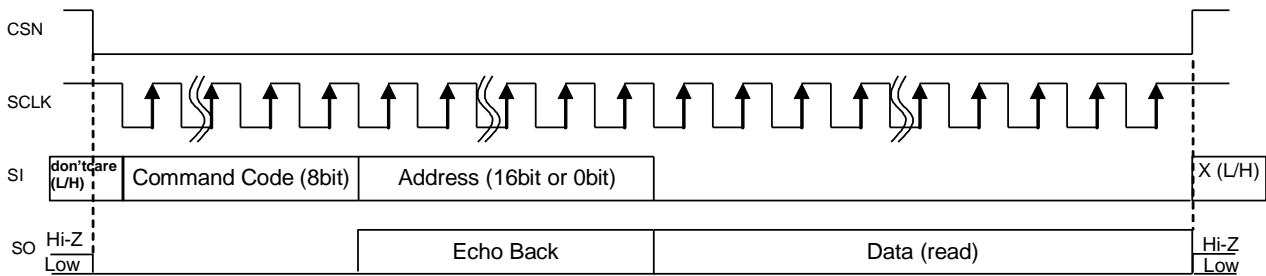
Figure 48. SPI Interface Read

2. Command Code

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R/W flag	Area to be accessed			Accompanying data to the access area			

R/W Flag: Write at "1", Read at "0".

Access data and accompanying data

BIT6	BIT5	BIT4	BIT3~0	
0	0	0	Number of Write	Write preparation to CRAM during RUN
0	0	1	Number of Write	Write preparation to OFREG during RUN
0	1	0	0100	Write operation to CRAM during RUN
			0010	Write operation to OFREG during RUN
0	1	1	1000	Write/Read operation to PRAM during system reset
			0100	Write/Read operation to CRAM during system reset
			0010	Write/Read operation to OFREG during system reset
			1011	Write/Read operation to ACCRAM (Accelerator Coefficient RAM) during system reset
1	0	0	Register Address	Internal control registers 00h~0Fh
1	0	1	Register Address	Internal control registers 10h~1Fh
1	1	0	0000	Device Identification (Read only)
			0110	Internal control registers 26h
			1010	Internal control registers 2Ah
1	1	1	0000	Error Status Read
			0010	CRC Write/Read
			0100	Write operation of JX code
			0110	Read operation from MIR1
			1000	Read operation from MIR2
			1010	Read operation from MIR3
			1100	Read operation from MIR4

3. Address

The address description is always LSB justified. Accessing command code BIT[6:4]= "000" to "011" requires a 16-bit address. Accessing command code BIT[6:4]= "100" to "111" requires no address.

4. Data

The length of write data depends on the write area size. When accessing RAM, data may be written to sequential address locations by writing data continuously.

Write

Command	Address	Data Length	Description
0x80~0x8F	16bit	24bit×n	Write preparation to CRAM during RUN. Command code BIT3~BIT0 bits determines the amount of write operation. (0x80 # of write: 1, 0x81 # of write: 2, ----, 0x8F # of write: 16) If the actual amount of write operations exceeds the defined amount, that data will be ignored.
0x90~0x9F	16bit	24bit×n	Write preparation to OFREG during RUN. Command code BIT3~BIT0 bits determines the amount of write operation. (0x90 # of write: 1, 0x91 # of write: 2, ----, 0x9F # of write: 16) If the actual amount of write operations exceeds the defined amount, that data will be ignored.
0xA2	16bit	None	Write operation to OFREG during RUN. 0 address should be written.
0xA4	16bit	None	Write operation to CRAM during RUN. 0 address should be written.
0xB2	16bit	24bit×n	Write operation to OFREG during system reset
0xB4	16bit	24bit×n	Write operation to CRAM during system reset
0xB8	16bit	40bit×n	Write operation to PRAM during system reset
0xBB	16bit	24bit×n	Write operation to ACCRAM during system reset
0xC0~0xDF	None	8bit	Write operation to Control Registers 00~1Fh
0xE6	None	8bit	Write operation to Control Register 26h
0xEA	None	8bit	Write operation to Control Register 2Ah
0xF2	None	16bit	CRC Write
0xF4	None	8bit	Write operation of External Conditional Jump Code

Data length is defined by the command code which specifies the area to be accessed. When accessing RAM, data may be read from sequential address locations by reading data continuously. Writing other than this command code is prohibited.

Read

Command	Address	Data Length	Description
0x24	16bit	24bit×n	CRAM/OFREG Preparation Data Read during RUN
0x32	16bit	24bit×n	Read operation form OFREG during system reset
0x34	16bit	24bit×n	Read operation from CRAM during system reset
0x38	16bit	40bit×n	Read operation from PRAM during system reset
0x3B	16bit	24bit×n	Read operation from ACCRAM during system reset
0x40~0x5F	None	8bit	Write operation to Control Registers 00~1Fh
0x60	None	8bit	Device Identification
0x66	None	8bit	Write operation to Control Register 26h
0x6A	None	8bit	Write operation to Control Register 2Ah
0x70	None	8bit	DSP Error Status Read
0x72	None	16bit	CRC result Read
0x76	None	32bit	Read operation from MIR1 28-bit is upper-bit justified. Lower 4-bits are for validity flags.
0x78	None	32bit	Read operation from MIR2 28-bit is upper-bit justified. Lower 4-bits are for validity flags.
0x7A	None	32bit	Read operation from MIR3 28-bit is upper-bit justified. Lower 4-bits are for validity flags.
0x7C	None	32bit	Read operation from MIR4 28-bit is upper-bit justified. Lower 4-bits are for validity flags.

Reading other than this command code is prohibited.

5. Echo-Back Mode

The AK7755 has an echo-back mode that the device outputs write data sequentially from the SO pin.

5-1. Write Sequence
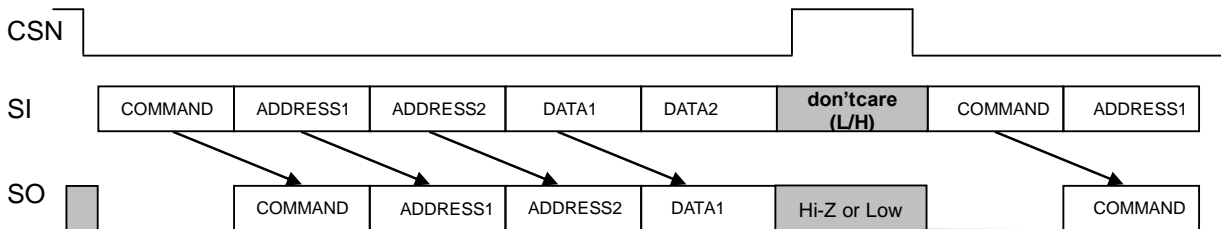
Figure 49. Echo-Back Writing 1 (SPI)

The input data of the SI pin is echoed back on the SO pin by shifting 8-bit to the right.
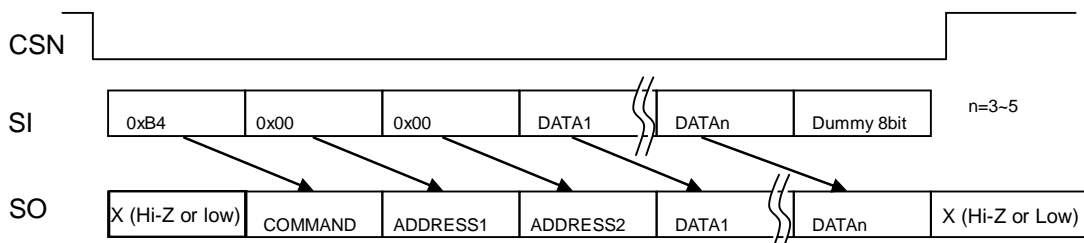
Figure 50. Echo-Back Writing 2 (SPI)

It is possible to verify the written data by inputting an extra 8-bit clock. If the dummy data is more than the data length, this dummy data is written on the next address. (40 bits for PRAM, 24 bits for CRAM and 24 bits for OFREG writings)

5-2. Read Sequence1 (with PRAM, CRAM, OFREG addresses)
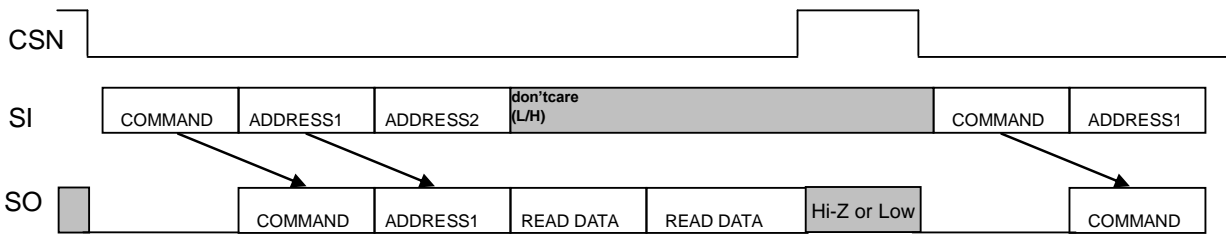
Figure 51. Read Sequence1 in Echo-Back Mode (SPI)

Data of the address2 field is not echoed back in read operation. The read data on the SO pin is output after writing to the address2 field.

5-3. Read Sequence2 (No Register address)
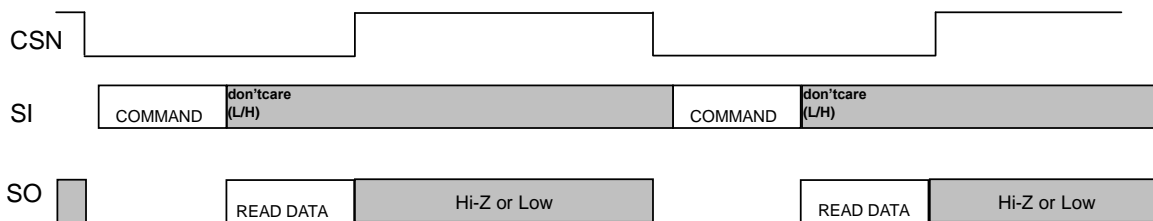
Figure 52. Read Sequence2 in Echo Back Mode (SPI)

Data output has priority in read sequence.

6. Format

6-1. Write Operation during System Reset

1. Program RAM (PRAM) Write (during system reset)

Field	Write data
(1) COMMAND Code	0xB8
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 0 0 0 0 0
(4) DATA1	0 0 0 0 D35 D34 D33 D32
(5) DATA2	D31~D24
(6) DATA3	D23~D16
(7) DATA4	D15~D8
(8) DATA5	D7~D0
	Five bytes of data may be written continuously for each address.

2. Coefficient RAM (CRAM) Write (during system reset)

Field	Write data
(1) COMMAND Code	0xB4
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8
(3) ADDRESS2	A7 A6 A5 A4 A3 A2 A1 A0
(4) DATA1	D23~D16
(5) DATA2	D15~D8
(6) DATA3	D7~D0
	Three bytes of data may be written continuously for each address.

3. Offset REG (OFREG) Write (during system reset)

Field	Write data
(1) COMMAND Code	0xB2
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 A5 A4 A3 A2 A1 A0
(4) DATA1	0 0 0 0 0 0 0 0
(5) DATA2	0 0 0 D12 D11 D10 D9 D8
(6) DATA3	D7~D0
	Three bytes of data may be written continuously for each address.

4. Accelerator Coefficient RAM (ACCRAM) Write (during system reset)

Field	Write data
(1) COMMAND Code	0xBB
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8
(3) ADDRESS2	A7 A6 A5 A4 A3 A2 A1 A0
(4) DATA1	D19~D12
(5) DATA2	D11~D4
(6) DATA3	D3~D0 0 0 0 0
	Three bytes of data may be written continuously for each address.

6-2. Write Operation during System Reset / RUN

1. Control Register Write (during system reset / RUN)

Field	Write data
(1) COMMAND Code	0xC0~0xDF, 0xE6, 0xEA
(2) DATA	D7~D0

2. External Conditional Jump Code Write (during system reset / RUN)

Field	Write data
(1) COMMAND Code	0xF4
(2) DATA	D7~D0

3. CRC Code Write (during system reset / RUN)

Field	Write data
(1) COMMAND Code	0xF2
(2) DATA	D15~D8
(3) DATA	D7~D0

6-3. Write Operation during RUN

1. Coefficient RAM (CRAM) Write Preparation (during RUN)

Preparation	Write data
(1) COMMAND Code	0x80~0x8F (one data at 80h, sixteen data at 8Fh)
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8
(3) ADDRESS2	A7 ~ A0
(4) DATA1	D23~D16
(5) DATA2	D15~D8
(6) DATA3	D7~D0

2. Coefficient RAM (CRAM) Write Operation (RUN)

Execute	Write data
(1) COMMAND Code	0xA4
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 0 0 0 0 0

Note 50. The COMMAND determines the length of the data. If the written data exceeds the allotted amount, the excess data is ignored.

3. Offset REG (OFREG) Write Preparation (during RUN)

Preparation	Write data
(1) COMMAND Code	0x90~0x9F (one data at 0x90, sixteen data at 0x9F)
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 A4 A3 A2 A1 A0
(4) DATA1	0 0 0 0 0 0 0 0
(5) DATA2	0 0 0 D12 D11 D10 D9 D8
(6) DATA3	D7~D0

4. Offset REG (OFREG) Write Operation (during RUN)

Execute	Write data
(1) COMMAND Code	0xA2
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 0 0 0 0 0

Note 51. The COMMAND determines the length of the data. If the written data exceeds the allotted amount, the excess data is ignored.

6-4. Read Operation during System Reset

1. Program RAM (PRAM) Read (during system reset)

Field	Write data	Readout data
(1) COMMAND Code	0x38	
(2) ADDRESS1	0 0 0 0 0 0 0 0	
(3) ADDRESS2	0 0 0 0 0 0 0 0	
(4) DATA1		0 0 0 0 D35 D34 D33 D32
(5) DATA2		D31~D24
(6) DATA3		D23~D16
(7) DATA4		D15~D8
(8) DATA5		D7~D0
	Five bytes of data may be written continuously for each address.	

2. Coefficient RAM (CRAM) Read (during system reset)

Field	Write data	Readout data
(1) COMMAND Code	0x34	
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8	
(3) ADDRESS2	A7 ~ A0	
(4) DATA1		D23~D16
(5) DATA2		D15~D8
(6) DATA3		D7~D0
	Three bytes of data may be written continuously for each address.	

3. Offset REG (OFREG) Read (during system reset)

Field	Write data	Readout data
(1) COMMAND Code	0x32	
(2) ADDRESS1	0 0 0 0 0 0 0 0	
(3) ADDRESS2	0 0 0 A4 A3 A2 A1 A0	
(4) DATA1		0 0 0 0 0 0 0 0
(5) DATA2		D15~D8
(6) DATA3		D7~D0
	Three bytes of data may be written continuously for each address.	

4. Accelerator Coefficient RAM (ACCRAM) Read (during system reset)

Field	Write data	Readout data
(1) COMMAND Code	0x3B	
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8	
(3) ADDRESS2	A7 ~ A0	
(4) DATA1		D19~D12
(5) DATA2		D11~D4
(6) DATA3		D3~D0 0 0 0 0
	Three bytes of data may be written continuously for each address.	

6-5. Read Operation during System Rest / RUN

1. Control Register Read (during system reset / RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x40~0x5F, 0x66, 0x6A	
(2) DATA		D7~D0

2. Device Identification (during system rest / RUN)

Field	Write data	Readout data							
(1) COMMAND Code	0x60								
(2) DATA		D7	D6	D5	D4	D3	D2	D1	D0
		0	1	0	1	0	1	0	1
		5				5			

3. CRC Result Reading (during system reset / RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x72	
(2) DATA1		D15~D8
(3) DATA2		D7~D0

4. DSP Error Status Read (during system reset / RUN)

Field	Write data	Output
(1) COMMAND Code	0x70	
(2) DATA		Active low output D7: CRCERRN: 0: CRC error D6: WDTERRN : 0: Watch Dog Timer error D5: GP0 0:clear 1: set D4: GP1 0:clear 1: set D3: PLLLOCK 0:unlock 1:lock D2: N/A D1: N/A D0: N/A

6-6. Read Operation during RUN

1. CRAM Write Preparation Read (during RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x24	
(2) ADDRESS1		A15~A8
(3) ADDRESS2		A8~A0
(4) DATA1		D23~D16
(5) DATA2		D15~D8
(6) DATA3		D7~D0

2. OFREG Write Preparation Read (during RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x24	
(2) ADDRESS1		A15~A8
(3) ADDRESS2		A8~A0
(4) DATA1		0 0 0 0 0 0 0 0
(5) DATA2		D15~D8
(6) DATA3		D7~D0

3. MIR1/2/3/4 Read   (during RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x76(MIR1) 0x78(MIR2) 0x7A(MIR3) 0x7C(MIR4)	
(2) DATA1		D27~D20
(3) DATA2		D19~D12
(4) DATA3		D11~D4
(5) DATA4		D3 D2 D1 D0 (flag3) (flag2) (flag1) (flag0)

Note 52. Data is valid only when all flags are zero.

7. Timing

7-1. RAM Writing Timing during System Reset

Write to Program RAM (PRAM), Coefficient RAM (CRAM), Offset REG (OFREG) and Accelerator Coefficient RAM (ACCRAM) during system reset in the order of command code, address and data. The PRAM start address is fixed to 0h. When writing the data to consecutive address locations, continue to input data only. PRAM address is incremented by 1 automatically.
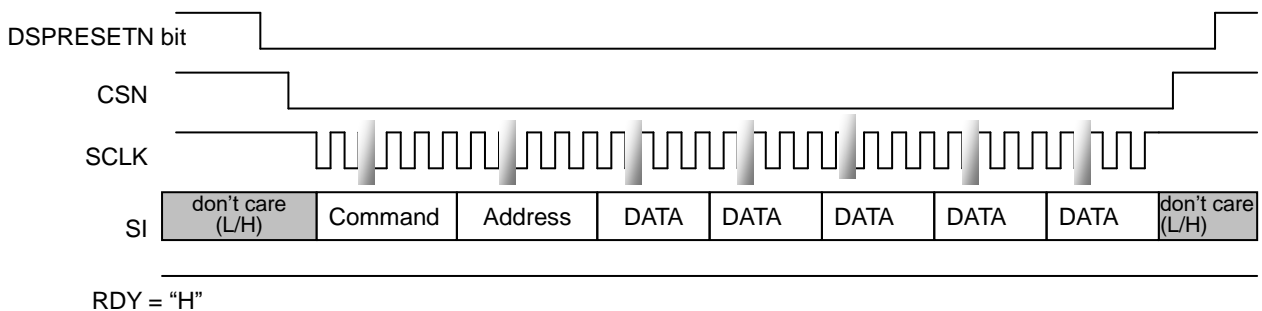
Figure 53. Writing to RAM at Consecutive Address Locations (SPI)
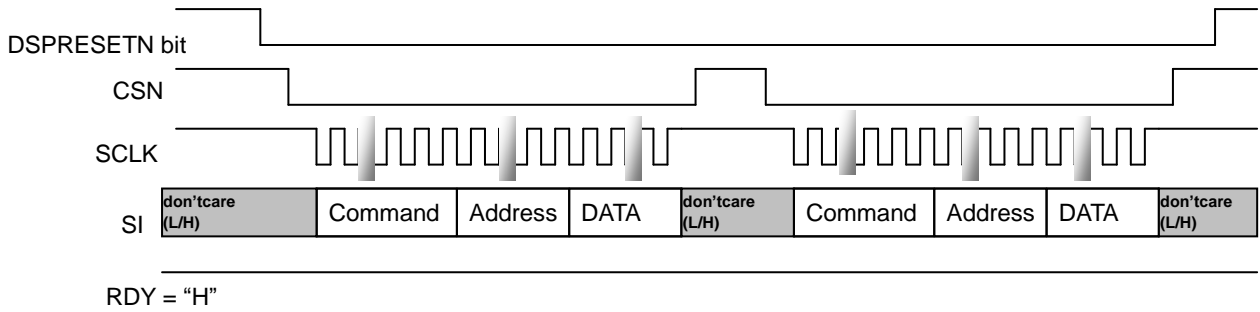
Figure 54. Writing to RAM at Random Address Locations (SPI)

7-2. RAM Writing Timing during RUN

These operations are to rewrite the Coefficient RAM (CRAM) and Offset REG (OFREG) during RUN. Data writing is executed in two steps; write preparation and write execution. The written data can be confirmed by reading the write preparation data.

1. Write Preparation
   After inputting the assigned command code (8 bits) to select the number of data from 1 to 16, input the starting address of write (16 bits all "0") and the number of data assigned by command code in this order. In slave mode, a write preparation command is prohibited for "2 LRCK" cycles (2/fs) after releasing DSP reset (DSPRESETN bit).

2. Write Preparation Data Confirmation
   After write preparation, prepared data for writing can be confirmed. Address and Data are read in this order by write preparation data confirmation command "24h". The data will be "0x000001" when reading more than write preparation data. Execute write preparation again when the address and data are disturbed by external noise.

3. Write Execution
   Upon completion of this operation, execute a RAM write during RUN by inputting the corresponding command code and address (16 bits, all "0") in this order.

Note 53. Execute write preparation, write preparation read and write execution in this order. When writing to RAM without a write preparation sequence, a malfunction occurs. Access operation by a microcontroller is prohibited until RDY changes to "H".

Write modification of the RAM content is executed whenever the RAM address for modification is assigned. For example, when 5 data are written, from RAM address "10", it is executed as shown below.

RAM execution address	7	8	9	10	11	13	16	11	12	13	14	15
				↓	↓				↓	↓	↓	
Write execution position				○	○	↑			○	○	○	
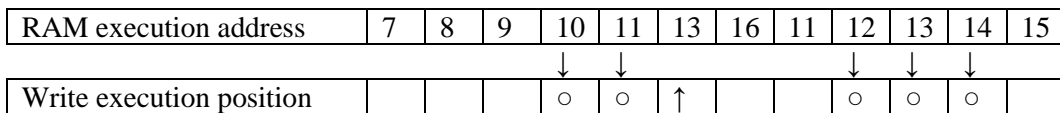
Note 54. Address "13" is not executed until rewriting address "12".

DSPRESETN bit= "1"

CSN

(Ex.) When # of DATA is 4

SCLK

CRAM Command Code 0x83
OFREG Command Code 0x93

SI | don't care (L/H) | Command Code | Address | DATA0 | DATA1 | DATAn-1 | DATAn | don'tcare (L/H)

RDY = "H"

CRAM   0x80(# of DATA: 1)~0x8F(# of DATA: 16)

OFREG   0x90(# of DATA: 1)~0x9F(# of DATA: 16)
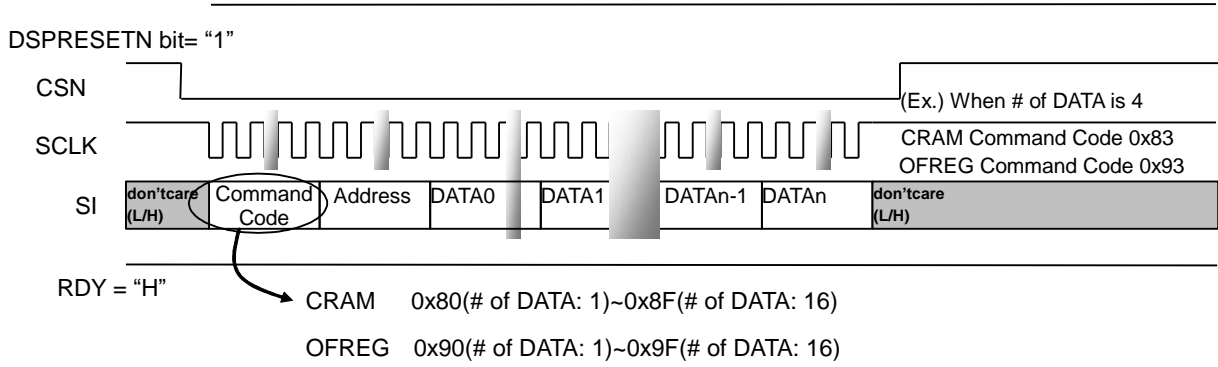
Figure 55. CRAM/OFREG Write Preparation (SPI)

DSPRESTN bit= "1"

CSN

SCLK

SI | don't care (L/H) | 0x24 | don't care (L/H)

SO   Hi-Z or Low
------- | Address | DATA | DATA | DATA | DATA | DATA | ------

RDY= "H"
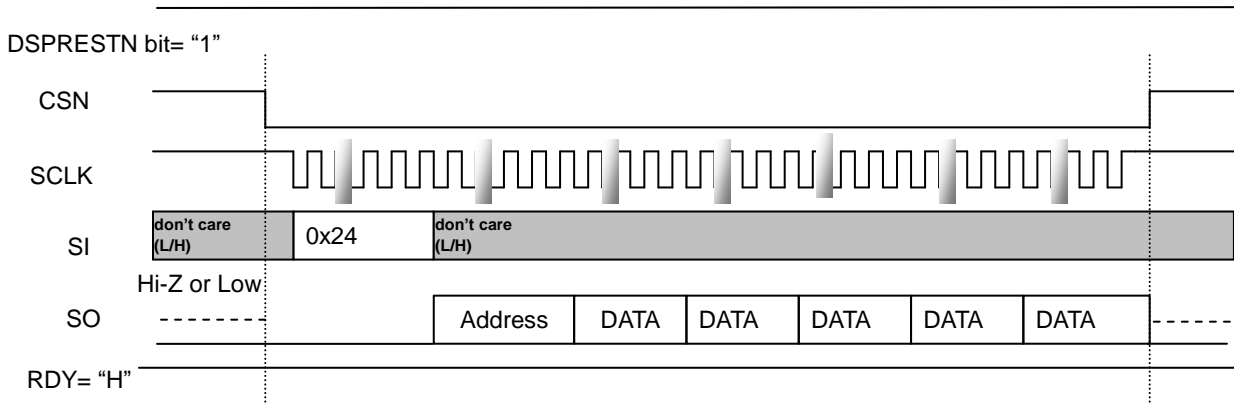
Figure 56. CRAM/OFREG Write Preparation Confirm (SPI)

DSPRESETN bit= "1"

CSN

SCLK

SI | don'tcare (L/H) | Command | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 |

CRAM:0xA4, OFREG:0xA2

max 400ns

RDY

RDYLG (Note 55)
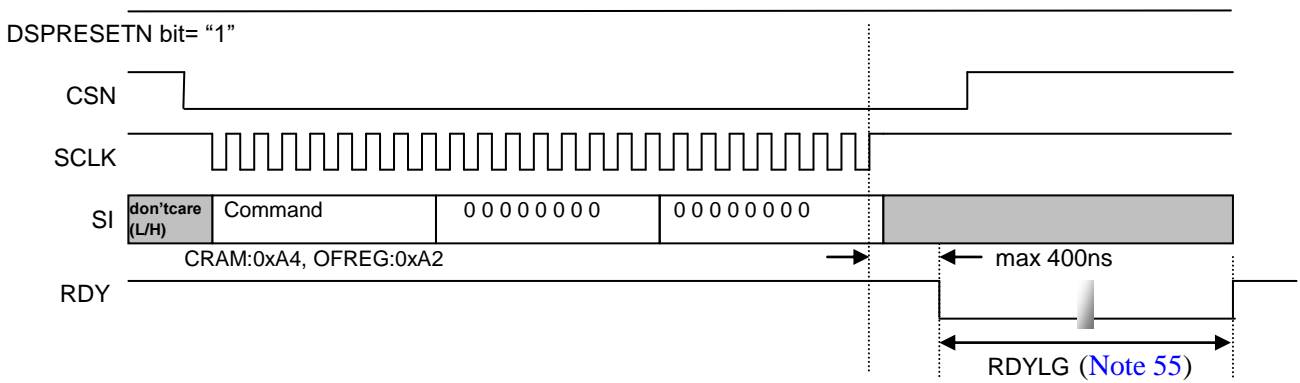
Figure 57. CRAM/OFREG Write (SPI)

Note 55. If the DSP program is designed to refer all coefficients which may be changed by an external microcontroller, RDY signal rises to high within 2LRCK after a writing command. No further access to DSP is permitted until this write operation is completed. However, while the CSN pin is "L" level, RDY signal keeps "L" level.

7-3. External Conditional Jump

External Conditional Jump Code Writing (during System Reset and RUN)

(1) COMMAND	0xF4
(2) DATA	D7~D0

External Conditional Jump code can be input during both DSP Reset and RUN. Input data is set to the designated register on the rising edge of LRCK. The RDY pin changes to "L" when the command code is transferred, and it changes to "H" when write operations are completed. When any single bit of "1" data in 8-bit External Jump code matches an "1" bit data in the IFCON field, a Jump instruction is executed. Then, the RDY pin changes to "H" when the rise of LRCK is captured. Access operation by microcontroller is prohibited until the RDY pin changes to "H". IFCON field is the area where the external conditions are written. This Jump code is reset to 00h by setting the PDN pin to "L", but it is not reset by System Reset.

```
                                 7   6   5   4   3   2   1   0
External Conditional Jump Code   ■   ■   ■   ■   ■   ■   ■   ■
                                             ↑
```

Check if "1" of IFCON field corresponds with External Conditional Jump including Jump pins by at least one at the same location.

```
                                 7           ↓               0
IFCON Field                      ♦   ♦   ♦   ♦   ♦   ♦   ♦   ♦
External Conditional Jump Code   ■   ■   ■   ■   ■   ■   ■   ■
```
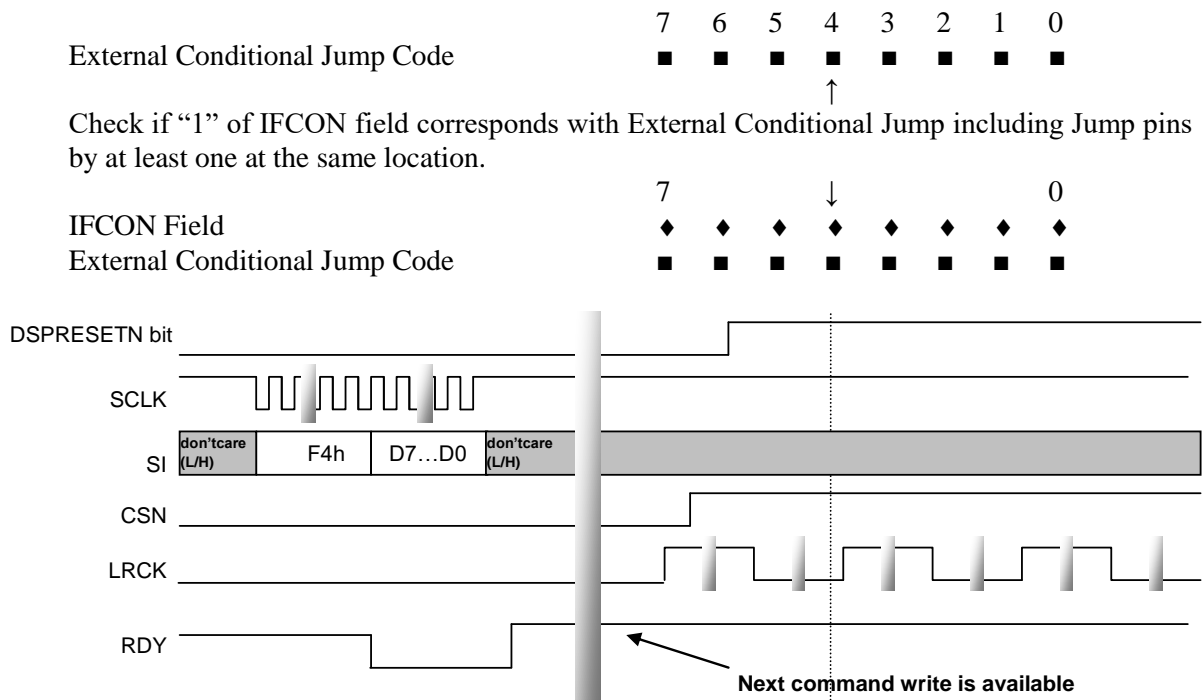

Figure 58. External Conditional Timing in System Reset (SPI)
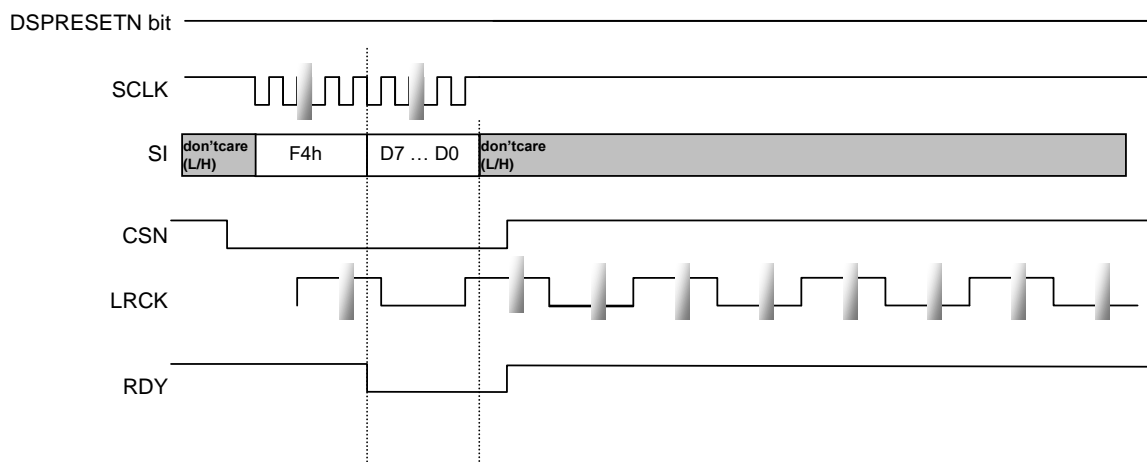
Figure 59. External Conditional Jump Timing during RUN (SPI)

7-4. RAM Reading Timing during System Reset

Read Program RAM (PRAM), Coefficient RAM (CRAM), Offset REG (OFREG) and Accelerator Coefficient RAM (ACCRAM) during System Reset in the order of the input Command code and the Address. After writing the Command, the data comes out from the SO pin synchronous with falling edge of SCLK. (The SI pin input data is "Don't care") When reading Data at consecutive address locations, continue to input SCLK as is.
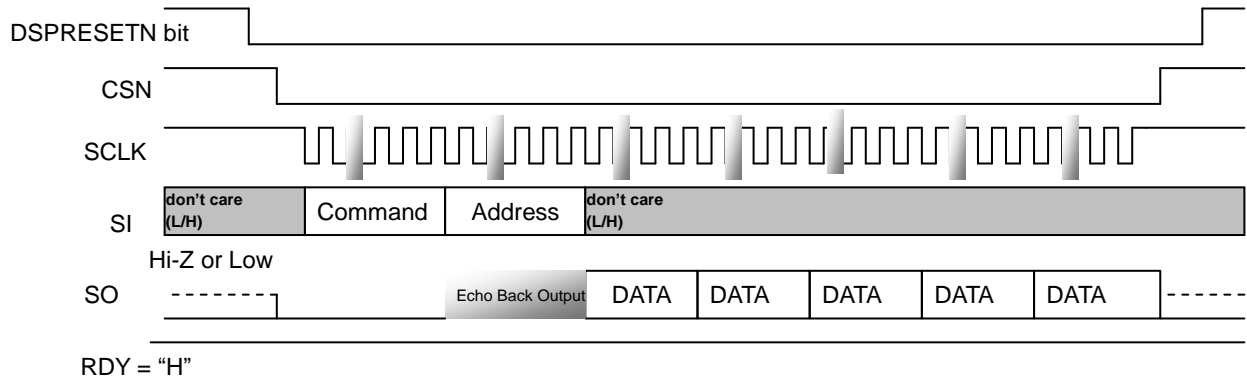

Figure 60. RAM Reading at Consecutive Address (SPI)

7-5. RAM Reading Timing during System Reset and RUN

Write a command code, to read control registers, device identification code, CRC result and error status during RUN time or system reset state. After completing a Command code write, the data comes out from the SO pin synchronous with falling edge of SCLK. (The SI pin input data is "Don't care")
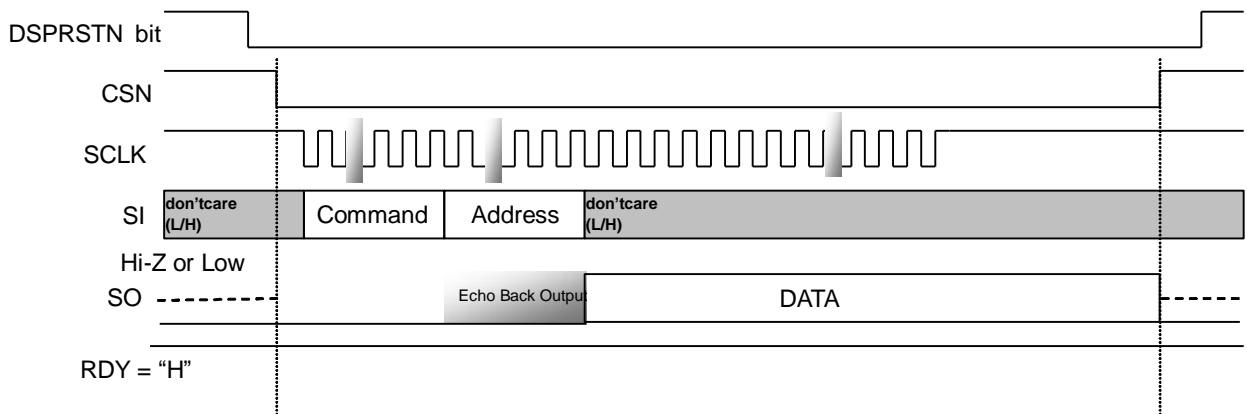
Figure 61. RAM Reading during System Reset/RUN (SPI)

■ I²C Bus Interface (I2CSEL pin= "H")

Access to the AK7755 registers and RAM is controlled by an I²C bus. The AK7755 supports fast-mode I²C-bus (max: 400kHz) only.

1. Data Transfer

In order to access any IC devices on the I²C bus, input a start condition first, followed by a single Slave address which includes the Devices Address. IC devices on the BUS compare this Slave address with their own addresses and the IC device which has an identical address with the Slave address generates an acknowledgement. An IC device with the identical address then executes either a read or a write operation. After the command execution, input a Stop condition.

1-1. Data Change

Change the data on the SDA line while the SCL line is "L". The SDA line condition must be stable and fixed while the clock is "H". Change the Data line condition between "H" and "L" only when the clock signal on the SCL line is "L". Change the SDA line condition while the SCL line is "H" only when the start condition or stop condition is input.
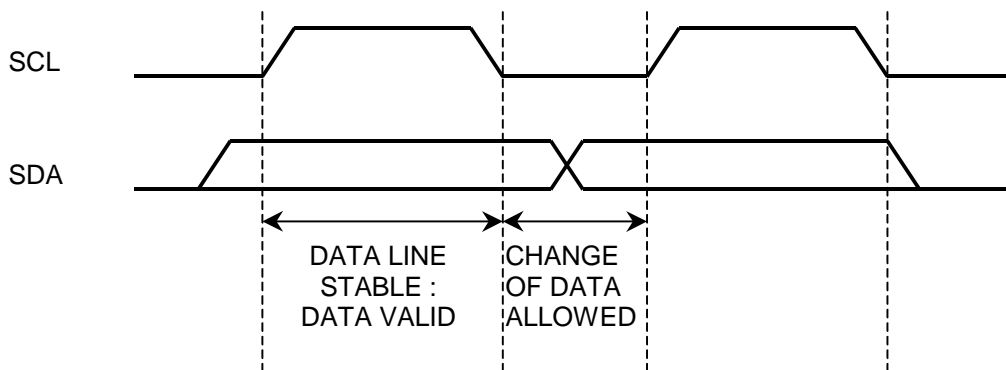
Figure 62. Data Change (I²C)

1-2. Start Condition and Stop Condition

A start condition is generated by the transition of "H" to "L" on the SDA line while the SCL line is "H". All instructions are initiated by a Start condition. A stop condition is generated by the transition of "L" to "H" on the SDA line while the SCL line is "H". All instructions end by a Stop condition.
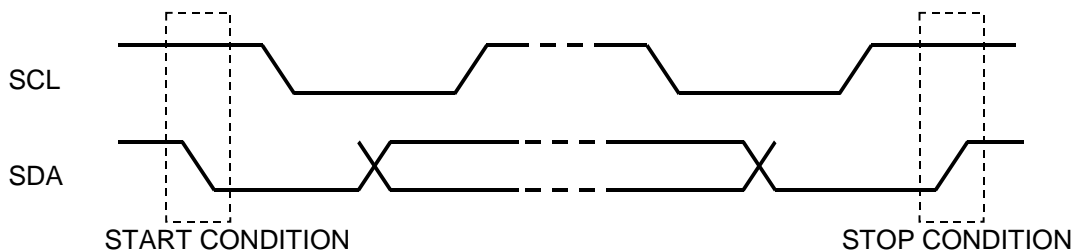
Figure 63. Start Condition and Stop Condition (I²C)

1-3. Repeated Start Condition

When a Start condition is received again instead of a Stop condition, the bus changes to a Repeated Start condition. A Repeated Start condition is functionally the same as a Start condition.
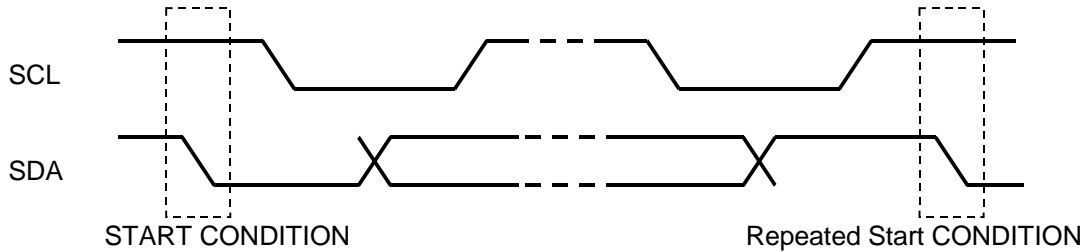

Figure 64. Repeated Start Conditions (I^2C)

1-4. Acknowledge

An external device that is sending data to the AK7755 releases the SDA line ("H") after receiving one byte of data. An external device that receives data from the AK7755 then sets the SDA line to "L" at the next clock. This operation is called "acknowledgement", and it enables verification that the data transfer has been properly executed. The AK7755 generates an acknowledgement upon receipt of a Start condition and a Slave address. For a write instruction, an acknowledgement is generated whenever receipt of each byte is completed. For a read instruction, succeeded by generation of an acknowledgement, the AK7755 releases the SDA line after outputting data at the designated address, and it monitors the SDA line condition. When the Master side generates an acknowledgement without sending a Stop condition, the AK7755 outputs data at the next address location. When no acknowledgement is generated, the AK7755 ends data output (not acknowledged).
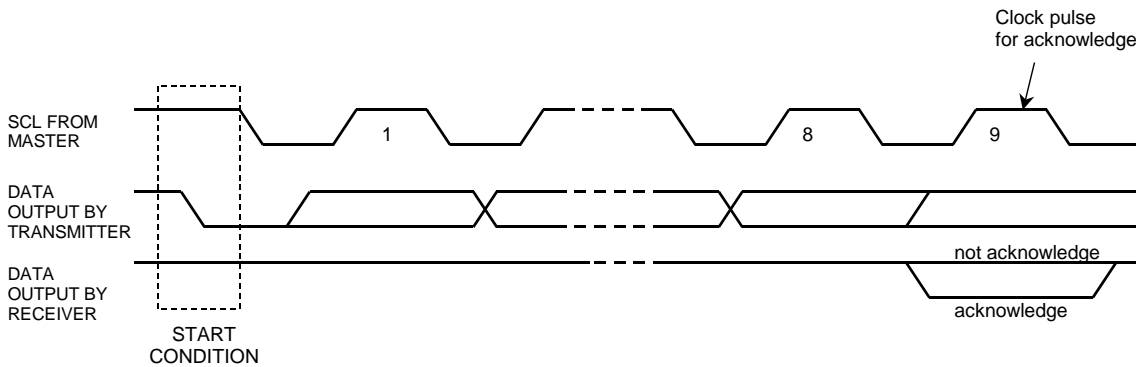
Figure 65. Generation of Acknowledgement (I^2C)

1-5. The First Byte

The First Byte, which includes the Slave-address, is input after the Start condition is set, and a target IC device that will be accessed on the bus is selected by the Slave-address. The Slave-address is configured with the upper 7-bits. When the I2CSEL pin = "H" and the EXTEEP pin = "L", data of the upper 6-bits is "001100". The next 1 bit is the address bits that select the desired IC which are set by the CAD pin. The slave address will be "0011000" when the I2CSEL pin ="H" and the EXTEEP pin = "H". However, if downloading from EEPROM by DLS bit, it should be set the I2CSEL pin = "H", the EXTEEP pin = "L" and the CAD pin = "L" and use the slave address as "0011000".

When the Slave-address is inputted, an external device that has the identical device address generates an acknowledgement and instructions are then executed. The 8th bit of the First Byte (lowest bit) is allocated as the R/W Bit. When the R/W Bit is "1", the read instruction is executed, and when it is "0", the write instruction is executed.

Note 56. In this document, there is a case that describes a "Write Slave-address assignment" when both address bits match and a Slave-address at R/W Bit = "0" is received. There is a case that describes "Read Slave-address assignment" when both address bits matches and a Slave-address at R/W Bit = "1" is received.

0	0	1	1	0	0	CAD	R/W

When I2CSEL pin = "H" and EXTEEP pin = "L"

0	0	1	1	0	0	0	R/W

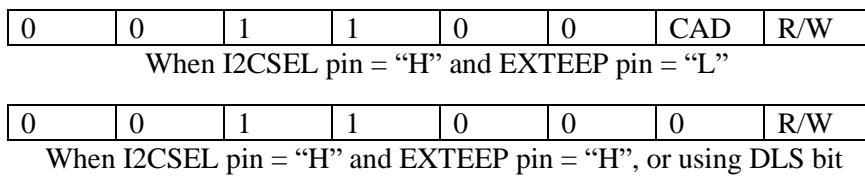When I2CSEL pin = "H" and EXTEEP pin = "H", or using DLS bit

Figure 66. First Byte Configuration (I²C)

1-6. The Second and Succeeding Bytes

The data format of the second and succeeding bytes of the AK7755 Transfer / Receive Serial data (command code, address and data in microcontroller interface format) on the I²C BUS are all configured with a multiple of 8-bits. When transferring or receiving those data on the I²C BUS, they are divided into an 8-bit data stream segment and they are transferred / received with the MSB side data first with an acknowledgement in-between.

Example)
When transferring / receiving A1B2C3 (hex) 24-bit serial data in microprocessor interface format:

(1) Microcontroller Interface Format   (2) I²C Format
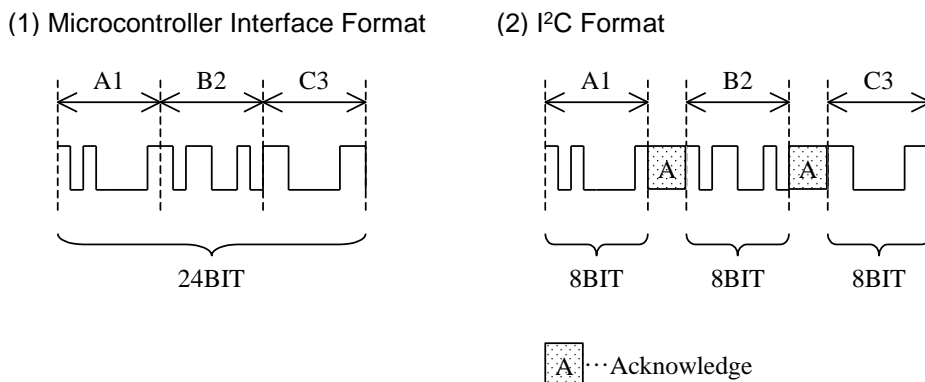

A ···Acknowledge

Figure 67. Division of Data (I²C)

Note 57. In this document, there is a case that describes a write instruction command code which is received at the second byte as "Write Command". There is a case that describes a read instruction command code which is received at the second byte as "Read Command".

2. Write Sequence

In the AK7755, when a "Write-Slave-address assignment" is received at the first byte, the write command at the second byte and data at the third and succeeding bytes are received. At the data block, address and write data are received in a single-byte unit each in accordance with a command code. The number of write data bytes is fixed by the received command code.
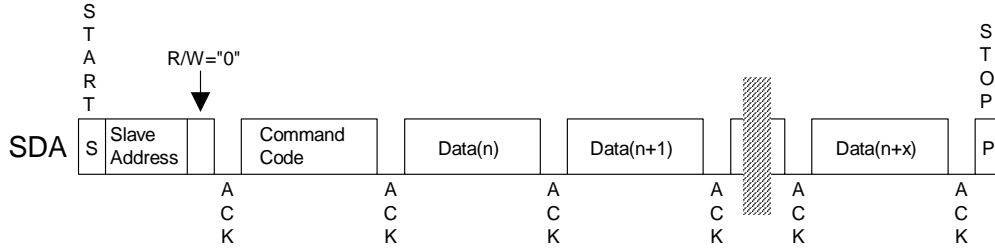
Figure 68. Write Sequence (I^{2}C)

3. Read Sequence

In the AK7755, when a "write- slave-address assignment" is received at the first byte, the read command at the second byte and the data at the third and succeeding bytes are received. At the data block, the address is received in a single byte unit in accordance with a read command code. When the last address byte (or command code if no address assignment is specified) is received and an acknowledgement is transferred, the read command waits for the next restart condition. When a "read slave-address assignment" is received at the first byte, data is transferred at the second and succeeding bytes. The number of readable data bytes is fixed by the received read command.

After reading the last byte, assure that a "not acknowledged" signal is received. If this "not acknowledged" signal is not received, the AK7755 continues to send data regardless whether data is present or not, and since it does not release the BUS, the stop condition cannot be properly received.
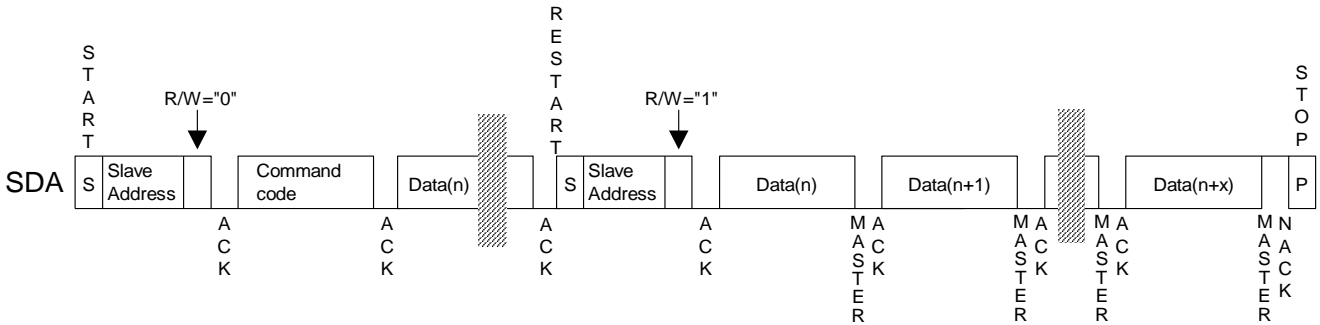
Figure 69. Read Sequence (I^{2}C)

4. Acknowledgement Polling

The AK7755 cannot receive instructions while the RDY pin (Data Write Ready pin) is at low level. The maximum transition time of the RDY pin from low level to high level is 2/fs (fs: sampling frequency), but it is possible to confirm in a faster cycle that the RDY pin has become high by checking the AK7755 internal condition, which is made by verifying the acknowledgement.

4-1. Generation of "Not Acknowledged"

The AK7755 does not accept command codes until the RDY pin is set to a high level, when a command is received to set the RDY pin to a low level. In order to confirm the RDY pin condition, a "Write Slave-Address assignment" should be sent after a Start condition. If the RDY pin is then at a low level, "Acknowledgement" is not generated at the succeeding clock (generation of "Not Acknowledged"). After sending "Not Acknowledged", the BUS is released and all receiving data are ignored until the next start condition (behaves as if it received Slave address of other device).

4-2. When Read Slave-address assignment is received without receiving read command code

Data read in the AK7755 can be made only in the previously documented Read sequence. Data cannot be read out without receiving a read command code. The AK7755 generates a "Not Acknowledged" when a "Read Slave-address Assignment" is received without proper receipt of read command.

5. Limitation in use of I²C Interface

The I2C interface does not support the following features.
No operation in Hs Mode (max:3.4MHz). The AK7755 Supports FAST mode (max:400KHz).

Note 58. Do not turn off the power of the AK7755 whenever the power supplies of other devices of the same system are turned on. The source of the pull-up of SDA and SCL of I²C BUS must not exceed the TVDD. (The diode exists for TVDD in the SDA and SCL pins.)

■ Analog Input Block

1. Microphone Input Selector

Either analog input or digital microphone interface can be chosen for the AK7755. Set AINE bit (CONT00: D3) to "1" when using #31-34 pins as analog input pins, and set DMIC1(CONT1E: D7) or DMIC2 bit (CONT1E: D4) to "1" when using these pins as digital microphone interface. ADC input signals can be switched by DIFL bit (CONT09: D5), DIFR bit (CONT09: D7), INL bit (CONT09: D4) and INTR bit (CONT09: D6) for analog inputs. When DIFL bit = "0" and DIFR bit = "0", input signals of IN1, IN2, IN3 and IN4 pins for microphone amplifiers can be selected by INL and INR bits. When DIFL bit = "1" and DIFR bit = "1", a differential input is acceptable as input pins becomes INP1/INN1 pins and INP2/INN2 pins.
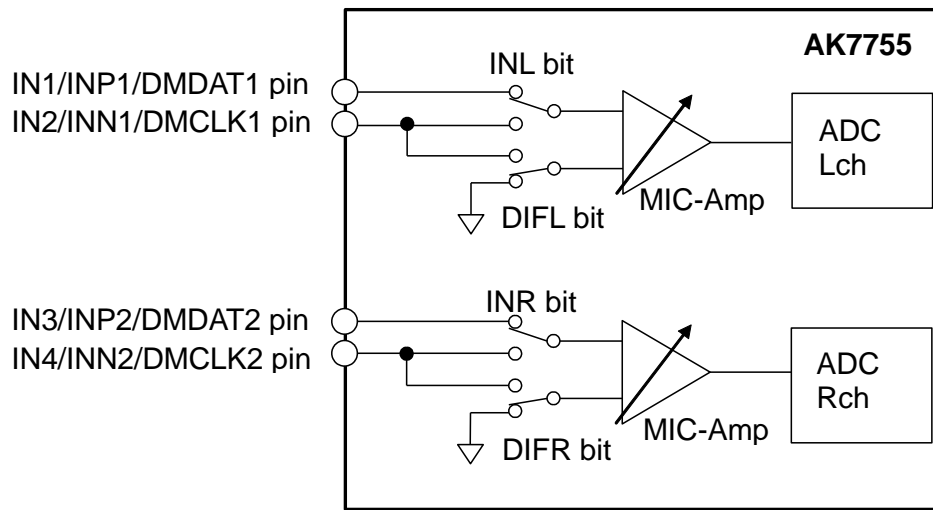

Figure 70. Microphone Input Selector

ADC Lch Microphone Input Selector

DIFL bit	INL bit	ADC Lch
0	0	IN1
0	1	IN2
1	X	INP1/INN1

(default)

(x: Do not care)

ADC Rch Microphone Input Selector

DIFR bit	INR bit	ADC Rch
0	0	IN3
0	1	IN4
1	X	INP2/INN2

(default)

(x: Do not care)

2. Microphone Input Gain

The AK7755 has a microphone gain amplifier. L and R channel gains can be set independently by MGNL[3:0] bits (CONT12: D3-D0) and MGNR[3:0] bits (CONT12: D7-D4). Input impedance is typ. 20kΩ. This gain amplifier executes zero cross detection when changing the gain by setting MICLZCE bit (CONT1A: D0) = "1" / MICRZCE bit (CONT1A: D1) = "1". Zero cross detection is executed on L and R channels independently. Timeout period of the zero cross detection is 16ms. When MICLZCE bit = "0" / MICRZCE bit = "0", zero cross detection is not performed and the volume is changed immediately when register is written.

When writing to MGNL3-0/MGNR3-0 bits continually, take an interval of zero crossing timeout periods or more. If the MGNL3-0/MGNR3-0 bits are changed before zero crossing, the volume of Lch and Rch may differ. When the volume that is same as the present is set, the zero crossing counter is not reset and timeout according to the previous writing timing.

Zero Crossing Timeout

When MICLZCE bit = "1" / MICRZCE bit = "1", the Lch/Rch volume level are changed independently by zero crossing detection or zero crossing timeout.

fs	Zero cross Timeout Period
48kHz	16ms

Mode	MGNL[3] MGNR[3]	MGNL[2] MGNR[2]	MGNL[1] MGNR[1]	MGNL[0] MGNR[0]	Input Gain	
0	0	0	0	0	0dB	(default)
1	0	0	0	1	2dB	
2	0	0	1	0	4dB	
3	0	0	1	1	6dB	
4	0	1	0	0	8dB	
5	0	1	0	1	10dB	
6	0	1	1	0	12dB	
7	0	1	1	1	14dB	
8	1	0	0	0	16dB	
9	1	0	0	1	18dB	
A	1	0	1	0	21dB	
B	1	0	1	1	24dB	
C	1	1	0	0	27dB	
D	1	1	0	1	30dB	
E	1	1	1	0	33dB	
F	1	1	1	1	36dB	

Table 3. Microphone Input Gain

3. Analog DRC (ADRC)

The microphone input gain can be set by DSP programs with the AK7755. This function is enabled by setting ADRCRE bit = "1"/ADRCLE bit = "1" (CONT1A: D3/D2). In this setting, control registers MGNL[3:0] and MDNR[3:0] bits (CONT12) are not valid. By reading AMGNL[3:0] (CONT1B: D3-D0) / AMGNR[3:0] (CONT1B: D7-D4) bits, gain settings can be downloaded externally.

When MICLZCE bit = "1"/MICRZCE bit = "1", the Lch/Rch volume level are changed independently by zero crossing detection or zero crossing timeout. Please refer to the AK7755 programing manual for DSP programs.

4. LINE Input Gain Amplifier

The AK7755 has a gain amplifier for line inputs. It is enabled by setting PMLI bit (CONT0F: D5) = "1", and it outputs a signal to the L channel of the ADC2. LIGN[3:0] bits (CONT13: D7-D4) controls the gain. The typical input impedance is 20kΩ (typ). A pop noise occurs if the input gain is changed during operation.
The AK7755 becomes digital microphone interface mode when DMIC2 bit (CONT1E: D4) = "1". Digital microphone input data to the DMDAT2 pin is input to the Lch/Rch of the ADC2.

ADC2 Input Setting

DMIC2 bit	ADC2 Lch Input	ADC2 Rch Input	
0	LIN	No	(default)
1	Digital Microphone	Digital Microphone	

Mode	LIGN[3]	LIGN[2]	LIGN[1]	LIGN[0]	Input Gain	
0	0	0	0	0	0dB	(default)
1	0	0	0	1	-3dB	
2	0	0	1	0	-6dB	
3	0	0	1	1	-9dB	
4	0	1	0	0	-12dB	
5	0	1	0	1	-15dB	
6	0	1	1	0	-18dB	
7	0	1	1	1	-21dB	
8	1	0	0	0	N/A	
9	1	0	0	1	+3dB	
A	1	0	1	0	+6dB	
B	1	0	1	1	+9dB	
C	1	1	0	0	+12dB	
D	1	1	0	1	+15dB	
E	1	1	1	0	+18dB	
F	1	1	1	1	+21dB	

Table 4. Line Input Gain

■ ADC Block

1. ADC High Pass Filter

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequency of the HPF is approximately 1Hz (at fs=48kHz).

fs	48kHz	44.1kHz	8kHz
Cut-off frequency	3.73Hz	3.43Hz	0.62Hz

2. ADC Soft Mute

2-1. Description

The ADC block has a digital soft mute circuit. The soft mute operation is performed in the digital domain. The output signal is attenuated to -∞ in "ADC Digital Volume Level x ATT transition time" from the current ADC Digital Volume Setting Level by setting ADMUTE and AD2MUTE bits to "1". When the ADMUTE (CONT1A: D7) and AD2MUTE (CONT1A: D6) bits are returned to "0", the mute is cancelled and the output attenuation gradually changes to ADC Digital Volume Setting Level in "ADC Digital Volume Level x ATT transition time". If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ADC Digital Volume Setting Level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission. The transition time from 0dB to -∞ and vice versa is 828 LRCK cycles.
The soft mute function works when the ADC is in operation. The attenuation value is initialized by the PDN pin = "L".
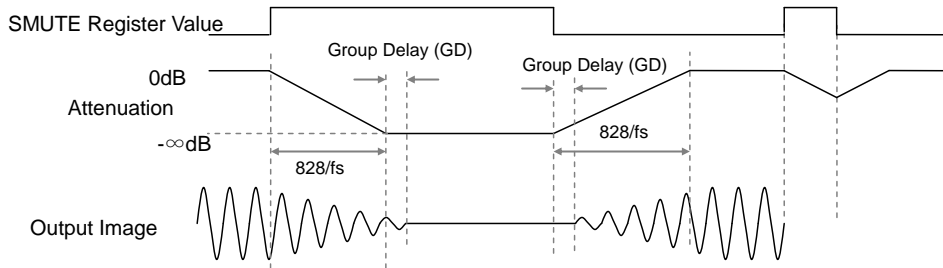

Figure 71. ADC Soft Mute

2-2. Input Selector Switching Sequence

The input selector should be changed after soft muting to avoid the switching noise of the input selector.

· Input Selector Switching Sequence
1. Enable soft mute before changing the channel.
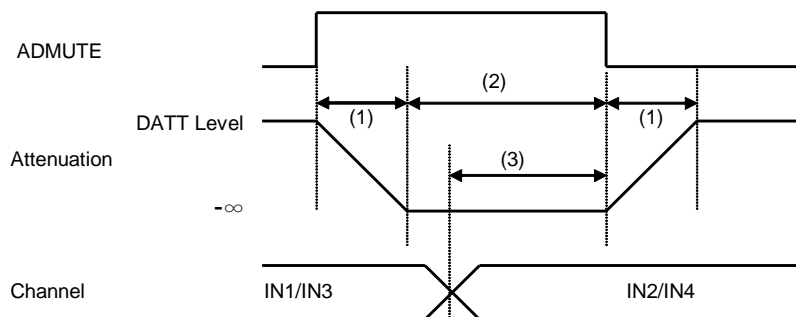2. Change the Channel.
3. Disable softer mute.

Figure 72. ADC Input Channel Switching Sequence Example

The period of (1) varies by the setting value of DATT bit. The transition time of attenuation amount from 0dB to -∞ and vice versa is shown below.

ATSPAD	(1)Period (max)			
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz
0	828/fs	17.25ms	18.82ms	103.5ms
1	828/fs x 4	69ms	75.27ms	414ms

When changing channels, the input channel should be changed during (2). The period of (2) should be around 200ms because there is some DC difference between the channels (3).

2-3. ADC Digital Volume

The ADC of the AK7755 has channel-independent digital volume control (256 levels, 0.5dB step).
VOLADL [7:0] bits (CONT15:D7-D0), VOLADR [7:0] bits (CONT16:D7-D0), VOLAD2L [7:0] bits (CONT17:D7-D0) and VOLAD2R [7:0] bits (CONT1D:D7-D0) control these volume values independently.

ADC Lch VOLADL [7:0]	ADC Rch VOLADR [7:0]	ADC2 Lch VOLAD2L [7:0]	ADC2 Rch VOLAD2R [7:0]	Attenuation Level	
00h	00h	00h	00h	+24.0dB	
01h	01h	01h	01h	+23.5dB	
02h	02h	02h	02h	+23.0dB	
:	:	:	:	:	
2Fh	2Fh	2Fh	2Fh	+0.5dB	
30h	30h	30h	30h	0.0dB	(default)
31h	31h	31h	31h	-0.5dB	
:	:	:	:	:	
FDh	FDh	FDh	FDh	-102.5dB	
FEh	FEh	FEh	FEh	-103.0dB	
FFh	FFh	FFh	FFh	Mute (-∞)	

Table 5. ADC Digital Volume Level Setting

Transition time between set values can be selected by ATSPAD bit (CONT0C: D5).

MODE	ATSPAD	ATT speed
0	0	1/fs
1	1	4/fs

Table 6. ADC Volume Transition Time Setting

The transition between set values is soft transition of 1021 levels in Mode 0. It takes 1021/fs (21.3ms@fs=48kHz) from 00h to FFh(MUTE). If the PDN pin is set to "L", the VOLADL/R[7:0] bits are initialized to 30h.

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB
00h	24.0	20h	8.0	40h	-8.0	60h	-24.0	80h	-40.0	A0h	-56.0	C0h	-72.0	E0h	-88.0
01h	23.5	21h	7.5	41h	-8.5	61h	-24.5	81h	-40.5	A1h	-56.5	C1h	-72.5	E1h	-88.5
02h	23.0	22h	7.0	42h	-9.0	62h	-25.0	82h	-41.0	A2h	-57.0	C2h	-73.0	E2h	-89.0
03h	22.5	23h	6.5	43h	-9.5	63h	-25.5	83h	-41.5	A3h	-57.5	C3h	-73.5	E3h	-89.5
04h	22.0	24h	6.0	44h	-10.0	64h	-26.0	84h	-42.0	A4h	-58.0	C4h	-74.0	E4h	-90.0
05h	21.5	25h	5.5	45h	-10.5	65h	-26.5	85h	-42.5	A5h	-58.5	C5h	-74.5	E5h	-90.5
06h	21.0	26h	5.0	46h	-11.0	66h	-27.0	86h	-43.0	A6h	-59.0	C6h	-75.0	E6h	-91.0
07h	20.5	27h	4.5	47h	-11.5	67h	-27.5	87h	-43.5	A7h	-59.5	C7h	-75.5	E7h	-91.5
08h	20.0	28h	4.0	48h	-12.0	68h	-28.0	88h	-44.0	A8h	-60.0	C8h	-76.0	E8h	-92.0
09h	19.5	29h	3.5	49h	-12.5	69h	-28.5	89h	-44.5	A9h	-60.5	C9h	-76.5	E9h	-92.5
0Ah	19.0	2Ah	3.0	4Ah	-13.0	6Ah	-29.0	8Ah	-45.0	AAh	-61.0	CAh	-77.0	EAh	-93.0
0Bh	18.5	2Bh	2.5	4Bh	-13.5	6Bh	-29.5	8Bh	-45.5	ABh	-61.5	CBh	-77.5	EBh	-93.5
0Ch	18.0	2Ch	2.0	4Ch	-14.0	6Ch	-30.0	8Ch	-46.0	ACh	-62.0	CCh	-78.0	ECh	-94.0
0Dh	17.5	2Dh	1.5	4Dh	-14.5	6Dh	-30.5	8Dh	-46.5	ADh	-62.5	CDh	-78.5	EDh	-94.5
0Eh	17.0	2Eh	1.0	4Eh	-15.0	6Eh	-31.0	8Eh	-47.0	AEh	-63.0	CEh	-79.0	EEh	-95.0
0Fh	16.5	2Fh	0.5	4Fh	-15.5	6Fh	-31.5	8Fh	-47.5	AFh	-63.5	CFh	-79.5	EFh	-95.5
10h	16.0	30h	0.0	50h	-16.0	70h	-32.0	90h	-48.0	B0h	-64.0	D0h	-80.0	F0h	-96.0
11h	15.5	31h	-0.5	51h	-16.5	71h	-32.5	91h	-48.5	B1h	-64.5	D1h	-80.5	F1h	-96.5
12h	15.0	32h	-1.0	52h	-17.0	72h	-33.0	92h	-49.0	B2h	-65.0	D2h	-81.0	F2h	-97.0
13h	14.5	33h	-1.5	53h	-17.5	73h	-33.5	93h	-49.5	B3h	-65.5	D3h	-81.5	F3h	-97.5
14h	14.0	34h	-2.0	54h	-18.0	74h	-34.0	94h	-50.0	B4h	-66.0	D4h	-82.0	F4h	-98.0
15h	13.5	35h	-2.5	55h	-18.5	75h	-34.5	95h	-50.5	B5h	-66.5	D5h	-82.5	F5h	-98.5
16h	13.0	36h	-3.0	56h	-19.0	76h	-35.0	96h	-51.0	B6h	-67.0	D6h	-83.0	F6h	-99.0
17h	12.5	37h	-3.5	57h	-19.5	77h	-35.5	97h	-51.5	B7h	-67.5	D7h	-83.5	F7h	-99.5
18h	12.0	38h	-4.0	58h	-20.0	78h	-36.0	98h	-52.0	B8h	-68.0	D8h	-84.0	F8h	-100.0
19h	11.5	39h	-4.5	59h	-20.5	79h	-36.5	99h	-52.5	B9h	-68.5	D9h	-84.5	F9h	-100.5
1Ah	11.0	3Ah	-5.0	5Ah	-21.0	7Ah	-37.0	9Ah	-53.0	BAh	-69.0	DAh	-85.0	FAh	-101.0
1Bh	10.5	3Bh	-5.5	5Bh	-21.5	7Bh	-37.5	9Bh	-53.5	BBh	-69.5	DBh	-85.5	FBh	-101.5
1Ch	10.0	3Ch	-.6.0	5Ch	-22.0	7Ch	-38.0	9Ch	-54.0	BCh	-70.0	DCh	-86.0	FCh	-102.0
1Dh	9.5	3Dh	-6.5	5Dh	-22.5	7Dh	-38.5	9Dh	-54.5	BDh	-70.5	DDh	-86.5	FDh	-102.5
1Eh	9.0	3Eh	-7.0	5Eh	-23.0	7Eh	-39.0	9Eh	-55.0	BEh	-71.0	DEh	-87.0	FEh	-103.0
1Fh	8.5	3Fh	-7.5	5Fh	-23.5	7Fh	-39.5	9Fh	-55.5	BFh	-71.5	DFh	-87.5	FFh	Mute

Table 7. ADC Digital Volume Setting List

■ DAC Blocks

1. De-emphasis Filter

The AK7755 has a digital de-emphasis filter (tc=50/15µs) by IIR filter, corresponding to 48kHz sampling frequency. DEM[1:0] bits control the de-emphasis filter.

DEM mode	DEM[1:0]	Sampling Frequency (fs)	
0	00	OFF	(default)
1	01	48kHz	
2	10	44.1kHz	
3	11	32kHz	

Table 8. De-emphasis Control

2. DAC Digital Volume Control

The DACs of the AK7755 have channel independent volume control (256 levels, 0.5 step). The VOLDAL/R[7:0] bits (CONT18: D7-D0 / CONT19: D7-D0), set the attenuation level of each DAC channel.

DAC Lch VOLDAL [7:0]	DAC Rch VOLDAR [7:0]	Attenuation Level	
00h	00h	+12.0dB	
01h	01h	+11.5dB	
02h	02h	+11.0dB	
:	:	:	
17h	17h	+0.5dB	
18h	18h	0.0dB	(default)
19h	19h	-0.5dB	
:	:	:	
FDh	FDh	-114.5dB	
FEh	FEh	-115.0dB	
FFh	FFh	Mute (-∞)	

Table 9. DAC Digital Volume Setting

Transition time between set values can be selected by ATSPDA bit (CONT0C: D5).

MODE	ATSPDA	ATT speed
0	0	1/fs
1	1	4/fs

Table 10. DAC Volume Transition Time Setting

The transition between set values is soft transition of 1021 levels in Mode 0. It takes 1021/fs (21.3ms@fs=48kHz) from 00h to FFh (MUTE) in Mode 0. If the PDN pin is set to "L", the VOLDAL/R[7:0] bits are initialized to 18h.

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	DB	code	dB
00h	12.0	20h	-4.0	40h	-20.0	60h	-36.0	80h	-52.0	A0h	-68.0	C0h	-84.0	E0h	-100.0
01h	11.5	21h	-4.5	41h	-20.5	61h	-36.5	81h	-52.5	A1h	-68.5	C1h	-84.5	E1h	-100.5
02h	11.0	22h	-5.0	42h	-21.0	62h	-37.0	82h	-53.0	A2h	-69.0	C2h	-85.0	E2h	-101.0
03h	10.5	23h	-5.5	43h	-21.5	63h	-37.5	83h	-53.5	A3h	-69.5	C3h	-85.5	E3h	-101.5
04h	10.0	24h	-.6.0	44h	-22.0	64h	-38.0	84h	-54.0	A4h	-70.0	C4h	-86.0	E4h	-102.0
05h	9.5	25h	-6.5	45h	-22.5	65h	-38.5	85h	-54.5	A5h	-70.5	C5h	-86.5	E5h	-102.5
06h	9.0	26h	-7.0	46h	-23.0	66h	-39.0	86h	-55.0	A6h	-71.0	C6h	-87.0	E6h	-103.0
07h	8.5	27h	-7.5	47h	-23.5	67h	-39.5	87h	-55.5	A7h	-71.5	C7h	-87.5	E7h	-103.5
08h	8.0	28h	-8.0	48h	-24.0	68h	-40.0	88h	-56.0	A8h	-72.0	C8h	-88.0	E8h	-104.0
09h	7.5	29h	-8.5	49h	-24.5	69h	-40.5	89h	-56.5	A9h	-72.5	C9h	-88.5	E9h	-104.5
0Ah	7.0	2Ah	-9.0	4Ah	-25.0	6Ah	-41.0	8Ah	-57.0	AAh	-73.0	CAh	-89.0	EAh	-105.0
0Bh	6.5	2Bh	-9.5	4Bh	-25.5	6Bh	-41.5	8Bh	-57.5	ABh	-73.5	CBh	-89.5	EBh	-105.5
0Ch	6.0	2Ch	-10.0	4Ch	-26.0	6Ch	-42.0	8Ch	-58.0	ACh	-74.0	CCh	-90.0	ECh	-106.0
0Dh	5.5	2Dh	-10.5	4Dh	-26.5	6Dh	-42.5	8Dh	-58.5	ADh	-74.5	CDh	-90.5	EDh	-106.5
0Eh	5.0	2Eh	-11.0	4Eh	-27.0	6Eh	-43.0	8Eh	-59.0	AEh	-75.0	CEh	-91.0	EEh	-107.0
0Fh	4.5	2Fh	-11.5	4Fh	-27.5	6Fh	-43.5	8Fh	-59.5	AFh	-75.5	CFh	-91.5	EFh	-107.5
10h	4.0	30h	-12.0	50h	-28.0	70h	-44.0	90h	-60.0	B0h	-76.0	D0h	-92.0	F0h	-108.0
11h	3.5	31h	-12.5	51h	-28.5	71h	-44.5	91h	-60.5	B1h	-76.5	D1h	-92.5	F1h	-108.5
12h	3.0	32h	-13.0	52h	-29.0	72h	-45.0	92h	-61.0	B2h	-77.0	D2h	-93.0	F2h	-109.0
13h	2.5	33h	-13.5	53h	-29.5	73h	-45.5	93h	-61.5	B3h	-77.5	D3h	-93.5	F3h	-109.5
14h	2.0	34h	-14.0	54h	-30.0	74h	-46.0	94h	-62.0	B4h	-78.0	D4h	-94.0	F4h	-110.0
15h	1.5	35h	-14.5	55h	-30.5	75h	-46.5	95h	-62.5	B5h	-78.5	D5h	-94.5	F5h	-110.5
16h	1.0	36h	-15.0	56h	-31.0	76h	-47.0	96h	-63.0	B6h	-79.0	D6h	-95.0	F6h	-111.0
17h	0.5	37h	-15.5	57h	-31.5	77h	-47.5	97h	-63.5	B7h	-79.5	D7h	-95.5	F7h	-111.5
18h	0.0	38h	-16.0	58h	-32.0	78h	-48.0	98h	-64.0	B8h	-80.0	D8h	-96.0	F8h	-112.0
19h	-0.5	39h	-16.5	59h	-32.5	79h	-48.5	99h	-64.5	B9h	-80.5	D9h	-96.5	F9h	-112.5
1Ah	-1.0	3Ah	-17.0	5Ah	-33.0	7Ah	-49.0	9Ah	-65.0	BAh	-81.0	DAh	-97.0	FAh	-113.0
1Bh	-1.5	3Bh	-17.5	5Bh	-33.5	7Bh	-49.5	9Bh	-65.5	BBh	-81.5	DBh	-97.5	FBh	-113.5
1Ch	-2.0	3Ch	-18.0	5Ch	-34.0	7Ch	-50.0	9Ch	-66.0	BCh	-82.0	DCh	-98.0	FCh	-114.0
1Dh	-2.5	3Dh	-18.5	5Dh	-34.5	7Dh	-50.5	9Dh	-66.5	BDh	-82.5	DDh	-98.5	FDh	-114.5
1Eh	-3.0	3Eh	-19.0	5Eh	-35.0	7Eh	-51.0	9Eh	-67.0	BEh	-83.0	DEh	-99.0	FEh	-115.0
1Fh	-3.5	3Fh	-19.5	5Fh	-35.5	7Fh	-51.5	9Fh	-67.5	BFh	-83.5	DFh	-99.5	FFh	Mute

Table 11. DAC Digital Volume Setting List

3. DAC Soft Mute

The DAC block has a digital soft mute circuit. The soft mute operation is performed in the digital domain. The input signal is attenuated to -∞ in "DAC Digital Volume Level x ATT transition time" from the current DAC Digital Volume Setting Level by setting DAMUTE bit (CONT1A: D5) to "1". When the DAMUTE bit is returned to "0", the mute is cancelled and the input attenuation gradually changes to DAC Digital Volume Setting Level in "DAC Digital Volume Level x ATT transition time". If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to DAC Digital Volume Setting Level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission. The soft mute function works when the DAC is in operation. Since the DAC block is in reset state, there is a possibility that a click noise occurs by a reset and a reset release when CRESETN bit (CONT0F: D3) = "0" and PMDAL/R bit (CONT0E: D0/D1) = "0". This click noise should be muted externally. The attenuation value is initialized by the PDN pin = "L".
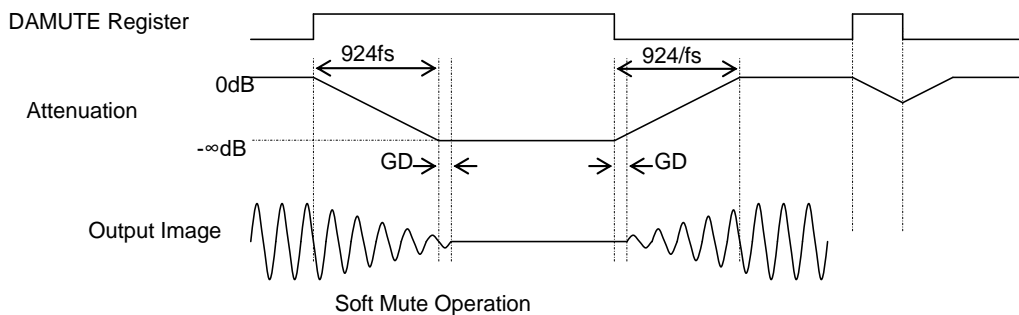

Figure 73. DAC Soft Mute Operation

■ Analog Output Block

The AK7755 can output an analog mixing signal of DAC and line-in amplifier outputs from the OUT3 pin. AD conversion is available by setting PMAD2L bit (CONT0E: D5) to "1" even when the analog mixing output is ON.
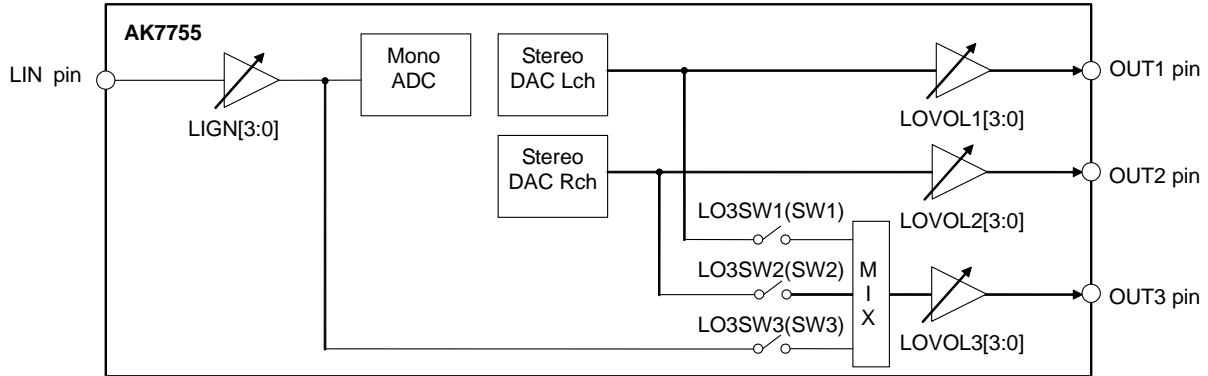

Figure 74. Analog Output Circuit

1. Line Output Amplifier

The AK7755 has a line output amplifier. The maximum amplitude is $0.76 \times$ AVDD (2.51[Vpp] @AVDD=3.3V) and load resistance is 10kΩ (min). LOVOL1/2/3[3:0] bits (CONT14: D3-D0/ CONT14: D7-D4/ CONT13: D3-D0) control the stereo line output volume. A pop noise occurs if the output gain is changed during operation.

LOVOL1,L2,L3[3:0]	Attenuation	LOVOL1, L2, L3[3:0]	Attenuation
0h	Mute(default)	8h	-14dB
1h	-28dB	9h	-12dB
2h	-26dB	Ah	-10dB
3h	-24dB	Bh	-8dB
4h	-22dB	Ch	-6dB
5h	-20dB	Dh	-4dB
6h	-18dB	Eh	-2dB
7h	-16dB	Fh	0dB

Table 12. Line Output Volume

2. Output1 and Output2

The OUT1 and OUT2 pins are connected to the L and R channels of the internal stereo DAC, respectively. The relationship of each control bit and the OUT1 and OUT2 pins are shown below.
The OUT1 and OUT2 pins output settings are controlled by PMLO1/2 bit (CONT0E: D2/D3), PMDAL/R bit (CONT0E: D0 /D1) and LOVOL1/2[3:0] bits (CONT014: D3-D0/D7-D4).

PMLO1 bit	PMDAL bit	LOVOL1[3:0] bits	OUT1 pin Output
0	X	X	Hi-Z
1	0	X	1/2 x AVDD
1	1	0h(mute)	1/2 x AVDD
1	1	1h-Fh	DAC Lch Output

PMLO2 bit	PMDAR bit	LOVOL2[3:0] bits	OUT2 pin Output
0	X	X	Hi-Z
1	0	X	1/2 x AVDD
1	1	0h(mute)	1/2 x AVDD
1	1	1h-Fh	DAC Rch Output

3. OUT3 (Analog Mixer）

The AK7755 can output an analog mixing signal of DAC and line-in amplifier outputs from the OUT3 pin by setting LO3SW1 bit (CONT09: D1), LO3SW2 bit (CONT09: D2) and LO3SW3 bit (CONT09: D3).

The line-out amplifier is powered up by setting PMLO3 bit = "1". Each switch is disconnected and the OUT3 pin outputs $1/2 \times$ AVDD when LOVOL3[3:0] bits (CONT13: D3-D0) = 0h. L and R channel signals of the DAC are input to the mixer by setting LO3SW1 bit and LO3SW2 bit to "1" while the setting of LOVOL3[3:0] bits is not 0h. L and R channel signals of the DAC are not gained by the mixer block.

The output signal of line-in amplifier is input to the mixer by setting LO3SW3 bit to "1" while the setting of LOVOL3[3:0] bits is not 0h. Adjust the input voltage and line-in amplifier gain (LIGN[3:0] bits (CONT13: D7-D4)) to prevent the mixing output exceeds $0.67 \times$ AVDD[Vpp] since the line-in amplifier output is gained +18dB by the mixer block.

The maximum amplitude of the line-out output is $0.76 \times$ AVDD[Vpp]. VOLDAL[7:0] bits (CONT18: D7-D0), VOLDAR[7:0] bits (CONT19: D7-D0), LIGN[3:0] bits and LOVOL3[3:0] bits should be adjusted to not exceed this maximum level.

PMLO3	LOVOL3[3:0]	LO3SW1	LO3SW2	LO3SW3	SW1	SW2	SW3
0	X	X	X	X	OFF	OFF	OFF
1	0h(mute)	X	X	X	OFF	OFF	OFF
1	1h-Fh	0	0	0	OFF	OFF	OFF
1	1h-Fh	0	0	1	OFF	OFF	ON
1	1h-Fh	0	1	0	OFF	ON	OFF
1	1h-Fh	0	1	1	OFF	ON	ON
1	1h-Fh	1	0	0	ON	OFF	OFF
1	1h-Fh	1	0	1	ON	OFF	ON
1	1h-Fh	1	1	0	ON	ON	OFF
1	1h-Fh	1	1	1	ON	ON	ON

Table 13. OUT3 pin Output Switching Setting

■ Simple Write Error Check

RAM and register data can be checked by cyclic redundancy check (CRC). It realizes a simple error check of a written data.

1. Checked Data

1-1. SPI Interface

The serial input data of the AK7755 can be checked from a falling edge of the CSN signal to rising edge of the CSN signal.

· Serial Data D (x): Input data from a falling edge to a rising edge of the CSN.
· Generating Polynomial: $G(x)=x^{16}+x^{12}+x^5+1$ (default=0)
· R(x) is defined as the remainder when D(x) is divided by G(x).
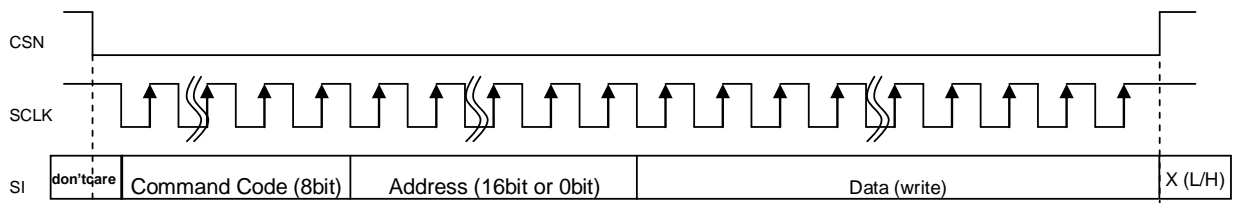
1-2. I²C Interface

The data after second byte: command code, address and data are checked. (Acknowledge is not included in the checked data. Therefore, if the command code, address and data are the same as when SPI interface is used, the CRC error result will also be the same.) The first byte which includes slave address is excluded. The first byte can be checked with Acknowledge.

· Serial Data D(x): Command Code, Address and Data (Expect slave address)
· Generating Polynomial: $G(x)=x^{16}+x^{12}+x^5+1$ (default=0)
· R (x) is defined as the remainder when D(x) is divided by G(x).

2. Simple Write Error Check Sequence

There are two ways to execute a simple write error check.

2-1. CRC Result Reading
(1) Write serial data D(x) that need to be checked.
(2) Read CRC result (the remainder R(x)) by the command code 72h.
(3) Check the result by a microcomputer.
(4) Repeat (1) ~ (3) when checking another serial data.
Note 59. The internal CRC result is not reflected by the command code

2-2. Checking by the STO pin
(1) Set control register CRCE bit to "1".
(2) Write serial data D(x) that need to be checked.
(3) Write the remainder R(x) of D(x) ti registers by the command code F2H.
(4) The SDO pin outputs "H" when the calculated remainder of D(x) divided by G(x) equals to the R(x) value. If not, the STO pin outputs "L".
(5) Repeat (2) ~ (4) when checking another serial data.
Note 60. The STO pin keeps "L" output until an appropriate remainder R(x) is written to the registers.

■ EEPROM Interface

1. Data Download

The AK7755 has EEPROM boot mode to read out necessary data from an external EEPROM to the internal memory via I^{2}C bus. A hands-free function is easily realized in the system using EEPROM without extra overloads on the microprocessor. The external EEPROM should be connected to the I^{2}C interface of the AK7755 (I2CSEL pin= "H"). A SPI interface type EEPROM cannot be connected. Write data as shown in "2. Program Map" to the EEPROM.
Control registers can shift the WRITE command code and data in 2 BYTE unit. However, the data location from the PRAM WRITE command code (0034h) to OFREG address 31LSB (689Ch) is fixed.
Set "1010000" to I^{2}C slave address of the EEPROM when 256K bit, and set "101000+A16" when 1M bit.

The AK7755 starts downloading the data from the EEPROM when setting the EXTEEP pin to "H" or DLS bit (CONT0D: D0) to "1" while the EXTEEP pin = "L" after inputting a 12.288MHz clock to the XTI pin or connecting a 12.288MHz crystal oscillator to the XTI pin and the XTO pin. The EEST (SDOUT1) pin goes to "H" while downloading data and the AK7755 becomes an I^{2}C master. Do not write/read to the other devices that are connected to the same I^{2}C bus during downloading. The EEST pin returns to "L" after downloading data and the AK7755 will be in I^{2}C slave mode. Interfacing to a microcontroller becomes available when the EEST pin = "L".

When accessing the AK7755 after downloading data by CRC function, set CRCE bit (CONT10: D6) to "0" before access the AK7755. The EEPROM download period is 0.8s (max). Set the EXTEEP pin "H" → "L" → "H" or DLS bit (CONT0D, D0) "1" → "0" → "1" to start a data downloading again. However, data downloading cannnot be executed by DLS bit when selecting memory mat (I2CSEL pin = MATSEL pin = "H").
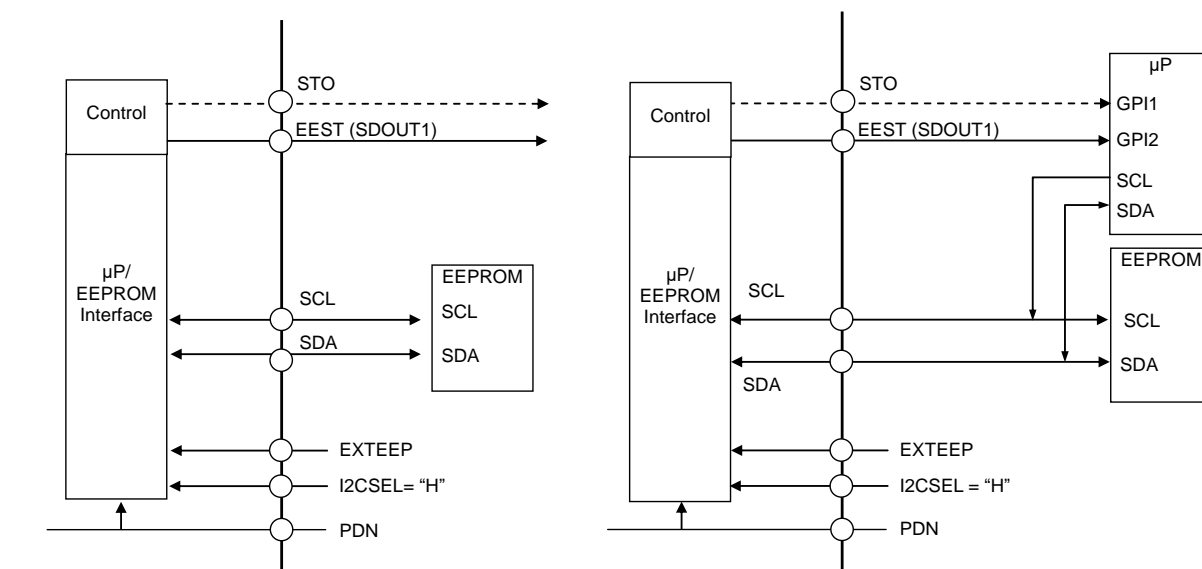
Figure 75. EEPROM Connection (Left: EEPROM only, Right: CPU and EEPROM)

2. Program Map

EEPROM Address	DATA	Note
0000h	C0h	CONT00 Write Command Code
0001h	DATA	CONT00 Data
0002h	C1h	CONT01 Write Command Code
0003h	DATA	CONT01 Data
0004h	C2h	CONT02 Write Command Code
0005h	DATA	CONT02 Data
0006h	C3h	CONT03 Write Command Code
0007h	DATA	CONT03 Data
0008h	C4h	CONT04 Write Command Code
0009h	DATA	CONT04 Data
000Ah	C5h	CONT05 Write Command Code
000Bh	DATA	CONT05 Data
000Ch	C6h	CONT06 Write Command Code
000Dh	DATA	CONT06 Data
000Eh	C7h	CONT07 Write Command Code
000Fh	DATA	CONT07 Data
0010h	C8h	CONT08 Write Command Code
0011h	DATA	CONT08 Data
0012h	C9h	CONT09 Write Command Code
0013h	DATA	CONT09 Data
0014h	CAh	CONT0A Write Command Code
0015h	DATA	CONT0A Data
0016h	CCh	CONT0CWrite Command Code
0017h	DATA	CONT0C Data
0018h	D0h	CONT10 Write Command Code
0019h	DATA	CONT10 Data
001Ah	D1h	CONT11 Write Command Code
001Bh	DATA	CONT11 Data
001Ch	D2h	CONT12 Write Command Code
001Dh	DATA	CONT12 Data
001Eh	D3h	CONT13 Write Command Code
001Fh	DATA	CONT13 Data
0020h	D4h	CONT14 Write Command Code
0021h	DATA	CONT14 Data
0022h	D5h	CONT15 Write Command Code
0023h	DATA	CONT15 Data
0024h	D6h	CONT16 Write Command Code
0025h	DATA	CONT16 Data
0026h	D7h	CONT17 Write Command Code
0027h	DATA	CONT17 Data
0028h	D8h	CONT18 Write Command Code
0029h	DATA	CONT18 Data
002Ah	D9h	CONT19 Write Command Code
002Bh	DATA	CONT19 Data
002Ch	DAh	CONT1A Write Command Code
002Dh	DATA	CONT1A Data
002Eh	00h	Dummy Data0　0 (Note 62)
002Fh	00h	Dummy Data0　1
0030h	00h	Dummy Data1　0
0031h	00h	Dummy Data1　1
0032h	00h	Dummy Data2　0 (Note 61)
0033h	00h	Dummy Data2　1

0034h	B8h	PRAM WRITE Command Code
0035h	00h	PRAM Address MSB side
0036h	00h	PRAM Address LSB side
0037h	PRAM0 DATA39-32	PRAM Address0 MSB 8-bit Data
0038h	PRAM0 DATA31-24	PRAM Address0 MSB-1 8-bit Data
0039h	PRAM0 DATA23-16	PRAM Address0 MSB-2 8-bit Data
003Ah	PRAM0:DATA15-8	PRAM Address0 MSB-3 8-bit Data
003Bh	PRAM0 DATA7-0	PRAM Address0 LSB 8-bit Data
003Ch	PRAM1 DATA39-32	PRAM Address1 MSB 8-bit Data
003Dh	PRAM1 DATA31-24	PRAM Address1 MSB-1 8-bit Data
003Eh	PRAM1 DATA23-16	PRAM Address1 MSB-2 8-bit Data
003Fh	PRAM1:DATA15-8	PRAM Address1 MSB-3 8-bit Data
0040h	PRAM1 DATA7-0	PRAM Address1 LSB 8-bit Data
0041h	PRAM2 DATA39-32	PRAM Address2 MSB-1 8-bit Data
• • •	• • •	
5031h	PRAM4094 DATA7-0	PRAM Address4094 LSB 8-bit Data
5032h	PRAM4095 DATA39-32	PRAM Address4095 MSB 8-bit Data
5033h	PRAM4095 DATA31-24	PRAM Address4095 MSB-1 8-bit Data
5034h	PRAM4095 DATA23-16	PRAM Address4095 MSB-2 8-bit Data
5035h	PRAM4095 DATA15-8	PRAM Address4095 MSB-3 8-bit Data
5036h	PRAM4095 DATA7-0	PRAM Address4095 LSB 8-bit Data
5037h	B4h	CRAM WRITE Command Code
5038h	00h	CRAM Address MSB side
5039h	00h	CRAM Address LSB side
503Ah	CRAM0 DATA23-16	CRAM Address0 MSB 8-bit Data
503Bh	CRAM0 DATA15-8	CRAM Address0 MSB-1 8-bit Data
503Ch	CRAM0 DATA7-0	CRAM Address0 LSB 8-bit Data
503Dh	CRAM1 DATA23-16	CRAM Address1 MSB 8-bit Data
• • •	• • •	
6836h	CRAM2046 DATA7-0	CRAM Address2046 LSB 8-bit Data
6837h	CRAM2047 DATA23-16	CRAM Address2047 MSB 8-bit Data
6838h	CRAM2047 DATA15-8	CRAM Address2047 MSB-1 8-bit Data
6839h	CRAM2047 DATA7-0	CRAM Address2047 LSB 8-bit Data
683Ah	B2h	OFREG WRITE Command Code
683Bh	00h	OFREG Address MSB side
683Ch	00h	OFREG Address LSB side
683Dh	OFREG0 DATA23-16	OFREG Address0 MSB 8-bit Data
683Eh	OFREG0 DATA15-8	OFREG Address0 MSB-1 8-bit Data
683Fh	OFREG0 DATA7-0	OFREG Address0 LSB 8-bit Data
6840h	OFREG1 DATA23-16	OFREG Address1 MSB 8-bit Data
• • •	• • •	
6899h	OFREG30 DATA7-0	OFREG Address30 LSB 8-bit Data
689Ah	OFREG31 DATA23-16	OFREG Address31 MSB 8-bit Data
689Bh	OFREG31 DATA15-8	OFREG Address31 MSB-1 8-bit Data
689Ch	OFREG31 DATA7-0	OFREG Address31 LSB 8-bit Data
689Dh	CDh	CONT0D Write Command Code
689Eh	40h	CONT0D Data
689Fh	E6h	CONT26 Write Command Code
68A0h	01h	CONT26 Data
68A1h	EAh	CONT2A Write Command Code
68A2h	80h	CONT2A Data
68A3h	CEh	CONT0E WRITE Command Code
68A4h	DATA	CONT0E Data
68A5h	CFh	CONT0F WRITE Command Code
68A6h	DATA	CONT0F Data
68A7h	00h	Dummy Data0_0
68A8h	00h	Dummy Data0_1
68A9h	00h	Dummy Data1_0
68AAh	00h	Dummy Data1_1

68ABh	00h	Dummy Data2_0
68ACh	00h	Dummy Data2_1
68ADh	00h	Dummy Data3_0
68AEh	00h	Dummy Data3_1
68AFh	00h	Dummy Data4_0
68B0h	00h	Dummy Data4_1
68B1h	00h	Dummy Data5_0
68B2h	00h	Dummy Data5_1
68B3h	00h	Dummy Data6_0
68B4h	00h	Dummy Data6_1
68B5h	F2h	CRC WRITE Command Code
68B6h	CRC DATA15-8	CRC MSB 8-bit Data
68B7h	CRC DATA7-0	CRC LSB 8-bit Data
68B8h	00h	Reserve
•••	•••	
7FFFh	00h	Reserve

Note 61. DSPRESETN bit (CONT0F: D2) must be "0" when downloading a DSP program. Especially this setting is necessary when changing the DSP program during operation by selecting EEPROM mat.

Note 62. A WRITE command for arbitrary control register can be written to Dummy data *_0, and write register setting for the control register to Dummy data*_1 in the table above.

Data transffer from EEPROM can be confirmed by writing R(x) (16-bit) data to CRCDATA (addr: 68B6h, 68B7h) which is the remainder of serial data D(x) from address 0000h to 68B4h devided by a generating polynominal; $G(x)=x^{16}+x^{12}+x^5+1$ (Initial Value= 0).

3. EEPROM Automatic Re-downloading

When a programmed WDT or CRC error is detected, automatic re-downloading of the EEPROM data is available up to 4 times by setting the EXPEEP pin = "H". When an error occurs after re-downloading more than 4 times, "L" level is output on the STO pin and the device stops. The device status can be checked by reading STO bit (CONT0D: D7). The CRC function is enabled by setting CRCE bit (CONT10: D6) to "1". The default setting of CRCE bit is "0" (disabled).
This setting is initialized (error count: 0) by the PDN pin = "L". It is not initialized by a clock reset.

4. EEPROM Mat Select

The pin number 20 becomes the MATSEL pin that enables EEPROM program mat selecting when the EXTEEP pin = "H".
Connect a 256K-bit EEPROM and bring the MATSEL pin = "L" when not selecting the EEPROM mat.
Connect a 1M-bit EEPROM and bring the MATSEL pin = "H" when selecting the EEPROM mat. In this case, the pin number 14 (MAT1) and 15 (MAT0) are address pins of the mat select.
Single program is stored in every 256K bits as a program map. The EEPROM can store four programs in total. The MAT1 and MAT0 pins select a program to download to the AK7755. OUT3E bit (CONT0A, D2) and OUT2E bit (CONT0A, D1) must not set to "1" when selecting an EEPROM mat (MATSEL pin = "H").

Program No.	MAT1 (14pin)	MAT0 (15pin)	EEPROM Storing Beginning Address	I^2C 1st Byte
1	0	0	17'h00000	"1 0 1 0 0 0 0 R/nW"
2	0	1	17'h08000	"1 0 1 0 0 0 0 R/nW"
3	1	0	17'h10000	"1 0 1 0 0 0 1 R/nW"
4	1	1	17'h18000	"1 0 1 0 0 0 1 R/nW"

■ Digital Microphone Interface

1. Digital MIC Connection

Four digital microphones can be connected to the AK7755 at the maximum. When DMIC1 (CONT1E: D7) or DMIC2 (CONT1E: D4) bit is set to "1", the #34 pin becomes DMDAT1 (digital microphone data input), the #33 pin becomes DMCLK1 (digital microphone clock supply) pins, the #32 pin becomes DMDAT2 pin and the #31 pin becomes DMCLK2 pin.

The DMCLK1/2 clock is an input to a digital microphone from the AK7755. The digital microphone outputs 1bit data, which is generated by ΔΣModulator using DMCLK1/2 clock, to the DMDAT1/2 pin. DMIC1/2 bit controls power up/down of the digital block (Decimation Filter and Digital Filter). DMCLKE1/2 bit (CONT1E: D5/D2) controls ON/OFF of the output clock from the DMCLK1/2 pin. When the AK7755 is powered down (PDN pin= "L"), the DMCLK1/2 and DMDAT1/2 pins become floating state. Pull-down resistors must be connected to DMCLK and DMDAT pins externally to avoid this floating state. Figure 76 shows a stereo 4ch connection example.
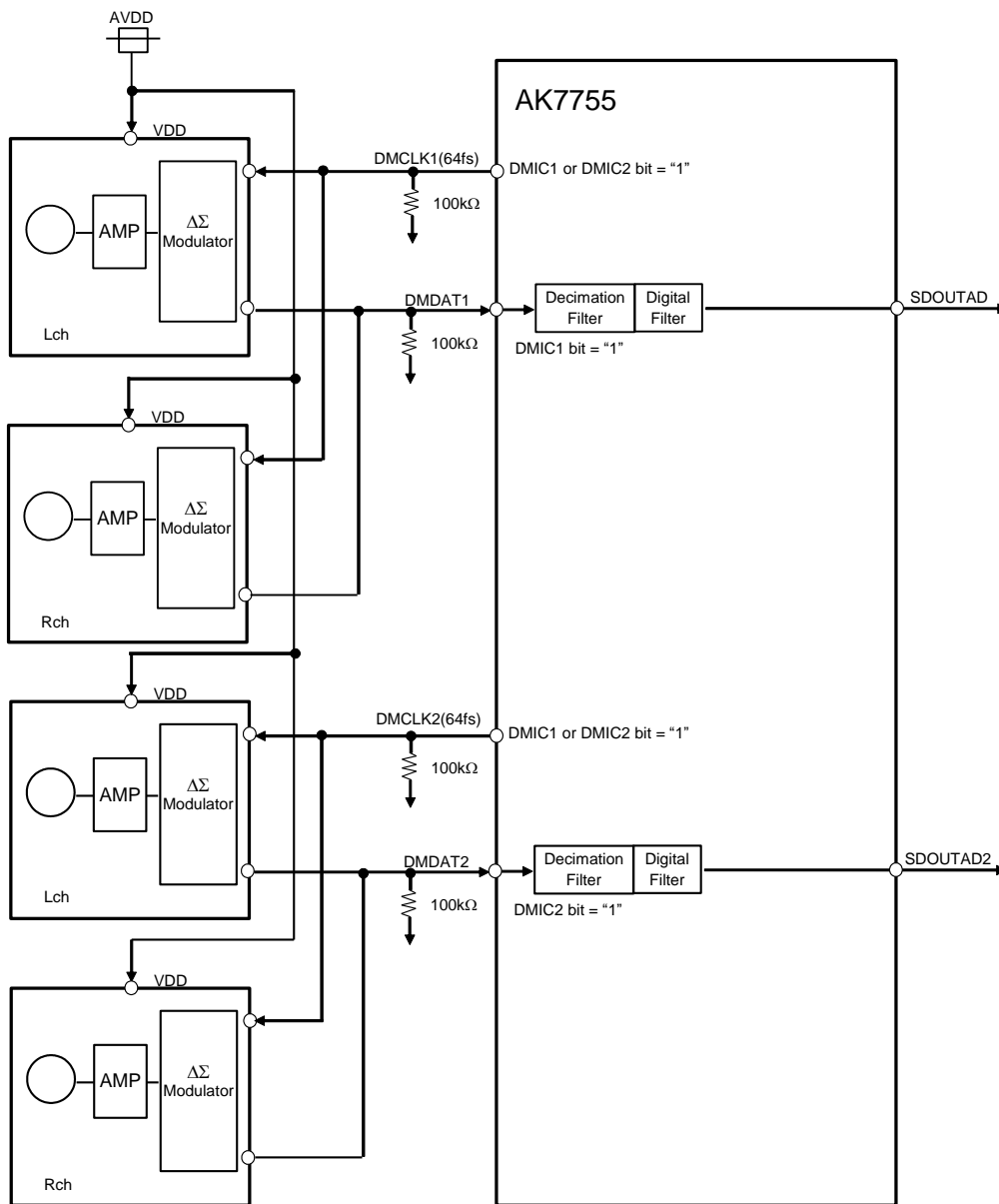
Figure 76. Connection Example for 4ch Stereo Digital Microphone

2. Interface

The input data channel of the DMDAT1/2 pin is set by DMCLKP1/2 bit (CONT1E: D6/D3). When DMCLKP1/2 bit = "1", L channel data is input to the decimation filter if the DMCLK1/2 pin= "H", and R channel data is input if the DMCLK1/2 = "L". When DMCLKP1/2 bit = "0", R channel data is input to the decimation filter while DMCLK1/2 pin= "H", and L channel data is input while DMCLK1/2 pin= "L". The DMCLK1/2 pin only supports 64fs. It outputs "L" when DMCLKE1/2 bit = "0", and outputs 64fs clock when DMCLKE1/2 bit = "1". The output data through "the Decimation and Digital Filters" is 24bit full scale when the 1bit data density is 0%~100%.

DMCLKP1 bit	DMCLK1 pin = "H"	DMCLK1 pin = "L"	
0	Rch	Lch	(default)
1	Lch	Rch	

DMCLKP2 bit	DMCLK2 pin = "H"	DMCLK2 pin = "L"	
0	Rch	Lch	(default)
1	Lch	Rch	

Table 14. Data Input/Output Timing with Digital MIC
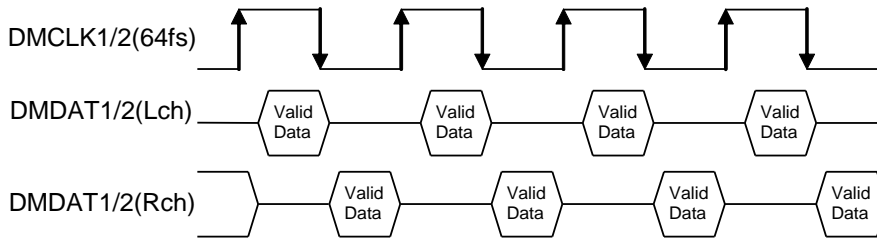
Figure 77. Data Input/Output Timing with Digital MIC (DMCLKP1/2 bit = "1")
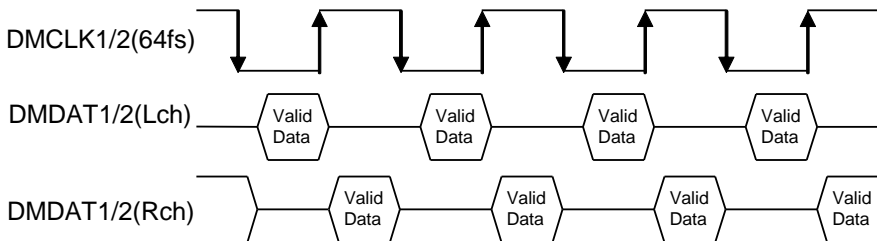
Figure 78. Data Input/Output Timing with Digital MIC (DMCLKP1/2 bit = "0")

■ Digital Mixer

ADC output (SDOUTAD), ADC2 output (SDOUTAD2) and DSP-DOUT4 data can be mixed into a signle serial data by a mixer circuit. SELMIX[2:0] bits (CONT09: D0, CONT08: D1, D0) control mixing setting. Delay time of the mixer circuit is 4Ts (4/fs).

SELMIX mode	SELMIX [2:0]	MIXOUT Lch	MIXOUT Rch	
0	000	SDOUTAD Lch	SDOUTAD Rch	(default)
1	001	SDOUTAD Lch/2 + SDOUTAD2 Lch/2	SDOUTAD Rch	
2	010	SDOUTAD Lch	SDOUTAD Lch/2 + SDOUTAD2 Lch/2	
3	011	SDOUTAD2 Lch	SDOUTAD2 Rch	
4	100	DSP-DOUT4 Lch	SDOUTAD2 Rch	
5	101	SDOUTAD2 Lch	DSP-DOUT4 Rch	
6	110	DSP-DOUT4 Lch	SDOUTAD Rch	
7	111	SDOUTAD Lch	DSP-DOUT4 Rch	

Table 15. Digital Mixer Output Setting

10. Recommended External Circuits

■ Connection Diagram

1. I2CSEL pin = "L", LDOE pin = "L"
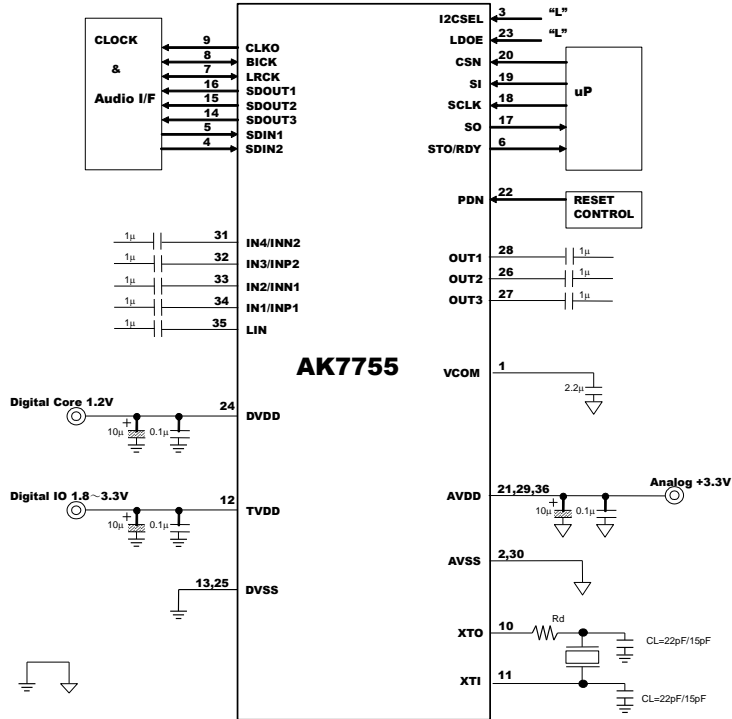
Figure 79. Serial Interface Connection with External Power Supply

2. I2CSEL pin = "L", LDOE pin = "H"
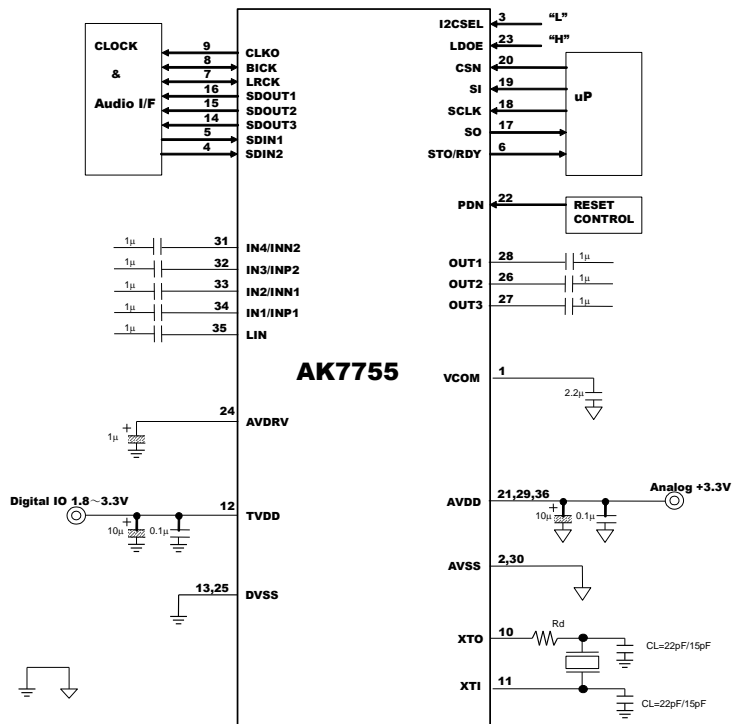
Figure 80. Serial Interface Connection with Internal LDO

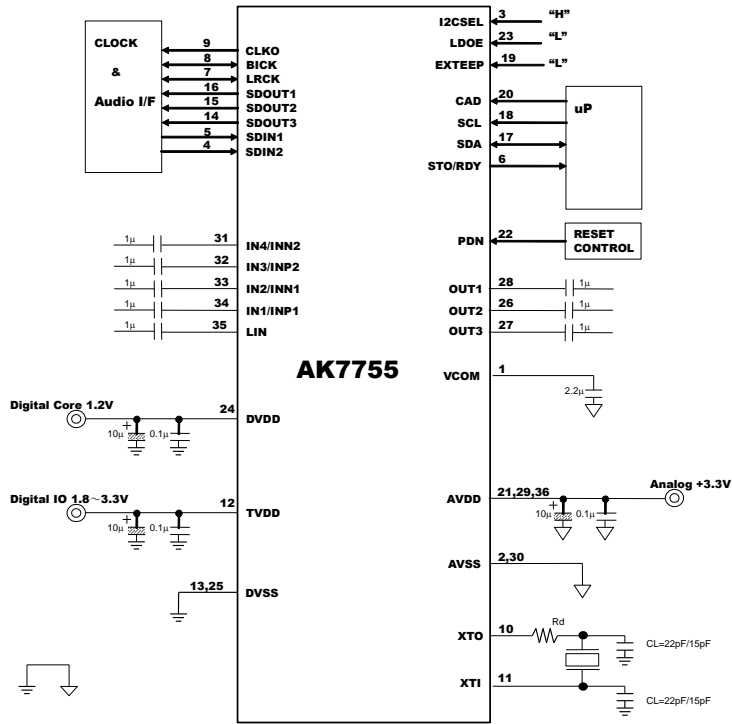## 3. I2CSEL pin = "H", EXTEEP pin = "L", LDOE pin = "L"

Figure 81. I²C Interface Connection with External Power Supply
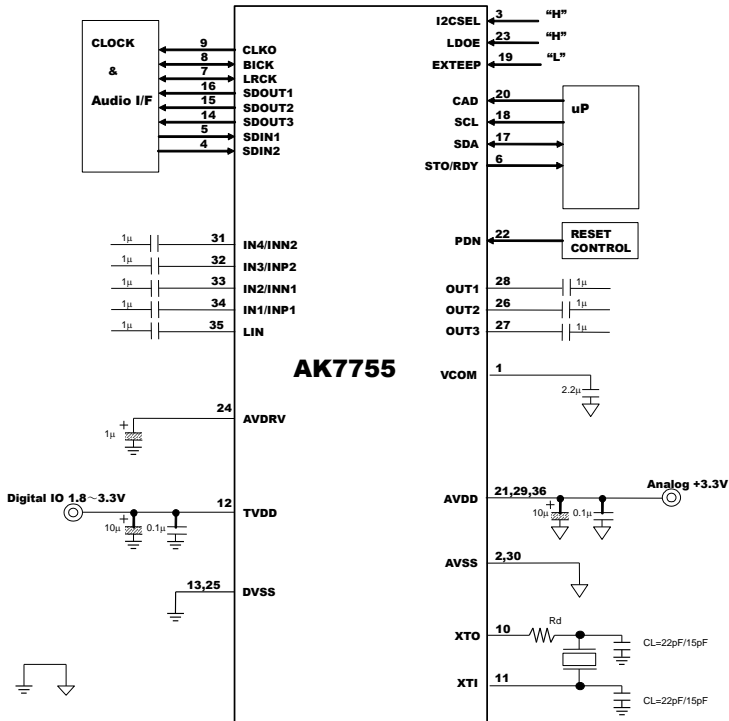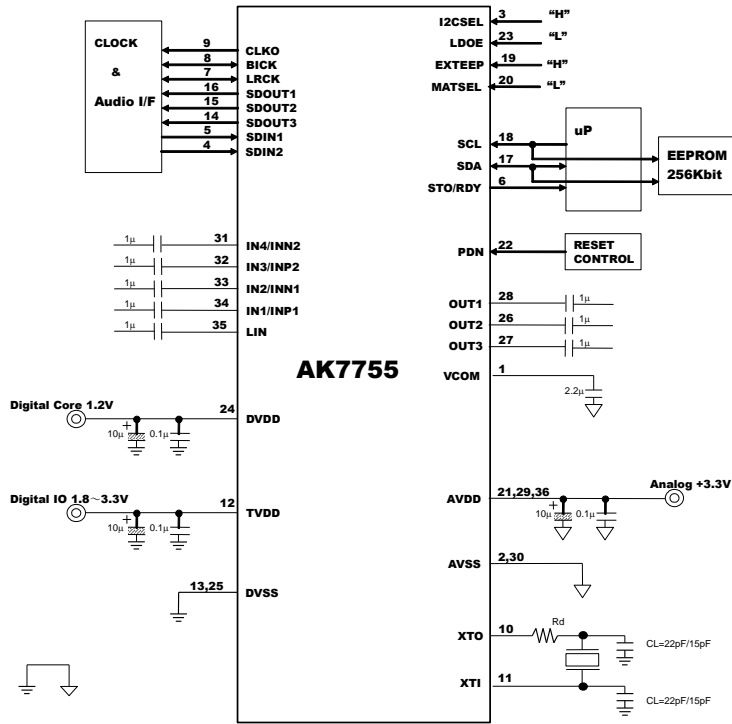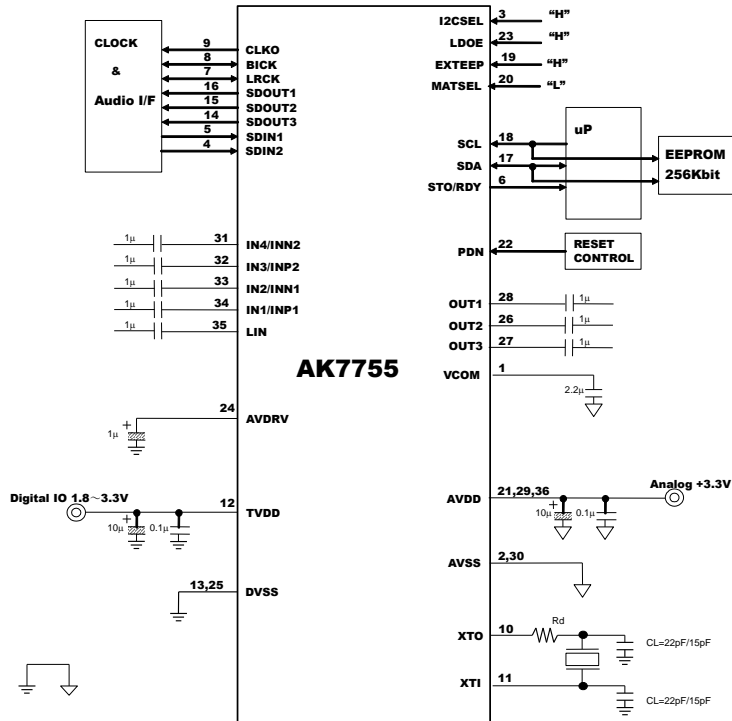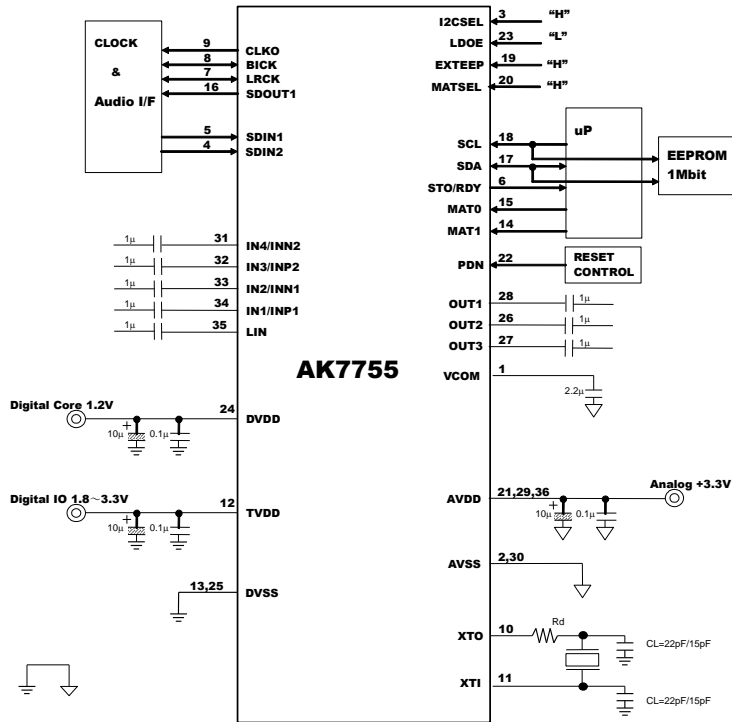
4. I2CSEL pin = "H", EXTEEP pin = "L", LDOE pin = "H"

Figure 82. I²C Interface Connection with Internal LDO

5. I2CSEL pin = "H", EXTEEP pin = "H", MATSEL pin = "L", LDOE pin = "L"

Figure 83. I²C Interface Connection with External Power Supply and EEPROM

6. I2CSEL pin = "H", EXTEEP pin = "H", MATSEL pin = "L", LDOE pin = "H"

Figure 84. I²C Interface Connection with Internal LDO and EEPROM

7. I2CSEL pin = "H", EXTEEP pin = "H", MATSEL pin = "H", LDOE pin = "L"

Figure 85. I²C Interface Connection with External Power Supply and EEPROM (Mat Select ON)

8. I2CSEL pin = "H", EXTEEP pin = "H", MATSEL pin = "H", LDOE pin = "H"
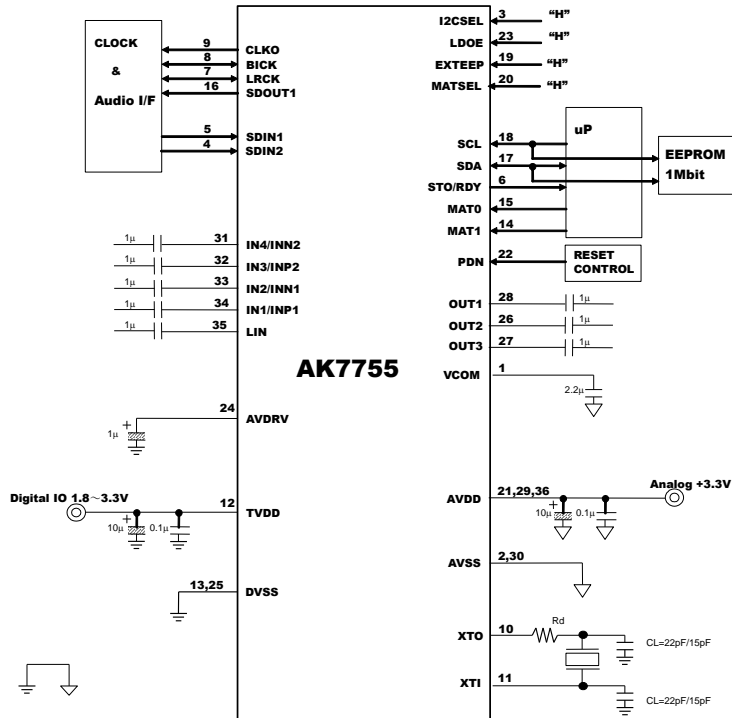
Figure 86. I²C Interface Connection with Internal LDO and EEPROM (Mat Select ON)

■ Peripheral Circuit

1. Ground

AVSS and DVSS must be connected to the same analog ground plane. Decoupling capacitors, particularly small capacity capacitors, should be connected as close as possible to the AK7755.

2. Reference Voltage

The AVDD voltage controls analog signal range. VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2μF ceramic capacitor connected between the VCOM and AVSS pins eliminates the effects of high frequency noise. The ceramic capacitor should be connected as close as possible to the VCOM pin. The VCOM pin must not be connected to external circuits. Digital signal lines, especially clock signal line should be kept away as far as possible from the VCOM pin in order to avoid unwanted coupling into the AK7755.

3. Analog Input

Analog input signals are applied to the modulator through the input pin of each channel. Input voltage is ±FS = ±(AVDD-AVSS) x 2.2/3.3 for differential pin and FS = (AVDD-AVSS) x 2.2/3.3 for single-end pin. When AVDD = 3.3V and AVSS=0.0V, the differential input range is ±2.20Vpp (typ) and it is 2.20Vpp (typ) for single-ended input. The digital output code format is 2's complements. DC offset can be cancelled by an internal HPF.

The AK7755 samples the analog inputs in 3.072MHz at fs = 48kHz. The digital filter removes noise in the range from 30kHz to 3.042MHz. The AK7755 includes an anti-aliasing filter (RC filter) to attenuate a noise around the range from 3.042MHz to 3.072MHz witch is not removed by the HPF. An external Low Pass Filter is not necessary since most of audio signals do not have large noise in the band around 3.072MHz. However, it is recommended to connect a Low Pass Filter before the ADC when a signal with large out-of-band noises is input.

The analog source voltage to the AK7755 is +3.3V (typ). Voltage of AVDD + 0.3V or more, voltage of AVSS – 0.3V or less, and current of 10mA or more must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. If the external analog circuit voltage is ±15V, the analog input pins must be protected from signals which are in absolute maximum rating level or more.
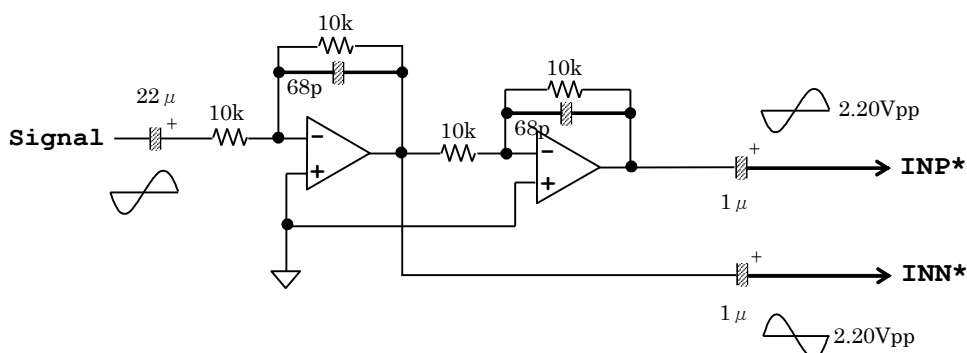

Figure 87. Input Buffer Circuit Example (Differential Input)

4. Analog Output

The analog line-outputs are single-ended. The output signal range is $0.76 \times$ AVDD Vpp (typ.) centered around VCOM voltage. The input code format is in 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal voltage at 000000H is VCOM. The VCOM voltage is AVDD/2 (typ). The internal switched-capacitor filter (SCF) and continuous-time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

5. Connection to Digital Circuit

To minimize the noise from digital circuits, the digital output of the AK7755 must be connected to CMOS or low voltage logic ICs such as 74HC and 74AC for CMOS and 74LV, 74LV-A, 74ALVC and 74AVC for low voltage logic ICs.

6. Cristal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown blow.

TVDD = 3.0 - 3.6V

CKM mode	XTAL Oscillator	R1_max	C0_max	XTI, XTO pin Connection Capacity
0	12.288MHz	120Ω	2.5pF	22pF
1	18.432MHz	80Ω	2.5pF	15pF

TVDD = 1.7 - 3.0V

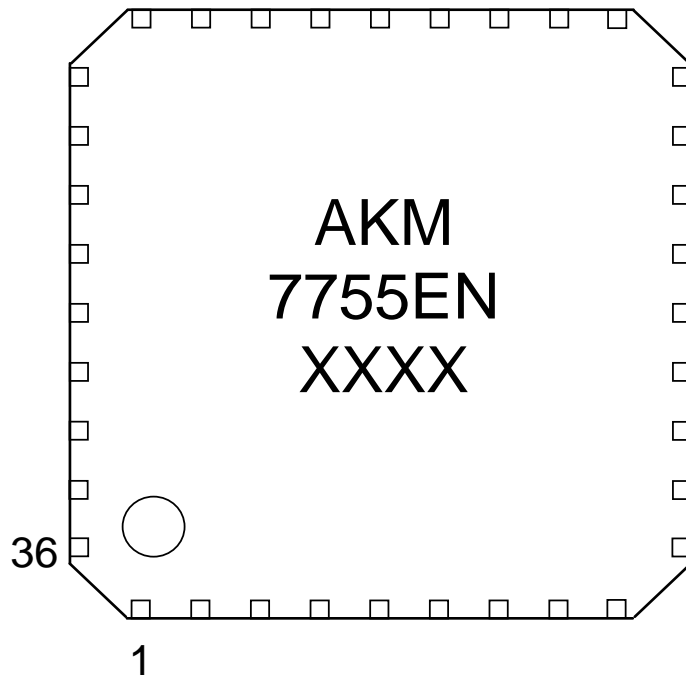| CKM mode	XTAL Oscillator	R1_max	C0_max	XTI, XTO pin Connection Capacity
0	12.288MHz	50Ω	1.2pF	10pF
1	18.432MHz	25Ω	1.2pF	10pF

Table 16. Crystal Oscillator

11. Package

■ Outline Dimensions
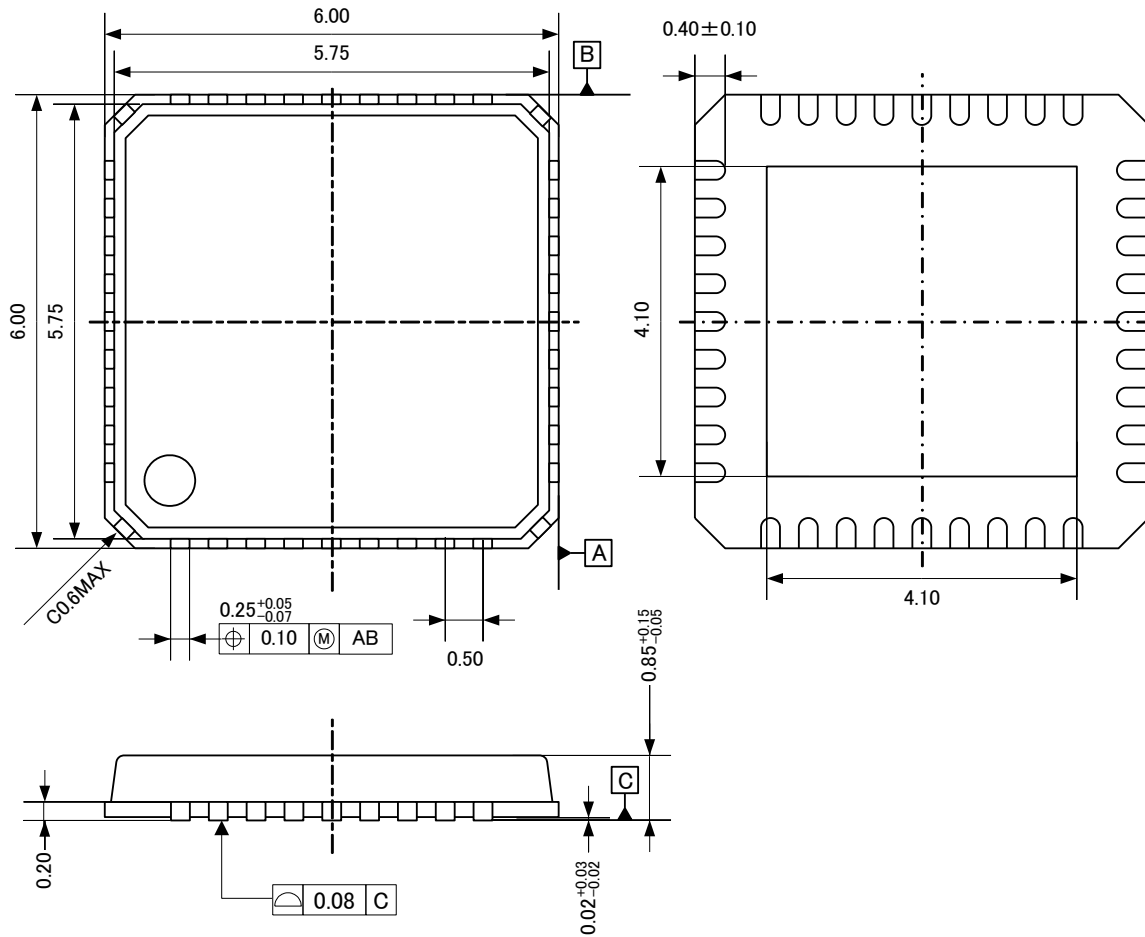
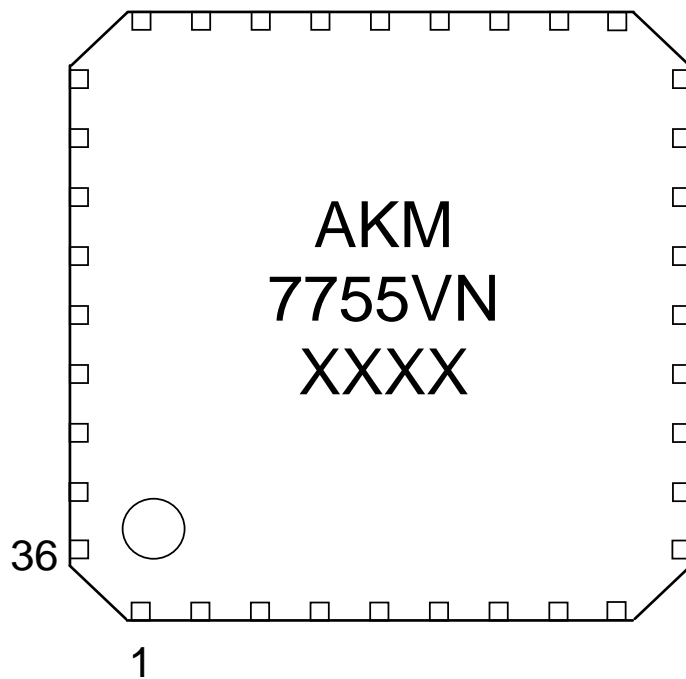## ■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

■ **Marking**

AKM
7755EN
XXXX

36

1

1) Pin #1 indication
2) Date Code: XXXX(4 digits)
3) Marking Code: 7755EN
4) Asahi Kasei Logo

AKM
7755VN
XXXX

36

1

1) Pin #1 indication
2) Date Code: XXXX(4 digits)
3) Marking Code: 7755VN
4) Asahi Kasei Logo

12. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
14/10/20	00	First Edition		
18/08/21	01	Error Correction	1	Features Two Digital Interfaces (I/F1, I/F2) "Digital Signal Input Port (6ch)" → "Digital Signal Output Port (6ch)"
		Specification Addition	13	MIC Amp + ADC Added explanation of Note 14 on the performance when DSM bit = "1"
		Error Correction	22	SPI Interface "CKRESTN" → "CKRESETN" "PLL Clock" → "PLL Lock"

		Specification Change	22	SPI Interface
				Changed specification of SPI interface
				Clock Reset (CKRESTEN bit = "0")
				  SCLK Frequency: max. 3.5MHz → max. 3MHz
				  SCLK Low Level Width: min. 120ns → min. 160ns
				  SCLK High Level Width: min. 120ns → min. 160ns
				PLL Lock(CKRESETN bit = "1")
				  SCLK Frequency: max. 7MHz → max. 6MHz
				  SCLK Low Level Width: min. 60ns → min. 72ns
				  SCLK High Level Width: min. 60ns → min. 72ns

		Error Correction	25	Figure 15. Digital Microphone Interface Timing Wave Form "tDMKL" →"tDMCKL", "DCLKP1" → "DMCLKP1", "DCLKP2" → "DMCLKP2"
			28	Figure 18. Slave Mode3 (CKM mode5) Sampling Frequency Setting SDIN2, SDOUT2, SDOUT3: fs=16kHz → 8kHz
			30	Control Register Settings "CKRESTN" → "CKRESETN"
			34	CONT03: Delay RAM, DSP Input / Output Setting <table><tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>↓<table><tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td></tr><tr><td>DIF2[1]</td><td>DIF2[0]</td><td>DOF2[1]</td><td>DOF2[0]</td></tr></table>
			41	CONT0A: D6: BICKOE BICK pin Output Setting "BICKO" → "BICK" D5: LRCKOE LRCK pin Output Setting "LRCKO" → "LRCK"
		Specification Addition	42	CONT0C: D7: DSM Delta Sigma Module Sampling CLK Setting: Added explanation on performance when DSM bit = "1" is set.
		Specification Change	45	CONT0F:D4: LRDETN Slave Mode Automatic System Reset Setting "if the LRCK is stopped or the LRCK phase is shifted more than 1/4fs " → "if LRCK and BICK are stopped"

Date (Y/M/D)	Revision	Reason	Page	Contents
18/08/21	01	Specification Addition	53,56	Power-up Sequence: Added the following specifications There is a possibility that glitch is occurred at the SO/SDA pin before the power supply for internal digital circuit is start up when the LDOE pin = "H". Do not make communication to other devises connected the AK7755 by SPI or I2C bus for 1ms after changing the PDN pin = "H".
		Specification Change	53	Figure 24. Power-up Sequence 1 is changed.
			54	Figure 25. Power-up Sequence 2 is changed.
			55	Figure 26. Power-up Sequence 3 is changed.
			55	Figure 27. Power-up Sequence 4 is changed.
			56	Figure 28. Power-up Sequence 5 is changed.
		Error Correction	57	Power-down and Reset "CKRESTN" → "CKRESETN"
		Specification Change	59	System Reset: Added the following specifications After setting power management bits of necessary blocks and releasing CODEC reset (CRESETN bit = "1"), the ADC, DAC and DSP blocks will be in normal operation by releasing DSP reset (DSPRESETN bit = "1").
			59	Figure 31. System Reset Structure is changed
			59	"if the LRCK is stopped or the LRCK phase is shifted more than 1/4fs " → "if LRCK and BICK are stopped" "if the LRCK is input again." → "if LRCK and BICK are input again."
		Specification Addition	59	Addition of specification of Note 47 and 48
			59	Restriction of DSP reset Description was added.
		Error Correction	60	Serial Data Interface Table2. Serial Data Format Setting is corrected.
			68,79,70, 72,74,75, 79	SPI Interface (I2CSEL pin = "L") "ACRAM" →"ACCRAM"
			78	External Conditional Jump "LRCLK" →"LRCK", "IRSTN" →"PDN"
			82	The First Byte "The slave address will be "0011000" when the I2CSEL pin ="H" and the EXTEEP pin = "L". → "The slave address will be "0011000" when the I2CSEL pin ="H" and the EXTEEP pin = "H".
			88	ADC Block: Figure 71. ADC Soft Mute is corrected.
			92	DAC Block: Figure 73. DAC Soft Mute is corrected.
			99	EEPROM Interface Program Map "CRCDATA (addr: 787Ch, 787Dh))" → "CRCDATA (addr: 68B6h, 68B7h)" "serial data D(x) from address 0000h to 68B7h" → "serial data D(x) from address 0000h to 68B4h"
			100, 101	Digital Microphone Interface "DCLKE1/2" → "DMCLKE1/2" "DCLKP1/2" → "DMCLKP1/2"

Date (Y/M/D)	Revision	Reason	Page	Contents
18/08/21	01	Error Correction	101	Digital Mixer "SDATAD" → "SDOUTAD" "SDATAD2" → "SDOUTAD2"

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