Click here to ask an associate for production status of specific part numbers.

Small, Single-/Multi-Cell Solar Harvester with MPPT and Harvest Counter

MAX20361

General Description

The MAX20361 is a fully integrated solution for harvesting energy from single-/multi-cell solar sources. The device includes an ultra-low quiescent current (360nA) boost converter that is capable of starting from input voltages as low as 225mV (typ). In order to maximize the power extracted from the source, the MAX20361 implements a proprietary maximum power point tracking (MPPT) technique that allows efficient harvesting from 15μW to over 300mW of available input power.

The MAX20361 also features an integrated charging and protection circuit that is optimized for Li-ion batteries, but can also be used to charge supercapacitors, thin-film batteries, or traditional capacitors. The charger features a programmable charging cut-off voltage with thresholds programmable through I^2C interface as well as temperature shutoff.

The MAX20361 is available in a 12-bump, 0.4mm pitch, 1.63mm x 1.23mm wafer-level package (WLP).

Applications

- Wearable Fitness
- Medical Devices
- Industrial IoT Sensors
- Asset Tracking Devices
- Wireless Sensor Networks

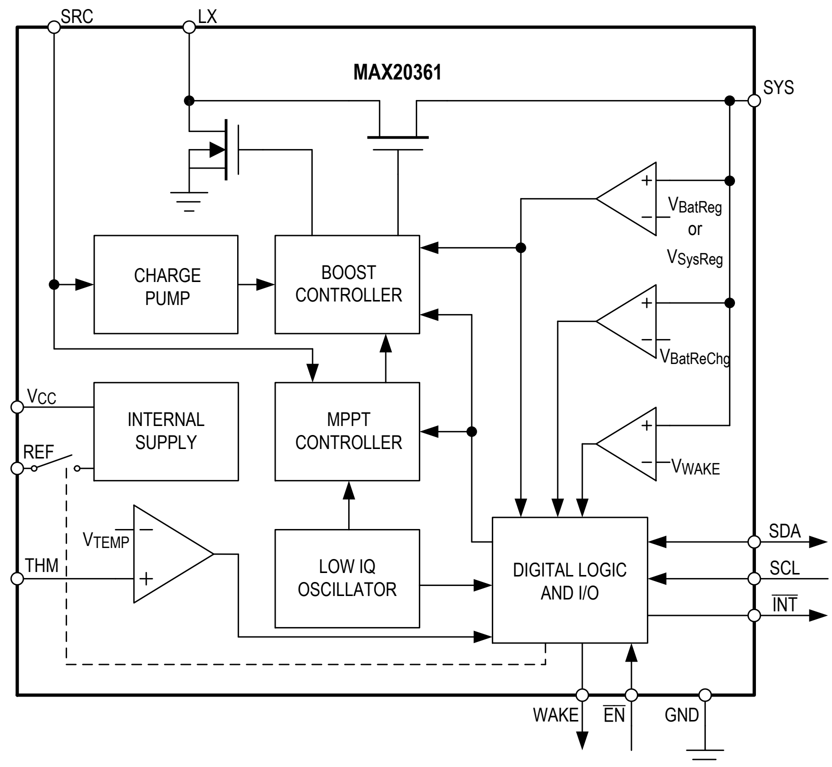
Benefits and Features

- Single-/Multi-Cell Solar Energy Harvester
  - 225mV to 2.5V (typ) Input-Voltage Range
  - Efficient Harvesting from 15μW to Over 300mW of Available Input Power
    - 86% Efficiency at V_{SYS} = 3.8V, I_{SRC} = 30mA
  - Small Solution Size
    - Utilizes Small 2016 4.7μH Inductor
- Maximum Power Point Tracking (MPPT) Technique Using Fractional VOC Method
  - Programmable Fractional VOC Regulation Point through I^2C Interface
- Battery/Supercapacitor Charger
  - Programmable Battery Termination Voltage through I^2C Interface
  - Programmable Power Good Wake-Up Signal Output Threshold through I^2C Interface

***Ordering Information* appears at end of data sheet**

19-100866; Rev 5; 8/23

Simplified Block Diagram



Absolute Maximum Ratings

SYS, V_{CC} to GND ....-0.3V to +6V
SRC to GND...-0.3V to +3.5V
$\overline{INT}$, $\overline{EN}$, SDA, SCL to GND.................................-0.3V to +6V
WAKE to GND....................................... -0.3V to (SYS + 0.3V)
REF, THM to GND.................................-0.3V to (V_{CC} + 0.3V)
LX to GND...-0.3V to (V_{CC} + 0.3V)
Continuous Current into LX, GND or SYS ....-0.5A to +0.5A
Continuous Current into any other Pin .... -0.05A to +0.05A
Continuous Power Dissipation (Multilayer Board) (T_A = +70ºC, derate 13.73mW/ºC above +70ºC) 1098.4mW
Operating Temperature Range ....-40ºC to +85ºC
Junction Temperature Range.........................-40ºC to +150ºC
Storage Temperature Range ....-40ºC to +150ºC
Soldering Temperature (reflow)..................................+260ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12-WLP

Package Code	W121C1+2
Outline Number	21-100426
Land Pattern Number	Refer to Application Note 1891
THERMAL RESISTANCE, FOUR LAYER BOARD	
Junction-to-Ambient (θ_{JA})	72.82ºC/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{SYS} = +3.0V to +4.2V, V_{SRC} = +0.3V to +2.5V, typical value is at V_{SYS} = +3.8V, V_{SRC} = +0.6V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
SYS Shutdown Supply Current	I_{SYS_SHDN}	DeviceEnb = 1, any V_{SRC}		190	650	nA
SYS Sleep Supply Current	I_{SYS_SLEEP}	DeviceEnb = 0, V_{SRC} = 0V		360	1200	nA
SYS Idle Supply Current	I_{SYS_IDLE}	$\overline{EN}$ = 0V, boost not switching, not in sleep mode		1.43		µA
SYSTEM CONTROL (SYS)						
System Termination Voltage-Programmable Range	V_{SYS_REG}	50mV steps, programmable through I2C		4 to 4.7		V
System Regulation-Voltage Accuracy	$V_{SYS\_REG\_ACC}$	T_A = 0°C to +60°C; SysReg[3:0] = 7, SYS rising	-1		+1	%
WAKE Voltage-Programmable Range	V_{WAKE_RANGE}	100mV steps, programmable through I2C		3 to 3.7		V
WAKE Voltage Accuracy	V_{WAKE_ACC}	WakeThr[2:0] = 0, SYS rising	-2		+2	%
WAKE Debounce Time	t_{WAKE_TDEB}		7 x Tmeas		8 x Tmeas	ms
BOOST REGULATOR						
Input Operating Voltage at SRC	V_{SRC_RANGE}		0		2.5	V
Minimum Cold-Start Voltage	V_{SC}	T_A = 25°C (Note 3)		225	350	mV
Efficiency	BOOST_EFF	V_{SRC} = 0.75V, V_{SYS} = 3.8V, I_{SRC} = 100µA, L = 4.7µH, DFE201612E-4R7M = P2 Series Inductor		77		%
		V_{SRC} = 0.75V, V_{SYS} = 3.8V, I_{SRC} = 30mA, L = 4.7µH, DFE201612E-4R7M = P2 Series Inductor		86		
LX Low-Side On Resistance	R_{ON_LXL}			0.1	0.14	Ω
LX SYS High-Side On Resistance	$R_{ON\_LX\_SYS}$			0.29	0.39	Ω
SRC LX Slow Snubber Resistance	R_{LX_SSNUB}			20		kΩ
SRC LX Snubber Resistance	R_{LX_SNUB}			342		Ω
Peak Current	I_{BSTpk0}			90		mA
	I_{BSTpk1}			120		
	I_{BSTpk2}			145		
	I_{BSTpk3}			180		
	I_{BSTpk4}			285		
	I_{BSTpk5}			355		
	I_{BSTpk6}			470		
	I_{BSTpk7}			715		
SRC METER						

(V_{SYS} = +3.0V to +4.2V, V_{SRC} = +0.3V to +2.5V, typical value is at V_{SYS} = +3.8V, V_{SRC} = +0.6V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SRC DAC Full-Scale	V_{DACFS}	SRC equivalent voltage		2.595		V
SRC Leakage	I_{LNKSRC}	V_{SRC} = 1V		0.75		µA
MAXIMUM POWER POINT TRACKING						
Fractional Open Circuit Voltage-Programmable Range	$V_{FRAC\_VOC\_P}$	1.5% steps, programmable through I²C		42.5 to 89.0		%
Error of Fractional VOC Regulation Point	$V_{FRAC\_VOC\_ERROR}$	V_{SRC} = 0.6V, includes measurement error of VOC and input voltage regulation error, excludes SRC ripple (Note 3); VOC[7:0] = 75, Frac[4:0] = 25, BSTpk = 3, I_{SRC} = 1mA	-4.7		+4.7	%
Open Circuit Measurement Period	t_{FRAC_VOC}	ATper = 0, Tper = 00, see text		64 * Tmeas		s
		ATper = 0, Tper = 01, see text		128 * Tmeas		
		ATper = 0, Tper = 10, see text		256 * Tmeas		
Open Circuit Measurement Settling Time	$t_{FRAC\_VOC\_SETTLE}$	ATmeas = 0, Tmeas = 00, see text		50		ms
		ATmeas = 0, Tmeas = 01, see text		100		
		ATmeas = 0, Tmeas = 10, see text		250		
		ATmeas = 0, Tmeas = 11, see text		500		
$\overline{\text{EN}}$						
$\overline{\text{EN}}$ Input Threshold	V_{ILENB}				0.4	V
	V_{IHENB}		1.0			
$\overline{\text{EN}}$ Input Resistance	R_{ENB}		0.7	1	1.3	MΩ
SCL, SDA, $\overline{\text{INT}}$						
SDA and $\overline{\text{INT}}$ Output-Low Voltage	V_{OLSDA}, $V_{OL\overline{INT}}$	I = 5mA			0.3	V
SDA, SCL, $\overline{\text{INT}}$ Input Current	I_{SDA}, I_{SCL}, $I_{\overline{INT}}$	V_ from 0V to 5.5V	-1	0	+1	µA
WAKE						
WAKE Output-Low Voltage	V_{OLWAKE}	I = 5mA			0.3	V
WAKE Output-High Voltage	V_{OHWAKE}	I = -5mA	SYS - 0.3			V
THERMAL MONITORING (REF, THM)						
REF Voltage	V_{REF}	I_{REF} from 0µA to 100µA	1.15	1.2	1.25	V
Cold Temperature Trip-Point Programmable Range	V_{COLD}		53.5	57.5	60	%V_{REF}
Hot Temperature Trip-Point Programmable Range	V_{HOT}		16.2	18.7	22	%V_{REF}
THM Input Leakage	I_{THM}		-1		+1	µA
I²C INTERFACE						

(V_{SYS} = +3.0V to +4.2V, V_{SRC} = +0.3V to +2.5V, typical value is at V_{SYS} = +3.8V, V_{SRC} = +0.6V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL and SDA Input Threshold	V_{IL}				0.4	V
	V_{IH}		1			
I^2C TIMINGS						
Serial Operating Frequency	f_{SCL}				400	kHz
Maximum Clock Period	t_{SCLMAX}		2.5			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
Repeat START Condition Setup Time	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$				0	ns
Data Valid to SCL Rise Time	$t_{SU:DAT}$		100			ns
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs

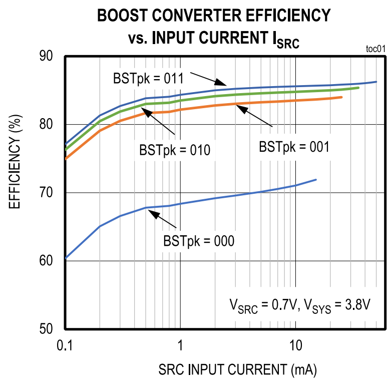
Note 1: All devices 100% productions tested at 25°C. Limits over the operating temperature range are guaranteed by design.

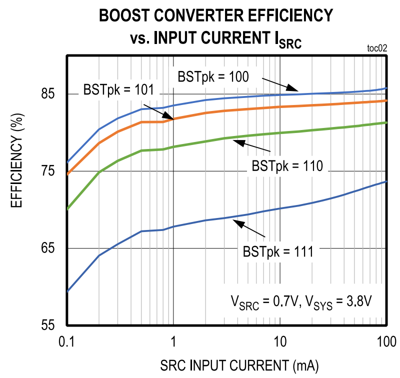
Note 2: All capacitance values listed in this document refer to effective capacitance. Be sure to specify capacitors that meets these requirements under typical system operating conditions, taking into consideration the effects of voltage and temperature.

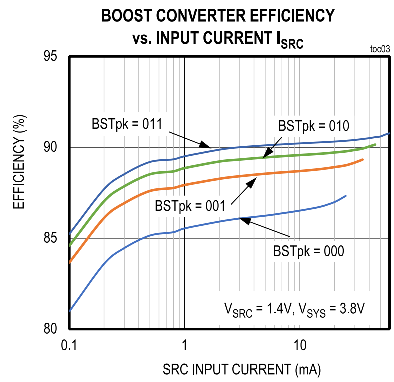
Note 3: Not production tested. Guaranteed by design.

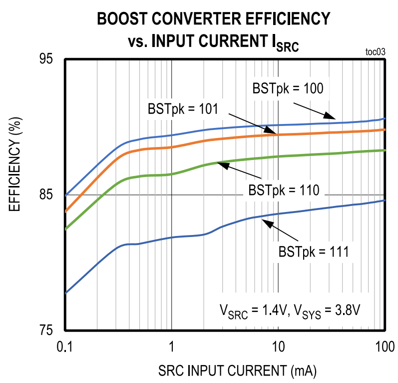
Typical Operating Characteristics

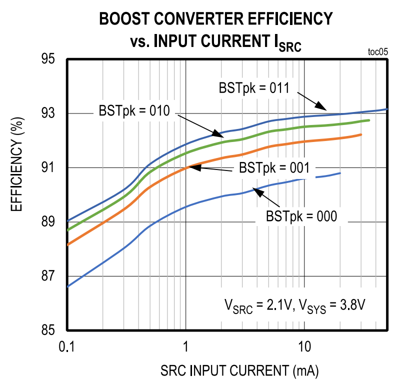
(T_A = 25°C, unless otherwise noted.)

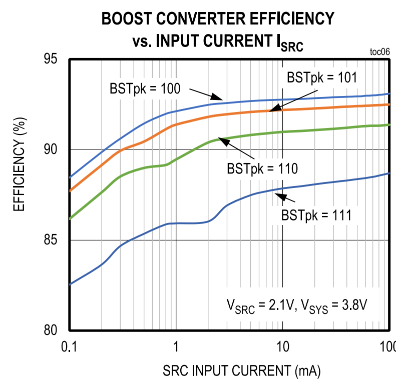


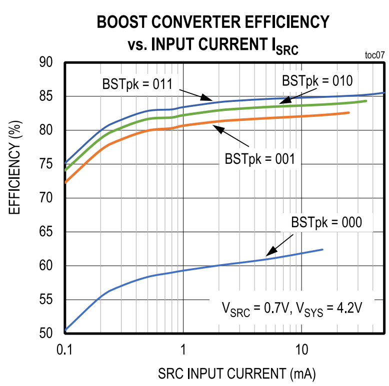


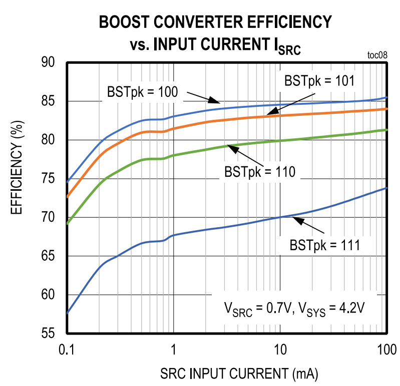


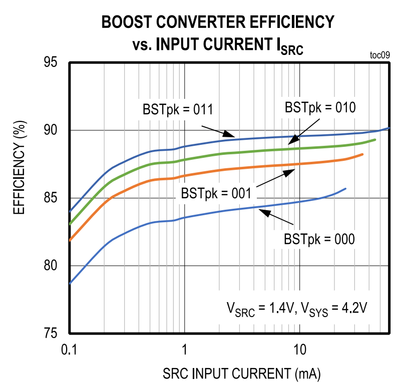












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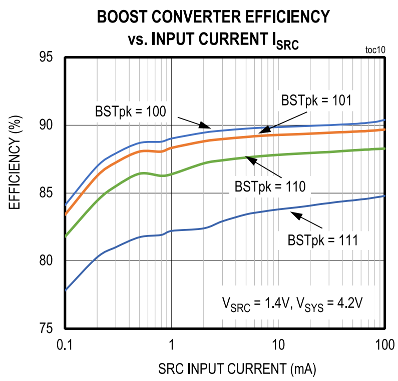

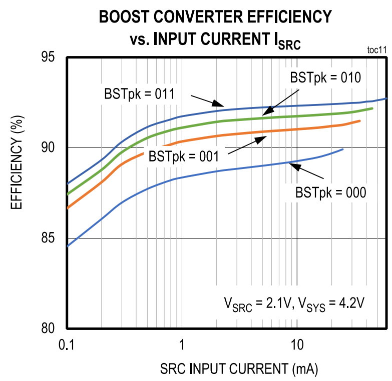

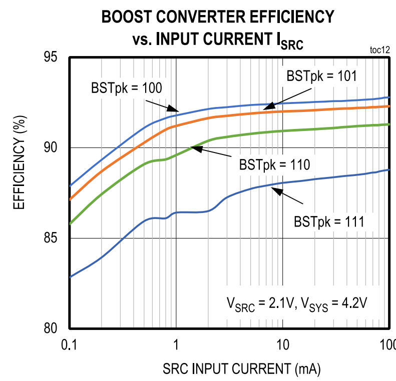

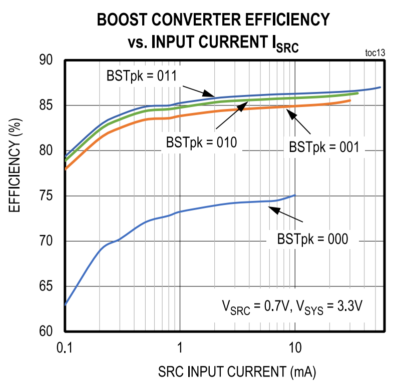

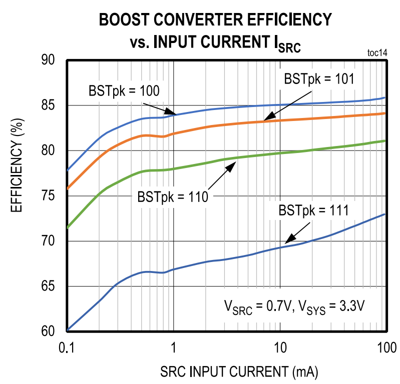

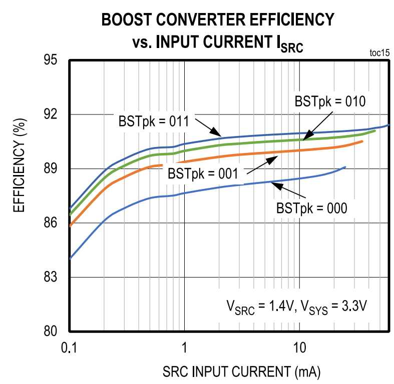

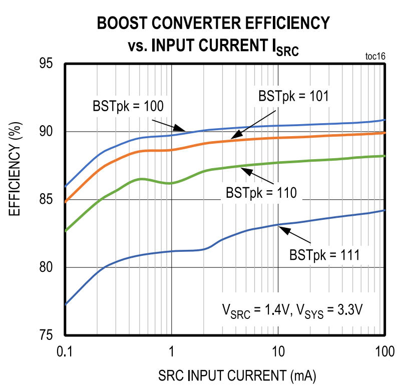

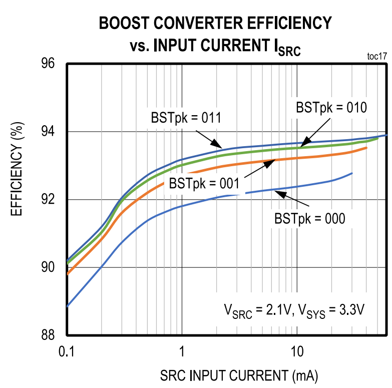

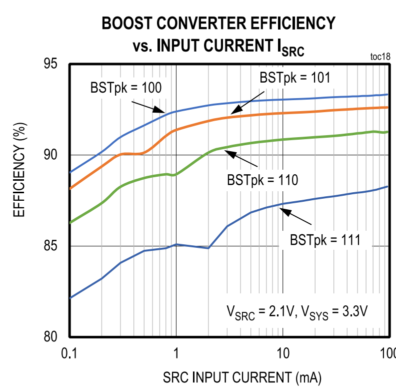

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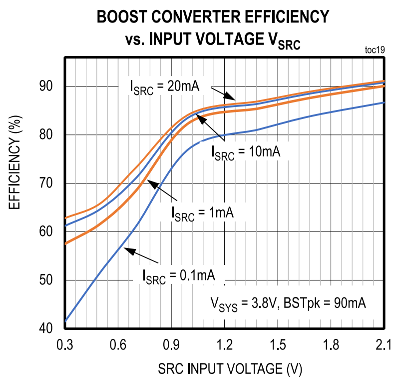

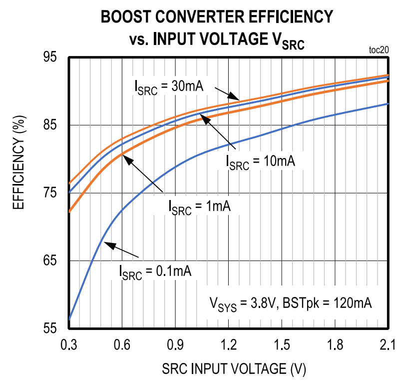

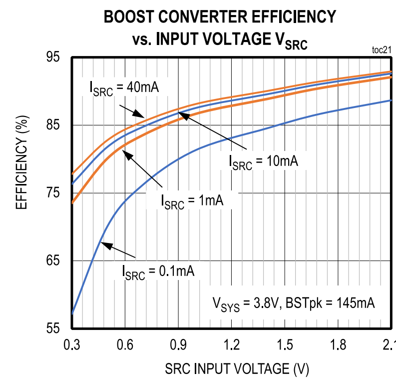

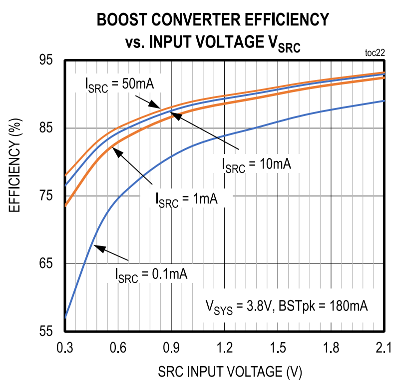

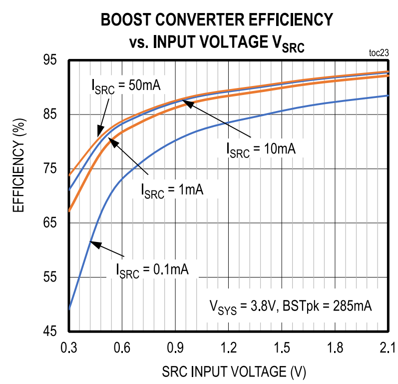

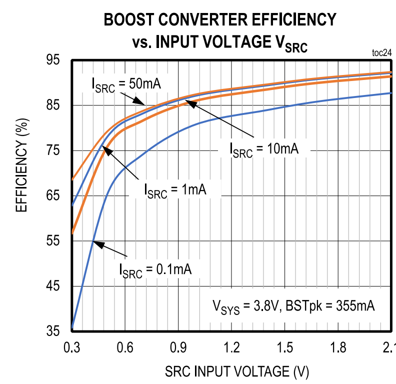

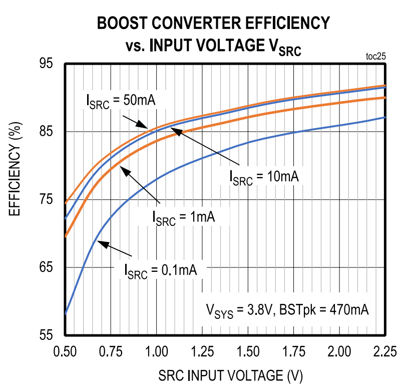

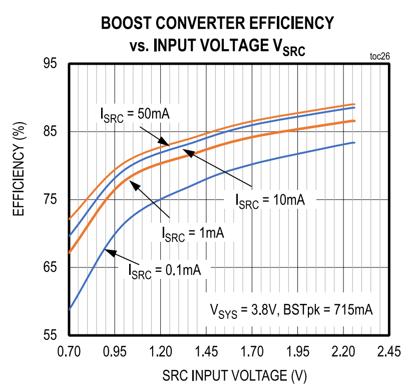

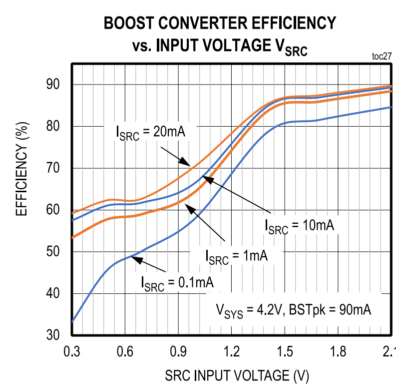

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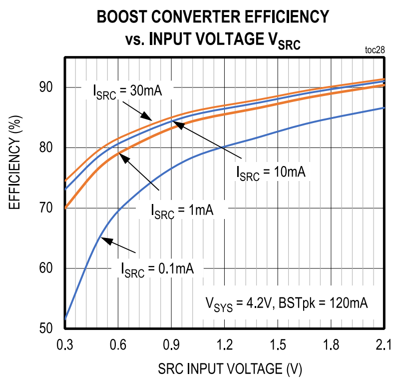

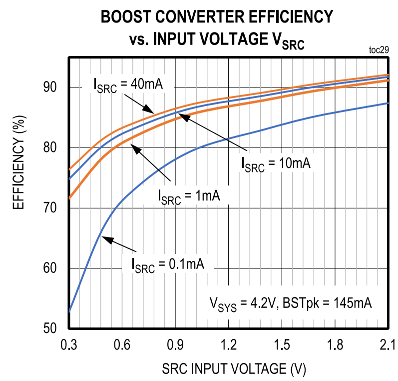

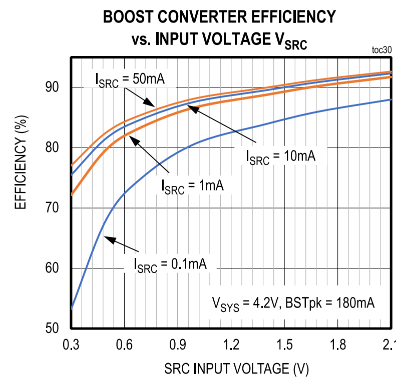

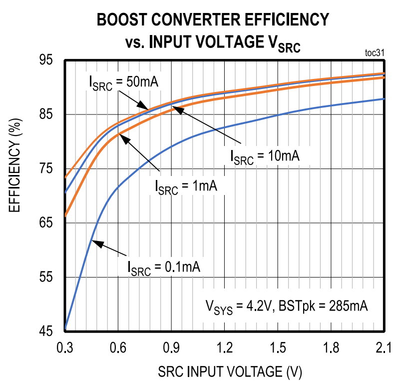

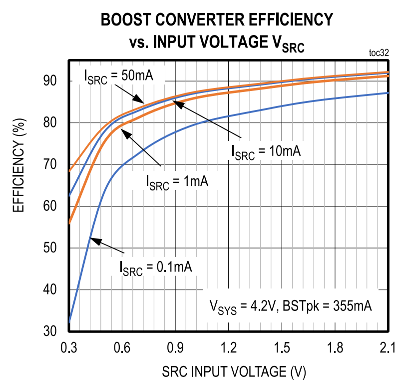

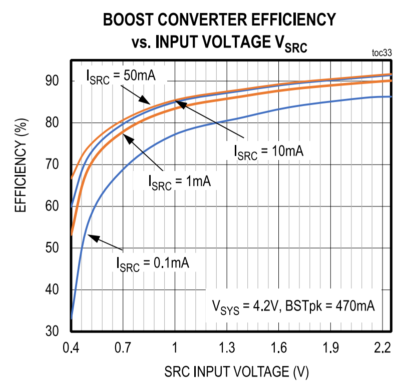

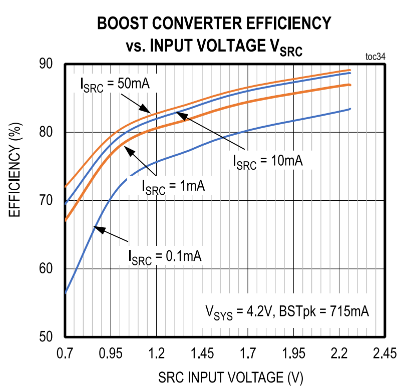

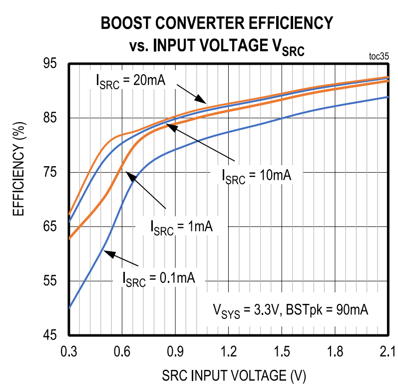

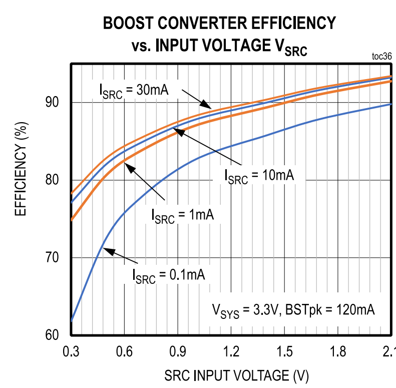

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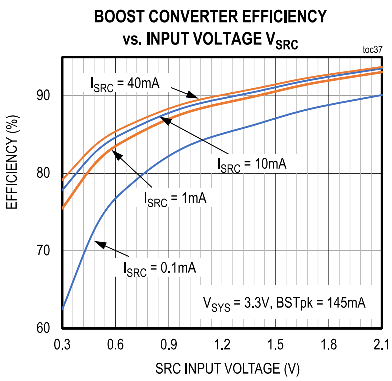
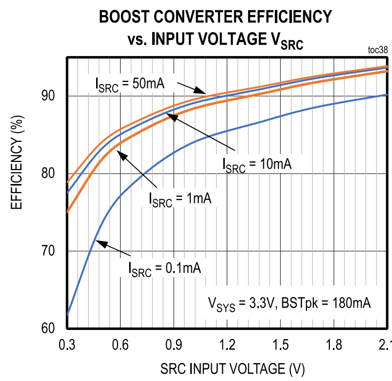
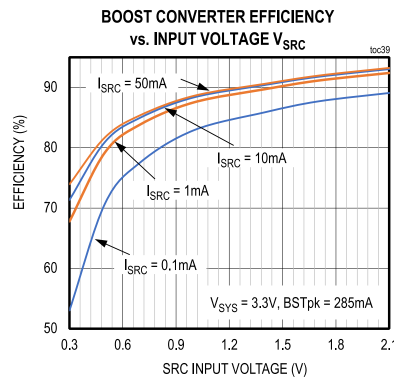
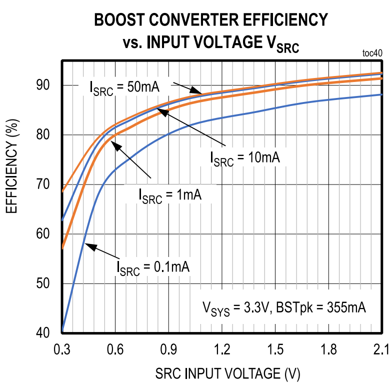
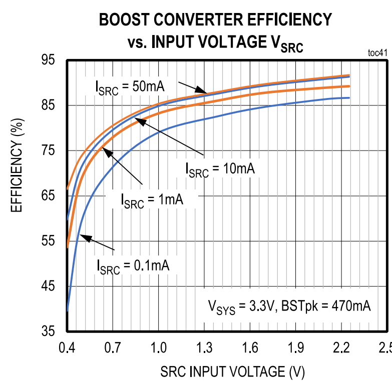
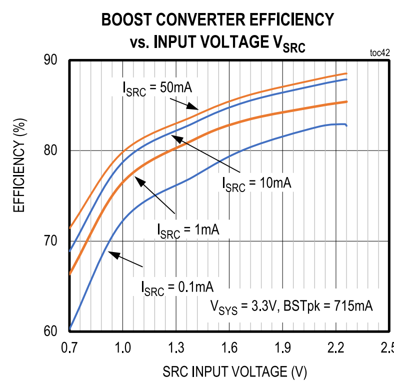




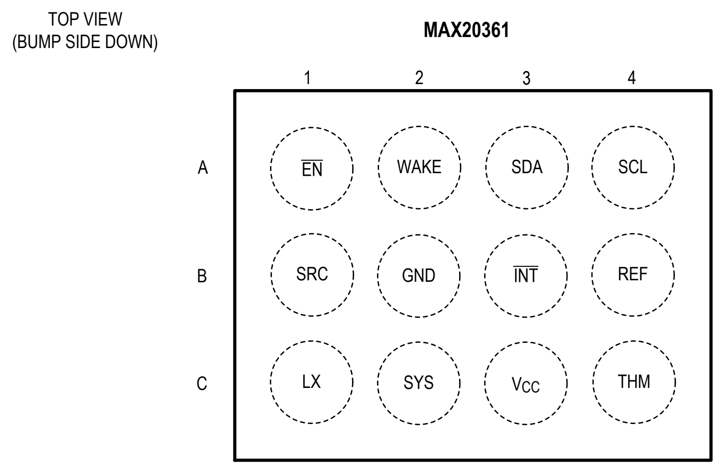








Bump Configuration



WLP

(1.63mm x 1.23mm, 0.4mm PITCH)

Pin Descriptions

PIN	NAME	FUNCTION
A1	$\overline{EN}$	Active Low Enable Input. When $\overline{EN}$ is high the device stops switching and enters a low power state. $\overline{EN}$ is internally pulled down to GND by a 1MΩ resistor. In the shutdown state, I^2C is still operational.
A2	WAKE	Wake Signal for System MCU. This push-pull output is asserted when SYS is above WakeThr[2:0] and the device is not in sleep mode.
A3	SDA	I^2C Serial Data
A4	SCL	I^2C Serial Clock
B1	SRC	Source Input. Connect the harvesting source power output to SRC. Connect a 10μF capacitor between SRC and GND.
B2	GND	Ground
B3	$\overline{INT}$	Open-Drain Interrupt Output
B4	REF	Internal-Voltage Reference
C1	LX	Boost-Converter Switching Node. Connect a 4.7μH inductor between LX and the harvesting source power output (e.g., anode of solar cell).
C2	SYS	System Output. Connect to system input of power management IC. Connect a 1μF bypass capacitor between SYS and GND.
C3	V_{CC}	Internal Supply. Connect a 1μF bypass capacitor between V_{CC} and GND.
C4	THM	Thermistor Input. Connect THM to a voltage divider formed by a pullup resistor and a pulldown thermistor.

Detailed Description

The MAX20361 is a fully integrated solution for harvesting energy from single-/multi-cell solar sources. The device includes an ultra-low quiescent-current boost converter that is capable of starting from input voltage as low as 225mV (typ). In order to maximize the power extracted from the source, the MAX20361 implements a proprietary maximum power point tracking (MPPT) technique that allows efficient harvesting from 15µW to over 300mW of available input power.

The MAX20361 also features an integrated charging and protection circuit that is optimized for Li-ion batteries, but can also be used to charge supercapacitors, thin-film batteries, or traditional capacitors. The charger features a programmable charging cut-off voltage with thresholds programmable through the I^2C interface as well as temperature shutoff.

Boost Converter

The MAX20361 boost converter is optimized to efficiently harvest energy from a single-/multi-cell solar source. The MAX20361 implements a boost converter, which collects the current from the low-voltage SRC input and transfers it to the higher-voltage SYS output.

The switching frequency is not fixed but changes with the SRC voltage, SYS voltage and inductance values. Each time the SRC voltage drops below its regulation point, the boost is halted. SRC capacitance is needed to reduce the SRC ripple, but its value is not critical for stability (see the *Applications Information* section for more details).

The SYS voltage is monitored and when it reaches the regulation point, the boost is halted to avoid overcharging of the the battery, or an overvoltage on the SYS node.

Harvesting Meter

The MAX20361 reports the count of the switching cycles of the boost converter during the last Tmeas[5:4](0x07) time in the HarvCntH(0x0A) and HarvCntL(0x0B) registers. This "harvesting count" is proportional to the current harvested during that period. To avoid a false read, the update of HarvCntH and HarvCntL is inhibited if the boost was halted in the last Tmeas period due to thermal monitoring, open-circuit voltage measurement, SYS overvoltage detected, sleep mode or I^2C commands.

Every time a new valid value of HarvCntH/L is loaded, the HARrdy[4](0x01) bit is set.

Maximum Power Point Tracking (MPPT)

During normal operation, the MAX20361 automatically measures the open-circuit voltage and computes the optimal SRC voltage to transfer the maximum power from the solar cell. Every Tper[1:0](0x07) (by default 64 x Tmeas, with Tmeas = 50ms, every 3.2s), or when requested by I^2C, the internal boost is halted for Tmeas[5:4](0x07) and the SRC voltage is measured with the internal 8-bit ADC.

The SRC regulation point is computed by multiplying the measured voltage at SRC by the Frac[4:0](0x06) field. At power-up, the MAX20361 regulates the SRC voltage at a level determined by the value of Frac[4:0] and the default value of VOC[7:0]. (For example, if Frac[4:0] is set to 80% and the default value of VOC[7:0] is 29 decimal, the SRC regulation voltage is 230mV typical, which is 80% of 290mV) until the first VOC measure or an I^2C write on VOC[7:0] register is performed. Refer to *Figure 1* for the operation of V_{SRC} during MPPT.

To adapt the SRC measurement time, if the ATmeas[3](0x07) bit is set, the MAX20361 modulates the measurement time based on the last measured "harvesting count" (HarvCntH/L registers), as specified in *Table 1* below.

Table 1. Measurement Time Based on Harvesting Count

HARVESTING COUNT VALUE	USED MEASUREMENT TIME
Less than 13	2 x Tmeas
Between 13 and 26	Tmeas
Between 26 and 52	Tmeas / 2
Above 52	Tmeas / 4

The MAX20361 automatically adapts the measurement period when the ATper[2](0x07) bit is set. After power-on reset, the device ignores the first result of harvesting count and stores the second result in the HarvCntH and HarvCntL registers.

If any future harvesting count is greater or lower than the existing stored harvesting count by a factor of 2, the Tper timer is reset and a new VOC measurement is forced immediately.

A VOC measurement can be requested through the FrcMeas[7](0x07) bit. The measurement starts within Tmeas and results are stored in the VOCMeas(0x09) register, and VOCrdy[3](0x01) bit is set with the corresponding interrupt.

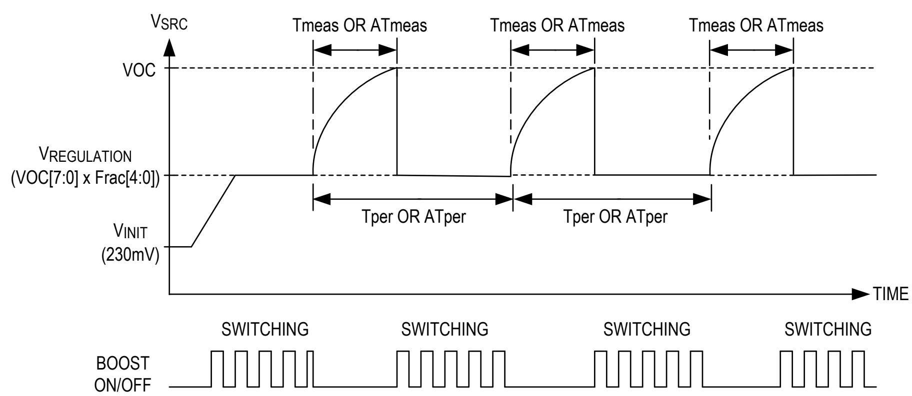


Figure 1. VSRC During Maximum Power Point Tracking

Low-Light Sleep Mode

To save power, the MAX20361 enters sleep mode when the harvesting meter value is below SlpThd[7:0](0x0C) threshold (default 0x00) or when VOC[7:0] is set below the default VOC value by either the VOC measurement or a direct I^2C write to it. In sleep mode, the internal reference, the boost and the THM monitor are turned off, and SYS and THM are not monitored, and WAKE output is forced low. The MAX20361 remains in sleep mode until the next VOC or THM measurement, or a write to VOC[7:0] with a value equal or above the default VOC value. Low-power mode is inhibited during cold startup.

WAKE Output

Except in Shutdown or Sleep modes, the MAX20361 monitors the SYS output. When SYS is above the WAKE threshold for at least 7 to 8 x Tmeas (typ), the WAKE output is asserted (and the WAKEbSt[0](0x01) bit is set to 0). When the device goes into Sleep or Shutdown mode, WAKE output is forced low. Refer to *Figure 2* for the waveform of V_{SYS} and WAKE output.

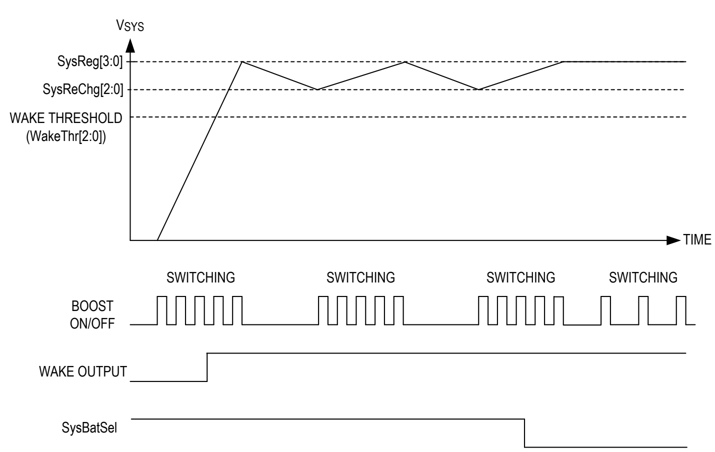


Figure 2. Waveform of VSYS and WAKE Output

Thermal Monitor

When ThmEn[3](0x08) is 1, the MAX20361 monitors the voltage on THM. The device checks V_{THM} once if FrcTHM[6](0x07) is 1 or periodically every Tper[1:0](0x07) time if THMper[6](0x05) is 1. During that process, the MAX20361 drives REF to 1.2V (typ) for 1ms (typ). The voltage divider, formed by the pullup resistor from THM to REF and the NTC thermistor from THM to ground, provides a voltage at THM proportional to the temperature as a fraction of V_{REF}. When V_{THM} is above 57.5% of V_{REF} or below 18.7% of V_{REF}, THMflag[6](0x01) is set and the boost is halted. These thresholds are equivalent to 0°C and 45°C if a 10kΩ NTC thermistor with β = 3380 and a 22kΩ pullup resistor are used.

The device also performs a THM check at power-on and on the $\overline{EN}$ falling edge. A fault condition is assumed until this first THM check is completed.

Shutdown

The device enters Shutdown mode when the $\overline{EN}$ pin is high or DeviceEnb[1](0x08) is 1. In this condition, current consumption is minimized, SYS, THM and SRC are not monitored, WAKE output is forced low and the internal oscillator is turned off. All internal logic, except those values under I^2C, is held in reset. In the shutdown state, only the POR on V_{CC} is active, and the V_{CC}-SYS switch is left open until V_{CC} is above the POR threshold. The device exits Shutdown mode when $\overline{EN}$ is low and DeviceEnb is 0.

Cold-Startup

The cold start feature of the MAX20361 allows the device to start up even if V_{SYS} is below the wake threshold or absent. For a cold startup, the device initially uses a low power charge pump to charge up V_{CC} from the power source (such as a solar cell) on SRC while SYS is not charged. Once V_{CC} is charged above the POR level, the internal references are enabled and the main boost takes over from the charge pump. As the main boost continues to charge, V_{CC} and SYS gets charged above the wake threshold, the V_{CC}-SYS switch is closed and the device is powered from SYS. This completes the cold startup, and the normal operation of the device assumes.

Source Clamp

By the DISintb[4](0x05) bit, the $\overline{INT}$ output can be reconfigured as a push-pull DISsrc output to drive an external clamp circuit used to prevent overvoltage on SRC. The clamp circuit (see *Figure 3*) can be formed by an external nMOS and a load resistor. When the clamp circuit is turned on, the SRC is discharged through the external load resistor. When the boost converter is enabled, the DISsrc is driven to divert excess input current in order to let SRC regulate. In shutdown mode, the DISsrc output is driven statically high. The DISsrc output is disabled during VOC measurement and sleep mode. Refer to the *nMOS Transistor Selection* section.

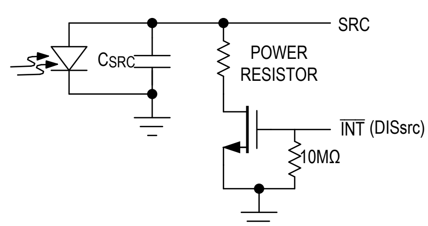


Figure 3. Source Clamp Circuitry

I2C Interface

The MAX20361 contains an I2C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

When writing to the MAX20361 using I2C, the master sends a START condition (S) followed by the MAX20361 I2C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I2C slave.

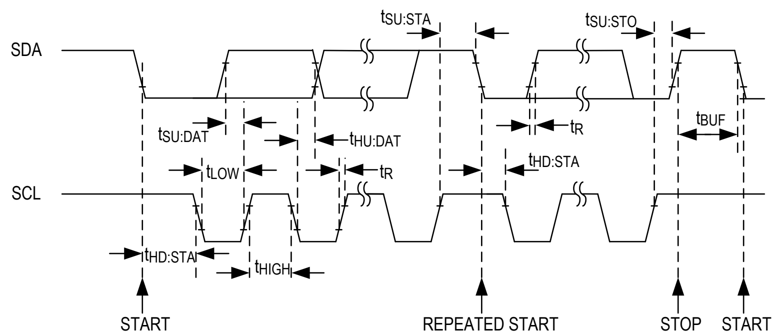


Figure 4. I2C Interface Timing

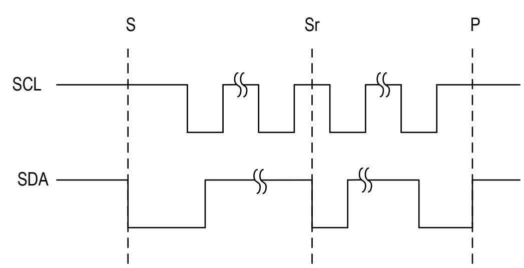


Figure 5. I2C START, STOP, and REPEATED START Conditions

Slave Address

Set the Read/Write bit high to configure the MAX20361 to read mode (see *Table 2*). Set the Read/Write bit low to configure the MAX20361 to write mode. The address is the first byte of information sent to the MAX20361 after the START condition.

Table 2. I2C Slave Addresses

ADDRESS FORMAT	HEX	BINARY
7-Bit Slave ID	0x15	0010101
Write Address	0x2A	00101010
Read Address	0x2B	00101011

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the Start, Stop, And Repeated Start Conditions section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device. The following procedure describes the single byte write operation:

1. The master sends a START condition.
2. The master sends the 7-bit slave address plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6. The master sends 8 data bits.
7. The slave asserts an ACK on the data line.
8. The master generates a STOP condition.

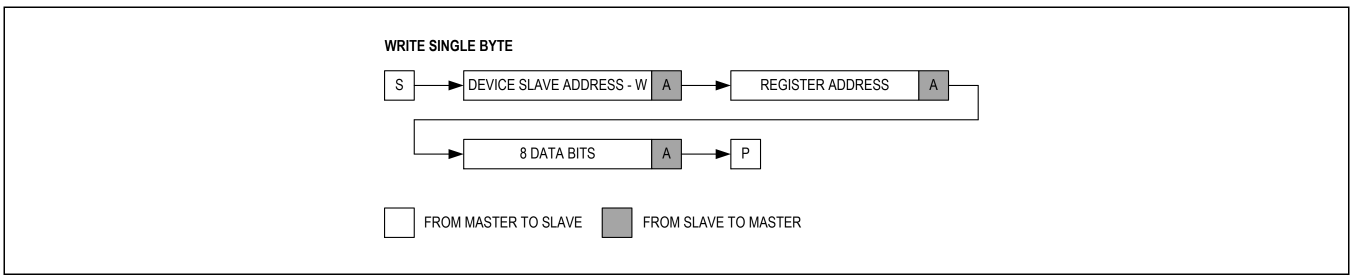


Figure 6. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device. The slave device automatically increments the register address after each data byte is sent. The following procedure describes the burst write operation:

1. The master sends a START condition.
2. The master sends the 7-bit slave address plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6. The master sends eight data bits.
7. The slave asserts an ACK on the data line.
8. Repeat 6 and 7 N-1 times.
9. The master generates a STOP condition.

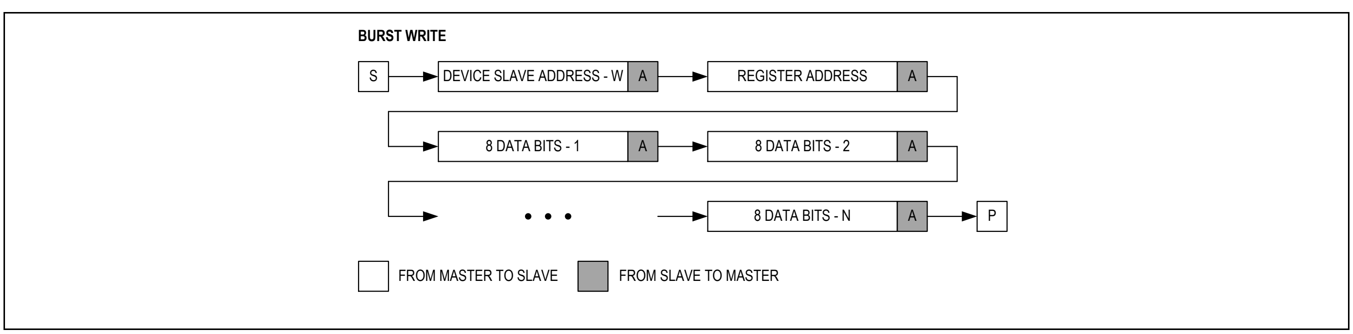


Figure 7. Burst Write Sequence

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device. The following procedure describes the single byte read operation:

1. The master sends a START condition.
2. The master sends the 7-bit slave address plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6. The master sends a REPEATED START condition.
7. The master sends the 7-bit slave address plus a read bit (high).bz
8. The addressed slave asserts an ACK on the data line.
9. The slave sends eight data bits.
10. The master asserts a NACK on the data line.
11. The master generates a STOP condition.

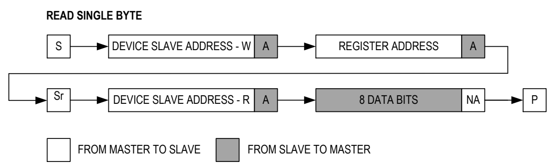


Figure 8. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device. The following procedure describes the burst byte read operation:

1. The master sends a START condition.
2. The master sends the 7-bit slave address plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6. The master sends a REPEATED START condition.
7. The master sends the 7-bit slave address plus a read bit (high).
8. The slave asserts an ACK on the data line.
9. The slave sends eight data bits.
10. The master asserts an ACK on the data line.
11. Repeat 9 and 10 N-2 times.
12. The slave sends the last eight data bits.
13. The master asserts a NACK on the data line.
14. The master generates a STOP condition.

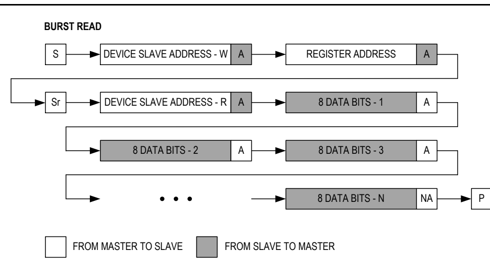


Figure 9. Burst Read Sequence

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX20361 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse. To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

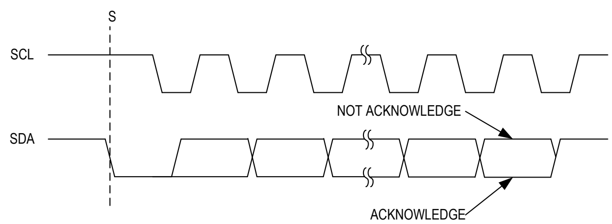


Figure 10. Acknowledge Bits

Register Map

MAX20361

ADDRESS	NAME	MSB							LSB
User Registers									
0x00	DeviceID[7:0]	ChipID[3:0]				ChipRev[3:0]			
0x01	Status[7:0]	VOCValid	THMflag	HSYSFlag	HARrdy	VOCrdy	Sleep	ENbStat	WAKEbSt
0x02	Int[7:0]	–	–	–	HARrdyInt	VOCrdyInt	VOCValidInt	EnbStatInt	WakebStInt
0x03	IntMsk[7:0]	–	–	–	HARrdyMsk	VOCrdyMsk	VOCValidMsk	EnbStatMsk	WakebStMsk
0x04	SysRegCfg[7:0]	SysBatSel	SysReChg[2:0]			SysReg[3:0]			
0x05	WakeCfg[7:0]	VOCper	THMper	–	DISintb	–	WakeThr[2:0]		
0x06	MpptCfg[7:0]	–	–	–	Frac[4:0]				
0x07	MeasCfg[7:0]	FrcMeas	FrcTHM	Tmeas[1:0]		ATmeas	ATper	Tper[1:0]	
0x08	DevCntl[7:0]	–	BSTpk[2:0]			ThmEn	FrcWAKE	DeviceEnb	BoostEnb
0x09	VOCMeas[7:0]	VOC[7:0]							
0x0A	HarvCntH[7:0]	HARhigh[7:0]							
0x0B	HarvCntL[7:0]	HARlow[7:0]							
0x0C	SleepThd[7:0]	SlpThd[7:0]							

Register Details

DeviceID (0x00)

BIT	7	6	5	4	3	2	1	0
Field	ChipID[3:0]				ChipRev[3:0]			
Reset	0x1				0x1			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
ChipID	7:4	Chip Identification
ChipRev	3:0	Chip Revision

Status (0x01)

BIT	7	6	5	4	3	2	1	0
Field	VOCValid	THMflag	HSYSFlag	HARrdy	VOCrdy	Sleep	ENbStat	WAKEbSt
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
VOCValid	7	Indicates if at least one SRC open-circuit measurement was performed since the last V_{CC} POR event. This bit is also reset when a write to the VOCMeas register is performed.This bit is not set after a VOC measurement. 0b0: No SRC open-circuit measurement was performed since the last V_{CC} POR event. 0b1: At least one SRC open-circuit measurement was performed since the last V_{CC} POR event.
THMflag	6	THM Fault Status 0b0: No THM fault detected 0b1: THM fault detected during the last Tmeas period
HSYSFlag	5	SysReg Overvoltage Fault Flag 0b0: V_{SYS} is not over V_{SYS_REG} 0b1: V_{SYS} is over V_{SYS_REG}
HARrdy	4	Harvest Meter Status 0b0: Harvest meter has not been updated since the last read of HarvCnth/L register. 0b1: Harvest meter has been updated since the last read of HarvCnth/L register. *Note: this bit is reset when the HarvCntH register is read.*
VOCrdy	3	Open-Circuit Voltage Status 0b0: No new open-circuit voltage measurement since the last read of VOCMeas register. 0b1: New open-circuit voltage available since the last read of VOCMeas register.
Sleep	2	Indicates if the Device is in Sleep Mode

BITFIELD	BITS	DESCRIPTION
		0b0: Device is not in sleep mode and it is harvesting. 0b1: Device is in sleep mode to save SYS power (no harvesting).
ENbStat	1	Indicates if the Device is in Shutdown (or Between ENb Pin Input and DeviceEnb Bit) 0b0: ENb pin low and DeviceEnb bit set to 0. 0b1: ENb pin high or DeviceEnb bit set to 1.
WAKEbSt	0	Indicates the Status of the WAKE Pin Output Only the SYS comparator; does not include the FrcWAKE). This bit is not valid if the Sleep flag is set. 0b0: WAKE pin high (SYS above WakeThr[2:0](0x05) threshold) 0b1: WAKE pin low (SYS below WakeThr[2:0](0x05) threshold)

Int (0x02)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	HARrdyInt	VOCrdyInt	VOCValidInt	EnbStatInt	WakebStInt
Reset	–	–	–	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
HARrdyInt	4	HARrdy Interrupt 0b0: No change in status of HARrdy 0b1: Change in status of HARrdy
VOCrdyInt	3	VOCrdy Interrupt 0b0: No change in status of VOCrdy 0b1: Change in status of VOCrdy
VOCValidInt	2	VOCValid Interrupt 0b0: No change in status of VOCValid 0b1: Change in status of VOCValid
EnbStatInt	1	EnbStat Interrupt 0b0: No change in status of EnbStat 0b1: Change in status of EnbStat

BITFIELD	BITS	DESCRIPTION
WakebStInt	0	WakebSt Interrupt 0b0: No change in status of WakebSt 0b1: Change in status of WakebSt

IntMsk (0x03)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	HARrdyMsk	VOCrdyMsk	VOCValidMsk	EnbStatMsk	WakebStMsk
Reset	–	–	–	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
HARrdyMsk	4	HARrdyInt Interrupt Mask 0b0: HARrdy interrupt not masked 0b1: HARrdy interrupt masked
VOCrdyMsk	3	VOCrdy Interrupt Mask 0b0: VOCrdy interrupt not masked 0b1: VOCrdy interrupt masked
VOCValidMsk	2	VOCValid Interrupt Mask 0b0: VOCValid interrupt not masked 0b1: VOCValid interrupt masked
EnbStatMsk	1	EnbStat Interrupt Mask 0b0: EnbStat interrupt not masked 0b1: EnbStat interrupt masked
WakebStMsk	0	WakebSt Interrupt Mask 0b0: WakebSt interrupt not masked 0b1: WakebSt interrupt masked

SysRegCfg (0x04)

BIT	7	6	5	4	3	2	1	0
Field	SysBatSel	SysReChg[2:0]			SysReg[3:0]			

Reset	0x0	0x0	0x7
Access Type	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SysBatSel	7	Selects Regulation Mode of SYS 0b0: The boost attempts to regulate the SYS node at V_{SysReg}. 0b1: The boost charges the SYS node until it reaches V_{SysReg} and then switches off until SYS drops to V_{SysReg} - $V_{SysReChg}$.
SysReChg	6:4	Battery Recharge Threshold Voltage 0b000: 25mV 0b001: 50mV 0b010: 75mV 0b011: 100mV 0b100: 150mV 0b101: 200mV 0b110: 250mV 0b111: 300mV
SysReg	3:0	System Regulation or Battery Termination Voltage On the SYS Node 0b0000: 4.0V … linear step, 50mV 0b1111: 4.75V

WakeCfg (0x05)

BIT	7	6	5	4	3	2	1	0
Field	VOCper	THMper	–	DISintb	–	WakeThr[2:0]		
Reset	0x1	0x0	–	0x0	–	0x7		
Access Type	Write, Read	Write, Read	–	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
VOCper	7	VOC Every Tper (Perform Open Circuit Measurement Every Tper Period) 0b0: VOC measurement performed only on request 0b1: VOC measurement performed every "Tper" time *Note: this bit also disables the first VOC measurement after POR.*
THMper	6	Thermal Monitor Every Tper

BITFIELD	BITS	DESCRIPTION
		0b0: Thermal monitoring is not performed every Tper time. 0b1: Thermal monitoring is performed every Tper time (only if also ThmEn is set).
DISintb	4	Disable the INTb Pin and Convert It Into a Push-Pull Output to Discharge SRC (Clamp SRC Voltage) 0b0: INTb is an open-drain output for interrupt. 0b1: INTb becomes a DISsrc push-pull output (to V_{CC}). When high, discharge SRC through a resistor.
WakeThr	2:0	Wake Threshold. When BAT reaches this voltage, the device asserts the WAKE output. 0b000: 3.0V 0b001: 3.1V 0b010: 3.2V 0b011: 3.3V 0b100: 3.4V 0b101: 3.5V 0b110: 3.6V 0b111: 3.7V

MpptCfg (0x06)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	Frac[4:0]				
Reset	–	–	–	0x19				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
Frac	4:0	Set the Fraction of the Open-Circuit Voltage to which the Boost Converter Attempts to Regulate at V_{SRC}. 0b00000: 42.5% …Linear scale, 1.5% / LSB 0b11111: 89.0%

MeasCfg (0x07)

BIT	7	6	5	4	3	2	1	0
Field	FrcMeas	FrcTHM	Tmeas[1:0]		ATmeas	ATper	Tper[1:0]	
Reset	0x0	0x0	0x0		0x1	0x1	0x2	

Access Type	Write Only Clears All	Write Only Clears All	Write, Read		Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
FrcMeas	7	Writing 1 to this bit forces a measure of an open-circuit voltage measurement (if NoVOCMeas is 0) at SRC. This bit is automatically forced to 0. The measurement algorithm and time for VOC at SRC is set by ATmeas and Tmeas bits. Until FrcMeas is set, the VOC register should not be written.
FrcTHM	6	Writing 1 to this bit forces a measure of thermal monitoring (only if ThmEn bit is 1). This bit is automatically forced to 0.
Tmeas	5:4	Set the Measurement Time 0b00: 50ms 0b01: 100ms 0b10: 250ms 0b11: 500ms
ATmeas	3	Set the Algorithm Used to Adjust the Settling Time for VOC Measure 0b0: The settling time is fixed and set by Tmeas bits. 0b1: Adaptative measuring time based on the current HarvCnt value, from Tmeas / 4 to 2 x Tmeas.
ATper	2	Adaptative Period (Valid Only If Tper < 0b11) 0b0: Disabled 0b1: Store HarvCntH/L after 2 x Tmeas (or more, see text). A measure is forced (if not in sleep) when the future harvesting value is greater or lower than the existing stored measurement by a factor of 2 (future HarvCnt/current HarvCnt < 0.5 or future HarvCnt/current HarvCnt > 2).
Tper	1:0	Set the Period of Automatic Measurement 0b00: 64 x Tmeas 0b01: 128 x Tmeas 0b10: 256 x Tmeas 0b11: Disabled When “Disabled”, VOC and THM are never automatically read. The system should periodically use the FrcMeas and FrcTHM bit to force measurements.

DevCntl (0x08)

BIT	7	6	5	4	3	2	1	0
Field	–	BSTpk[2:0]			ThmEn	FrcWAKE	DeviceEnb	BoostEnb

Reset	–	0x3	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BSTpk	6:4	Select the Peak Current for The Boost Converter 0b000: 90mA 0b001: 120mA 0b010: 145mA 0b011: 180mA 0b100: 285mA 0b101: 355mA 0b110: 470mA 0b111: 715mA
ThmEn	3	Thermal Monitoring Enable Bit 0b0: Thermal monitoring is not enabled, and temperature does not affect boost operation. 0b1: Thermal monitoring is enabled. The thermal monitoring circuit on every Tper period (if THMper is set) or when FrcTHM is set, and if necessary, turns off the boost converter to halt charging of the battery.
FrcWAKE	2	I²C Control of The WAKE Output 0b0: WAKE output is controlled by the WAKE comparator. 0b1: WAKE output is high regardless of the status of the WAKE comparator.
DeviceEnb	1	I²C Control of Device Enable 0b0: Device enable is controlled by the ENb pin. 0b1: Device disabled regardless of the status of the ENb pin.
BoostEnb	0	I²C Enable of the Boost Converter 0b0: Boost converter is controlled by the internal digital logic. 0b1: Boost converter is disabled regardless of the internal digital logic.

VOCMeas (0x09)

BIT	7	6	5	4	3	2	1	0
Field	VOC[7:0]							
Reset	0x1D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VOC	7:0	Most Recent Result of Open-Circuit Voltage Measurement at SRC. This value can be read anytime without triggering the FrcMeas bit. 0: 0V … 255: 2.55V This register can be written to override the VOC measure. Every time the VOC register is updated to value below the default VOC value (either by VOC measurement or by I²C writing), the boost is halted and sleep mode is entered to save power, until the next VOC measurement (upon Tper or FrcVOC) or until VOC is written to a higher value. The VOC register should not be written to when FrcMeas is set.

HarvCntH (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	HARhigh[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HARhigh	7:0	Return the Number of “LX Pulses” of the Boost, the only 8 MSBits of Counter. This number is valid only when SYS is above the WAKE threshold. This number is proportional to the SYS “charging” current. When the counter overflows, it returns to 0xFFFF. *Note: the HarvCnt is not updated when the device is in sleep mode.*

HarvCntL (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	HARlow[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HARlow	7:0	Return the Number of “LX Pulses” of the Boost, the only 8 LSBs of the Counter. This number is valid only when SYS is above WAKE threshold. This number is

BITFIELD	BITS	DESCRIPTION
		proportional to the SYS "charging" current. When the counter overflows, it returns to 0xFFFF.

SleepThd (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	SlpThd[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SlpThd	7:0	The "Harvesting Count" Threshold to Enter Sleep Mode Until the Next VOC Measure. This value is compared with the HarvCnt (the bits returned in registers HarvCntH/L). This feature is ignored if SlpThd = 0.

Applications Information

Inductor Selection

The operation of the boost regulator requires a properly sized inductor with the appropriate value. The inductor must be connected between SRC (pin B1) and LX (pin C1). The boost regulator performance, such as efficiency, is optimized to control the switching behavior with a nominal inductance of 4.7μH ± 20%. The inductor must have low series resistance (DCR) to minimize loss and maintain high efficiency. The recommended inductance range is between 4.7μH and 22μH. Refer to *Table 3* for a list of recommended inductors.

Table 3. Boost Regulator Inductor Recommendation

INDUCTANCE (μH)	DIMENSIONS (mm)	PART NUMBER	MANUFACTURER
4.7	2 x 1.6 x 1.2	DFE201612E-4R7M=P2	Murata
4.7	2.5 x 2 x 1	DFE252010F-4R7M=P2	Murata
4.7	4.8 x 4.8 x 3	744043004	Wurth
15	3.8 x 3.8 x 1.8	744031150	Wurth
22	7.3 x 7.3 x 4.5	7447779122	Wurth

Capacitor Selection

All selected capacitors need to have low leakage. Any leakage from capacitors contributes to the loss of efficiency, increases the quiescent current, and reduces the effectiveness of the energy harvesting process. The capacitance specified in the data sheet refers to the effective capacitance after accounting for the voltage derating. Small ceramic capacitors tend to lose effective capacitance very quickly as DC bias is increased. Ensure that DC degradation would not affect the effective capacitance of bypass capacitors located at V_{CC}, SRC, and SYS.

SRC Capacitance

The capacitor connected to pin SRC (C_{SRC}) is used to initially store energy from the harvesting input source. The output capacitance of the input energy source determines the value of the SRC capacitor. A minimum effective capacitance of 10μF is recommended. Larger capacitance (22μF) is recommended for 10μH and 22μH inductances.

SYS and V_{CC} Capacitance

Connect a bypass capacitor to the system output (C_{SYS}) of the MAX20361. This capacitor needs to have low equivalent series resistance (ESR). An effective capacitance of 1μF is recommended.

nMOS Transistor Selection

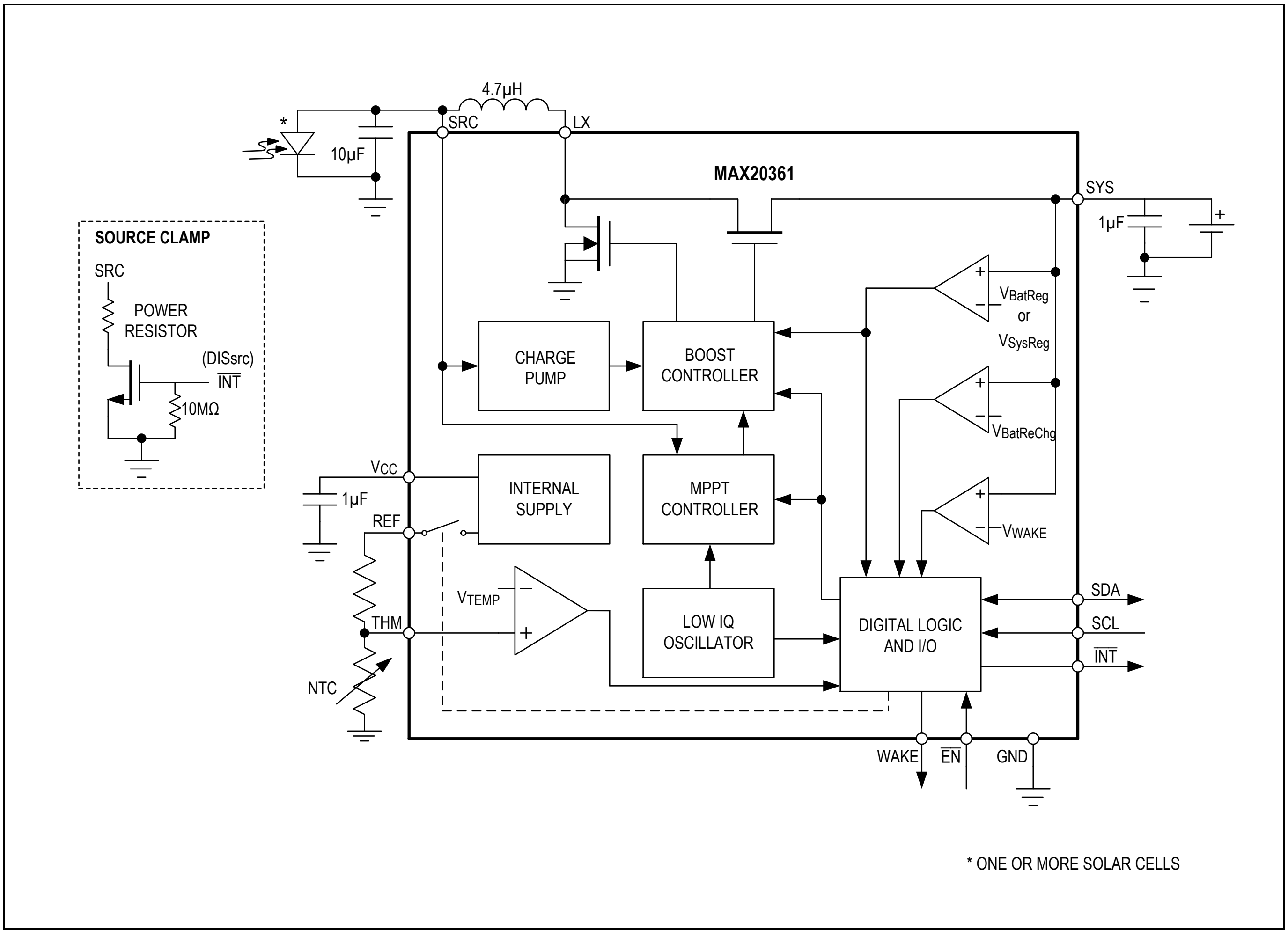
See *Table 4* for a list of recommended nMOS transistors used for the source clamp circuitry. The gate to source threshold voltage and drive voltage must be lower than 2V for this application.

Table 4. nMOS Transistor Recommendation

MANUFACTURER	PART NUMBER	DRAIN-TO-SOURCE VOLTAGE (V)	CONTINUOUS-DRAIN CURRENT (A)	GATE-TO-SOURCE VOLTAGE THRESHOLD (V)	DRIVE VOLTAGE (V)
Diodes Incorporated	DMN2230U-7	20	2	1	1.8
ON Semiconductor	FDMA410NZ	20	9.5	1	1.5
Diodes Incorporated	DMC1028UVT-7	12	6.1	1	1.8

Typical Application Circuits

Solar Application Circuit



Register Bit Default Values

Table 5 shows the default settings for different versions. These default values are OTP programmable. Some bits can be changed through the I2C interface after power-up, while some bits are set through OTP.

Table 5. Device Default Settings

REGISTER BITS	MAX20361A	MAX20361B	MAX20361C	MAX20361D
SysBatSel	0	0	0	0
SysReChg [2:0]	25mV	25mV	25mV	25mV
SysReg [3:0]	4.35V	4.1V	4.1V	4.1V
BSTpk0[2:0]	3	3	3	3
ThmEn	Disabled	Enabled	Disabled	Enabled
WakeThr [2:0]	3.7V	3.1V	3.7V	3.1V
Frac [4:0]	80.0%	80.0%	80.0%	80.0%
VOCper	Enabled	Enabled	Enabled	Enabled
THMper	Disabled	Enabled	Disabled	Enabled
Tmeas[1:0]	50ms	50ms	50ms	50ms
ATmeas	1	1	1	1
ATper	Enabled	Enabled	Enabled	Enabled
Tper [1:0]	0b10	0b10	0b10	0b10
VOC [7:0]	0.29V	0V	0.29V	0.05V
SlpThd [7:0]	0V	0V	0V	0V

Register Default Values

Table 6 shows the default values of all the registers.

Table 6. I2C Direct Register Defaults

REGISTER ADDRESS	REGISTER NAME	MAX20361A	MAX20361B	MAX20361C	MAX20361D
0x00	DeviceID	0x11	0x11	0x11	0x11
0x01	Status	0x00	0x00	0x00	0x00
0x02	Int	0x00	0x00	0x00	0x00
0x03	IntMsk	0x00	0x00	0x00	0x00
0x04	SysRegCfg	0x07	0x02	0x02	0x02
0x05	WakeCfg	0x87	0xC1	0x87	0xC1
0x06	MpptCfg	0x19	0x19	0x19	0x19
0x07	MeasCfg	0x0E	0x0E	0x0E	0x0E
0x08	DevCntl	0x30	0x38	0x30	0x38
0x09	VOCMeas	0x1D	0x00	0x1D	0x05
0x0A	HarvCntH	0x00	0x00	0x00	0x00
0x0B	HarvCntL	0x00	0x00	0x00	0x00
0x0C	SleepThd	0x00	0x00	0x00	0x00

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX20361AEWC+	-40°C to +85°C	12 WLP
MAX20361AEWC+T	-40°C to +85°C	12 WLP
MAX20361BEWC+	-40°C to +85°C	12 WLP
MAX20361BEWC+T	-40°C to +85°C	12 WLP
MAX20361CEWC+	-40°C to +85°C	12 WLP
MAX20361CEWC+T	-40°C to +85°C	12 WLP
MAX20361DEWC+	-40°C to +85°C	12 WLP
MAX20361DEWC+T	-40°C to +85°C	12 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/20	Release for Market Intro	—
1	9/20	Updated the General Description, Benefits and Features, Electrical Characteristics, and Detailed Description	1, 4, 13
2	12/22	Added Table 5 and Table 6. Added MAX20361BEWC+ and MAX20361BEWC+T in Ordering Information	31, 32
3	3/23	Updated Maximum Power Point Tracking section, Low-Light Sleep Mode section, and VOC register. Added MAX20361CEWC+ and MAX20361CEWC+T in Table 5 and Table 6 and Ordering Information.	13, 14, 28, 32, 33
4	5/23	Updated HSYSFlag description in Register Map.	21
5	8/23	Added MAX20361DEWC+ and MAX20361DEWC+T in Table 5, Table 6, and Ordering Information.	32,33