Product Document

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TSL2585

Miniature Ambient Light Sensor with UV and Light Flicker Detection

General Description

The TSL2585 incorporates Photopic, IR and UV photodiodes that are connected to 3 modulators, provides concurrent ambient light sensing, UV sensing and light flicker detection. The device comes in a low-profile and small footprint, L2.0mm x W1.0mm x H0.35mm OLGA package.

The Photopic photodiode area is covered with an optimized Photopic filter. In association with dedicated IR channel, this architecture accurately measures ambient light and enables the calculation of irradiance of different light sources. Calculation results help to automatically optimize display brightness under different lighting conditions for a better user experience.

The device also integrates functionality of ambient light flicker detection. It is executed in parallel with ambient light sensing by using the same photodiodes. The flicker detection engine will sample and buffer data for calculating flicker frequencies externally on a host CPU.

The UV photodiode area is covered with a band-pass UV filter. In combination with Photopic and IR channels, it is possible to estimate ambient UV index by running an algorithm externally on a host CPU.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2585 are listed below:

Figure 1:
Added Value of Using TSL2585

Benefits	Features

• Invisible ALS sensing under any glass type	• Configurable, high sensitivity
	  • Programmable gain and integration time
	  • 4096x dynamic range by gain adjustment only
	  • 1mlux detectable illuminance
	• Tailored ALS response
	  • Photopic filter for visible channel
	  • Independent IR channel
	• ALS interrupt with thresholds

• Integrated light flicker detection on chip	• Concurrent flicker and ALS measurement with new simplified readout methodology • Independently configurable sample time • Up to 7kHz flicker detection (14kHz sampling) • FIFO buffer interrupt
• Auxiliary information for ambient UV index estimation	• UVA channel with independent and programmable channel gain • Photopic filter for visible channel • Independent IR channel
• Low power consumption and minimum I²C traffic	• 1.8V_{DD} operation • Configurable sleep mode • Interrupt-driven device • I²C interface up to 1Mbit/s (Fast mode)
• Integrated status checking for all functions	• Digital and analog saturation flags
• Reduced I²C bus traffic load	• On chip data compression

Applications

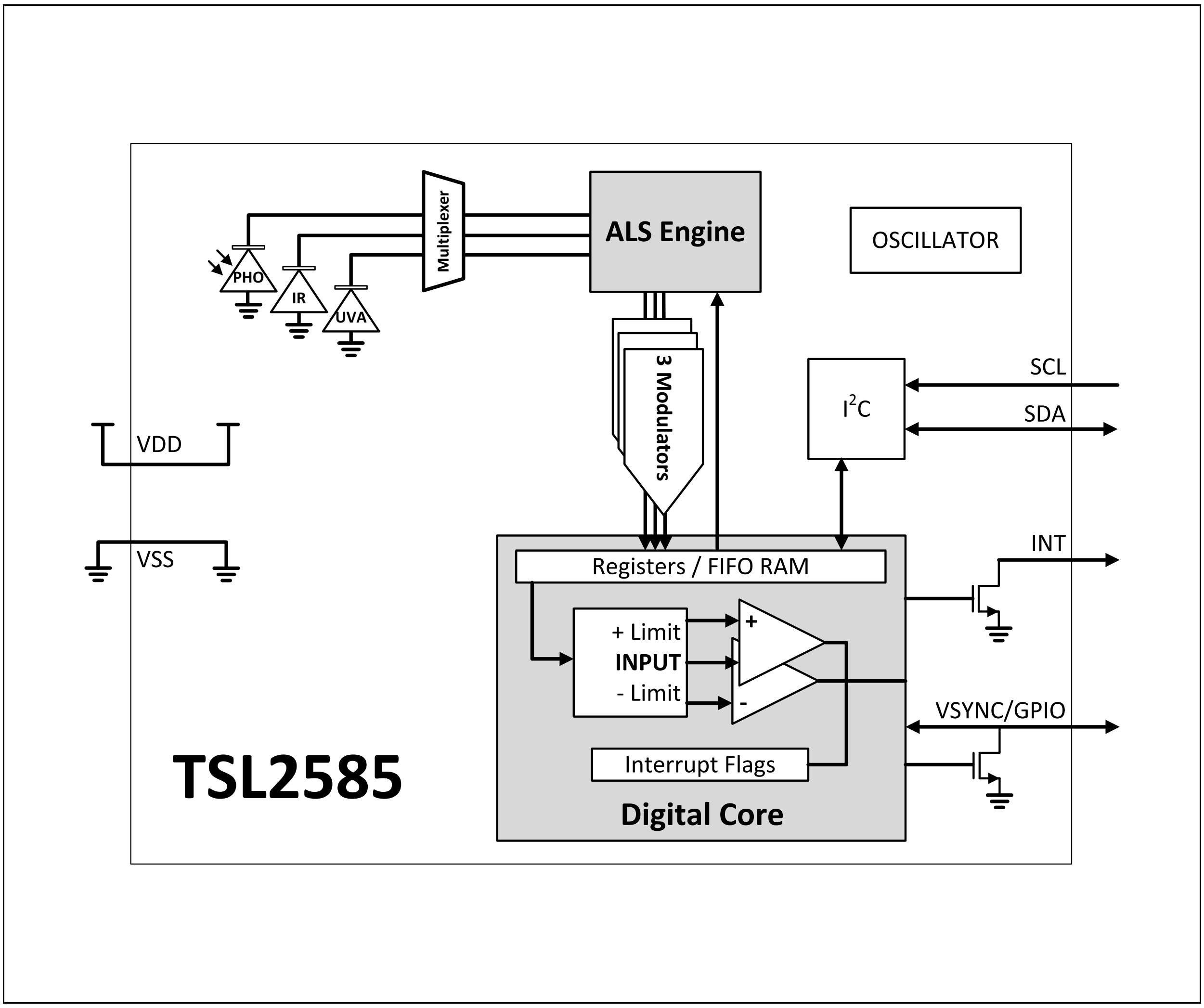
TSL2585 integrates multiple applications within one device. The applications include:

- Ambient light sensing for display brightness management
- Ambient UV index estimation
- Auto exposure and flicker detection for camera assistance

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TSL2585



Pin Assignment and Photodiodes

Figure 3:
Pin Diagram and Photodiode Location of TSL2585 (top view)

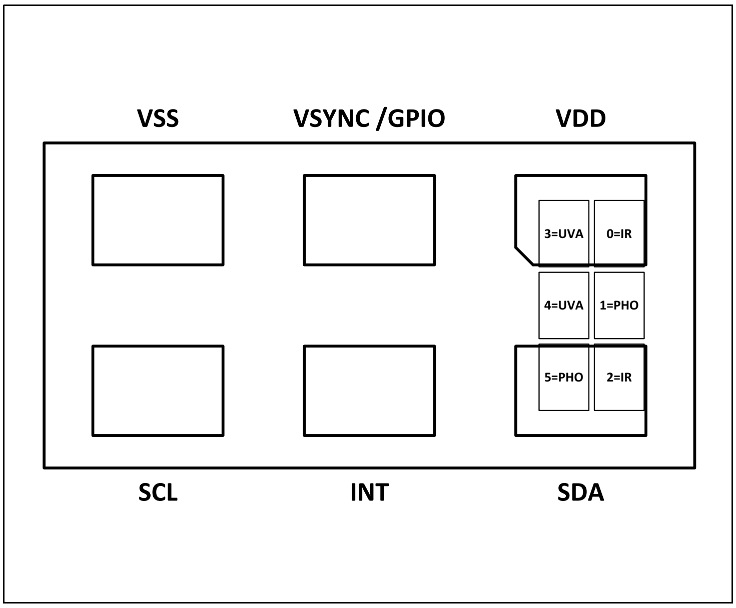


Figure 4:
Pin Description of TSL2585

Pin Number	Pin Name	Description
1	VDD	Supply voltage (1.8V).
2	VSYNC/GPIO	Synchronization input or General Purpose open-drain Input/Output.
3	VSS	Ground. All voltages are referenced to VSS.
4	SCL	I^2C serial clock terminal.
5	INT	Interrupt. Open-drain output.
6	SDA	I^2C serial data I/O terminal.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages with respect to VSS. Device parameters are guaranteed at V_{DD} = 1.8V and T_A = 25°C unless otherwise noted.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD}	Supply voltage	-0.3	1.98	V	
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V	
I_{IO}	Output terminal current	-1	20	mA	
Electrostatic Discharge					
ESD_{HBM}	HBM electrostatic discharge	± 2000		V	ANSI/ESDA/JEDEC JS-001-2017
ESD_{CDM}	CDM electrostatic discharge	± 500		V	ANSI/ESDA/JEDEC JS-002-2018
I_{SCR}	Input current (latch-up immunity)	± 100		mA	JEDEC JESD78E Class II
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage temperature range	-40	85	°C	
T_A	Operating temperature range	-30	85	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”
RH_{NC}	Relative humidity (non-condensing)		85	%	
MSL	Moisture sensitivity level	3			Represents a max. floor life time of 168h

Optical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Device parameters are guaranteed with V_{DD} = 1.8V and T_A = 25°C unless otherwise noted.

Figure 6:
ALS Characteristics of TSL2585, ALS Gain = 128x, Integration Time = 10ms (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Dark ADC count value [(1)]	E_e = 0μW/cm^2 ALS gain: 512x Integration time: 98ms	0	1	3	counts
ALS gain ratios [(2)]	0.5x	1/270.78	1/249.13	1/230.68	
	1x	1/133.17	1/123.85	1/115.74	
	2x	1/66.99	1/62.97	1/59.41	
	4x	1/33.39	1/31.72	1/30.21	
	8x	1/16.17	1/15.53	1/14.93	
	16x	1/8.30	1/7.97	1/7.66	
	32x	1/4.15	1/3.99	1/3.83	
	64x	1/2.09	1/2.01	1/1.93	
	256x	1.78	1.93	2.07	
	512x	3.42	3.80	4.18	
	1024x	6.16	7.42	8.68	
	2048x	10.26	14.06	17.86	
	4096x	11.41	25.35	39.29	
ADC noise [(3)]	White LED, 2700K [(4)] Integration time: 100ms		0.05		%
Photopic channel irradiance responsivity	White LED, 2700K [(4)]	62.7	73.7	84.8	counts/ (μW/cm^2)

Parameter	Conditions	Min	Typ	Max	Unit
IR channel irradiance responsivity	IR LED =940nm (5)		74.8		counts/ (µW/cm^2)
UV channel irradiance responsivity	UV LED =365nm (6) ALS gain: 1024x		82.8		
IR / Photopic channel ratio	White LED, 2700K		2.9		%
UV / Photopic channel ratio	White LED, 2700K		0.0		
Photopic / IR channel ratio	IR LED = 940nm		1.3		
UV / IR channel ratio	IR LED = 940nm		0.2		

Note(s):

1. The typical 3-sigma distribution shows less than 1 count. For this measurement, each modulator is always connected to one photodiode whereas the photodiodes are sequentially multiplexed.
2. The gain ratios are calculated relative to the response with ALS gain = 128x.
3. ADC noise is calculated as the standard deviation relative to full scale. It is lab characterization from limited samples.
4. The White LED is an InGaN light-emitting diode with integrated phosphor and the following characteristic: correlated color temperature = 2700K.
5. The IR LED is an AlGaAs light-emitting diode with a peak wavelength of λ_P = 940nm.
6. The UV LED is an light-emitting diode with a peak wavelength of λ_P = 365nm.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 7:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Comments
Electrical Parameters						
V_{DD}	Supply voltage	1.7	1.8	1.98	V	
$V_{DD/IO}$	I/O supply voltage	1.62	1.8	3.3	V	
Temperature Ranges and Storage Conditions						
T_A	Operating free-air temperature (1)	-30	25	85	°C	

Note(s):

1. While the device is operational across the temperature range, functionality will vary with temperature.

Figure 8:
Electrical Characteristics of TSL2585, V_{DD} = 1.8V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD;ALS}$	ALS supply current	Active ALS state (1) (PON=AEN=1)		235	290	µA
$I_{DD;IDLE}$	Idle current	Idle state (2) (PON=1, AEN=0; FDEN=0)		60		
$I_{DD;SLEEP}$	Sleep current	Sleep state (3)		0.7	5	
I_{LEAK}	Leakage current	Measured on SDA, SCL, INT, GPIO	-5		5	
V_{OL}	INT, SDA, GPIO output low voltage	6mA sink current			0.4	V
V_{IH}	SCL, SDA, VSYNC input high voltage		1.26			
V_{IL}	SCL, SDA, VSYNC input low voltage				0.54	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input pin capacitance			10		pF
t_{ACTIVE}	Time from Power-On to Ready to Receive I^2C Commands			0.5		ms

Note(s):

1. This parameter indicates the supply current during periods of ALS integration. The ALS gain setting will have an effect on the active supply current. The ALS gain setting used for this parameter is 128x and there are 3 modulators active.
2. Idle state occurs when PON=1 and all functions are disabled. This parameter is measured with LOWPOWER_IDLE=1.
3. Sleep state occurs when PON = 0 and I^2C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Timing Characteristics

The timing parameters are specified by design and characterization and are not production tested unless otherwise noted. All parameters are measured with V_{DD} = 1.8V and T_A = 25°C unless otherwise noted.

Figure 9:
I²C Timing Characteristics of TSL2585

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I²C clock frequency	0		400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3			µs
$t_{HD;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated	0.6			µs
$t_{SU;STA}$	Repeated start condition setup time	0.6			µs
$t_{SU;STO}$	Stop condition setup time	0.6			µs
t_{LOW}	SCL clock low period	1.3			µs
t_{HIGH}	SCL clock high period	0.6			µs
$t_{HD;DAT}$	Data hold time	0			ns
$t_{SU;DAT}$	Data setup time	100			ns
t_F	Clock/data fall time			300	ns
t_R	Clock/data rise time			300	ns

Figure 10:
Timing Diagram for TSL2585

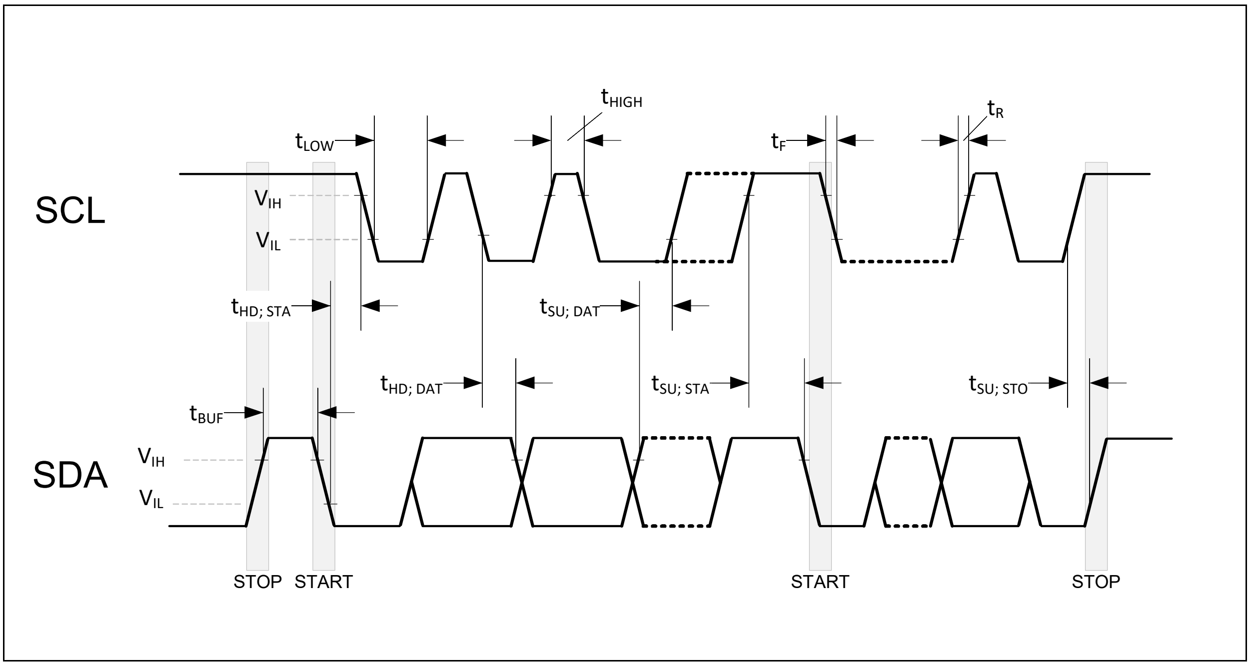


Figure 11:
Functional Timing Characteristics of TSL2585

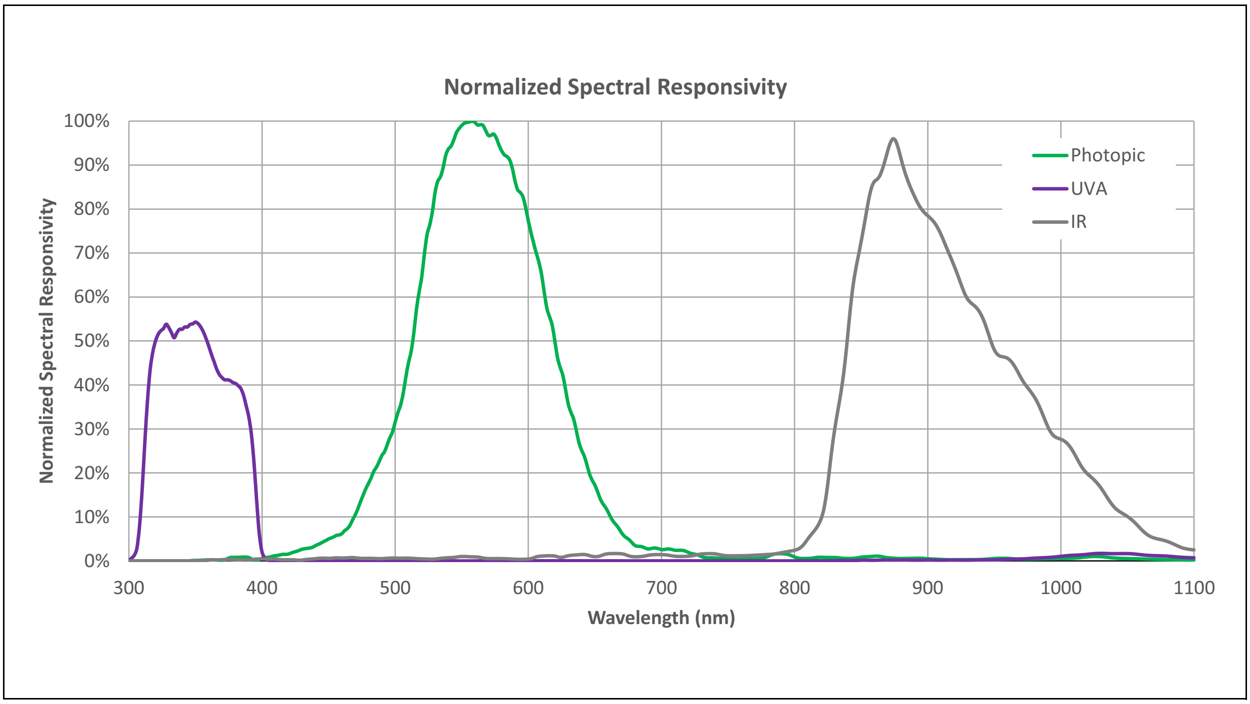
Symbol	Parameter	Min	Typ	Max	Unit
f_{OSC}	Oscillator clock frequency (1)	700	720	740	kHz

Note(s):

1. 100% production tested.

Typical Operating Characteristics

Figure 12:
Spectral Responsivity



Note(s):

1. The spectral responsivities shown in the figure are measured with 128x AGAIN and 100ms integration time for the Photopic and IR channels and 1024x AGAIN and 100ms integration time for the UV channel. The spectral responsivities are normalized to the Photopic channel.
2. The measurements are performed with collimated light and using a rubber boot to block the light leakage through the side walls of the clear mold package.

Figure 13:
Normalized Angular Response X-Axis

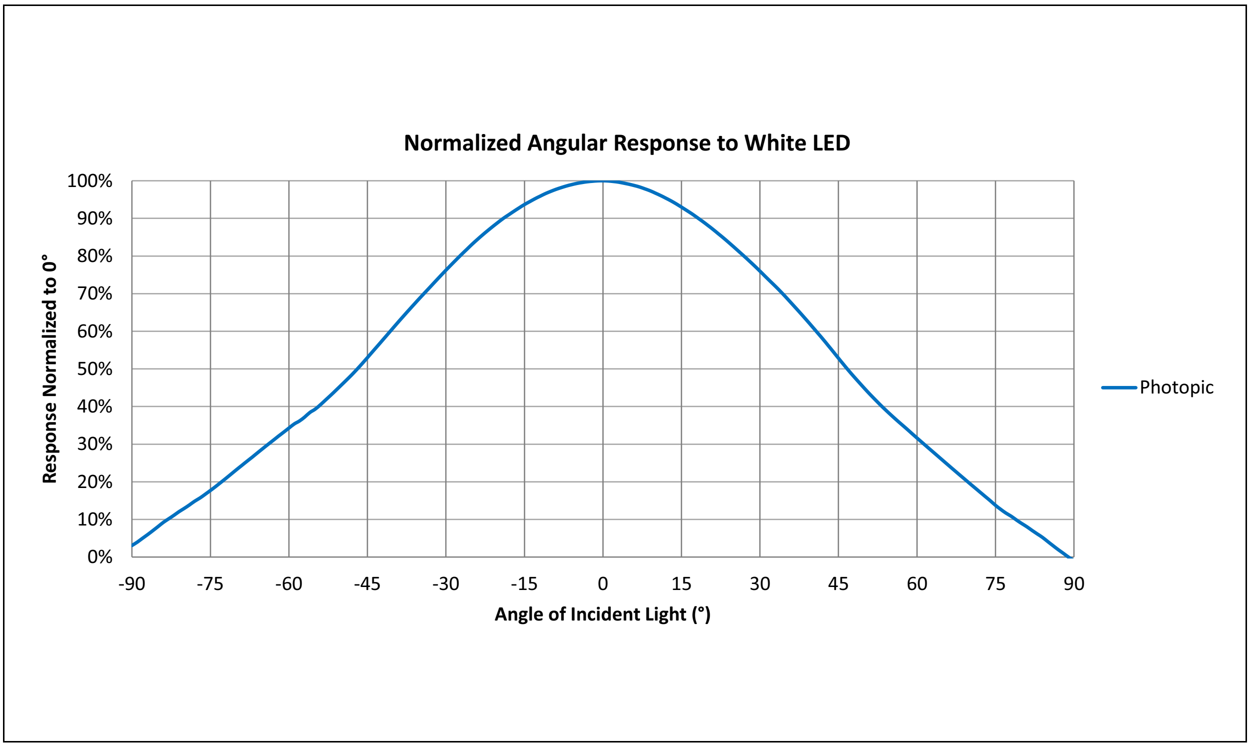
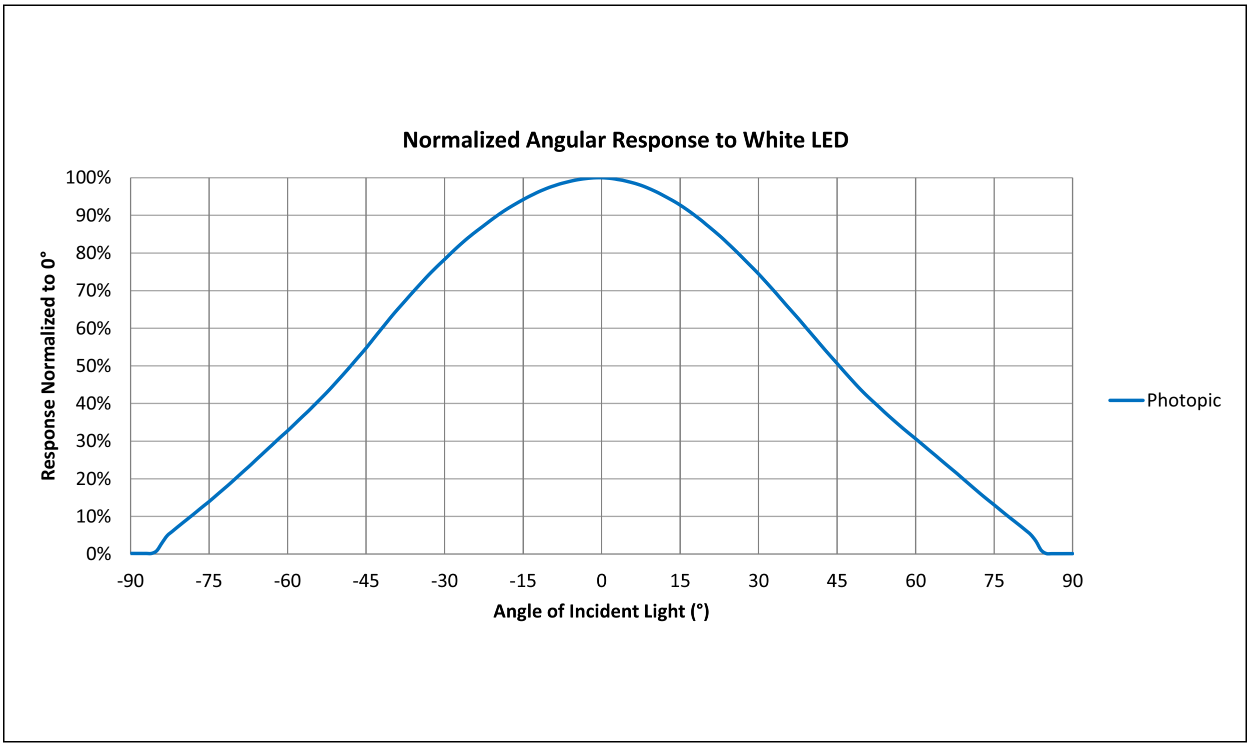


Figure 14:
Normalized Angular Response Y-Axis



Note(s):

1. The X and Y angular scans have been performed in the lab using an aperture which blocks light leakage through side walls of clear mold package

Detailed Description

Upon power-up, POR, the device initializes. During initialization (typically 500µs), the device will deterministically send NAK on I^2C and cannot accept I^2C transactions. All communication with the device must be delayed, and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I^2C transaction occurs during this state, the I^2C core wakes up temporarily to service the communication. Once the Power ON bit, PON, is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever a function is enabled (AEN = 1)the device exits the IDLE state. If all functions are disabled (AEN = 0), the device returns to the IDLE state.

As depicted in Figure 15 and Figure 16, the ambient light sensing and flicker sampling functions operate in parallel when enabled. Each function is individually configured (e.g. gain, ADC integration time, wait time, persistence, thresholds, etc.).

If Sleep after Interrupt is enabled (SAI = 1 in register 0xA1), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI_ACTIVE bit is cleared (the status bit is in register 0x9F and the clear status bit is in register 0xB1).

State Machine Diagrams

Figure 15:
Simplified State Diagram

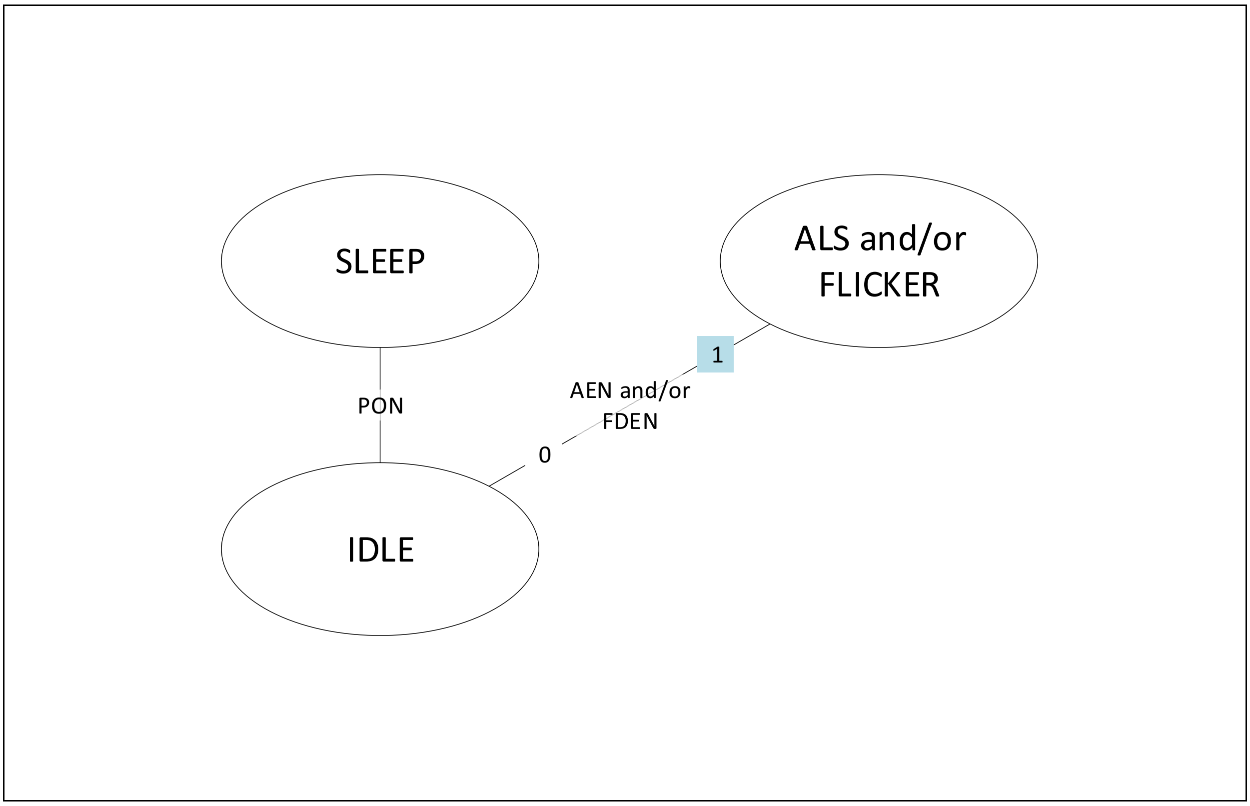
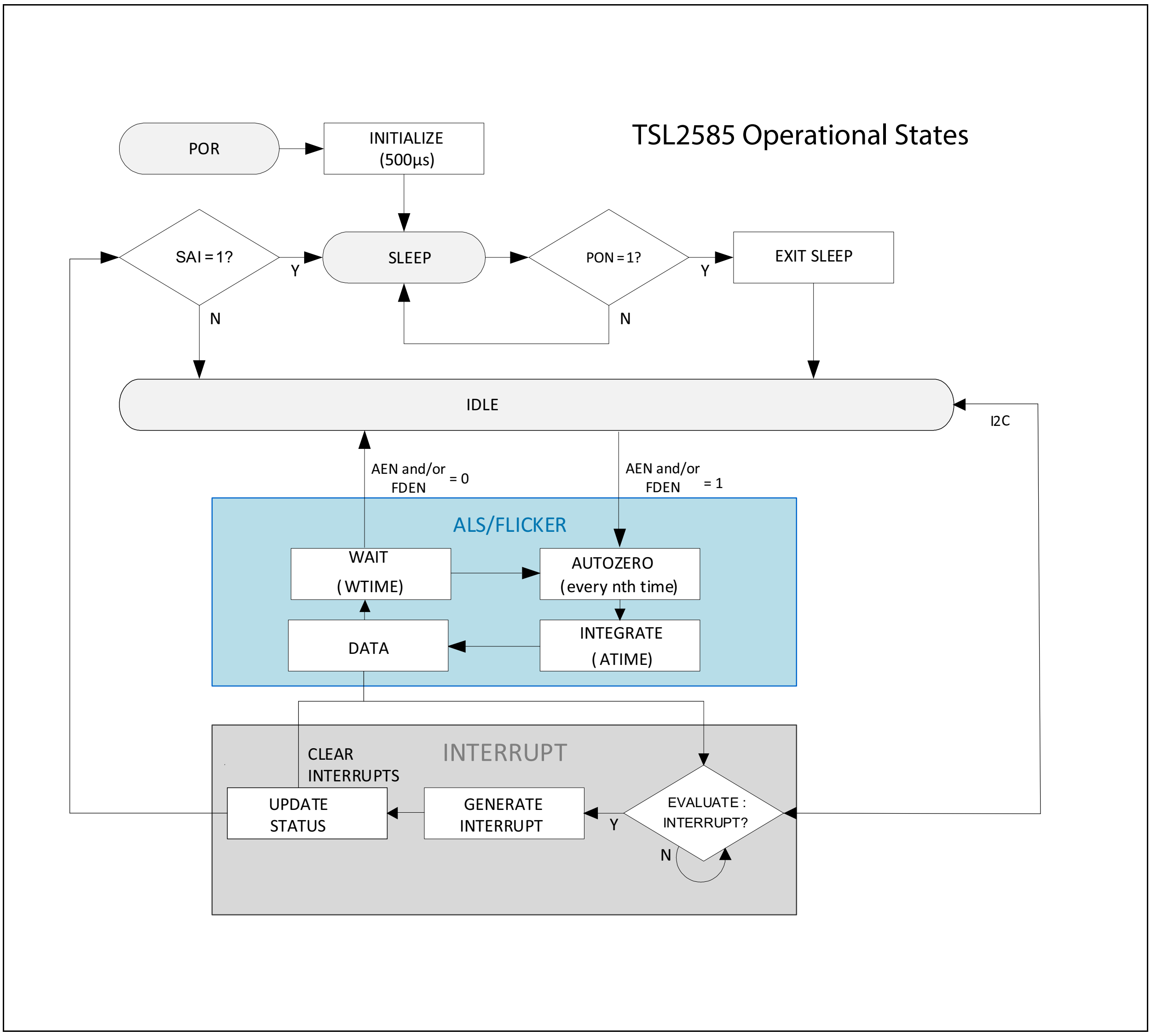


Figure 16:
Detailed State Diagram



I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (I.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

All 16-bit fields have a latching scheme for reading and writing. In general it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP. Following each byte (9^{th} clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9^{th} clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Register Overview

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide device control functions and are read to determine device status and acquire device data.

Register Map

The register set is summarized in Figure 17. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. The power-on reset values of each bit are indicated in these columns. Two-byte fields are always latched with the low byte followed by the high byte.

Figure 17:
Register Map

Addr	Name	Description	Reset
0x08	UV_CALIB	UV calibration factor	OTP
0x40	MOD_CHANNEL_CTRL	Modulator channel control	0x00
0x80	ENABLE	Enables device states	0x00
0x81	MEAS_MODE0	Measurement mode settings 0	0x04
0x82	MEAS_MODE1	Measurement mode settings 1	0x0C
0x83	SAMPLE_TIME0	Flicker sample time settings 0 [7:0]	0xB3
0x84	SAMPLE_TIME1	Flicker sample time settings 1 [10:8]	0x00
0x85	ALS_NR_SAMPLES0	ALS measurement time settings 0 [7:0]	0x00
0x86	ALS_NR_SAMPLES1	ALS measurement time settings 1 [10:8]	0x00
0x87	FD_NR_SAMPLES0	Flicker number of samples 0 [7:0]	0x00
0x88	FD_NR_SAMPLES1	Flicker number of samples 1 [10:8]	0x00
0x89	WTIME	Wait time	0x00
0x8A	AILT0	ALS Interrupt Low Threshold [7:0]	0x00
0x8B	AILT1	ALS Interrupt Low Threshold [15:8]	0x00
0x8C	AILT2	ALS Interrupt Low Threshold [23:16]	0x00
0x8D	AIHT0	ALS Interrupt High Threshold [7:0]	0x00
0x8E	AIHT1	ALS Interrupt High Threshold [15:8]	0x00
0x8F	AIHT2	ALS interrupt High Threshold [23:16]	0x00
0x90	AUX_ID	Auxiliary Identification	0x06
0x91	REV_ID	Revision Identification	0x11
0x92	ID	Device Identification	0x5C

Addr	Name	Description	Reset
0x93	STATUS	Device Status information 1	0x00
0x94	ALS_STATUS	ALS Status information 1	0x00
0x95	ALS_DATA0[7:0]	ALS data channel 0 low byte [7:0]	0x00
0x96	ALS_DATA0[15:8]	ALS data channel 0 high byte [15:8]	0x00
0x97	ALS_DATA1[7:0]	ALS data channel 1 low byte [7:0]	0x00
0x98	ALS_DATA1[15:8]	ALS data channel 1 high byte [15:8]	0x00
0x99	ALS_DATA2[7:0]	ALS data channel 2 low byte [7:0]	0x00
0x9A	ALS_DATA2[15:8]	ALS data channel 2 high byte [15:8]	0x00
0x9B	ALS_STATUS2	ALS Status information 2	0x00
0x9C	ALS_STATUS3	ALS Status information 3	0x00
0x9D	STATUS2	Device Status information 2	0x00
0x9E	STATUS3	Device Status information 3	0x08
0x9F	STATUS4	Device Status information 4	0x00
0xA0	STATUS5	Device Status information 5	0x00
0xA1	CFG0	Configuration 0	0x08
0xA2	CFG1	Configuration 1	0x00
0xA3	CFG2	Configuration 2	0x01
0xA4	CFG3	Configuration 3	0x00
0xA5	CFG4	Configuration 4	0x00
0xA6	CFG5	Configuration 5	0x00
0xA7	CFG6	Configuration 6	0x03
0xA8	CFG7	Configuration 7	0x01
0xA9	CFG8	Configuration 8	0xC4
0xAA	CFG9	Configuration 9	0x00
0xAC	AGC_NR_SAMPLES[7:0]	Number of samples for measurement with AGC low [7:0]	0x00
0xAD	AGC_NR_SAMPLES[10:8]	Number of samples for measurement with AGC high [10:8]	0x00
0xAE	TRIGGER_MODE	Wait Time Mode	0x00
0xB1	CONTROL	Device control settings	0x00
0xBA	INTENAB	Enable interrupts	0x00

Addr	Name	Description	Reset
0xBB	SIEN	Enable saturation interrupts	0x00
0xCE	MOD_COMP_CFG1	Adjust AutoZero range	0x80
0xCF	MEAS_SEQR_FD_0	Flicker measurement with sequencer on modulator0	0x01
0xD0	MEAS_SEQR_ALS_FD_1	ALS measurement with sequencer on all modulators	0x01
0xD1	MEAS_SEQR_APERS_AND_VSYNC_ WAIT	Defines the measurement sequencer pattern	0x01
0xD2	MEAS_SEQR_RESIDUAL_0	Residual measurement configuration with sequencer on modulator0 and modulator1	0xFF
0xD3	MEAS_SEQR_RESIDUAL_1_AND_WAIT	Residual measurement configuration with sequencer on modulator2 and wait time configuration for all sequencers	0x1F
0xD4	MEAS_SEQR_STEP0_MOD_GAINX_L	Gain of modulator0 and modulator1 for sequencer step 0	0x88
0xD5	MEAS_SEQR_STEP0_MOD_GAINX_H	Gain of modulator2 for sequencer step 0	0x08
0xD6	MEAS_SEQR_STEP1_MOD_GAINX_L	Gain of modulator0 and modulator1 for sequencer step 1	0x88
0xD7	MEAS_SEQR_STEP1_MOD_GAINX_H	Gain of modulator2 for sequencer step 1	0x08
0xD8	MEAS_SEQR_STEP2_MOD_GAINX_L	Gain of modulator0 and modulator1 for sequencer step 2	0x88
0xD9	MEAS_SEQR_STEP2_MOD_GAINX_H	Gain of modulator2 for sequencer step 2	0x08
0xDA	MEAS_SEQR_STEP3_MOD_GAINX_L	Gain of modulator0 and modulator1 for sequencer step 3	0x88
0xDB	MEAS_SEQR_STEP3_MOD_GAINX_H	Gain of modulator2 for sequencer step 3	0x08
0xDC	MEAS_SEQR_STEP0_MOD_PHDX_ SMUX_L	Photodiode 0-3 to modulator mapping through multiplexer for sequencer step 0	0x66
0xDD	MEAS_SEQR_STEP0_MOD_PHDX_ SMUX_H	Photodiode 4-5 to modulator mapping through multiplexer for sequencer step 0	0x06
0xDE	MEAS_SEQR_STEP1_MOD_PHDX_ SMUX_L	Photodiode 0-3 to modulator mapping through multiplexer for sequencer step 1	0x84
0xDF	MEAS_SEQR_STEP1_MOD_PHDX_ SMUX_H	Photodiode 4-5 to modulator mapping through multiplexer for sequencer step 1	0xF3
0xE0	MEAS_SEQR_STEP2_MOD_PHDX_ SMUX_L	Photodiode 0-3 to modulator mapping through multiplexer for sequencer step 2	0x07
0xE1	MEAS_SEQR_STEP2_MOD_PHDX_ SMUX_H	Photodiode 4-5 to modulator mapping through multiplexer for sequencer step 2	0xF8

Addr	Name	Description	Reset
0xE2	MEAS_SEQR_STEP3_MOD_PHDX_ SMUX_L	Photodiode 0-3 to modulator mapping through multiplexer for sequencer step 3	0x24
0xE3	MEAS_SEQR_STEP3_MOD_PHDX_ SMUX_H	Photodiode 4-5 to modulator mapping through multiplexer for sequencer step 3	0x03
0xE4	MOD_CALIB_CFG0	Modulator calibration config0	0xFF
0xE6	MOD_CALIB_CFG2	Modulator calibration config2	0xD3
0xF2	VSYNC_PERIOD[7:0]	Measured VSYNC period	0x00
0xF3	VSYNC_PERIOD[15:8]	Read and clear measured VSYNC period	0x00
0xF4	VSYNC_PERIOD_TARGET[7:0]	Targeted VSYNC period	0x00
0xF5	VSYNC_PERIOD_TARGET[14:8]	Alternative target VSYNC period	0x00
0xF6	VSYNC_CONTROL	Control of VSYNC period	0x00
0xF7	VSYNC_CFG	Configuration of VSYNC input	0x00
0xF8	VSYNC_GPIO_INT	Configuration of GPIO pin	0x02
0xF9	MOD_FIFO_DATA_CFG0	Configuration of FIFO access for modulator 0	0x8F
0xFA	MOD_FIFO_DATA_CFG1	Configuration of FIFO access for modulator 1	0x8F
0xFB	MOD_FIFO_DATA_CFG2	Configuration of FIFO access for modulator 2	0x8F
0xFC	FIFO_THR	Configuration of FIFO threshold interrupt	0x7F
0xFD	FIFO_STATUS0	FIFO status information 0	0x00
0xFE	FIFO_STATUS1	FIFO status information 1	0x00
0xFF	FIFO_DATA	FIFO readout	0x00

Register Descriptions

UV_CALIB Register

Figure 18:
UV_CALIB

<table>
<tr><th colspan="2">Addr: 0x08</th><th colspan="3">UV_CALIB</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="12">7:0</td><td rowspan="12">UV_CALIB</td><td rowspan="12">OTP</td><td rowspan="12">R</td><td colspan="2">The UV response of each device is calibrated, and the calibration result is saved in the UV_CALIB OTP register. The UV_CALIB value is in percentage with a resolution of 1%. The UV_CALIB value of 127 means the UV response of the device is close to the target and the calibration factor is 0%.
$$UV_{Calibrated\_Data} = UV_{Raw\_Data}/(1 - \frac{"UV\_CALIB" - 127}{100})$$
Where, the UV_{Raw_Data} is the raw value read from the ALS_DATA registers or FIFO.</td></tr>
<tr><td>UV_CALIB</td><td>UV Calibration Factor</td></tr>
<tr><td>0</td><td></td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>124</td><td>-3%</td></tr>
<tr><td>125</td><td>-2%</td></tr>
<tr><td>126</td><td>-1%</td></tr>
<tr><td>127</td><td>0%</td></tr>
<tr><td>128</td><td>1%</td></tr>
<tr><td>129</td><td>2%</td></tr>
<tr><td>130</td><td>3%</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td></td><td></td><td></td><td></td><td>255</td><td></td></tr>
</table>

Note(s):

1. Return to the Register Map (0x08).

MOD_CHANNEL_CTRL Register

Figure 19:
MOD_CHANNEL_CTRL

Addr: 0x40		MOD_CHANNEL_CTRL		
Bit	Field	Reset	Type	Bit Description
7:3	Reserved	0		
2	MOD2_DISABLE	0	R/W	When asserted modulator 2 is disabled
1	MOD1_DISABLE	0	R/W	When asserted modulator 1 is disabled
0	MOD0_DISABLE	0	R/W	When asserted modulator 0 is disabled

Note(s):

1. Return to the Register Map (0x40).

ENABLE Register

Figure 20:
ENABLE

Addr: 0x80		ENABLE		
Bit	Field	Reset	Type	Bit Description
7	Reserved	0		
6	FDEN	0	R/W	**Flicker Detection Enable**. Writing a 1 activates flicker detection. Writing a 0 disables flicker detection.
5:2	Reserved	0		
1	AEN	0	R/W	**ALS Enable**. Writing a 1 enables ALS. Writing a 0 disables ALS.
0	PON	0	R/W	**Power ON**. When asserted, the internal oscillator is activated, allowing timers and modulator channels to operate. Writing a 0 disables the oscillator and clears FDEN, and AEN. Only set this bit after all other registers have been initialized by the host.

Note(s):

1. Return to the Register Map (0x80).

MEAS_MODE0 Register

Figure 21:
MEAS_MODE0

Addr: 0x81		MEAS_MODE0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	STOP_AFTER_NTH_ ITERATION	0	R/W	Stops a measurement after n^{th} iterations by setting FDEN and AEN to 0. PON will stay at 1. Per default it stops after one measurement, which can be used for manual calibration.
6	ENABLE_AGC_ASAT_ DOUBLE_STEP_DOWN	0	R/W	Enables two gain steps down at once in case of an analogue AGC saturation and at a gain step still >0. This will allow a faster reach of 25% full-scale range and a more prompt reaction if analogue saturations occurs.
5	MEASUREMENT_ SEQUENCER_SINGLE_ SHOT_MODE	0	R/W	Start one measurement cycle with sequencer settings and stop it by asserting Sleep After Interrupt (SAI)
4	MOD_FIFO_ALS_STATUS_ WRITE_ENABLE	0	R/W	Enables writing of ALS status to the FIFO RAM in case ALS data scaling is used as well as 16-bit ALS data writing. It is needed to be able to correctly interpret the ALS data.
3:0	ALS_SCALE	0x4	R/W	ALS_SCALE is used to avoid that redundant ALS MSBs are transmitted and are reducing possible resolution, since the ALS data register is only 16 bits wide (internally the result can be 26 bits wide = 11-bit samples + 11-bit sampling time + 4-bit residuals - ALS_MSB_POSITION). The ALS_SCALE register defines the number of MSBs which must be 0 so that the scaled representation is used in the ALS data registers instead of the unscaled representation.

Note(s):

1. Return to the Register Map (0x81).

MEAS_MODE1 Register

Figure 22:
MEAS_MODE1

Addr: 0x82		MEAS_MODE1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MOD_FIFO_FD_END_MARKER_WRITE_ENABLE	0	R/W	Enables writing of end marker to FIFO after each complete flicker measurement.
6	MOD_FIFO_FD_CHECKSUM_WRITE_ENABLE	0	R/W	Enables writing of flicker checksum to FIFO after each complete flicker measurement.
5	MOD_FIFO_FD_GAIN_WRITE_ENABLE	0	R/W	Enables writing of gain to FIFO after each complete flicker measurement. This is required in case AGC is enabled.
4:0	ALS_MSB_POSITION	0x0C	R/W	Internally the result can be 26 bits wide = 11-bit samples + 11-bit sampling time + 4-bit residuals and is stored in a 32-bit register. ALS_MSB_POSITION defines the MSB in this 32-bit register

Note(s):

1. Return to the Register Map (0x82).

SAMPLE_TIME0 Register

Figure 23:
SAMPLE_TIME0

Addr: 0x83		SAMPLE_TIME0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	SAMPLE_TIME[7:0]	0xB3	R/W	Flicker sampling time and ALS measurement time step. Sets the time in steps of 1.388889µs modulator clock. The modulator clock can be divided with MOD_DIVIDER_SELECT in register CFG7. Please observe that SAMPLE_TIME needs to be set in register 0x83 and 0x84 (11-bit wide). It counts from 0-2047 (2048 counts). SAMPLE_TIME+1 = 1/FlickerSamplingTime/1.388889µs Default: 179+1 = 1/4000Hz / 1.388889µs (180 counts as counted 0-179) ALSIntegrationTimeStep = (SAMPLE_TIME+1) x 1.388889µs Default: 250µs = (179+1) x 1.388889µs

Note(s):

1. Return to the Register Map (0x83).

SAMPLE_TIME1 Register

Figure 24:
SAMPLE_TIME1

Addr: 0x84		SAMPLE_TIME1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2:0	SAMPLE_TIME[10:8]	0	R/W	Please see SAMPLE_TIME0.

Note(s):

1. Return to the Register Map (0x84).

ALS_NR_SAMPLES0 Register

Figure 25:
ALS_NR_SAMPLES0

Addr: 0x85		ALS_NR_SAMPLES0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	ALS_NR_ SAMPLES[7:0]	0	R/W	ALS_NR_OF_SAMPLES defines the total measurement time for ALS ATIME= (ALS_NR_ SAMPLES+1) x (SAMPLE_TIME+1) x 1.388889µs

Note(s):

1. Return to the Register Map (0x85).

ALS_NR_SAMPLES1 Register

Figure 26:
ALS_NR_SAMPLES1

Addr: 0x86		ALS_NR_SAMPLES1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2:0	ALS_NR_SAMPLES[10:8]	0	R/W	Please see ALS_NR_SAMPLES0.

Note(s):

1. Return to the Register Map (0x86).

FD_NR_SAMPLES0 Register

Figure 27:
FD_NR_SAMPLES0

Addr: 0x87		FD_NR_SAMPLES0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FD_NR_SAMPLES[7:0]	0	R/W	FD_NR_OF_SAMPLES defines the number of samples+1 measured in one sequencer step. The sample time is defined in SAMPLE_TIME[10:0]

Note(s):

1. Return to the Register Map (0x87).

FD_NR_SAMPLES1 Register

Figure 28:
FD_NR_SAMPLES1

Addr: 0x88		FD_NR_SAMPLES1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	FD_NR_SAMPLES_ INFINITE	0	R/W	When asserted flicker measurement sequences will be infinitely repeated. In this mode, no end markers are inserted but results are continuously written into the FIFO.
6:3	Reserved	0		
2:0	FD_NR_SAMPLES[10:8]	0	R/W	Please see FD_NR_SAMPLES0.

Note(s):

1. Return to the Register Map (0x88).

WTIME Register

Figure 29:
WTIME

Addr: 0x89				WTIME
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	WTIME	0	R/W	Sets the WaitTime between 2 measurements of the modulator or sequencer. WTIME together with MOD_TRIGGER_TIMING (in register 0xAE TRIGGER_MODE) define the actual time between measurements. WaitTime = MOD_TRIGGER_TIMING x WTIME Default: 0 = 0 x (0+1) no WaitTime.

Note(s):

1. Return to the Register Map (0x89).

ALS Interrupt Low Threshold Registers

Figure 30:
ALS Interrupt Low Threshold

Addr	Bit	Field	Reset	Type	Description
0x8A	7:0	AILT0	0	R/W	**ALS Interrupt Low Threshold** The ALS interrupt threshold registers are 24-bit wide. ALS interrupt level detection compares the threshold registers with the data accumulated by the selected modulator. The modulator can be selected via ALS_THRESHOLD_ CHANNEL. If AIEN is asserted and the accumulated data is below AILT for the number of consecutive samples specified in APERS, an interrupt is asserted on the interrupt pin (internally AINT_AILT and AINT are asserted).
0x8B	7:0	AILT1	0	R/W	
0x8C	7:0	AILT2	0	R/W	

Note(s):

1. Return to the Register Map (0x8A, 0x8B, 0x8C).

ALS Interrupt High Threshold Registers

Figure 31:
ALS Interrupt High Threshold

Addr	Bit	Field	Reset	Type	Description
0x8D	7:0	AIHT0	0	R/W	**ALS Interrupt High Threshold** The ALS interrupt threshold registers are 24-bit wide. ALS interrupt level detection compares the threshold registers with the data accumulated by the selected modulator. The modulator can be selected via ALS_THRESHOLD_ CHANNEL. If AIEN is asserted and the accumulated data is above AIHT for the number of consecutive samples specified in APERS, an interrupt is asserted on the interrupt pin (internally AINT_AIHT and AINT are asserted).
0x8E	7:0	AIHT1	0	R/W	
0x8F	7:0	AIHT2	0	R/W	

Note(s):

1. Return to the Register Map (0x8D, 0x8E, 0x8F).

Device Identification Registers

Figure 32:
Device Identification

Addr	Bit	Field	Reset	Type	Description
0x90	3:0	AUX_ID	0110b	R	**Device Identification** **AUX_ID:** Identifies package and wafer factory. **REV_ID:** Identifies function ID and revision number of CMOS die. **ID:** Device identification
0x91	7:0	REV_ID	0x11 00010001b	R	
0x92	7:0	ID	0x5C 01011100b	R	

Note(s):

1. Return to the Register Map (0x90, 0x91, 0x92).

STATUS Register

Figure 33:
STATUS

Addr: 0x93		STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MINT	0	R/W	**Modulator Interrupt**. Indicates that a modulator interrupt has occurred because of saturation. Check the STATUS2 register to differentiate between analog or digital saturation. Writing 1 to this bit clear MINT and all subsequent interrupts.
6:4	Reserved	0		
3	AINT	0	R/W	**ALS Interrupt**. If AIEN is set, this interrupt indicates that an ALS event that met the programmed ALS thresholds (AILT or AIHT) and persistence (APERS) occurred. Check the STATUS3 register to differentiate. Writing 1 to this bit clear AINT and all subsequent interrupts.
2	FINT	0	R/W	**FIFO Interrupt**. Indicates that the data level in the FIFO met the programmed FIFO thresholds (FIFO_LVL and FIFO_THR). This interrupt is automatically asserted/removed depending on the programmed FIFO thresholds. Writing 1 to this bit clears FINT. The interrupt, however, will be promptly asserted again in case the FIFO has not been read out or cleared.

Addr: 0x93		STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
1	Reserved	0		
0	SINT	0		**System Interrupt**. If SIEN is set, indicates that one or more of several events has occurred or is complete. The events related to this interrupt are indicated in the STATUS5 register.

Note(s):

1. Return to the Register Map (0x93)

ALS_STATUS Register

Figure 34:
ALS_STATUS

Addr: 0x94		ALS_STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	MEAS_SEQR_STEP	0	R	Contains the sequencer step where ALS data was measured.
5	ALS_DATA0_ANALOG_SATURATION_STATUS	0	R	Indicates analog saturation of ALS data0 in data registers ALS_ADATA0.
4	ALS_DATA1_ANALOG_SATURATION_STATUS	0	R	Indicates analog saturation of ALS data1 in data registers ALS_ADATA1.
3	ALS_DATA2_ANALOG_SATURATION_STATUS	0	R	Indicates analog saturation of ALS data2 in data registers ALS_ADATA2.
2	ALS_DATA0_SCALED_STATUS	0	R	Indicates if ALS data0 needs to be multiplied if bit is set to, 0: 2^(ALS_SCALED) 1: 1
1	ALS_DATA1_SCALED_STATUS	0	R	Indicates if ALS data1 needs to be multiplied if bit is set to, 0: 2^(ALS_SCALED) 1: 1
0	ALS_DATA2_SCALED_STATUS	0	R	Indicates if ALS data2 needs to be multiplied if bit is set to, 0: 2^(ALS_SCALED) 1: 1

Note(s):

1. Return to the Register Map (0x94).

ALS Data Registers

Figure 35:
ALS Data Registers

Addr	Bit	Field	Reset	Type	Description
0x95	7:0	ALS_DATA0[7:0]	0	R	**ALS Data Registers.** In order to update ALS Data Registers ALS_STATUS must be read first. The ALS channel data is stored in two 8-bit registers and shall be interpreted as 16-bit data across 2 registers. All ALS data samples stored are generated in the same integration cycle. Reading these bytes consecutively (low byte before high byte) ensures that the data is concurrent. The data, stored in the ALS_DATA registers, is obtained from a 26-bit wide result buffer depending on settings of ALS_SCALE in MEAS_MODE0 and ALS_MSB_POSITION in MEAS_MODE1. The ALS_STATUS register indicates whether the ALS data is scaled or unscaled. In case ALS_MSB_POSITION is exceeded, data is 0xFFFE. In case of analog saturation, data is 0xFFFF.
0x96	7:0	ALS_DATA0[15:8]	0	R	
0x97	7:0	ALS_DATA1[7:0]	0	R	
0x98	7:0	ALS_DATA1[15:8]	0	R	
0x99	7:0	ALS_DATA2[7:0]	0	R	
0x9A	7:0	ALS_DATA2[15:8]	0	R	

Note(s):

1. Return to the Register Map (0x95, 0x96, 0x97, 0x98, 0x99, 0x9A).

ALS_STATUS2 Register

Figure 36:
ALS_STATUS2

Addr: 0x9B		ALS_STATUS2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	ALS_DATA1_GAIN_STATUS	0	R	Contains gain for data in ALS_DATA1 registers.
3:0	ALS_DATA0_GAIN_STATUS	0	R	Contains gain for data in ALS_DATA0 registers.

Note(s):

1. Return to the Register Map (0x9B).

ALS_STATUS3 Register

Figure 37:
ALS_STATUS3

Addr: 0x9C		ALS_STATUS3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3:0	ALS_DATA2_GAIN_STATUS	0	R	Contains gain for data in ALS_DATA2 registers.

Note(s):

1. Return to the Register Map (0x9C).

STATUS2 Register

Figure 38:
STATUS2

Addr: 0x9D		STATUS2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0	R	
6	ALS_DATA_ VALID	0	R	**ALS Data Valid.** Indicates that the ALS state has completed a cycle since either an assertion of AEN or the last readout of the ALS_STATUS register.
5	Reserved	0	R	
4	ALS_DIGITAL_ SATURATION	0	R	**ALS Digital Saturation.** Indicates that a counter value has been reached that cannot be expressed with the selected data format defined with ALS_MSB_POSITION. Maximum counter value also depends on integration time set in the ATIME register.
3	FD_DIGITAL_ SATURATION	0	R	**Flicker Detect Digital Saturation.** Indicates that the maximum counter value has been reached during flicker detection.
2	MOD_ ANALOG_ SATURATION2	0	R	**ALS Analog Saturation of modulator 2.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
1	MOD_ ANALOG_ SATURATION1	0	R	**ALS Analog Saturation of modulator 1.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
0	MOD_ ANALOG_ SATURATION0	0	R	**ALS Analog Saturation of modulator 0.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.

Note(s):

1. Return to the Register Map (0x9D).

STATUS3 Register

Figure 39:
STATUS3

Addr: 0x9E		STATUS3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	AINT_HYST_ STATE_VALID	0	R	Indicates that the ALS interrupt hysteresis state AINT_HYST_STATE is valid. It will get asserted as soon as the value exceeds the high or the low ALS interrupt thresholds by APERS times. It is automatically cleared with AEN or PON set to 0.
6	AINT_HYST_ STATE_RD	0	R	This bit indicates the state in the hysteresis defined with AINT_AILT and AINT_AIHT, Preset of state is possible before AEN is set. The contents of this register is forwarded to the INT/VSYNC_GPIO pin in case of AINT interrupt direct mode.
5	AINT_AIHT	0	R/W	**ALS Interrupt High**. Indicates that an ALS interrupt occurred because the ALS data exceeded the high threshold. Writing '1' to this bit clears this interrupt.
4	AINT_AILT	0	R/W	**ALS Interrupt Low.** Indicates that an ALS interrupt occurred because the ALS data is below the low threshold. Writing '1' to this bit clears this interrupt.
3	VSYNC_LOST	1	R	Indicates that synchronization is out of sync with clock provided at vsync pin. Default value is "1" since device always starts unsynchronized. The detected vsync clock is not within the expected range. Please see VSYNC_PERIOD_TARGET for more details.
2	Reserved	0		
1	OSC_CALIB_ SATURATION	0	R	Indicates that oscillator calibration with the current values of TRIM_OSC and OSC_TUNE is out of range abs(TRIM_OSC+OSC_TUNE) > 32
0	OSC_CALIB_ FINISHED	0	R	Indicates that oscillator calibration is finished.

Note(s):

1. Return to the Register Map (0x9E).

STATUS4 Register

Figure 40:
STATUS4

Addr: 0x9F		STATUS4		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3	MOD_SAMPLE_ TRIGGER_ERROR	0	R	Indicates that measured data is corrupted. For a valid measurement, this bit must not be asserted. This error condition does not trigger an interrupt, however AEN and FDEN will be cleared and SINT_MEASURMENT_SEQUENCER will be set. Writing "1" clears this bit.
2	MOD_TRIGGER_ ERROR	0	R	Indicates that WTIME is too short for the programmed configuration (SAMPLE_TIME, ALS_ NR_SAMPLES, FD_NR_SMAPLES). This error condition does not trigger an interrupt. Writing "1" clears this bit.
1	SAI_ACTIVE	0	R	**Sleep After Interrupt Active.** Indicates that the device is in sleep due to an interrupt. To exit sleep mode, clear this bit by writing '1' to CLEAR_SAI_ ACTIVE.
0	INIT_BUSY	0	R	**Initialization Busy.** Indicates that the device is initializing. This bit will remain 1 for about 300µs after power on. Do not interact with the device until initialization is complete (e.g. via I^2C).

Note(s):

1. Return to the Register Map (0x9F).

STATUS5 Register

Figure 41:
STATUS5

Addr: 0xA0		STATUS5		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:2	Reserved	0		
1	SINT_MEASUREMENT_ SEQUENCER	0	R/W	Indicates a measurement sequencer system interrupt in case MOD_SAMPLE_TRIGGER_ERROR occurs or after each sequencer step/round depending on the status of MEASUREMENT_SEQUENCER_SIENT_PER_STEP. In parallel SIEN_MEASUREMENT_SEQUENCER must be set. Writing '1' to this bit clears this interrupt.

Addr: 0xA0		STATUS5		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
0	SINT_VSYNC	0	R/W	Indicates that SYNCH_LOST is set or reset. SYNCH_LOST gets set if the waiting timeout for VSYNC_TIMEOUT is reached. In parallel SIEN_VSYNC must be set. Writing '1' to this bit clears this interrupt.

Note(s):

1. Return to the Register Map (0xA0).

CFG0 Register

Figure 42:
CFG0

Addr: 0xA1		CFG0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	SAI	0	R/W	**Sleep After Interrupt.** If asserted, the oscillator is turned off whenever interrupt is active (low). SAI_ ACTIVE is set in this event. To activate the oscillator again, service and clear all interrupts plus clear the SAI_ ACTIVE bit by writing "1" to CLEAR_SAI_ACTIVE. Sleep after interrupt is asserted only in combination with MEASUREMENT_SEQUENCER_SINT_PER_STEP or SIEN or SIEN_MEASUREMENT_SEQUENCER.
5	LOWPOWER_IDLE	0	R/W	**Low Power Idle.** When asserted, the device will automatically run in a low power mode whenever all functions are in wait states or disabled.
4:0	Reserved	01000b	R	Do not overwrite default.

Note(s):

1. Return to the Register Map (0xA1).

CFG1 Register

Figure 43:
CFG1

Addr: 0xA2		CFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		

Addr: 0xA2		CFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
2	DO_ALS_FINAL_ PROCESSING	0	R/W	If this bit is set to "1" and flicker measurement takes longer than ALS measurement, ALS measurement writings are postponed until flicker measurement is finished. Otherwise ALS data is not written to FIFO.
1:0	Reserved	0		

Note(s):

1. Return to the Register Map (0xA2).

CFG2 Register

Figure 44:
CFG2

Addr: 0xA3		CFG2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	AINT_DIRECT	0	R/W	**ALS Interrupt Direct.** Enables the direct mode of ALS interrupt. ALS interrupts are only generated when ALS_DATA (selected by ALS_THRESHOLD_ CHANNEL) moves over the hysteresis edges (AINT_ AILT and AINT_AIHT). If bit is "0", interrupts are always generated if ALS_DATA is above AIHT or below AILT. The status of the ALS interrupt is directly output on the INT or GPIO pin if this mode is enabled and either of those pins are configured to do so according to the INT_PINMAP and VSYNC_GPIO_ PINMAP settings.
6:1	Reserved	0		
0	FIFO_THR[0]	1	R/W	FIFO threshold LSB. Please see FIFO_THR for information.

Note(s):

1. Return to the Register Map (0xA3).

CFG3 Register

Figure 45:
CFG3

Addr: 0xA4		CFG3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	0		
5:4	INT_PINMAP	0	R/W	**Interrupt Pin Mapping.** Defines internal signal which is routed to the external INT pin. 00: Default, INTERRUPT 01: AINT_HYST_STATE 10: Reserved, do not use 11: Reserved, do not use
3:2	Reserved	0		
1:0	VSYNC_GPIO_PINMAP	0	R/W	Vsync/GPIO Pin Mapping. Defines internal signal which is routed to the external VSYNC/GPIO pin. 00: Default, VSYNC_GPIO_OUT 01: AINT_HYST_STATE 10: Reserved, do not use 11: Reserved, do not use

Note(s):

1. Return to the Register Map (0xA4).

CFG4 Register

Figure 46:
CFG4

Addr: 0xA5		CFG4		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	MOD_CALIBRATION_ NTH_ITERATION_ STEP_ENABLE	0	R/W	Enable a modulator calibration with nth iterations per sequencer step instead of waiting for a full round for all sequencers to be finished. In case of AGC enabled (MOD_CALIB_NTH_ITERATION_AGC_ ENABLE) this bit must be set "0", otherwise AGC will not properly work.
5	MEASUREMENT_ SEQUENCER_AGC_ PREDICT_TARGET_ LEVEL	0	R/W	Sets the target measurement levels for AGC prediction. 0: 50% of max value 1: 25% of max value
4	MEASURMENT_ SEQUENCER_ SINT_PER_STEP	0	R/W	Invokes the system interrupt SINT_MEASUREMENT_ SEQUENCER per sequencer step instead of after a full sequencer round.
3	OSC_TUNE_NO_ RESET	0	R/W	OSC_TUNE is set to "0" at each transition of PON from "0" to "1". If OSC_TUNE_NO_RESET is asserted, OSC_TUNE is not reset to "0".
2	Reserved	0		
1:0	MOD_ALS_FIFO_ DATA_FORMAT	0	R/W	Sets the format for ALS data written to FIFO. Please observe readout pattern if digital or analog saturation has occurred. 00: 16-bit (0xFFFF is encoded as analog saturation, 0xFFFE is encoded as digital saturation). 01: 24-bit (0xFFFFFF is encoded as analog saturation, 0xFFFFFE is encoded as digital saturation). 10: Reserved. 11: 32-bit (0xFFFFFFFF is encoded as analog saturation, no digital saturation will happen).

Note(s):

1. Return to the Register Map (0xA5).

CFG5 Register

Figure 47:
CFG5

Addr: 0xA6		CFG5		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	0		
5:4	ALS_THRESHOLD_ CHANNEL	0	R/W	Selects the modulator channel used for the ALS threshold metering and subsequent interrupt. 00: Default, modulator0 01: Modulator1 10: Modulator2 11: Modulator0
3:0	APERS	0	R/W	ALS Interrupt Persistence. Defines a filter for the number of consecutive occurrences that ALS measurement data must remain outside the threshold range between AILT and AIHT before an interrupt is generated. The ALS data channel used for the persistence filter is set by ALS_THRESHOLD_ CHANNEL. Any sample that is inside the threshold range resets the counter to 0. Interrupts are generated at 0x0: Every ALS cycle 0x1: Any ALS value outside the threshold range 0x2: 2 consecutive ALS values outside the range 0x3: 3 consecutive ALS values outside the range 0x4: 5 … 0x5: 10 … …… continued in increments of 5 values 0xE: 55 … 0xF: 60 consecutive ALS values outside the range

Note(s):

1. Return to the Register Map (0xA6).

CFG6 Register

Figure 48:
CFG6

Addr: 0xA7		CFG6		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	0		
5	MOD_MEASUREMENT_ COMPLETE_STARTUP	0	R/W	Activated complete start procedure in for each measurement sample. This reduces measurement time per sample by 9 modulator clock cycles.
4	Reserved	0		
3:2	MOD_MINIMUM_ RESIDUAL_BITS	0	R/W	Limits the number of residual bits to a minimum within this value. ATTENTION: When this function is used, the default settings for the gains are not correct anymore. Thus a residual calibration is mandatory (use MOD_CALIB_RESIDUAL_ ENABLE_AUTO_CALIB_ON_GAIN_CHANGE or MOD_CALIB_NTH_ITERATION_RC_ ENABLE to enforce residual calibration) 00b: 0 residual bits at minimum (default, turned off) 01b: 1 residual bits at minimum 10b: 2 residual bits at minimum 11b: 3 residual bits at minimum
1:0	MOD_MAXIMUM_ RESIDUAL_BITS	0x3	R/W	Limits the number of residual bits to a maximum within this value. ATTENTION: When this function is used, the default settings for the gains are not correct anymore. Thus a residual calibration is mandatory (use MOD_CALIB_RESIDUAL_ ENABLE_AUTO_CALIB_ON_GAIN_CHANGE or MOD_CALIB_NTH_ITERATION_RC_ ENABLE to enforce residual calibration) 00b: 1 residual bits at maximum 01b: 2 residual bits at maximum 10b: 3 residual bits at maximum (default) 11b: 4 residual bits at maximum

Note(s):

1. Return to the Register Map (0xA7).

CFG7 Register

Figure 49:
CFG7

Addr: 0xA8		CFG7		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	Reserved	0x01		

Note(s):

1. Return to the Register Map (0xA8).

CFG8 Register

Figure 50:
CFG8

Addr: 0xA9		CFG8		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_SEQUENCER_ MAX_MOD_GAIN	0x0C	R/W	Sets the maximum gain for all channels in all sequencer steps.
3:0	MEASUREMENT_SEQUENCER_ AGC_PREDICT_MOD_GAIN_ REDUCTION	0x04	R/W	Sets the modulator gain reduction in AGC predict mode. All channels in the actual measurement sequence are reduced by the programmed gain reduction before gain prediction starts.

Note(s):

1. Return to the Register Map (0xA9).

CFG9 Register

Figure 51:
CFG9

Addr: 0xAA		CFG9		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:2	Reserved	0		
1:0	MOD_RESIDUAL_ BITS_IGNORE	0	R/W	Sets the number of residual bits ignored and shifted in flicker data. Please observe to set MOD_FD_FIFO_ DATAx_WIDTH accordingly.

Note(s):

1. Return to the Register Map (0xAA).

AGC Number of Samples Registers

Figure 52:
AGC Number of Samples

Addr	Bit	Field	Reset	Type	Description
0xAC	7:0	AGC_NR_SAMPLES[7:0]	0	R/W	AGC Number of Samples Sets the time for every AGC measurement and is calculated as: agc_atime = (AGC_NR_SAMPLES+1) x (SAMPLE_TIME+1) x 1.388889µs
0xAD	7:3	Reserved	0		
0xAD	2:0	AGC_NR_SAMPLES[10:8]	0	R/W	

Note(s):

1. Return to the Register Map (0xAC, 0xAD).

TRIGGER_MODE Register

Figure 53:
TRIGGER_MODE

Addr: 0xAE		TRIGGER_MODE		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2:0	MOD_TRIGGER_ TIMING	0	R/W	Sets the repetition rate of a modulator or sequencer measurement. Counting will immediately start or will wait for the first vsync pulse. 000: OFF 001: Normal = 2.844ms * WTIME 010: Long = 45.511ms * WTIME 011: Fast = 88.889µs * WTIME 100: Fastlong = 1.422ms * WTIME 101: vsync = One vsync per WTIME step 110: Reserved 111: Reserved

Note(s):

1. Return to the Register Map (0xAE).

CONTROL Register

Figure 54:
CONTROL

Addr: 0xB1		CONTROL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3	SOFT_RESET	0	R/W	Software Reset. If set and executable, the Software Reset will initialize the device in the same way as hardware reset. Prior to invoking a SOFT_RESET the oscillator must be switched on. Set PON=1.
2	Reserved	0		
1	FIFO_CLR	0	R/W	Setting this bit will clear the FIFO, as well as FINT, FIFO_OVERFLOW, FIFO_UNDERFLOW and FIFO_LVL.
0	CLEAR_SAI_ACTIVE	0	R/W	Setting this bit will clear the Sleep After Interrupt Active SAI_ACTIVE and start measurements if enabled.

Note(s):

1. Return to the Register Map (0xB1).

INTENAB Register

Figure 55:
INTENAB

Addr: 0xBA		INTENAB		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MIEN	0	R/W	Modulator Interrupt Enable. Setting this bit will allow a modulator interrupt on the external INT pin. Please check in STATUS2 for the reason of the interrupt.
6:4	Reserved	0		
3	AIEN	0	R/W	ALS Interrupt Enable. Setting this bit will allow an ALS interrupt on the external INT pin. Please check in STATUS3 for the reason of the interrupt.
2	FIEN	0		FIFO Interrupt Enable. Setting this bit will allow a FIFO interrupt on the external INT pin. Check FINT for further information.
1	Reserved	0		
0	SIEN		R/W	System Interrupt Enable. Setting this bit will allow a system interrupt on the external INT pin. Please check in STATUS3 for the reason of the interrupt.

Note(s):

1. Return to the Register Map (0xBA).

SIEN Register

Figure 56:
SIEN

Addr: 0xBB		SIEN		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:2	Reserved	0		
1	SIEN_MEASUREMENT_ SEQUENCER	0	R/W	Measurement Sequencer Interrupt Enable. Setting this bit will allow a system interrupt SINT as soon as invoked by a measurement sequencer event. Please see SINT_MEASUREMENT_ SEQUENCER for further information.
0	SIEN_VSYNC	0	R/W	**VSYNC Interrupt Enable.** Setting this bit will allow a system interrupt SINT as soon as a VSYNC interrupt occurs. Please see SINT_VSYNC for further information.

Note(s):

1. Return to the Register Map (0xBB).

MOD_COMP_CFG1 Register

Figure 57:
MOD_COMP_CFG1

Addr: 0xCE		MOD_COMP_CFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	MOD_IDAC_RANGE	10b	R/W	Sets the auto zero range of the current digital-to-analog converter. 00: 58µV 01: 38µV 10: 18µV 11: 9µV
5:0	Reserved	0		

Note(s):

1. Return to the Register Map (0xCE).

MEAS_SEQR_FD_0 Register

Figure 58:
MEAS_SEQR_FD_0

Addr: 0xCF		MEAS_SEQR_FD_0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_MOD1_ FD_PATTERN	0	R/W	Defines the sequence of a flicker measurement on modulator 1. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0.
3:0	MEASUREMENT_ SEQUENCER_MOD0_ FD_PATTERN	0x1	R/W	Defines the sequence of a flicker measurement on modulator 0. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default sequencer step 0 is used on modulator 0.

Note(s):

1. Return to the Register Map (0xCF).

MEAS_SEQR_ALS_FD_1 Register

Figure 59:
MEAS_SEQR_ALS_FD_1

Addr: 0xD0		MEAS_SEQR_ALS_FD_1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_MOD2_ FD_PATTERN	0	R/W	Defines the sequence of a flicker measurement on modulator 2. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0.
3:0	MEASUREMENT_ SEQUENCER_ALS_ PATTERN	0x1	R/W	Defines the sequence of an ALS measurement on all modulators. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default sequencer step 0 is executed on all modulators.

Note(s):

1. Return to the Register Map (0xD0).

MEAS_SEQR_APERS_AND_VSYNC_WAIT Register

Figure 60:
MEAS_SEQR_APERS_AND_VSYNC_WAIT

Addr: 0xD1		MEAS_SEQR_APERS_AND_VSYNC_WAIT		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_VSYNC_ WAIT_PATTERN	0	R/W	Defines if a measurement sequence shall wait for a VSYNC before starting the measurement. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0.
3:0	MEASUREMENT_ SEQUENCER_APERS_ PATTERN	0x1	R/W	Defines the sequencer steps where an ALS persistence evaluation shall be performed on modulator data selected by ALS_THRESHOLD_ CHANNEL. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default step 0 is used on all modulators.

Note(s):

1. Return to the Register Map (0xD1).

MEAS_SEQR_RESIDUAL_0 Register

Figure 61:
MEAS_SEQR_RESIDUAL_0

Addr: 0xD2		MEAS_SEQR_RESIDUAL_0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_MOD1_ RESIDUAL_ENABLE_ PATTERN	0xF	R/W	Defines if a residual measurement on modulator 1 shall be executed. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default a residual measurement is done in all sequencer steps.
3:0	MEASUREMENT_ SEQUENCER_MOD0_ RESIDUAL_ENABLE_ PATTERN	0xF	R/W	Defines if a residual measurement on modulator 0 shall be executed. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default a residual measurement is done in all sequencer steps.

Note(s):

1. Return to the Register Map (0xD2).

MEAS_SEQR_RESIDUAL_1_AND_WAIT Register

Figure 62:
MEAS_SEQR_RESIDUAL_1_AND_WAIT

Addr: 0xD3		MEAS_SEQR_RESIDUAL_1_AND_WAIT		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ WAIT_PATTERN	0x1	R/W	Defines if a sequencer step will wait for the modulator trigger timer to finish as programmed in MOD_TRIGGER_TIMING and WTIME. At the same time the timer is restarted. In case this bit is not set, the next sequencer step will start as soon as all measurements in the prior step are completed. Please observe that MOD_TRIGGER_TIMING is “0” by default. In this case the programmed wait pattern is ignored since measurement time has always priority over wait time. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of “0000” refers to sequencer step 3, the rightmost refers to sequencer step 0. By default the wait is executed for sequencer step 3 (last sequencer step).
3:0	MEASUREMENT_ SEQUENCER_MOD2_ RESIDUAL_ENABLE_ PATTERN	0xF	R/W	Defines if a residual measurement on modulator 2 shall be executed. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of “0000” refers to sequencer step 3, the rightmost refers to sequencer step 0. By default a residual measurement is done in all sequencer steps.

Note(s):

1. Return to the Register Map (0xD3).

MEAS_SEQR_STEP0_MOD_GAINX_L Register

Figure 63:
MEAS_SEQR_STEP0_MOD_GAINX_L

Addr: 0xD4		MEAS_SEQR_STEP0_MOD_GAINX_L		
Bit	Field	Reset	Type	Bit Description
7:4	MEASUREMENT_SEQUENCER_STEP0_MOD_GAIN1	0x8	R/W	Defines the gain of modulator 1 for the measurement sequencer step 0. The gain is also updated by the AGC, if activated. 0x00: 1/2x 0x01: 1x 0x02: 2x 0x03: 4x 0x04: 8x 0x05: 16x 0x06: 32x 0x07: 64x 0x08: 128x 0x09: 256x 0x0A: 512x 0x0B: 1024x 0x0C: 2048x 0x0D: 4096x
3:0	MEASUREMENT_SEQUENCER_STEP0_MOD_GAIN0	0x8	R/W	Defines the gain of modulator 0 for the measurement sequencer step 0. The gain is also updated by the AGC, if activated. Gain steps see under modulator 1 above.

Note(s):

1. Return to the Register Map (0xD4).

MEAS_SEQR_STEP0_MOD_GAINX_H Register

Figure 64:
MEAS_SEQR_STEP0_MOD_GAINX_H

Addr: 0xD5		MEAS_SEQR_STEP0_MOD_GAINX_H		
Bit	Field	Reset	Type	Bit Description
7:4	Reserved	0		
3:0	MEASUREMENT_SEQUENCER_STEP0_MOD_GAIN2	0x8	R/W	Defines the gain of modulator 2 for the measurement sequencer step 0. The gain is also updated by the AGC, if activated.

Note(s):

1. Return to the Register Map (0xD5).

MEAS_SEQR_STEP1_MOD_GAINX_L Register

Figure 65:
MEAS_SEQR_STEP1_MOD_GAINX_L

Addr: 0xD6		MEAS_SEQR_STEP1_MOD_GAINX_L		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_SEQUENCER_STEP1_MOD_GAIN1	0x8	R/W	Defines the gain of modulator 1 for the measurement sequencer step 1.
3:0	MEASUREMENT_SEQUENCER_STEP1_MOD_GAIN0	0x8	R/W	Defines the gain of modulator 0 for the measurement sequencer step 1.

Note(s):

1. Return to the Register Map (0xD6).

MEAS_SEQR_STEP1_MOD_GAINX_H Register

Figure 66:
MEAS_SEQR_STEP1_MOD_GAINX_H

Addr: 0xD7		MEAS_SEQR_STEP1_MOD_GAINX_H		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3:0	MEASUREMENT_SEQUENCER_STEP1_MOD_GAIN2	0x8	R/W	Defines the gain of modulator 2 for the measurement sequencer step 1.

Note(s):

1. Return to the Register Map (0xD7).

MEAS_SEQR_STEP2_MOD_GAINX_L Register

Figure 67:
MEAS_SEQR_STEP2_MOD_GAINX_L

Addr: 0xD8		MEAS_SEQR_STEP2_MOD_GAINX_L		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_STEP2_ MOD_GAIN1	0x8	R/W	Defines the gain of modulator 1 for the measurement sequencer step 2.
3:0	MEASUREMENT_ SEQUENCER_STEP2_ MOD_GAIN0	0x8	R/W	Defines the gain of modulator 0 for the measurement sequencer step 2.

Note(s):

1. Return to the Register Map (0xD8).

MEAS_SEQR_STEP2_MOD_GAINX_H Register

Figure 68:
MEAS_SEQR_STEP2_MOD_GAINX_H

Addr: 0xD9		MEAS_SEQR_STEP2_MOD_GAINX_H		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3:0	MEASUREMENT_ SEQUENCER_STEP2_ MOD_GAIN2	0x8	R/W	Defines the gain of modulator 2 for the measurement sequencer step 2.

Note(s):

1. Return to the Register Map (0xD9).

MEAS_SEQR_STEP3_MOD_GAINX_L Register

Figure 69:
MEAS_SEQR_STEP3_MOD_GAINX_L

Addr: 0xDA		MEAS_SEQR_STEP3_MOD_GAINX_L		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_STEP3_ MOD_GAIN1	0x8	R/W	Defines the gain of modulator 1 for the measurement sequencer step 3.
3:0	MEASUREMENT_ SEQUENCER_STEP3_ MOD_GAIN0	0x8	R/W	Defines the gain of modulator 0 for the measurement sequencer step 3.

Note(s):

1. Return to the Register Map (0xDA).

MEAS_SEQR_STEP3_MOD_GAINX_H Register

Figure 70:
MEAS_SEQR_STEP3_MOD_GAINX_H

Addr: 0xDB		MEAS_SEQR_STEP3_MOD_GAINX_H		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3:0	MEASUREMENT_ SEQUENCER_STEP3_ MOD_GAIN2	0x8	R/W	Defines the gain of modulator 2 for the measurement sequencer step 3.

Note(s):

1. Return to the Register Map (0xDB).

MEAS_SEQR_STEP0_MOD_PHDX_SMUX_L Register

Figure 71:
MEAS_SEQR_STEP0_MOD_PHDX_SMUX_L

Addr: 0xDC		MEAS_SEQR_STEP0_MOD_PHDX_SMUX_L		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	MEASUREMENT_ SEQUENCER_STEP0_ MOD_PHD3_SMUX	01b	R/W	Defines connection of photodiode 3 to modulator for sequencer step 0 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
5:4	MEASUREMENT_ SEQUENCER_STEP0_ MOD_PHD2_SMUX	10b	R/W	Defines connection of photodiode 2 to modulator for sequencer step 0 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
3:2	MEASUREMENT_ SEQUENCER_STEP0_ MOD_PHD1_SMUX	01b	R/W	Defines connection of photodiode 1 to modulator for sequencer step 0 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
1:0	MEASUREMENT_ SEQUENCER_STEP0_ MOD_PHD0_SMUX	10b	R/W	Defines connection of photodiode 0 to modulator for sequencer step 0 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2

Note(s):

1. Return to the Register Map (0xDC).

MEAS_SEQR_STEP0_MOD_PHDX_SMUX_H Register

Figure 72:
MEAS_SEQR_STEP0_MOD_PHDX_SMUX_H

Addr: 0xDD		MEAS_SEQR_STEP0_MOD_PHDX_SMUX_H		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3:2	MEASUREMENT_ SEQUENCER_STEP0_ MOD_PHD5_SMUX	01b	R/W	Defines connection of photodiode 5 to modulator for sequencer step 0 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
1:0	MEASUREMENT_ SEQUENCER_STEP0_ MOD_PHD4_SMUX	10b	R/W	Defines connection of photodiode 4 to modulator for sequencer step 0 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2

Note(s):

1. Return to the Register Map (0xDD).

MEAS_SEQR_STEP1_MOD_PHDX_SMUX_L Register

Figure 73:
MEAS_SEQR_STEP1_MOD_PHDX_SMUX_L

Addr: 0xDE		MEAS_SEQR_STEP1_MOD_PHDX_SMUX_L		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	MEASUREMENT_ SEQUENCER_STEP1_ MOD_PHD3_SMUX	10b	R/W	Defines connection of photodiode 3 to modulator for sequencer step 1 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
5:4	MEASUREMENT_ SEQUENCER_STEP1_ MOD_PHD2_SMUX	00b	R/W	Defines connection of photodiode 2 to modulator for sequencer step 1 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
3:2	MEASUREMENT_ SEQUENCER_STEP1_ MOD_PHD1_SMUX	01b	R/W	Defines connection of photodiode 1 to modulator for sequencer step 1 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
1:0	MEASUREMENT_ SEQUENCER_STEP1_ MOD_PHD0_SMUX	00b	R/W	Defines connection of photodiode 0 to modulator for sequencer step 1 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2

Note(s):

1. Return to the Register Map (0xDE).

MEAS_SEQR_STEP1_MOD_PHDX_SMUX_H Register

Figure 74:
MEAS_SEQR_STEP1_MOD_PHDX_SMUX_H

Addr: 0xDF		MEAS_SEQR_STEP1_MOD_PHDX_SMUX_H		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_AGC_ ASAT_PATTERN	1111b	R/W	Defines the sequencer steps where analog saturation AGC is enabled for the corresponding measurement. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default this feature is enabled for all sequencer steps.
3:2	MEASUREMENT_ SEQUENCER_STEP1_ MOD_PHD5_SMUX	00b	R/W	Defines connection of photodiode 5 to modulator for sequencer step 1 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
1:0	MEASUREMENT_ SEQUENCER_STEP1_ MOD_PHD4_SMUX	11b	R/W	Defines connection of photodiode 4 to modulator for sequencer step 1 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2

Note(s):

1. Return to the Register Map (0xDF).

MEAS_SEQR_STEP2_MOD_PHDX_SMUX_L Register

Figure 75:
MEAS_SEQR_STEP2_MOD_PHDX_SMUX_L

Addr: 0xE0		MEAS_SEQR_STEP2_MOD_PHDX_SMUX_L		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	MEASUREMENT_ SEQUENCER_STEP2_ MOD_PHD3_SMUX	00b	R/W	Defines connection of photodiode 3 to modulator for sequencer step 2 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
5:4	MEASUREMENT_ SEQUENCER_STEP2_ MOD_PHD2_SMUX	00b	R/W	Defines connection of photodiode 2 to modulator for sequencer step 2 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
3:2	MEASUREMENT_ SEQUENCER_STEP2_ MOD_PHD1_SMUX	01b	R/W	Defines connection of photodiode 1 to modulator for sequencer step 2 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
1:0	MEASUREMENT_ SEQUENCER_STEP2_ MOD_PHD0_SMUX	11b	R/W	Defines connection of photodiode 0 to modulator for sequencer step 2 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2

Note(s):

1. Return to the Register Map (0xE0).

MEAS_SEQR_STEP2_MOD_PHDX_SMUX_H Register

Figure 76:
MEAS_SEQR_STEP2_MOD_PHDX_SMUX_H

Addr: 0xE1		MEAS_SEQR_STEP2_MOD_PHDX_SMUX_H		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_AGC_ PREDICT_PATTERN	1111b	R/W	Defines the sequencer steps where predict AGC is enabled for the corresponding measurement. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default this feature is enabled for all sequencer steps.
3:2	MEASUREMENT_ SEQUENCER_STEP2_ MOD_PHD5_SMUX	10b	R/W	Defines connection of photodiode 5 to modulator for sequencer step 2 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
1:0	MEASUREMENT_ SEQUENCER_STEP2_ MOD_PHD4_SMUX	00b	R/W	Defines connection of photodiode 4 to modulator for sequencer step 2 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2

Note(s):

1. Return to the Register Map (0xE1).

MEAS_SEQR_STEP3_MOD_PHDX_SMUX_L Register

Figure 77:
MEAS_SEQR_STEP3_MOD_PHDX_SMUX_L

Addr: 0xE2		MEAS_SEQR_STEP3_MOD_PHDX_SMUX_L		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	MEASUREMENT_ SEQUENCER_STEP3_ MOD_PHD3_SMUX	00b	R/W	Defines connection of photodiode 3 to modulator for sequencer step 3 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
5:4	MEASUREMENT_ SEQUENCER_STEP3_ MOD_PHD2_SMUX	10b	R/W	Defines connection of photodiode 2 to modulator for sequencer step 3 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
3:2	MEASUREMENT_ SEQUENCER_STEP3_ MOD_PHD1_SMUX	01b	R/W	Defines connection of photodiode 1 to modulator for sequencer step 3 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
1:0	MEASUREMENT_ SEQUENCER_STEP3_ MOD_PHD0_SMUX	00b	R/W	Defines connection of photodiode 0 to modulator for sequencer step 3 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2

Note(s):

1. Return to the Register Map (0xE2).

MEAS_SEQR_STEP3_MOD_PHDX_SMUX_H Register

Figure 78:
MEAS_SEQR_STEP3_MOD_PHDX_SMUX_H

Addr: 0xE3		MEAS_SEQR_STEP3_MOD_PHDX_SMUX_H		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0000b		
3:2	MEASUREMENT_ SEQUENCER_STEP3_ MOD_PHD5_SMUX	00b	R/W	Defines connection of photodiode 5 to modulator for sequencer step 3 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2
1:0	MEASUREMENT_ SEQUENCER_STEP3_ MOD_PHD4_SMUX	11b	R/W	Defines connection of photodiode 4 to modulator for sequencer step 3 00: No connection 01: Modulator 0 10: Modulator 1 11: Modulator 2

Note(s):

1. Return to the Register Map (0xE3).

MOD_CALIB_CFG0 Register

Figure 79:
MOD_CALIB_CFG0

Addr: 0xE4		MOD_CALIB_CFG0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MOD_CALIB_NTH_ ITERATION	0xFF	R/W	Defines the repetition rate of calibrations in sequencer rounds or steps depending on MOD_ CALIB_NTH_ITERATION_STEP_ENABLE. 0x00: Never 0x01-0xFE: Every n^{th} time 0xFF: Only once at start

Note(s):

1. Return to the Register Map (0xE4).

MOD_CALIB_CFG2 Register

Figure 80:
MOD_CALIB_CFG2

Addr: 0xE6		MOD_CALIB_CFG2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MOD_CALIB_NTH_ ITERATION_RC_ ENABLE	1	R/W	Enables a residual calibration during the n^{th} iteration. Please observe that this residual calibration feature only makes sense for modulators which are enabled in the first sequences step, since a gain calibration only happens in the first sequencer step.
6	MOD_CALIB_NTH_ ITERATION_AZ_ ENABLE	1	R/W	Enables auto-zero calibration during the n^{th} iteration.
5	MOD_CALIB_NTH_ ITERATION_AGC_ ENABLE	0	R/W	Enables AGC calibration during the n^{th} iteration. Please observe in this case, that MOD_CALIB_NTH_ ITERATION_STEP_ENABLE must be "0" otherwise AGC will not be properly executed.
4	MOD_CALIB_ RESIDUAL_ENABLE_ AUTO_CALIB_ON_ GAIN_CHANGE	1	R/W	Enables an automatic re-calibration in case of a change in gain. This re-calibration is executed at the beginning of each sequencer step.
3:0	Reserved	0x3		

Note(s):

1. Return to the Register Map (0xE6).

VSYNC Period Registers

Figure 81:
VSYNC Period

Addr	Bit	Field	Reset	Type	Description
0xF2	7:0	VSYNC_PERIOD[7:0]	0	R/W	VSYNC Period Contains the measured VSYNC in multiples of 1.3888µs Reading this register clears HOLD_VSYNC_PERIOD
0xF3	7:0	VSYNC_PERIOD[15:8]	0	R/W	

Note(s):

1. Return to the Register Map (0xF2, 0xF3).

VSYNC_PERIOD_TARGET Registers

Figure 82:
VSYNC_PERIOD_TARGET

Addr	Bit	Field	Reset	Type	Description
0xF4	7:0	VSYNC_PERIOD_TARGET[7:0]	0	R/W	VSYNC Period Target Defines the ideal target value for the VSYNC_PERIOD. Configure properly before enabling the oscillator calibration, otherwise it will cause malfunction or overflow. See VSYNC_PERIOD_USE_FAST_TIMING_EVAL for the calculation of VSYNC_PERIOD_TARGET.
0xF5	6:0	VSYNC_PERIOD_TARGET[14:8]	0	R/W	
0xF5	7	VSYNC_PERIOD_USE_FAST_TIMING_EVAL	0	R/W	If set to "0", the VSYNC_PERIOD_TARGET shall match VSYNC_PERIOD[15:1], supports range from 15Hz to 500Hz. VSYNC_PERIOD_TARGET = (720KHz / f_{VSYNC})/2 e.g. for f_{VSYNC} = 60Hz, VSYNC_PERIOD_TARGET = 0x1770 If set to "1", the VSYNC_PERIOD_TARGET shall match VSYNC_PERIOD[14:0], supports range from 30Hz to 1KHz. VSYNC_PERIOD_TARGET = 720KHz / f_{VSYNC} e.g. for f_{VSYNC} = 60Hz, VSYNC_PERIOD_TARGET = 0x2EE0

Note(s):

1. Return to the Register Map (0xF4, 0xF5).

VSYNC_CONTROL Register

Figure 83:
VSYNC_CONTROL

Addr: 0xF6		VSYNC_CONTROL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:2	Reserved	0		
1	HOLD_VSYNC_PERIOD	0	R/W	If set to "1" VSYNC_PERIOD[15:8] and VSYNC_PERIOD[7:0] cannot be updated until VSYNC_PERIOD[15:8] has been read. It will avoid that updates during I^2C readings.
0	SW_VSYNC_TRIGGER	0	R/W	If VSYNC_MODE is set to "1", this bit can be used to trigger a SW sync. In case the exact time is known between two consecutive I^2C reading the offset of the oscillator frequency can be calculated from the result in VSYNC_TRIGGER.

Note(s):

1. Return to the Register Map (0xF6).

VSYNC_CFG Register

Figure 84:
VSYNC_CFG

Addr: 0xF7		VSYNC_CFG		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	OSC_CALIB_MODE	0	R/W	Oscillator Calibration Mode Register 00: Osc cal disabled 01: Osc cal after PON, if PON goes to "1" or after each VSYNC_LOST goes to "0" an oscillator calibration is performed if no measurement cycle is active 10: Osc cal always on, an oscillator calibration is permanently performed if no measurement cycle is active and no VSYNC_LOST is set. 11: Reserved, do not use.
5:3	Reserved	0		
2	VSYNC_MODE	0	R/W	Determines which VSYNC signal is used as a trigger 0: Use the external pin signal from VSYNC/GPIO/INT as a trigger 1: Use SW_VSYNC_TRIGGER as a trigger.
1	VSYNC_SELECT	0	R/W	Determines whether the external VSYNC/GPIO pin or the INT pin is used a trigger signal 0: VSYNC/GPIO 1: INT
0	VSYNC_INVERT	0	R/W	If set to "1" the VSYNC input signal is inverted.

Note(s):

1. Return to the Register Map (0xF7).

VSYNC_GPIO_INT Register

Figure 85:
VSYNC_GPIO_INT

Addr: 0xF8		VSYNC_GPIO_INT		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	INT_INVERT	0	R/W	If set to "1" the INT pin output is inverted. This applies to all output signals as selected in INT_PINMAP.
5	INT_IN_EN	0	R/W	If programmed to "1" the INT pin is set as input. Please observe that the connected net must not be floating since INT is an open drain input.
4	INT_IN	0	R	External HIGH or LOW value applied to INT pin.
3	VSYNC_GPIO_INVERT	0	R/W	If set to "1" the VSYNC/GPIO pin output is inverted. This applies to all output signals as selected in VSYNC_GPIO_PINMAP.
2	VSYNC_GPIO_IN_EN	0	R/W	If programmed to "1" the VSYNC/GPIO pin is set as input. Please observe that the connected net must not be floating since VSYNC/GPIO is an open drain input.
1	VSYNC_GPIO_OUT	1	R/W	Programs the VSYNC/GPIO pin HI or LOW. Since the pin is an open drain I/O pin, the default value is HIGH to avoid any unintended power consumption through pull-up resistor. The routed internal signal is selected in VSYNC_GPIO_PINMAP.
0	VSYNC_GPIO_IN	0	R	External HIGH or LOW value applied to VSYNC/GPIO pin.

Note(s):

1. Return to the Register Map (0xF8).

MOD_FIFO_DATA_CFG0 Register

Figure 86:
MOD_FIFO_DATA_CFG0

Addr: 0xF9		MOD_FIFO_DATA_CFG0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MOD_ALS_FIFO_DATA0_ WRITE_ENABLE	1	R/W	Enables to write ALS data of modulator 0 into the FIFO under the following conditions: • Flicker measurement is disabled in the sequencer step or flicker measurement has been finished (ALS_NR_SAMPLES >= FD_NR_ SAMPLES). • In case (ALS_NR_SAMPLES < FD_NR_SAMPLES) then DO_ALS_FINAL_PROCESSING_AFTER_ FLICKER must be set to "1".
6	Reserved	0		
5	MOD_FD_FIFO_DATA0_ COMPRESSION_ENABLE	0	R/W	Enables data compression in case of flicker measurements.
4	MOD_FD_FIFO_DATA0_ DIFFERENCE_ENABLE	0	R/W	If set, only the delta value between two consecutive samples is written into FIFO. The setting makes only sense in combination with enabled data compression (MOD_FD_FIFO_ DATA0_COMPRESSION_ENABLE).
3:0	MOD_FD_FIFO_ DATA0_WIDTH	0xF	R/W	Defines absolute number of bits from a sample written to FIFO E.g. if set to 10, 11 bits (0-10) are written into the FIFO.

Note(s):

1. Return to the Register Map (0xF9).

MOD_FIFO_DATA_CFG1 Register

Figure 87:
MOD_FIFO_DATA_CFG1

Addr: 0xFA		MOD_FIFO_DATA_CFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MOD_ALS_FIFO_DATA1_ WRITE_ENABLE	1	R/W	Enables to write ALS data of modulator 1 into the FIFO under the following conditions: • Flicker measurement is disabled in the sequencer step or flicker measurement has been finished (ALS_NR_SAMPLES >= FD_NR_ SAMPLES). • In case (ALS_NR_SAMPLES < FD_NR_SAMPLES) then DO_ALS_FINAL_PROCESSING_AFTER_ FLICKER must be set to "1".
6	Reserved	0		
5	MOD_FD_FIFO_DATA1_ COMPRESSION_ENABLE	0	R/W	Enables data compression in case of flicker measurements.
4	MOD_FD_FIFO_DATA1_ DIFFERENCE_ENABLE	0	R/W	If set, only the delta value between two consecutive samples is written into FIFO. The setting makes only sense in combination with enabled data compression (MOD_FD_FIFO_DATA1_ COMPRESSION_ENABLE).
3:0	MOD_FD_FIFO_ DATA1_WIDTH	0xF	R/W	Defines absolute number of bits from a sample written to FIFO E.g. if set to 10, 11 bits (0-10) are written into the FIFO.

Note(s):

1. Return to the Register Map (0xFA).

MOD_FIFO_DATA_CFG2 Register

Figure 88:
MOD_FIFO_DATA_CFG2

Addr: 0xFB		MOD_FIFO_DATA_CFG2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MOD_ALS_FIFO_DATA2_ WRITE_ENABLE	1	R/W	Enables to write ALS data of modulator 2 into the FIFO under the following conditions: • Flicker measurement is disabled in the sequencer step or In case (ALS_NR_SAMPLES < FD_NR_ SAMPLES) then flicker measurement has been finished (ALS_NR_SAMPLES >= FD_NR_ SAMPLES). • DO_ALS_FINAL_PROCESSING_AFTER_FLICKER must be set to "1".
6	Reserved	0		
5	MOD_FD_FIFO_DATA2_ COMPRESSION_ENABLE	0	R/W	Enables data compression in case of flicker measurements.
4	MOD_FD_FIFO_DATA2_ DIFFERENCE_ENABLE	0	R/W	If set, only the delta value between two consecutive samples is written into FIFO. The setting makes only sense in combination with enabled data compression (MOD_FD_FIFO_DATA2_ COMPRESSION_ENABLE).
3:0	MOD_FD_FIFO_ DATA2_WIDTH	0xF	R/W	Defines absolute number of bits from a sample written to FIFO E.g. if set to 10, 11 bits (0-10) are written into the FIFO.

Note(s):

1. Return to the Register Map (0xFB).

FIFO_THR Register

Figure 89:
FIFO_THR

Addr: 0xFC		FIFO_THR		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FIFO_THR[8:1]	0x7F	R/W	If FIFO_LVL > FIFO_THR a FIFO interrupt FINT is invoked.

Note(s):

1. Return to the Register Map (0xFC).

FIFO_STATUS0 Register

Figure 90:
FIFO_STATUS0

Addr: 0xFD		FIFO_STATUS0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FIFO_LVL[9:2]	0	R	**FIFO Level**. Indicates the number of bytes in FIFO. The FIFO size is 512byte, thus FIFO_LVL ranges between 0 (empty) and 512 (full). Always read FIFO_STATUS0 first and then FIFO_ STATUS1 to get correct FIFO_LVL and the status information.

1. Return to the Register Map (0xFD).

FIFO_STATUS1 Register

Figure 91:
FIFO_STATUS1

Addr: 0xFE		FIFO_STATUS1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	FIFO_OVERFLOW	0	R	If set to “1” a FIFO overflow has occurred and data for the FIFO was lost (e.g. reading from FIFO was too slow). This flag is cleared by PON and FIFO_CLR. Always check this flag before and after reading the FIFO.
6	FIFO_UNDERFLOW	0	R	If set to “1” the FIFO was read out too often and has returned 0 at least once. In such case the read-out data may not consistent anymore. This flag is cleared by PON and FIFO_CLR. Always check this flag before and after reading the FIFO.
5:2	Reserved	0		
1:0	FIFO_LVL[1:0]	0	R	See FIFO_STATUS0 for description.

Note(s):

1. Return to the Register Map (0xFE).

FIFO_DATA Registers

Figure 92:
FIFO_DATA

Addr: 0xFF		FIFO_DATA		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FIFO_DATA	0	R	The register FIFO_DATA can be read-out with single reads or with a block-read. Upon reading out FIFO_DATA, the internal FIFO read pointer is advanced and FIFO_LVL is decreased. A false reading upon the FIFO_LVL will return 0 and set the FIFO_UNDERFLOW flag.

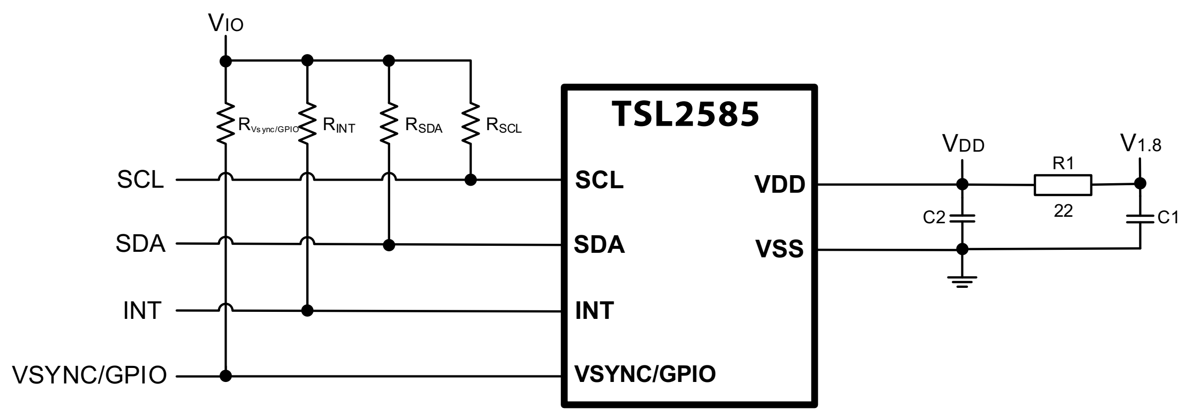
Note(s):

1. Return to the Register Map (0xFF).

Application Information

It is highly recommended to consult the ams OSRAM application team for circuit diagram and layout review at design-in.

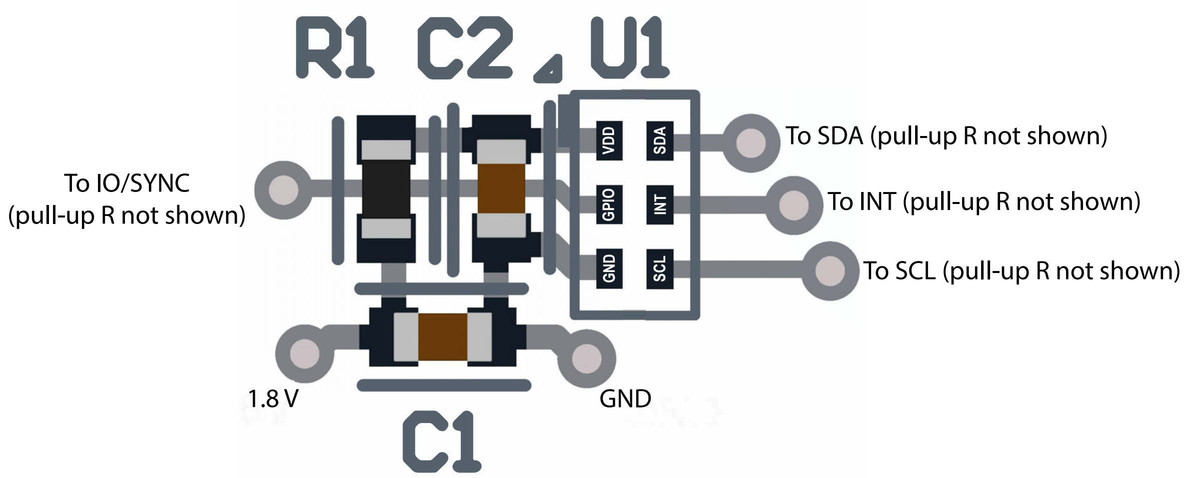
Figure 93:
TSL2585 Typical Application Circuit



Note(s):

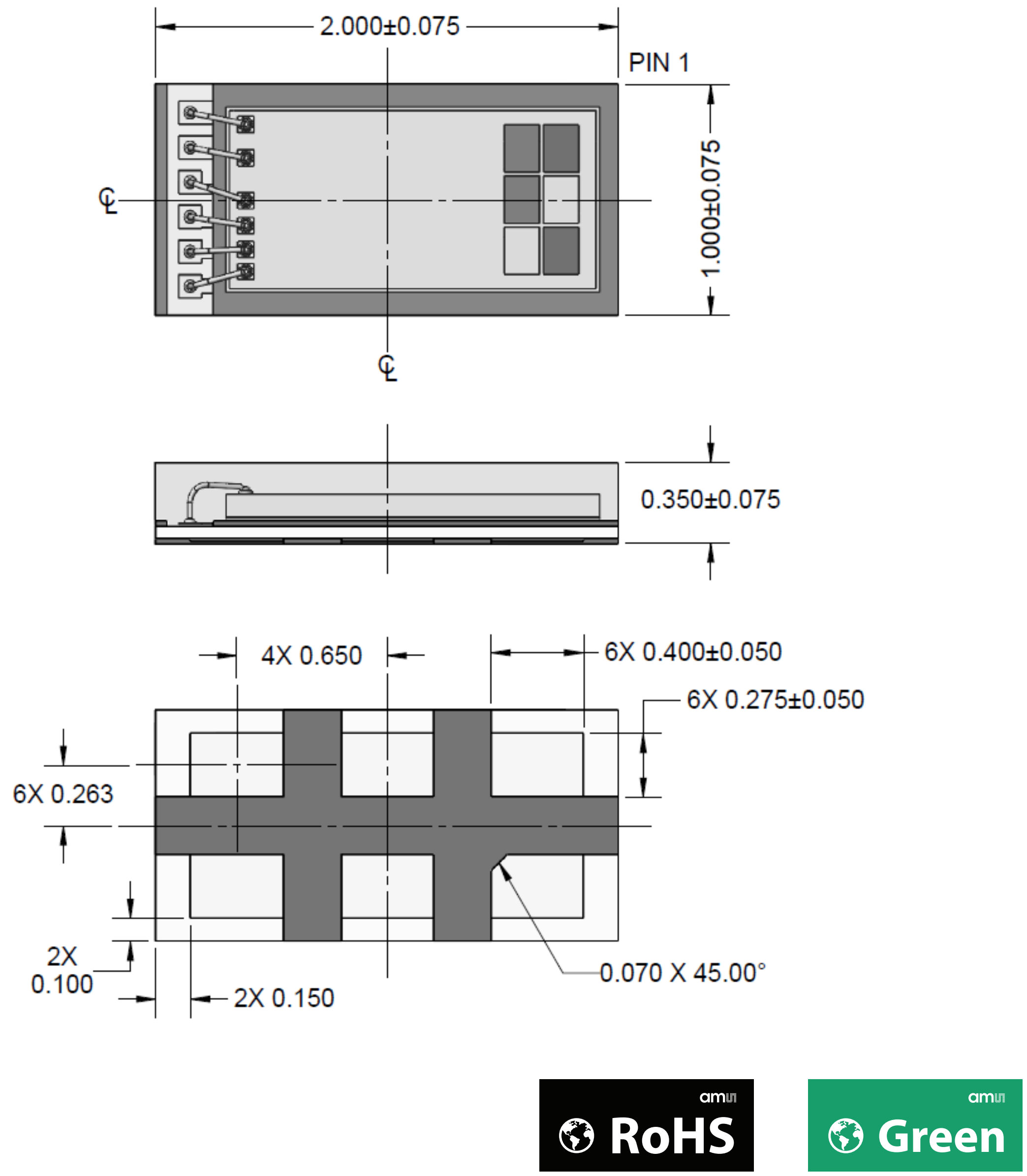
1. C1 in the graphic above shall be 4.7µF, 6.3V, 10% and C2 in the graphic above shall be 1µF, 6.3V, 20%. All ground vias shall be connected to a solid ground plane.

Figure 94:
TSL2585 Recommended Part Placement



Package Drawings & Markings

Figure 95:
TSL2585 Module Dimensions



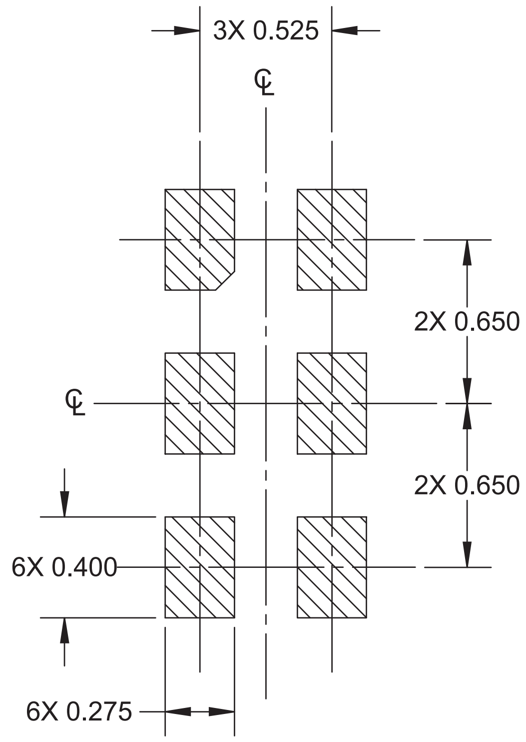
Note(s):

1. All linear dimensions are in millimeters.
2. The die is centered within the package within a tolerance of ±75 micrometers.
3. Dimension tolerances are ±0.05mm unless otherwise noted
4. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
5. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish (ENEPIG).
6. This package contains no lead (Pb).
7. This drawing is subject to change without notice.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 96:
Recommended PCB Pad Layout

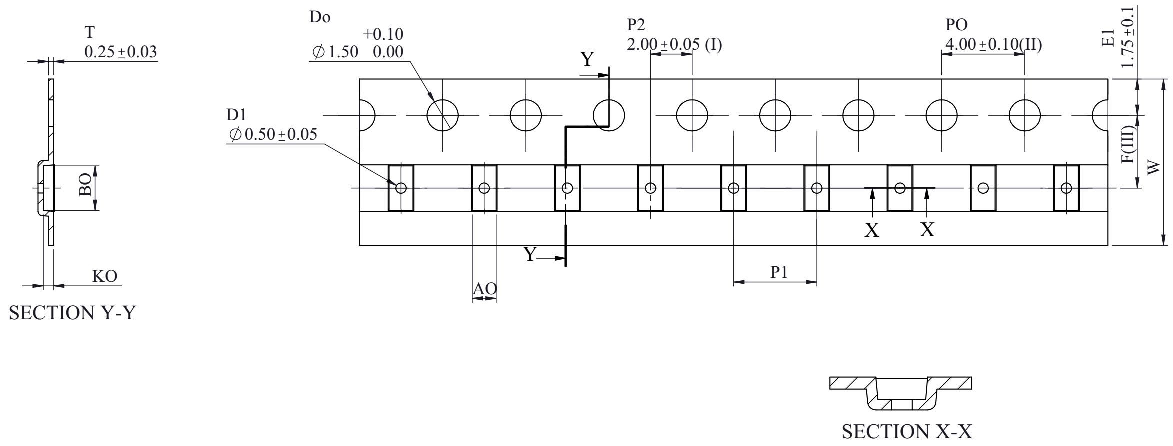


Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

Tape & Reel Information

Figure 97:
Tape and Reel Mechanical Drawing



Ao	1.15	+/- 0.05
Bo	2.15	+/- 0.05
Ko	0.50	+/- 0.05
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.00	+/- 0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481-B 2001.
4. ams OSRAM packaging tape and reel conform to the requirements of EIA Standard 481-B.
5. In accordance with EIA standard device pin 1 is located next to the sprocket holes in the tape.
6. This drawing is subject to change without notice.

Soldering & Storage Information

Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

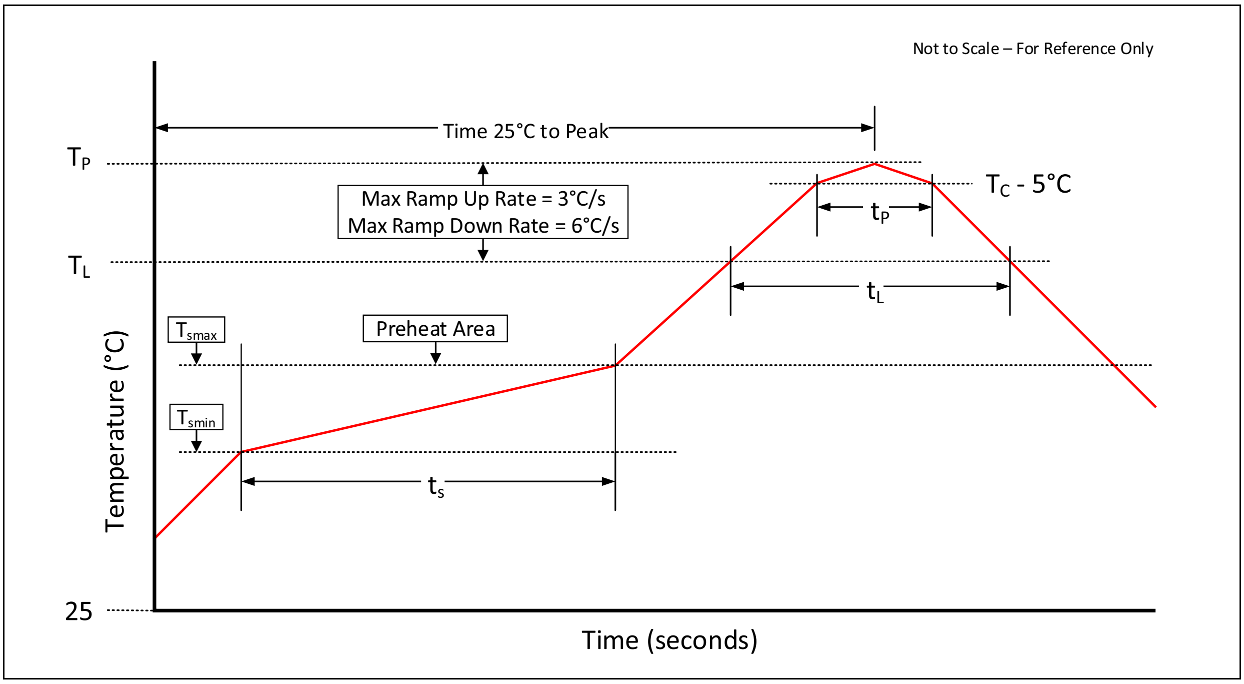
Figure 98:
Solder Reflow Profile

Profile Feature Preheat/Soak	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Temperature Min (T_{smin})	100°C	150°C
Temperature Max (T_{smax})	150°C	200°C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp of 235°C For suppliers T_P must equal or exceed the Classification temp of 235°C	For users T_P must not exceed the Classification temp of 260°C For suppliers T_P must equal or exceed the Classification temp of 260°C
Time (t_P) (1) within 5°C of the specified classification temperature (T_c)	20 (1) seconds	30 (1) seconds
Ramp-down rate (T_P to T_L)	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

Note(s):

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

Figure 99:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 24 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 100:
Ordering Information

Ordering Code	Address	Interface	Delivery Form	Delivery Quantity
TSL25853P	0x39	1.8V I^2C	Tape & Reel	10000 pcs/reel
TSL25853PM	0x39	1.8V I^2C	Tape & Reel	1000 pcs/reel

Buy our products or get free samples online at:
www.ams.com/Products

Technical Support is available at:
www.ams.com/Technical-Support

Provide feedback about this document at:
www.ams.com/Document-Feedback

For further information and requests, e-mail us at:
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ams Green (RoHS compliant and no Sb/Br/Cl): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material) and do not contain Chlorine (Cl not exceed 0.1% by weight in homogeneous material).

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 3-00 (2022-Nov-04) to current revision 4-00 (2022-Dec-22)	Page
Updated Package Drawings (no design change)	72
Updated Shelf Life	76

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide