

# Product Document

# TCS3408

## ALS/Color Sensor with Selective Flicker Detection

### General Description

The TCS3408 features ambient light and color (RGB) sensing, as well as flicker detection which suppresses cross-coupling from 940nm IR, if generated by adjacent circuits (e.g. TOF). The device comes in a low-profile and small footprint, L2.5mm x W2.0mm x H0.5mm package.

The Ambient Light and Color Sensing function provides five concurrent ambient light sensing channels: Red, Green, Blue, Clear, and Wideband. The RGB and Clear channels have a UV/IR blocking filter. This architecture accurately measures ambient light and enables the calculation of illuminance, chromaticity, and color temperature to manage display appearance.

The device integrates direct detection of 50Hz or 60Hz ambient light flicker. Flicker detection is executed in parallel with ambient light and color sensing and has independent gain configuration. The flicker detection engine can also buffer data for calculating other flicker frequencies externally.

*[Ordering Information](#) and [Content Guide](#) appear at end of datasheet.*

## Key Benefits & Features

The benefits and features of TCS3408 are listed below:

**Figure 1:**  
**Added Value of Using TCS3408**

| Benefits                                                                                                   | Features                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>Invisible ALS and color sensing under any glass type</li> </ul>     | <ul style="list-style-type: none"> <li>Configurable, high sensitivity <ul style="list-style-type: none"> <li>Programmable gain and integration time</li> <li>2048x dynamic range by gain adjustment only</li> <li>1 mlux minimum detectable illuminance (100ms)</li> </ul> </li> <li>Tailored ALS and color response <ul style="list-style-type: none"> <li>UV/IR blocking filter for RGBC channels</li> <li>Wideband reference channel without filters</li> </ul> </li> <li>ALS/color interrupt with thresholds</li> </ul> |
| <ul style="list-style-type: none"> <li>Unique fast ALS integration mode</li> </ul>                         | <ul style="list-style-type: none"> <li>Flicker-immune ALS sensing within 10ms</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <ul style="list-style-type: none"> <li>Integrated ambient light flicker detection on chip</li> </ul>       | <ul style="list-style-type: none"> <li>Independently configurable timing and gain</li> <li>Automatic gain adjustment</li> <li>50Hz and 60Hz flicker detection flags</li> <li>Flicker detected interrupt</li> </ul>                                                                                                                                                                                                                                                                                                          |
| <ul style="list-style-type: none"> <li>Low power consumption and minimum I<sup>2</sup>C traffic</li> </ul> | <ul style="list-style-type: none"> <li>1.8V<sub>DD</sub> operation</li> <li>Configurable sleep mode</li> <li>Interrupt-driven device</li> <li>On-chip self-calibration of ALS</li> </ul>                                                                                                                                                                                                                                                                                                                                    |
| <ul style="list-style-type: none"> <li>Integrated status checking for all functions</li> </ul>             | <ul style="list-style-type: none"> <li>Digital and analog ALS saturation flags</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                   |

## Applications

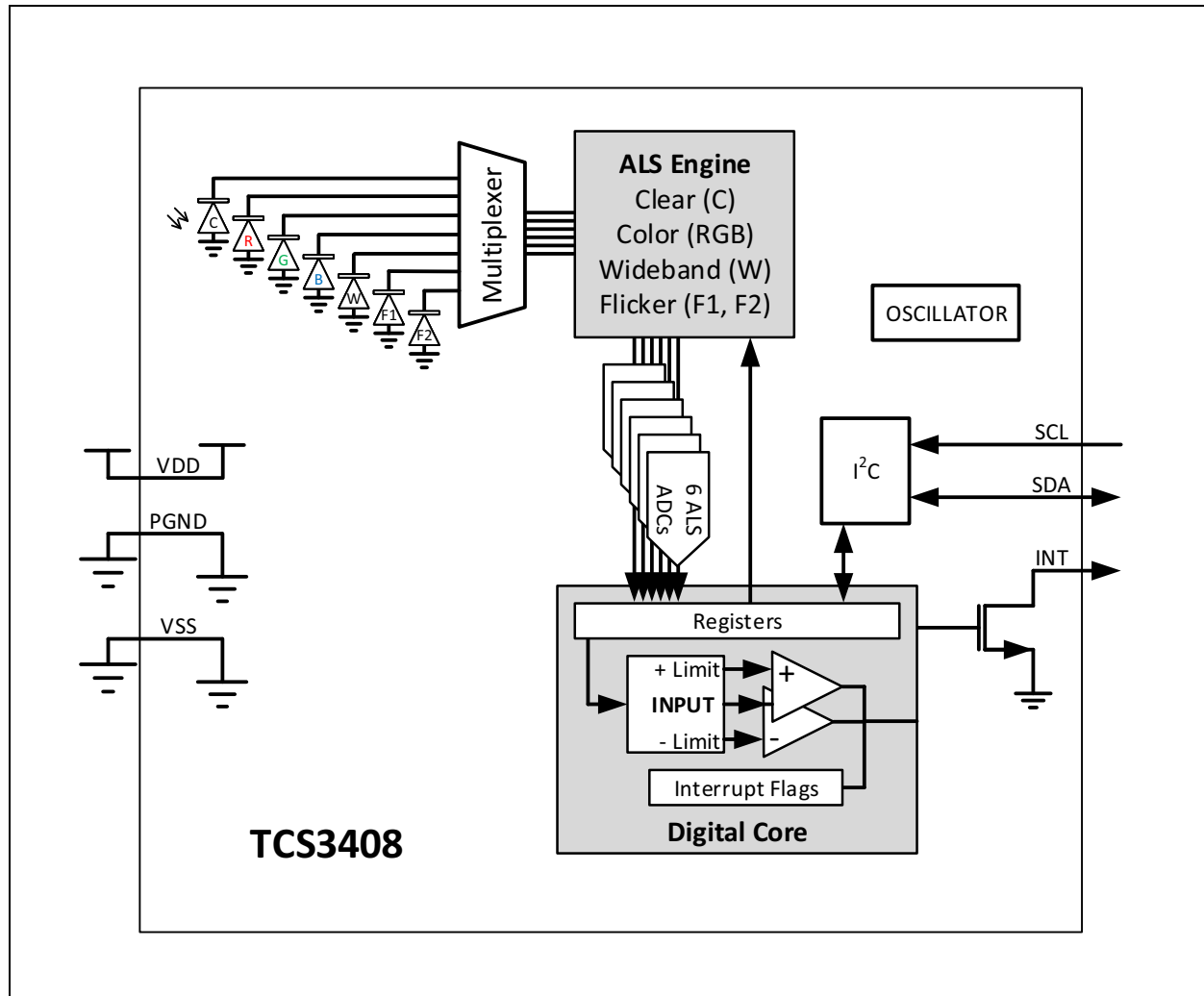
TCS3408 integrates multiple applications within one device. The applications for TCS3408 include:

- Brightness management for displays
- Color management for displays
- Camera image processing
- Flicker-immune camera operation

## Block Diagram

The functional blocks of this device are shown below:

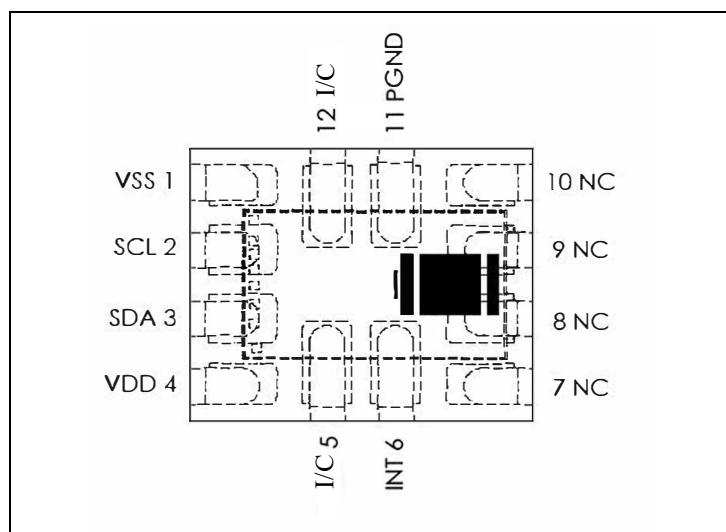
**Figure 2:**  
**Functional Blocks of TCS3408**



## Pin Assignments

Device pinout is described below.

**Figure 3:**  
**Pin Diagram of TCS3408**



**Figure 4:**  
**Pin Description of TCS3408**

| Pin Number | Pin Name | Description                                                                                        |
|------------|----------|----------------------------------------------------------------------------------------------------|
| 1          | VSS      | Ground. All voltages are referenced to VSS/PGND, and both ground pins must be connected to ground. |
| 2          | SCL      | I <sup>2</sup> C serial clock terminal                                                             |
| 3          | SDA      | I <sup>2</sup> C serial data I/O terminal                                                          |
| 4          | VDD      | Supply voltage (1.8V)                                                                              |
| 5          | I/C      | Internal connection. Connect to ground.                                                            |
| 6          | INT      | Interrupt. Open-drain output plus supports additional output options.                              |
| 7          | NC       | No connect                                                                                         |
| 8          | NC       | No connect                                                                                         |
| 9          | NC       | No connect                                                                                         |
| 10         | NC       | No connect                                                                                         |
| 11         | PGND     | Ground. All voltages are referenced to VSS/PGND, and both ground pins must be connected to ground. |
| 12         | I/C      | Internal connection. Connect to ground.                                                            |

**Note(s):**

1. NC pins do not have an internal electrical connection. For device. ESD protection, it is recommended to connect it to ground.

## Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages with respect to VSS/PGND. Device parameters are guaranteed at  $V_{DD} = 1.8\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise noted.

**Figure 5:**  
**Absolute Maximum Ratings**

| Symbol                                    | Parameter                    | Min   | Max | Units | Comments                  |
|-------------------------------------------|------------------------------|-------|-----|-------|---------------------------|
| Electrical Parameters                     |                              |       |     |       |                           |
| V <sub>DD</sub>                           | Supply voltage               | -0.3  | 2.2 | V     |                           |
| V <sub>IO</sub>                           | Digital I/O terminal voltage | -0.3  | 3.6 |       |                           |
| I <sub>IO</sub>                           | Output terminal current      | -1    | 20  | mA    |                           |
| Electrostatic Discharge                   |                              |       |     |       |                           |
| ESD <sub>HBM</sub>                        | Electrostatic discharge HBM  | ±2000 |     | V     | JEDEC/ESDA<br>JS-001-2014 |
| Temperature Ranges and Storage Conditions |                              |       |     |       |                           |
| T <sub>STRG</sub>                         | Storage temperature range    | -40   | 85  | °C    |                           |
| T <sub>A</sub>                            | Operating temperature range  | -30   | 85  |       |                           |

**Figure 6:**  
**Recommended Operating Conditions**

| Symbol                                           | Parameter                                     | Min | Typ | Max | Units            | Comments |
|--------------------------------------------------|-----------------------------------------------|-----|-----|-----|------------------|----------|
| <b>Electrical Parameters</b>                     |                                               |     |     |     |                  |          |
| $V_{DD}$                                         | Supply voltage                                | 1.7 | 1.8 | 2.0 | V                |          |
| $V_{LDR}$                                        | External LED anode supply                     |     | 3.3 |     | V                |          |
| <b>Temperature Ranges and Storage Conditions</b> |                                               |     |     |     |                  |          |
| $T_A$                                            | Operating free-air temperature <sup>(1)</sup> | -30 | 25  | 70  | $^\circ\text{C}$ |          |

**Note(s):**

1. While the device is operational across the temperature range, functionality will vary with temperature.

## Optical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Device parameters are guaranteed with  $V_{DD} = 1.8\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise noted.

**Figure 7:**  
ALS/Color Characteristics of TCS3408, ALS Gain = 128x, Integration Time = 11ms  
(unless otherwise noted)

| Parameter                                | Conditions                                                                   | Min  | Typ   | Max  | Unit                                     |
|------------------------------------------|------------------------------------------------------------------------------|------|-------|------|------------------------------------------|
| Dark ADC count value <sup>(1)</sup>      | $E_e = 0\mu\text{W}/\text{cm}^2$<br>ALS gain: 512x<br>Integration time: 98ms | 0    | 0     | 3    | counts                                   |
| ALS gain ratios <sup>(2)</sup>           | 0.5x                                                                         |      | 1/256 |      |                                          |
|                                          | 1x                                                                           |      | 1/128 |      |                                          |
|                                          | 2x                                                                           |      | 1/64  |      |                                          |
|                                          | 4x                                                                           |      | 1/32  |      |                                          |
|                                          | 8x                                                                           |      | 1/16  |      |                                          |
|                                          | 16x                                                                          |      | 1/8   |      |                                          |
|                                          | 32x                                                                          |      | 1/4   |      |                                          |
|                                          | 64x                                                                          |      | 1/2   |      |                                          |
|                                          | 256x                                                                         |      | 2.05  |      |                                          |
|                                          | 512x                                                                         |      | 4.33  |      |                                          |
|                                          | 1024x                                                                        |      | 8.38  |      |                                          |
|                                          | 2048x                                                                        |      | 17.3  |      |                                          |
| Clear channel irradiance responsivity    | White LED, 2700K <sup>(3)</sup>                                              | 56.4 | 66.3  | 76.2 | counts/<br>( $\mu\text{W}/\text{cm}^2$ ) |
| Wideband channel irradiance responsivity |                                                                              |      | 23.4  |      |                                          |
| Lux accuracy <sup>(4)</sup>              | White LED, 2700K <sup>(3)</sup>                                              | 90   | 100   | 110  | %                                        |
| ADC noise <sup>(5)</sup>                 | White LED, 2700K <sup>(3)</sup><br>Integration time: 100ms                   |      | 0.05  |      |                                          |

| Parameter                        | Conditions                                           | Min | Typ | Max | Unit |
|----------------------------------|------------------------------------------------------|-----|-----|-----|------|
| Red/Clear channel ratios         | White LED, 2700K                                     | 52  |     | 72  | %    |
|                                  | Blue LED, $\lambda_D = 465\text{nm}$ <sup>(6)</sup>  | 0   |     | 20  |      |
|                                  | Red LED, $\lambda_D = 615\text{nm}$ <sup>(7)</sup>   | 81  |     | 111 |      |
| Green/Clear channel ratios       | White LED, 2700K                                     | 21  |     | 42  | %    |
|                                  | Green LED, $\lambda_D = 525\text{nm}$ <sup>(8)</sup> | 63  |     | 86  |      |
|                                  | Red LED, $\lambda_D = 615\text{nm}$                  | 0   |     | 20  |      |
| Blue/Clear channel ratios        | White LED, 2700K                                     | 1   |     | 30  | %    |
|                                  | Blue LED, $\lambda_D = 465\text{nm}$                 | 73  |     | 100 |      |
|                                  | Red LED, $\lambda_D = 615\text{nm}$                  | 0   |     | 20  |      |
| Wideband/Clear channel ratio     | White LED, 2700K                                     | 26  |     | 44  |      |
| Wideband/Flicker_1 channel ratio | White LED, 2700K                                     | 18  |     | 25  |      |

**Note(s):**

1. The typical 3-sigma distribution shows less than 1 count for an ATIME setting of less than 98ms.
2. The gain ratios are calculated relative to the response with integration time = 27.8ms and ALS gain = 128x.
3. The White LED is an InGaN light-emitting diode with integrated phosphor and the following characteristic: correlated color temperature = 2700K.
4. Lux accuracy is an illuminance estimated using the red, green, blue, and clear channels and is not 100% production tested.
5. ADC noise is calculated as the standard deviation relative to full scale.
6. The Blue LED is an InGaN light-emitting diode with the following characteristics: dominant wavelength  $\lambda_D = 465\text{nm}$ , spectral halfwidth  $\Delta\lambda_{1/2} = 22\text{nm}$ .
7. The Red LED is an AlInGaP light-emitting diode with the following characteristics: dominant wavelength  $\lambda_D = 615\text{nm}$ , spectral halfwidth  $\Delta\lambda_{1/2} = 15\text{nm}$ .
8. The Green LED is an InGaN light-emitting diode with the following characteristics: dominant wavelength  $\lambda_D = 525\text{nm}$ , spectral halfwidth  $\Delta\lambda_{1/2} = 35\text{nm}$ .

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 8:**  
Electrical Characteristics of TCS3408,  $V_{DD} = 1.8\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| Symbol         | Parameter                         | Conditions                                     | Min  | Typ | Max  | Unit          |
|----------------|-----------------------------------|------------------------------------------------|------|-----|------|---------------|
| $I_{DD;ALS}$   | ALS supply current                | Active ALS state <sup>(1)</sup><br>(PON=AEN=1) |      | 196 | 280  | $\mu\text{A}$ |
| $I_{DD;IDLE}$  | Idle current                      | Idle state <sup>(2)</sup><br>(PON=1, AEN=0)    |      | 40  | 60   |               |
| $I_{DD;SLEEP}$ | Sleep current                     | Sleep state <sup>(3)</sup>                     |      | 0.7 | 5    |               |
| $I_{LEAK}$     | Leakage current                   | Measured on SDA, SCL, INT, GPIO                | -5   |     | 5    |               |
| $V_{OL}$       | INT, SDA, GPIO output low voltage | 6mA sink current                               |      |     | 0.4  | V             |
| $V_{IH}$       | SCL, SDA input high voltage       |                                                | 1.26 |     |      |               |
| $V_{IL}$       | SCL, SDA input low voltage        |                                                |      |     | 0.54 |               |
| $C_I$          | Input pin capacitance             |                                                |      | 10  |      | pF            |

### Note(s):

1. This parameter indicates the supply current during periods of ALS integration. The ALS gain setting will have an effect on the active supply current. The ALS gain setting used for this parameter is 128x.
2. Idle state occurs when PON=1 and all functions are disabled. This parameter is measured with LOWPOWER\_IDLE=1.
3. Sleep state occurs when PON = 0 and I<sup>2</sup>C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

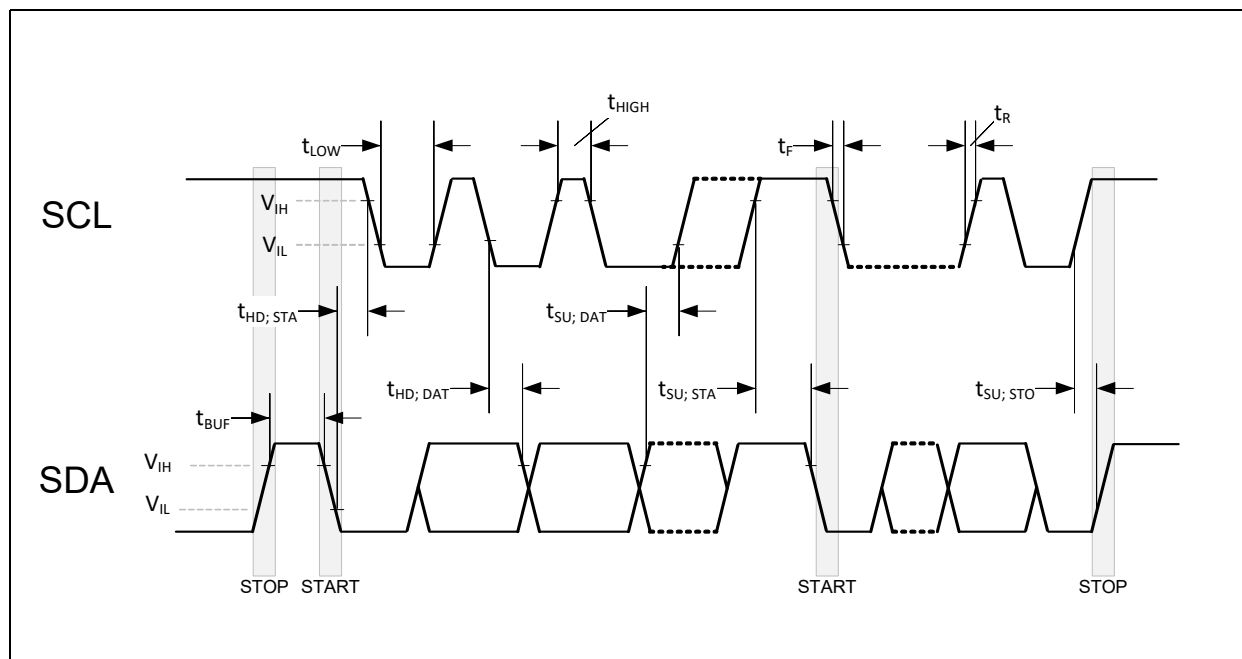
## Timing Characteristics

The timing parameters are specified by design and characterization and are not production tested unless otherwise noted. All parameters are measured with  $V_{DD} = 1.8\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise noted.

**Figure 9:**  
**I<sup>2</sup>C Timing Characteristics of TCS3408**

| Symbol       | Parameter                                                                                   | Min | Typ | Max | Unit          |
|--------------|---------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| $f_{SCL}$    | I <sup>2</sup> C clock frequency                                                            | 0   |     | 400 | kHz           |
| $t_{BUF}$    | Bus free time between start and stop condition                                              | 1.3 |     |     | $\mu\text{s}$ |
| $t_{HD;STA}$ | Hold time after (repeated) start condition. After this period, the first clock is generated | 0.6 |     |     |               |
| $t_{SU;STA}$ | Repeated start condition setup time                                                         | 0.6 |     |     |               |
| $t_{SU;STO}$ | Stop condition setup time                                                                   | 0.6 |     |     |               |
| $t_{LOW}$    | SCL clock low period                                                                        | 1.3 |     |     |               |
| $t_{HIGH}$   | SCL clock high period                                                                       | 0.6 |     |     |               |
| $t_{HD;DAT}$ | Data hold time                                                                              | 0   |     |     | ns            |
| $t_{SU;DAT}$ | Data setup time                                                                             | 100 |     |     |               |
| $t_F$        | Clock/data fall time                                                                        |     |     | 300 |               |
| $t_R$        | Clock/data rise time                                                                        |     |     | 300 |               |

**Figure 10:**  
Timing Diagram for TCS3408



**Figure 11:**  
Functional Timing Characteristics of TCS3408

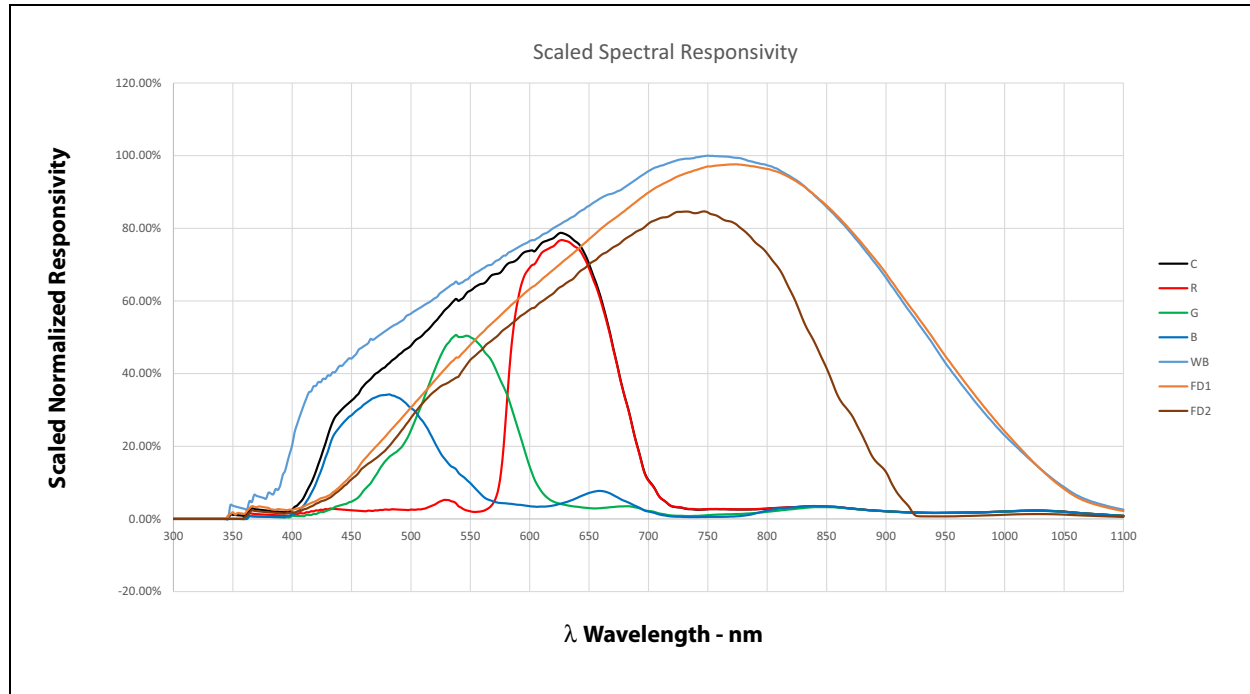
| Symbol    | Parameter                                 | Min  | Typ  | Max  | Unit    |
|-----------|-------------------------------------------|------|------|------|---------|
| $f_{OSC}$ | Oscillator clock frequency <sup>(1)</sup> | 700  | 720  | 740  | kHz     |
| $t_{OSL}$ | Oscillator clock cycle <sup>(1)</sup>     | 1.35 | 1.39 | 1.43 | $\mu s$ |

**Note(s):**

1. 100% production tested.

## Typical Operating Characteristics

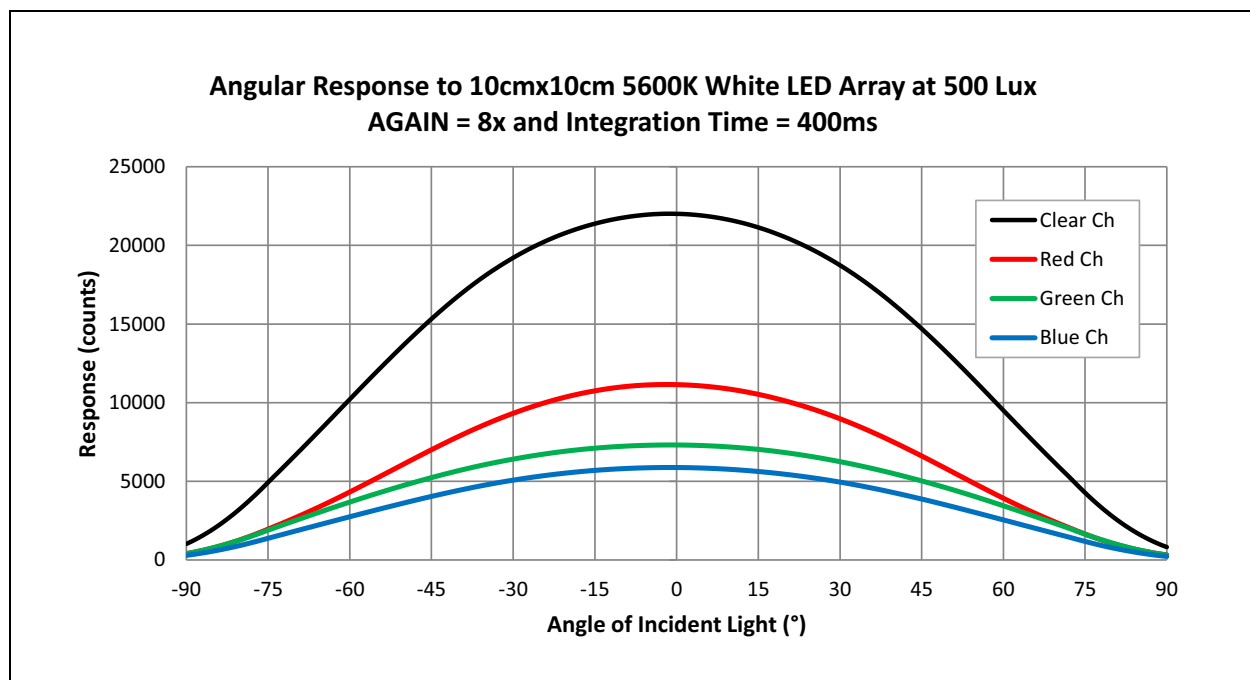
**Figure 12:**  
Spectral Responsivity



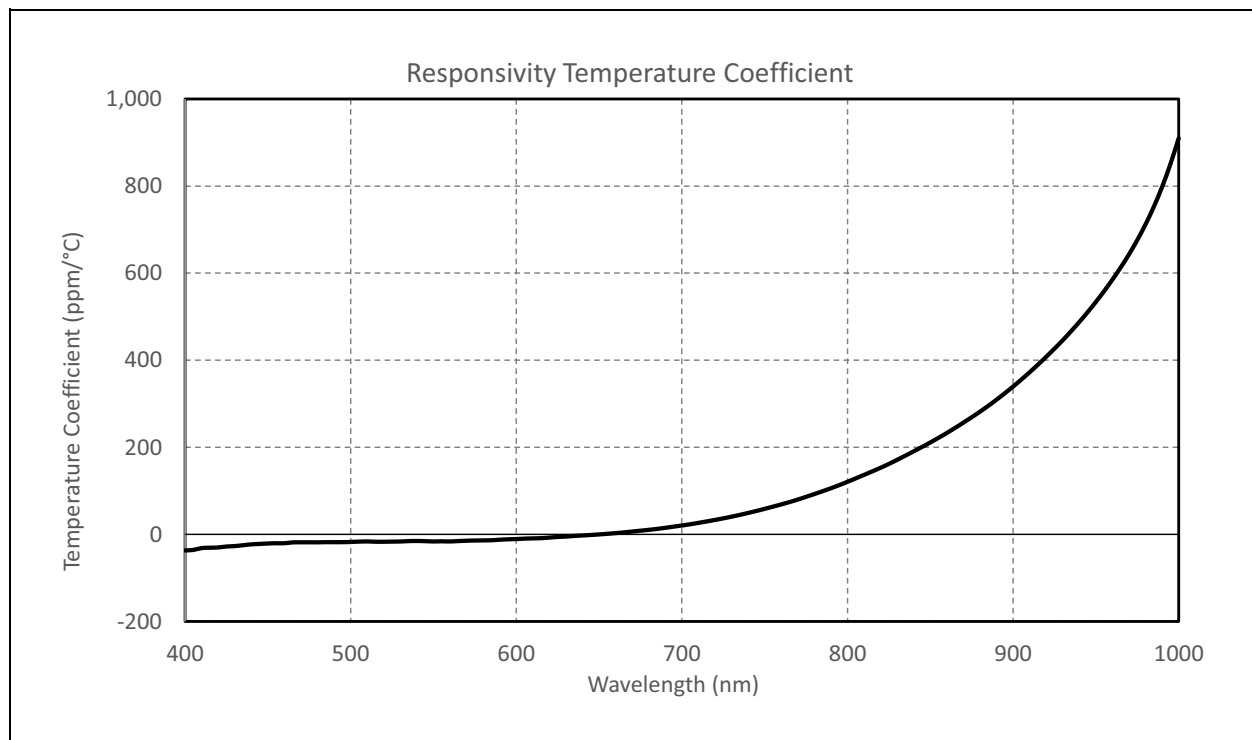
**Note(s):**

1. The spectral responsivities shown in the figure are measured under a diffuser and scaled based on the photodiode area of each channel. The scaling factors used to generate this figure are (relative to CLEAR): 3.2 for WIDEBAND, and 0.54 for FLICKER. Once scaled, the responsivities are normalized.

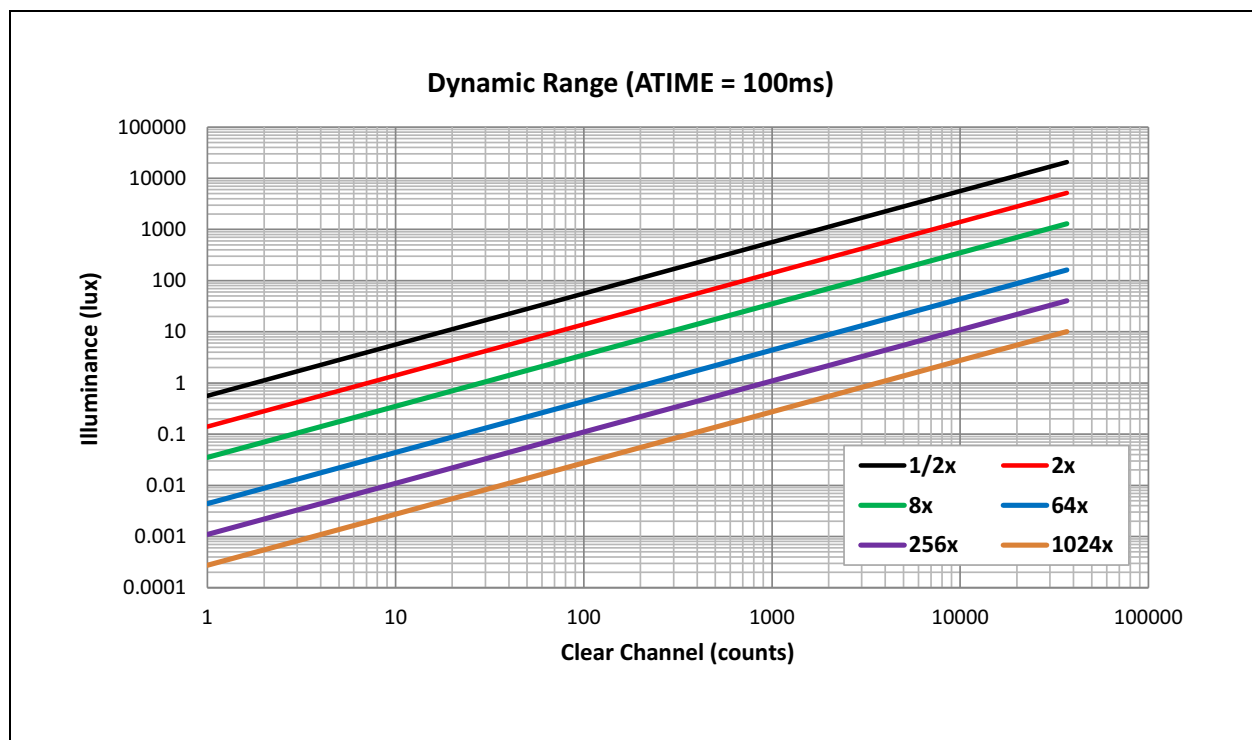
**Figure 13:**  
Normalized Angular Response



**Figure 14:**  
Responsivity Temperature Coefficient



**Figure 15:**  
Illuminance (Lux) vs. Counts (Clear Channel)



## Detailed Description

Upon power-up, POR, the device initializes. During initialization (typically 200µs), the device will deterministically send NAK on I<sup>2</sup>C and cannot accept I<sup>2</sup>C transactions. All communication with the device must be delayed, and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I<sup>2</sup>C transaction occurs during this state, the I<sup>2</sup>C core wakes up temporarily to service the communication. Once the Power ON bit, PON, is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever a function is enabled (AEN = 1) the device exits the IDLE state. If all functions are disabled (AEN = 0), the device returns to the IDLE state.

As depicted in [Figure 16](#) and [Figure 17](#), the CRGBW color sensing functions operate in parallel when enabled (CONCURRENT\_PROX\_AND\_ALS = 1). Each function is individually configured (e.g. gain, ADC integration time, wait time, persistence, thresholds, etc.).

If Sleep after Interrupt is enabled (SAI = 1 in register 0xAC), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI\_ACTIVE bit is cleared (the status bit is in register 0xA7 and the clear status bit is in register 0xFA).

## State Machine Diagrams

**Figure 16:**  
**Simplified State Diagram**

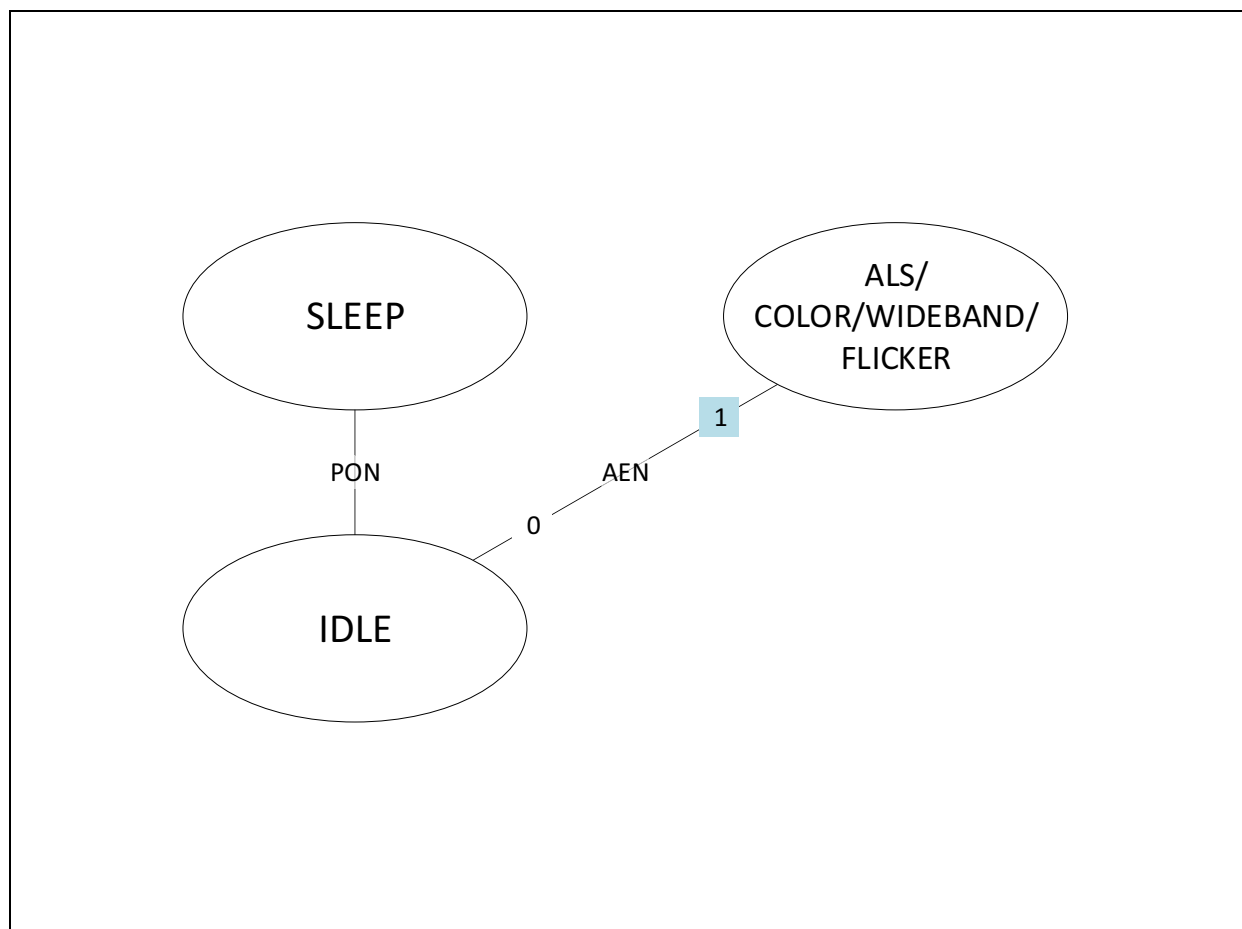
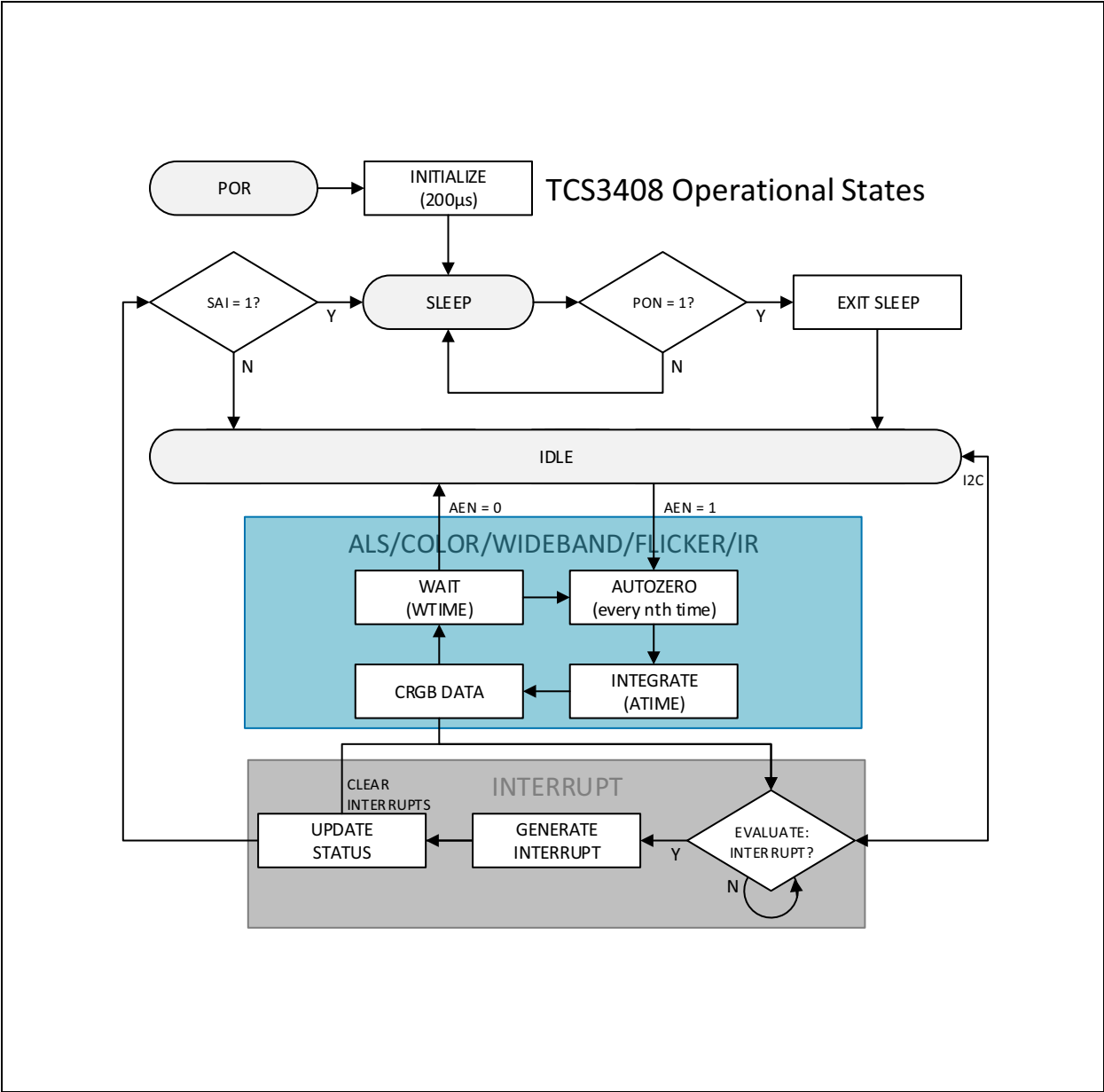


Figure 17:  
Detailed State Diagram



## I<sup>2</sup>C Protocol

The device uses I<sup>2</sup>C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). For a complete description of the I<sup>2</sup>C protocol, please review the NXP I<sup>2</sup>C design specification.

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I<sup>2</sup>C bus is released). During consecutive Read transactions, the future/repeated I<sup>2</sup>C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

All 16-bit fields have a latching scheme for reading and writing. In general it is recommended to use I<sup>2</sup>C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

## Register Overview

The device is controlled and monitored by registers accessed through the I<sup>2</sup>C serial interface. These registers provide device control functions and are read to determine device status and acquire device data.

### Register Map

The register set is summarized in [Figure 18](#). The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. The power-on reset values of each bit are indicated in these columns. Two-byte fields are always latched with the low byte followed by the high byte.

**Figure 18:**  
Register Map

| Addr | Name                    | Type | Description                  | Reset |
|------|-------------------------|------|------------------------------|-------|
| 0x80 | <a href="#">ENABLE</a>  | R/W  | Enable device states         | 0x00  |
| 0x81 | <a href="#">ATIME</a>   | R/W  | ALS integration time         | 0x00  |
| 0x83 | <a href="#">WTIME</a>   | R/W  | Wait time                    | 0x00  |
| 0x84 | <a href="#">AILT</a>    | R/W  | ALS interrupt low threshold  | 0x00  |
| 0x85 |                         |      |                              | 0x00  |
| 0x86 | <a href="#">AIHT</a>    | R/W  | ALS interrupt high threshold | 0x00  |
| 0x87 |                         |      |                              | 0x00  |
| 0x90 | <a href="#">AUXID</a>   | R    | Auxiliary identification     | 0x4A  |
| 0x91 | <a href="#">REVID</a>   | R    | Revision identification      | 0x53  |
| 0x92 | <a href="#">ID</a>      | R    | Device identification        | 0x18  |
| 0x93 | <a href="#">STATUS</a>  | R/W  | Device status one            | 0x00  |
| 0x94 | <a href="#">ASTATUS</a> | R    | ALS status                   | 0x00  |
| 0x95 | <a href="#">ADATA0</a>  | R    | ALS channel zero data        | 0x00  |
| 0x96 |                         |      |                              | 0x00  |
| 0x97 | <a href="#">ADATA1</a>  | R    | ALS channel one data         | 0x00  |
| 0x98 |                         |      |                              | 0x00  |
| 0x99 | <a href="#">ADATA2</a>  | R    | ALS channel two data         | 0x00  |
| 0x9A |                         |      |                              | 0x00  |
| 0x9B | <a href="#">ADATA3</a>  | R    | ALS channel three data       | 0x00  |
| 0x9C |                         |      |                              | 0x00  |

| Addr | Name         | Type | Description                          | Reset |
|------|--------------|------|--------------------------------------|-------|
| 0x9D | ADATA4       | R    | ALS channel four data                | 0x00  |
| 0x9E |              |      |                                      | 0x00  |
| 0x9F | ADATA5       | R    | ALS channel five data                | 0x00  |
| 0xA0 |              |      |                                      | 0x00  |
| 0xA3 | STATUS2      | R/W  | Device status two                    | 0x00  |
| 0xA4 | STATUS3      | R/W  | Device status three                  | 0x08  |
| 0xA6 | STATUS5      | R/W  | Device status five                   | 0x00  |
| 0xA7 | STATUS6      | R/W  | Device status six                    | 0x00  |
| 0xA9 | CFG0         | R/W  | Configuration zero                   | 0x00  |
| 0xAA | CFG1         | R/W  | Configuration one                    | 0x09  |
| 0xAC | CFG3         | R/W  | Configuration three                  | 0x0C  |
| 0xAD | CFG4         | R/W  | Configuration four                   | 0x00  |
| 0xAF | CFG6         | R/W  | Configuration six                    | 0x00  |
| 0xB1 | CFG8         | R/W  | Configuration eight                  | 0x80  |
| 0xB2 | CFG9         | R/W  | Configuration nine                   | 0x00  |
| 0xB3 | CFG10        | R/W  | Configuration ten                    | 0xF2  |
| 0xB4 | CFG11        | R/W  | Configuration eleven                 | 0x40  |
| 0xB5 | CFG12        | R/W  | Configuration twelve                 | 0x00  |
| 0xBD | PERS         | R/W  | Persistence configuration            | 0x00  |
| 0xCA | ASTEP        | R/W  | ALS integration step size            | 0xE7  |
| 0xCB |              |      |                                      | 0x03  |
| 0xCF | AGC_GAIN_MAX | R/W  | Maximum AGC gains                    | 0x99  |
| 0xD6 | AZ_CONFIG    | R/W  | Autozero configuration               | 0xFF  |
| 0xDB | FD_STATUS    | R    | Flicker detection configuration zero | 0x00  |
| 0xF9 | INTENAB      | R/W  | Enable interrupts                    | 0x00  |
| 0xFA | CONTROL      | R/W  | Control                              | 0x00  |

## Register Descriptions

### Power, Enable, and Operation

The enable register has fields that power on the device and enable the functions. To operate the device, first set all configuration fields for all functions, then set PON = 1, and finally enable functions. Changing configuration register values while functions are operating may result in invalid results. PEN, and AEN require PON to be asserted for each respective function to operate correctly. When PEN, or AEN are asserted, the visible bit is only updated when the state machine has completed the process of enabling the associated function.

**Figure 19:**  
**ENABLE**

| Addr: 0x80 |          | ENABLE |      |                                                                                                                                                                                                                                                                |
|------------|----------|--------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field    | Reset  | Type | Bit Description                                                                                                                                                                                                                                                |
| 7          | Reserved | 0      |      |                                                                                                                                                                                                                                                                |
| 6          | FDEN     | 0      | R/W  | <b>Flicker Detection Enable.</b> Writing a 1 activates flicker detection. Writing a 0 disables flicker detection.                                                                                                                                              |
| 5:4        | Reserved | 0      |      |                                                                                                                                                                                                                                                                |
| 3          | WEN      | 0      | R/W  | <b>Wait Enable.</b> Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.                                                                                                                                                                 |
| 2          | Reserved | 0      |      |                                                                                                                                                                                                                                                                |
| 1          | AEN      | 0      | R/W  | <b>ALS Enable.</b> Writing a 1 enables ALS/Color. Writing a 0 disables ALS/Color.                                                                                                                                                                              |
| 0          | PON      | 0      | R/W  | <b>Power ON.</b> When asserted, the internal oscillator is activated, allowing timers and ADC channels to operate. Writing a 0 disables the oscillator and clears PEN, and AEN. Only set this bit after all other registers have been initialized by the host. |

**Note(s):**

1. Return to the Register Map ([0x80](#)).

**Figure 20:**  
**INTENAB**

| Addr: 0xF9 |          | INTENAB |      |                                                                                                                                               |
|------------|----------|---------|------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field    | Reset   | Type | Bit Description                                                                                                                               |
| 7          | ASIEN    | 0       | R/W  | <b>ALS and Flicker Detect Saturation Interrupt Enable.</b> When asserted permits ALS saturation interrupts to be generated.                   |
| 6:4        | Reserved | 0       |      |                                                                                                                                               |
| 3          | AIEN     | 0       | R/W  | <b>ALS Interrupt Enable.</b> When asserted permits ALS interrupts to be generated, subject to the ALS thresholds and persistence filter.      |
| 2          | Reserved | 0       |      |                                                                                                                                               |
| 1          | Reserved | 0       |      |                                                                                                                                               |
| 0          | SIEN     | 0       | R/W  | <b>System Interrupt Enable.</b> When asserted permits system interrupts to be generated. Indicates that flicker detection status has changed. |

**Note(s):**

1. Return to the Register Map ([0xF9](#)).

**Figure 21:**  
**CONTROL**

| Addr: 0xFA |                  | CONTROL |      |                                                                                                                                        |
|------------|------------------|---------|------|----------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field            | Reset   | Type | Bit Description                                                                                                                        |
| 7:3        | Reserved         | 0       |      |                                                                                                                                        |
| 2          | ALS_MANUAL_AZ    | 0       | R/W  | <b>ALS Manual Autozero.</b> Starts a manual autozero of the ALS engines. Set AEN = 0 before starting a manual autozero for it to work. |
| 1          | Reserved         | 0       |      |                                                                                                                                        |
| 0          | CLEAR_SAI_ACTIVE | 0       | R/W  | <b>Clear Sleep-After-Interrupt Active.</b> Clears SAI_ACTIVE, ends sleep, and restarts device operation.                               |

**Note(s):**

1. Return to the Register Map ([0xFA](#)).

### Identification

The identification registers provide auxiliary identification for special cases, wafer revision data, and device identification. All identification registers are read only.

**Figure 22:**  
**Identification Registers**

| Bits | Addr | Field | Description                     |
|------|------|-------|---------------------------------|
| 7:0  | 0x90 | AUXID | Auxiliary Identification (0x4A) |
| 7:0  | 0x91 | REVID | Revision Identification (0x53)  |
| 7:0  | 0x92 | ID    | Device Identification (0x18)    |

**Note(s):**

1. Return to the Register Map ([0x90](#), [0x91](#), [0x92](#)).

### ALS Configuration

The ALS/color integration time is set using the ATIME field and ASTEP field (ASTEP register). The ALS integration time, in milliseconds, is equal to  $(\text{ATIME} + 1) \times (\text{ASTEP} + 1) / 360$ . The reset value for ASTEP is 999 (2.78ms), and the recommended configuration for these two fields is  $\text{ASTEP} = 599$  and  $\text{ATIME} = 29$ , which results in an integration time of 50ms. The ALS integration time also establishes the full scale ADC range, which is equal to  $(\text{ATIME} + 1) \times (\text{ASTEP} + 1)$ .

If wait is enabled ( $\text{WEN} = 1$ ), each new ALS sample is started based on WTIME. It is necessary for WTIME to be sufficiently large for ALS integration and any other functions to be completed within the time frame. The device will warn the user if the timing is configured incorrectly. If WTIME is too short, then ALS\_TRIGGER\_ERROR will be 1.

**Figure 23:**  
ATIME

| Addr: 0x81 |       | ATIME |      |                                                                                            |
|------------|-------|-------|------|--------------------------------------------------------------------------------------------|
| Bit        | Field | Reset | Type | Description                                                                                |
| 7:0        | ATIME | 0x00  | R/W  | <b>ALS Integration Time.</b> Sets the number of ALS/color integration steps from 1 to 256. |
|            |       |       |      | <b>VALUE</b> <b>INTEGRATION TIME</b>                                                       |
|            |       |       |      | 0      ASTEP                                                                               |
|            |       |       |      | n $\text{ASTEP} \times (n+1)$                                                              |
|            |       |       |      | 255 $256 \times \text{ASTEP}$                                                              |

**Note(s):**

- Return to the Register Map (0x81).

**Figure 24:**  
**ASTEP**

| Addr: 0x82 |       | ASTEP |                                                                                                                                                  |                |
|------------|-------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| Bits       | Field | Reset | Description                                                                                                                                      |                |
| 7:0        | ASTEP | 0xE7  | <b>ALS Integration Time Step Size.</b> Sets the integration time per step in increments of 2.78μs. The default value is 999. Type is read/write. |                |
| 15:8       |       | 0x03  | VALUE                                                                                                                                            | STEP SIZE      |
|            |       |       | 0                                                                                                                                                | 2.78μs         |
|            |       |       | n                                                                                                                                                | 2.78μs × (n+1) |
|            |       |       | 599                                                                                                                                              | 1.67ms         |
|            |       |       | 999                                                                                                                                              | 2.78ms         |
|            |       |       | 17999                                                                                                                                            | 50ms           |
|            |       |       | 65535                                                                                                                                            | 182ms          |

**Note(s):**

- Return to the Register Map ([0xCA](#), [0xCB](#)).

**Figure 25:**  
**WTIME**

| Addr: 0x83 |       | WTIME |      |                                                                   |                               |
|------------|-------|-------|------|-------------------------------------------------------------------|-------------------------------|
| Bit        | Field | Reset | Type | Description                                                       |                               |
| 7:0        | WTIME | 0x00  | R/W  | <b>Wait Time.</b> Sets the sample rate of the ALS/color function. |                               |
|            |       |       |      | <b>VALUE</b>                                                      | <b>TIME</b>                   |
|            |       |       |      | 0                                                                 | 2.844ms                       |
|            |       |       |      | n                                                                 | $2.844\text{ms} \times (n+1)$ |
|            |       |       |      | 255                                                               | 728ms                         |

**Note(s):**

- Return to the Register Map ([0x83](#)).

ALS level detection uses data generated by the ADC Channel X. The channel can be selected via ALS\_TH\_CHANNEL (see [CFG12](#)). The ALS Interrupt Threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit ADATA values. If AIEN is enabled and ADATA is not between AILT and AIHT for the number of consecutive samples specified in APERS an interrupt is asserted on the interrupt pin. These registers are read/write.

**Figure 26:**  
**ALS Interrupt Thresholds**

| Bits | Addr | Field | Description                  |
|------|------|-------|------------------------------|
| 7:0  | 0x84 | AILT  | ALS Interrupt Low Threshold  |
| 15:8 | 0x85 |       |                              |
| 7:0  | 0x86 | AIHT  | ALS Interrupt High Threshold |
| 15:8 | 0x87 |       |                              |

**Note(s):**

1. Return to the Register Map ([0x84](#), [0x85](#), [0x86](#), [0x87](#)).

**Figure 27:**  
**CFG1**

| Addr: 0xAA |          | CFG1  |      |                                            |             |
|------------|----------|-------|------|--------------------------------------------|-------------|
| Bit        | Field    | Reset | Type | Bit Description                            |             |
| 7:5        | Reserved | 0     |      |                                            |             |
| 4:0        | AGAIN    | 9     | R/W  | <b>ALS Gain.</b> Sets the ALS sensitivity. |             |
|            |          |       |      | <b>VALUE</b>                               | <b>GAIN</b> |
|            |          |       |      | 0                                          | 0.5x        |
|            |          |       |      | 1                                          | 1x          |
|            |          |       |      | 2                                          | 2x          |
|            |          |       |      | 3                                          | 4x          |
|            |          |       |      | 4                                          | 8x          |
|            |          |       |      | 5                                          | 16x         |
|            |          |       |      | 6                                          | 32x         |
|            |          |       |      | 7                                          | 64x         |
|            |          |       |      | 8                                          | 128x        |
|            |          |       |      | 9                                          | 256x        |
|            |          |       |      | 10                                         | 512x        |
|            |          |       |      | 11                                         | 1024x       |
|            |          |       |      | 12                                         | 2048x       |

**Note(s):**

1. Return to the Register Map ([0xAA](#)).

**Figure 28:**  
**CFG10**

| Addr: 0xB3 |                   | CFG10 |      |                                                                                                                                                                                                                                                                                                    |
|------------|-------------------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field             | Reset | Type | Bit Description                                                                                                                                                                                                                                                                                    |
| 7:6        | ALS_AGC_HIGH_HYST | 3     | R/W  | <b>ALS AGC High Hysteresis.</b> Sets the ALS data threshold at which AGAIN is reduced when ALS AGC mode is enabled. The threshold is automatically calculated internally as a percentage of full-scale. Note that full-scale is equal to $(ATIME + 1) \times (ASTEP + 1)$ .                        |
|            |                   |       |      | <b>VALUE</b> <b>SIGNAL</b>                                                                                                                                                                                                                                                                         |
|            |                   |       |      | 0      50%                                                                                                                                                                                                                                                                                         |
|            |                   |       |      | 1      62.5%                                                                                                                                                                                                                                                                                       |
|            |                   |       |      | 2      75%                                                                                                                                                                                                                                                                                         |
|            |                   |       |      | 3      87.5%                                                                                                                                                                                                                                                                                       |
| 5:4        | ALS_AGC_LOW_HYST  | 3     | R/W  | <b>ALS AGC Low Hysteresis.</b> Sets the ALS data threshold at which AGAIN is increased when ALS AGC mode is enabled. The threshold is automatically calculated internally as a percentage of full-scale. Note that full-scale is equal to $(ATIME + 1) \times (ASTEP + 1)$ .                       |
|            |                   |       |      | <b>VALUE</b> <b>SIGNAL</b>                                                                                                                                                                                                                                                                         |
|            |                   |       |      | 0      12.5%                                                                                                                                                                                                                                                                                       |
|            |                   |       |      | 1      25%                                                                                                                                                                                                                                                                                         |
|            |                   |       |      | 2      37.5%                                                                                                                                                                                                                                                                                       |
|            |                   |       |      | 3      50%                                                                                                                                                                                                                                                                                         |
| 3          | Reserved          | 0     |      |                                                                                                                                                                                                                                                                                                    |
| 2:0        | FD_PERS           | 2     | R/W  | <b>Flicker Detect Persistence.</b> Sets the number of consecutive flicker detect results that must be different before the flicker detect status will be changed. Flicker detection interrupts on SINT are affected by this setting. Flicker detect persistence is equal to $2^{(FD\_PERS - 1)}$ . |

**Note(s):**

1. Return to the Register Map ([0xB3](#)).

**Figure 29:**  
**CFG12**

| Addr: 0xB5 |                | CFG12 |      |                                                                                                                                                                 |                |                |
|------------|----------------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------------|
| Bit        | Field          | Reset | Type | Bit Description                                                                                                                                                 |                |                |
| 7:3        | Reserved       | 0     |      |                                                                                                                                                                 |                |                |
| 2:0        | ALS_TH_CHANNEL | 0     | R/W  | <b>ALS Thresholds Channel.</b> Sets the channel used by interrupts, persistence, and the ALS AGC, if enabled, to determine device status and ALS gain settings. |                |                |
|            |                |       |      | <b>VALUE</b>                                                                                                                                                    | <b>CHANNEL</b> | <b>DEFAULT</b> |
|            |                |       |      | 0                                                                                                                                                               | 0              | CLEAR          |
|            |                |       |      | 1                                                                                                                                                               | 1              | RED            |
|            |                |       |      | 2                                                                                                                                                               | 2              | GREEN          |
|            |                |       |      | 3                                                                                                                                                               | 3              | BLUE           |
|            |                |       |      | 4                                                                                                                                                               | 4              | WIDEBAND       |

**Note(s):**

1. Return to the Register Map ([0xB5](#)).

ALS autozero configuration is used to set how often the ALS engine offsets are reset to compensate for changes in device temperature.

**Figure 30:**  
**AZ\_CONFIG**

| Addr: 0xD6 |                  | AZ_CONFIG |      |                                                                                                                   |
|------------|------------------|-----------|------|-------------------------------------------------------------------------------------------------------------------|
| Bit        | Field            | Reset     | Type | Bit Description                                                                                                   |
| 7:0        | AZ_NTH_ITERATION | 255       | R/W  | <b>ALS Autozero Frequency.</b> Sets the frequency at which the device performs autozero of the ALS pulse counter. |
|            |                  |           |      | <b>VALUE</b> <b>AUTOZERO FREQUENCY</b>                                                                            |
|            |                  |           |      | 0      Never                                                                                                      |
|            |                  |           |      | 1      Every cycle                                                                                                |
|            |                  |           |      | 2      Every 2 cycles                                                                                             |
|            |                  |           |      | ...      Every (AZ_NTH_ITERATION) cycles                                                                          |
|            |                  |           |      | 253      Every 253 cycles                                                                                         |
|            |                  |           |      | 254      Every 254 cycles                                                                                         |
|            |                  |           |      | 255      Only once (before 1 <sup>st</sup> cycle)                                                                 |

**Note(s):**

1. Return to the Register Map ([0xD6](#)).

**Figure 31:**  
**AGC\_GAIN\_MAX**

| Addr: 0xCF |                 | AGC_GAIN_MAX |      |                                                                                                                                                                                                     |
|------------|-----------------|--------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field           | Reset        | Type | Bit Description                                                                                                                                                                                     |
| 7:4        | AGC_FD_GAIN_MAX | 9            | R/W  | <b>Flicker Detection AGC Gain Max.</b> Sets the maximum gain for flicker detection to $2^{(AGC\_FD\_GAIN\_MAX - 1)}$ . Reset value is 9 (256x). This field has a range from 0 (0.5x) to 11 (1024x). |
| 3:0        | AGC_AGAIN_MAX   | 9            | R/W  | <b>ALS AGC Gain Max.</b> Sets the maximum gain for the ALS AGC engine to $2^{(AGC\_AGAIN\_MAX - 1)}$ . Reset value is 9 (256x). This field has a range from 0 (0.5x) to 11 (1024x).                 |

**Note(s):**

1. Return to the Register Map ([0xCF](#)).

### General Configuration

The configuration registers include fields used to control device operation for all functions.

**Figure 32:**  
**CFG0**

| Addr: 0xA9 |                  | CFG0  |      |                                                                                                                                                    |
|------------|------------------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field            | Reset | Type | Bit Description                                                                                                                                    |
| 7:6        | Reserved         | 0     |      |                                                                                                                                                    |
| 5          | LOWPOWER_IDLE    | 0     | R/W  | <b>Low Power Idle.</b> When asserted, the device will automatically run in a low power mode whenever all functions are in wait states or disabled. |
| 4:3        | Reserved         | 0     |      |                                                                                                                                                    |
| 2          | ALS_TRIGGER_LONG | 0     | R/W  | <b>ALS Trigger Long.</b> Increases the WTIME setting by a factor of 16.                                                                            |
| 1:0        | RAM_BANK         | 0     | R/W  | <b>RAM Bank Selection.</b> Specifies the RAM bank to access in registers 0x00 to 0x7F.                                                             |
|            |                  |       |      | <b>VALUE</b> <b>BANK</b>                                                                                                                           |
|            |                  |       |      | 0              0                                                                                                                                   |
|            |                  |       |      | 1              1                                                                                                                                   |
|            |                  |       |      | 2 or 3      Other <sup>(1)</sup>                                                                                                                   |

**Note(s):**

1. Set RAM\_BANK = 2 or 3 to access the 16 words at 0xB0 ... 0xBF. These words are the time table for remote control and are mirrored over the entire 0x00 to 0x7F range.
2. Return to the Register Map ([0xA9](#)).

**Figure 33:**  
**CFG3**

| Addr: 0xAC |          | CFG3  |      |                                                                                                                                                                                                                                                |
|------------|----------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field    | Reset | Type | Bit Description                                                                                                                                                                                                                                |
| 7:5        | Reserved | 0     |      |                                                                                                                                                                                                                                                |
| 4          | SAI      | 0     | R/W  | <b>Sleep After Interrupt.</b> If asserted, the oscillator is turned off whenever interrupt is active (low). SAI_ACTIVE is set in this event. To activate the oscillator again, service and clear all interrupts plus clear the SAI_ACTIVE bit. |
| 3:0        | Reserved | 12    |      |                                                                                                                                                                                                                                                |

**Note(s):**

1. Return to the Register Map ([0xAC](#)).

**Figure 34:**  
**CFG4**

| Addr: 0xAD |            | CFG4  |      |                                                                                         |                   |
|------------|------------|-------|------|-----------------------------------------------------------------------------------------|-------------------|
| Bit        | Field      | Reset | Type | Bit Description                                                                         |                   |
| 7          | Reserved   | 0     |      |                                                                                         |                   |
| 6:4        | INT_PINMAP | 0     | R/W  | <b>Interrupt Pin Map.</b> Selects the signal to output on the INT pin.                  |                   |
|            |            |       |      | <b>VALUE</b>                                                                            | <b>SIGNAL</b>     |
|            |            |       |      | 0                                                                                       | Normal interrupts |
|            |            |       |      | 1                                                                                       | RESERVED          |
|            |            |       |      | 2                                                                                       | AIN1              |
|            |            |       |      | 3                                                                                       | PINT0             |
|            |            |       |      | 4                                                                                       | PINT1             |
| 3          | INT_INVERT | 0     | R/W  | <b>Interrupt Invert.</b> If asserted, the interrupt signal is inverted (active = high). |                   |
| 2:0        | Reserved   | 0     |      |                                                                                         |                   |

**Note(s):**

1. Return to the Register Map ([0xAD](#)).

**Figure 35:**  
**CFG6**

| Addr: 0xAF |                        | CFG6  |      |                                                                                                                                                                                                                                                                                                                               |
|------------|------------------------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field                  | Reset | Type | Bit Description                                                                                                                                                                                                                                                                                                               |
| 7          | Reserved               | 0     |      |                                                                                                                                                                                                                                                                                                                               |
| 6          | ALS_AGC_MAX_GAIN_START | 0     | R/W  | Enables the same AGC behavior for ALS as used during flicker detection for finding the highest reasonable again setting. The AGC will start with agc_again_max as the again value. The again setting is reduced to the next lower setting until the output does not result in asat_analog or until again=0 (0.5x) is reached. |
| 5:0        | Reserved               | 0     |      |                                                                                                                                                                                                                                                                                                                               |

**Note(s):**

1. Return to the Register Map ([0xAF](#)).

**Figure 36:**  
**CFG8**

| Addr: 0xB1 |                | CFG8  |      |                                                                                                                                              |
|------------|----------------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field          | Reset | Type | Bit Description                                                                                                                              |
| 7:6        | Reserved       | 2     |      |                                                                                                                                              |
| 5:3        | Reserved       | 0     |      |                                                                                                                                              |
| 2          | ALS_AGC_ENABLE | 0     | R/W  | <b>ALS AGC Enable.</b> If asserted, device uses automatic gain control for the ALS engines to maximize ALS signal while avoiding saturation. |
| 1:0        | Reserved       | 0     |      |                                                                                                                                              |

**Note(s):**

1. Return to the Register Map ([0xB1](#)).

**Figure 37:**  
**CFG9**

| Addr: 0xB2 |          | CFG9  |      |                                                                                                                        |
|------------|----------|-------|------|------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field    | Reset | Type | Bit Description                                                                                                        |
| 7          | Reserved | 0     |      |                                                                                                                        |
| 6          | SIEN_FD  | 0     | R/W  | <b>System Interrupt Flicker Detection.</b> Enables system interrupt when flicker detection status change has occurred. |

| Addr: 0xB2 |          | CFG9  |      |                 |
|------------|----------|-------|------|-----------------|
| Bit        | Field    | Reset | Type | Bit Description |
| 5:0        | Reserved | 0     |      |                 |

**Note(s):**

1. Return to the Register Map ([0xB2](#)).

**Figure 38:**  
**CFG11**

| Addr: 0xB4 |             | CFG11 |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------------|-------------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field       | Reset | Type | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 7          | AINT_DIRECT | 0     | R/W  | <b>ALS Interrupt Direct.</b> Enables the direct mode of ALS interrupt. Interrupts (aint) are only generated when adataX (selected by als_th_channel) moves over the hysteresis edges (aint_ailt and aint_aiht). If "0", interrupts are always generated if adataX is above aiht or below ailt. The status of the ALS interrupt is directly output on the INT or GPIO pin if this mode is enabled and either of those pins are configured to do so according to the INT_PINMAP and GPIO_PINMAP settings. |
| 6:0        | Reserved    | 64    |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

**Note(s):**

1. Return to the Register Map ([0xB4](#)).

Persistence filters limit the rate of interrupts generated for proximity and ALS/color data.

**Figure 39:**  
**PERS**

| Addr: 0xBD |          | PERS  |      |                                                                                                                                                                                                                                                                                                                                                                        |                                                    |
|------------|----------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|
| Bit        | Field    | Reset | Type | Bit Description                                                                                                                                                                                                                                                                                                                                                        |                                                    |
| 7:4        | Reserved | 0     |      |                                                                                                                                                                                                                                                                                                                                                                        |                                                    |
| 3:0        | APERS    | 0     | R/W  | <b>ALS Interrupt Persistence.</b> Defines a filter for the number of consecutive occurrences that ALS/color data must remain outside the threshold range between AILT and AIHT before an interrupt is generated. The ALS data channel used for the persistence filter is set by ALS_TH_CHANNEL. Any sample that is inside the threshold range resets the counter to 0. |                                                    |
|            |          |       |      | <b>VALUE</b>                                                                                                                                                                                                                                                                                                                                                           | <b>CONSECUTIVE ADATA OUT OF RANGE TO INTERRUPT</b> |
|            |          |       |      | 0                                                                                                                                                                                                                                                                                                                                                                      | Every ALS cycle generates an interrupt.            |
|            |          |       |      | 1                                                                                                                                                                                                                                                                                                                                                                      | 1                                                  |
|            |          |       |      | 2                                                                                                                                                                                                                                                                                                                                                                      | 2                                                  |
|            |          |       |      | 3                                                                                                                                                                                                                                                                                                                                                                      | 3                                                  |
|            |          |       |      | 4                                                                                                                                                                                                                                                                                                                                                                      | 5                                                  |
|            |          |       |      | 5                                                                                                                                                                                                                                                                                                                                                                      | 10                                                 |
|            |          |       |      | ...                                                                                                                                                                                                                                                                                                                                                                    | $5 \times (\text{APERS} - 3)$                      |
|            |          |       |      | 14                                                                                                                                                                                                                                                                                                                                                                     | 55                                                 |
|            |          |       |      | 15                                                                                                                                                                                                                                                                                                                                                                     | 60                                                 |

**Note(s):**

1. Return to the Register Map ([0xBD](#)).

### Status Registers

The primary status register for TCS3408 indicates if there are saturation or interrupt events that need to be handled by the user. This register is self-clearing, meaning that writing a 1 to any bit in the register clears that status bit. In this way, the user should read the STATUS register, handle all indicated event(s), then write the register value back to STATUS to clear the handled events. Writing 0 to these bits will not clear those bits if they have a value of 1, which means that new events that occurred since the last read of the STATUS register will not be accidentally cleared.

**Figure 40:**  
**STATUS**

| Addr: 0x93 |          | STATUS |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------|----------|--------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field    | Reset  | Type | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7          | ASAT     | 0      | R    | <b>ALS and Flicker Detect Saturation.</b> If ASIEN is set, indicates ALS saturation. Check the STATUS2 register to differentiate between analog or digital saturation.                                                                                                                                                                                                                                                                          |
| 6:4        | Reserved | 0      | R    |                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 3          | AINT     | 0      | R    | <b>ALS Interrupt.</b> If AIEN is set, indicates that an ALS event that met the programmed ALS thresholds (AILT or AIHT) and persistence (APERS) occurred.                                                                                                                                                                                                                                                                                       |
| 2          | Reserved | 0      |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1          | CINT     | 0      | R    | <b>Calibration Interrupt.</b> If CIEN is set, indicates that either calibration is finished or that one of certain events have occurred during normal operation. If each function is enabled, CINT will be asserted if too many zeroes occur too often in a period of samples, if the proximity baseline has decreased, or if at least one offset register has been adjusted. Check the CALIBSTAT register to identify the triggering event(s). |
| 0          | SINT     | 0      | R    | <b>System Interrupt.</b> If SIEN is set, indicates that one or more of several events has occurred or is complete. The events related to this interrupt are indicated in the STATUS5 register (0xA6): flicker detection register status has changed.                                                                                                                                                                                            |

**Note(s):**

1. Return to the Register Map ([0x93](#)).

Additional status registers indicate details about saturation, interrupts, and device execution.

**Figure 41:**  
**STATUS2**

| Addr: 0xA3 |               | STATUS2 |      |                                                                                                                                                                                     |
|------------|---------------|---------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field         | Reset   | Type | Bit Description                                                                                                                                                                     |
| 7          | Reserved      | 0       |      |                                                                                                                                                                                     |
| 6          | AVALID        | 0       | R    | <b>ALS Valid.</b> Indicates that the ALS state has completed a cycle since either an assertion of AEN or the last readout of the ASTATUS register.                                  |
| 5          | Reserved      | 0       |      |                                                                                                                                                                                     |
| 4          | ASAT_DIGITAL  | 0       | R    | <b>ALS Digital Saturation.</b> Indicates that the maximum counter value has been reached. Maximum counter value depends on integration time set in the ATIME register.              |
| 3          | ASAT_ANALOG   | 0       | R    | <b>ALS Analog Saturation.</b> Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.                                  |
| 2          | Reserved      | 0       |      |                                                                                                                                                                                     |
| 1          | FDSAT_ANALOG  | 0       | R    | <b>Flicker Detect Analog Saturation.</b> Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit for flicker detection. |
| 0          | FDSAT_DIGITAL | 0       | R    | <b>Flicker Detect Digital Saturation.</b> Indicates that the maximum counter value has been reached during flicker detection.                                                       |

**Note(s):**

1. Return to the Register Map ([0xA3](#)).

**Figure 42:**  
**STATUS3**

| Addr: 0xA4 |           | STATUS3 |      |                                                                                                                       |
|------------|-----------|---------|------|-----------------------------------------------------------------------------------------------------------------------|
| Bit        | Field     | Reset   | Type | Bit Description                                                                                                       |
| 7:6        | Reserved  | 0       |      |                                                                                                                       |
| 5          | AINT_AIHT | 0       | R    | <b>ALS Interrupt High.</b> Indicates that an ALS interrupt occurred because the ALS data exceeded the high threshold. |
| 4          | AINT_AILT | 0       | R    | <b>ALS Interrupt Low.</b> Indicates that an ALS interrupt occurred because the ALS data is below the low threshold.   |
| 3:0        | Reserved  | 8       |      |                                                                                                                       |

**Note(s):**

1. Return to the Register Map ([0xA4](#)).

**Figure 43:**  
**STATUS5**

| Addr: 0xA6 |          | STATUS5 |      |                                                                                                               |
|------------|----------|---------|------|---------------------------------------------------------------------------------------------------------------|
| Bit        | Field    | Reset   | Type | Bit Description                                                                                               |
| 7:4        | Reserved | 0       |      |                                                                                                               |
| 3          | SINT_FD  | 0       | R    | <b>Flicker Detect Interrupt.</b> If SIEN_FD is set, indicates that the FD_STATUS register status has changed. |
| 2:0        | Reserved | 0       |      |                                                                                                               |

**Note(s):**

1. Return to the Register Map ([0xA6](#)).

**Figure 44:**  
**STATUS6**

| Addr: 0xA7 |                   | STATUS6 |      |                                                                                                                                                                                                 |
|------------|-------------------|---------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field             | Reset   | Type | Bit Description                                                                                                                                                                                 |
| 7:6        | Reserved          | 0       |      |                                                                                                                                                                                                 |
| 5          | OVTEMP_DETECTED   | 0       | R    | <b>Over Temperature Detected.</b> Indicates the device temperature is too high. Write 1 to clear this bit.                                                                                      |
| 4          | FD_TRIGGER_ERROR  | 0       | R    | <b>Flicker Detect Trigger Error.</b> Indicates that there is a timing error that prevents flicker detect from functioning correctly.                                                            |
| 3          | Reserved          | 0       |      |                                                                                                                                                                                                 |
| 2          | ALS_TRIGGER_ERROR | 0       | R    | <b>ALS Trigger Error.</b> Indicates that there is a timing error that prevents ALS from functioning correctly. The WTIME is too short for the ATIME configured for the device.                  |
| 1          | SAI_ACTIVE        | 0       | R    | <b>Sleep After Interrupt Active.</b> Indicates that the device is in SLEEP due to an interrupt. To exit SLEEP mode, clear this bit.                                                             |
| 0          | INIT_BUSY         | 0       | R    | <b>Initialization Busy.</b> Indicates that the device is initializing. This bit will remain 1 for about 300µs after power on. Do not interact with the device until initialization is complete. |

**Note(s):**

1. Return to the Register Map ([0xA7](#)).

### ALS Data and Status

The ASTATUS register is required for automatic gain control (AGC). It provides an ALS saturation and ALS gain status associated to each set of ALS data. Reading the ASTATUS register (0x94) latches all 12 ALS data bytes to that status read. Reading these 13 bytes consecutively (0x94 - 0xA0) ensures that the data is concurrent. All ALS data are stored as 16-bit values. If flicker detection is enabled, ALS channel five is used for the flicker detection function and ADATA5 will read 0. The ASTATUS and ALS data registers are read only.

**Figure 45:**  
ASTATUS

| Addr: 0x94 |              | ASTATUS |      |                                                                                                                                                                                                  |
|------------|--------------|---------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field        | Reset   | Type | Bit Description                                                                                                                                                                                  |
| 7          | ASAT_STATUS  | 0       | R    | <b>ALS Saturation Status.</b> Indicates if the latched data is affected by analog or digital saturation.                                                                                         |
| 6:4        | Reserved     | 0       |      |                                                                                                                                                                                                  |
| 3:0        | AGAIN_STATUS | 0       | R    | <b>ALS Gain Status.</b> Indicates the ALS gain applied for the ALS data latched to this ASTATUS read. The ALS gain from this status read is required to calculate ALS results if AGC is enabled. |

**Note(s):**

1. Return to the Register Map ([0x94](#)).

**Figure 46:**  
ALS Data Registers

| Bits | Addr | Field  | Description                              |
|------|------|--------|------------------------------------------|
| 7:0  | 0x95 | ADATA0 | <b>ALS Channel Zero Data:</b> CLEAR data |
| 15:8 | 0x96 |        |                                          |
| 7:0  | 0x97 | ADATA1 | <b>ALS Channel One Data.</b> RED data    |
| 15:8 | 0x98 |        |                                          |
| 7:0  | 0x99 | ADATA2 | <b>ALS Channel Two Data.</b> GREEN data  |
| 15:8 | 0x9A |        |                                          |
| 7:0  | 0x9B | ADATA3 | <b>ALS Channel Three Data.</b> BLUE data |
| 15:8 | 0x9C |        |                                          |

| Bits | Addr | Field  | Description                                 |
|------|------|--------|---------------------------------------------|
| 7:0  | 0x9D | ADATA4 | <b>ALS Channel Four Data.</b> WIDEBAND data |
| 15:8 | 0x9E |        |                                             |
| 7:0  | 0x9F | ADATA5 | <b>ALS Channel Five Data.</b> FLICKER data  |
| 15:8 | 0xA0 |        |                                             |

**Note(s):**

- Return to the Register Map (0x95, 0x96, 0x97, 0x98, 0x99, 0x9A, 0x9B, 0x9C, 0x9D, 0x9E, 0x9F, 0xA0).

The flicker detection status register indicates if flicker detection data is valid and whether 100Hz or 120Hz ambient light flicker frequencies are present.

**Figure 47:**  
**FD\_STATUS**

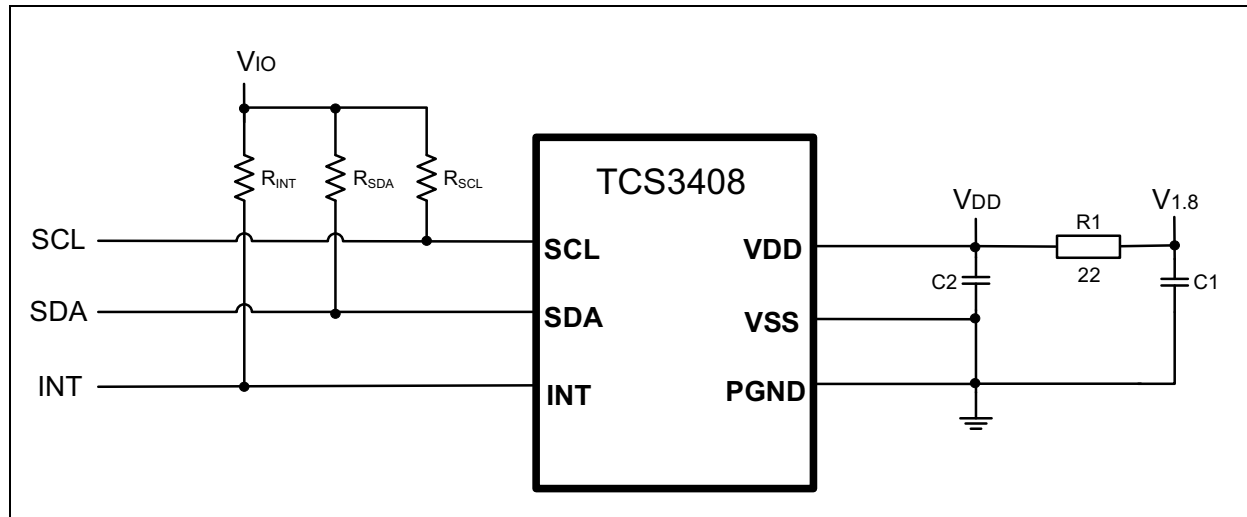
| Addr: 0xDB |                        | FD_STATUS |      |                                                                                                                                                                                                 |
|------------|------------------------|-----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Field                  | Reset     | Type | Bit Description                                                                                                                                                                                 |
| 7:6        | Reserved               | 0         |      |                                                                                                                                                                                                 |
| 5          | FD_MEASUREMENT_VALID   | 0         | R    | <b>Flicker Detection Measurement Valid.</b> Indicates that flicker detection measurement is complete. Write 1 to this bit to clear this field.                                                  |
| 4          | FD_SATURATION_DETECTED | 0         | R    | <b>Flicker Saturation Detected.</b> Indicates that saturation occurred during the last flicker detection measurement, and the result may not be valid. Write 1 to this bit to clear this field. |
| 3          | FD_120HZ_FLICKER_VALID | 0         | R    | <b>Flicker Detection 120Hz Flicker Valid.</b> Indicates that the 120Hz flicker detection calculation is valid. Write 1 to this bit to clear this field.                                         |
| 2          | FD_100HZ_FLICKER_VALID | 0         | R    | <b>Flicker Detection 100Hz Flicker Valid.</b> Indicates that the 100Hz flicker detection calculation is valid. Write 1 to this bit to clear this field.                                         |
| 1          | FD_120HZ_FLICKER       | 0         | R    | <b>Flicker Detected at 120Hz.</b> Indicates if an ambient light source is flickering at 120Hz.                                                                                                  |
| 0          | FD_100HZ_FLICKER       | 0         | R    | <b>Flicker Detected at 100Hz.</b> Indicates if an ambient light source is flickering at 100Hz.                                                                                                  |

**Note(s):**

- Return to the Register Map (0xDB).

It is highly recommended to consult the ams OSRAM application team for circuit diagram and layout review at design-in.

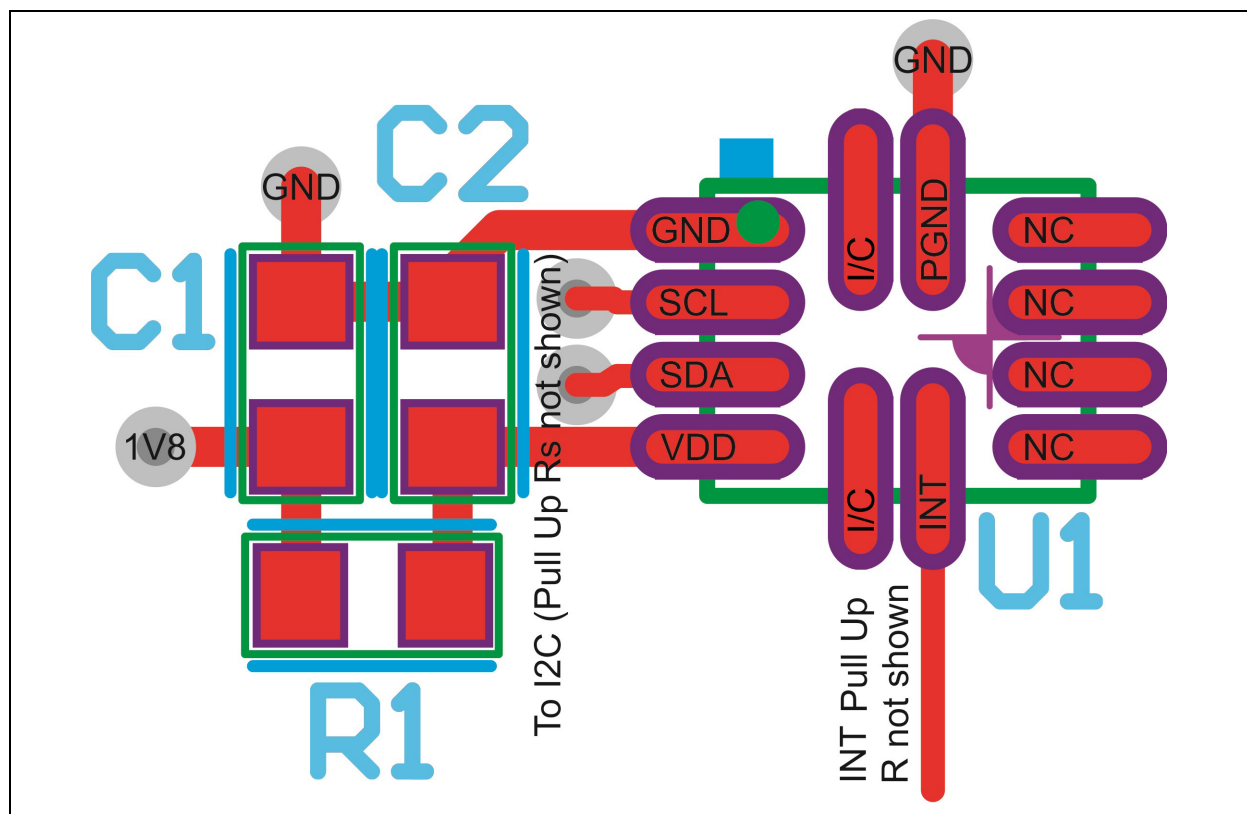
**Figure 48:**  
**TCS3408 Typical Application Circuit**



**Note(s):**

1. C1 in the graphic above shall be 4.7 $\mu$ F, 6.3V, 10% and C2 in the graphic above shall be 1 $\mu$ F, 6.3V, 20%. All ground vias shall connected to a solid ground plane.

**Figure 49:**  
**TCS3408 Recommended Part Placement**

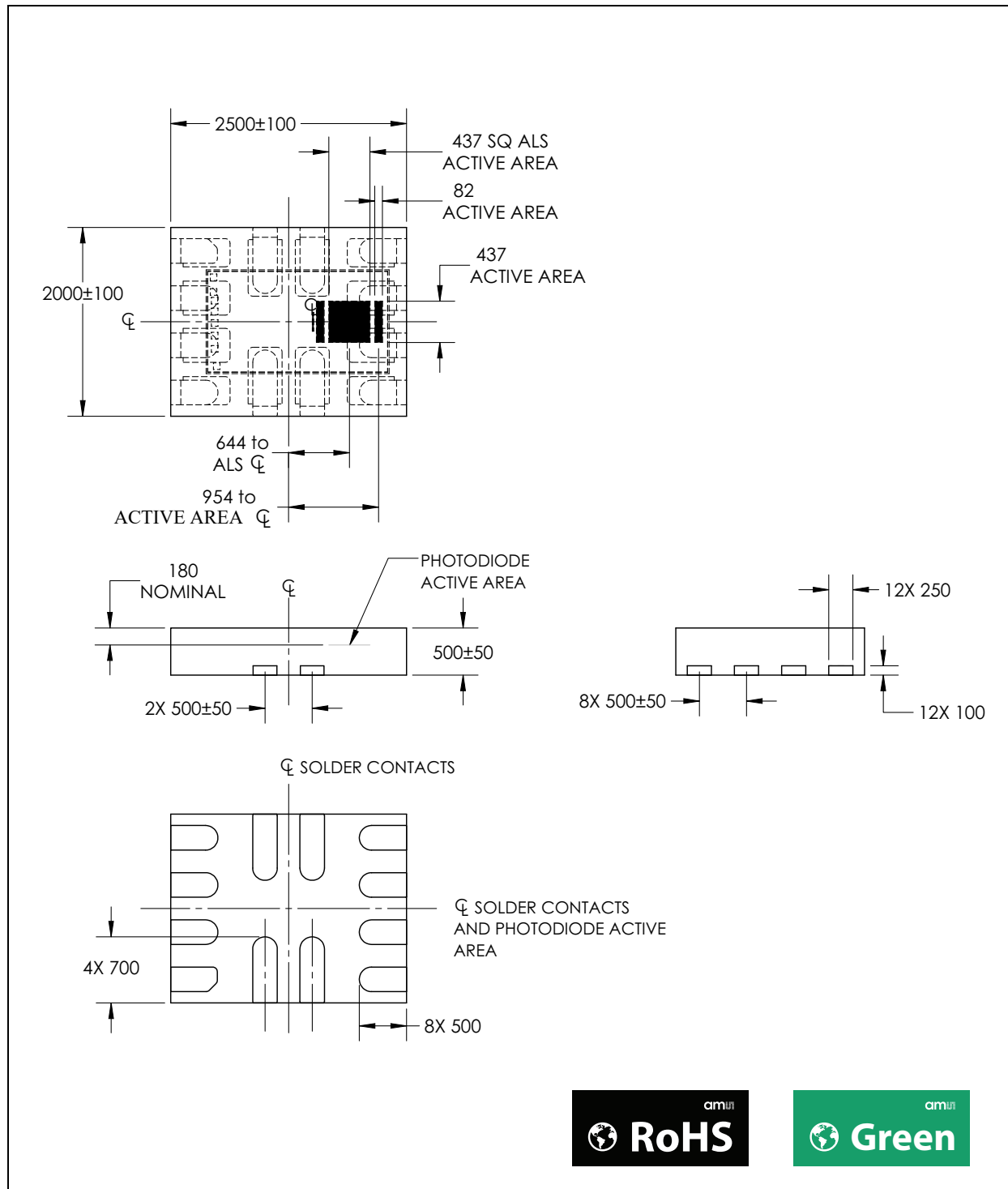


**Note(s):**

1. NC pins do not have an internal electrical connection. For device ESD protection, it is recommended to connect it to ground.

## Package Drawings & Markings

**Figure 50:**  
TCS3408 Module Dimensions



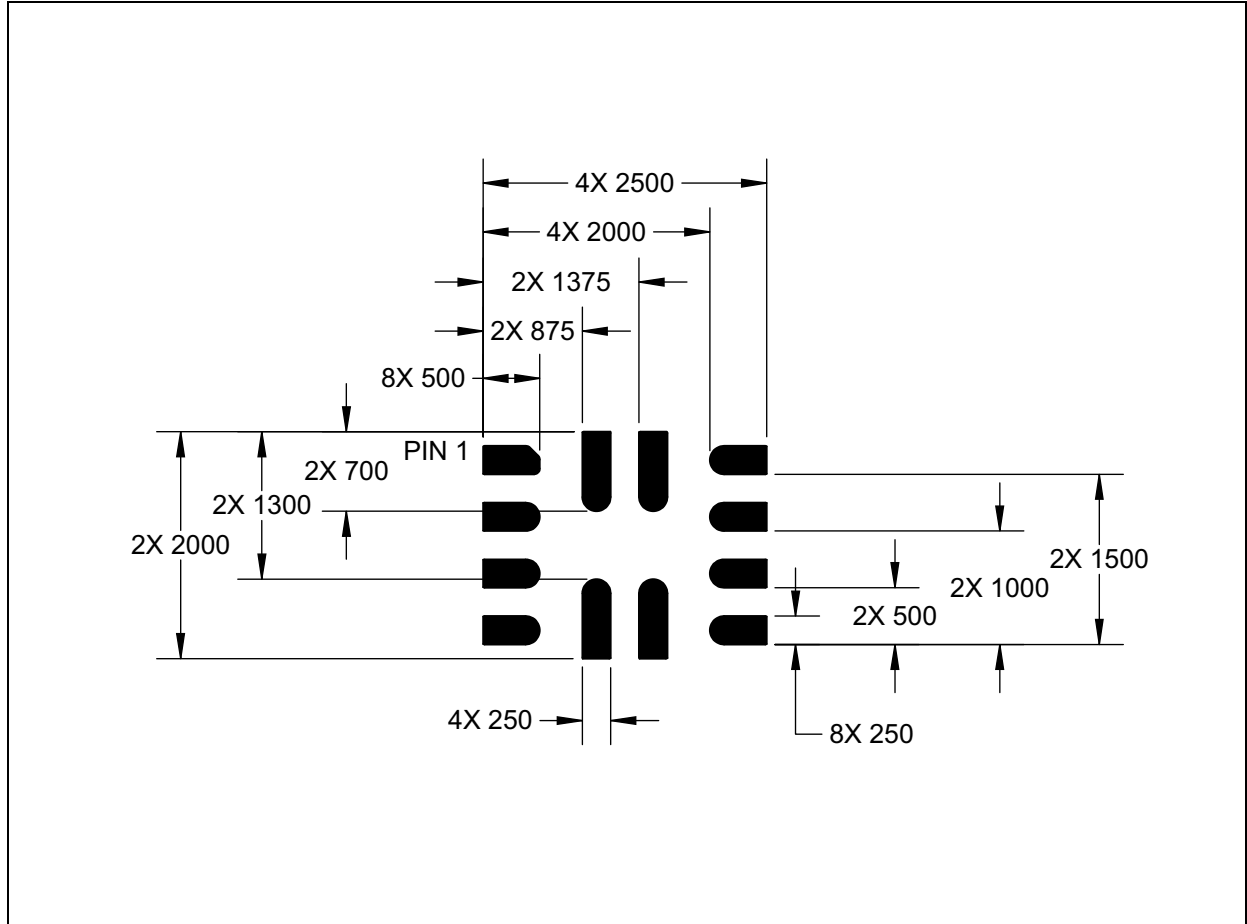
**Note(s):**

1. All linear dimensions are in micrometers.
2. The die is centered within the package within a tolerance of  $\pm 75$  micrometers.
3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

## PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

**Figure 51:**  
Recommended PCB Pad Layout

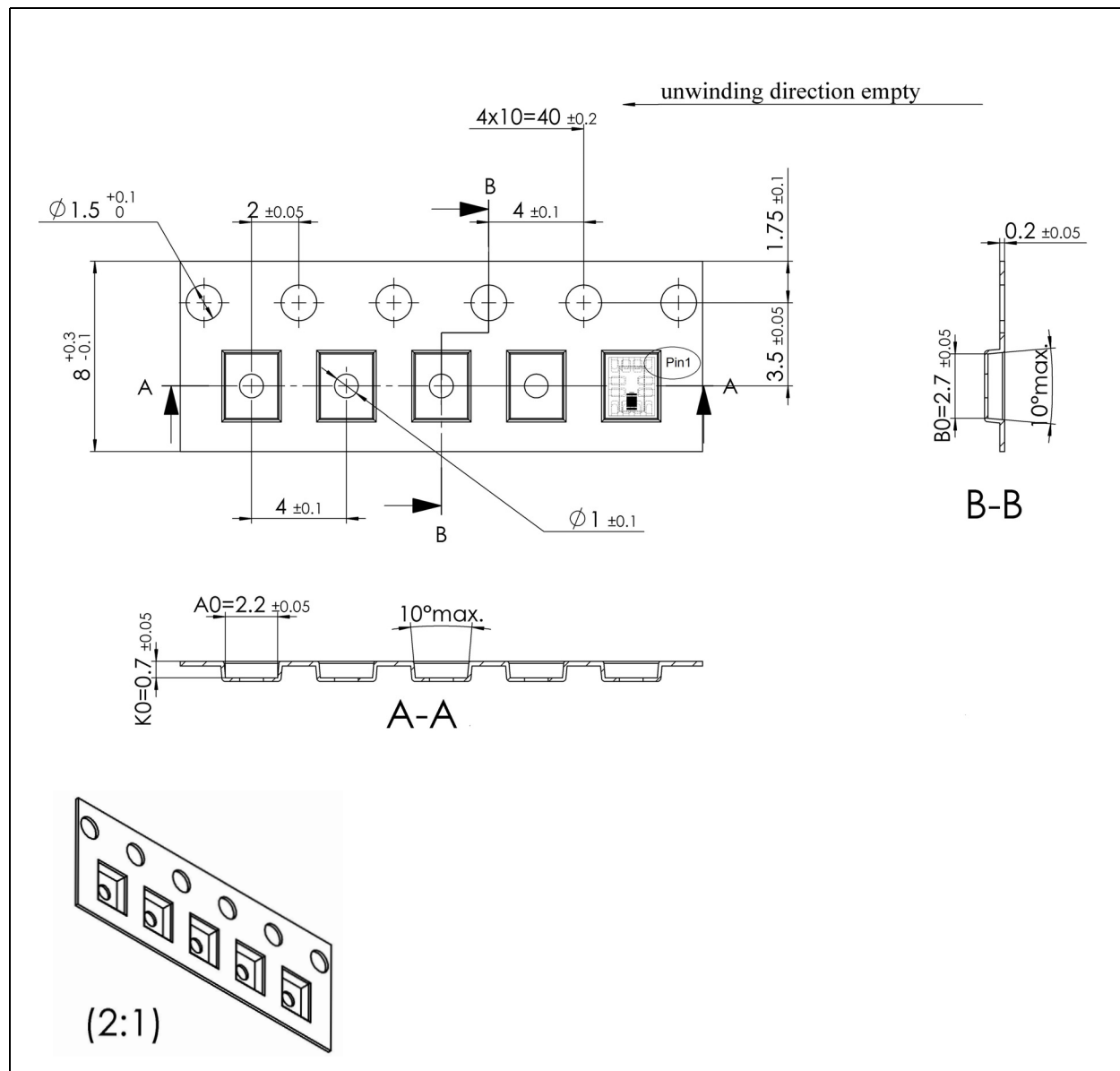


**Note(s):**

1. All linear dimensions are in micrometers.
2. Dimension tolerances are  $\pm 0.05\text{mm}$  unless otherwise noted.
3. This drawing is subject to change without notice.

## Tape & Reel Information

**Figure 52:**  
Tape and Reel Mechanical Drawing



**Note(s):**

1. All linear dimensions are in millimeters. Dimension tolerance is  $\pm 0.10$  mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A0, B0, and K0 are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is generally 330 millimeters in diameter and contains 10000 parts. Please reconfirm for actual orders.
5. ams OSRAM packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

## Soldering & Storage Information

### Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

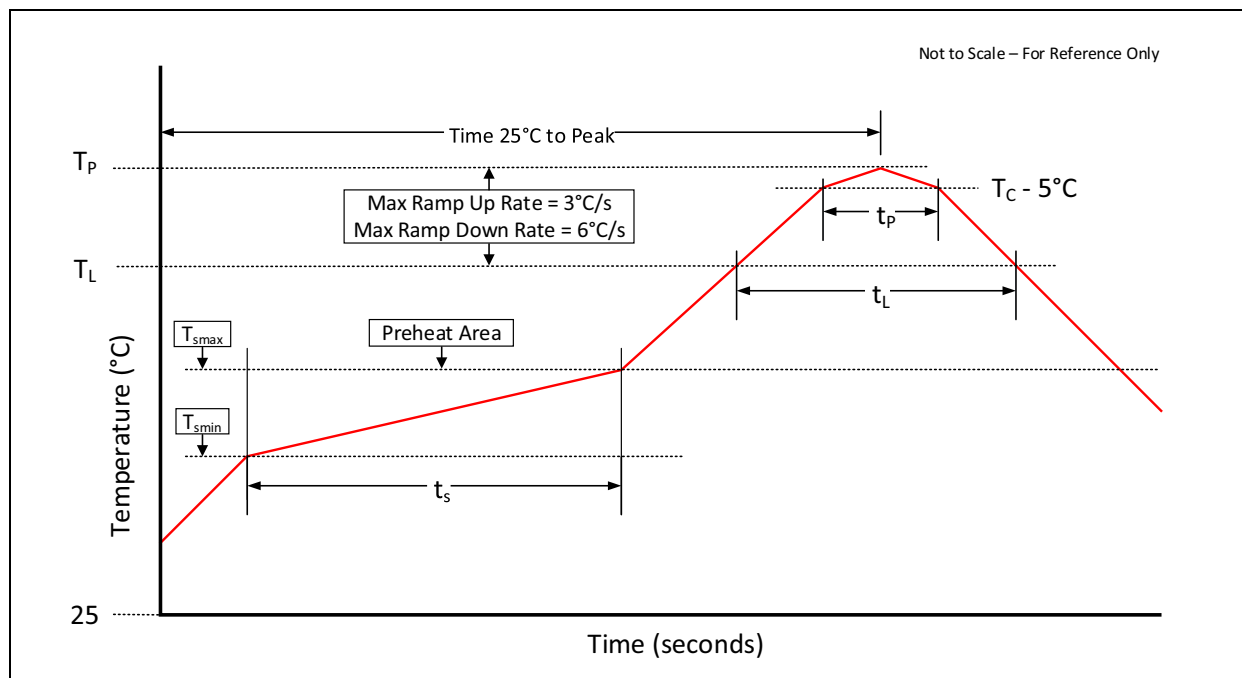
**Figure 53:**  
Solder Reflow Profile

| Profile Feature Preheat/Soak                                                                   | Sn-Pb Eutectic Assembly                                                                                                                       | Pb-Free Assembly                                                                                                                              |
|------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Temperature Min ( $T_{smin}$ )                                                                 | 100°C                                                                                                                                         | 150°C                                                                                                                                         |
| Temperature Max ( $T_{smax}$ )                                                                 | 150°C                                                                                                                                         | 200°C                                                                                                                                         |
| Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ )                                               | 60-120 seconds                                                                                                                                | 60-120 seconds                                                                                                                                |
| Ramp-up rate ( $T_L$ to $T_P$ )                                                                | 3°C/second max.                                                                                                                               | 3°C/second max.                                                                                                                               |
| Liquidous temperature ( $T_L$ )<br>Time ( $t_L$ ) maintained above $T_L$                       | 183°C<br>60-150 seconds                                                                                                                       | 217°C<br>60-150 seconds                                                                                                                       |
| Peak package body temperature ( $T_P$ )                                                        | For users $T_P$ must not exceed the Classification temp of 235°C<br>For suppliers $T_P$ must equal or exceed the Classification temp of 235°C | For users $T_P$ must not exceed the Classification temp of 260°C<br>For suppliers $T_P$ must equal or exceed the Classification temp of 260°C |
| Time ( $t_p$ ) <sup>(1)</sup> within 5°C of the specified classification temperature ( $T_C$ ) | 20 <sup>(1)</sup> seconds                                                                                                                     | 30 <sup>(1)</sup> seconds                                                                                                                     |
| Ramp-down rate ( $T_P$ to $T_L$ )                                                              | 6°C/second max.                                                                                                                               | 6°C/second max.                                                                                                                               |
| Time 25°C to peak temperature                                                                  | 6 minutes max.                                                                                                                                | 8 minutes max.                                                                                                                                |

**Note(s):**

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

**Figure 54:**  
**Solder Reflow Profile Graph**



## Storage Information

### Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

### Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 24 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

**Floor Life**

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

**Rebaking Instructions**

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

## Ordering & Contact Information

**Figure 55:**  
**Ordering Information**

| Ordering Code | Address | Interface             | Delivery Form | Delivery Quantity |
|---------------|---------|-----------------------|---------------|-------------------|
| TCS34083      | 0x39    | 1.8V I <sup>2</sup> C | Tape & Reel   | 10000 pcs/reel    |
| TCS34087      | 0x29    | 1.8V I <sup>2</sup> C | Tape & Reel   | 10000 pcs/reel    |
| TCS34083M     | 0x39    | 1.8V I <sup>2</sup> C | Tape & Reel   | 1000 pcs/reel     |
| TCS34087M     | 0x29    | 1.8V I <sup>2</sup> C | Tape & Reel   | 1000 pcs/reel     |

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| Document Status          | Product Status  | Definition                                                                                                                                                                                                                                                               |
|--------------------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Preview          | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice                                                                          |
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## Revision Information

| Changes from 1-01 (2021-Jul-28) to current revision 2-00 (2023-Feb-01) | Page |
|------------------------------------------------------------------------|------|
| Updated "Shelf Life" to 24 months                                      | 45   |

**Note(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

## Content Guide

|           |                                                 |
|-----------|-------------------------------------------------|
| <b>1</b>  | <b>General Description</b>                      |
| 2         | Key Benefits & Features                         |
| 2         | Applications                                    |
| 3         | Block Diagram                                   |
| <b>4</b>  | <b>Pin Assignments</b>                          |
| <b>5</b>  | <b>Absolute Maximum Ratings</b>                 |
| <b>6</b>  | <b>Optical Characteristics</b>                  |
| <b>8</b>  | <b>Electrical Characteristics</b>               |
| <b>9</b>  | <b>Timing Characteristics</b>                   |
| <b>11</b> | <b>Typical Operating Characteristics</b>        |
| <b>13</b> | <b>Detailed Description</b>                     |
| 14        | State Machine Diagrams                          |
| 16        | I <sup>2</sup> C Protocol                       |
| <b>17</b> | <b>Register Overview</b>                        |
| 17        | Register Map                                    |
| 19        | Register Descriptions                           |
| 19        | Power, Enable, and Operation                    |
| 21        | Identification                                  |
| 22        | ALS Configuration                               |
| 29        | General Configuration                           |
| 34        | Status Registers                                |
| 38        | ALS Data and Status                             |
| <b>40</b> | <b>Application Information</b>                  |
| <b>41</b> | <b>Package Drawings &amp; Markings</b>          |
| <b>42</b> | <b>PCB Pad Layout</b>                           |
| <b>43</b> | <b>Tape &amp; Reel Information</b>              |
| <b>44</b> | <b>Soldering &amp; Storage Information</b>      |
| 44        | Soldering Information                           |
| 45        | Storage Information                             |
| 45        | Moisture Sensitivity                            |
| 45        | Shelf Life                                      |
| 46        | Floor Life                                      |
| 46        | Rebaking Instructions                           |
| <b>47</b> | <b>Ordering &amp; Contact Information</b>       |
| <b>48</b> | <b>RoHS Compliant &amp; ams Green Statement</b> |
| <b>49</b> | <b>Copyrights &amp; Disclaimer</b>              |
| <b>50</b> | <b>Document Status</b>                          |
| <b>51</b> | <b>Revision Information</b>                     |