Product Document

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AS5130

8-Bit Programmable Magnetic Rotary Encoder with Motion Detection and Multiturn

General Description

The AS5130 is a contactless magnetic rotary encoder for accurate angular measurement over a full turn of 360°. It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device. The angle can be measured using only a simple two-pole magnet rotating over the center of the chip. The magnet may be placed above or below the IC. The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 8-bit = 256 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal. The AS5130 can be operated in pulsed mode (V_{supply}=off), which reduces the average power consumption significantly. During V_{supply}=off, the measured angle can be stored using an internal storage register supplied by a low power voltage line. This mode achieves very low power consumption during polling of the rotary position of the magnet. If the position of the magnet changes, then the motion detection feature wakes up an external system. The device is capable of counting the amount of magnet revolutions. The multi turn counter value is stored in a register and can be read in addition to the angle information. Furthermore, any arbitrary position can be set as zero-position. The system is tolerant to misalignment, air gap variations, temperature variations and external magnetic fields and high reliability due to non-contact sensing.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5130, 8-Bit Programmable Magnetic Rotary Encoder with Motion Detection and Multiturn are listed below:

Figure 1:
Added Value of Using AS5130

Benefits	Features
• Easy to use and cost efficient system design possible	• 360° contactless angular position encoding

• Optimized for BLDC motor control	• Two digital 8-bit absolute outputs:
	  • Serial interface
	  • Pulse width modulated (PWM) output

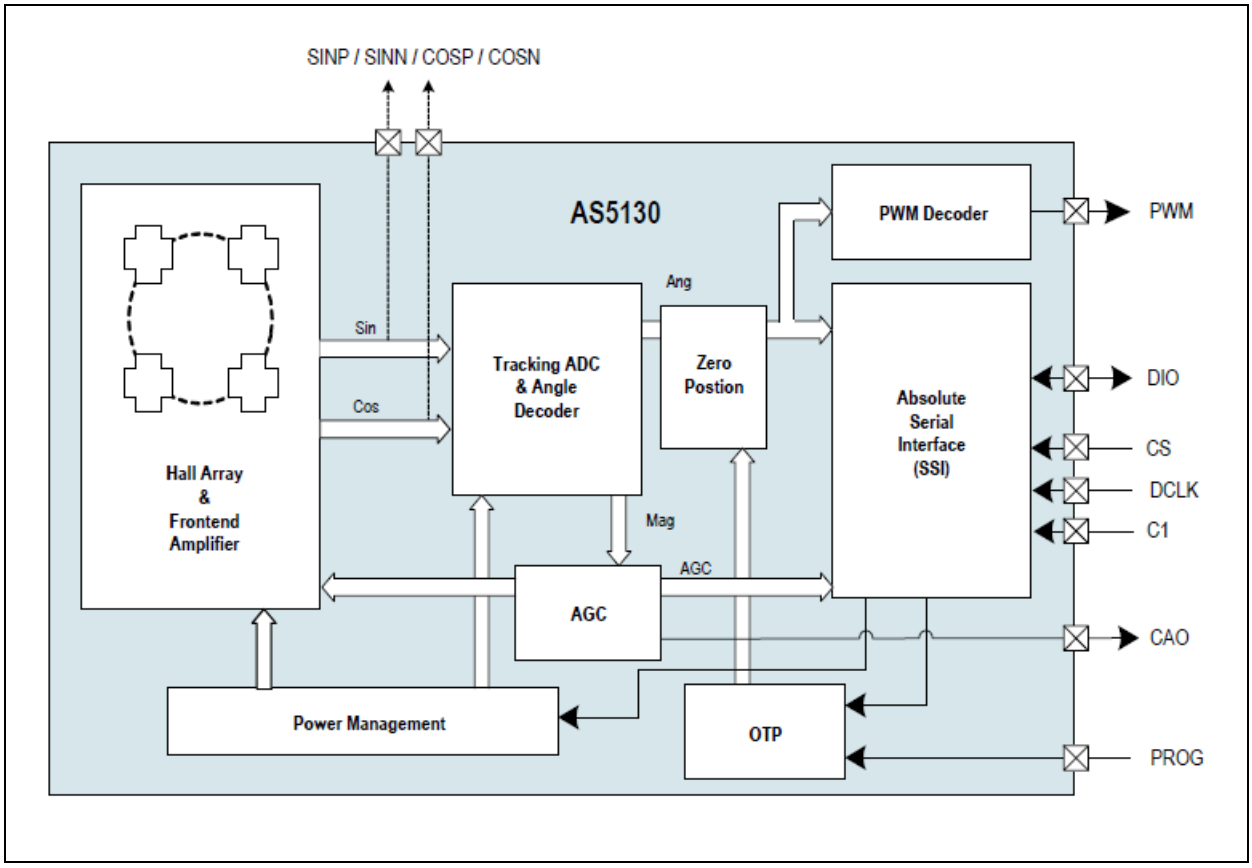
• Flexible magnet positioning	• User programmable zero position
• Absolute angle information over several rotations	• Multi turn counter / Movement detection
• Suited for challenging automotive applications	• Automotive qualified to AEC-Q100, grade 1

Applications

The AS5130 applications include:

- Ignition key position sensing
- Steering wheel position sensing
- Transmission gearbox encoder
- Front panel rotary switches
- Replacement of potentiometers

Figure 2:
AS5130 Block Diagram



Pin Assignment

Figure 3:
Pin Diagram (Top View)

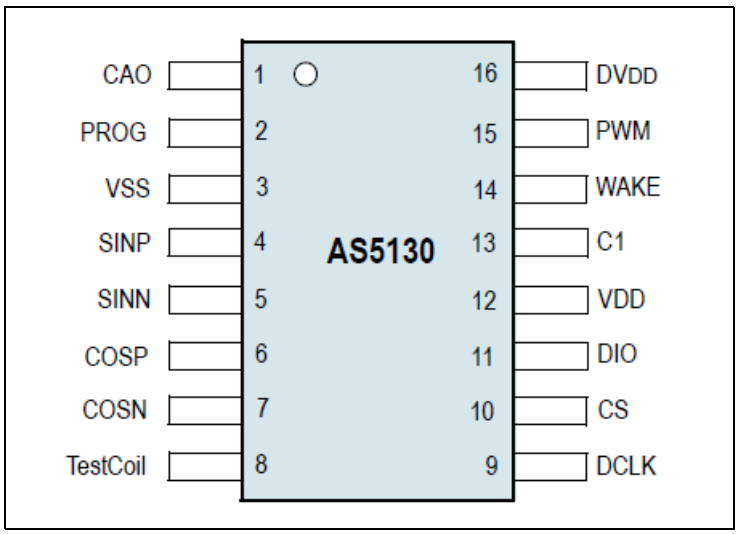


Figure 4:
Pin Descriptions

Pin Name	Pin Number	Description
CAO	1	Indicates if the magnetic field is present. If the field is too low, the signal is HI.
PROG	2	**OTP programming pad, programming voltage.** For normal operation it must be left unconnected.
VSS	3	Supply ground.
SINP	4	Used for factory testing. For normal operation it must be left unconnected.
SINN	5	Used for factory testing. For normal operation it must be left unconnected.
COSP	6	Used for factory testing. For normal operation it must be left unconnected.
COSN	7	Used for factory testing. For normal operation it must be left unconnected.
Test Coil	8	**Test pin.** Must be left unconnected.
DCLK	9	**Clock source for SSI communication.** Schmitt trigger input.
CS	10	**Chip select for SSI.** Active high. Schmitt trigger input.

Pin Name	Pin Number	Description
DIO	11	Data input / output for SSI communication.
VDD	12	Positive supply voltage 5V.
C1	13	**Test mode selector.** For normal operation it must be connected to VSS.
WAKE	14	**Interrupt output.** Used for polling mode. Open Drain NMOS. Use pull-up resistor with >1.5kΩ.
PWM	15	**Pulse width modulation output.** 0.5µs width step per LSB.
DV_{DD}	16	Pin to connect to low power supply for polling mode. Must be connected to VSS in normal mode.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Supply voltage	0.3	7	V	Only relevant for polling operation mode, supply voltage with capacitor of the integrated storage register during t_{off} phase of VDD
Input pin voltage	V_{SS}-0.5	VDD	V	
Input current (latchup immunity)	-100	100	mA	AEC-Q100-004
Electrostatic discharge		±2	kV	AEC-Q100-002
Package thermal resistance SSOP-16	133	168	K/W	Still Air / Single Layer PCB
Storage temperature	-55	150	°C	
Ambient temperature	-40	125	°C	
Junction temperature		150	°C	
Package body temperature		260	°C	IPC/JEDEC J-STD-020.The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 *"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Relative humidity (non-condensing)	5	85	%	
Moisture sensitivity level (MSL)	3			Represents a maximum floor life time of 168h

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

T_{AMB} = -40°C to 125°C, unless otherwise noted.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Positive supply voltage	Except OTP programming	4.5	5	5.5	V
DV_{DD}	Polling mode supply voltage		3.6	5	5.5	V
IDD	Power supply current		14		24	mA
I_{off}	Power down mode			1.4	2	mA
N	Resolution			8		bit
				1.406		deg
T_{PwrUp}	Power up time	Startup from zero			2000	µs
		Startup with preset AGC - Polling mode (Supplied during t_{off} phase of VDD from the external buffer capacitor via DV_{DD} pin)			250	
		Startup from low power mode			150	
t_{da}	Propagation delay	Analog signal path; over full temperature range		15	17	µs
t_{dd}	Tracking rate	Step rate of tracking ADC; 1 step = 1.406°	0.85	1.15	1.45	µs
t_{delay}	Signal processing delay	Total signal processing delay, Analog + Digital + SSI readout (t_{da} + t_{dd} + t_{SSI})			21.55	µs
T	Analog filter time constant	Internal lowpass filter	4.1	6.6	12.5	µs
INL_{cm}	Accuracy	Centered Magnet	-2		2	
		Within horizontal displacement radius (see parameters for magnet)	-3		3	
TN	Transition noise	rms (1 sigma)			0.235	

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POR_r	Power-on-reset levels	VDD rising	3.7	4	4.3	V
POR_f		VDD falling	3.4	3.7	3.9	V
Parameters for Magnet						
n	Rotational speed	Frequencies above 1000 rpm causes an additional not specified DNL Error	-30000		30000	rpm
MD	Magnet diameter	Diametrically magnetized		6		mm
MT	Magnet thickness			2.5		mm
B_i	Magnetic input range	Valid for use of full range of sensitivity	32		75	mT
s	Magnetic sensitivity of AGC	AGC value available at SSI	0.5		5	LSB/ mT
B_{DC}	Magnetic offset	Magnetic stray field without gradient			4	mT
DC/AC Characteristics for Digital Inputs and Outputs						
CMOS Input						
V_{IH}	High level input voltage		$0.7 \times V_{DD}$			V
V_{IL}	Low level input voltage				$0.3 \times V_{DD}$	V
I_{LEAK}	Input leakage current				1	µA
CMOS Output						
V_{OH}	High level output voltage		V_{DD} -0.5			V
V_{OL}	Low level output voltage				VSS + 0.4	V
C_L	Capacitive load				35	pF
t_{slew}	Slew rate	External capacitive load C_L = 35pF External series resistance R = 0Ω Junction temperature T_J = 136°C Rise time of the internal driver t_rise = 3ns Fall time of the internal driver t_fall = 3ns			30	ns
t_{delay}	Time rise fall				15	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{out\_wake\ up}$	Wake up output	Open drain output with tri-state behavior			5	V
Programming Parameters						
V_{PROG}	Programming voltage	Static voltage at pin PROG	8.0		8.5	V
I_{PROG}	Programming current				100	mA
$Tamb_{PROG}$	Programming ambient temperature	During programming	0		85	°C
t_{PROG}	Programming time	Timing is internally generated	2		4	µs
$V_{R,prog}$	Analog readback voltage	During analog readback mode at pin PROG			0.5	V
$V_{R,unprog}$			2.2		3.5	
$Wake_{LSB}$	Angle difference threshold for wake up generation	Factory setting is 4 LSB, value is accessible by SSI in buffered register and can be changed by customer.	0		127	LSB
8-Bit PWM Output						
N_{PWM}	PWM resolution			8		bit
PW_{MIN}	PWM pulse width	Angle = 0° (00_H)	0.71	0.55	0.43	µs
PW_{MAX}	PWM pulse width	Angle = 358.6° (FF_H)	182.88	142.24	108.48	µs
PW_P	PWM period	Over full temperature range	183.6	142.8	108.9	µs
f_{PWM}	PWM frequency	=1 / PWM period	5.44	7	9.18	kHz
Hyst	Digital hysteresis	At change of rotation direction		1		bit
Serial 8-Bit Output						
f_{CLK}	Clock frequency	Normal operation			6	MHz
t_{CLK}			166.6			ns
$f_{CLK,P}$	Clock frequency	During OTP programming	250		500	kHz

Timing Characteristics

T_{AMB} = -40°C to 125°C, unless otherwise noted.

Figure 7:
Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t0	Rising CLK to CS		15		--	ns
t1	Chip select to positive edge of CLK		15		--	ns
t2	Chip select to drive bus externally		--		--	ns
t3	Setup time command bit, data valid to positive edge of CLK		30			ns
t4	Hold time command bit, data valid after positive edge of CLK		30			ns
t5	Float time, positive edge of CLK for last command bit to bus float		30		CLK/2	ns
t6	Bus driving time, positive edge of CLK for last command bit to bus drive		CLK/2+0		CLK/2+30	ns
t7	Setup time data bit, data valid to positive edge of CLK		CLK/2+0		CLK/2+30	ns
t8	Hold time data bit, data valid after positive edge of CLK		CLK/2+0		CLK/2+30	ns
t9	Hold time chip select, positive edge CLK to negative edge of chip select		30			ns
t10	Bus floating time, negative edge of chip select to float bus		0		30	ns
t_{TO}	Timeout period in 2-wire mode (from rising edge of CLK)		20		24	µs

Magnetic Input Range

The magnetic input range is defined by the AGC loop. This regulating loop keeps the Hall sensor output in the optimum range for low SNR by adjusting the Hall bias current. This loop can adjust to a magnetic field strength variation of ±38%. The AGC output voltage is an indicator for the magnetic field.

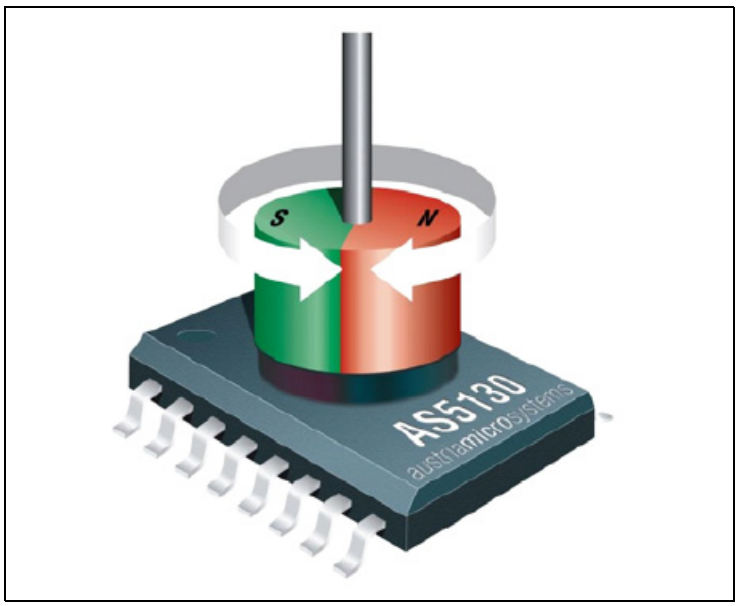
The nominal magnetic field for a balanced AGC is defined by the Hall bias and the Hall sensitivity and can be set by a variable gain in the signal path. The gain can be set in 8 steps in the OTP or by the SSI in a mirror register. The resulting magnetic input range is a value of $B_{nominal}$ ±38% inside of a range of 32mT to 75mT, if the trimming is performed by the customer.

Figure 8:
Magnetic Input Range

Setting	0	1	2	3	4	5	6	7
Binary	000	001	010	011	100	101	110	111
Gain A	0.9	1.05	1.2	1.4	1.65	1.9	2.2	2.55
B_{limit}	Max. 75mT							Min. 32mT

Detailed Description

Figure 9:
Typical Arrangement of AS5130 and Magnet



Connecting the AS5130

The AS5130 can be connected to an external controller in several ways as listed below:

- Serial 3-wire connection (default setting)
- Serial 3-wire connection (OTP programming option)
- 1-wire PWM connection
- Analog output
- Analog Sin/Cos outputs with external interpolator

Serial 3-Wire Connection (Default Setting)

In this mode, the AS5130 is connected to the external controller via three SSI signals: Chip Select (CS), Clock (CLK) input and DIO (Data) in/output. This configuration not only helps to read and write data but also defines different operation modes. The data transfer in all cases is done via the DIO port.

Figure 10:
Standard SSI Serial Data Interface

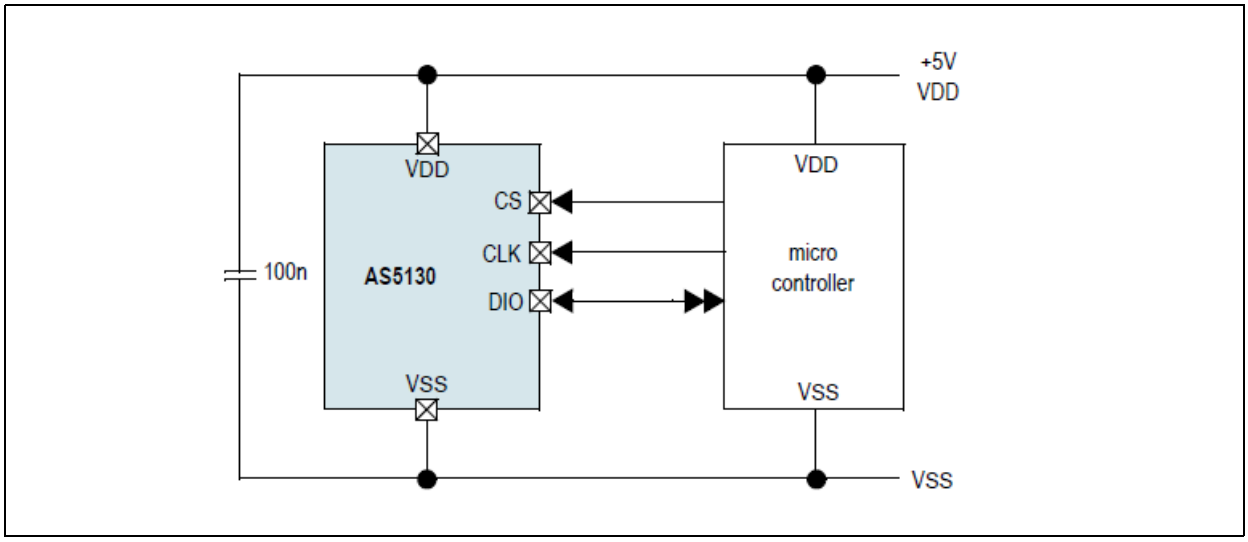


Figure 11:
Normal Operation Mode

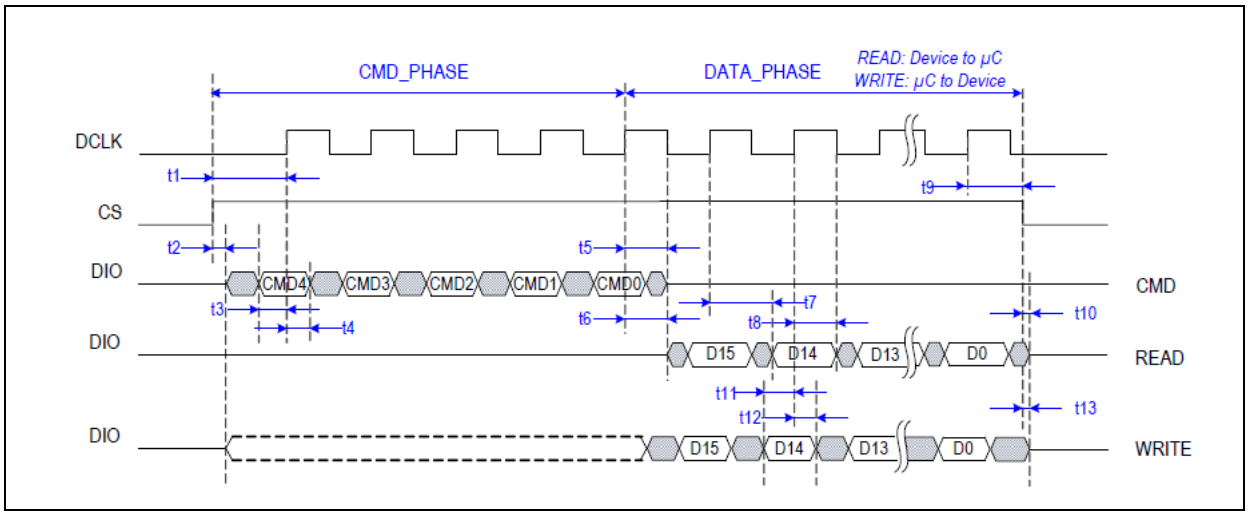


Figure 12:
Serial Bit Sequence (16-Bit Read/Write)

Write Command					Read/Write Data														
C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	9	8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 13:
Extended Operation Mode (For Access of OTP Only)

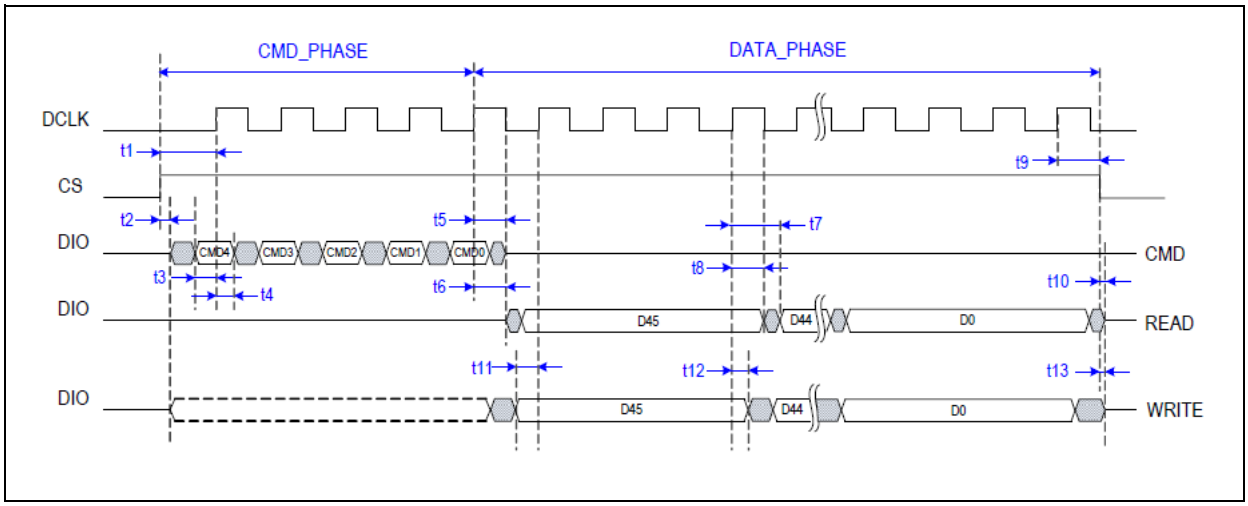


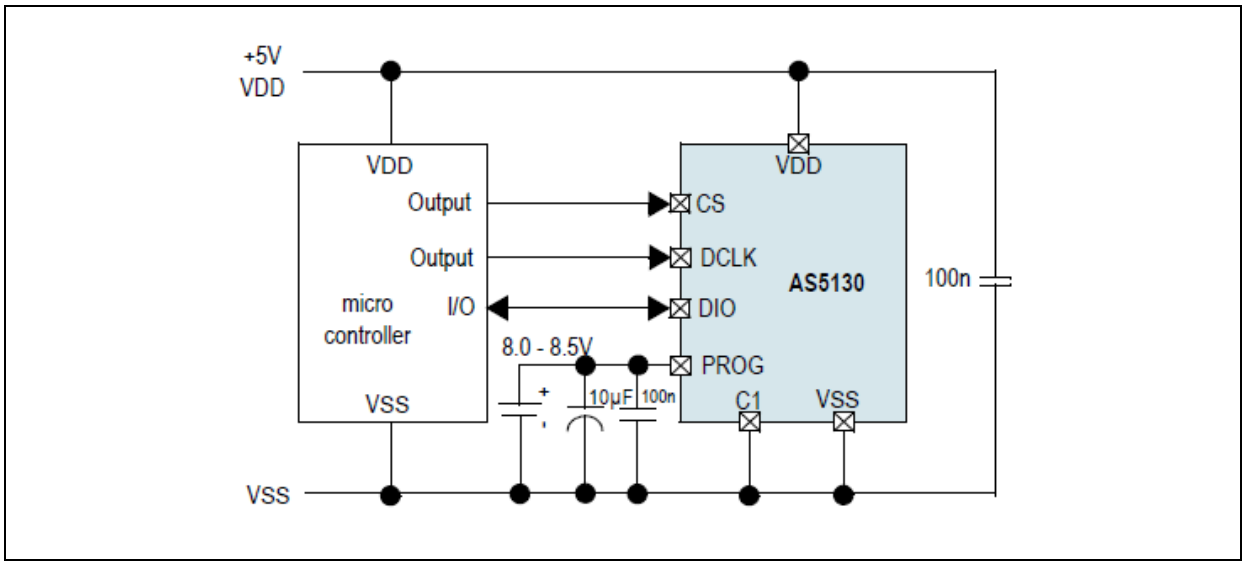
Figure 14:
Serial Bit Sequence (16-Bit Read/Write)

Write Command					Read/Write Data														
C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	9	8	D7	D6	D5	D4	D3	D2	D1	D0

Serial 3-Wire Connection (OTP Programming Option)

This mode provides with an option to configure the serial interface for programming the OTP register. Using a clock input (CLK), DIO (Data) in/output and CS pin, it is possible to write and read out data from the OTP Register. The data transfer is done via the DIO channel. For programming, the PROG pin must be connected to +8V. Analog readout for trimming verification is mandatory.

Figure 15:
Serial Data Transmission in Continuous Readout Mode



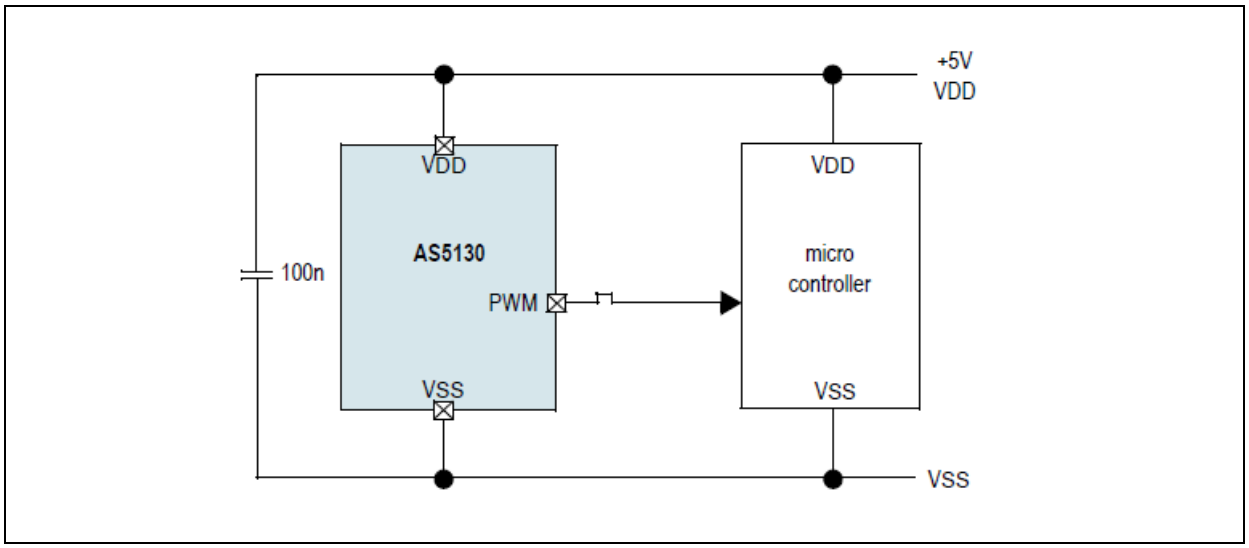
Note(s):

1. For further details on OTP programming, please refer to OTP Programming.

1-Wire PWM Connection

If the line (PWM) is used as angle output, the total number of connections can be reduced to three, including the supply lines. This type of configuration is especially useful for remote sensors. Low power mode is not possible in this configuration. If the AS5130 angular data is invalid, the PWM output will remain at low state.

Figure 16:
Data Transmission With Pulse Width Modulated (PWM) Output



The minimum PWM pulse width t_{ON} (PWM = high) is 1 LSB @ 0° (Angle reading = 00_H). 1LSB = nom.,0.556µs. The PWM pulse width increases with 1LSB per step. At the maximum angle 358.6° (Angle reading = FF_H), the pulse width t_{ON} (PWM = high) is 256 LSB and the pause width t_{OFF} (PWM = low) is 1 LSB. This leads to a total period (t_{ON} + t_{OFF}) of 257LSB.

Figure 17:
PWM Output Signal

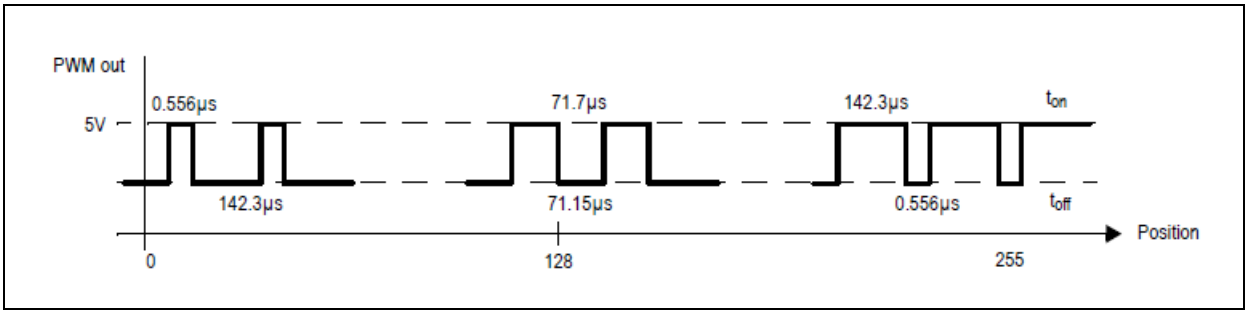


Figure 18:
PWM Signal Parameters

Position	Angle	LSB @ High	t_high	Low Column	t_low	Duty-Cycle
0	0°	1	0.556µs	256	142.3µs	0.39%
127	178.59°	128	71.15µs	129	71.7µs	49.4%
128	180°	129	71.7µs	128	71.15µs	50.2%
255	358.59°	256	142.3µs	1	0.556µs	99.6%

This means that the PWM pulse width is (position + 1) LSB, where position is 0 to 255.

The tolerance of the absolute pulse width and frequency can be eliminated by calculating the angle with the duty cycle rather than with the absolute pulse width:

(EQ1)
$$angle[8-bit] = \left(257\frac{t_{ON}}{t_{ON}+t_{OFF}}\right) - 1$$

results in an 8-bit value from 00_H to FF_H,

(EQ2)
$$angle[^{o}] = \frac{360}{256}\left[\left(257\frac{t_{ON}}{t_{ON}+t_{OFF}}\right) - 1\right]$$

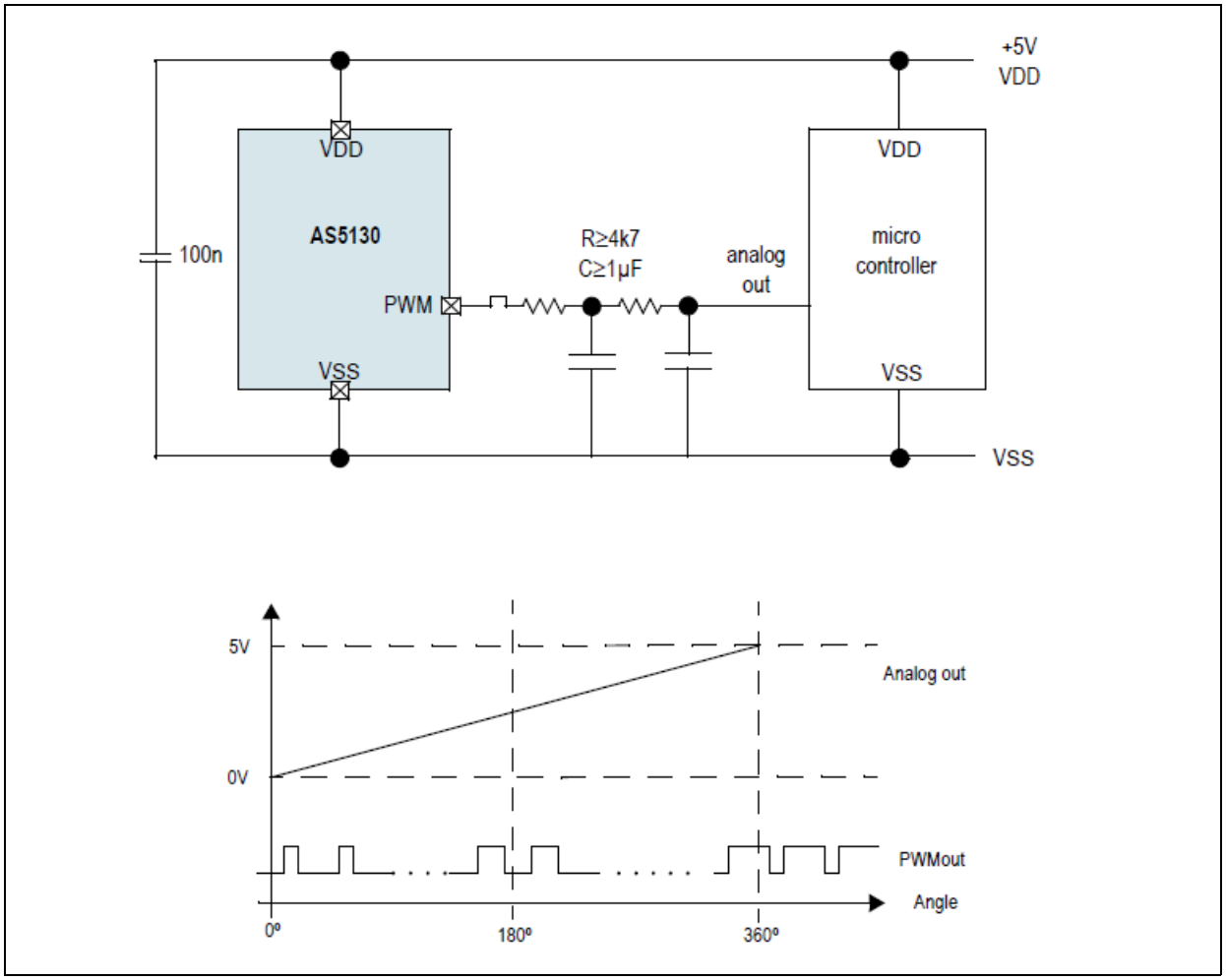
results in a degree value from 0° to 358.6°

Note(s): The absolute frequency tolerance is eliminated by dividing t_{ON} by (t_{ON}+T_{OFF}), as the change of the absolute timing effects both T_{ON} and T_{OFF} in the same way.

Analog Output

The AS5130 can generate a ratiometric analog output voltage by low-pass filtering the PWM output. Figure 19 shows a simple passive 2nd order low pass filter as an example. In order to minimize the ripple on the analog output, the cut-off frequency of the low pass filter should be well below the PWM base frequency.

Figure 19:
Ratiometric Analog Output



Analog Sin/Cos Outputs With External Interpolator

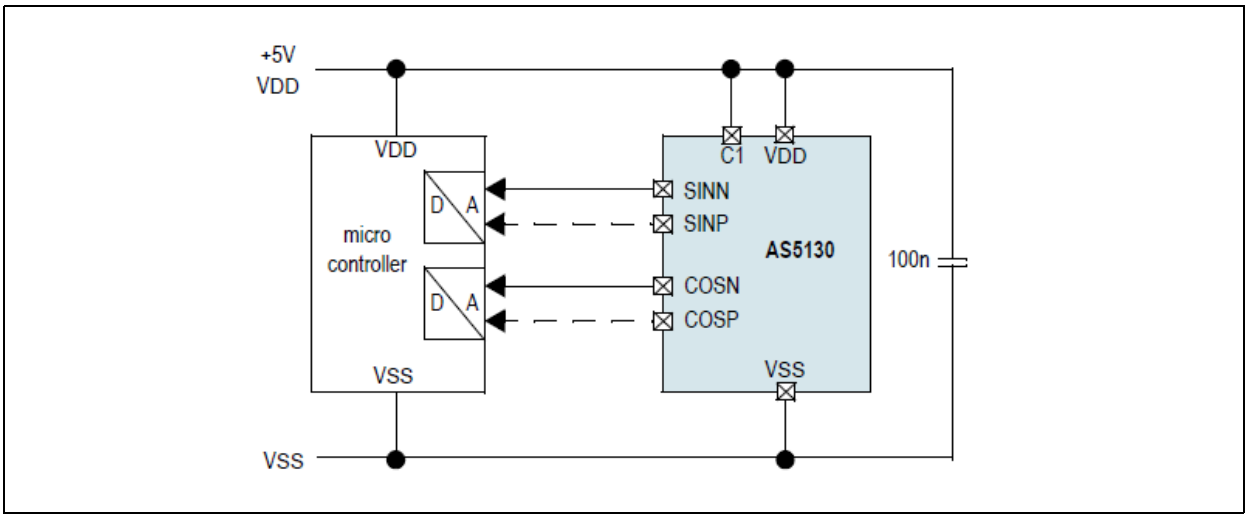
By connecting C1 to V_{DD}, the AS5130 provides analog Sine and Cosine outputs (SINP, COSP) of the Hall array front-end for test purposes. These outputs allow the user to perform the angle calculation by an external ADC + µC, e.g. to compute the angle with a high resolution. In addition, the inverted Sinus and Cosine signals (SINN, COSN; see dotted lines) are available for differential signal transmission.

The input resistance of the receiving amplifier or ADC should be greater than 100kΩ. The signal lines should be kept as short as possible, longer lines should be shielded in order to achieve best noise performance.

The SINN / COSN / SINP / COSP signals are amplitude controlled to ~1.3Vp (differential) by the internal AGC controller. The DC bias voltage is 2.25 V.

If the SINN and COSN outputs cannot be sampled simultaneously, it is recommended to disable the automatic gain control (Figure 21) as the signal amplitudes may be changing between two readings of the external ADC. This may lead to less accurate results.

Figure 20:
Sine and Cosine Outputs for External Angle Calculation



Serial Synchronous Interface (SSI)

Commands of the SSI in Normal Mode

Figure 21:
SSI in Normal Mode

#	Cmd	Bin	Mode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23	WRITE CUST	10111	write	wlsb <6:0>							gain <2:0>			nc					
22	WD2COS	10110	write	xen_7	inv_7	xen_6	inv_6	xen_5	inv_5	xen_4	inv_4	xen_3	inv_3	xen_2	inv_2	xen_1	inv_1	xen_0	inv_0
21	SET TEST CFG1	10101	write						gen_rst										
20	reserved	10100	write																
19	HYST_RST	10011	write	rst_otp	nc	rst_multi	nc	setHyst											
18	WD2SIN	10010	write	xen_7	inv_7	xen_6	inv_6	xen_5	inv_5	xen_4	inv_4	xen_3	inv_3	xen_2	inv_2	xen_1	inv_1	xen_0	inv_0
17	WRITE CONFIG	10001	write	go2sleep															
16	---	10000	write																
7	READ CUST	00111	read	wlsb <6:0>							gain <2:0>			nc					parity
6	RD2COS	00110	read	xen_7	inv_7	xen_6	inv_6	xen_5	inv_5	xen_4	inv_4	xen_3	inv_3	xen_2	inv_2	xen_1	inv_1	xen_0	inv_0
5		00101	read																
4	RD_BOTH	00100	read	Multiturn <7:0>							angle <7:0>								
3	STORE REF	00011	read	store_ok	vdd_ok	reg_set	nc				angle_stored <7:0>								parity

#	Cmd	Bin	Mode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	RD2SIN	00010	read	xen_7	inv_7	xen_6	inv_6	xen_5	inv_5	xen_4	inv_4	xen_3	inv_3	xen_2	inv_2	xen_1	inv_1	xen_0	inv_0
1	RD_MULTI	00001	read	lock	agc <5:0>						Multiturn <7:0>								parity
0	RD_ANGLE	00000	read	lock	agc <5:0>						angle <7:0>								parity

WD2COS / WD2SIN: xen_X disables Hall element X from the sensor array in the cosine or sine channel; xinv_X inverts the voltage output of Hall element X in the channels.

RD2COS / RD2SIN: The Hall array configuration for cosine and sine channel can be read out by these commands, initial values are 0.

SET TEST CFG 1: gen_rst HI triggers a digital reset.

WRITE CONFIG: go2sleep HI activates the low power mode of the AS5130. The power consumption is significantly reduced. go2sleep LO returns to normal operation mode. During low power mode, the lock bit in command 0 and command 1 is LO.

WRITE CUST: With "wlsb_x" the threshold level for generation of a WAKE pulse is set (only important in polling mode). The initial value is 4 LSB. No value lower than 4 LSB can be set. The maximum value is 127 LSB.

"gain_x" sets the gain in the signal.

HYST_RST: "setHyst" enables an additional hysteresis of the digital output signal. It is enabled by default. Only after 2 consecutive equal signals the output is changed.

"rst_otp" forces the IC to read out the OTP in polling mode. This reset has to be performed after initial startup and every WAKE signal.

"rst_multi" resets the multi turn counter to 0.

READ CUST: With this command "wlsb_x" and "gain_x" can be read out.

RD_BOTH: Angle and multi turn counter value can be read out simultaneously by this command. Due to limited data size, the parity bit is not available in this command.

STORE REF: This command stores the actual angle as reference angle in the storage registers (only important in polling mode). The output is the stored angle (angle_stored), a flag, if the voltage at DV_{DD} is OK (store_ok), a flag, if the supply voltage is OK (vdd_ok) and a check bit, if the register was written.

RD_MULTI: Command for read out of multi turn register (multiturn) and AGC value (agc). “Lock” indicates a locked ADC and “parity” an even parity checksum.

RD_ANGLE: Command for read out of angle value and AGC value (agc). “Lock” indicates a locked ADC and “parity” an even parity checksum.

Commands of the SSI in Extended Mode

For programming or readout of the OTP data, the chip has to be started with DV_{DD} at a low voltage (polling mode off or cap discharged) or the OTP reset has to be performed. If not, the OTP is not read out and the OTP data is not available.

Figure 22:
SSI in Extended Mode

#	Cmd	Bin	Mode	<45:44>	<43:32>	<31:28>	<27:26>	<25>	<24:23>	<22:20>	<19:16>	<15:12>	<11:9>	<8>	<7:0>
31	WRITE_ OTP	11111	xt write	OTP Test	ID			OTP lock	VREF	Hall Bias	Osc	Redundancy	Sensitivity	Wake enable	Zero Angle
30		11110	xt write												
29		11101	xt write												
28		11100	xt write												
27		11011	xt write												
26		11010	xt write												
25	PROG_ OTP	11001	xt write	OTP Test	ID			OTP lock	VREF	Hall Bias	Osc	Redundancy	Sensitivity	Wake enable	Zero Angle
24		11000	xt write												
15		01111	xt read	OTP Test	ID			OTP lock	VREF	Hall Bias	Osc	Redundancy	Sensitivity	Wake enable	Zero Angle

#	Cmd	Bin	Mode	<45:44>	<43:32>	<31:28>	<27:26>	<25>	<24:23>	<22:20>	<19:16>	<15:12>	<11:9>	<8>	<7:0>
14		01110	xt read												
13		01101	xt read												
12		01100	xt read												
11		01011	xt read												
10		01010	xt read												
9	RD_OTP_ ANA	01001	xt read												
8		01000	xt read												

WRITE OTP: Writing of the OTP register. The written data is volatile. “Zero Angle” is the angle, which is set for zero position. “Wake enable” enables the polling mode. “Sensitivity” is the gain setting in the signal path. “Redundancy is a number of bits, which allows the customer to overwrite one of the customer OTP bits <0:11>.

PROG_OTP: Programming of the OTP register. Only Bits <0:15> can be programmed by the customer.

RD_OTP: Read out the content of the OTP register. Data written by WRITE_OTP and PROG_OTP is read out.

RD_OTP_ANA: Analog read out mode. The analog value of every OTP bit is available at pin 2 (PROG), which allows for a verification of the fuse process. No data is available at the SSI.

OTP Programming

For programming of the OTP, an additional voltage has to be applied to the pin PROG. It has to be buffered by a fast 100nF capacitor (ceramic) and a 10µF capacitor. The information to be programmed is set by command 25. The OTP bits 16 to 45 are used for ams OSRAM factory trimming and cannot be overwritten.

Figure 23:
OTP Programming Connection

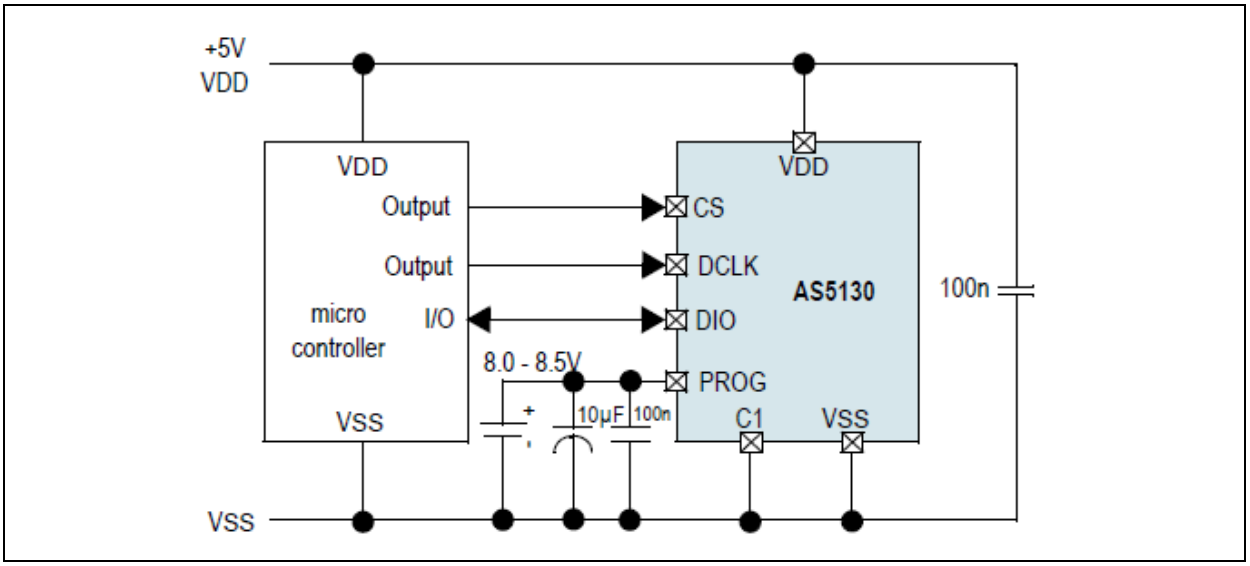


Figure 24:
External Circuitry for OTP Programming

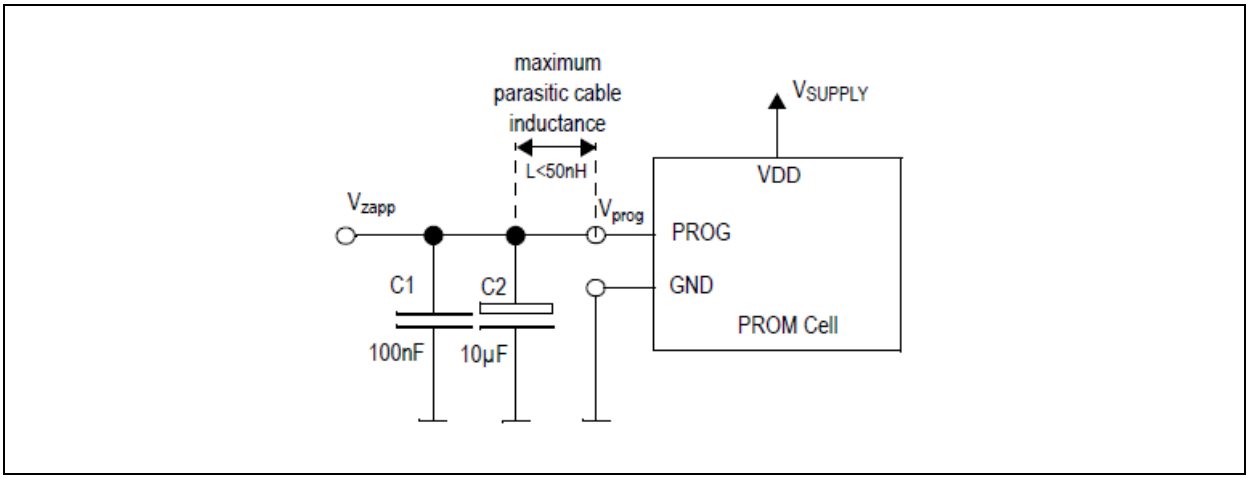


Figure 25:
OTP Programming Parameters

Symbol	Parameter	Min	Max	Unit	Notes
VDD	Supply voltage	5	5.5	V	
GND	Ground level	0	0	V	

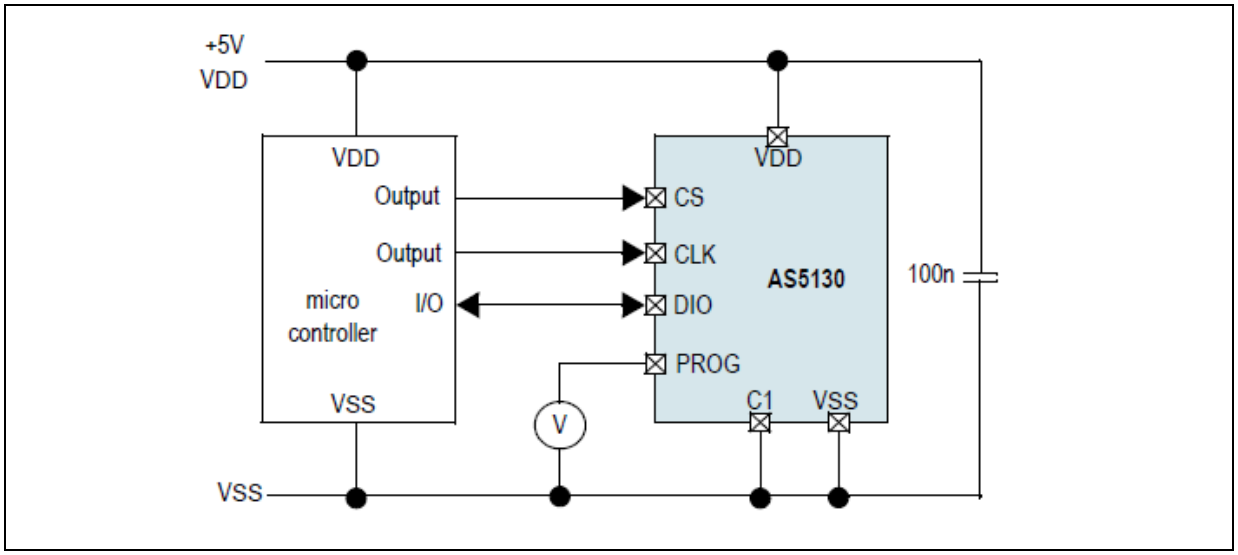
Symbol	Parameter	Min	Max	Unit	Notes
V_zapp	Programming voltage	8	8.5	V	At pin PROG
T_zapp	Temperature	0	85	°C	
f_clk	CLK frequency		100	kHz	At pin DCLK

Programming Verification. After programming, the programmed OTP bits are verified in following two ways:

By Digital Verification: This is simply done by sending a READ OTP command (#0FH, Refer to Figure 22). The structure of this register is the same as for the OTP PROG or OTP WRITE commands.

By Analog Verification: By sending an ANALOG OTP READ command (#09H), pin PROG becomes an output, sending an analog voltage with each clock, representing a sequence of the bits in the OTP register. A voltage of <500mV indicates a correctly programmed bit("1") while a voltage level between 2.2V and 3.5V indicates a correctly unprogrammed bit("0"). Any voltage level in between indicates improper programming.

Figure 26:
Analog OTP Verification



Redundancy Decoding. If a bit is not fused properly (analog readout levels violated), the redundancy bits can be used as shown in the table below. Only one single bit can be overwritten with a logic HI. An improper fusing cannot be made undone.

Figure 27:
Redundancy Bits

<15:12>	Replaced Bit	<15:12>	Replaced Bit
0000	none	1000	7
0001	0	1001	8
0010	1	1010	9
0011	2	1011	10
0100	3	1100	11
0101	4	1101	none
0110	5	1110	none
0111	6	1111	none

Multi Turn Counter

An 8-bit register is used for counting the magnet's revolutions. With each zero transition in any direction, the output of a special counter is incremented or decremented. The initial value after reset is 0 LSB.

The multi turn value is encoded as complement on two. Clockwise rotation gives increasing angle values and positive turn count. Counter clockwise rotation exhibits decreasing angle values and a negative turn count respectively.

Bit Code	Decimal Value
01111111	127
---	---
00000011	+3
00000010	+2
00000001	+1
00000000	0
11111111	-1
11111110	-2
11111101	-3
---	---
10000000	-128

The counter output can be reset by using command 19 – HYST_RST. It is immediately reset by the rising clock edge of this bit. Any zero crossing between the clock edge and the next counter readout changes the counter value.

AS5130 Status Indicators

Lock Status Bit

The Lock signal indicates whether the angle information is valid (ADC locked, Lock = high) or invalid (ADC unlocked, Lock = low). To determine a valid angular signal at best performance, the following indicators should be set:

Lock = 1

0x00h < AGC < 0x2Fh

Note(s): The angle signal may also be valid (Lock = 1), when the AGC is out of range (00H or 2FH), but the accuracy of the AS5130 may be reduced due to the out of range condition of the magnetic field strength.

Magnetic Field Strength Indicators

The AS5130 is not only able to sense the angle of a rotating magnet, it can also measure the magnetic field strength (and hence the vertical distance) of the magnet. This additional feature can be used for several purposes:

- As a safety feature by constantly monitoring the presence and proper vertical distance of the magnet
- As a state-of-health indicator, e.g. for a power-up self test
- As a pushbutton feature for rotate-and-push types of manual input devices

The magnetic field strength information is available in two forms – Magnetic field strength hardware indicator and Magnetic field strength software indicator.

Magnetic Field Strength Hardware Indicator. Pin CAO (#1) will be low, when the magnetic field is too weak. The switching limit is determined by the value of the AGC. If the AGC value is <3FH, the CAO output will be high (green range), If the AGC is at its upper limit (3FH), the CAO output will be low (red range).

Magnetic Field Strength Software Indicator. D13:D7 in the serial data that is obtained by command READ ANGLE (Figure 21) contains the 6-bit AGC information. The AGC is an automatic gain control that adjusts the internal signal amplitude obtained from the Hall elements to a constant level. If the magnetic field is weak, e.g. with a large vertical gap between magnet and IC, with a weak magnet or at elevated temperatures of the magnet, the AGC value will be high. Likewise, the AGC value will be lower when the magnet is closer to the IC, when strong magnets are used and at low temperatures.

The best performance of the AS5130 will be achieved when operating within the AGC range. It will still be operational outside the AGC range, but with reduced performance especially with a weak magnetic field due to increased noise.

Factors Influencing the AGC Value. In practical use, the AGC value will depend on several factors:

- **The initial strength of the magnet.** Aging magnets may show a reducing magnetic field over time which results in an increase of the AGC value. The effect of this phenomenon is relatively small and can easily be compensated by the AGC.
- **The vertical distance of the magnet.** Depending on the mechanical setup and assembly tolerances, there will always be some variation of the vertical distance between magnet and IC over the lifetime of the application using the AS5130. Again, vertical distance variations can be compensated by the AGC.
- **The temperature and material of the magnet.** The recommended magnet for the AS5130 is a diametrically magnetized 6mm diameter magnet. Other magnets may also be used as long as they can maintain to operate the AS5130 within the AGC range. Every magnet has a temperature dependence of the magnetic field strength. The temperature coefficient of a magnet depends on the used material. At elevated temperatures, the magnetic field strength of a magnet is reduced, resulting in an increase of the AGC value. At low temperatures, the magnetic field strength is increased, resulting in a decrease of the AGC value. The variation of magnetic field strength over temperature is automatically compensated by the AGC.

OTP Sensitivity Adjustment. To obtain best performance and tolerance against temperature or vertical distance fluctuations, the AGC value at normal operating temperature should be in the middle between minimum and maximum, hence it should be around 32 (20H). To facilitate the “vertical centering” of the magnet+IC assembly, the sensitivity of the AS5130 can be adjusted in the OTP register in 8 steps (Figure 22). The OTP sensitivity setting corresponds to the customer register setting gain <2:0>.

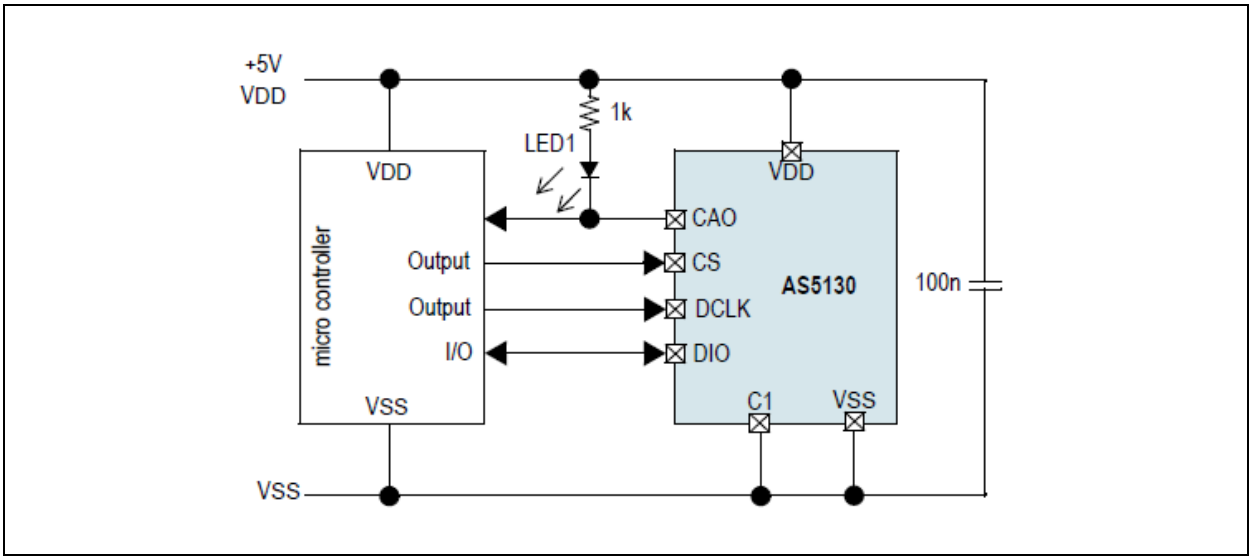
“Pushbutton” Feature

Using the magnetic field strength software and hardware indicators described above, the AS5130 provides a useful method of detecting both rotation and vertical distance simultaneously. This is especially useful in applications implementing a rotate-and-push type of human interface (e.g. in panel knobs and switches).

The CAO output is low, when the magnetic field is below the low limit (weak or no magnet) and high when the magnetic field is above the low limit (in-range or strong magnet).

A finer detection of a vertical distance change, for example when only short vertical strokes are made by the pushbutton, is achieved by memorizing the AGC value in normal operation and triggering on a change from that nominal the AGC value to detect a vertical movement.

Figure 28:
Magnetic Field Strength Indicator



High Speed Operation

The AS5130 is using a fast tracking ADC (TADC) to determine the angle of the magnet. The TADC has a tracking rate of 1.15µs (typ).

Once the TADC is synchronized with the angle, it sets the LOCK bit in the status register (Figure 21). In worst case, usually at start-up, the TADC requires a maximum of 127 steps (127 * 1.15µs = 146.05µs) to lock. Once it is locked, it requires only one cycle (1.15µs) to track the moving magnet.

The AS5130 can operate in locked mode at rotational speeds up to 30,000 rpm.

In Low Power Mode, the position of the TADC is frozen. It will continue from the frozen position once it is powered up again. If the magnet has moved during the power down phase, several cycles will be required before the TADC is locked again. The tracking time to lock in with the new magnet angle can be roughly calculated as:

(EQ3) $$t_{LOCK} = 1.15\mu s * |NewPos - OldPos|$$

Where:

t_{LOCK} = time required to acquire the new angle after power up from one of the reduced power modes [µs]

OldPos = Angle position when one of the reduced power modes is activated [°]

NewPos = Angle position after resuming from reduced power mode [°]

Propagation Delay

The Propagation delay is the time required from reading the magnetic field by the Hall sensors to calculating the angle and making it available on the serial or PWM interface. While the propagation delay is usually negligible on low speeds, it is an important parameter at high speeds. The longer the propagation delay, the larger becomes the angle error for a rotating magnet as the magnet is moving while the angle is calculated. The position error increases linearly with speed. The main factors that contribute to the propagation delay are discussed in detail further in this document.

Sampling Rate

For high speed applications, fast ADCs are essential. The ADC sampling rate directly influences the propagation delay. The fast tracking ADC used in the AS5130 with a tracking rate of only 1.15µs (typ) is a perfect fit for both high speed and high performance.

Chip Internal Lowpass Filtering

A commonplace practice for systems using analog-to-digital converters is to filter the input signal by an anti-aliasing filter. The filter characteristic must be chosen carefully to balance propagation delay and noise. The lowpass filter in the AS5130 has a cutoff frequency of typ. 23.8kHz and the overall propagation delay in the analog signal path is typ. 15.6µs.

Digital Readout Rate

Aside from the chip-internal propagation delay, the time required to read and process the angle data must also be considered. Due to its nature, a PWM signal is not very usable at high speeds, as you get only one reading per PWM period. Increasing the PWM frequency may improve the situation but causes problems for the receiving controller to resolve the PWM steps. The frequency on the AS5130 PWM output is typ. 1.95kHz with a resolution of 2µs/step. A more suitable approach for high speed absolute angle measurement is using the serial interface. With a clock rate of up to 6MHz, a complete set of data (21-bits) can be read in >3.5µs.

Total Propagation Delay of the AS5130

The total propagation delay of the AS5130 is the delay in the analog signal path and the tracking rate of the ADC:

(EQ4) $$15.6\mu S + 1.15\mu S = 16.75\mu S$$

If only the SIN-/COS-outputs are used, the propagation delay is the analog signal path delay only (typ. 15.6µs).

Position Error Over Speed: The angle error over speed caused by the propagation delay is calculated as:

(EQ5) $$\Delta\theta_{pd} = rpm*6*16.75E^{-6}\ in\ degrees$$

In addition, the anti-aliasing filter causes an angle error calculated as:

(EQ6) $$\Delta\theta_{lpf} = ArcTan[rpm/(60*f0)]$$

Figure 29:
Examples of the Overall Position Error Caused by Speed (Includes Both Propagation Delay and Filter Delay)

Speed (rpm)	Total Position Error ($\Delta\theta_{pd}$ + $\Delta\theta_{lpf}$)
100	0.0175°
1000	0.175°
10000	1.75°

Reduced Power Modes

The AS5130 can be operated in three reduced power modes. All three modes have in common that they switch off or freeze parts of the chip during intervals between measurements. In Low Power Mode or Ultra Low Power Mode, the AS5130 is not operational, but due to the fast start-up, an angle measurement can be accomplished very quickly and the chip can be switched to reduced power immediately after a valid measurement has been taken. Depending on the intervals between measurements, very low average power consumption can be achieved using such a strobed measurement mode.

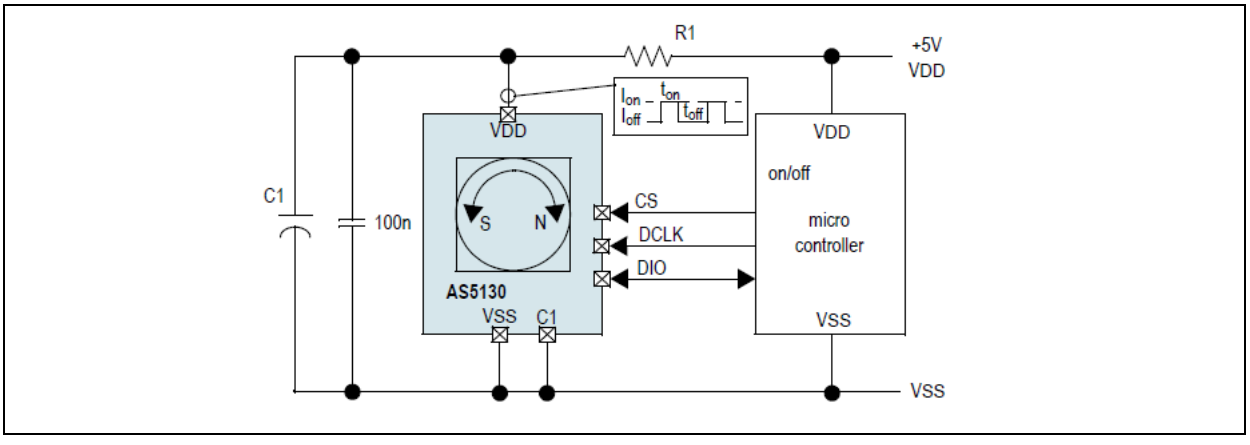
- Low Power Mode: reduced current consumption, very fast start-up. Ideal for short sampling intervals (<3ms).
- Power Cycling Mode: zero power consumption (externally switched off) during sampling intervals, but slower start-up than Polling Mode. Ideal for sampling intervals 200ms.
- Polling Mode: for reduction of the average power consumption; especially suited for battery powered applications.

Low Power Mode

The AS5130 can be put in Low Power Mode by simple serial commands, using the regular SSI commands. The required serial command is WRITE CONFIG (17H,Figure 10). The angle data is valid, as soon as the LOCK- Flag is 1(Figure 21).

In Reduced Power Modes, the AS5130 is inactive. The last state, e.g. the angle, AGC value, etc. is frozen and the chip starts from this frozen state when it resumes active operation. This method provides much faster start-up than a "cold start" from zero.

Figure 30:
Low Power Mode and Ultra Low Power Mode Connection



If the AS5130 is cycled between active and reduced current mode, a substantial reduction of the average supply current can be achieved. The minimum dwelling time in active mode is the wake-up time. The actual active time depends on how much the magnet has moved while the AS5130 was in reduced power mode. The angle data is valid, when the status bit LOCK has

been set (Figure 21). Once a valid angle has been measured, the AS5130 can be put back to reduced power mode. The average power consumption can be calculated as:

(EQ7)
$$I_{avg} = \frac{I_{active} * t_{on} + I_{powerdown} * t_{off}}{t_{on} + t_{off}}$$

$$sampling\ interval = t_{on} + t_{off}$$

Where:

I_{avg} = Average current consumption

I_{active} = Current consumption in active mode

I_{power_down} = Current consumption in reduced power mode

t_{on} = Time period during which the chip is operated in active mode

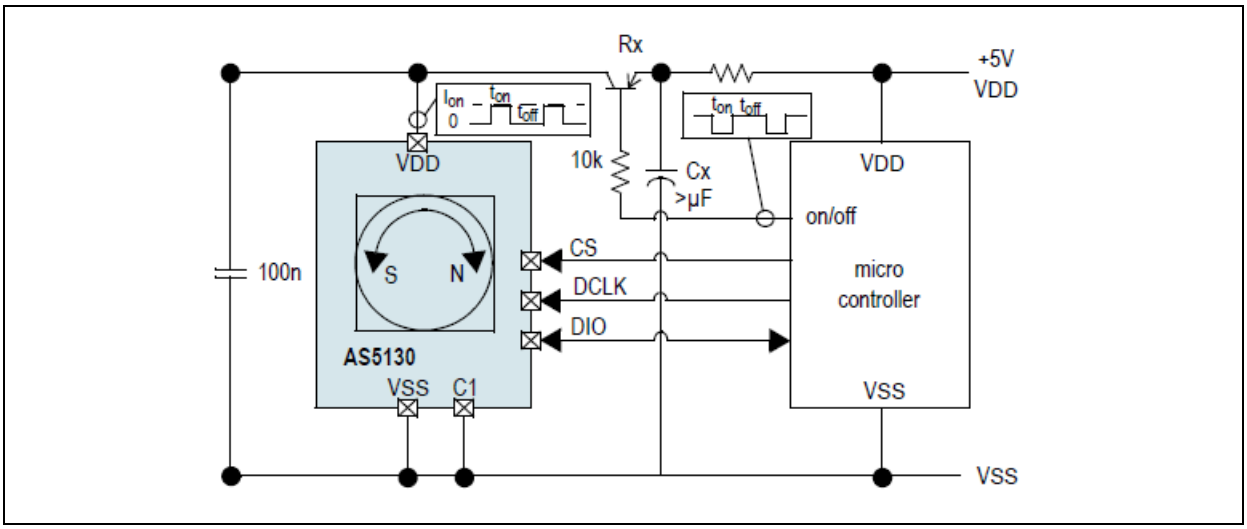
t_{off} = Time period during which the chip is in reduced power mode

Reducing Power Supply Peak Currents. An optional RC-filter (Rx/Cx) may be added to avoid peak currents in the power supply line when the AS5130 is toggled between active and reduced power mode. Rx must be chosen such that it can maintain a VDD voltage of 4.5 – 5.5V under all conditions, especially during long active periods when the charge on Cx has expired. Cx should be chosen such that it can support peak currents during the active operation period. For long active periods, Cx should be large and Rx should be small.

Power Cycling Mode

The power cycling method shown in Figure 31 cycles the AS5130 by switching it on and off, using an external PNP transistor high side switch. The current consumption in off-mode is zero. It also has the longest start-up time of all modes, as the chip must always perform a "cold start" from zero, which takes about 2ms (Compare with Low Power Mode).

Figure 31:
Power Cycling Mode

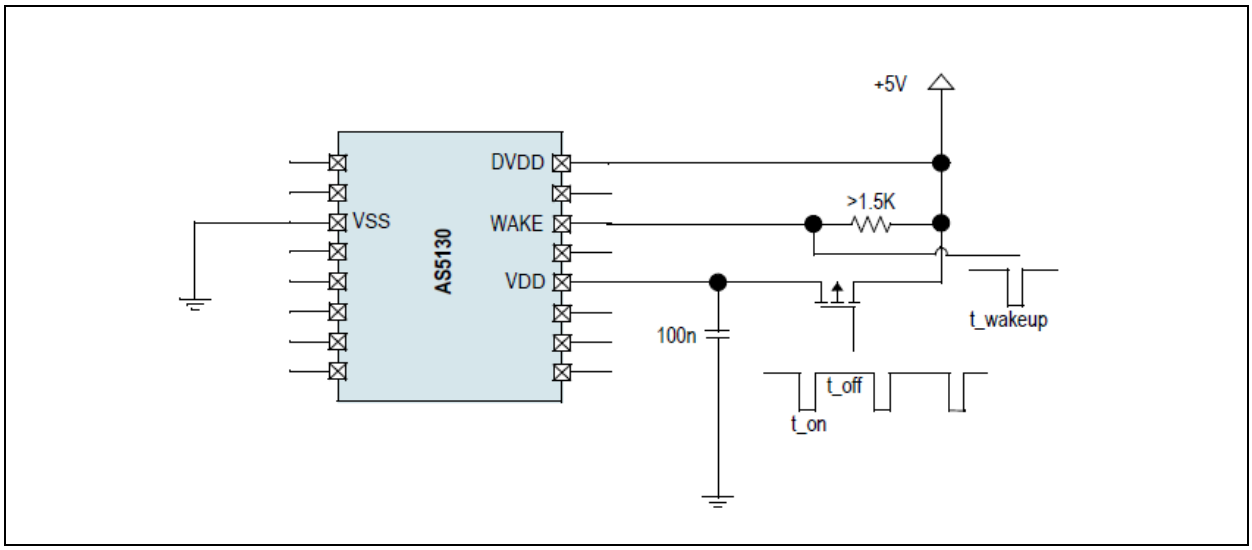


The optional filter Rx/Cx may again be added to reduce peak currents in the 5V power supply line (see Reducing Power Supply Peak Currents).

Polling Mode

Target of this mode is a reduction of the average power consumption. In this mode, the IC supply is pulsed, thereby reducing the average power consumption to a fraction. The actual angle information and multi turn count value is not lost; polling mode is especially suited for battery powered applications. The IC is furthermore capable of generating a WAKE signal as soon as the magnet's position has changed, but only if the supply of the IC is powered-on again. By means of the WAKE signal, the system's power consumption can be further decreased, if certain modules are activated on demand.

Figure 32:
External Circuitry for Polling Mode



The voltage at pin 16 (DV_{DD}) determines whether polling mode is activated or not. Any voltage above 3.6V activates the polling functionality.This voltage must always be present at DV_{DD} in order to hold the information in the registers.

The procedure is as follows:

1. Initial startup: The circuit starts up with invalid trim values, which are read back from the storage registers; the command rst_otp (command 19 – 10011) must be sent to read out valid trim values from the OTP.
2. These values are copied to the storage registers if OTP<8> (Wake enable) is set (must be set for polling mode).
3. The values of AGC counter, actual angle, multi turn counter, hysteresis setting, wake threshold and gain setting are continuously updated in the storage registers.
4. The actual angle is stored as a reference by sending command STORE REF (command 3 – 00011). Without this reference angle, a WAKE is generated at every startup.

5. The update of the storage registers is stopped if V_{DD} drops below 4.45V and then the information is stored (DV_{DD}) at the next startup (V_{DD} on), the values are read back from the storage registers and the measured angle is compared with the stored reference angle; if the difference between both exceeds the threshold, a WAKE pulse is generated.

Figure 33:
Wake Up Signal Flowchart

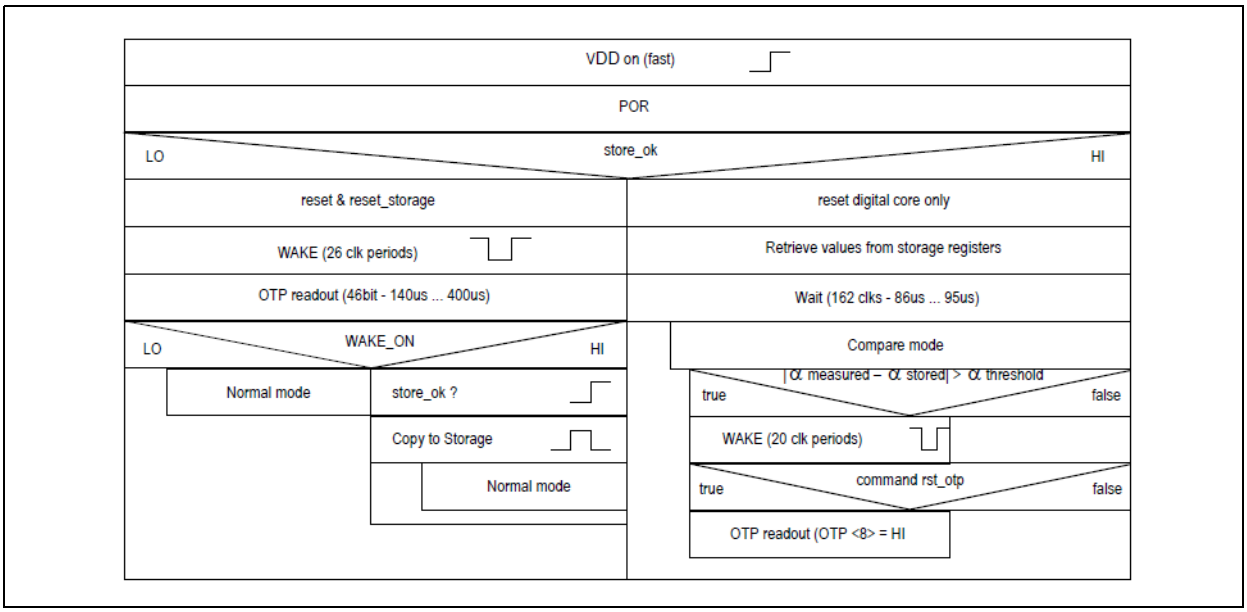


Figure 36 shows the behavior of the wake up signal. The wake up signal will be low for t_{wakeup} = 10µs. After that, the wake up signal will go to tristate condition. In case of an angle comparison with a result below the threshold, the signal will remain in tri-state condition. After switching on VDD, the system needs max. 250µs to generate an angle with maximum accuracy. A WAKE signal cannot be expected until the end of this period.

WAKE Interface. An open drain NMOS structure is used in the WAKE pad. In order to generate a clear output signal level, a pull up resistor is required. The pad can drive 4mA.

Figure 34:
WAKE Output Pin

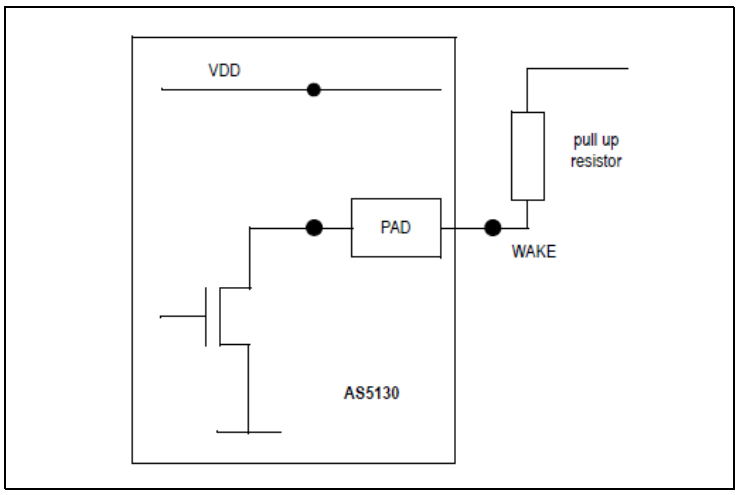
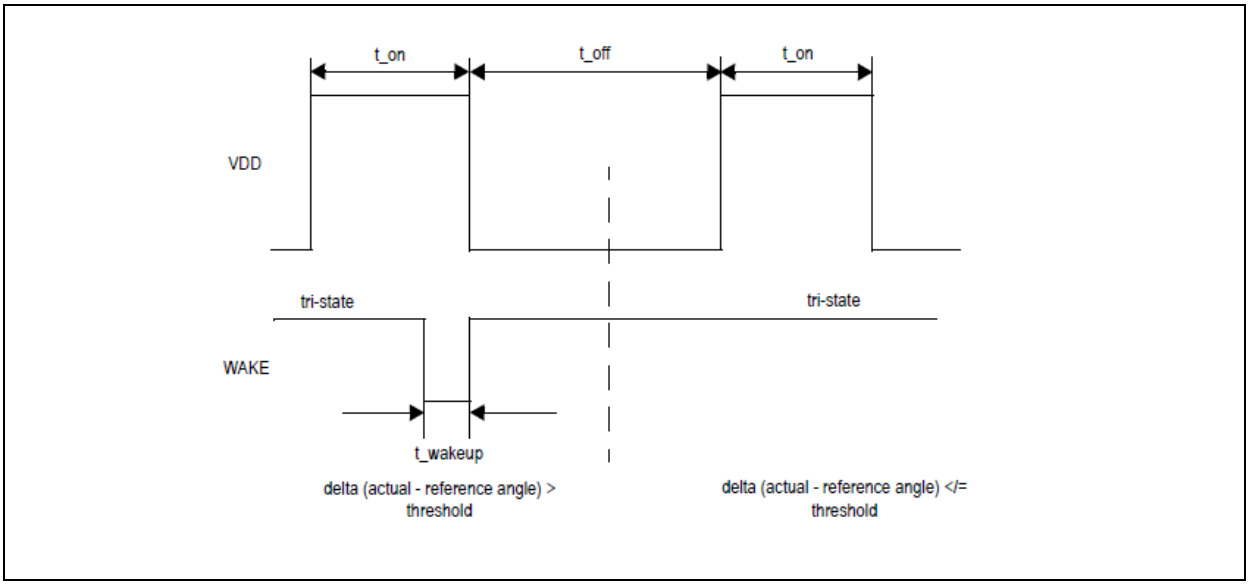


Figure 35:
WAKE Interface Parameters

Symbol	Parameter	Min	Max	Unit	Notes
R_{pull_up}	Pull up resistor	1.5	100	kΩ	The used pad can drive 4mA.
$t_{wake\ up}$	Wake up pulse	10	17	µs	Interrupt signal to external devices, tri-state output, low active.
t_{on}	On-time	250	---	µs	Time for power up in polling mode.
t_{off}	Off-time	---	---	ms	No limit unless DV_{DD} is always supplied.

Figure 36:
Wake Up Signal During Polling Mode of VDD



Application Information

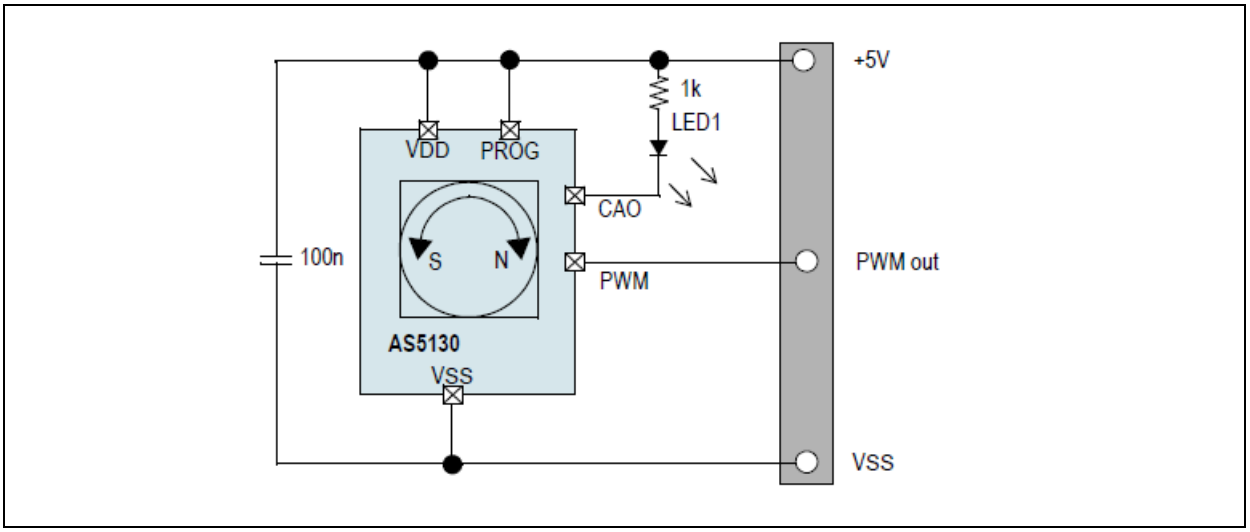
Benefits of AS5130 are as following:

- Complete system-on-chip
- Flexible system solution providing absolute angle position, with serial data and PWM output
- Ideal for applications in harsh environments due to magnetic sensing principle
- High reliability due to non-contact sensing
- Robust system, tolerant to misalignment, airgap variations, temperature variations and external magnetic fields

Application Example I: 3-Wire Sensor With Magnetic Field Strength Indication

In Figure 37, a simple 360° sensor with PWM output is shown. The complete application requires only three wires, VDD, VSS and the PWM output. The circle over the center of the chip represents the diametrically polarized magnet. Additionally, the CAO pin will deliver an analog voltage indicating a missing magnetic field. This signal could be used to drive an external LED or to detect an alert signal.

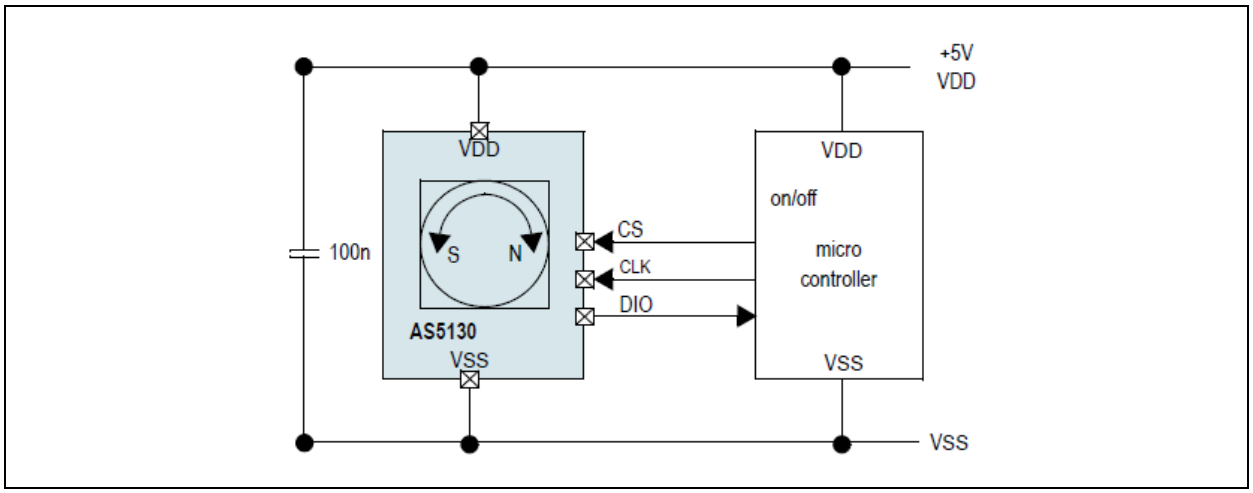
Figure 37:
3-Wire Angle Sensor



Application Example II: Low-Power Encoder

Via SSI, the AS5130 will be able to toggle between active mode and low power mode. In active mode, the current consumption is ~15mA and in low power mode 2mA. The fastest possible startup time from low power mode is 150µs. The AS5130 can be periodically switched between active and low power mode, the average power consumption depends on the duty cycle. In order to read out the correct data, the active mode time must be larger than 150µs.

Figure 38:
Low Power Encoder



(EQ8) $$I_{avg} = \frac{I_{active} * t_{on} + I_{powerdown} * t_{off}}{t_{on} + t_{off}}$$

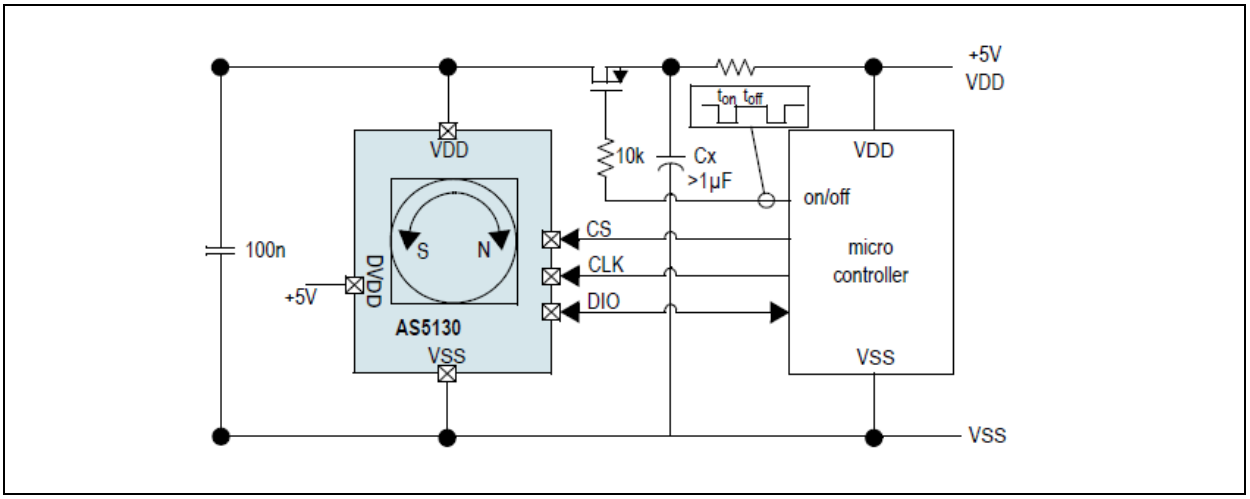
Example: sampling period = one measurement every 10ms.

System constants = I_{active} = 15mA, I_{power_down} = 2mA, t_{off} = 9.85ms, t_{on}(min) = 150µs (start-up from low power mode):

(EQ9) $$I_{avg} = \frac{15mA * 150\mu s + 2mA * 9.85ms}{150\mu s + 9.85ms} = 2.195mA$$

Application Example III: Polling Mode

Figure 39:
Polling Mode



Once powered up for at least 2.5ms, the AS5130 can be operated in a pulsed mode, where it is periodically turned on/off by a high side FET (PMOS) switching transistor with a low Ron (<10Ω). The on-time is at least 250µs in order to perform one measurement. A valid measurement result can be verified by checking the lock bit (ADC is locked) in the serial data stream.

After startup an OTP reset has to be performed in order to read out valid trimming information. Then a special SSI command (STORE REF) copies the actual angle into a buffered reference angle register. Now the AS5130 can be turned off. Special registers will be buffered by the low power supply and will keep the actual settings. After a t_{on} of min. 250µs, the actual angle is compared with the stored reference angle. If the angle. If the angle difference is larger than a threshold value (wlsb, SSI command WRITE CUST), the AS5130 will send an interrupt request to an external device via the WAKE pin.

Due to the internal POR level of the IC, t_{on} starts after VDD has reached 4.3V (worst case POR level). The average power consumption in this pulsed mode depends on the supply current in active mode and the duty cycle of the on/off pulse:

(EQ10)
$$I_{avg} = \frac{I_{active} * t_{on}}{t_{on} + t_{off}}$$

Example: Sampling period = one measurement every 100ms. System constants = I_{active} = 19mA, t_{on}(min) = 250µs:

(EQ11)
$$I_{avg} = \frac{19mA * 250\mu s}{250\mu s + 99.75ms} = 47.5\mu A$$

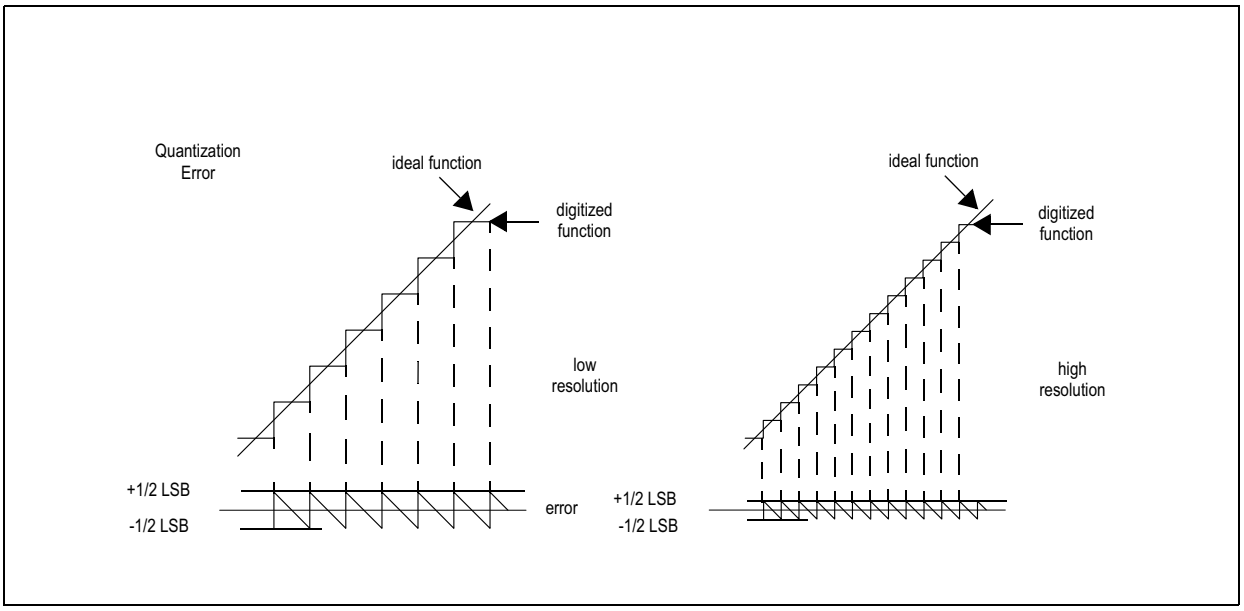
Accuracy of the Encoder System

This section enlightens on the individual factors that influence the accuracy of the encoder system, and provides techniques to improve them. Accuracy is defined as the difference between measured angle and actual angle. This is not to be confused with resolution, which is the smallest step that the system can resolve. The two parameters are not necessarily linked together. A high resolution encoder may not necessarily be highly accurate as well.

Quantization Error

There is however a direct link between resolution and accuracy, which is the quantization error:

Figure 40:
Quantization Error of a Low Resolution and a High Resolution System



The resolution of the encoder determines the smallest step size. The angle error caused by quantization cannot get better than ±½ LSB. As shown in Figure 40, a higher resolution system (right picture) has a smaller quantization error, as the step size is smaller. For the AS5130, the quantization error is ± ½ LSB = ± 0.7°.

Figure 41:
Typical INL Error Over 360°

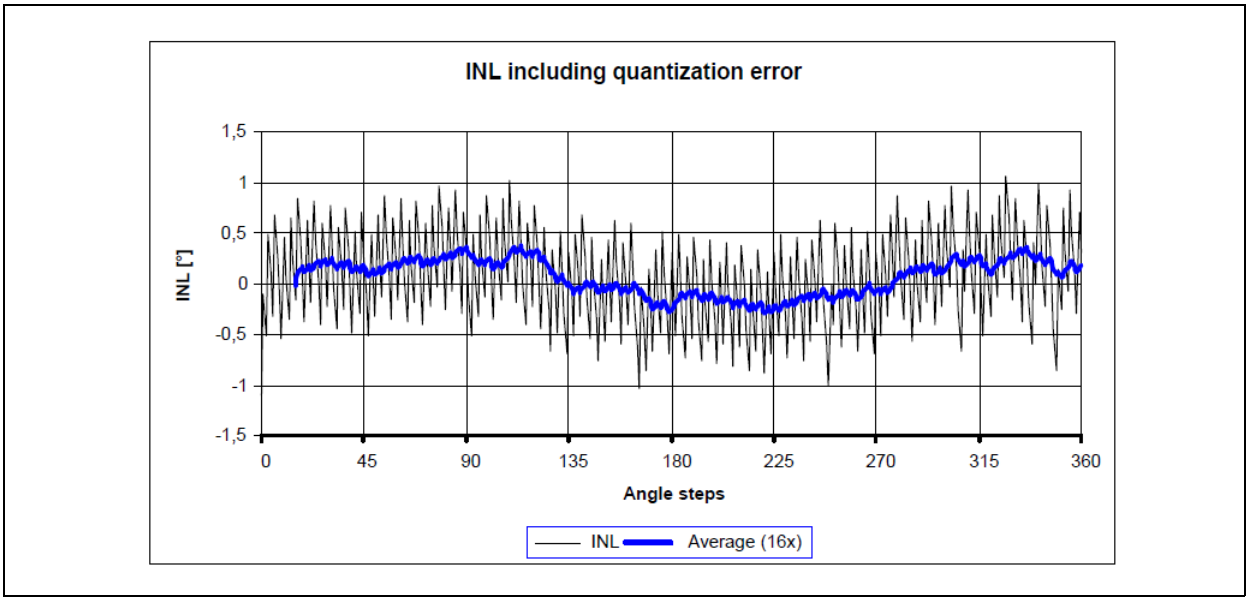


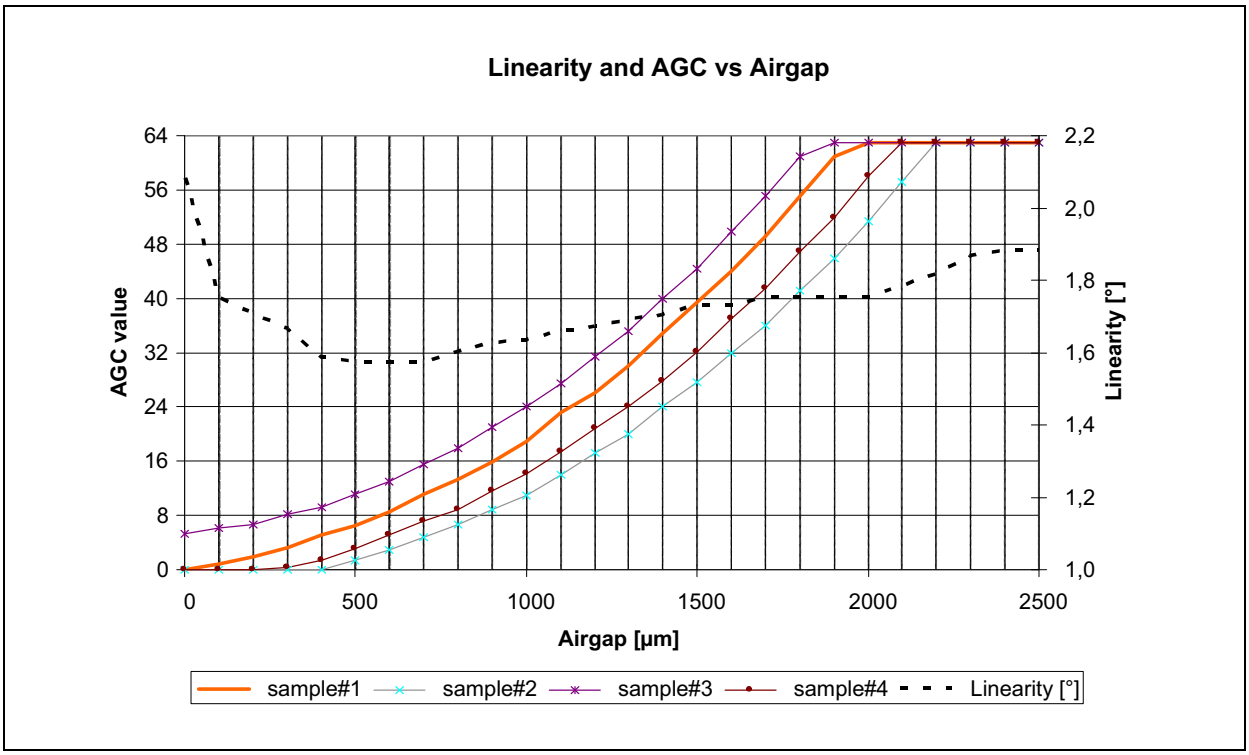
Figure 41 shows a typical example of an error curve over a full turn of 360° at a given X-Y- displacement. The curve includes the quantization error, transition noise and the system error. The total error is ~2.2° peak/peak (+/-1.1°).

The sawtooth-like quantization error (Figure 40) can be reduced by averaging, provided that the magnet is in constant motion and there are an adequate number of samples available. The solid bold line in Figure 41 shows the moving average of 16 samples. The INL (intrinsic non-linearity) is reduced to from ~+/- 1.1° down to ~ +/-0.3°. The averaging however, also increases the total propagation delay, therefore it may be considered for low speeds only or adaptive; depending on speed (see Position Error Over Speed).

Vertical Distance of the Magnet

The chip-internal automatic gain control (AGC) regulates the input signal amplitude for the tracking-ADC to a constant value. This improves the accuracy of the encoder and enhances the tolerance for the vertical distance of the magnet.

Figure 42:
Typical Curves for Vertical Distance Versus ACG Value on Several Untrimmed Samples



As shown in Figure 42, the AGC value (left Y-axis) increases with vertical distance of the magnet. Consequently, it is a good indicator for determining the vertical position of the magnet, for example as a pushbutton feature, as an indicator for a defective magnet or as a preventive warning (e.g. for wear on a ball bearing etc.) when the nominal AGC value drifts away. If the magnet is too close or the magnetic field is too strong, the AGC will be reading 0. If the magnet is too far away (or missing) or if the magnetic field is too weak, the AGC will be reading 63 (3FH).

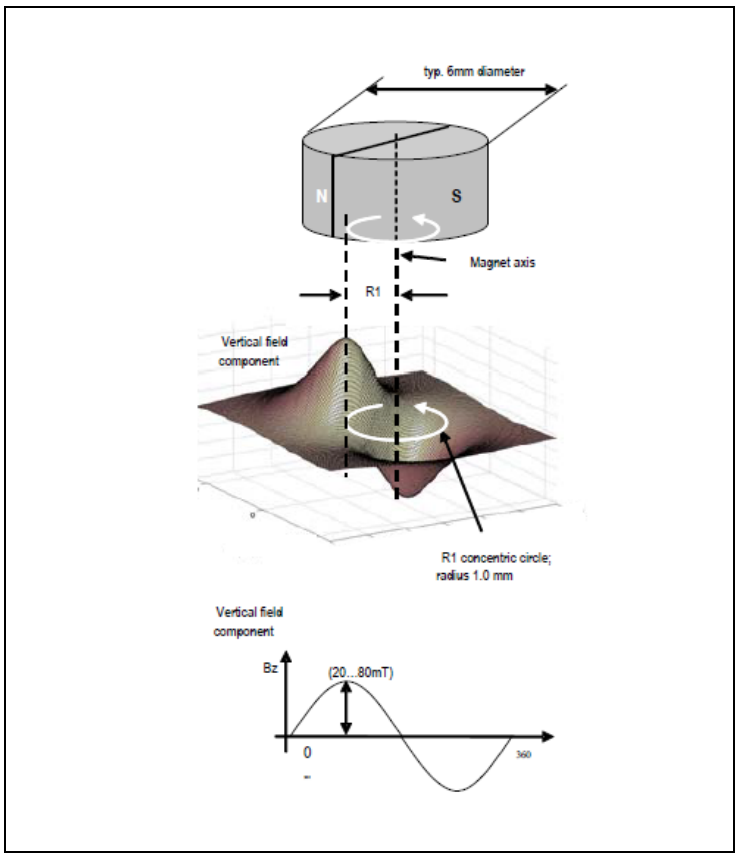
The AS5130 will still operate outside the AGC range, but the accuracy may be reduced as the signal amplitude can no longer be kept at a constant level. The linearity curve in Figure 42 (right Y-axis) shows that the accuracy of the AS5130 is best within the AGC range, even slightly better at small airgaps (0.4 – 0.8mm). At very short distances (0 – 0.1) the accuracy is reduced, mainly due to nonlinearities in the magnetic field. At larger distances, outside the AGC range (~2.0 – 2.5mm and more) the accuracy is still very good, only slightly decreased from the nominal accuracy. Since the field strength of a magnet changes with temperature, the AGC will also change when the temperature of the magnet changes. At low temperatures, the magnetic field

will be stronger and the AGC value will decrease. At elevated temperatures, the magnetic field will be weaker and the AGC value will increase.

Choosing the Proper Magnet

There is no strict requirement on the type or shape of the magnet to be used with the AS5130. It can be cylindrical as well as square in shape. The key parameter is that the vertical magnetic field B_Z measured at a radius of 1mm from the rotation axis is sinusoidal with a peak amplitude of 20mT to 80mT (Figure 43).

Figure 43:
Vertical Magnetic Fields of a Rotating Magnet



Magnet Placement

Ideally, the center of the magnet, the diagonal center of the IC and the rotation axis of the magnet should be in one vertical line. The lateral displacement of the magnet should be within ±0.25mm from the IC package center or +/-0.5mm from the IC center, including the placement of the chip within the IC package. The vertical distance should be chosen such that the magnetic field on the die surface is within the specified limits. The typical distance "z" between the magnet and the package surface is 0.5mm to 1.8mm with the recommended magnet (6mm × 2.5mm). Larger gaps are possible, as long as the required magnetic field strength stays within the defined limits. A magnetic field outside the specified range may still produce acceptable results, but with reduced accuracy. The out-of-range condition will be indicated, when the AGC is at the limits (AGC= 0: field too strong; AGC=63=($3F_H$): field too weak or missing magnet).

Figure 44:
B_z Field Distribution Along the X-axis of a 6mm ϕ Diametric Magnetized Magnet

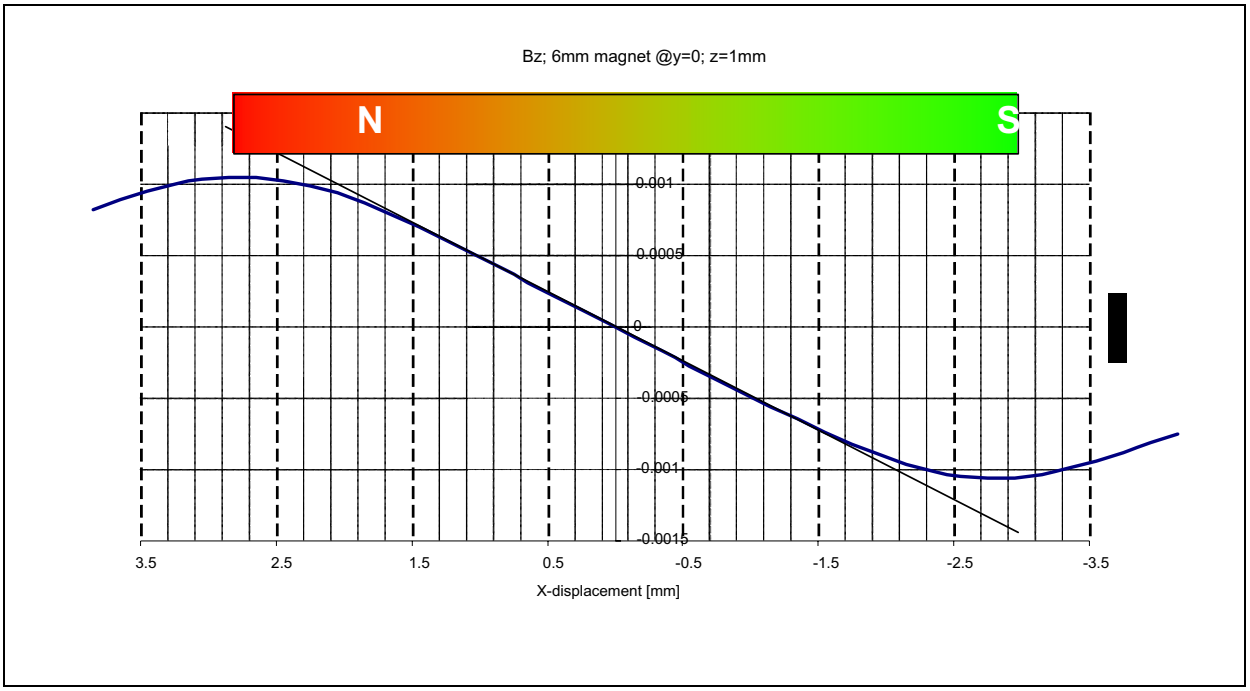


Figure 44 shows a cross sectional view of the vertical magnetic field component B_z between the north and south pole of a 6mm diameter magnet, measured at a vertical distance of 1mm. The poles of the magnet (maximum level) are about 2.8mm from the magnet center, which is almost at the outer magnet edges. The magnetic field reaches a peak amplitude of ~±106mT at the poles.The Hall elements are located at a radius of 1mm (indicated as squares at the bottom of the graph). Due to the side view, the two Hall elements at the Y-axis are overlapping at X=0mm, therefore only 3 Hall elements are shown. At 1mm radius, the peak amplitude is ~±46mT, respectively a differential amplitude of 92mT. The vertical magnetic field B_z follows a fairly

linear pattern up to about 1.5mm radius. Consequently, even if the magnet is not perfectly centered, the differential amplitude will be the same as for a centered magnet.

For example, if the magnet is misaligned in X-axis by -0.5mm, the two X-Hall sensors will measure 70mT (@ x = -1.5mm) and -22mT (@ x = - 0.5mm). Again, the differential amplitude is 92mT. At larger displacements however, the B_z amplitude becomes nonlinear, which results in larger errors that mainly affect the accuracy of the system (see Figure 46).

Figure 45:
Vertical Magnetic Field Distribution of a Cylindrical 6mm Ø Diametric Magnetized Magnet at 1mm Gap

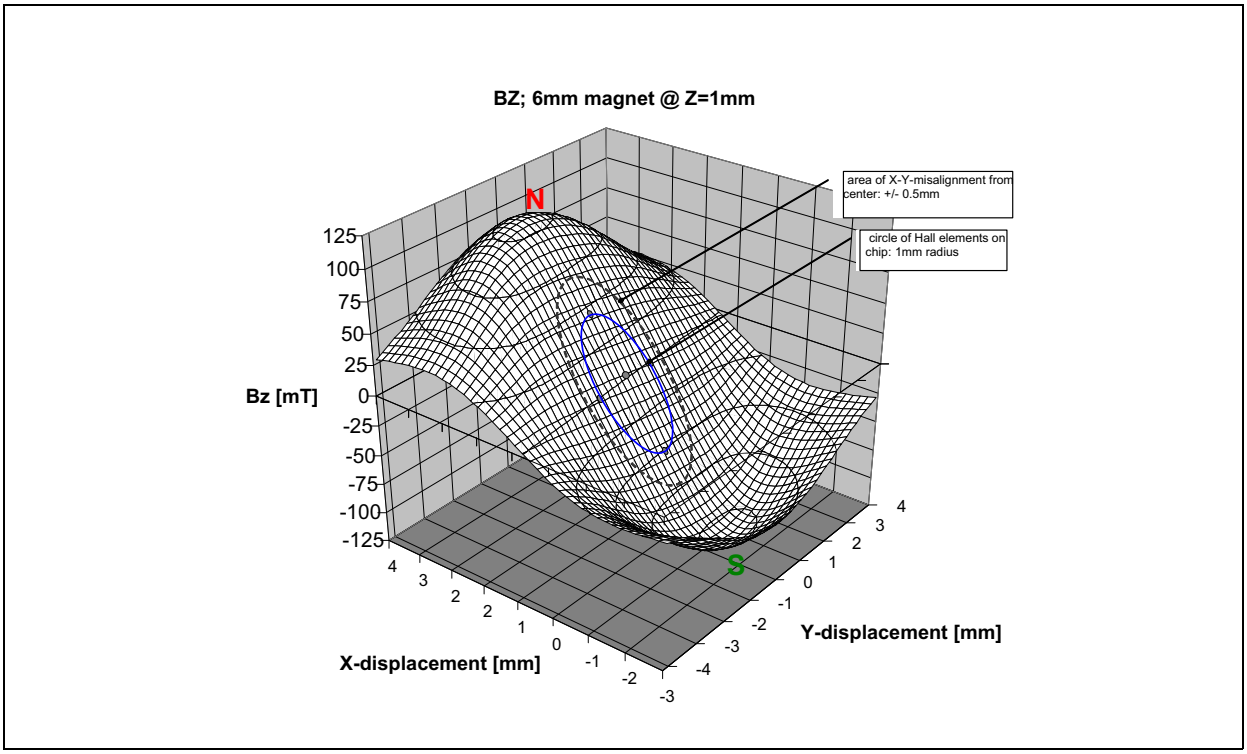


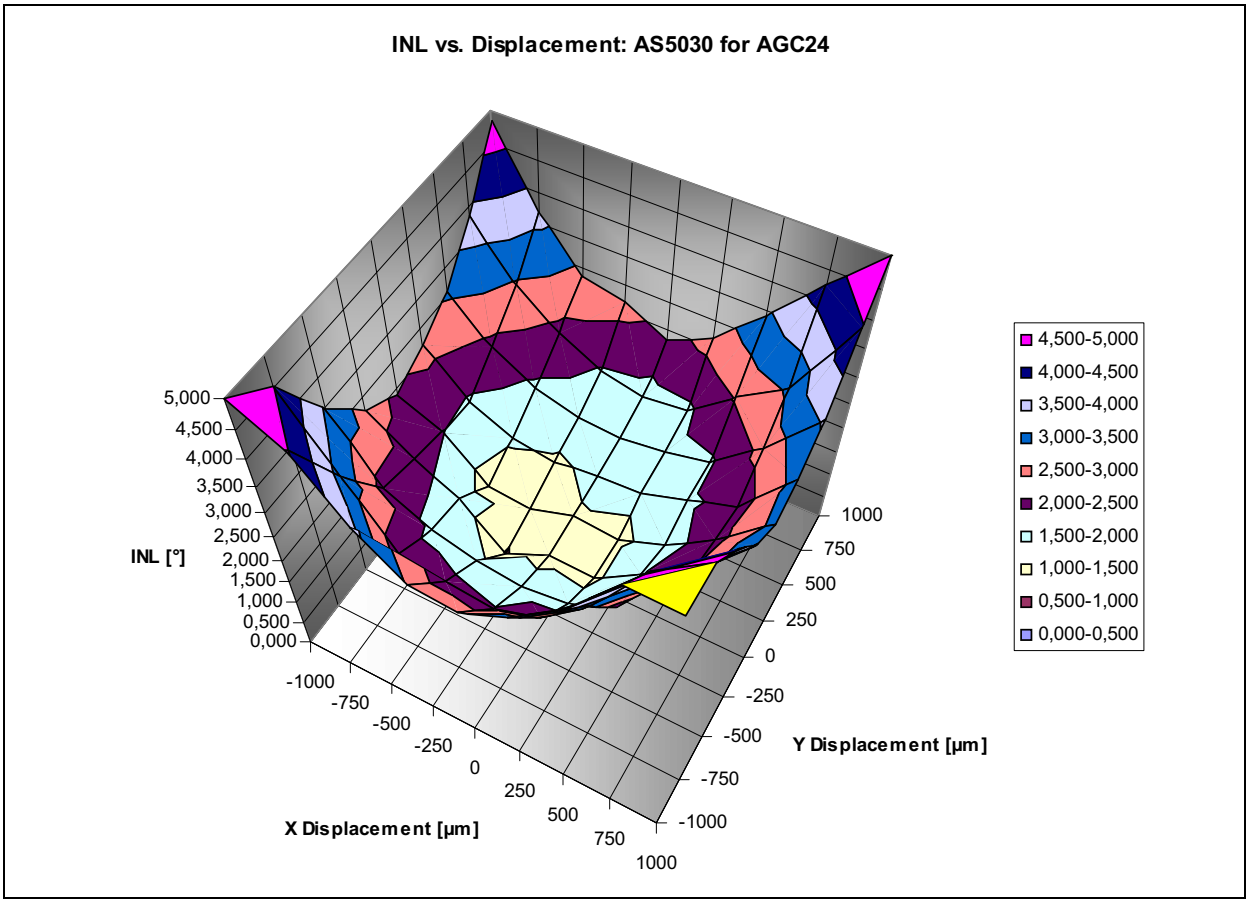
Figure 45 shows the same vertical field component Figure 44, but in a 3-dimensional view over an area of ±4mm from the rotational axis.

Lateral Displacement of the Magnet

As shown in the magnet specifications (see Parameters for Magnet under Electrical Characteristics), the recommended horizontal position of the magnet axis with respect to the IC package center is within a circle of 0.25mm radius. This includes the placement tolerance of the IC within the package.

Figure 46 shows a typical error curve at a medium vertical distance of the magnet around 1.2mm (AGC = 24). The X- and Y- axis of the graph indicate the lateral displacement of the magnet center with respect to the IC center. At X=Y=0, the magnet is perfectly centered over the IC. The total displacement plotted on the graph is for ±1mm in both directions. The Z-axis displays the worst case INL error over a full turn at each given X-and Y- displacement. The error includes the quantization error of ±0.7° (refer to Quantization Error). For example, the accuracy for a centered magnet is between 1.0 – 1.5° (spec = 2° over full temperature range). Within a radius of 0.5mm, the accuracy is better than 2.0° (spec = 3° over temperature).

Figure 46:
Typical Error Curve of INL Error Over Lateral Displacement (Including Quantization Error)



Magnet Size

Figure 44 to Figure 46 illustrate a cylindrical magnet with a diameter of 6mm. Smaller magnets may also be used, but since the poles are closer together, the linear range will also be smaller and consequently the tolerance for lateral misalignment will also be smaller.

If the ±0.25mm lateral misalignment radius (rotation axis to IC package center) is too tight, a larger magnet can be used. Larger magnets have a larger linear range and allow more misalignment. However at the same time the slope of the magnet is more flat, which results in a lower differential amplitude. This requires either a stronger magnet or a smaller gap between IC and magnet in order to operate in the amplitude controlled area (AGC > 0 and AGC < 63).

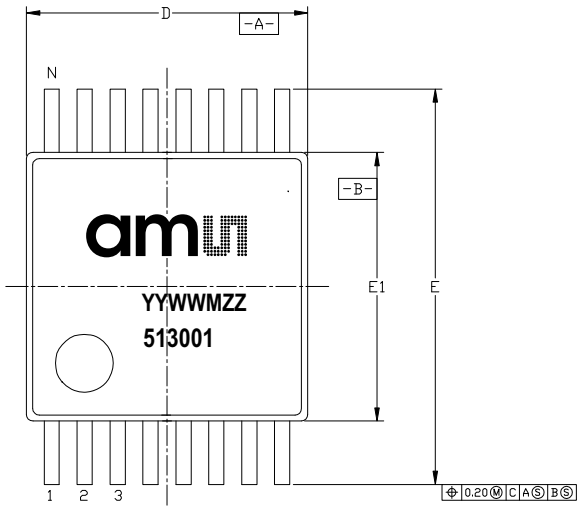
In any case, if a magnet other than the recommended 6mm diameter magnet is used, two parameters should be verified:

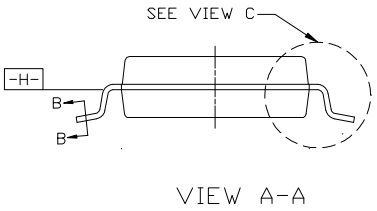
- Verify, that the magnetic field produces a sinusoidal wave, when the magnet is rotated. Note that this can be done with the SIN-/COS- outputs of the AS5130; e.g. rotate the magnet at constant speed and analyze the SIN- (or COS-) output with an FFT-analyzer. It is recommended to disable the AGC for this test Analog Sin/Cos Outputs With External Interpolator).
- Verify that the B_z-Curve between the poles is as linear as possible (Figure 44). This curve may be available from the magnet supplier(s). Alternatively, the SIN- or COS- output of the AS5130 may also be used together with an X-Y- table to get a B_z-scan of the magnet (as in Figure 44 or Figure 45). Furthermore, the sine wave tests described above may be re-run at defined X-and Y- misplacements of the magnet to determine the maximum acceptable lateral displacement range. It is recommended to disable the AGC for both these tests (Analog Sin/Cos Outputs With External Interpolator).

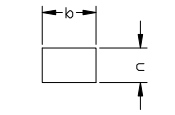
Note(s): For preferred magnet suppliers, please refer to the ams website (Position Sensors section).

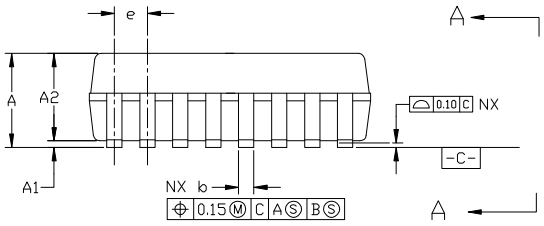
Package Drawings & Markings

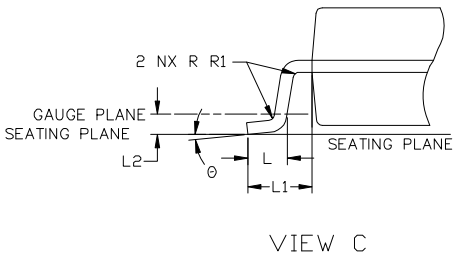
Figure 47:
Package Drawings and Dimensions











Symbol	Min	Nom	Max
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
b	0.22	0.30	0.38
c	0.09	0.17	0.25
D	5.90	6.20	6.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	-	0.65BSC	-
L	0.55	0.75	0.95
L1	-	1.25REF	-
L2	-	0.25BSC	-
R	0.09	-	-
Θ	0°	4°	8°
N	16		

Note(s):

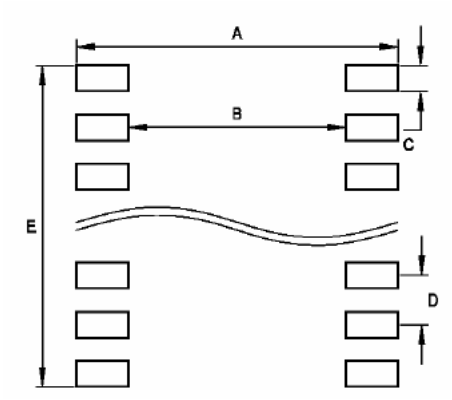
1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angles are in degrees.

Figure 48:
Marking: YYWWMZZ

YY	WW	M	ZZ
Year	Manufacturing Week	Assembly plant identifier	Assembly traceability code

Recommended PCB Footprint

Figure 49:
PCB Footprint



Recommended Footprint Data		
Symbol	mm	inch
A	9.02	0.355
B	6.16	0.242
C	0.46	0.018
D	0.65	0.025
E	5.01	0.197

Ordering & Contact Information

The devices are available as the standard products shown in Figure 50.

Figure 50:
Ordering Information

Ordering Code	Description	Delivery Form	Package
AS5130-ASSM	8-bit Magnetic Rotary Encoder with Multiturn function	Tape & Reel	16-pin SSOP (5.3mm × 6.2mm)

Buy our products or get free samples online at:
www.ams.com/Products

Technical Support is available at:
www.ams.com/Technical-Support

Provide feedback about this document at:
www.ams.com/Document-Feedback

For further information and requests, e-mail us at:
ams_sales@ams.com

For sales offices, distributors and representatives, please visit:
www.ams.com/Contact

Headquarters
ams-OSRAM AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

Website: www.ams.com

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ams Green (RoHS compliant and no Sb/Br/Cl): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material) and do not contain Chlorine (Cl not exceed 0.1% by weight in homogeneous material).

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1.12 (2011-May-12) to current revision 2-01 (2022-Aug-23)	Page
1.12 (2011-May-12) to 2-00 (2022-Jul-28)	
Content of austriamicrosystems datasheet was converted to latest **ams** design	
Updated Ordering & Contact Information	53
2-00 (2022-Jul-28) to 2-01 (2022-Aug-23)	
Updated Figure 5 (Absolute Maximum Ratings)	6

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide