High-Accuracy Hall-Effect Transmission Speed Gear Tooth Sensor IC

FEATURES AND BENEFITS

- **Differential Hall-effect sensor** measures ferrous targets with inherent stray field immunity
- **SolidSpeed Digital Architecture** supports advanced algorithms, maintaining pitch and duty cycle accuracy during dynamic air gap disturbances
- **Integrated solution** includes back-biased magnet and capacitor in a single overmolded package
- **ISO 26262:2011 ASIL B** with integrated diagnostics and certified safety design process
- **Two-wire current source output** protocol supporting speed and ASIL error reporting
- **EEPROM** enables factory traceability throughout product life cycle

A²-SIL™

SOLIDSPEED
DIGITAL ARCHITECTURE

PACKAGE:

3-Pin SIP
(suffix SN)

Not to scale

DESCRIPTION

The ATS19420 is an advanced Hall-effect integrated circuit (IC) that uses a fully integrated back-biased magnet to measure the speed of rotating ferrous targets. The package features an integrated capacitor for electromagnetic compatibility (EMC).

The ATS19420 SolidSpeed Digital Architecture offers intelligent algorithms capable of stable operation during sudden and dynamic air gap movements. The sophisticated digital controller provides highly accurate speed detection ideal for transmission applications. In addition, the ATS19420 differential sensing offers inherent rejection of interfering common-mode magnetic fields.

The ATS19420 was developed in accordance with ISO 26262:2011 as a hardware safety element out of context with ASIL B capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

The ATS19420 is provided in a 3-pin SIP package (suffix SN) that is lead (Pb) free, with tin leadframe plating. The SN package includes an IC, magnet, and capacitor integrated into a single overmolded package, with an additional molded lead-stabilizing bar for robust shipping and ease of assembly.
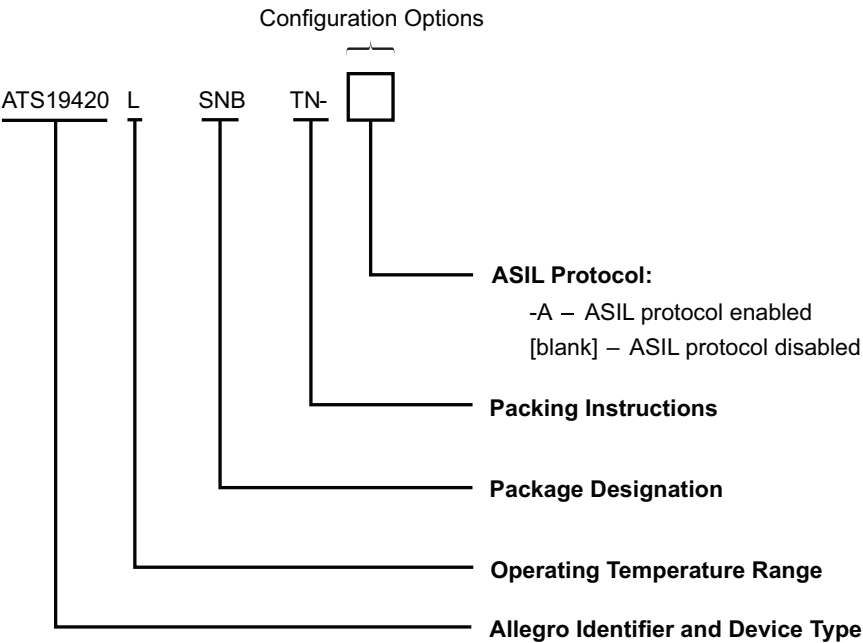
Functional Block Diagram
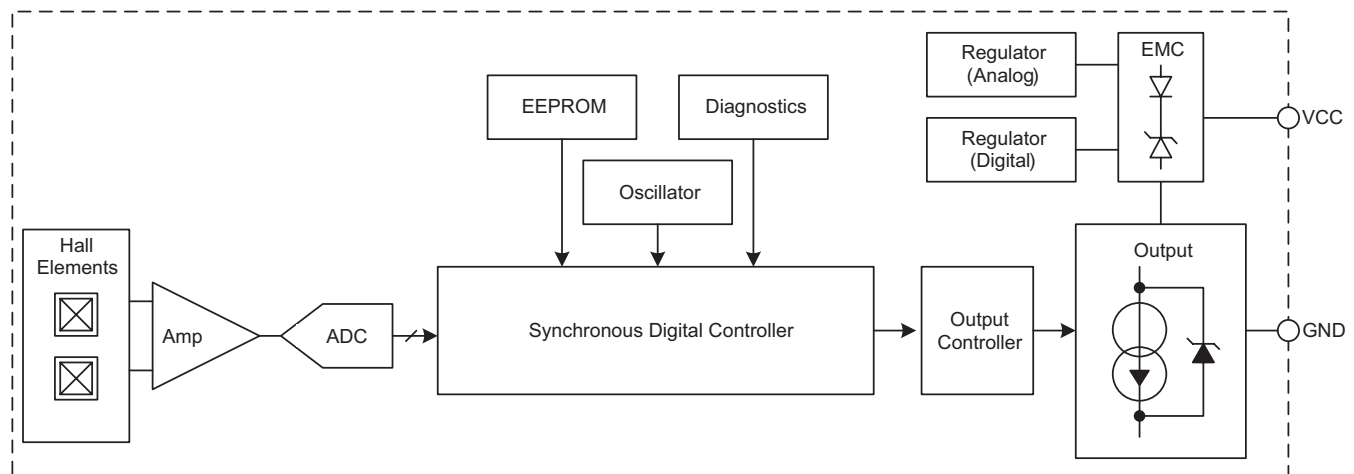
SELECTION GUIDE [1]

Part Number	Packing
ATS19420LSNBTN	Tape and reel, 13-in. reel, 800 pieces per reel

[1] Not all combinations are available. Contact Allegro sales for availability and pricing of custom programming options.

Configuration Options

ATS19420 L SNB TN- ☐

ASIL Protocol:

-A – ASIL protocol enabled

[blank] – ASIL protocol disabled

Packing Instructions

Package Designation

Operating Temperature Range

Allegro Identifier and Device Type

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to Power Derating section	28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A		–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

PINOUT DIAGRAM
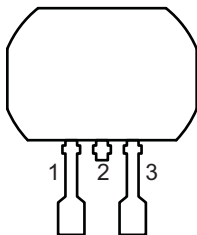
SN Package, 3-Pin SIP

PINOUTS

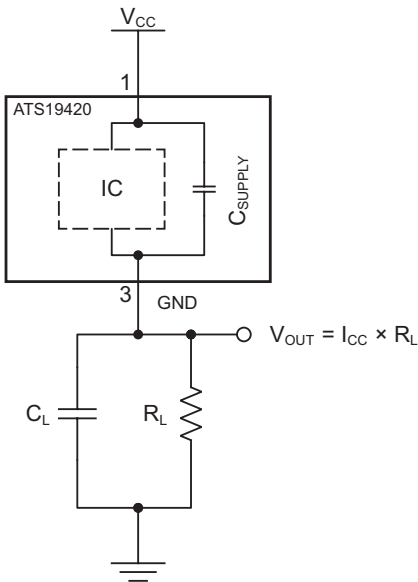| Name	Number	Function
VCC	1	Supply Voltage
VCC	2	Supply Voltage
GND	3	Ground

Figure 1: Typical Application Circuit

INTERNAL DISCRETE CAPACITOR RATINGS

Characteristic	Symbol	Notes	Value (Typ.)	Unit
Nominal Supply Capacitance	C_{SUPPLY}	Connected between pin 1 and pin 3 (refer to Figure 1)	10	nF

OPERATING CHARACTERISTICS: Valid over operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
ELECTRICAL SUPPLY CHARACTERISTICS						
Supply Voltage [2]	V_{CC}	Voltage across VCC and GND; does not include voltage across R_L; see Figure 1	4	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	V_{CC} 0 V → 5 V or 5 V → 0 V	–	3.6	3.95	V
Reverse Supply Current [3]	I_{RCC}	$V_{CC} = V_{RCC(max)}$	–10	–	–	mA
Supply Current	$I_{CC(LOW)}$	Low-current state	5.9	7	8	mA
	$I_{CC(HIGH)}$	High-current state	12	14	16	mA
	$I_{CC(HIGH)}/I_{CC(LOW)}$	Ratio of high current to low current (isothermal)	1.9	–	–	–
ASIL Safety Current	I_{RESET}	See Figure 7	1.5	–	3.9	mA
ELECTRICAL PROTECTION CHARACTERISTICS						
Supply Zener Clamp Voltage	$V_{Zsupply}$	I_{CC} = 19 mA	28	–	–	V
POWER-ON CHARACTERISTICS						
Power-On State	POS	$V_{CC} > V_{CC(min)}$		$I_{CC(LOW)}$		mA
Power-On Time [4]	t_{PO}	Time from $V_{CC} > V_{CC(min)}$; time to when device is ready to give an output transition	–	–	1	ms
CALIBRATION CHARACTERISTICS						
First Output Edge	–	Amount of target rotation (constant direction) following t_{PO} until first electrical output transition; see Figure 2	–	–	1.5	T_{CYCLE}
Initial Calibration	–	Number of electrical output transitions	–	–	3	edge
OUTPUT CHARACTERISTICS						
Output Rise Time	t_r	Voltage measured at pin 3, R_L = 100 Ω, C_L = 10 pF, see Figure 1; measured between 90% and 10% of the $I_{CC(HIGH)}$ and $I_{CC(LOW)}$ signal transition	0	2	4	µs
Output Fall Time	t_f	Voltage measured at pin 3, R_L = 100 Ω, C_L = 10 pF, see Figure 1; measured between 90% and 10% of the $I_{CC(HIGH)}$ and $I_{CC(LOW)}$ signal transition	0	2	4	µs
Pulse Width, ASIL Warning [5]	$t_{w(ASILwarn)}$	R_L = 100 Ω, C_L = 10 pF, see Figure 1	63	–	121	µs
Pulse Width, ASIL Critical [5]	$t_{w(ASILcrit)}$	R_L = 100 Ω, C_L = 10 pF, see Figure 1	4	–	8	ms

Continued on next page...

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative for Power Derating discussions.
[3] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[4] Output transients prior to t_{PO} should be ignored.
[5] Measured pulse width will vary on load circuit configurations and thresholds. Pulse width measured at threshold of ($I_{RESET} + I_{CC(LOW)}$) / 2.

OPERATING CHARACTERISTICS (continued): Valid over operating ranges, unless otherwise specified

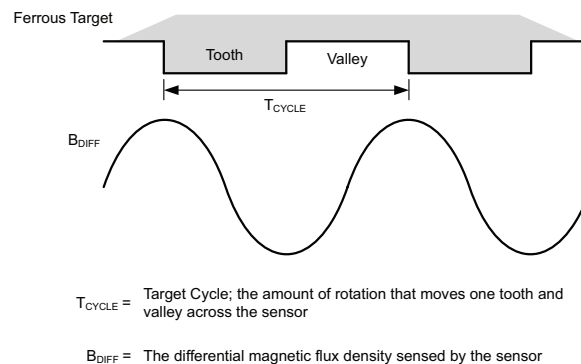| Characteristic	Symbol	Test Conditions	Min.	Typ. [6]	Max.	Unit
PERFORMANCE CHARACTERISTICS						
Air Gap Range	AG	Using Reference Target 60-0, Tested at 2000 rpm [7]	0.5	–	3	mm
Allowable User-Induced Offset		Differential magnitude valid for differential magnetic channel	–400	–	400	G
Duty Cycle Tolerance	ΔD	Using a single revolution of Reference Target 60-0, wobble < 0.5 mm, (maximum duty cycle – minimum duty cycle)	–	–	10	%
Operating Frequency	f_{OP}	Sinusoidal magnetic input signal	–	–	12	kHz
Over Frequency Warning	$f_{OP(WARN)}$	Threshold for $t_{w(ASILwarn)}$	–	15	–	kHz
Operating Magnetic Input Signal Variation	$\Delta B_{DIFF(pk-pk)}$	Bounded amplitude ratio within T_{WINDOW} [8]; no missed output transitions [9]; see Figure 3 and Figure 4	0.55	–	–	–
Operating Magnetic Input Signal Window	T_{WINDOW}	Rolling window in which $\Delta B_{DIFF(pk-pk)}$ cannot exceed bounded ratio; see Figure 2, Figure 3, and Figure 4	3	–	–	T_{CYCLE}
THERMAL CHARACTERISTICS						
Package Thermal Resistance [10]	$R_{\theta JA}$	Minimum-K PCB, single-layer, single-sided, with copper limited to solder pads	–	150	–	°C/W

T_{CYCLE} = Target Cycle; the amount of rotation that moves one tooth and valley across the sensor

B_{DIFF} = The differential magnetic flux density sensed by the sensor

Figure 2: Definition of T_{CYCLE}

[6] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[7] Speed-related effects on maximum air gap are highly dependant upon specific target geometry. Consult with Allegro field applications engineering for aid with assessment of target geometries.
[8] Symmetrical signal variation is defined as the largest amplitude ratio from B_n to B_n+T_{WINDOW}. Signal variation may occur continuously while B_{DIFF} remains in the operating magnetic range.
[9] While (0.5 mm ≤ AG ≤ 3.0 mm) sensor output will never permanently cease to switch with target rotation present.
[10] Additional thermal information is available on the Allegro website.
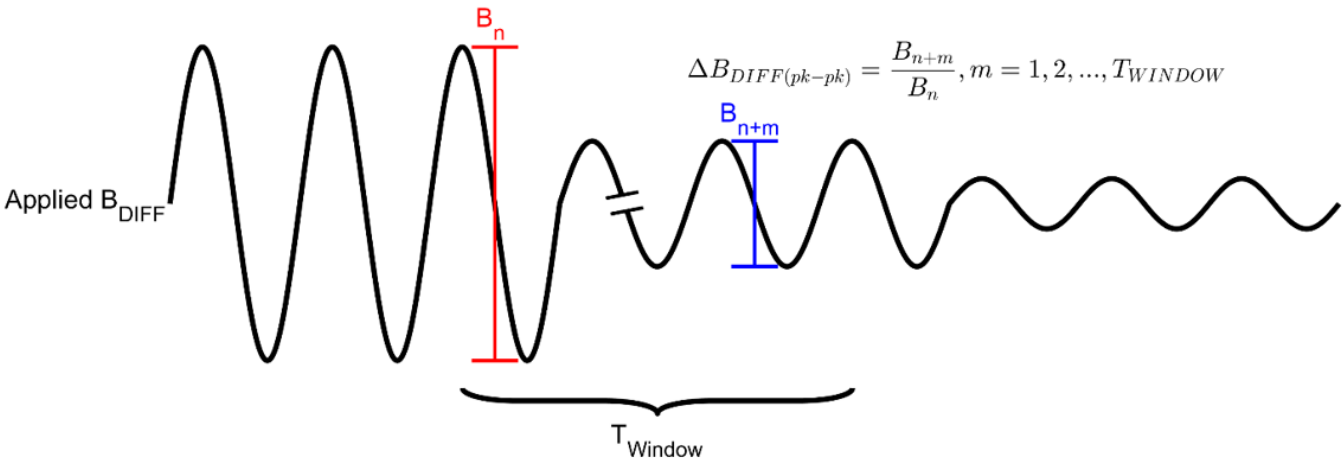
$$\Delta B_{DIFF(pk-pk)} = \frac{B_{n+m}}{B_n}, m = 1, 2, ..., T_{WINDOW}$$

Figure 3: Single Period-to-Period Variation

$$\Delta B_{DIFF(pk-pk)} = \frac{B_{n+m}}{B_n}, m = 1, 2, ..., T_{WINDOW}$$
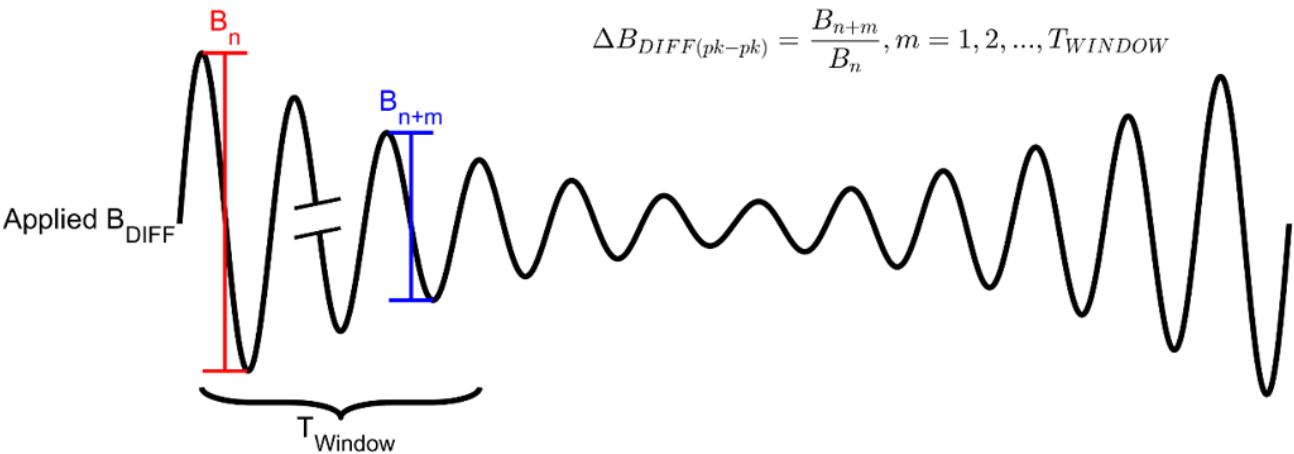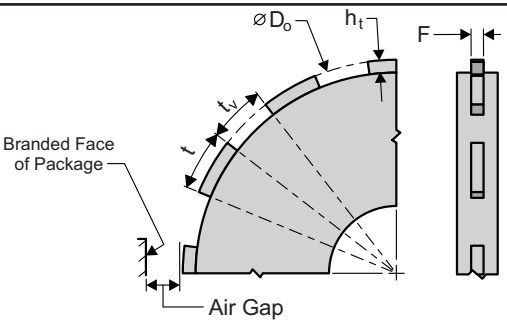
Figure 4: Repeated Period-to-Period Variation

Reference Target 60-0 (60 Tooth Target)

Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	D_o	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face	6	mm	
Circular Tooth Length	t	Length of tooth, with respect to branded face	3	deg.	
Circular Valley Width	t_v	Length of valley, with respect to branded face	3	deg.	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	
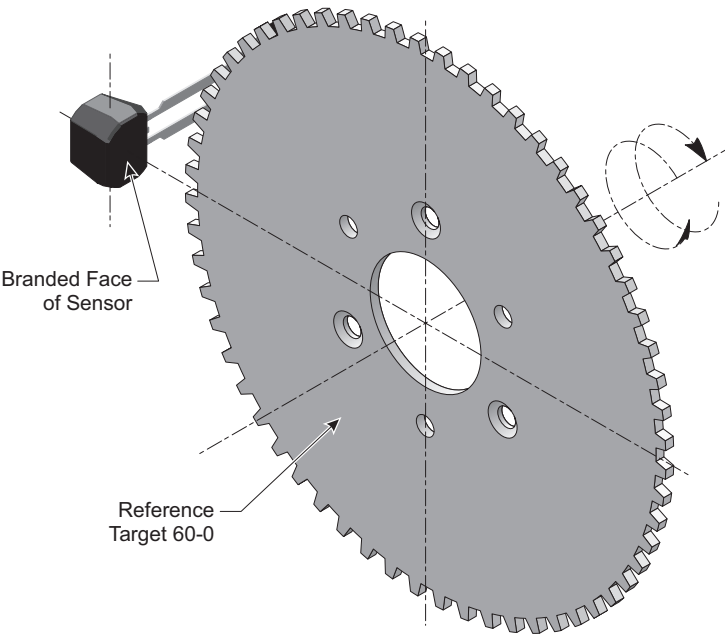
Figure 5: 60-0 Reference Target Drawing

FUNCTIONAL DESCRIPTION

The ATS19420 sensor IC contains a single-chip Hall-effect circuit that supports one differential channel used to convey accurate speed and edge position data over a two-wire digital interface. The sensor is intended for use with ferrous targets. The IC detects the peaks of the sensed magnetic signals and sets dynamic thresholds based on these detected signals. Output edges are triggered by B_{DIFF} transitions through the switch points.

Mechanical sensor to target relationship is depicted from Figure 5 for this radial type target. For best signal conduction, it is recommended to align the Hall elements center point, refer to Figure 8,

with the center of the target diameter (D_o) and the center of the tooth breadth (F).

Figure 6 demonstrates how the ferrous target magnetic systems generate magnetic fields. From generated magnetic fields, the ATS19420 derives a differential electrical signal using Hall elements, and converts the analog signal into a digital value using a full input range analog-to-digital converter. The low noise analog-to-digital converter allows for accurate peak detection, low gauss operation, and precise position information.
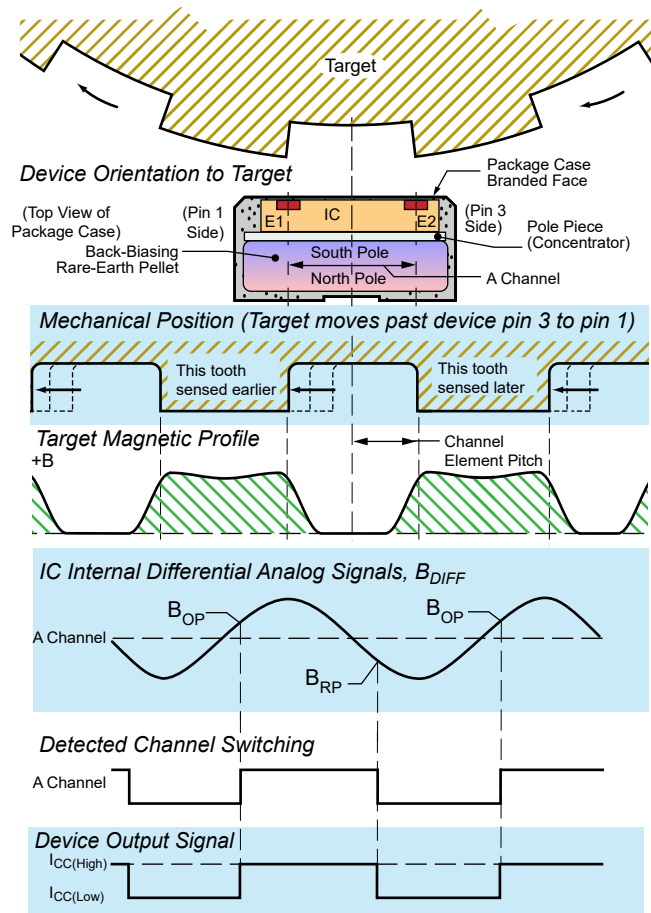

Figure 6: Magnetic Profile

Safe State Description

The -A variant contains diagnostic circuitry that will continuously monitor occurrences of failure defects within the IC. Refer to Figure 7 for the output protocol of the ASIL Safe State after a fault has been detected. Error protocol will result from faults which cause incorrect signal transmission (i.e., too few or too many output edges).

Note: If a fault exists continuously, the device will attempt recovery indefinitely. Refer to the ATS19420 Safety Manual for additional details on the ASIL Safe State Output Protocol.
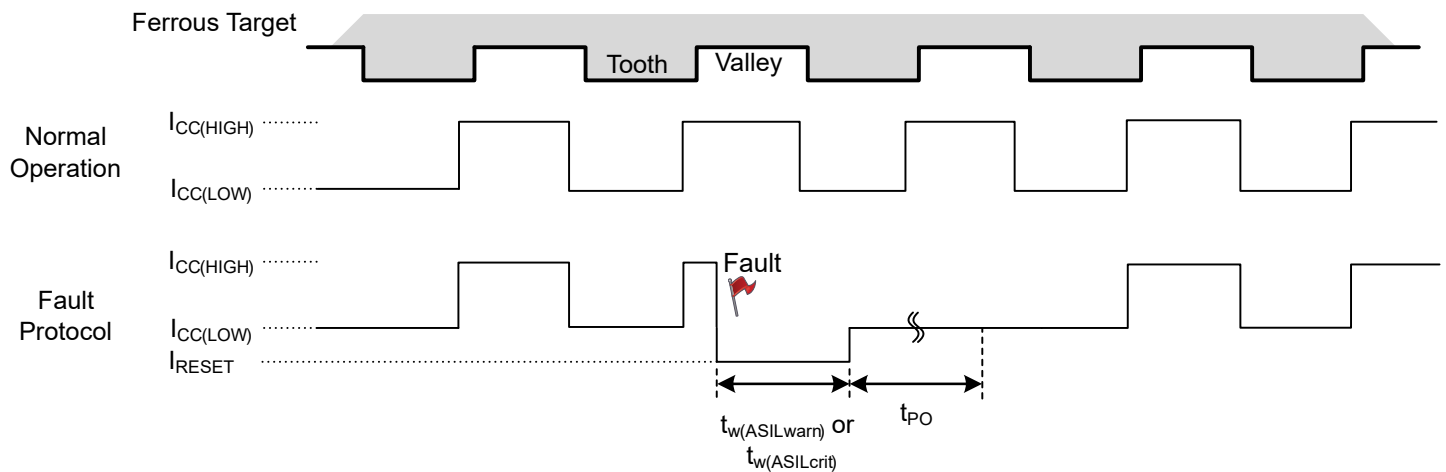
Figure 7: Output Protocol (ASIL Safe State)

POWER DERATING

The device must be operated below the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is a relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation or P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \qquad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \qquad (2)$$

$$T_J = T_A + \Delta T \qquad (3)$$

For example, given common conditions such as: $T_A = 25°C$, $V_{CC} = 12$ V, $I_{CC(avg)} = 10.5$ mA, and $R_{\theta JA} = 150°C/W$, then:

$$P_D = V_{CC} \times I_{CC(avg)} = 12\ V \times 10.5\ mA = 126\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 126\ mW \times 150°C/W = 18.9°C$$

$$T_J = T_A + \Delta T = 25°C + 18.9°C = 43.9°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at $T_A = 150°C$, package SN, using single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA} = 150°C/W$, $T_{J(max)} = 165°C$, $V_{CC(max)} = 24$ V, and $I_{CC(max)} = 16$ mA.

Calculate the maximum allowable power level ($P_{D(max)}$). First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

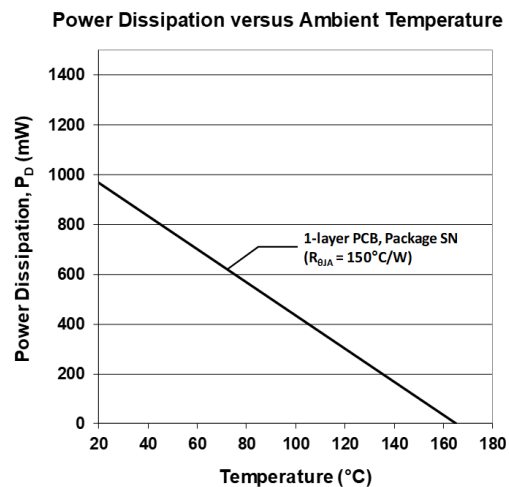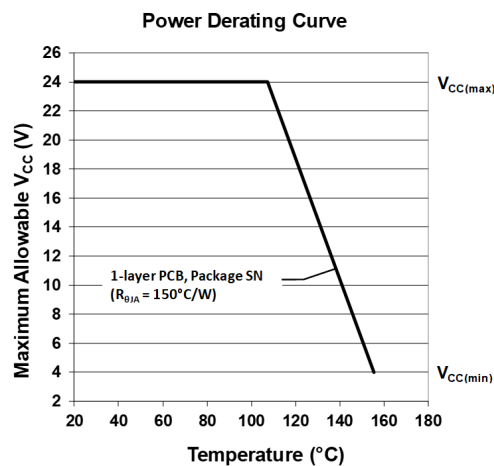This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 150°C/W = 100\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 100\ mW \div 16\ mA = 6.25\ V$$

The results indicate that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

Power Derating Curve

1-layer PCB, Package SN ($R_{\theta JA} = 150°C/W$)

$V_{CC(max)}$ / $V_{CC(min)}$

Maximum Allowable V_{CC} (V) vs Temperature (°C)

Power Dissipation versus Ambient Temperature

1-layer PCB, Package SN ($R_{\theta JA} = 150°C/W$)

Power Dissipation, P_D (mW) vs Temperature (°C)
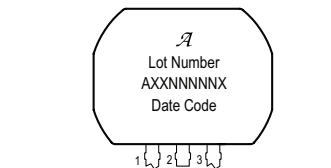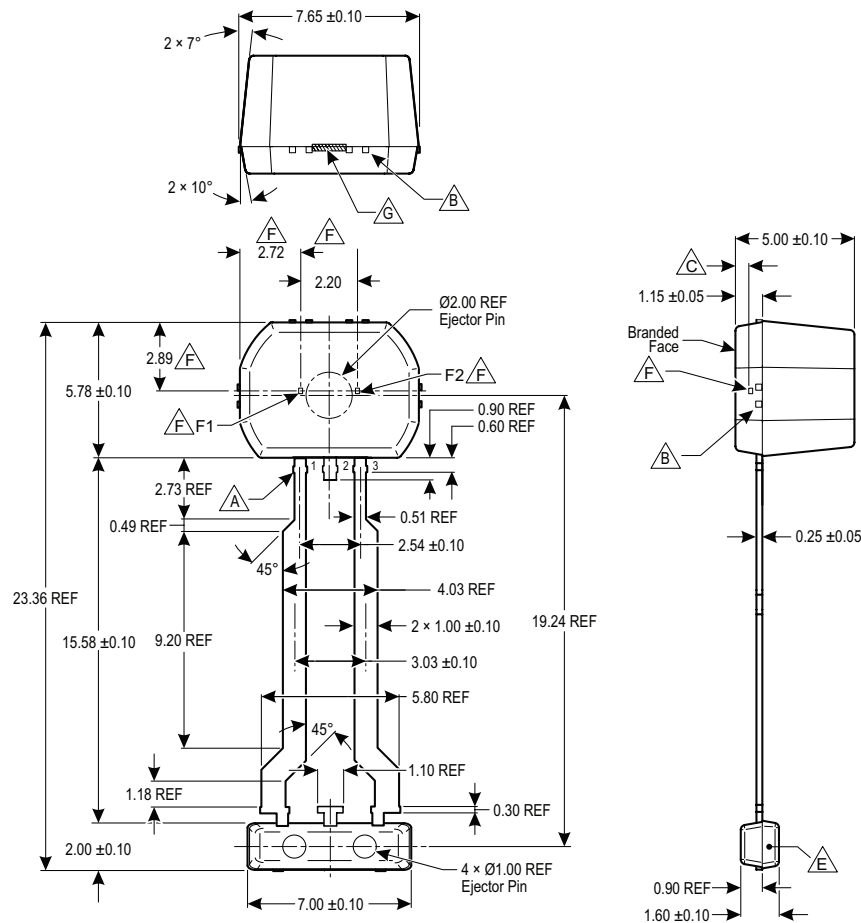
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use
(Reference DWG-0000429, Rev.4)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

Notes:

△A Dambar removal protrusion (12×)

△B Tie bars (8×)

△C Active Area Depth, 0.40 ±0.05 mm

△D Branding scale and appearance at supplier discretion

△E Molded lead bar for preventing damage to leads during shipment

△F Hall elements (F1 and F2); not to scale

△G Gate location

△D **Standard Branding Reference View**

Lines 1, 2, 3, 4: Up to 10 characters, centered

Line 1: Logo A
Line 2: Characters 5, 6, 7, 8, 9, 10, 11 of
            Assembly Lot Number
Line 3: 3 Character Prefix, 5 Digit Part Number,
            Package Variant
Line 4: 4 digit Date Code

Figure 8: Package SN, 3-Pin SIP

Revision History

Number	Date	Description
–	October 31, 2019	Initial release
1	June 29, 2021	Updated ASIL status (pages 1-2)

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