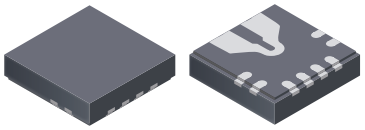
Hall-Effect Linear Current Sensor with Overcurrent Fault Output for <100 V Isolation Applications

FEATURES AND BENEFITS

- No external sense resistor required; single package solution
- Reduced power loss:
  - □ 0.6 mΩ internal conductor resistance
- Economical low- and high-side current sensing
- Output voltage proportional to AC or DC currents
- ±15.5 A and ±31 A full-scale sensing ranges
- Overcurrent $\overline{\text{FAULT}}$ trips and latches at 100% of full-scale current
- Low-noise analog signal path
- 100 kHz bandwidth
- Small footprint, low-profile SOIC8 and QFN packages
- New automotive-qualified wettable flank QFN package
- 3 to 5.5 V single supply operation
- Integrated electrostatic shield for output stability
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Zero magnetic hysteresis
- Ratiometric output from supply voltage

PACKAGE:

12-contact QFN
3 mm × 3 mm × 0.75 mm
(EX package with wettable flank)



Not to scale

DESCRIPTION

The Allegro™ ACS711 provides economical and precise solutions for AC or DC current sensing in <100 V audio, communications systems, and white goods. The device package allows for easy implementation by the customer. Typical applications include circuit protection, current monitoring, and motor and inverter control. The new wettable flank QFN package offering is ideally suited for in-cabin automotive applications and is automotive qualified.

The device consists of a linear Hall sensor circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer.

The output of the device has a positive slope proportional to the current flow from IP+ to IP– (pins 1 and 2, to pins 3 and 4). The internal resistance of this conductive path is 0.6 mΩ, providing a non-intrusive measurement interface that saves power in applications that require energy efficiency.

The ACS711 is optimized for low-side current sensing applications, although the terminals of the conductive path are electrically isolated from the sensor IC leads, providing sufficient internal creepage and clearance dimensions for a low AC or DC working voltage applications. The thickness of the copper conductor allows survival of the device at up to 5× overcurrent conditions.

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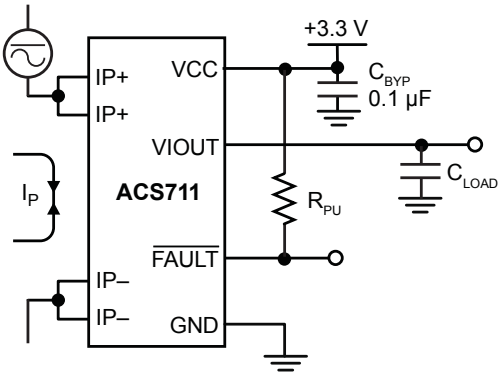
Typical Application



Application 1. The ACS711 outputs an analog signal, V_{IOUT}, that varies linearly with the bi-directional AC or DC primary current, I_P, within the range specified. The $\overline{\text{FAULT}}$ pin trips when I_P reaches ±100% of its full-scale current.

DESCRIPTION (CONTINUED)

The ACS711 is provided in a small, surface-mount packages: QFN12. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

SELECTION GUIDE

Part Number	T_A (°C)	Optimized Accuracy Range, I_P (A)	Sensitivity [1], Sens (Typ) (mV/A)	Package	Packing [2]
ACS711KEXLT-15AB-J	–40 to 125	±15.5	90	12-contact QFN with fused current loop and wettable flank	1500 pieces/reel
ACS711KEXLT-31AB-J	–40 to 125	±31	45		

[1] Sensitivity measured with V_{CC} = 3.3 V.
[2] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		7	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Output Voltage	V_{IOUT}		7	V
Reverse Output Voltage	V_{RIOUT}		–0.1	V
Working Voltage for Basic Isolation	$V_{WORKING}$	Voltage applied between pins 1-4 and 5-8	100	VAC peak or VDC
$\overline{\text{FAULT}}$ Pin Voltage	V_{FAULT}		7	V
Overcurrent Transient Tolerance	I_{POC}	1 pulse, 100 ms	100	A
Nominal Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

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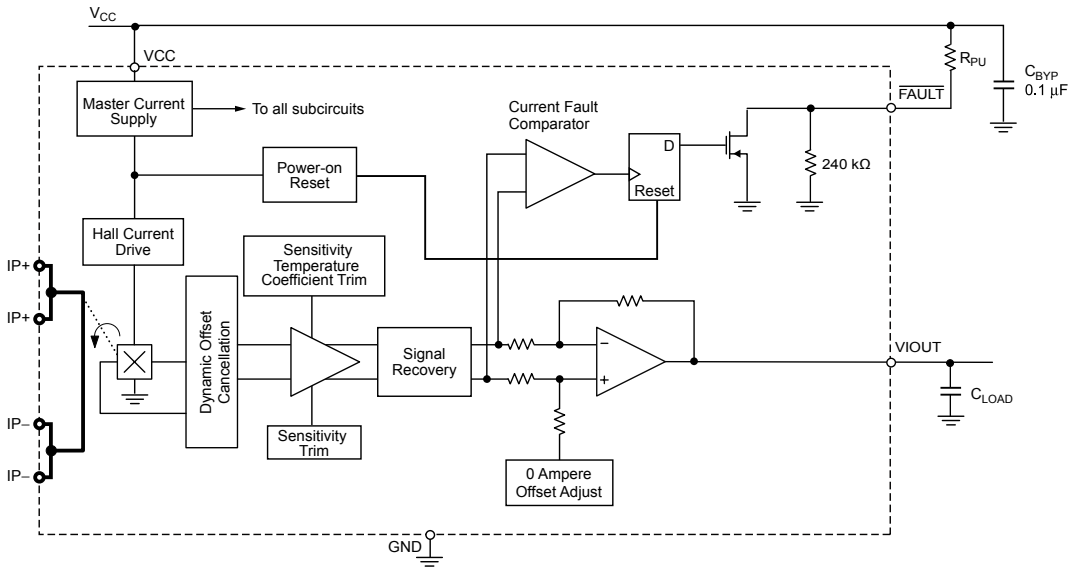
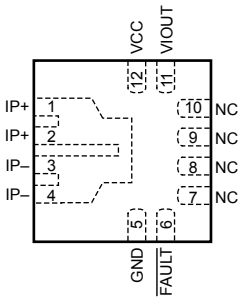
Functional Block Diagram



PINOUT DIAGRAM



EX Package

TERMINAL LIST TABLE

Name	Number	Description
GND	5	Signal ground terminal
$\overline{\text{FAULT}}$	6	Overcurrent fault; active low
IP–	3 and 4	Terminals for current being sensed; fused internally
IP+	1 and 2	Terminals for current being sensed; fused internally
NC	7, 8, 9, 10	No connection; connect to GND for optimal ESD performance.
VCC	12	Device power supply terminal
VIOUT	11	Analog output signal

COMMON OPERATING CHARACTERISTICS: Valid at T_A = 25°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1]	V_{CC}		3	3.3	5.5	V
Supply Current	I_{CC}	V_{CC} = 3.3 V, output open	–	4	5.5	mA
Output Capacitance Load	C_{LOAD}	VIOUT to GND	–	–	1	nF
Output Resistive Load	R_{LOAD}	VIOUT to GND	15	–	–	kΩ
Primary Conductor Resistance	R_{IP}		–	0.6	–	mΩ
VIOUT Rise Time	t_r	I_P = I_{PMAX}, T_A = 25°C, COUT = open	–	3.5	–	µs
Propagation Delay Time	t_{PROP}	I_P = I_P(max), T_A = 25°C, COUT = open	–	1.2	–	µs
Response Time	$t_{RESPONSE}$	I_P = I_P(max), T_A = 25°C, COUT = open	–	4.6	–	µs
Internal Bandwidth [2]	BW_I	–3 dB, T_A = 25°C	–	100	–	kHz
Nonlinearity	E_{LIN}	Over full range of I_P	–	±1	–	%
Symmetry	E_{SYM}	Apply full scale I_P	–	100	–	%
VIOUT Saturation Voltages	V_{IOH}		V_{CC} – 0.3	–	–	V
	V_{IOL}		–	–	0.3	V
Quiescent Output Voltage	$V_{IOUT(Q)}$	I_P = 0 A, T_A = 25°C	–	V_{CC} / 2	–	V
Power-On Time	t_{PO}	Output reaches 90% of steady-state level, T_A = 25°C, 20 A present on primary conductor	–	35	–	µs
$\overline{\text{FAULT}}$ PIN CHARACTERISTICS						
$\overline{\text{FAULT}}$ Operating Point	I_{FAULT}		–	±1 × I_P	–	A
$\overline{\text{FAULT}}$ Output Pullup Resistor	R_{PU}		1	–	–	kΩ
$\overline{\text{FAULT}}$ Output Voltage	V_{OH}		–	V_{CC} – 0.3	–	V
	V_{OL}	R_{PU} = 1 kΩ	–	0.3	–	V
$\overline{\text{FAULT}}$ Response Time	t_{FAULT}	Measured from | I_P | > | I_{FAULT} | to V_{FAULT} ≤ V_{OL}	–	1.3	–	µs
V_{CC} Off Voltage Level for Fault Reset [3]	V_{CCFR}		–	–	200	mV
V_{CC} Off Duration for Fault Reset [3]	t_{CCFR}		100	–	–	µs

[1] Devices are programmed for maximum accuracy at 3.3 V V_{CC} levels. The device contains ratiometry circuits that accurately alter the 0 A Output Voltage and Sensitivity level of the device in proportion to the applied V_{CC} level. However, as a result of minor nonlinearities in the ratiometry circuit additional output error will result when V_{CC} varies from the 3.3 V V_{CC} level. Customers that plan to operate the device from a 5 V regulated supply should contact their local Allegro sales representative regarding expected device accuracy levels under these bias conditions.

[2] Calculated using the formula BW_I = 0.35 / t_r.

[3] After the $\overline{\text{FAULT}}$ pin is latched low, the only way to reset it is through a power-off and power-on cycle on the VCC pin. For fault reset, V_{CC} must stay below V_{CCFR} for a period greater than t_{CCFR} before settling to the normal operation voltage (3 to 5.5 V).

x15AB PERFORMANCE CHARACTERISTICS [1]

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–15.5	–	15.5	A
Sensitivity	Sens	Across full range of I_P	–	90	–	mV/A
Noise [2]	V_{NOISE}	No external low pass filter on VIOUT	–	11	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to T_A(max)	–	±40	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±50	–	mV
Total Output Error [3]	E_{TOT}	I_P = ±12.5 A, T_A = –40°C to T_A(max)	–	±5	–	%

[1] See Characteristic Performance Data for parameter distributions across the full temperature range.

[2] ±3 sigma noise voltage.

[3] Percentage of I_P, with I_P = ±15.5 A.

x31AB PERFORMANCE CHARACTERISTICS [1]

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–31	–	31	A
Sensitivity	Sens	Across full range of I_P	–	45	–	mV/A
Noise [2]	V_{NOISE}	No external low pass filter on VIOUT	–	8	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to T_A(max)	–	±30	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±35	–	mV
Total Output Error [3]	E_{TOT}	I_P = ±12.5 A, T_A = 25°C to 125°C	–	±5	–	%
		I_P = ±12.5 A, T_A = –40°C to 25°C	–	±7	–	%

[1] See Characteristic Performance Data for parameter distributions across the full temperature range.

[2] ±3 sigma noise voltage.

[3] Percentage of I_P, with I_P = ±31 A.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [1]	Value	Units
Package Thermal Resistance, Junction to Lead	$R_{\theta JL}$		5	°C/W
Package Thermal Resistance, Junction to Ambient [2]	$R_{\theta JA}$	Mounted on Allegro 85-0528 evaluation board, includes the power consumed by the board	24	°C/W

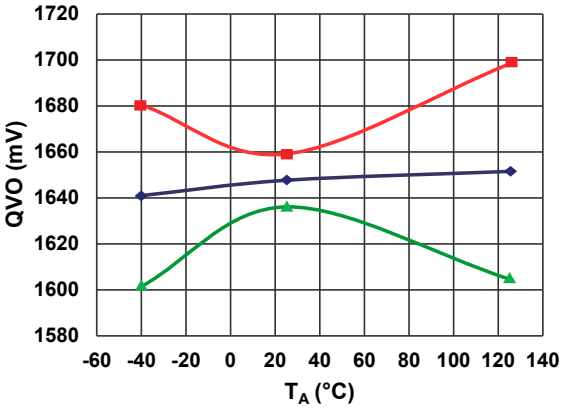
[1] Additional thermal information available on the Allegro website.

[2] The Allegro evaluation board has 1500 mm^2 of 2 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB. Further details on the board are available from the Frequently Asked Questions document on our website.

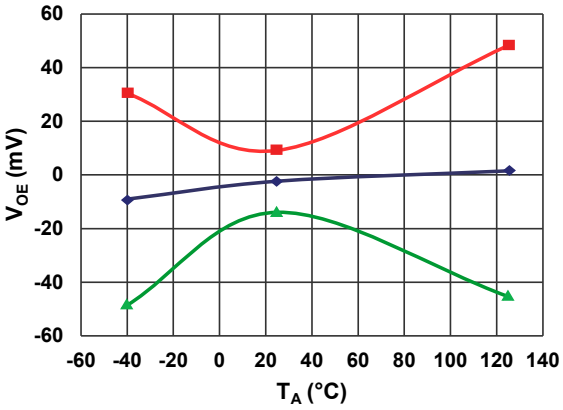
Characteristic Performance Data

Data taken using the ACS711KEX-15A, V_{CC} = 3.3 V

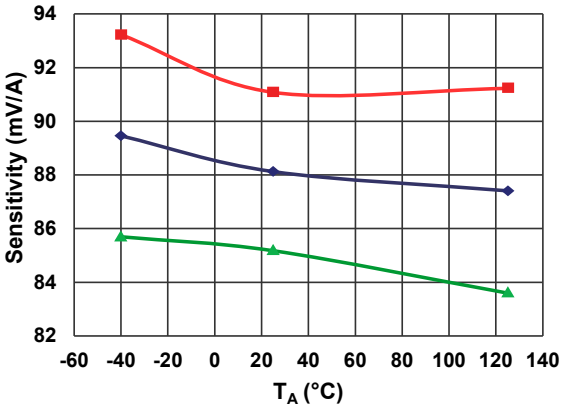
QVO versus Ambient Temperature



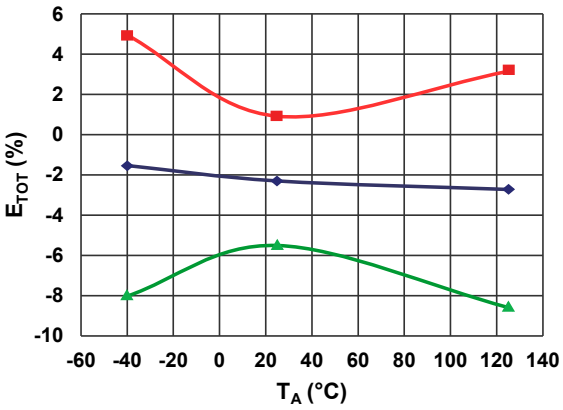
QVO Error versus Ambient Temperature



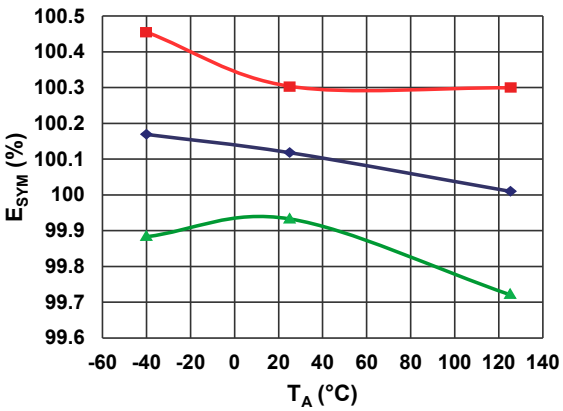
Sensitivity versus Ambient Temperature



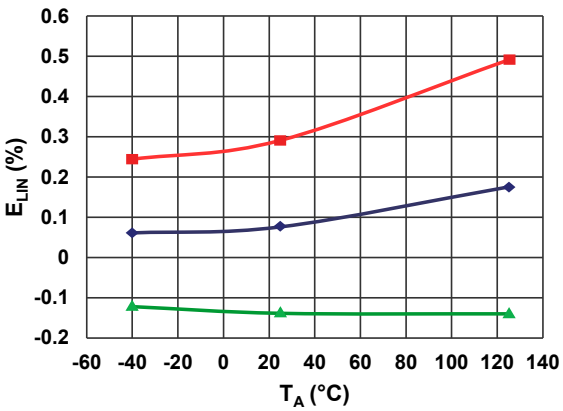
Total Error versus Ambient Temperature

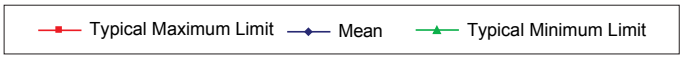


Symmetry versus Ambient Temperature



Nonlinearity versus Ambient Temperature





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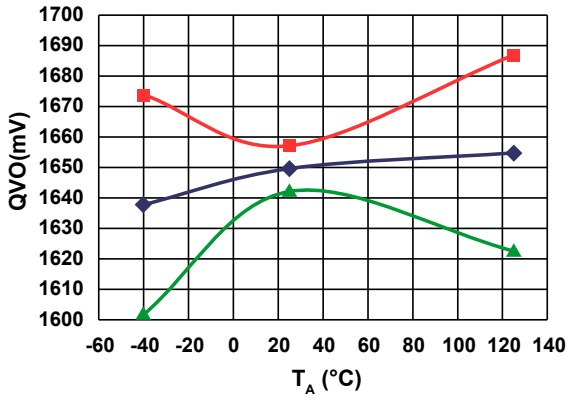
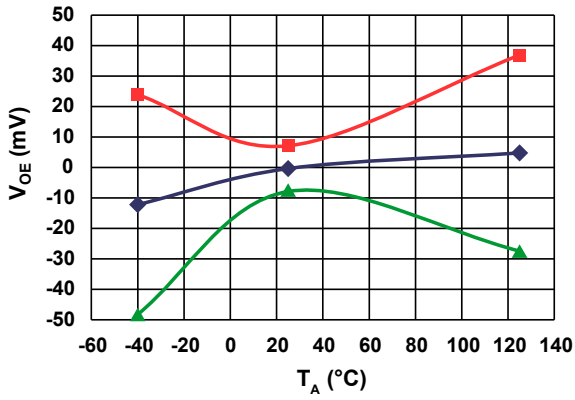
CHARACTERISTIC PERFORMANCE DATA

Data taken using the ACS711KEX-31AB, V_{CC} = 3.3 V

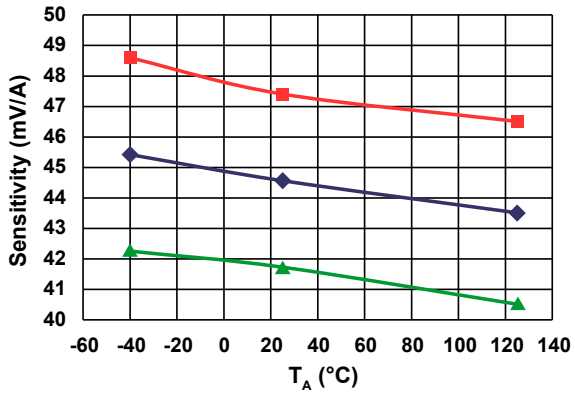
QVO versus Ambient Temperature



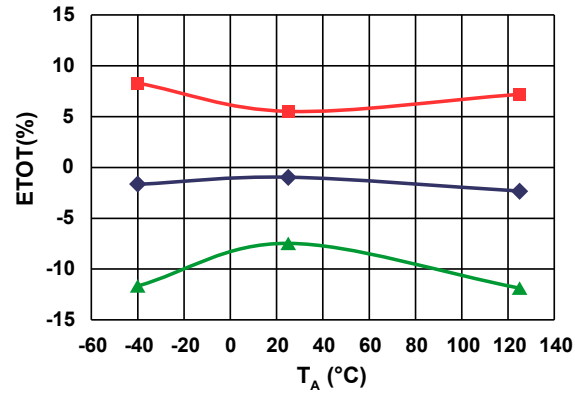
QVO Error versus Ambient Temperature



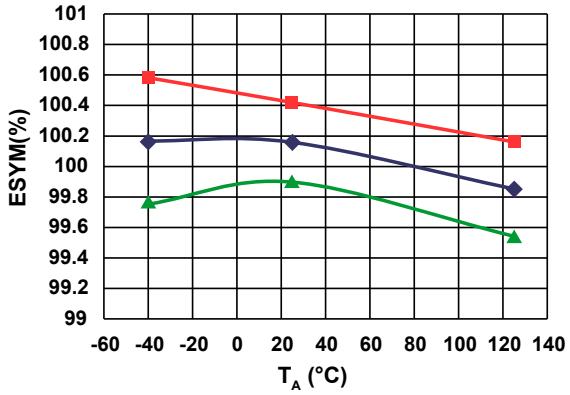
Sensitivity versus Ambient Temperature



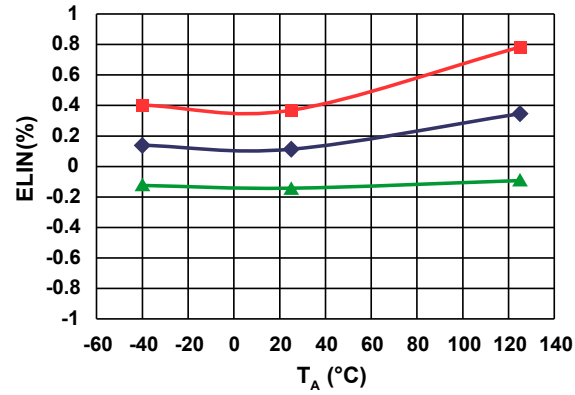
Total Error versus Ambient Temperature

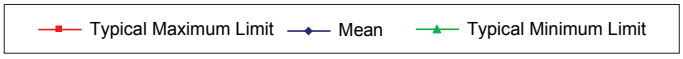


Symmetry versus Ambient Temperature



Nonlinearity versus Ambient Temperature





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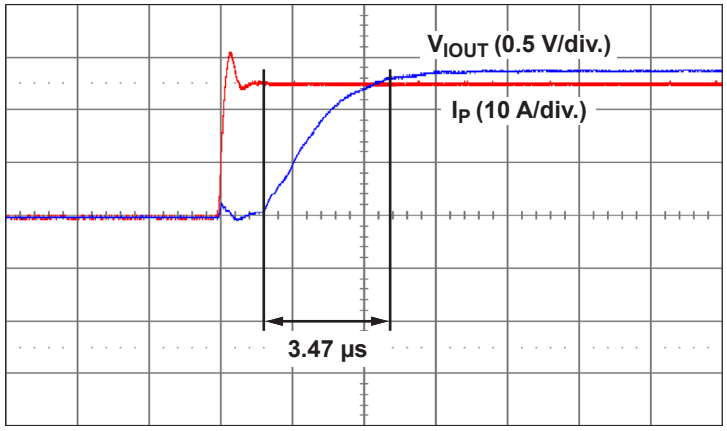
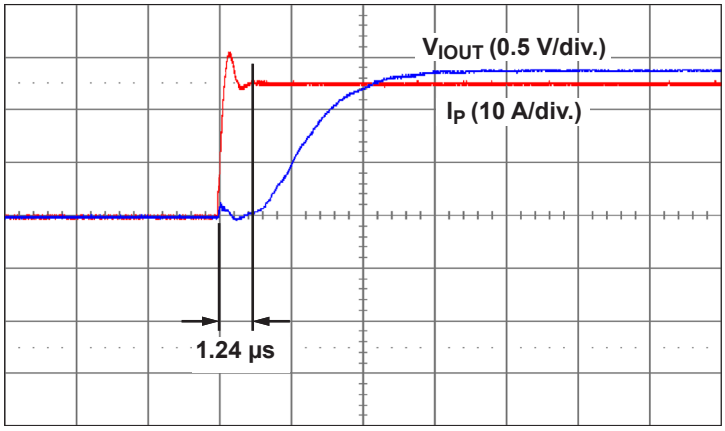
CHARACTERISTIC PERFORMANCE DATA

Timing Data

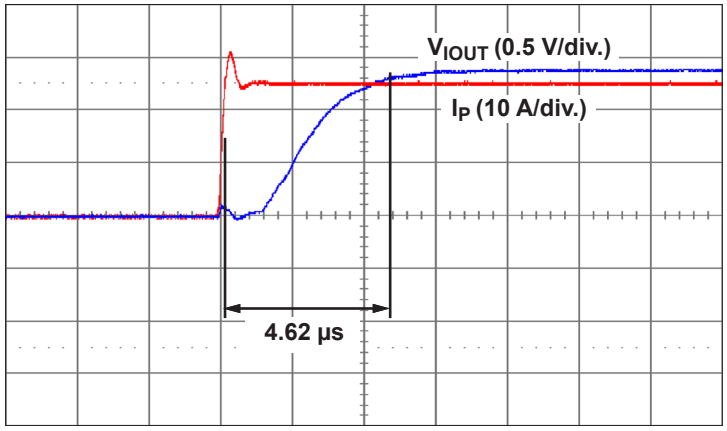
Rise Time



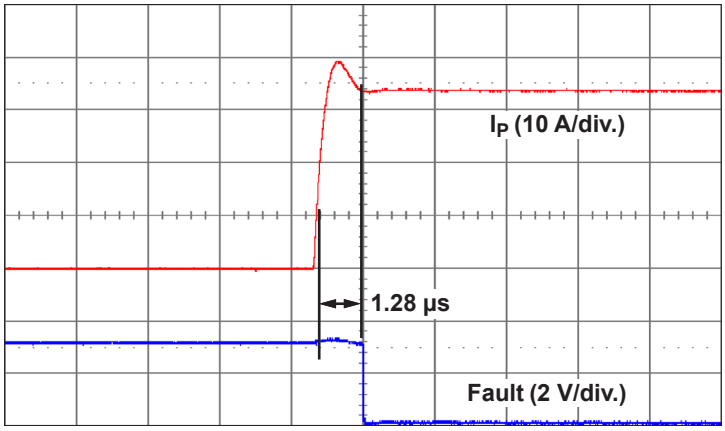
Propagation Delay Time



Response Time



Fault Response



DEFINITIONS OF ACCURACY CHARACTERISTICS

Sensitivity (Sens). The change in sensor output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}). The product of the linear IC amplifier gain (mV) and the noise floor for the Allegro Hall effect linear IC. The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}). The degree to which the voltage output from the sensor varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100\left\{1-\left[\frac{\Delta\,\text{gain}\times\%\,\text{sat}\,(V_{\text{IOUT\_full-scale amperes}}-V_{\text{IOUT(Q)}})}{2\,(V_{\text{IOUT\_half-scale amperes}}-V_{\text{IOUT(Q)}})}\right]\right\}$$

where $V_{\text{IOUT\_full-scale amperes}}$ = the output voltage (V) when the sensed current approximates full-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the sensor varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

$$100\left(\frac{V_{\text{IOUT\_+ full-scale amperes}}-V_{\text{IOUT(Q)}}}{V_{\text{IOUT(Q)}}-V_{\text{IOUT\_–full-scale amperes}}}\right)$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the sensor when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 3.3 V translates into $V_{IOUT(Q)}$ = 1.65 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Accuracy (E_{TOT}). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total ouput error. The accuracy is illustrated graphically in the output voltage versus current chart below.

Ratiometry. The ratiometric feature means that its 0 A output, $V_{IOUT(Q)}$, (nominally equal to $V_{CC}/2$) and sensitivity, Sens, are proportional to its supply voltage, V_{CC}. The following formula is used to derive the ratiometric change in 0 A output voltage, $\Delta V_{IOUT(Q)RAT}$ (%):

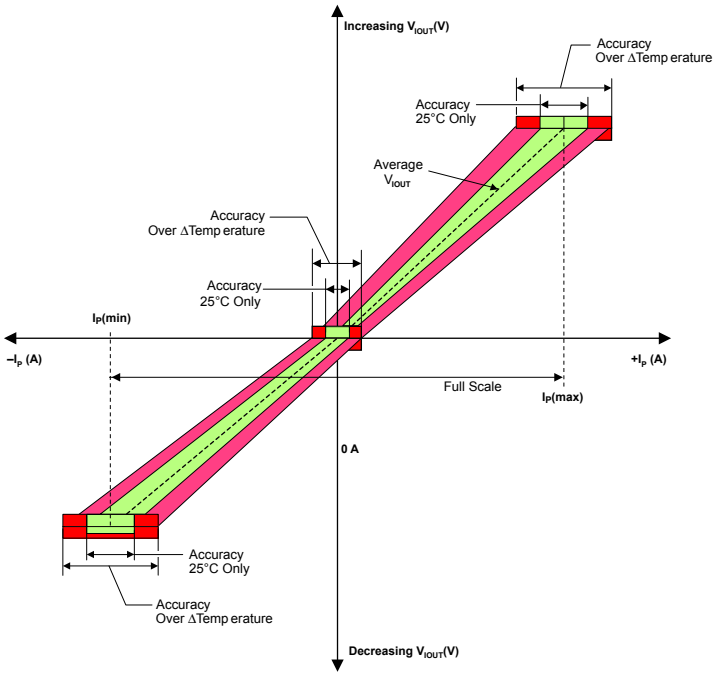
The ratiometric change in sensitivity, $\Delta Sens_{RAT}$ (%), is defined as:

$$100\left(\frac{V_{\text{IOUT(Q)VCC}}/V_{\text{IOUT(Q)3.3V}}}{V_{CC}/3.3\text{ V}}\right)$$

$$100\left(\frac{Sens_{\text{VCC}}/Sens_{\text{3.3V}}}{V_{CC}/3.3\text{ V}}\right)$$

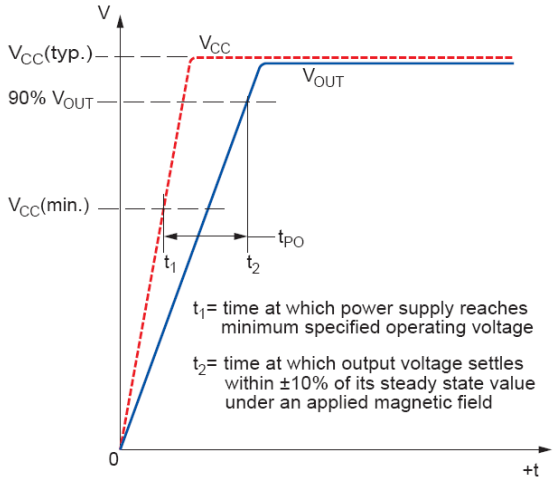
Output Voltage versus Sensed Current

Accuracy at 0 A and at Full-Scale Current

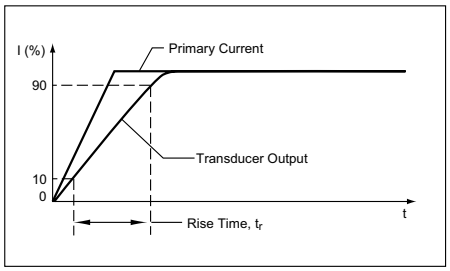


DEFINITIONS OF DYNAMIC RESPONSE CHARACTERISTICS

Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO} , is defined as the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.



Rise time (t_r). The time interval between a) when the sensor reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the current sensor, in which $f(-3\ dB) = 0.35 / t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

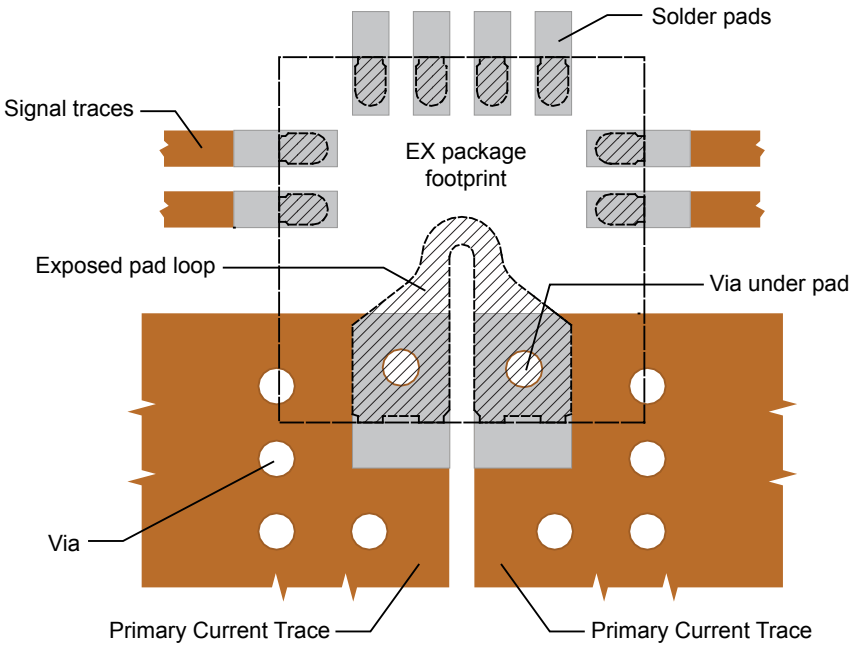


APPLICATION INFORMATION

Layout

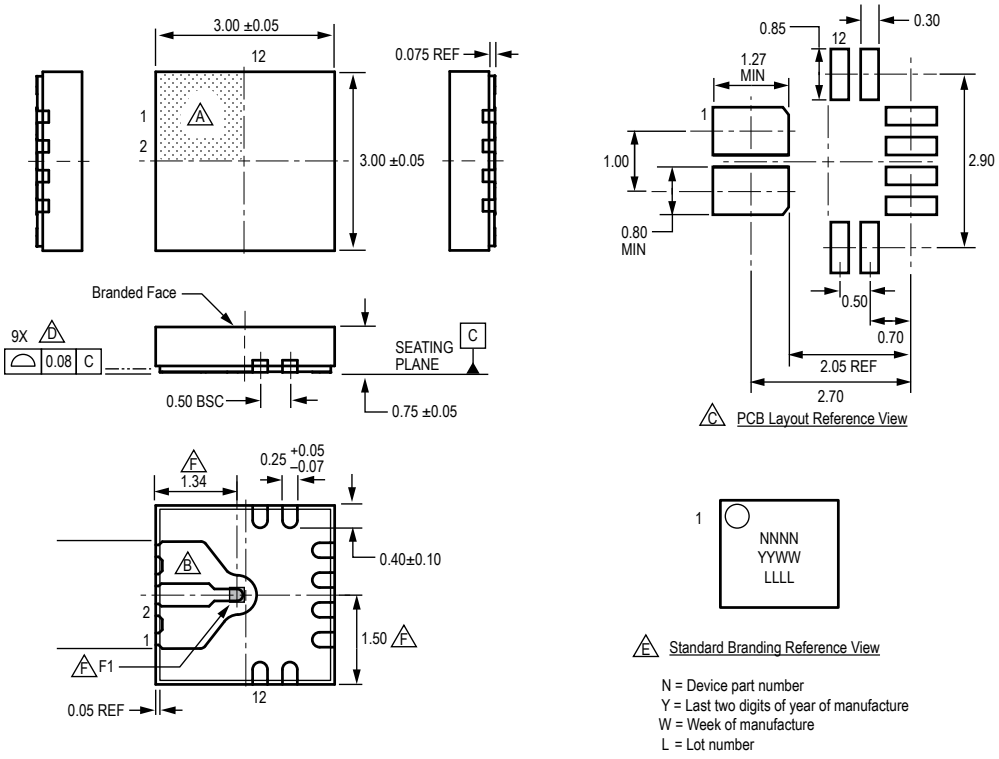
To optimize thermal and electrical performance, the following features should be included in the printed circuit board:

- The primary leads should be connected to as much copper area as is available.
- The copper should be 2 oz. or heavier.
- Additional layers of the board should be used for conducting the primary current if possible, and should be connected using the arrangement of vias shown below.
- The two solder pads at the ends of the exposed pad loop should be placed directly on the copper trace that conducts the primary current.
- When using vias under exposed pads, such as with the EX package, using plugged vias prevents wicking of the solder from the pad into the via during reflow. Whether or not to use plugged vias should be evaluated in the application.



Suggested Layout. EX package shown.

Package EX, 12-Contact QFN With Fused Sensed Current Loop and Wettable Flank



For reference only, not for tooling use (reference JEDEC MO-220WEED except for fused current path and wettable flank)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Fused sensed current path

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed current path and terminals

E Branding scale and appearance at supplier discretion

F Hall elements (F1); not to scale

Revision History

Number	Date	Description
–	September 26, 2017	Initial release
1	October 12, 2018	Minor editorial updates

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