Final

Am2971A

Enhanced Programmable Event Generator (PEG)™

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

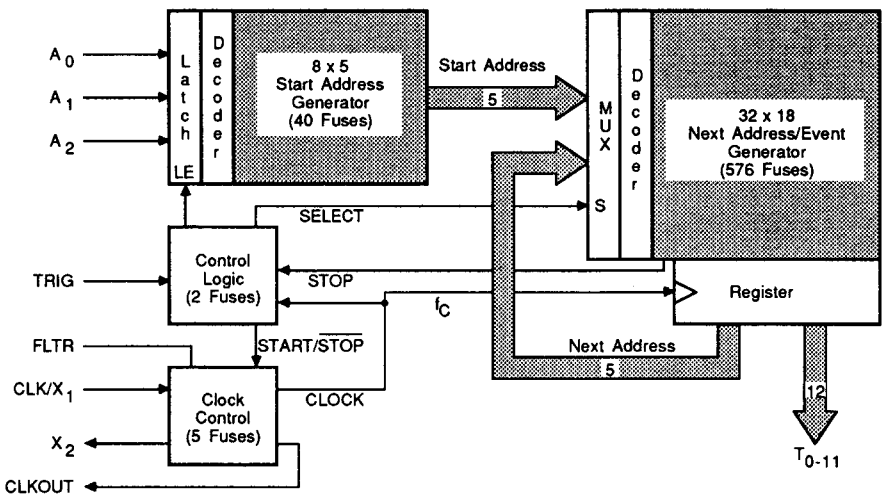
- **Generates arbitrarily defined output sequences on 12 parallel outputs**
- **Timing resolution down to 10 ns**
- **Internal frequency-multiplying Phase-Locked Loop (PLL)**
- **Crystal-controlled on-chip oscillator**
- **Programmable trigger polarity and STOP function**

GENERAL DESCRIPTION

The PEG is a versatile source of 12 simultaneous timing sequences. It can act as a digital substitute for multiple tapped delay lines or as a general-purpose user-programmable waveform generator.

Timing is derived from an external TTL source or an on-chip crystal oscillator, combined with an on-chip programmable frequency-multiplying PLL and clock divider. This achieves excellent timing resolution, down to 10 ns, from low-cost stable frequency sources of 10 MHz or less. The PEG uses platinum-silicide fuse technology and is programmed similar to any other AMD PROM.

BLOCK DIAGRAM

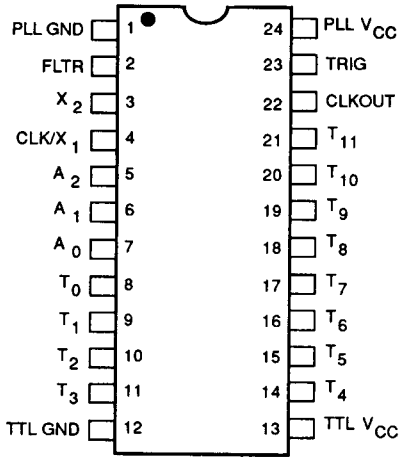


05280-001A

Publication# 05280 Rev. E Amendment /0
Issue Date: January 1990

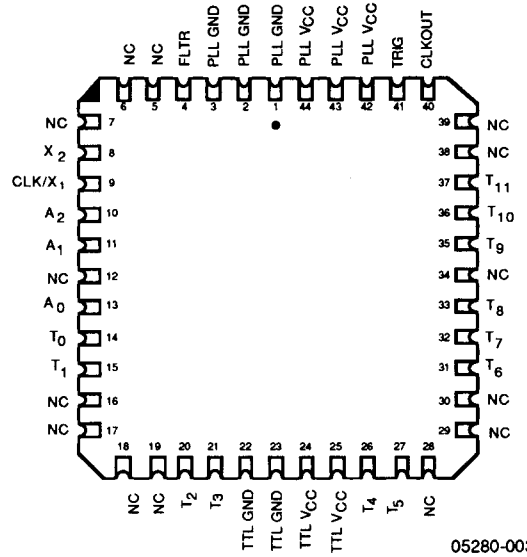
CONNECTION DIAGRAMS

DIP



05280-002A

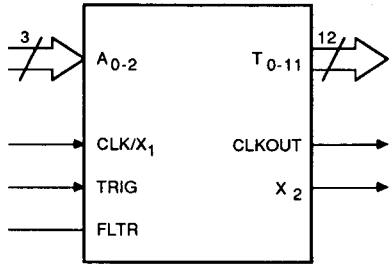
LCC*



05280-003A

* Top View, JEDEC type-C package (NC = No Connection)

LOGIC SYMBOL



Approximate Gate Count: 100

Die Size: 0.173" x 0.257"

05280-004A

THERMAL CHARACTERISTICS

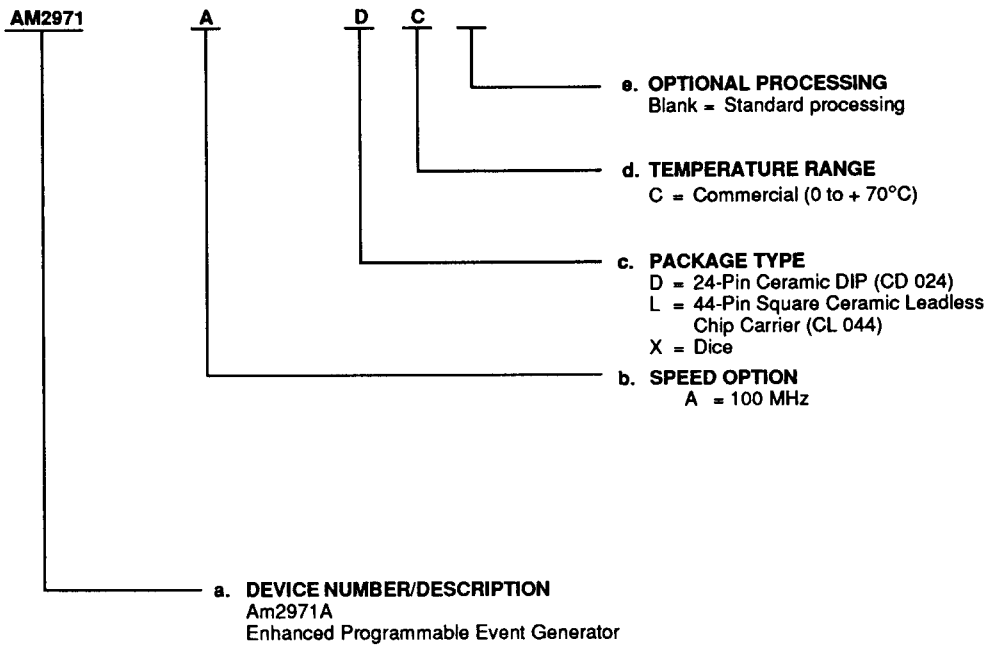
	24-pin Ceramic DIP	44-pin Ceramic LCC	Unit
θ_{JC} Max.	11	15	°C/W
θ_{JA} Max.	49	75	°C/W

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM2971A	DC, LC, XC

Valid Combinations

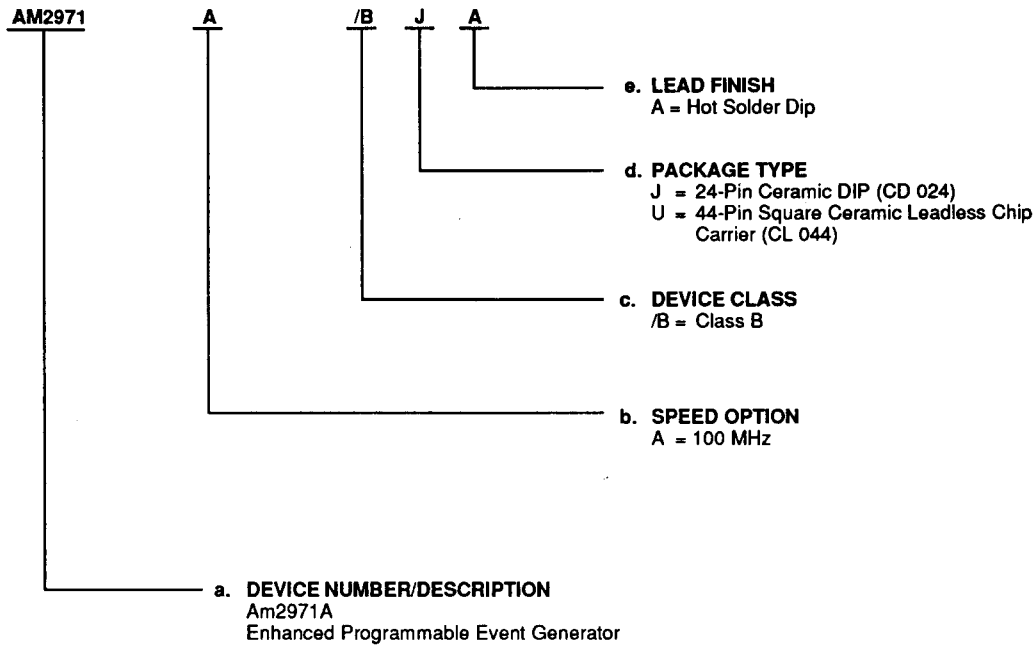
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2971A	/BJA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A_0–A_2
Addresses (Inputs)

These three bits access the Start Address Generator which contains eight user-programmed start locations. Each cycle starts at the location pointed to by the Start Address Generator word selected by the A_0–A_2 inputs. In the Program Mode, these inputs are unused and may be allowed to float.

CLK/X_1 and X_2
Clock/Crystal (Input/Output)

A TTL-level clock may be applied to the CLK/X_1 input, with the X_2 output left floating, or an AT-cut parallel resonant crystal may be connected between these two pins.

CLKOUT
Output Clock (Output)

CLKOUT is a clock output pin which may be used for system reference. The output frequency for CLKOUT (f_O) is fuse-programmable to be either 0.5, 1, or 2 times the input frequency. This output is not valid in the Bypass Mode. In the Program Mode a high-voltage pulse is applied to CLKOUT to blow selected fuses.

FLTR
Filter

This pin is used to connect a 0.47-µF filter capacitor between the Phase-Locked Loop and ground when an external crystal is used or the PLL is selected. When clocking the PEG with an external TTL source greater than 10 MHz in the Bypass Mode, this pin should be tied LOW. See Figure 8 for proper device decoupling with the PLL Bypassed.

T_0–T_{11}
Timing Outputs (Outputs; Active HIGH)

These are the twelve timing outputs which follow a user-programmed timing pattern. They are registered for glitch-free operation. In the Program and Verify Modes, T_0–T_{10} function as address inputs to access each individual fuse. T_0–T_5 serve as Row Address inputs, and T_6–T_{10} serve as Column Address inputs (see Table 6). After power-up, these outputs are all LOW. T_{11} functions as data input in the Program Mode and as data output in the Verify Mode.

TRIG
Trigger (Input)

The timing cycle of the PEG can be started by either the rising or falling edge of the start (TRIG) pulse; the polarity is defined as a fuse option (fuse #621) in the TRIGGER POLARITY block. The trailing edge of the start (TRIG) pulse stops the timing sequence if the STOP TRIG fuse (fuse #622) is left unprogrammed (0).

POWER, GROUND
TTL/PLL Power Pair

There are two sets of V_{CC} and ground pins. One power pair is used by the PLL (Phase-Locked Loop) and the internal ECL circuitry. The other power pair is used by the remainder of the chip (TTL). Surface-mount packages have additional supply connections. All power and grounds must be connected regardless of mode of operation.

FUNCTIONAL DESCRIPTION

The leading edge of the trigger pulse (polarity is fuse-programmable) causes the continuously running internal clock to step through the on-chip PROM addresses, starting at one of eight fuse-programmed locations selected by the A_{0-2} inputs.

Each addressed PROM location generates a fuse-programmed 12-bit pattern on the T_{0-11} outputs, and internally generates the fuse-programmable next PROM address as well as a fuse-programmable STOP bit, if desired. Since there is no program counter, there is an almost infinite number of ways of programming the PEG for any desired output pattern. The user will most likely choose an ascending address sequence, but this is only one of many arbitrary choices.

The address sequence can loop but cannot execute conditional jumps.

The sequence of operations stops either as a result of the trailing edge of the trigger pulse (if so enabled by a fuse) or by the programmable STOP bit. A new sequence can only be started after the previous sequence has stopped.

The internal clock frequency, f_C (see Operational Description for an explanation of all internal and external signal frequencies), is derived from and is proportional to the frequency on the X_1 input, which is either an external TTL signal or the resonant frequency of a crystal connected between X_1 and X_2. Controlled by programmable fuses, the frequency on X_1 is either used directly or is first multiplied by a factor of 1.25, 2.5, 5, or 10 to generate the internal clock frequency. A clock output is available; its frequency (fuse-programmable) is either half, double, or equal to the frequency on X_1. This output is not valid in the Bypass Mode.

Operational Description

Frequency Definitions

To avoid confusion, the definitions of the various frequencies associated with the PEG are given below:

f_I = This is the user's Input Frequency into the CLK/X_1 pin.

f_O = This is the PEG's Output Frequency at the CLKOUT pin. A CLKOUT signal is valid only when the PLL is used.

f_C = This is the Internal Clock Frequency, which is gated into the event generator state machine. When a timing sequence has been stopped, there is no f_C.

f_A = This is the Internal Altered Input Frequency, which is equivalent to f_C in value. This frequency is always generated, but it is not gated to the state machine (thus becoming f_C) unless a sequence is started.

f_{PLL} = This is the Phase-Locked Loop Frequency (f_I x 5 or f_I x 10).

TRIG-to-Output Delay

Operation of the PEG is initiated by a transition (of programmed polarity) on the TRIG input. This transition starts a series of internal events which lead to the clocking of the T_0–T_{11} output registers and to programmed changes on these outputs.

There are two possible conditions:

If the TRIG transition is synchronous with the frequency on X_1 (i.e., X_1 is a TTL clock signal and TRIG is synchronized with it), then the TRIG-to-output delay can be well-controlled, but the designer must analyze the timing and programming relationship carefully, as described below.

In the more normal case where TRIG is asynchronous to the frequency on X_1, the TRIG-to-output delay can be described very simply, but has an unavoidable uncertainty of one internal clock period.

Trigger Asynchronous

Start Delay

The delay from the active trigger edge to the first possible change of output pattern on T_0–T_{11} is the sum of:

1) Propagation delays in the trigger circuit plus output driver,
2) Up to one clock period of f_A due to the asynchronous relationship between TRIG and f_A, and
3) One clock period of f_A (used internally to prevent metastable operation).

Stop Delay

A timing sequence can be stopped either by the trailing edge of the start (TRIG) pulse (if so enabled by leaving fuse #622 unprogrammed) or by a programmed STOP bit in the Next Address/Event Generator fuse block.

The timing sequence stops when it detects either or both of these conditions. If stopped by a programmed STOP bit, the outputs remain at the level that is programmed in the same address location as the STOP bit. If stopped from the TRIG input, there is a delay equivalent to the starting delay.

Trigger Synchronous

Detailed Analysis of the Start and Stop Timing Sequences

The operation of the TRIG function can best be described by a synchronous state machine which uses f_A as the clock. All transitions occur on the rising clock edge. Figure 1 is the state diagram, Figure 2 the equivalent timing diagram. The state diagram uses the terms "active" and "inactive" edges of TRIG, since the actual polarity of TRIG is user-programmable.

State A is the idle state, after a reset or after operation has stopped for more than two periods of f_A. In state A, Select and f_C are HIGH (i.e., the Next Address/Event Generator PROM is addressed from the Start Address Generator PROM), but the output registers are not clocked; they retain their previous value.

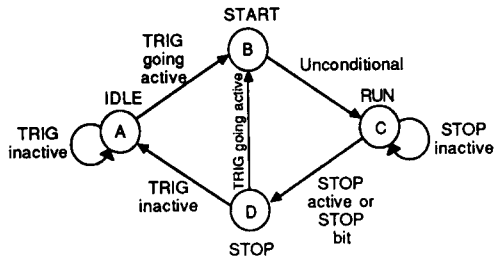
When TRIG goes active, the next rising edge of f_A forces the state machine into state B and causes f_C to be equal to f_A. The output registers are still not clocked.

The next rising edge of f_A forces the state machine into state C, clocks the output from the Next Address/Event Generator PROM into the output register and forces Select LOW. Subsequent cycles use the registered "next address" output as an address to the Next Address/Event Generator PROM. State C lasts until a STOP condition is encountered.

When a STOP condition is encountered, the next rising edge of f_C forces the state machine into state D. If TRIG goes active while the state machine is in state D, the next rising edge of f_A will cause it to go to state B; otherwise it will go to state A.

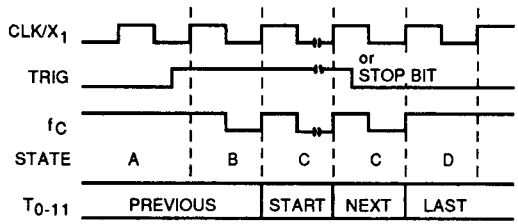
The shortest possible sequence is A-B-C-D-A, staying one f_A period in states B, C, D.

The fastest possible retrigger goes C-D-B-C, staying one f_A period in states D and B, at frequencies below 50 MHz. At frequencies greater than 50 MHz, the PEG will stay two clock periods in state D.



05280-005A

Figure 1. State Machine Diagram



05280-006A

Figure 2. State Machine Timing (Bypass Mode)

Start And Stop Timing Synchronous With f_I

The following paragraphs describe in detail the timing relationship and requirements between TRIG and the output changes on T_0–T_{11}, provided that TRIG is synchronous with f_I.

Bypass Mode ($f_C = f_I$)

TRIG must change from inactive to active for a specified setup time before the rising edge on X_1 and must stay active at least until 5 ns after the next subsequent rising edge on X_1. If the inactive-going edge of TRIG is programmed as a STOP condition, the shortest legitimate TRIG pulse will cause the state machine to cycle from state A to B to C to D, clocking the output register twice (first with the code accessed by the start address, then with the code accessed by the "next address" bits). If TRIG lasts additional X_1 clock periods, the state machine will spend this additional time in state C and the PEG will step through more codes.

PLL x5 or x10 Mode

When the f_{PLL} output is used as f_A, either 5 or 10 internal clock cycles occur for every f_I clock cycle. Since f_A is phase-synchronized to the rising edge of X_1, the timing analysis is very similar to the previous one, with f_A substituted for periods on X_1. The setup times associated with f_I also apply to f_A, since f_A is in phase with f_I. If the TRIG setup time with respect to X_1 exceeds one f_{PLL} period, then the state machine may trigger on the earlier internal clock. Because of the spread of guaranteed device parameters, an uncertainty is introduced. Thus, using the "STOP-from-TRIG" feature to generate a predetermined number of output sequences could result in an incorrect number of transitions (either more or less).

+2 or +4 Mode

In this mode the rising transitions of f_A are no longer uniquely related to the rising transitions of f_I or f_{PLL}, since the +2 counter can be in either of two starting states and the +4 counter can be in any one of four possible starting states.

The START and STOP sequences, therefore, have an additional unpredictable delay of either a 0 or 1/2 period of f_A (if +2 is chosen), or either a 0, 1/4, 1/2, or 3/4 period of f_A (if +4 if chosen).

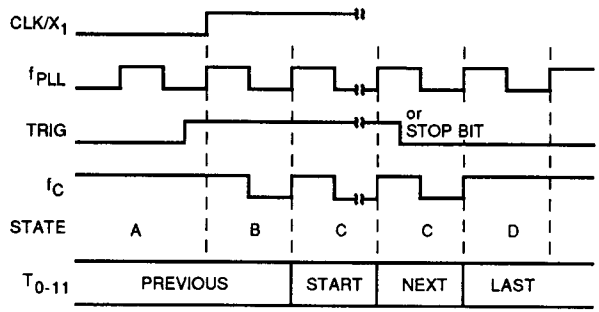


Figure 3. PLL Mode

05280-007A

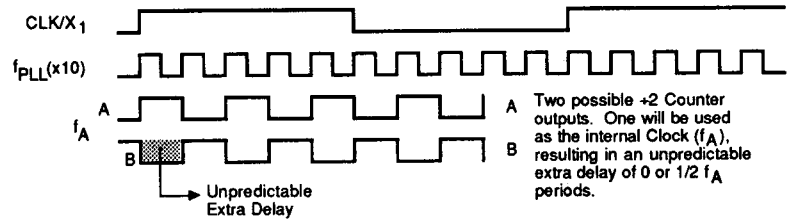


Figure 4. ÷2 Mode 05280-008A

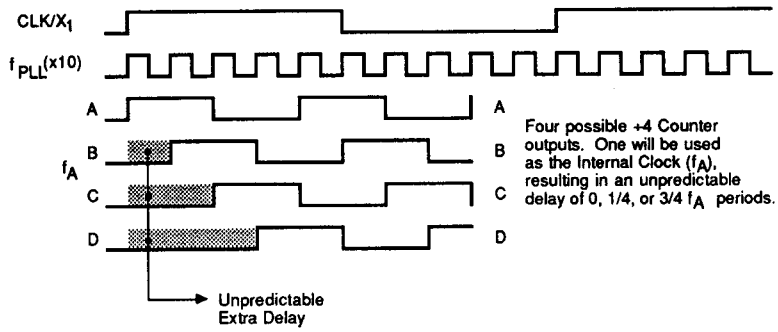


Figure 5. ÷4 Mode 05280-009A

Output Skew and Jitter

The twelve timing waveform outputs (T_0–T_{11}) are synchronized internally in an output register in order to minimize output skew.

The guaranteed maximum value for the remaining skew is specified by parameters 6–10 in the Switching Characteristics Table (depending upon the PEG version used and the number and type of transitions).

See Switching Characteristics for tighter skew specifications of certain outputs. More closely matched outputs should be used for more critical timing.

Any oscillator, and especially a Phase-Locked Loop, exhibits a certain amount of jitter — random phase modulation of the internal clock. Such jitter affects all outputs together (synchronously).

Jitter is typically less than ±1.0 ns for the ceramic DIP and Flatpack, and less than ±0.5 ns for the LCC package.

Output Event Resolution

Each of the twelve timing waveform outputs (T_0–T_{11}) can be programmed to change on any rising edge of the internal clock frequency (f_C), with the following restrictions:

The Am2971A has a maximum operating frequency of 100 MHz with a TTL source, all outputs in use. An output resolution of 10 ns for transitions of the same output or between transitions of different outputs is obtainable when a maximum of nine outputs (any nine) are switched simultaneously. If more than nine outputs are used, resolution within the same output is 20 ns, and 10 ns between outputs. If a crystal is used to clock the Am2971A, all outputs may be used, but only six outputs (any six) can be programmed to switch simultaneously. The output resolution with six outputs switching can be 10 ns within or between outputs. At internal frequencies less than 85 MHz, there are no programming restrictions (all outputs can switch simultaneously).

Table 1. Output Resolution (Between Successive Transitions of the Same Output)

Number of outputs switching simultaneously		12, 11, 10	9, 8, 7	6, 5, 4, 3, 2, 1
TTL Clock Source	PLL	20 ns	10 ns	10 ns
	Bypass			
Crystal Clock Source		Not Allowed	Not Allowed	10 ns

Oscillator

The Am2971A contains an inverting linear amplifier which can be used as a crystal oscillator. Various types of crystals are available, and the manufacturers' literature should be consulted to determine the appropriate type.

Crystal frequency varies with load capacitance. It is therefore important to match the load specified by the crystal manufacturer for a standard crystal (usually 32 pF), or to specify the load when ordering a special crystal.

The circuit of a typical 1st-harmonic oscillator is shown in Figure 6. The crystal load is comprised of the two 68-pF capacitors effectively in series. This 34 pF approximates the standard 32-pF crystal load. If a closer match is required, one of the capacitors should be replaced with a parallel combination of a fixed capacitor and a trimmer.

A typical crystal specification for use in this circuit is:

Frequency Range: 2–20 MHz
Resonance: AT, Parallel Resonant Mode
Load: 32 pF
Stability: to match system requirements

In order to eliminate stray pick-up, it is good practice to ground the case of the crystal and to keep all connections as short as possible.

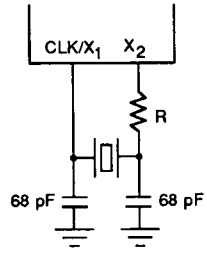
At fundamental frequencies below 6 MHz, the crystal might accidently operate in 3rd-harmonic mode. To prevent this, a resistor should be added in series with the X_2 pin as shown in the circuit diagram (Figure 6).

The resistor value should equal the impedance of C:

$$R = XC = \frac{1}{2\pi f^{*}C} = \frac{2342\ \Omega}{f(MHz)}$$ Example: R = 390 Ω for 6 MHz

Design Considerations

1) Oscillator external connections must be less than 1" long—wirewrap is not recommended.
2) V_{CC} and GND connections to power plane should be less than 1/2" long.
3) Effective supply decoupling over a broad frequency range is mandatory (Reference Figures 7 and 8).



05280-010A

Figure 6. Am2971A Crystal Oscillator Circuit

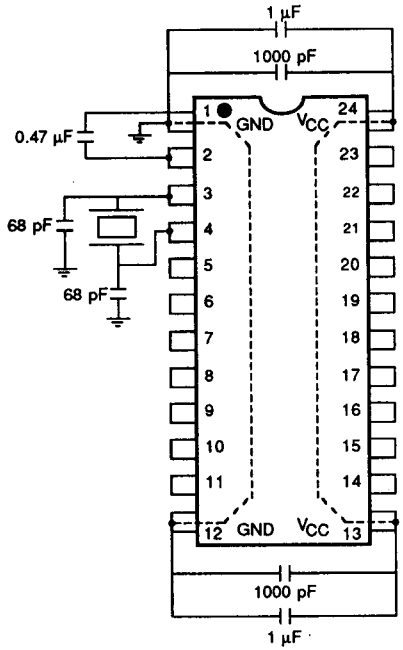


Figure 7. Am2971A Recommended Layout and Decoupling (Crystal Input)

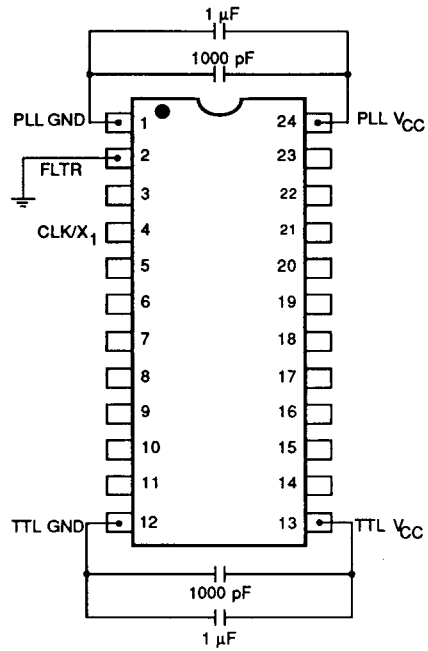


Figure 8. PEG Decoupling With PLL Bypassed

Bypass Mode Decoupling

When using the PEG with a direct TTL source above 10 MHz with the PLL bypassed, the decoupling shown in Figure 8 is mandatory.

The decoupling of the FLTR (filter) pin is necessary at frequencies higher than 10 MHz because the PLL will attempt to lock onto the incoming clock signal at CLK/X_1. This can cause anomalies in device operation and increase device jitter. Grounding the FLTR pin will isolate the PLL from the incoming clock and permit proper operation of the PEG.

PROGRAMMING

JEDEC Fuse Map

Table 6 shows the JEDEC fuse map and describes the fuse-addressing mechanism. For programming purposes the fuses are addressed by using T_0–T_{10} as inputs.

Each of the 622 fuses is addressed individually and programmed (output HIGH) or left unprogrammed (output LOW) by the equivalent level on T_{11}.

The fuses are addressed by a row/column matrix:

Input signals on pins T_0–T_5 define the row (T_0 = LSB, T_5 = MSB).

Input signals on pins T_6–T_{10} define the column (T_6 = LSB, T_{10} = MSB).

(Table 6 uses decimal notation for rows and columns. Note that there is no direct relationship between the row and column addresses and the fuse number. The fuse number is only used to refer to a particular fuse.)

In the Next Address/Event Block, each row describes the fuses used in one event. The bits accessed by columns 0 to 4 represent the Next Address column (address 0 accesses the LSB of the next address), the bits accessed by columns 5 through 16 represent the 12 output levels (column address 5 accesses the bit that uses T_0 as an output), and column address 17 accesses the STOP bit.

In the Start Address Block, the eight starting addresses are programmed by row addresses 32–39 (row address 32 programs the 5-bit word that defines the starting address selected by a 0 on the A_0– A_2 inputs, row address 39 programs the word that defines the starting address selected by a 7 on the A_0–A_2 inputs).

The Control Fuses (Reference Tables 2, and 6, and Figure 9) are accessed by row address 40 and column addresses 23–29. The functions of these fuses are described below:

Fuse #616: 0 = Divide-by-2 divider is not selected
1 = Divide-by-2 divider is selected (#617 must be zero)

Fuse #617: 0 = Divide-by-4 divider is not selected
1 = Divide-by-4 divider is selected (#616 must be zero)

Fuse #618: 0 = f_A is generated from PLL output
1 = $f_A = f_I$

Fuse #619: 0 = PLL multiplies by 10
1 = PLL multiplies by 5

Fuse #620: 0 = $f_O = f_{PLL}$ divided by 10
1 = $f_O = f_{PLL}$ divided by 5

Fuse #621: 0 = Start on rising edge of TRIG
1 = Stop on falling edge of TRIG

Fuse #622: 0 = Stop on trailing edge of TRIG (polarity defined by #621)
1 = No stop on trailing edge of TRIG

Table 2. Clock Logic Control Fuses

Fuse Pattern					Internal Clock		CLKOUT	
#616	#617	#618	#619	#620	f_A	(f_C)	f_O	
0	0	0	0	0	10	X f_I	1	X f_I
1	0	0	0	0	5	X f_I	1	X f_I
0	1	0	0	0	2.5	X f_I	1	X f_I
0	0	0	0	1	10	X f_I	2	X f_I
1	0	0	0	1	5	X f_I	2	X f_I
0	1	0	0	1	2.5	X f_I	2	X f_I
0	0	0	1	0	5	X f_I	0.5	X f_I
1	0	0	1	0	2.5	X f_I	0.5	X f_I
0	1	0	1	0	1.25	X f_I	0.5	X f_I
0	0	0	1	1	5	X f_I	1	X f_I
1	0	0	1	1	2.5	X f_I	1	X f_I
0	1	0	1	1	1.25	X f_I	1	X f_I
X	X	1	0	0	1	X f_I	1	X f_I
X	X	1	0	1	1	X f_I	2	X f_I
X	X	1	1	0	1	X f_I	0.5	X f_I
X	X	1	1	1	1	X f_I	1	X f_I
1	1	X	X	X	Illegal code			

Note: f_I is the frequency on the X_1 input.

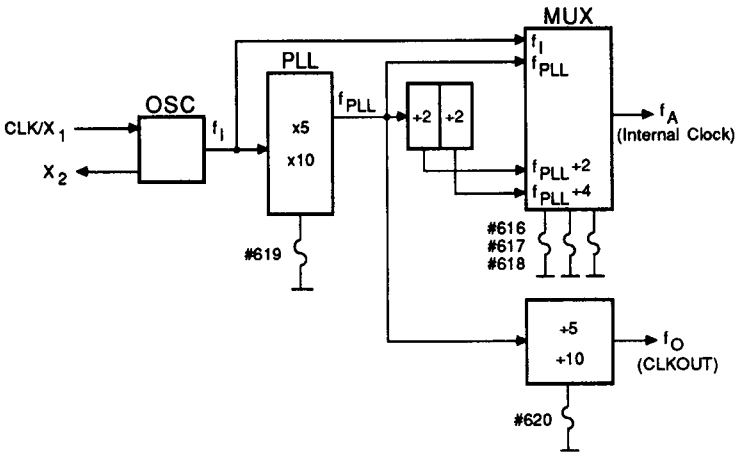


Figure 9. Clock Logic Control Fuse Locations

05280-012A

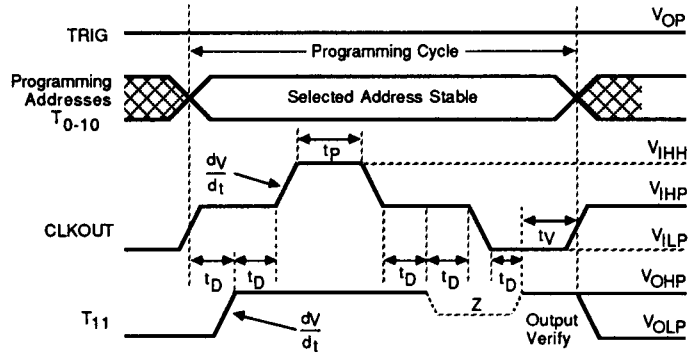


Figure 10. Programming and Verify Mode Timing

05280-013A

Programming Procedure

The following section describes the hardware requirements for programming the PEG.

This information is supplied for the designer of programming equipment. Normally the user of a PEG will utilize commercially available programming equipment and therefore has no need to study these pages (programming equipment information can be found in Table 3).

The PEG, like all AMD bipolar PROMs and PALs®, is programmed by selectively blowing platinum-silicide fuse links, one link at a time.

The table of programming parameters specifies not only the required voltage levels, but also the delays between the various actions (rise times for T_{11} and CLKOUT), and the length of the programming pulse t_P.

During the program and verify operation, TRIG must be pulled to V_{OP} (15 V) which disables the T_0–T_{11} and CLKOUT outputs. The fuse to be programmed (or verified) is selected by applying Row and Column addresses (see Figure 10) to T_0–T_{10}. (T_0 is the LSB of the Row address, T_6 is the LSB of the Column address). The selected fuse is programmed (blown, changed from 0 to 1) by a logic HIGH on T_{11} and a V_{IHH} pulse (12 V, 40–100 µs) on CLKOUT. It is common practice to verify each fuse-programming operation by three-stating the signal driving T_{11} and then applying a LOW level to CLKOUT. A blown link is indicated by a HIGH output on T_{11}.

Most links will open within the specified programming time. Occasionally a link might be stronger and require an additional programming pulse of longer duration (4 to 10 ms).

After the link has been verified, programming proceeds to the next link. After all links have been programmed, the entire array should be verified. An unprogrammed fuse (0) is indicated by a LOW on T_{11}; a programmed fuse (1) by a HIGH on T_{11}.

All unprogrammed (unblown) fuses are 0.

An unprogrammed fuse in the Next Event/Address Block generates a LOW on the outputs and a 0 as the next address. (The user can take advantage of this fact to "repair" a program error. For example: If address 31 had been left unprogrammed, any erroneously programmed location (0–3) can be moved to address 31 by programming the additional "1's" in the Next-Address field of the preceding word).

Table 3 is a list of recommended suppliers for Am2971A programming support. Each supplier is required to complete qualification by AMD to ensure high programming yields. An asterisk indicates a certified supplier (qualification complete). Consult your AMD Sales Representative to determine the current status of vendors noted as TBD or for other available models.

Table 3. Programming Equipment Information

Supplier and Location	Programmer Model(s)	Personality Modules	Socket Adaptors	Development Software
*Digelec, Inc. Ocean, NJ 201-493-2420	u803B	FAM 12	DA 42	—
	860	—	—	—
Stag Microsystems Santa Clara, CA 800-227-8836 800-222-7824	ZM 2200	—	—	—
Varix, Inc. Dallas, TX 214-437-0777	SP 0300	—	—	—
	GP 1140			
*AMD, Inc. Sunnyvale, CA 800-538-8450	Data I/O Model 29/B	UniPak™ 2/2B	AmPEGASUS™	AmPEGPDS
Inlab, Inc. Broomfield, CO 800-237-6759	Inlab 28	—	—	A.C.E.
Kontron, Inc. Mountain View, CA 415-965-7020	EPP80	UPM/B	—	—
Minato, KK Tokyo, Japan	TBD	TBD	TBD	—
Data I/O, Inc. Redmond, WA 206-881-6444	UniSite™ 40	—	—	—

*Certified supplier (qualification complete).

UniPak and UniSite are trademarks of Data I/O Corporation.

Table 4. Programming Procedure

Step	Item	Description
1	Determine location of fuses which are to be blown	
2	Set TRIG = V_{OP}	This disables T_0–T_{11} as outputs and prepares the chip for programming.
3	Set CLKOUT = V_{IHP}	This will three-state T_{11} and cause it to float up to V_{IHP}.
4	Set T_{11} = V_{IHP} after t_D	This prepares T_{11} to accept the programming current which will be gated through CLKOUT.
5	Set CLKOUT = V_{IHH} after t_D for programming time, t_{PF}	This gates the programming current to T_{11}.
6	Set CLKOUT = V_{IHP}	This removes the programming current from CLKOUT.
7	Remove applied voltage from T_{11}	This sets up T_{11} as output for Program Verification.

Table 5. Programming Verification Procedure

Step	Item	Description
1	Set TRIG = V_{OP} after t_D	TRIG remains at V_{OP} during the entire programming/verify cycle.
2	Set CLKOUT = V_{ILP} after t_D	This enables T_{11} as an output.
3a	Verify T_{11} = V_{OHP} (Note 1)	This condition occurs if programming has been successful.
3b	Verify T_{11} = V_{OLP} (Note 2)	This condition occurs if programming has been unsuccessful.

Notes: 1. If verify indicates programming has been successful, proceed to the next fuse and program using the programming steps of the previous table.

2. If verify indicates programming has been unsuccessful, return to the same fuse and re-attempt programming using the programming time t_{PS}.

Table 6. JEDEC Fuse Numbers*

FUSE																													BLOCK
COLUMN																													
	LSB	NEXT ADDRESS			MSB	LSB	CURRENT EVENT T_0–T_{11}										MSB	STOP BIT	LSB				MSB							
ROW	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	—	—	—	—	—	—	—	—	—	—	—	—	
1	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	—	—	—	—	—	—	—	—	—	—	—	—	
2	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	—	—	—	—	—	—	—	—	—	—	—	—	
3	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	—	—	—	—	—	—	—	—	—	—	—	—	
4	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	—	—	—	—	—	—	—	—	—	—	—	—	
5	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	—	—	—	—	—	—	—	—	—	—	—	—	
6	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	—	—	—	—	—	—	—	—	—	—	—	—	
7	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	—	—	—	—	—	—	—	—	—	—	—	—	
8	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	—	—	—	—	—	—	—	—	—	—	—	—	
9	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	—	—	—	—	—	—	—	—	—	—	—	—	
10	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	—	—	—	—	—	—	—	—	—	—	—	—	
11	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	—	—	—	—	—	—	—	—	—	—	—	—	
12	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	—	—	—	—	—	—	—	—	—	—	—	—	
13	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	—	—	—	—	—	—	—	—	—	—	—	—	
14	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	—	—	—	—	—	—	—	—	—	—	—	—	
15	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	—	—	—	—	—	—	—	—	—	—	—	—	NEXT ADDRESS/ EVENT GENERATOR FUSES
16	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	—	—	—	—	—	—	—	—	—	—	—	—	
17	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	—	—	—	—	—	—	—	—	—	—	—	—	
18	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	—	—	—	—	—	—	—	—	—	—	—	—	
19	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	—	—	—	—	—	—	—	—	—	—	—	—	
20	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	—	—	—	—	—	—	—	—	—	—	—	—	
21	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	—	—	—	—	—	—	—	—	—	—	—	—	
22	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	—	—	—	—	—	—	—	—	—	—	—	—	
23	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	—	—	—	—	—	—	—	—	—	—	—	—	
24	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	—	—	—	—	—	—	—	—	—	—	—	—	
25	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	—	—	—	—	—	—	—	—	—	—	—	—	
26	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	—	—	—	—	—	—	—	—	—	—	—	—	
27	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	—	—	—	—	—	—	—	—	—	—	—	—	
28	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	—	—	—	—	—	—	—	—	—	—	—	—	
29	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	—	—	—	—	—	—	—	—	—	—	—	—	
30	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	—	—	—	—	—	—	—	—	—	—	—	—	
31	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	—	—	—	—	—	—	—	—	—	—	—	—	
32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	576	577	578	579	580	—	—	—	—	—	—	—	START ADDRESS FUSES
33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	581	582	583	584	585	—	—	—	—	—	—	—	
34	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	586	587	588	589	590	—	—	—	—	—	—	—	
35	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	591	592	593	594	595	—	—	—	—	—	—	—	
36	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	596	597	598	599	600	—	—	—	—	—	—	—	
37	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	601	602	603	604	605	—	—	—	—	—	—	—	
38	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	606	607	608	609	610	—	—	—	—	—	—	—	
39	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	611	612	613	614	615	—	—	—	—	—	—	—	
40	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	616	617	618	619	620	621	622	CLOCK CONTROL & TRIGGER POLARITY FUSES**

* Row and Column numerals in this table are decimal number representations of the Binary Row and Column address signals applied to T_5–T_0 and T_{10}–T_6 respectively to program or verify each fuse individually. In this table, the reader should not confuse the use of T_{10}–T_0 as address inputs to program or verify fuses and the use of T_{11}–T_0 as Timing Outputs providing 12 programmable, registered output waveforms during normal operation (the output, T_{11}, provides the fuse condition during program or verify).

** Includes: $f_{internal}$ CLK, CLKOUT, TRIG Polarity and Stop Bit.

PROGRAMMING PARAMETERS (T_A, T_C = +25°C)

Parameter Symbol	Parameter Description		Min.	Typ.	Max.	Unit
V_{IHH}	Control Pin Extra HIGH Level		11	12	13	V
V_{OP}	Program Voltage at 15–200 mA		14	15	16	V
V_{IHP}	Input HIGH Level During Programming and Verify		2.4	5	5.5	V
V_{ILP}	Input LOW Level During Programming and Verify		0	0.3	0.5	V
V_{CCP}	V_{CC} During Programming @ I_{CC} = 250 mA	COM'L	5	5.2	5.5	V
		MIL	5	5.2	5.5	
dV_{T11}/dt	Rate of Output Enable Voltage Change (T_{11} Rising Edge)		20		250	V/µs
dV_{CLKOUT}/dt	Rate of Fuse Enable Voltage Change (CLKOUT Rising Edge)		100		1000	V/µs
t_P	Programming Time First Attempt, t_{PF}		40	50	100	µs
	Programming Time Subsequent Attempts, t_{PS}		4	5	10	ms
t_D	Delays Between Various Level Changes		100	200	1000	ns
t_V	Period During which Timing Output, T_n is Valid for Program Verification				500	ns
V_{OHP}	Output HIGH Level During Programming and Verify		2.5	5	5.5	V
V_{OLP}	Output LOW Level During Programming and Verify		0	0.3	0.4	V

Note: 1. Parameters are not tested, but are guaranteed by design.

Table 7. PEG Summary

Parameter Description	Am2971A
Max. Operating Frequency	100 MHz
Max. 12-Output Skews:	
LOW-to-HIGH	2.5 ns
HIGH-to-LOW	2.5 ns
Opposite	6.5 ns
Max. Matched Output Skews: *	Down to:
LOW-to-HIGH	1.0 ns
HIGH-to-LOW	1.0 ns
Opposite	6.5 ns
I_{CC}, Maximum	425 mA
On-Chip Crystal Oscillator	Yes
Minimum Output Resolution:	
Between Outputs	10 ns
Same Output	10 ns

* See AC Switching Characteristics

PEG SUPPORT

AmPEGASUS

AMD's PEG Adaptor Socket and Universal Software (Am-PEGASUS) is a passive programmer adaptor socket made for use in conjunction with Data I/O Corporation's Model 29/29A/29B Universal Programmer equipped with a UniPak 2/2A/2B adaptor. This passive unit makes use of the generic 2K x 8 PROM socket by reassigning the PROM configuration into a PEG pin configuration and programming algorithm. The socket draws its power from the Model 29 and contains protective circuitry to provide additional safeguards for the UniPak. Additional information can be obtained from the AmPEGASUS User's Manual, PID# 09241A.

AmPEGPDS

AMD's PEG Programming Development Software (Am-PEGPDS) is a software tool designed to aid the user in creating fuse map in the JEDEC standard for programming a PEG device. The main purpose of the software is to create and translate the input specification into a format that can be accepted by the programmer. The input specification is created by the designer using Am-PEGPDS as an editor. AmPEGPDS is available on a standard 5-1/4" floppy disk, included in both of the PEG Application Kits described as follows.

PEG Application Kits

The **PEG Starter Kit** includes:

- Am2971A PEG Data Sheet
- AmPEGPDS
- AmPEGPDS Software User's Manual
- Two PEG Unprogrammed Samples
- Applications Articles
- Am2971A Product Description

The PEG Starter Kit is available free of charge from any AMD Sales Representative.

The **PEG Design Kit** includes the **PEG Starter Kit** plus:

- AmPEGASUS Programming Adaptor Socket (customer to specify DIP or LCC)
- AmPEGASUS Translation Software
- AmPEGASUS User's Manual

Consult your AMD Sales Representative for pricing information on the PEG Design Kit.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Ambient Temperature with Power Applied	–55 to +125°C
Supply Voltage to Ground Potential Continous (TLL and PLL V_{CC})	0 to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	0 to + V_{CC} Max.
DC Input Voltage	–0.5 to +5.5 V
DC Input Current	–18 to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
TLL and PLL Supply Voltage (V_{CC})	5.0 V ± 10%
Min.	4.5 V
Max.	5.5 V

Military* (M) Devices

Case Temperature (T_C)	–55 to +125°C
TLL and PLL Supply Voltage (V_{CC})	5.0 V ± 10%
Min.	4.5 V
Max.	5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

** Military Product 100% tested at T_C = +25°C, +125°C, and –55°C.*

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)*	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = −1 mA V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL}		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all Inputs (Note 2)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for all Inputs (Note 2)		0.8	V
V_{IHC}	Input HIGH Voltage to CLK/X_1	Guaranteed Input HIGH Voltage for all Inputs	3.0		V
V_{ILC}	Input LOW Voltage to CLK/X_1	Guaranteed Input LOW Voltage for all Inputs		0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min. I_{IN} = −18 mA (Note 2)		−1.2	V
I_{IH}	Input HIGH Current	V_{CC} = Min. CLK/X_1 V_{IN} = 3.0 V		700	µA
		V_{CC} = Max. A_0–A_2 and TRIG V_{IN} = 2.7 V		20	
I_{IL}	Input LOW Current	V_{CC} = Max. CLK/X_1 V_{IN} = 0.5 V		−500	µA
		V_{CC} = Max. A_0–A_2 and TRIG V_{IN} = 0.5 V		−250	
I_I	Input Current	V_{CC} = Min. CLK/X_1 V_{IN} = 4.0 V		1.2	mA
		V_{CC} = Max. A_0–A_2 V_{IN} = 5.5 V		100	µA
		V_{CC} = Max. TRIG V_{IN} = V_{CC} − 0.5 V		100	
I_{SC}	Output Short-Circuit Current	V_{CC} = Max. T_0–T_{11}, CLKOUT V_{OUT} = 0 V	−15	−100	mA
I_{CC}	Power Supply Current	V_{CC} = Max.		425	mA
		V_{CC} = 5.0 V T_C = 25°C (Note 4)		370	

*Key: C = COM'L Devices
M = MIL Devices

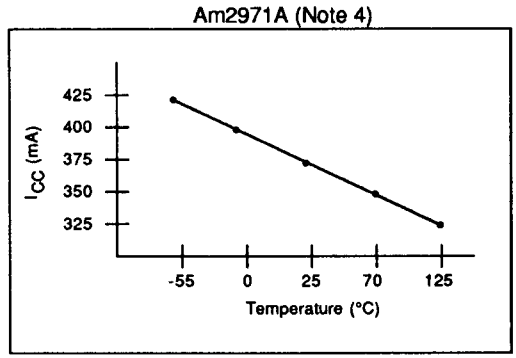
Notes: 1. For conditions shown as Min. or Max., use appropriate value specified under Operating Range for the applicable device type.

2. Does not apply to CLK/X_1 and X_2.

3. No more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

4. I_{CC} varies with temperature and oscillation frequency. Worst-case I_{CC} is at minimum temperature. Typical I_{CC} (V_{CC} = 5.0 V, T_A, T_C = +25°C) represents nominal units and is not tested. See the following graph.

Typical Power Supply Current (Nominal Unit)



05280-015A

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, and 11 are tested unless otherwise noted)

Clock Control Logic: PLL Bypassed

No.	Parameter Symbol	Parameter Description	Test Conditions*		Am2971A Min.	Am2971A Max.	Unit
1	f_I	Direct TTL Clock Source, Input Frequency at CLK/X_1 with PLL Multiplier set to "x1" (Fuse #618 = 0)	(Notes 1, 4)	C	0	100	MHz
				M	0	100	
		Crystal Clock Source (Note 6). Input Frequency at CLK/X_1 and X_2 with PLL Multiplier set to "x1" (Fuse #618 = 1)		C	0	100	
				M	0	100	
2	t_{RCO}	Rise Time of Clock Out (CLKOUT) Signal	(Note 1)	C		10	ns
				M		10	
3	t_{FCO}	Fall Time of Clock Out (CLKOUT) Signal	(Note 1)	C		10	ns
				M		10	
4	t_{RTO}	Rise Time of T_n Outputs	(Note 1)	C		8	ns
				M		8	
5	t_{FTO}	Fall Time of T_n Outputs	(Note 1)	C		8	ns
				M		8	
6	t_{SKEWLH}	Skew Time between T_n Outputs. All Outputs Switching ↑	C_L = 50 pF (Note 5)	C		2.5	ns
				M		2.5	
6a	t_{SKEWHL}	Skew Time between T_n Outputs. All Outputs Switching ↓	C_L = 50 pF (Note 5)	C		2.5	ns
				M		2.5	
7	t_{SKEW8}	Skew Time between Matched T_n Outputs. Eight Outputs Switching ↑ or ↓ ($T_{0-3, 5, 6, 10, 11}$)	C_L = 50 pF (Note 5)	C		2	ns
				M		2	
8	t_{SKEW6}	Skew Time between Matched T_n Outputs. Six Outputs Switching ↑ or ↓ ($T_{1-3, 5, 10, 11}$)	C_L = 50 pF (Note 5)	C		1.5	ns
				M		1.5	
9	t_{SKEW4}	Skew Time between Matched T_n Outputs. Four Outputs Switching ↑ or ↓ ($T_{2, 3, 10, 11}$)	C_L = 50 pF (Note 5)	C		1	ns
				M		1.5	
10	t_{SKEW}	Skew Time between T_n Outputs. All Outputs Switching Mixed Transition	C_L = 50 pF (Note 5)	C		6.5	ns
				M		6.5	
11	$t_{SET\ TCA}$	TRIG Active to CLK/X_1 ↑ Setup Time to Start an Output (T_n) Sequence		C	8		ns
				M	8		
12	$t_{SET\ TCI}$	TRIG Inactive to CLK/X_1 ↑ Setup Time to Terminate an Output (T_n) Sequence		C	4		ns
				M	4		

SWITCHING CHARACTERISTICS — Clock Control Logic: PLL Bypassed (Cont'd.)

No.	Parameter Symbol	Parameter Description	Test Conditions*		Am2971A Min.	Am2971A Max.	Unit
13	$t_{PD\,CTO}$	Propagation Delay from an Input Clock Edge (CLK/X_1) ↑ to an Active T_n Output		C	10	22	ns
				M	10	22	
14	$t_{SET\,AT}$	A_{0-2} Inputs to TRIG ↑ Setup Time	(Note 2)	C	1		ns
				M	2		
15	$t_{HOLD\,AT}$	A_{0-2} Inputs to TRIG ↑ Hold Time	(Note 2)	C	8		ns
				M	8		
16	t_{RCVRY} (Min.)	Chip Recovery/Reset Time between New (TRIG Active) Timing Sequences when Halting via STOP Bits	(Note 1)	C		$2/f_I$	ns
				M		$2/f_I$	
		Chip Recovery/Reset Time between New (TRIG Active) Timing Sequences when Halting via TRIG Inactive		C		$2/f_I$	
				M		$2/f_I$	
17	$t_{PD\,TTA}$	Propagation Delay from TRIG Active to Start of First T_n Output Signals	(Note 3)	C	$18+1/f_I$	$30+1/f_I$	ns
				M	$18+1/f_I$	$30+1/f_I$	
18	$t_{PD\,TTI}$	Propagation Delay from TRIG Inactive to Completion of Last T_n Output Signals	(Note 3)	C	$14+1/f_I$	$26+1/f_I$	ns
				M	$14+1/f_I$	$26+1/f_I$	
19	$t_{PWH\,T}$	TRIG Input Pulse Width in HIGH State	(Note 3)	C	13		ns
				M	13		
20	$t_{PWL\,T}$	TRIG Input Pulse Width in LOW State	(Note 3)	C	13		ns
				M	13		
21	$t_{PRD\,TO}$	T_n Output Period/Timing Resolution between T_n Outputs	(Note 3)	C	$1/f_I$		ns
				M	$1/f_I$		

*Key: C = COM'L Devices
M = MIL Devices

SWITCHING CHARACTERISTICS — Clock Control Logic: PLL Selected (Cont'd.)

No.	Parameter Symbol	Parameter Description	Test Conditions*		Am2971A Min.	Am2971A Max.	Unit
1	f_I	Direct TTL Clock Source. Input Frequency at CLK/X_1 with PLL Multiplier set to "x10" (Fuse #619 = "0")	(Notes 1, 4)	C	1	10	MHz
				M	1	10	
		Direct TTL Clock Source. Input Frequency at CLK/X_1 with PLL Multiplier set to "x5" (Fuse #619 = "1")		C	2	20	
				M	2	20	
		Crystal Clock Source (Note 6). Input Frequency at CLK/X_1 and X_2 with PLL Multiplier set to "x10" (Fuse #619 = "0")		C	1	10	
				M	1	10	
		Crystal Clock Source (Note 6). Input Frequency at CLK/X_1 and X_2 with PLL Multiplier set to "x5" (Fuse #619 = "1")		C	2	20	
				M	2	20	
2	t_{RCO}	Rise Time of Clock Out (CLKOUT) Signal	(Note 1)	C		10	ns
				M		10	
3	t_{FCO}	Fall Time of Clock Out (CLKOUT) Signal	(Note 1)	C		10	ns
				M		10	
4	t_{RTO}	Rise Time of T_n Outputs	(Note 1)	C		8	ns
				M		8	
5	t_{FTO}	Fall Time of T_n Outputs	(Note 1)	C		8	ns
				M		8	
6	t_{SKEWLH}	Skew Time between T_n Outputs. All Outputs Switching ↑	C_L = 50 pF (Note 5)	C		2.5	ns
				M		2.5	
6a	t_{SKEWHL}	Skew Time between T_n Outputs. All Outputs Switching ↓	C_L = 50 pF (Note 5)	C		2.5	ns
				M		2.5	
7	t_{SKEW8}	Skew Time between Matched T_n Outputs. Eight Outputs Switching ↑ or ↓ ($T_{0-3, 5, 6, 10, 11}$)	C_L = 50 pF (Note 5)	C		2.0	ns
				M		2.0	
8	t_{SKEW6}	Skew Time between Matched T_n Outputs. Six Outputs Switching ↑ or ↓ ($T_{1-3, 5, 10, 11}$)	C_L = 50 pF (Note 5)	C		1.5	ns
				M		1.5	
9	t_{SKEW4}	Skew Time between Matched T_n Outputs. Four Outputs Switching ↑ or ↓ ($T_{2, 3, 10, 11}$)	C_L = 50 pF (Note 5)	C		1.0	ns
				M		1.5	
10	t_{SKEW}	Skew Time between Tn Outputs. All Outputs Switching Mixed Transition	C_L = 50 pF (Note 5)	C		6.5	ns
				M		6.5	

SWITCHING CHARACTERISTICS — Clock Control Logic: PLL Selected (Cont'd.)

No.	Parameter Symbol	Parameter Description	Test Conditions*		Am2971A Min.	Am2971A Max.	Unit
11	$t_{SET\ TCA}$	TRIG Active to CLK/X_1 (↑) Setup Time to Start an Output (T_n) Sequence		C	8		ns
				M	8		
12	$t_{SET\ TCI}$	TRIG Inactive to CLK/X_1 (↑) Setup Time to Terminate an Output (T_n) Sequence		C	4		ns
				M	4		
13a	$t_{PD\ CTO}$	Propagation Delay from an Input Clock Edge (CLK/X_1) (↑) to an Active T_n Output when "/1" has been Selected (Fuses #616 and 617 = "0")		C	10	20	ns
				M	10	26	
13b	$t_{PD\ CTO}$	Propagation Delay from an Input Clock Edge (CLK/X_1) (↑) to an Active T_n Output when "/2" has been Selected (Fuses #616 = "1" and 617 = "0")	(Note 3)	C	10+ 1/2f_C	20+ 1/2f_C	ns
				M	10+ 1/2f_C	26+ 1/2f_C	
13c	$t_{PD\ CTO}$	Propagation Delay from an Input Clock Edge (CLK/X_1) (↑) to an Active T_n Output when "/4" has been Selected (Fuses #616 = "0" and Fuse 617 = "1")	(Note 3)	C	10+ 3/4f_C	20+ 3/4f_C	ns
				M	10+ 3/4f_C	26+ 3/4f_C	
14	$t_{SET\ AT}$	A_{0-2} Inputs to TRIG (↑) Setup Time	(Note 2)	C	1.0		ns
				M	2.0		
15	$t_{HOLD\ AT}$	A_{0-2} Inputs to TRIG (↑) Hold Time	(Note 2)	C	8		ns
				M	8		
16	t_{RCVRY} (Min.)	Chip Recovery/Reset Time between New (TRIG Active) Timing Sequence when Halting via STOP Bits	(Note 1)	C		2/f_C	ns
				M		2/f_C	
		Chip Recovery/Reset Time between New (TRIG Active) Timing Sequence when Halting via TRIG Inactive		C		2/f_C	
				M		2/f_C	
17a	$t_{PD\ TTA}$	Propagation Delay from TRIG Active to Start of First T_n Output Signal when "/1" has been Selected (Fuses #616 and 617 = "0")	(Note 3)	C	18+ 1/f_C	28+ 1/f_C	ns
				M	18+ 1/f_C	34+ 1/f_C	
17b	$t_{PD\ TTA}$	Propagation Delay from TRIG Active to Start of First T_n Output Signal when "/2" has been Selected (Fuse #616 = "1" and Fuse 617 = "0")	(Note 3)	C	18+ 1/2f_C	28+ 1/2f_C	ns
				M	18+ 1/2f_C	34+ 1/2f_C	

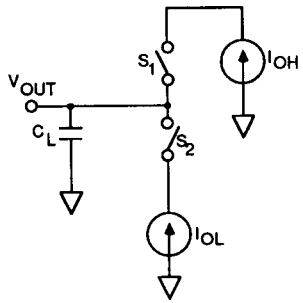
SWITCHING CHARACTERISTICS — Clock Control Logic: PLL Selected (Cont'd.)

No.	Parameter Symbol	Parameter Description	Test Conditions*		Am2971A Min.	Am2971A Max.	Unit
17c	$t_{PD\,TTA}$	Propagation Delay from TRIG Active to Start of First T_n Output Signal when "/4" has been Selected (Fuse #616 = "0" and Fuse 617 = "1")	(Note 3)	C	18+ 3/4f_C	28+ 3/4f_C	ns
				M	18+ 3/4f_C	34+ 3/4f_C	
18	$t_{PD\,TTI}$	Propagation Delay from TRIG Inactive to Completion of Last T_n Output Signals	(Note 3)	C	14+ 1/f_C	24+ 1/f_C	ns
				M	14+ 1/f_C	30+ 1/f_C	
19	$t_{PWH\,T}$	TRIG Input Pulse Width in HIGH State when "/1" has been Selected (Fuses #616 and 617 = "0")	(Note 3)	C	13		ns
				M	13		
20	t_{PWLT}	TRIG Input Pulse Width in LOW State	(Note 3)	C	13		ns
				M	13		
21	$t_{PRD\,TO}$	T_n Output Period/Timing Resolution between T_n Outputs	(Note 3)	C	1/f_C		ns
				M	1/f_C		
22	$t_{PD\,CTC}$	Propagation Delay from an Input Clock Edge (CLK/X_1) (↑) to an Output Clock Edge (Fuses #616 and 617 = "0")	(Note 1)	C	10	19	ns
				M	10	21	

*Key: C = COM'L Devices
M = MIL Devices

Notes:
1. Not production tested due to automatic test equipment limitation; guaranteed by characterization.
2. Only A_2 is tested.
3. Not tested; calculated from other parameters.
4. f_I input clock duty cycle should be 50% ± 10%.
5. Not tested. Skew times shown each case are guaranteed by characterization for specific outputs listed with any number of outputs switching.
6. The Am2971A has a maximum operating frequency of 100 MHz with a TTL source, all outputs in use, but only nine outputs (any nine) may be programmed to switch simultaneously. If a crystal is used to clock the Am2971A, all outputs may be used, buy only six outputs (any six) can be programmed to switch simultaneously.

SWITCHING TEST CIRCUIT



A. Outputs 05280-016A

Notes: 1. C_L = 50 pF. The load capacitance includes scope probe, wiring, and stray capacitance without the device in the test fixture.

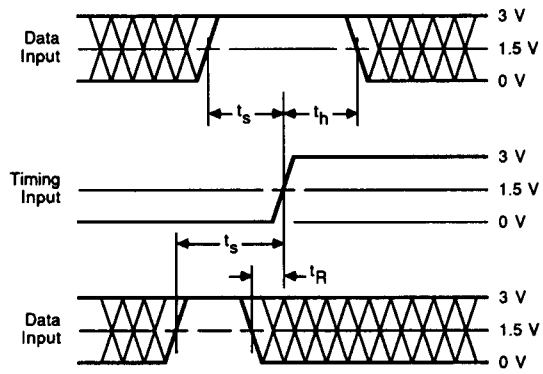
2. S_1 and S_2 are open during all DC and functional testing.

3. During AC testing, switches are set as follows:

   1) For V_{OUT} > 1.5 V, S_1 is closed and S_2 open

   2) For V_{OUT} < 1.5 V, S_1 is open and S_2 closed

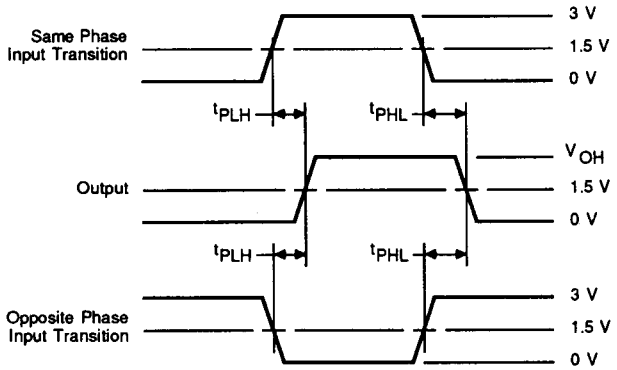
SWITCHING TEST WAVEFORMS



A. Setup, Hold, and Release Times 05280-017A

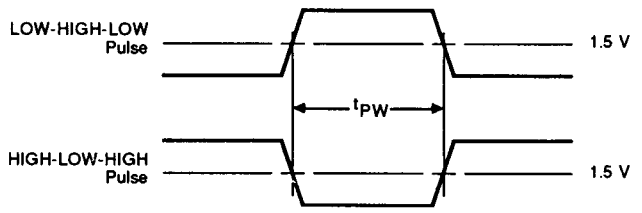
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.

2. Cross-hatched area is don't care condition.



05280-018A

B. Propagation Delay



05280-019A

C. Pulse Width

General Test Notes

Automatic tester hardware and handler hardware add additional round-trip AC delay to test measurements. Actual propagation delay testing may incorporate a correlation factor to negate the additional delay.

Function testing is done with input LOW less than V_{IL}, and input HIGH greater than V_{IH}. A single trip point at the approximate threshold voltage is used to determine output logic level.

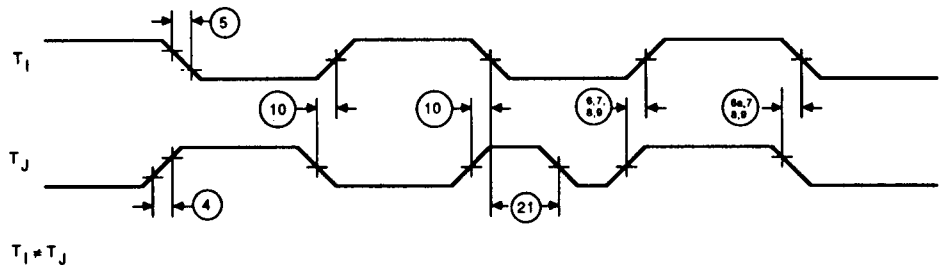
Some Setup and Hold tests are not performed due to tester accuracy limitation. They are guaranteed by correlation.

AC loads specified in this data sheet are used for bench testing. Programmable loads, which simulate data sheet loads, are used during automatic production testing.

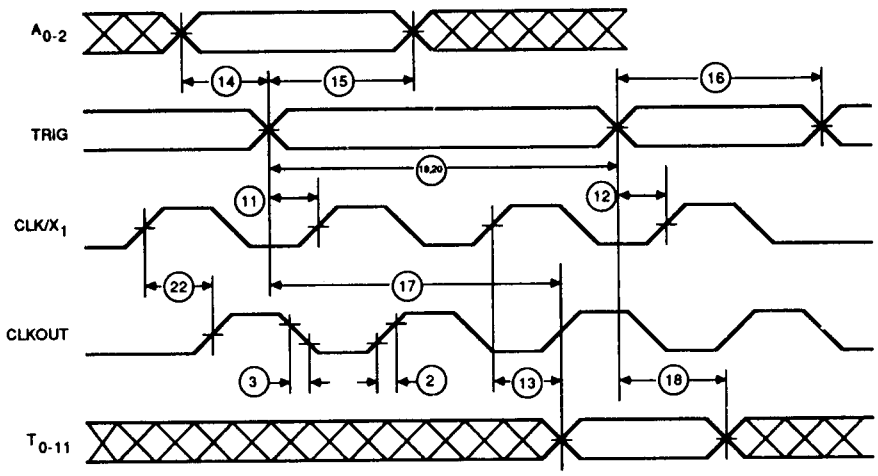
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

SWITCHING WAVEFORMS

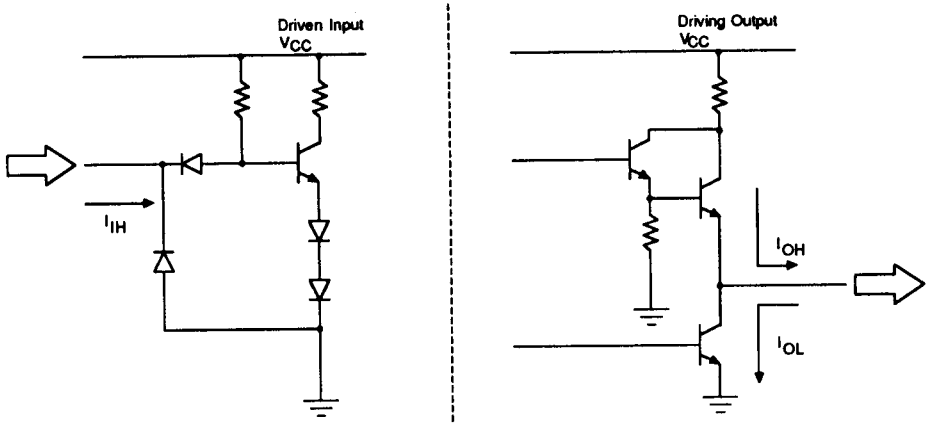


Rise Time/Fall Time /Skews 05280-023A

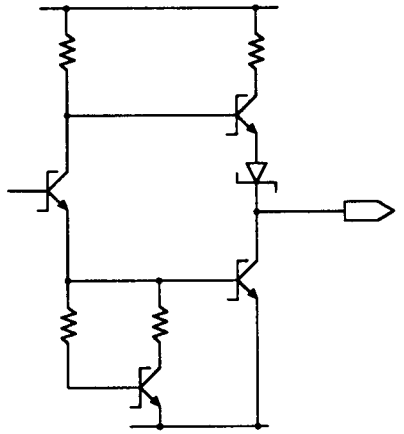


05280-022A

INPUT/OUTPUT CIRCUIT DIAGRAMS



05280-020A



Output Configuration for CLKOUT

05280-021A