

This IC, developed by CMOS technology, is a high-accuracy Hall effect latch IC that operates with high temperature and high-withstand voltage.

The output voltage changes when this IC detects the intensity level of magnetic flux density and a polarity change. Using this IC with a magnet makes it possible to detect the rotation status in various devices.

This IC includes a reverse voltage protection circuit and an output current limit circuit.

High-density mounting is possible by using the small SOT-23-3S package.

Due to its high-accuracy magnetic characteristics, this IC enables the user to reduce the operational variation in the system.

ABLIC Inc. offers a "magnetic simulation service" that provides the ideal combination of magnets and our Hall effect ICs for customer systems. Our magnetic simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.

For more information regarding our magnetic simulation service, contact our sales office.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.

■ Features

- | | |
|---|--|
| • Pole detection: | Bipolar latch |
| • Output logic*1: | V _{OUT} = "L" at S pole detection |
| | V _{OUT} = "H" at S pole detection |
| • Output form: | Nch open-drain output |
| • Magnetic sensitivity*1: | B _{OP} = 0.5 mT typ. |
| | B _{OP} = 1.5 mT typ. |
| | B _{OP} = 2.2 mT typ. |
| | B _{OP} = 3.0 mT typ. |
| • Chopping frequency: | f _C = 500 kHz typ. |
| • Output delay time: | t _D = 8.0 μs typ. |
| • Power supply voltage range: | V _{DD} = 2.7 V to 26.0 V |
| • Built-in regulator | |
| • Built-in reverse voltage protection circuit | |
| • Built-in output current limit circuit | |
| • Operation temperature range: | T _a = -40°C to +150°C |
| • Lead-free (Sn 100%), halogen-free | |
| • AEC-Q100 qualified *2 | |

*1. The option can be selected.

*2. Contact our sales office for details.

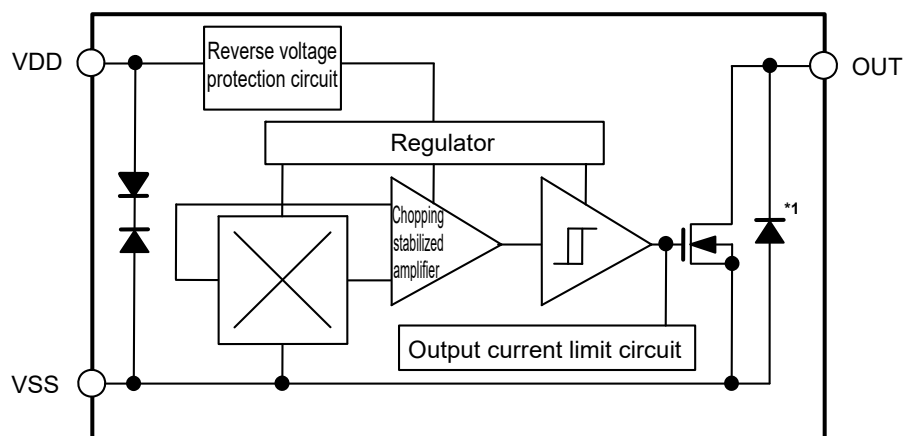
■ Applications

- Automobile equipment
- Home appliance
- DC brushless motor
- Housing equipment
- Industrial equipment

■ Package

- SOT-23-3S

■ Block Diagram



*1. Parasitic diode

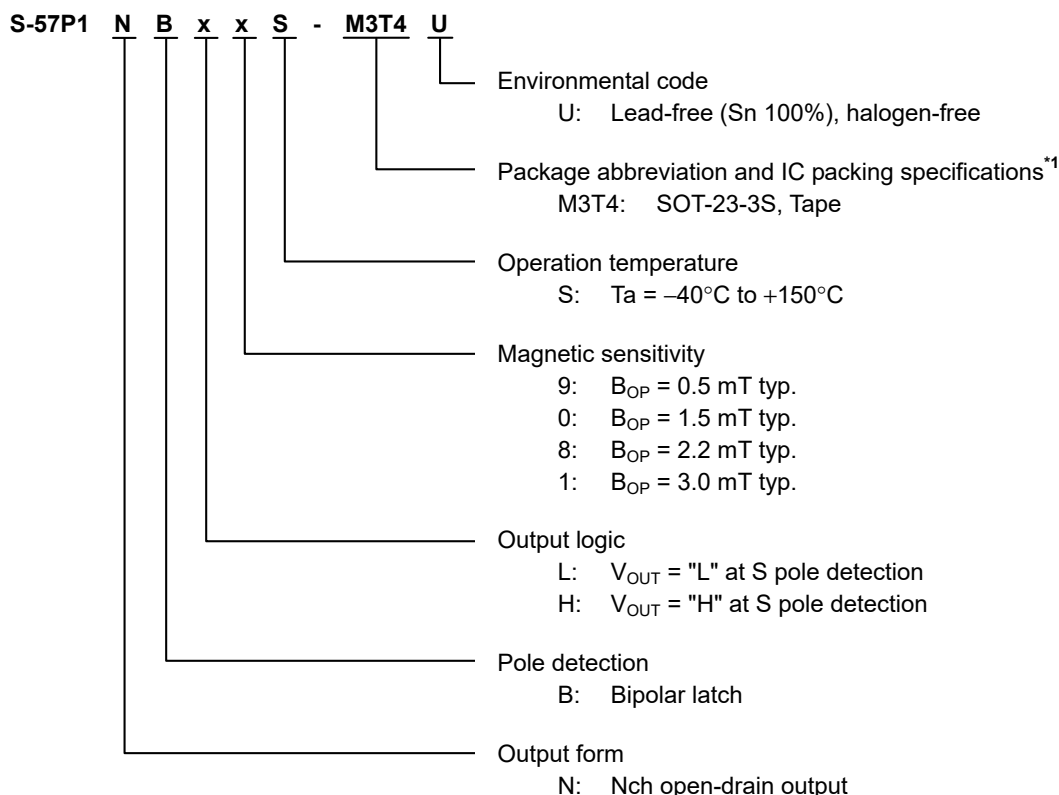
Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 0.
 Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



*1. Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
SOT-23-3S	MP003-D-P-SD	MP003-D-C-SD	MP003-D-R-SD

3. Product name list

Table 2

Product Name	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B _{OP})
S-57P1NBL9S-M3T4U	Nch open-drain output	Bipolar latch	V _{OUT} = "L" at S pole detection	0.5 mT typ.
S-57P1NBL0S-M3T4U	Nch open-drain output	Bipolar latch	V _{OUT} = "L" at S pole detection	1.5 mT typ.
S-57P1NBL8S-M3T4U	Nch open-drain output	Bipolar latch	V _{OUT} = "L" at S pole detection	2.2 mT typ.
S-57P1NBL1S-M3T4U	Nch open-drain output	Bipolar latch	V _{OUT} = "L" at S pole detection	3.0 mT typ.
S-57P1NBH9S-M3T4U	Nch open-drain output	Bipolar latch	V _{OUT} = "H" at S pole detection	0.5 mT typ.
S-57P1NBH0S-M3T4U	Nch open-drain output	Bipolar latch	V _{OUT} = "H" at S pole detection	1.5 mT typ.
S-57P1NBH1S-M3T4U	Nch open-drain output	Bipolar latch	V _{OUT} = "H" at S pole detection	3.0 mT typ.

Remark Please contact our sales office for products other than the above.

■ Pin Configuration

1. SOT-23-3S

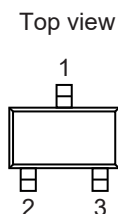


Figure 2

Table 3

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Power supply pin
3	OUT	Output pin

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	VDD	VSS – 28.0 to VSS + 28.0	V
Output current	IOUT	20	mA
Output voltage	VOUT	VSS – 0.3 to VSS + 28.0	V
Junction temperature	Tj	–40 to +170	°C
Operation ambient temperature	Topr	–40 to +150	°C
Storage temperature	Tstg	–40 to +170	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Table 5							
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{ja}	SOT-23-3S	Board A	–	200	–	°C/W
			Board B	–	165	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ Power Dissipation" and "Test Board" for details.

■ Electrical Characteristics

Table 6

(Ta = +25°C, V_{DD} = 12.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V _{DD}	—	2.7	12.0	26.0	V	—
Current consumption	I _{DD}	Average value	—	3.0	4.0	mA	1
Current consumption during reverse connection	I _{DDREV}	V _{DD} = -26.0 V	-0.1	—	—	mA	1
Output voltage	V _{OUT}	I _{OUT} = 10 mA	—	—	0.4	V	2
Leakage current	I _{LEAK}	Output transistor Nch, V _{OUT} = 26.0 V	—	—	1	μA	3
Output limit current	I _{OM}	V _{OUT} = 12.0 V	22	—	70	mA	3
Output delay time	t _D	—	—	8.0	—	μs	—
Chopping frequency	f _C	—	—	500	—	kHz	—
Start up time	t _{PON}	—	—	20	—	μs	4
Output rise time	t _R	C = 20 pF, R = 820 Ω	—	—	2.0	μs	5
Output fall time	t _F	C = 20 pF, R = 820 Ω	—	—	2.0	μs	5

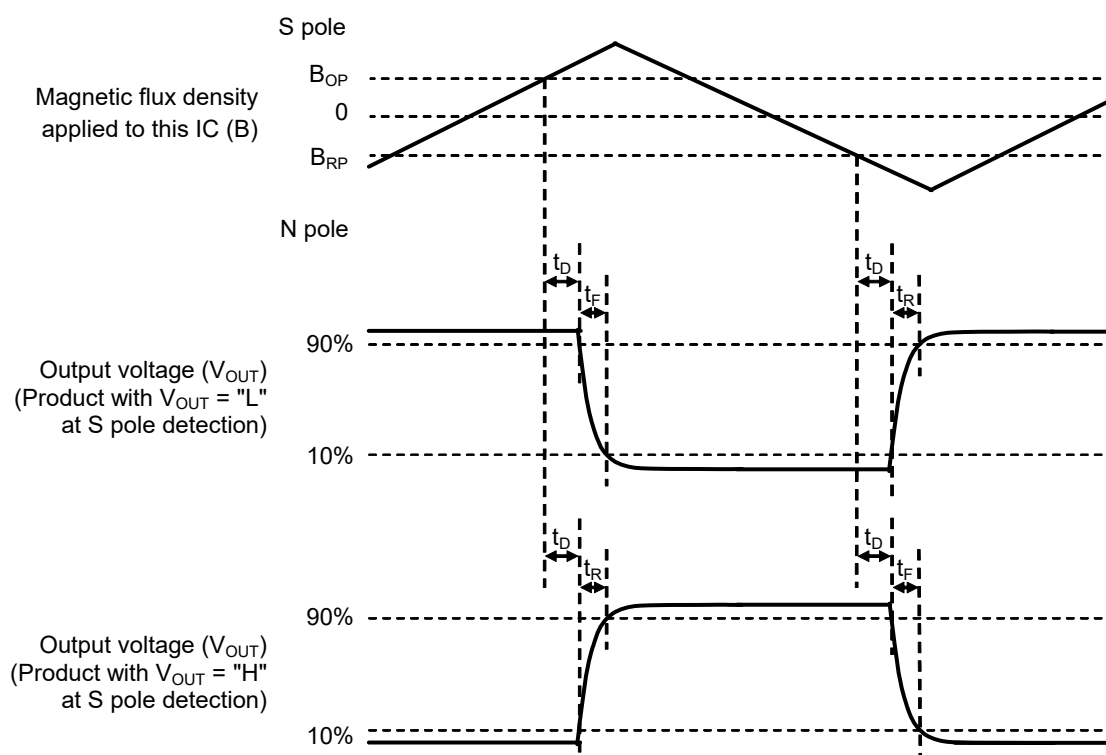


Figure 3 Operation Timing

■ Magnetic Characteristics

1. Product with $B_{OP} = 0.5 \text{ mT typ.}$

Table 7

($T_a = +25^\circ\text{C}$, $V_{DD} = 12.0 \text{ V}$, $V_{SS} = 0 \text{ V}$ unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point* ¹	S pole	B _{OP}	–	–0.5	0.5	1.5	mT	4
Release point* ²	N pole	B _{RP}	–	–1.5	–0.5	0.5	mT	4
Hysteresis width* ³		B _{HYS}	B _{HYS} = B _{OP} – B _{RP}	–	1.0	–	mT	4

2. Product with $B_{OP} = 1.5 \text{ mT typ.}$

Table 8

($T_a = +25^\circ\text{C}$, $V_{DD} = 12.0 \text{ V}$, $V_{SS} = 0 \text{ V}$ unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point* ¹	S pole	B _{OP}	–	0.5	1.5	2.5	mT	4
Release point* ²	N pole	B _{RP}	–	–2.5	–1.5	–0.5	mT	4
Hysteresis width* ³		B _{HYS}	B _{HYS} = B _{OP} – B _{RP}	–	3.0	–	mT	4

3. Product with $B_{OP} = 2.2 \text{ mT typ.}$

Table 9

($T_a = +25^\circ\text{C}$, $V_{DD} = 12.0 \text{ V}$, $V_{SS} = 0 \text{ V}$ unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point* ¹	S pole	B _{OP}	–	1.2	2.2	3.2	mT	4
Release point* ²	N pole	B _{RP}	–	–3.2	–2.2	–1.2	mT	4
Hysteresis width* ³		B _{HYS}	B _{HYS} = B _{OP} – B _{RP}	–	4.4	–	mT	4

4. Product with $B_{OP} = 3.0 \text{ mT typ.}$

Table 10

($T_a = +25^\circ\text{C}$, $V_{DD} = 12.0 \text{ V}$, $V_{SS} = 0 \text{ V}$ unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point* ¹	S pole	B _{OP}	–	2.0	3.0	4.0	mT	4
Release point* ²	N pole	B _{RP}	–	–4.0	–3.0	–2.0	mT	4
Hysteresis width* ³		B _{HYS}	B _{HYS} = B _{OP} – B _{RP}	–	6.0	–	mT	4

***1. B_{OP} : Operation point**

B_{OP} is the value of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (S pole) is increased (by moving the magnet closer).

V_{OUT} retains the status until a magnetic flux density of the N pole higher than B_{RP} is applied.

***2. B_{RP} : Release point**

B_{RP} is the value of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole) is increased (by moving the magnet closer).

V_{OUT} retains the status until a magnetic flux density of the S pole higher than B_{OP} is applied.

***3. B_{HYS} : Hysteresis width**

B_{HYS} is the difference of magnetic flux density between B_{OP} and B_{RP} .

Remark The unit of magnetic density mT can be converted by using the formula $1 \text{ mT} = 10 \text{ Gauss}$.

■ Test Circuits

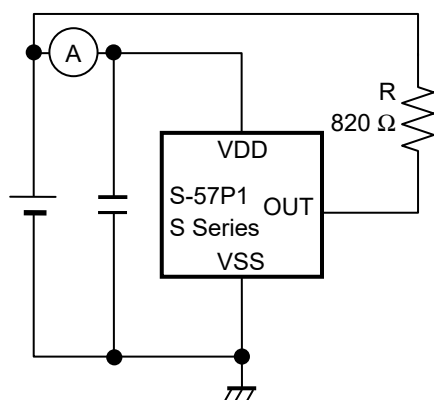


Figure 4 Test Circuit 1

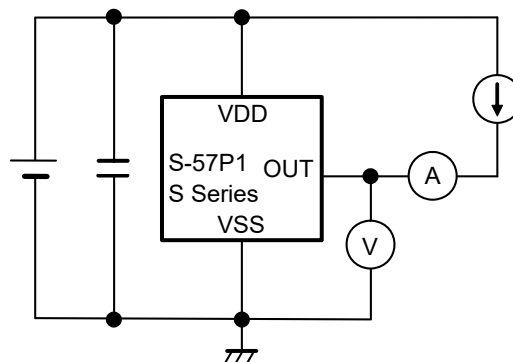


Figure 5 Test Circuit 2

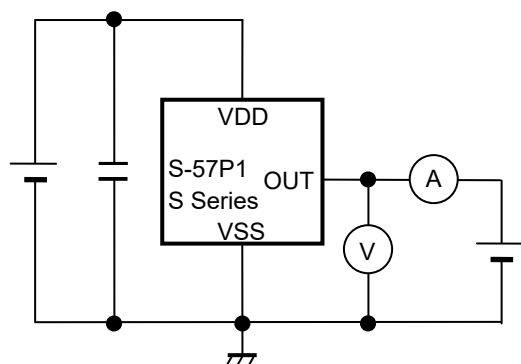


Figure 6 Test Circuit 3

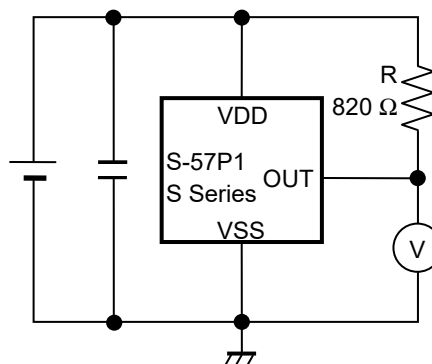


Figure 7 Test Circuit 4

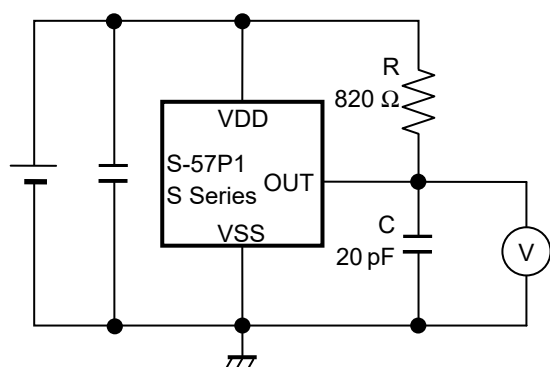


Figure 8 Test Circuit 5

■ Standard Circuit

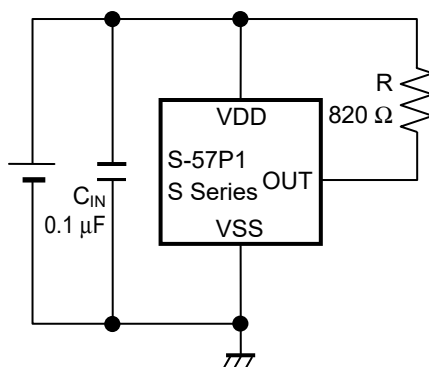


Figure 9

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Operation

1. Direction of applied magnetic flux

This IC detects the magnetic flux density which is vertical to the marking surface.

Figure 10 shows the direction in which magnetic flux is being applied.

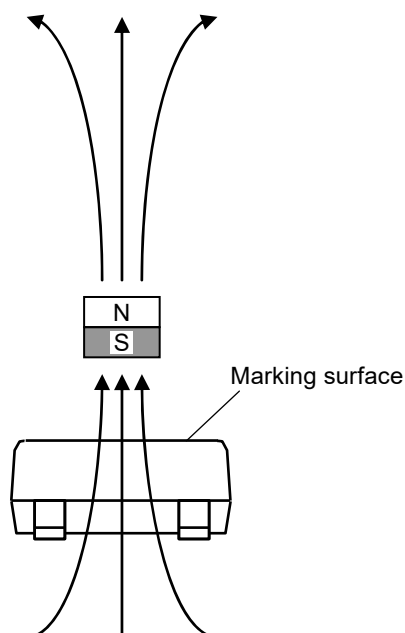


Figure 10

2. Position of Hall sensor

Figure 11 shows the position of Hall sensor.

The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.

The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

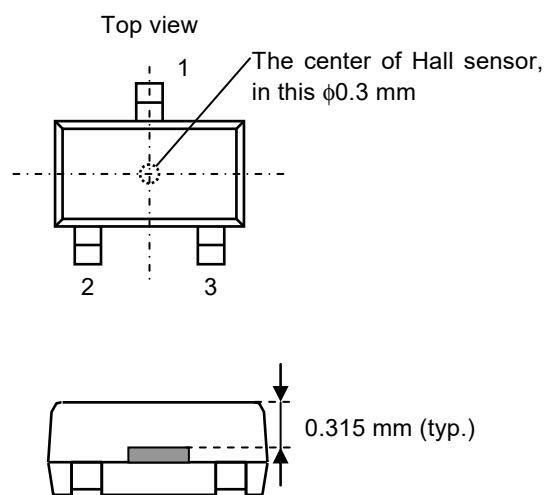


Figure 11

3. Basic operation

This IC changes the output voltage (V_{OUT}) according to the level of the magnetic flux density (N pole or S pole) and a polarity change applied by a magnet.

3.1 Product with $V_{OUT} = "L"$ at S pole detection

When the magnetic flux density of the S pole perpendicular to the marking surface exceeds the operation point (B_{OP}) after the S pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "H" to "L". When the N pole of a magnet is moved closer to the marking surface of this IC and the magnetic flux density of the N pole is higher than the release point (B_{RP}), V_{OUT} changes from "L" to "H". In case of $B_{RP} < B < B_{OP}$, V_{OUT} retains the status. **Figure 12** shows the relationship between the magnetic flux density and V_{OUT} .

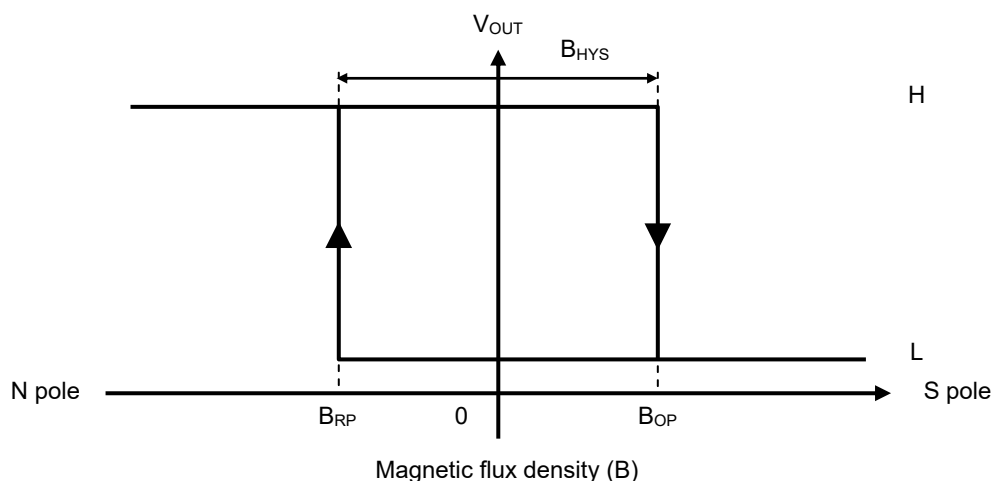


Figure 12

3.2 Product with $V_{OUT} = "H"$ at S pole detection

When the magnetic flux density of the S pole perpendicular to the marking surface exceeds B_{OP} after the S pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "L" to "H". When the N pole of a magnet is moved closer to the marking surface of this IC and the magnetic flux density of the N pole is higher than B_{RP} , V_{OUT} changes from "H" to "L". In case of $B_{RP} < B < B_{OP}$, V_{OUT} retains the status.

Figure 13 shows the relationship between the magnetic flux density and V_{OUT} .

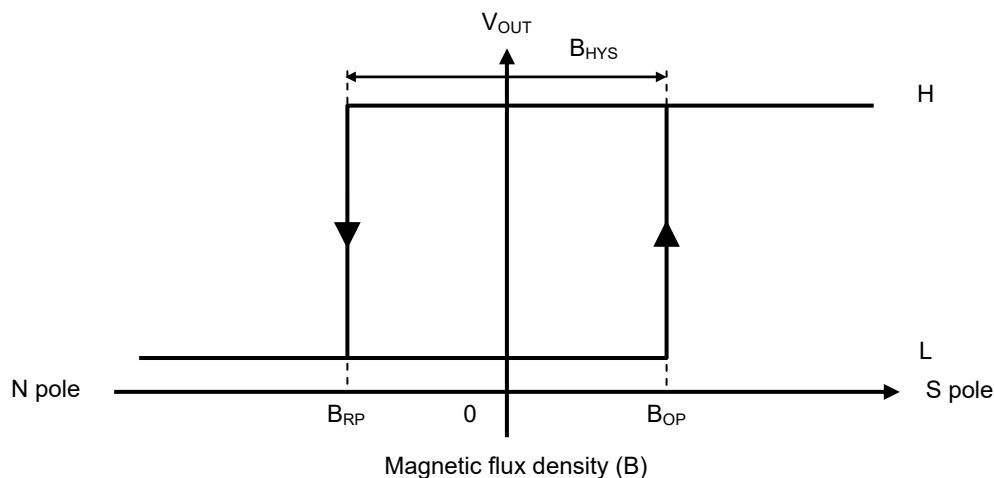


Figure 13

4. Timing chart

Figure 14 shows the timing chart at power-on for product with $V_{OUT} = "L"$ at S pole detection.
 The initial output voltage at rising of power supply voltage (V_{DD}) is "H".
 In case of $B > B_{OP}$ at the time when the start up time (t_{PON}) is passed after rising of V_{DD} , this IC outputs "L".
 In case of $B < B_{OP}$ at the time when t_{PON} is passed after rising of V_{DD} , this IC maintains "H".

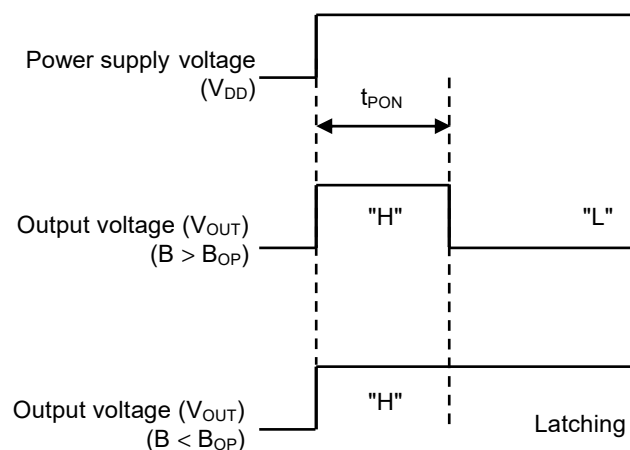


Figure 14

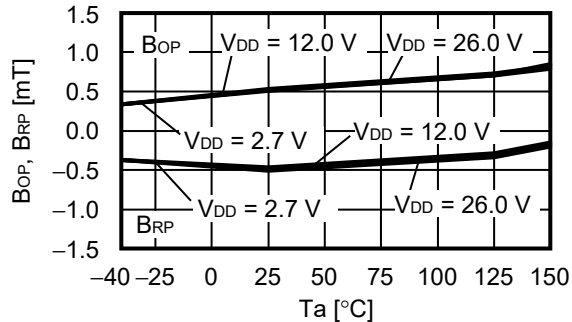
■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes. When the IC is used under the environment where the power supply voltage rapidly changes, it is recommended to judge the output voltage of the IC by reading it multiple times.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Although this IC has a built-in output current limit circuit, it may suffer physical damage such as product deterioration under the environment where the absolute maximum ratings are exceeded.
- Although this IC has a built-in reverse voltage protection circuit, it may suffer physical damage such as product deterioration under the environment where the absolute maximum ratings are exceeded.
- The application conditions for the power supply voltage, the pull-up voltage, and the pull-up resistor should not exceed the power dissipation.
- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

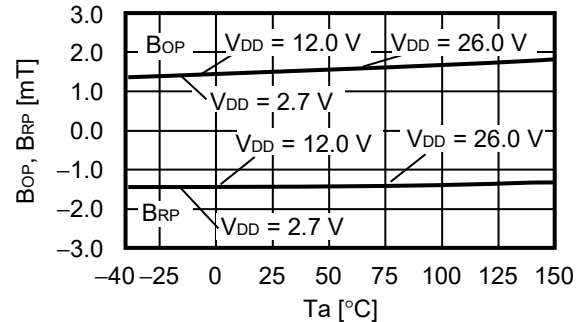
■ Characteristics (Typical Data)

1. Operation point, release point (B_{OP} , B_{RP}) vs. Temperature (T_a)

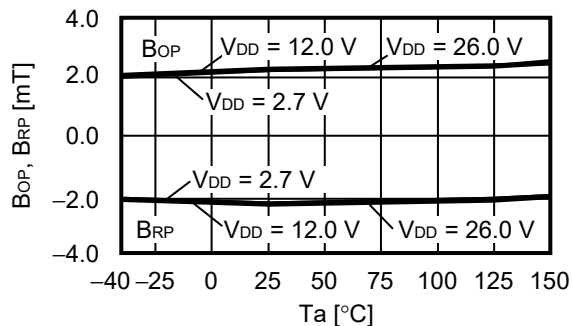
1.1 S-57P1NBx9S



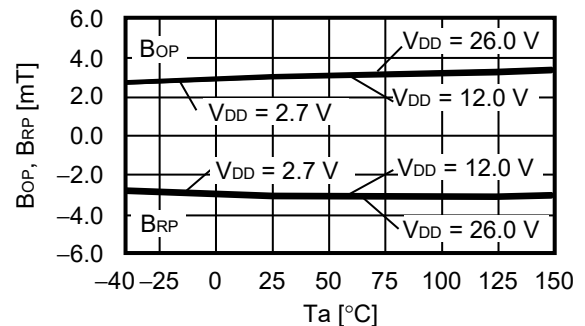
1.2 S-57P1NBx0S



1.3 S-57P1NBx8S

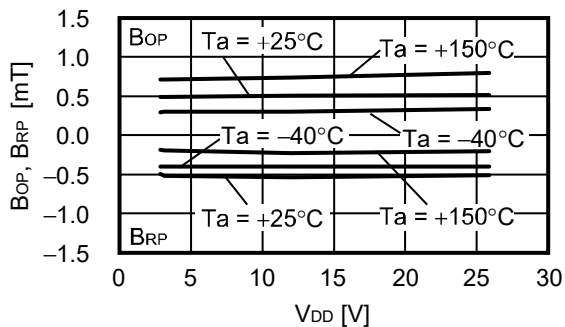


1.4 S-57P1NBx1S

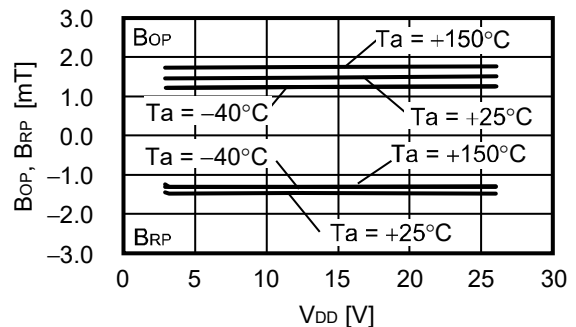


2. Operation point, release point (B_{OP} , B_{RP}) vs. Power supply voltage (V_{DD})

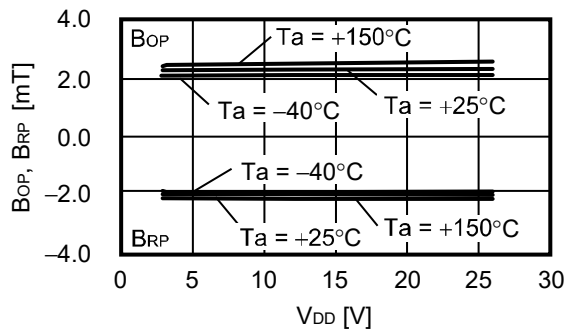
2.1 S-57P1NBx9S



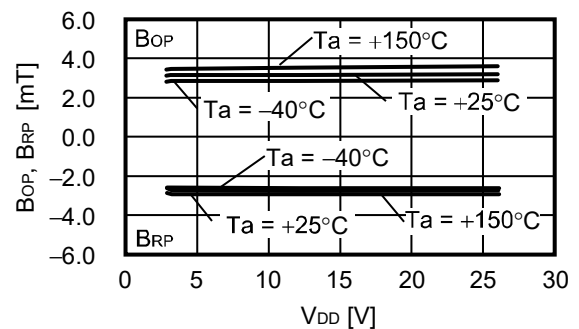
2.2 S-57P1NBx0S



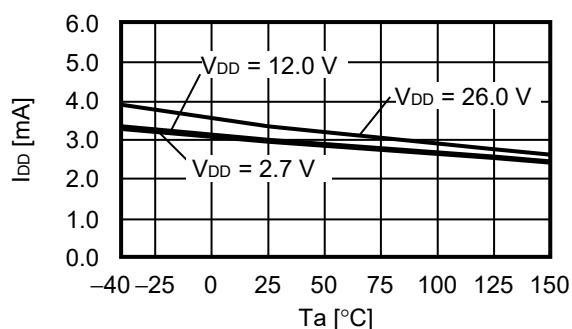
2.3 S-57P1NBx8S



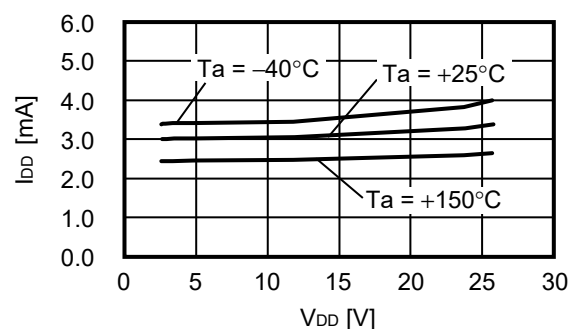
2.4 S-57P1NBx1S



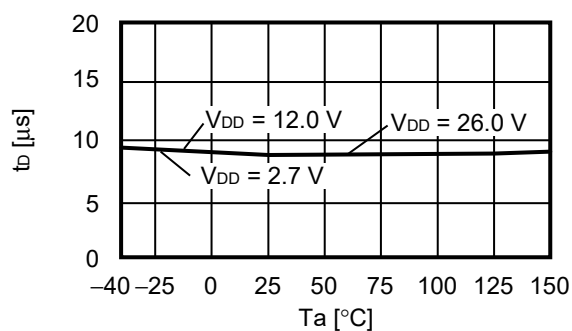
3. Current consumption (I_{DD}) vs. Temperature (T_a)



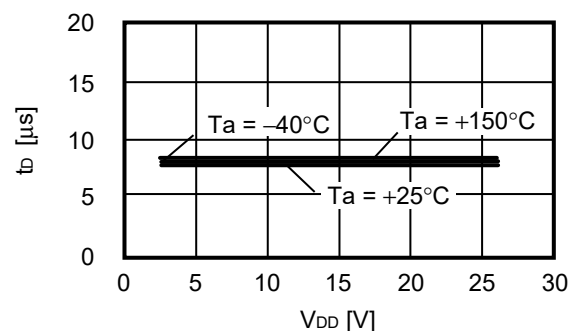
4. Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



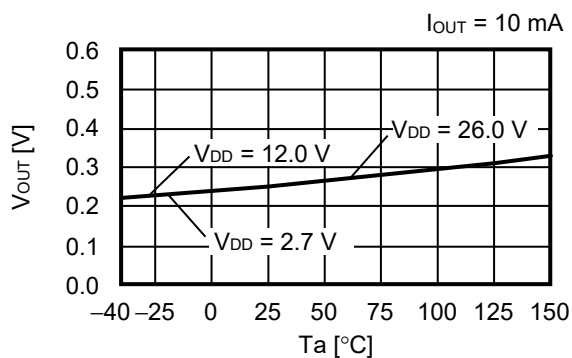
5. Output delay time (t_b) vs. Temperature (T_a)



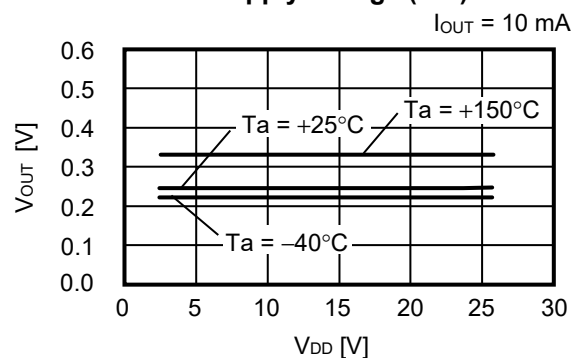
6. Output delay time (t_b) vs. Power supply voltage (V_{DD})



7. Output voltage (V_{OUT}) vs. Temperature (T_a)

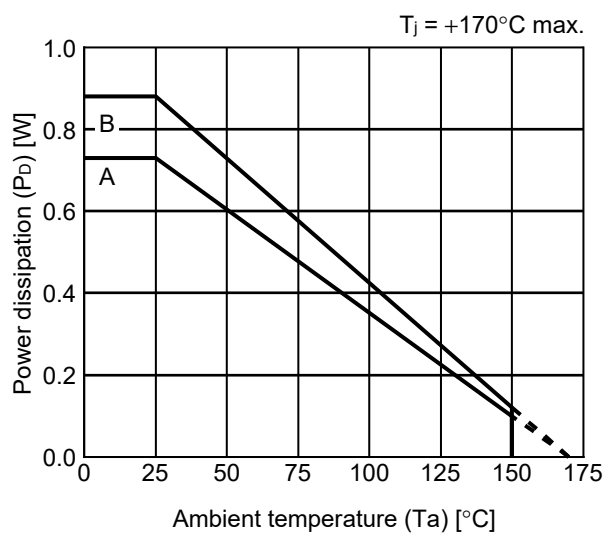


8. Output voltage (V_{OUT}) vs. Power supply voltage (V_{DD})



■ Power Dissipation

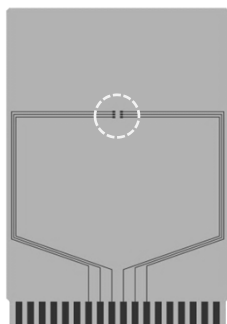
SOT-23-3S



Board	Power Dissipation (P_D)
A	0.73 W
B	0.88 W
C	—
D	—
E	—

SOT-23-3/3S/5/6 Test Board

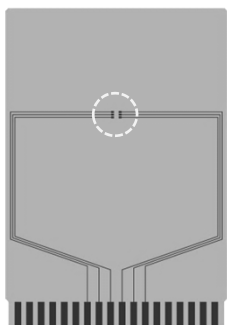
(1) Board A



 IC Mount Area

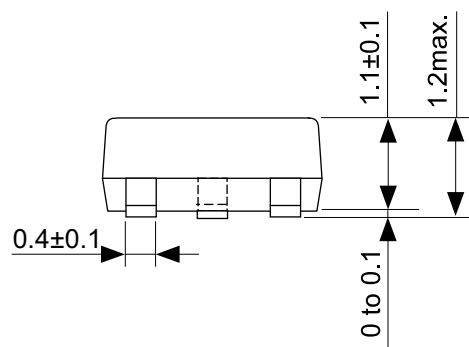
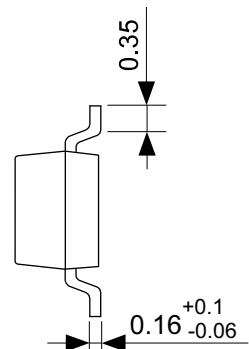
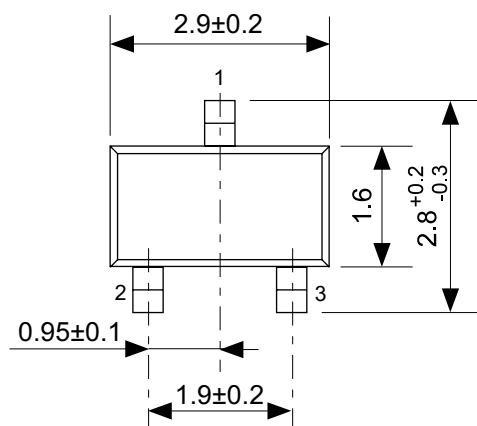
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B




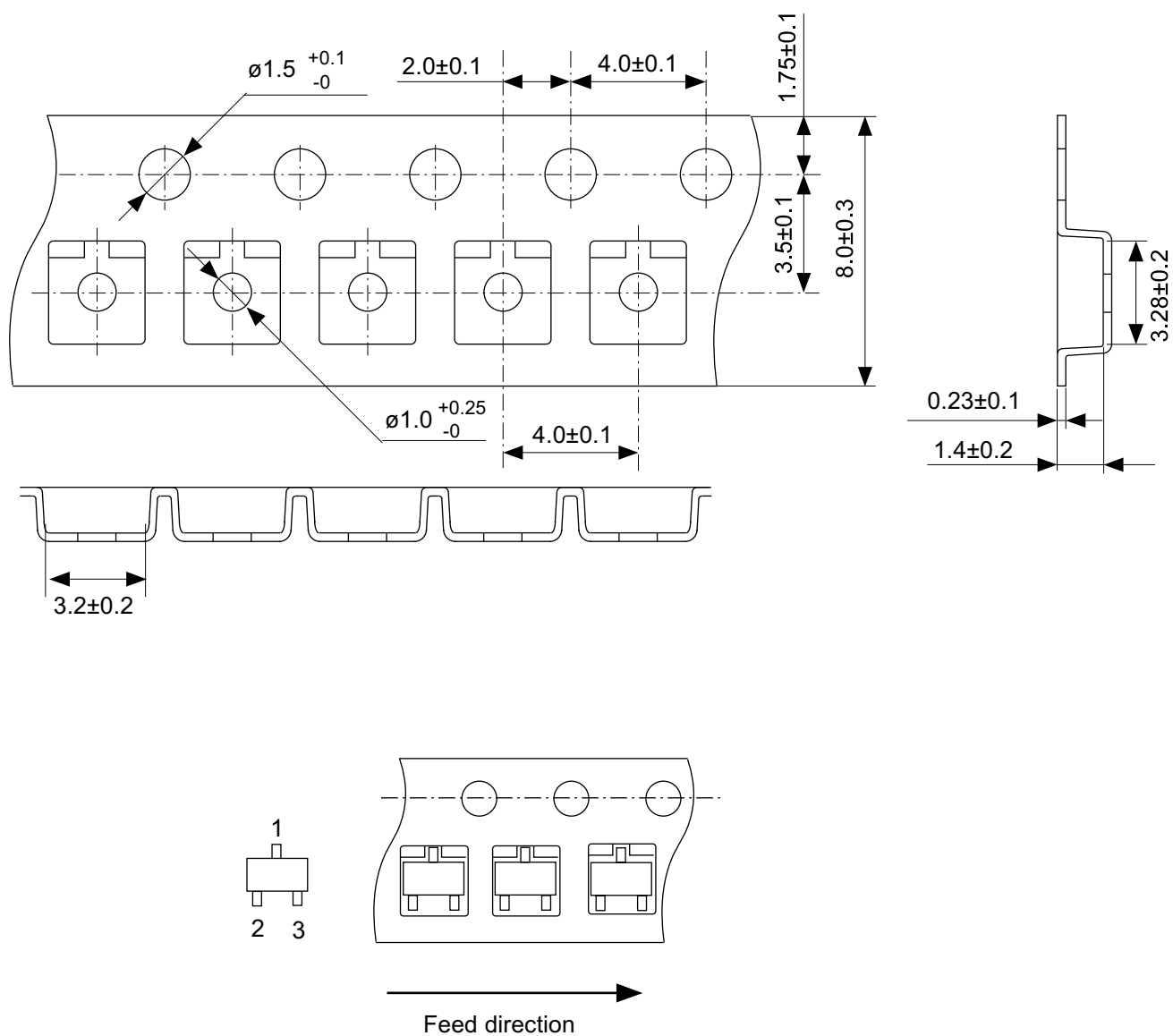
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SOT23x-A-Board-SD-2.0



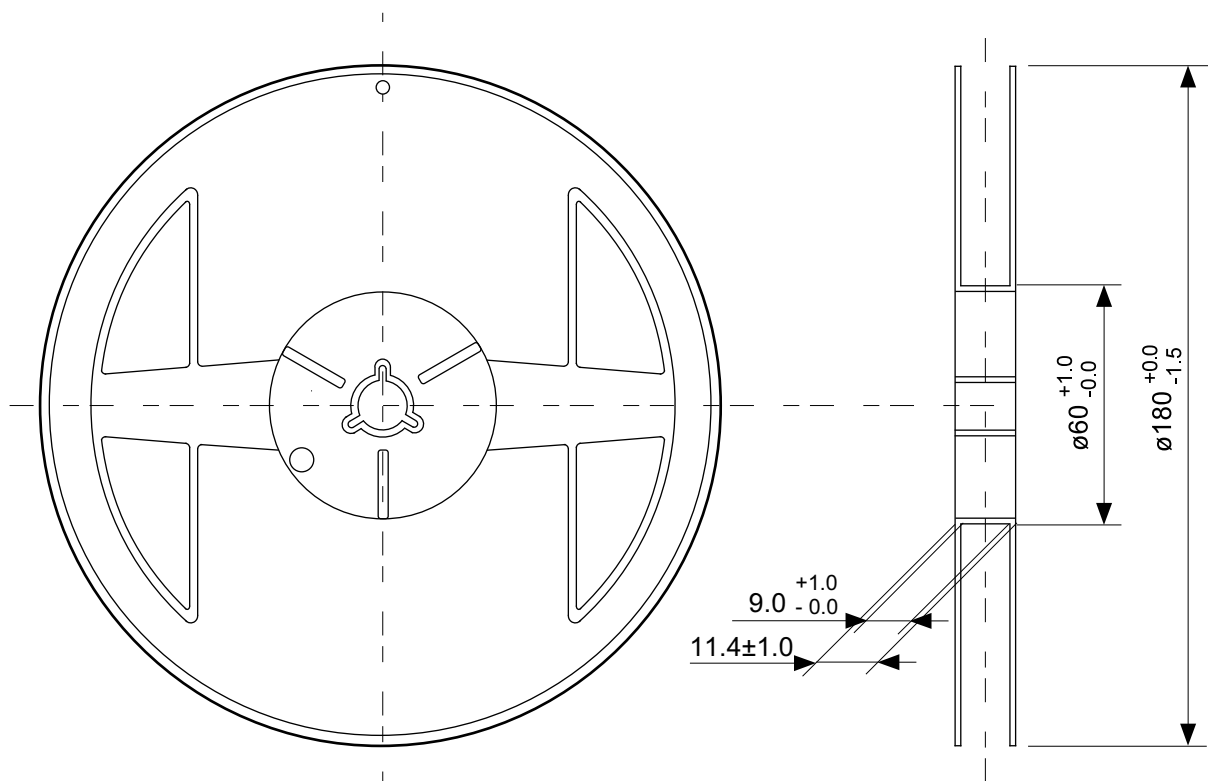
No. MP003-D-P-SD-1.1

TITLE	SOT233S-A-PKG Dimensions
No.	MP003-D-P-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	

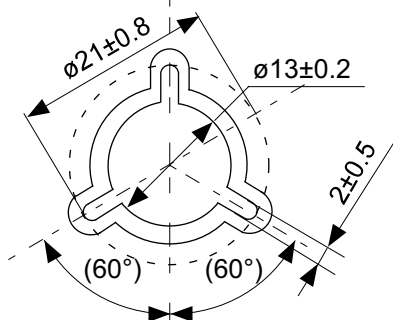


No. MP003-D-C-SD-1.0

TITLE	SOT23S-A-Carrier Tape
No.	MP003-D-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. MP003-D-R-SD-1.0

TITLE	SOT233S-A-Reel		
No.	MP003-D-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07